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Transcript of Joseph C. McAlexander, III

Date: September 18, 2025

Case: Monolithic Power Systems, Inc. -v- Reed Semiconductor Corp., et al.

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1	IN THE UNITED STATES DISTRICT COURT	
2	FOR THE DISTRICT OF DELAWARE	
3	MONOLITHIC POWER)	
	SYSTEMS, INC.,)	
	)	
4	Plaintiff,)	
	Counterclaim-Defendant,)	
5	)	C.A. No.
	v.)	1:23-cv-01155-
6	)	JFM
	REED SEMICONDUCTOR)	
7	CORP,)	
	)	
8	Defendant,)	
	Counterclaim-Plaintiff)	
9	)	

	MONOLITHIC POWER)	
10	SYSTEMS, INC.,)	
	)	
11	Plaintiff,)	C.A. No.
	Counterclaim-Defendant,)	1:24-cv-00165-
12	)	JFM
	V.)	
13	REED SEMICONDUCTOR)	
	CORP,)	
14	)	
	Defendant,)	
15	Counterclaim-Plaintiff)	C.A. No.
	)	1:24-cv-00166-
16	-----	
	MONOLITHIC POWER)	JFM
	SYSTEMS, INC.,)	
17	)	
	Plaintiff,)	
18	)	Pages 1 - 241
	V.)	
19	)	
	(Caption Continued))	

THIS TRANSCRIPT IS DESIGNATED

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REMOTE VIDEOTAPED DEPOSITION OF

JOSEPH C. McALEXANDER, III

THURSDAY, SEPTEMBER 18, 2025

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1 (Caption Continued.)

2
3 NENGDA MICROELECTRONICS)
4 (SHENZHEN) CO., LTD. and)
5 NENGDA SEMICONDUCTOR)
6 TECHNOLOGY (SHENZHEN))
7 CO., LTD.)
8)
9 Defendants.)

10
11 Reported By:

12 BRENDA R. COUNTZ, RPR-CRR

13 CSR NO. 12563

14 Job No. 600660

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21 Remote Videotaped Deposition of
22 JOSEPH C. McALEXANDER, III Taken Via Zoom or
23 teleconference in Los Angeles, California, on
24 Thursday, September 18, 2025, Before Brenda R.
25 Countz, CSR No. 12563.

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JOSEPH C. McALEXANDER, III		
	Mr. Devkar	9
	Mr. Patariu	224

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(Confidential Exhibits 7 and 10 withdrawn and retained by
by counsel. Exhibit 11 was omitted.)

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1	So it's not the same, not for an AC.	16:08:30
2	MR. DEVKAR: Okay, let's take a break.	16:08:35
3	THE VIDEOGRAPHER: Okay, we are going off	16:08:38
4	the record. The time is 4:08 p.m.	16:08:40
5	(Break taken.)	16:22:39
6	THE VIDEOGRAPHER: We are back on the	16:29:45
7	record. The time is 4:30 p.m.	16:30:30
8	BY MR. DEVKAR:	16:30:37
9	Q. I'd like to turn to Exhibit 1, your expert	16:30:38
10	report, at paragraph 204, please.	16:30:43
11	A. (Perusing.)	16:30:51
12	Q. Let me know when you have that open,	16:30:57
13	please.	16:31:02
14	A. Okay, I'm there.	16:32:01
15	Q. In paragraph 204 you identify the control	16:32:03
16	signal in blue in your annotated figure and as	16:32:09
17	"PWMHS (PWM)", is that correct?	16:32:21
18	A. In green, yes.	16:32:45
19	Q. Can you please turn to page 117 of your	16:34:35
20	report?	16:34:39
21	A. (Perusing.)	16:35:02
22	Q. On page 117 of your report you identify	16:35:03
23	the control signal as the output of the flip-flop	16:35:07
24	labeled PWMHS, correct?	16:35:11
25	A. I have identified that in paragraph 254,	16:35:34

1	yes.	16:35:45
2	Q. And you point to the flip-flop with your	16:35:58
3	orange arrow in the figure, correct?	16:36:06
4	A. Correct.	16:36:17
5	Q. The output of the flip-flop is not PWMHS,	16:36:23
6	correct?	16:36:30
7	MR. PATARIU: Object to form.	16:36:32
8	THE WITNESS: If you are asking about the	16:37:51
9	actual physical output of the flip-flop, it does	16:37:52
10	not have a name associated with it as far as the	16:37:58
11	output node of the flip-flop but the signal that's	16:38:04
12	generated is PWMHS.	16:38:10
13	BY MR. DEVKAR:	09:06:04
14	Q. PWMHS is the output of the flip-flop NOR,	16:38:18
15	that's N-O-R, with several other signals and then	16:38:26
16	inverted before generating the PWMHS signal,	16:38:30
17	correct?	16:38:35
18	MR. PATARIU: Object to form.	16:38:38
19	THE WITNESS: As far as from the physical	16:38:39
20	output node of the flip-flop, there are other gates	16:38:41
21	such as the NOR and invert.	16:38:47
22	But again, in this claim language it	16:38:51
23	doesn't say the -- it says that the flip-flop is	16:38:55
24	coupled to the AND gate to receive the output	16:39:04
25	signal and then it generates the control signal.	16:39:09

1 And it doesn't mean that it has to be literally at 16:39:13
2 that output pin. 16:39:16

3 But the PWMHS is generated by that 16:39:18
4 flip-flop. And yes, there is an inverter in 16:39:23
5 between that and that's why the label in my report, 16:39:28
6 the PWMHS bar as well as the PWMHS, that's a 16:39:33
7 control signal that's generated by the flip-flop. 16:39:40

8 BY MR. DEVKAR: 16:39:57

9 Q. Is the signal that's generated by the 16:39:57
10 flip-flop the same signal that exists at the output 16:40:00
11 of the inverter? 16:40:26

12 MR. PATARIU: Object to form. 16:40:40

13 THE WITNESS: The content of the PWMHS 16:40:41
14 signal is a double inversion to the NOR in the 16:40:44
15 inverter so it is literally a mirror of the signal 16:40:48
16 that is on the input-output node of that flip-flop. 16:40:52

17 So whatever happens on the output of the 16:40:59
18 flip-flop through that NOR gate, the output of the 16:41:02
19 NOR gate reflects that and the inverter reflects 16:41:05
20 the opposite of that. So it's literally a mirror 16:41:08
21 of that output for the flip-flop. 16:41:13

22 So yes, I consider that to be the control 16:41:16
23 signal that's generated by the flip-flop. 16:41:21

24 BY MR. DEVKAR: 09:06:04

25 Q. I see. So the signal can remain the same 16:41:24

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1	signal if it's changed so long as it's changed back	16:41:28
2	by other circuitry before a later point that you	16:41:39
3	are considering whether the signal is the same or	16:41:47
4	not, correct?	16:41:51
5	MR. PATARIU: Object to form.	16:41:53
6	THE WITNESS: Well, I don't agree with	16:41:54
7	your language.	16:41:57
8	When you develop signals for propagation,	16:42:00
9	the signal in your design, the signal that is	16:42:05
10	output, the output of the flip-flop itself is	16:42:14
11	designed specifically with small transistors to be	16:42:18
12	a very small signal output so that you have to	16:42:21
13	buffer it, or whatever you want to call it, because	16:42:27
14	what the inverter does is it creates additional	16:42:31
15	drive capability so you can drive the load and not	16:42:34
16	lose the speed.	16:42:37
17	If you took the signal out of the gate of	16:42:43
18	the flip-flop and tried to drive a long wire to a	16:42:44
19	lot of loads, it would not work. The load would	16:42:47
20	pull it down. So it is that signal. It's just a	16:42:49
21	signal that has been generated and empowered to	16:42:52
22	drive the load that it would be connected to. And	16:43:02
23	again the word is "generate."	16:43:06
24	BY MR. DEVKAR:	09:06:04
25	Q. The output of the flip-flop is connected	16:43:10

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1	to a gate of a transistor in the NOR gate, correct?	16:43:13
2	MR. PATARIU: Object to form.	16:43:19
3	THE WITNESS: Yeah, it's the literal	16:43:26
4	output node of the flip-flop is connected to a NOR	16:43:27
5	gate which is shown there in the middle, followed	16:43:31
6	by an inverter and the output of that circuit is	16:43:34
7	PWMHS.	16:43:41
8	BY MR. DEVKAR:	09:06:04
9	Q. So here a signal that goes to the gate of	16:43:49
10	a transistor in a logic gate passes through to the	16:43:52
11	output of the logic gate?	16:44:10
12	MR. PATARIU: Object to form.	16:44:14
13	THE WITNESS: Again, you are trying to	16:44:15
14	equate this based on what we talked about earlier.	16:44:17
15	Here we're talking about the fact that it	16:44:22
16	generates the control signal and it's that	16:44:25
17	generated control signal that is used downstream by	16:44:30
18	other circuits.	16:44:34
19	BY MR. DEVKAR:	09:06:04
20	Q. And the control signal that's generated is	16:44:40
21	not changed by any of the intervening logic, in	16:44:43
22	your opinion; is that correct?	16:44:48
23	MR. PATARIU: Object to form.	16:44:50
24	THE WITNESS: It is not because when you	16:44:56
25	generate a one on the output, it immediately flips	16:44:57

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1	the NOR gate to a zero on the output.	16:45:00
2	So yes, that signal, whatever the	16:45:04
3	flip-flop defines, that is what the PWMHS signal is	16:45:08
4	going to reflect.	16:45:14
5	BY MR. DEVKAR:	09:06:04
6	Q. I'm not sure I followed. Did you say that	16:45:16
7	if you generate a one --	16:45:19
8	A. If you generate a one on an input of that	16:45:23
9	NOR gate, it automatically flips to a zero on that	16:45:26
10	output.	16:45:31
11	Q. So the one and the zero reflect the same	16:45:32
12	signal, in your opinion?	16:45:35
13	A. Yes.	16:45:36
14	Q. But if the one remained a one at the	16:45:46
15	output, it would not be the same signal?	16:45:49
16	A. Well, again, you are trying to relate this	16:45:51
17	to an output of the flip-flop. The claim says the	16:45:53
18	flip-flop has a set terminal, reset terminal -- the	16:45:57
19	flip-flop has a set terminal, a reset terminal and	16:46:10
20	an output terminal. Those are the three physical	16:46:14
21	terminals.	16:46:17
22	And the reset terminal is coupled to the	16:46:19
23	on-time generator to receive the on-time signal.	16:46:22
24	It doesn't mean it receives the on-time signal	16:46:25
25	directly. It's coupled to it. It's coupled to	16:46:28

1 receive. And the set terminal is coupled to
2 receive.

3 But then it says based upon those two
4 signals, the flip-flop generates the control
5 signal. And I'm saying that signal, PWMHS, is what
6 is generated.

7 Q. When the signal that's generated passes
8 through the NOR gate, is it changed?

9 MR. PATARIU: Object to form.

10 THE WITNESS: Well, again, you're still
11 trying to go back to the other language which is
12 written differently. This language, the two inputs
13 are coupled to receive signals and that flip-flop
14 does have two terminal inputs and an output.

15 But the claim language does not require
16 that, in quotes, "The control signal be the signal
17 that's on the output pin, the output node."

18 It just says that the flip-flop has three
19 terminals. But when it comes to the generation, it
20 generates the control signal. And I'm saying the
21 signal that it generates is the one that's over the
22 PWMHS. That is the signal that's generated.

23 BY MR. DEVKAR:

24 Q. The signal that is generated needs to be
25 the same signal that is received by the power stage

16:46:32

16:46:35

16:46:37

16:46:40

16:46:45

16:46:52

16:47:03

16:47:10

16:47:23

16:47:24

16:47:27

16:47:30

16:47:34

16:47:39

16:47:44

16:47:48

16:47:52

16:47:57

16:47:59

16:48:03

16:48:06

16:48:09

16:48:14

16:48:14

16:48:16

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1	in element 18-S, correct?	16:48:28
2	MR. PATARIU: Object to form.	16:48:32
3	THE WITNESS: And I'm indicating this PWM	16:48:33
4	signal is that which is received.	16:48:36
5	BY MR. DEVKAR:	09:06:04
6	Q. And so what I'm trying to get at is as the	16:48:38
7	signal that you say is generated by the flip-flop	16:48:44
8	passes through the intervening logic, I'm trying to	16:48:48
9	get your position as to whether it's changed in	16:48:52
10	that intervening logic?	16:48:55
11	MR. PATARIU: Object to form.	16:48:57
12	THE WITNESS: What I'm saying is you are	16:48:58
13	imposing intervening logic. There is nothing that	16:49:00
14	says in the claim that the signal has to be the one	16:49:03
15	that I've defined on the output pin of the	16:49:06
16	flip-flop.	16:49:09
17	It's the flip-flop that generates the	16:49:10
18	signal. And that signal that it generates is	16:49:11
19	PWMHS. I'm not talking about intervening logic or	16:49:16
20	anything. That's the signal that's generated.	16:49:18
21	BY MR. DEVKAR:	09:06:04
22	Q. And does that signal need to be received	16:49:23
23	by the power stage?	16:49:27
24	A. The power stage -- the language is not	16:49:49
25	receiving the control signal. The power stage is	16:49:54

1	coupled to receive the control signal.	16:49:57
2	Q. Okay.	16:50:06
3	A. Coupled means there could be and certainly	16:50:06
4	is allowed to be some intervening circuitry, if you	16:50:10
5	will, as an interface is a coupling aspect.	16:50:15
6	But the output -- it is physically coupled	16:50:21
7	to the output of the flip-flop and the power stage	16:50:28
8	is also coupled to receive the control signal.	16:50:31
9	And yes, the PWMHS signal is that which it	16:50:35
10	is coupled to receive.	16:50:40
11	Q. So is it your position or not that the	16:50:54
12	power stage needs to receive the same control	16:50:57
13	signal that was generated by the flip-flop?	16:51:01
14	MR. PATARIU: Object to form.	16:51:07
15	THE WITNESS: Well, the power stage has	16:51:45
16	shown -- and the MS_Reed 0111592 shows that the	16:51:54
17	power stage receives the PWMHS signal. So the	16:52:00
18	answer is yes.	16:52:03
19	BY MR. DEVKAR:	09:06:04
20	Q. Putting aside the accused products, I'm	16:52:06
21	just referring to Claim 18.	16:52:13
22	In Claim 18, does the power stage need to	16:52:16
23	receive the same control signal that was generated	16:52:22
24	by the flip-flop?	16:52:26
25	A. Yeah. There was only one control signal	16:52:28

1 and the antecedent basis for the control signal is 16:52:31
2 the A control signal that's generated by the 16:52:34
3 flip-flop. 16:52:38

4 Q. Do you agree that the control signal 16:52:39
5 generated by the flip-flop passes through some 16:52:41
6 logic before being received by the power stage? 16:52:47

7 MR. PATARIU: Object to form. 16:52:53

8 THE WITNESS: I disagree that the PWMHS 16:52:54
9 signal that I've identified as the control signal 16:52:57
10 is the signal that is received by the power stage. 16:53:00

11 BY MR. DEVKAR: 09:06:04

12 Q. You disagree that the PWMHS signal that 16:53:32
13 you've identified is the control signal that is 16:53:36
14 received by the power stage? Did I hear that 16:53:41
15 correctly? 16:53:47

16 A. I said just the opposite. I said that is 16:53:47
17 the control signal that is received by the power 16:53:49
18 stage. 16:53:54

19 Q. And where does that PWMHS signal get 16:53:54
20 generated? 16:54:00

21 A. It gets generated in the flip-flop, as I 16:54:02
22 have shown. 16:54:05

23 Q. But you disagree that the PWMHS signal 16:54:11
24 generated by the flip-flop passes through any logic 16:54:14
25 before being received by the power stage? 16:54:19

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1	MR. PATARIU: Object to form.	16:54:28
2	THE WITNESS: I'm not aware of the PWMHS	16:54:28
3	signal passing through any additional logic before	16:54:31
4	it gets to the power stage, and I'm sitting here	16:54:36
5	looking at the schematic.	16:54:39
6	BY MR. DEVKAR:	09:06:04
7	Q. Does the PWMHS signal generated by the	16:55:23
8	flip-flop pass through a NOR gate and an inverter	16:55:30
9	prior to reaching the power stage?	16:55:42
10	MR. PATARIU: Object to form.	16:55:46
11	THE WITNESS: Again, the PWMHS signal is	16:55:47
12	after the NOR gates that you refer to. So no, it	16:55:51
13	doesn't pass through those gates in order to get to	16:55:59
14	the power stage.	16:56:02
15	BY MR. DEVKAR:	09:06:04
16	Q. Perhaps I'm looking at something different	16:56:05
17	than you. I'm referring to the figure under	16:56:11
18	paragraph 253 of your infringement report.	16:56:16
19	Are you looking at that figure?	16:56:21
20	A. Yes, sir, I am.	16:56:22
21	Q. The flip-flop is what's pointed to by your	16:56:29
22	orange arrow, correct?	16:56:32
23	A. Correct. The makeup of the flip-flop	16:56:33
24	itself is there.	16:56:36
25	Q. Where in that figure is the PWMHS signal	16:56:38

1	that is generated reflected in the figure?	16:56:44
2	A. It's reflected in the ellipse or the oval	16:56:47
3	that I've highlighted.	16:56:52
4	Q. That's all the way at the right side of	16:56:59
5	the figure, correct?	16:57:02
6	A. It's at the right side of the figure, yes.	16:57:03
7	That's the signal that's being generated by the	16:57:06
8	flip-flop.	16:57:09
9	Q. And that's the label for that signal,	16:57:10
10	correct?	16:57:12
11	A. That is correct, the PWMHS.	16:57:12
12	Q. In order for the signal coming out of the	16:57:18
13	flip-flop to reach that label that you've labeled	16:57:21
14	as PWMHS, do you see a NOR gate and an inverter?	16:57:25
15	A. Yes, certainly.	16:57:33
16	Q. And so how would the signal get to the	16:57:34
17	PWMHS location without passing through that NOR	16:57:42
18	gate and inverter?	16:57:46
19	A. You are trying to read the claim language	16:57:53
20	as if the control signal that's generated has to be	16:57:55
21	on the output terminal. There's no claim	16:57:58
22	limitation to that.	16:58:02
23	There's claim limitations to the reset and	16:58:03
24	the set terminal of the input and even in those	16:58:08
25	cases, they are coupled to receive. They don't	16:58:13

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1	have to receive it directly. They are coupled to	16:58:17
2	receive.	16:58:20
3	And likewise on the output, it just says	16:58:21
4	it generates the control signal. And I'm saying	16:58:24
5	that where I've identified the PWMHS, that is the	16:58:27
6	control signal that is generated by the flip-flop.	16:58:31
7	Q. What is, then, the signal that would be at	16:58:36
8	the upper-right corner of the flip-flop? What is	16:58:43
9	generated outside of that output terminal?	16:58:49
10	MR. PATARIU: Object to form.	16:58:53
11	THE WITNESS: What are you referring to	16:59:22
12	again?	16:59:25
13	BY MR. DEVKAR:	09:06:04
14	Q. I'm referring to the flip-flop that you've	16:59:26
15	labeled with your orange arrow. Do you see that?	16:59:29
16	A. I see that.	16:59:31
17	Q. Do you see the upper-right of that	16:59:32
18	rectangle that's pointed to by the flip-flop arrow?	16:59:39
19	Do you see that? There's four locations entering	16:59:43
20	this flip-flop, would you agree? Actually, there's	16:59:58
21	five but I'm talking about the upper-right one.	17:00:02
22	A. There's four inputs and one output. The	17:00:06
23	output is the upper-right one.	17:00:09
24	Q. Okay. So what signal is generated by the	17:00:11
25	flip-flop at that upper-right location?	17:00:14

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1	MR. PATARIU: Object to form.	17:00:19
2	THE WITNESS: It is an output -- there is	17:00:20
3	a signal generated on that output that doesn't have	17:00:23
4	a name but it generates the PWMHS signal. That's	17:00:26
5	the name that's actually -- I don't want to use	17:00:35
6	necessarily the word "buffer" but that's truthfully	17:00:39
7	what happens when you take it through an inverter;	17:00:43
8	you are basically staging it to drive a larger	17:00:46
9	load.	17:00:50
10	So I'm looking at that collectively as	17:00:50
11	what is being generated by that flip-flop.	17:00:53
12	BY MR. DEVKAR:	09:06:04
13	Q. But with respect to Claim 18, that output	17:00:56
14	of the flip-flop is not the control signal, is that	17:01:03
15	your position?	17:01:09
16	MR. PATARIU: Object to form.	17:01:11
17	THE WITNESS: The PWMHS signal is what is	17:01:12
18	generated by that flip-flop. And I don't know how	17:01:16
19	else to say it. That's what it is.	17:01:27
20	BY MR. DEVKAR:	09:06:04
21	Q. Okay, but the flip-flop at its output has	17:01:29
22	not generated the control signal, is that your	17:01:33
23	position?	17:01:35
24	MR. PATARIU: Object to form.	17:01:42
25	THE WITNESS: It has generated an output	17:01:43

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1 that is buffered, which is what the inverter does,
2 so that it can drive a load.

3 The transistors that are a part of the
4 flip-flop are too small to drive the power stage.
5 So this is taking that output, buffering it and
6 basically giving it more power strength to drive
7 the load.

8 And that's what I'm calling the signal,
9 the control signal that's generated.

10 BY MR. DEVKAR:

11 Q. Is it your position that the NOR gate and
12 the inverter are part of the flip-flop?

13 MR. PATARIU: Object to form.

14 THE WITNESS: In this case they are
15 circuits that condition the signal that's generated
16 by the last transistor within that flip-flop
17 itself, the circuit of the flip-flop, and
18 conditions that signal for package, which I'm
19 saying it has size in the transistors that are able
20 to drive a larger load and that is what that signal
21 is.

22 You know, I could take the exact same
23 signal out of the flip-flop at its output terminal
24 itself and if it was robust enough, I could drive
25 the power stage with that just as well. It's the

1	same.	17:03:12
2	But in terms of putting and instantiating	17:03:13
3	a circuit that drives from a small to a larger	17:03:17
4	load, this is the way in which it's done. There's	17:03:22
5	nothing that changes what the flip-flop is	17:03:26
6	generating from what is actually going to the	17:03:29
7	high-side driver.	17:03:33
8	BY MR. DEVKAR:	09:06:04
9	Q. You pointed to the rectangle at the end of	17:03:37
10	the orange arrow as the flip-flop, correct?	17:03:42
11	A. Correct.	17:03:45
12	Q. At its output, has this flip-flop	17:03:47
13	generated the control signal PWMHS?	17:03:54
14	A. I'll use the word precursor. It's	17:04:06
15	generating a precursor that is going to be the	17:04:09
16	PWMHS signal that now has the power to drive that	17:04:12
17	down-stage power circuit.	17:04:16
18	Q. But the flip-flop standing alone has not	17:04:18
19	yet generated the control signal at its output, is	17:04:22
20	that your position?	17:04:26
21	MR. PATARIU: Object to form.	17:04:28
22	THE WITNESS: My position is the PWMHS	17:04:33
23	signal is the generated control signal by the	17:04:37
24	flip-flop.	17:04:41
25	BY MR. DEVKAR:	17:04:42

1 Q. So at the output of the flip-flop, does
2 the PWMHS signal that you're calling the control
3 signal exist at that juncture?

17:04:42

17:04:49

17:04:54

4 A. The signal at that particular point, the
5 only thing that happens to it is it's conditioned
6 to driving the power stage load.

17:05:02

17:05:09

17:05:14

7 And what occurs at the output of the
8 flip-flop also occurs at PWMHS. Again, PWMHS in my
9 belief is the generated control signal.

17:05:18

17:05:20

17:05:29

10 Q. In paragraph 256, the figure below it I
11 believe shows the circuitry for driving the power
12 stage, is that correct?

17:05:46

17:05:51

17:05:57

13 A. That is correct.

17:05:58

14 Q. And does this not include the drivers for
15 driving the power stage?

17:06:02

17:06:07

16 A. That's part of the power stage, yes.

17:06:09

17 Q. And this only drives a portion of the
18 power stage, not the entire power stage; is that
19 correct?

17:07:02

17:07:05

17:07:08

20 A. I hope so.

17:07:08

21 Q. And in particular it drives the high-side
22 switch; is that correct?

17:07:11

17:07:14

23 A. This one drives the high-side switch, that
24 is correct. It drives the high-side switch within
25 the power stage.

17:07:15

17:07:19

17:07:22

1 Q. We are referring back to the figure under
2 paragraph 253 of your report. I just want to be
3 clear on whether your position is that the
4 flip-flop includes the NOR gate and the inverter.

5 MR. PATARIU: Object to form.

6 THE WITNESS: I placed that not in the
7 power stage, nor do I put that in the flip-flop.
8 That is in the coupling.

9 The power stage is coupled to the output
10 terminals of the flip-flop and when it is coupled
11 to the output of the flip-flop, one of the results
12 is it receives the control signal that the
13 flip-flop generated.

14 If there was not any coupling circuitry
15 there, you know, that's the way it's electrically
16 connected together through that coupling. But
17 again, the PWMHS signal is that which the power
18 stage -- is the signal that the power stage
19 receives. That is the signal that's generated by
20 the flip-flop and there is some coupling circuitry
21 that's claimed as well.

22 BY MR. DEVKAR:

23 Q. What are you referring to by the coupling
24 circuitry that's claimed?

25 A. The last element of the claim is a power

17:07:30
17:07:35
17:07:42
17:07:47
17:08:04
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17:08:35
17:08:41
17:08:43
17:08:46
17:08:48
17:08:53
17:09:00
17:09:03
17:09:07
17:09:09
17:09:12
17:09:16
17:09:16
17:09:18
17:09:20
17:09:23

1 stage coupled to the output terminal. There's not
2 any restriction as to how it's coupled but there is
3 a coupling electrically coupled to the output
4 terminal.

5 Q. And in this case it's coupled via a NOR
6 gate?

7 A. A NOR gate and an inverter.

8 Q. Right, and your position is that NOR gate
9 and that inverter do not change the signal that is
10 output by the flip-flop at its output terminal?

11 A. I've never said that. No, I've never said
12 that. That is your surmising that somehow the
13 signal has to be on the output terminal of the
14 flip-flop. There's no restriction in this claim
15 for that at all.

16 There is a flip-flop that has three
17 terminals, including an output terminal, but the
18 only restriction in the claim for the output
19 terminal is that it's coupled to the power stage.

20 And so that's different than the
21 generation of the signal. The signal is not
22 something that's coupled. It's the coupling to the
23 output stage -- excuse me, it's the power stage
24 coupled to the output terminal.

25 The flip-flop is also coupled to receive

17:09:27
17:09:30
17:09:33
17:09:38
17:09:39
17:09:44
17:09:44
17:09:46
17:09:48
17:09:52
17:09:57
17:10:00
17:10:03
17:10:05
17:10:08
17:10:10
17:10:12
17:10:15
17:10:18
17:10:24
17:10:26
17:10:29
17:10:34
17:10:37
17:10:40

1 the control signal but it doesn't have to be 17:10:42
2 literally the node on the output of the flip-flop. 17:10:46
3 And I think that the way I have read this is 17:10:52
4 correct and that's why I pointed to the PWMHS as 17:10:57
5 the signal because that is the signal that's 17:11:01
6 generated by the flip-flop. 17:11:03

7 There's coupling of circuitry as well is 17:11:06
8 required, but that signal that is generated, PWMHS 17:11:10
9 is the signal. That control signal is the control 17:11:16
10 signal that's received by the power stage. 17:11:20

11 Q. Is PWMHS the signal that is generated by 17:11:24
12 the flip-flop at its output? 17:11:31

13 MR. PATARIU: Object to form. 17:11:36

14 THE WITNESS: There's nothing in the claim 17:11:40
15 limitation that does what you just said. You just 17:11:42
16 said it generates the control signal at the output. 17:11:47
17 There's nothing in the claim that says that. 17:11:53

18 BY MR. DEVKAR: 09:06:04

19 Q. The claim says the flip-flop generates the 17:11:55
20 control signal. 17:11:58

21 A. That's right, it generates the control 17:11:59
22 signal. 17:12:02

23 Q. But not by itself? Is that your position? 17:12:02

24 A. No. You added in additional words that 17:12:07
25 the control signal that is generated has to be 17:12:13

1 literally only at the output terminal of that
2 flip-flop. There's nothing in the claim that says
3 that.

4 The only thing in the output terminal is
5 that the flip-flop has an output terminal and that
6 output terminal is coupled to the power stage.

7 Q. Right. But the claim also says that the
8 flip-flop generates the control signal.

9 A. And I'm saying the PWMHS is the control
10 signal that is generated.

11 Q. Does PWMHS control the power stage or do
12 you also need PWMLS to control the power stage?

13 MR. PATARIU: Object to form.

14 THE WITNESS: Irrelevant. You do use
15 PWMLS -- you use a different signal going to the
16 power stage for other purposes as well but that
17 doesn't change the fact that the power stage is
18 coupled to receive the control signal, PWMHS,
19 wherein, based on the control signal, the power
20 stage converts an input voltage into a switching
21 signal, period. That's it.

22 So whether it has additional things coming
23 to the power stage is beyond the scope of this
24 claim. You can have other things. It's a
25 comprising claim.

1 BY MR. DEVKAR:

17:14:10

2 Q. How does it convert the input voltage into
3 a switching signal without PWMLS?

17:14:10

17:14:14

4 MR. PATARIU: Object to form.

17:14:25

5 THE WITNESS: Because as soon as you
6 generate a PWMHS signal, that PWM -- I'm getting
7 lost on the words here. That PWMHS signal to the
8 power stage drives the high-side driver which then
9 changes the switching signal.

17:14:25

17:14:27

17:14:36

17:14:44

17:14:51

10 I mean the switching signal can only get a
11 higher value than where it is at by the high-side
12 driver. That's what the high-side driver does. It
13 influences the switching signal by providing
14 additional voltage to it.

17:14:55

17:15:02

17:15:06

17:15:10

17:15:13

15 BY MR. DEVKAR:

17:15:19

16 Q. I'd like to turn to paragraph 214 of your
17 report at Exhibit 1.

17:15:19

17:15:28

18 A. (Perusing.)

17:15:45

19 Q. Are you there?

17:15:47

20 A. Yes, I am.

17:15:47

21 Q. And in paragraph 214 you state: "The
22 control signal input to the minimum off time
23 generator is highlighted below. The claimed
24 control signal controls the LS_BLANK input to the
25 LSOC_NOC_15V schematic."

17:15:50

17:15:54

17:15:57

17:16:01

17:16:08

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1	Do you see that?	17:16:17
2	A. I do.	17:16:17
3	Q. Is there a flip-flop and an inverter	17:16:27
4	between your purported control signal PWMHS and	17:16:32
5	LS_BLANK?	17:16:40
6	MR. PATARIU: Object to form.	17:16:56
7	THE WITNESS: In this schematic that's	17:17:36
8	shown here in paragraph 214, the PWM signal is the	17:17:38
9	input on the input side and there's a flip-flop	17:17:46
10	that then an output is the LS_BLANK, if that's what	17:17:51
11	you were asking.	17:17:57
12	BY MR. DEVKAR:	09:06:04
13	Q. The output of the flip-flop appears at the	17:17:59
14	upper-right of the flip-flop?	17:18:03
15	A. Yes, that is correct.	17:18:05
16	Q. And does that output pass through an	17:18:06
17	inverter?	17:18:09
18	A. No, it does not.	17:18:13
19	Q. What is shown to the right of the output	17:18:16
20	of the flip-flop?	17:18:20
21	A. It's a buffer; just adds extra voltage to	17:18:21
22	it, extra driver capability.	17:18:28
23	Q. So the control signal that you've asserted	17:18:32
24	as PWMHS passes through a flip-flop and a buffer	17:18:38
25	before reaching the location labeled LS_BLANK; is	17:18:53

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1	that correct?	17:18:59
2	MR. PATARIU: Object to form.	17:19:00
3	THE WITNESS: I don't quite get your	17:19:08
4	point. The control signal that's received by this	17:19:10
5	circuit is the PWM signal and what I said at 214 is	17:19:13
6	that controls the LS_BLANK input to the LSOC	17:19:19
7	schematic.	17:19:29
8	BY MR. DEVKAR:	09:06:04
9	Q. Where is the off time generator that you	17:19:34
10	have labeled in this figure?	17:19:37
11	A. It is what you see in that figure.	17:19:44
12	Q. The entirety of the figure?	17:19:48
13	A. Yeah, because you've got an input that is	17:19:49
14	PWM and the output is the LSOC. Yes, it is that	17:19:52
15	circuit.	17:20:48
16	Q. Would you agree that the output to the	17:20:59
17	flip-flop we were discussing earlier that generates	17:21:04
18	the control signal that you've identified passes	17:21:11
19	through multiple logic elements before being	17:21:16
20	received by the off time generator that you've	17:21:28
21	labeled in this figure?	17:21:33
22	MR. PATARIU: Object to form.	17:21:40
23	THE WITNESS: Well, I've highlighted on	17:26:18
24	page 98 the minimum off time generator and that's	17:26:23
25	the circuitry within that blue box. And I said the	17:26:33

1 minimum off-time signal that's generated is on the 17:26:42
2 right side of the box, it's the LSOC. 17:26:45

3 And the LSOC is generated by a circuitry 17:27:05
4 that has its input LS_BLANK which comes from the 17:27:09
5 PWM. 17:27:13

6 So the PWM signal, it is the minimum off 17:27:14
7 time generator input. It's the signal input which 17:27:20
8 is the control signal. And within that box that 17:27:23
9 I've identified on page 98 there is an LS_BLANK 17:27:28
10 signal that is input, the output of which is the 17:27:35
11 LSOC. 17:27:44

12 So that's the circuitry I've identified. 17:27:45
13 So we have PWN in and LSOC out. 17:27:47

14 BY MR. DEVKAR: 17:27:54

15 Q. So in the figure on page 99, what is 17:27:54
16 reflected by the sort of greyed-out, highlighted 17:28:01
17 area on the right side of the figure? 17:28:05

18 A. That's the block diagram where you have an 17:28:08
19 output of LSOC and you have an input of LS_BLANK. 17:28:14

20 It's not greyed out. It comes from the 17:28:19
21 printout in which the IO pins were identified. 17:28:22

22 It's an overlay. And so if you look underneath 17:28:28
23 that overlay, you would see that box that's within 17:28:32
24 it has LSOC as the output and LS_BLANK as the 17:28:40
25 input. 17:28:47

1 And what I've shown in this circuit here
2 that is a part of that entire minimum off time
3 generator is that the PWM signal is the input to
4 it. Within that circuitry there is an LS-blank
5 that's generated and within that box that you call
6 greyed out, that LS_BLANK eventually spawns the
7 LSOC which is the output.

17:28:47

17:28:49

17:28:53

17:28:58

17:29:02

17:29:06

17:29:10

8 Q. Okay.

17:29:14

9 A. It's a large circuit area.

17:29:15

10 Q. But the entirety of the figure that you've
11 shown on page 99 is what you're calling the minimum
12 off time generator; is that correct?

17:29:18

17:29:21

17:29:26

13 A. Yes, sir, that is correct.

17:29:28

14 Q. And then on page 98 what's outlined in
15 blue is another reflection of the same off time
16 generator?

17:29:29

17:29:35

17:29:43

17 MR. PATARIU: Object to form.

17:29:45

18 THE WITNESS: 98 is what I've colored in
19 the blue box as the off-time generator. And I've
20 also identified the LSOC on the right side in that
21 red circle. That's the LSOC. You can see the
22 greyed out area also just to the left of that red
23 circle.

17:29:46

17:29:49

17:29:54

17:30:00

17:30:04

17:30:08

24 And so what you are seeing on the next
25 page is an enlargement of that area that shows that

17:30:09

17:30:12

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1	the LSOC in that greyed out area is an output of	17:30:16
2	circuitry that has LS_BLANK as an input of that	17:30:21
3	circuit, and the LS_BLANK is created from the PWM	17:30:25
4	input to the overall minimum off-time generator.	17:30:28
5	MR. DEVKAR: Can we please upload	17:31:12
6	Exhibit 7 to the chat window?	17:31:16
7	THE WITNESS: (Perusing.)	17:31:21
8	(McAlexander Exhibit 7,	17:31:21
9	Confidential-Withdrawn by Counsel,	17:31:21
10	was marked for identification.)	17:31:21
11	MR. PATARIU: If we're switching lines of	17:31:25
12	questioning, I think we've been on the record for	17:31:26
13	an hour. I think we could take our next break.	17:31:28
14	MR. DEVKAR: That's fine.	17:31:33
15	THE VIDEOGRAPHER: Off the record, the	17:31:35
16	time is 5:31 p.m.	17:31:37
17	(Break taken.)	17:32:09
18	THE VIDEOGRAPHER: We're back on the	17:44:18
19	record. The time is 5:44 p.m.	17:44:30
20	BY MR. DEVKAR:	17:44:38
21	Q. I'd like to turn to paragraph 630 of	17:44:39
22	Exhibit 1, your opening report. This is the	17:44:45
23	section entitled "License Agreements."	17:45:01
24	Please let me know when you're there?	17:45:03
25	A. Okay, I've got it.	17:45:21