

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,
Petitioner,

v.

MONOLITHIC POWER SYSTEMS, INC.,
Patent Owner,

Case No. IPR2024-01158

Patent No. 9,041,377

PATENT OWNER'S ORAL HEARING DEMONSTRATIVES

Dated: October 21, 2025 Foley & Lardner LLP 11988 El Camino Real, Suite 400 San Diego, CA 92130 (858) 720-5700	Respectfully submitted, By: <u> / Miguel Bombach /</u> Miguel Bombach, Reg. No. 68,636 Back-Up Counsel John P. Schnurer, Reg. No. 52,196 Lead Counsel Back-Up Counsel: John D. Esterhay, Reg. No. 73,512 <i>Attorneys for Patent Owner Monolithic Power Systems, Inc.</i>
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CERTIFICATE OF SERVICE

The undersigned hereby certifies that on October 21, 2025, a true and correct copy of the foregoing PATENT OWNER'S ORAL HEARING DEMONSTRATIVES EXHIBIT 2009 was served electronically on counsel of record for Petitioner to the email addresses below:

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Dated: October 21, 2025

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Reed Semiconductor Corp.
v.
Monolithic Power Systems, Inc.

IPR2024-01158

Patent Owner's Demonstratives
October 23, 2025

Instituted Grounds

Ground	Claims	Description
1	1-4, 9-14, and 17-18	Anticipated under §102 by Tateishi and/or the Tateishi Patent.
2	5, 7-8, and 15	Rendered obvious under §103 by Tateishi and/or the Tateishi Patent.

(Paper 1 at 24)

Tateishi is prior art under (pre-AIA) §102(b) because it was published more than one year before the earliest effective filing date of the '377 Patent. Tateishi issued as U.S. Patent No. 8,476,887 ("Tateishi Patent") on July 2, 2013. *See* EX1005. The Tateishi Patent is also prior art under (pre-AIA) §102(e) because it was filed (February 6, 2009) prior to the earliest effective filing date of the claimed invention.

(Paper 1 at 23)

Anticipation

“All of the elements and limitations of the claim must be shown in a single prior reference, arranged as in the claim.” *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). “‘It is not sufficient to constitute an anticipation that the device relied upon might, *by modification*, be made to accomplish the function performed by the patent in question, if it were not designed by its maker, nor adapted, nor actually used, for the performance of such functions.’ In other words, a prior art reference anticipates a claim only if it discloses all the elements ‘in the same form and order as in the claim.’” *In re Chudik*, 851 F.3d at 1372 (citing *Topliff v. Topliff*, 145 U.S. 156, 161 (1892) & *Abbott Labs. v. Sandoz, Inc.*, 544 F.3d 1341, 1345 (Fed. Cir. 2008)).

(Paper 23 at 14)

Anticipation

- ***BlephEx, LLC v. Myco Indus., Inc.***, 24 F.4th 1391, 1402 (Fed. Cir. 2022) (affirming finding of no anticipation where prior art reference's first figure disclosed a wand and a second figure disclosed a hand-held device, but the references could not be combined to support anticipation of the claimed swab connected to an electromechanical device because no technical discussion other than attorney argument was presented to argue that a POSITA would "at once envisage" the combination of the references)
- ***Wonderland Nurserygoods Co. v. Baby Trend, Inc.***, 727 F. App'x 1017, 1019-20 (Fed. Cir. 2018) (reversing anticipation finding made in an IPR proceeding because the claims required that there was a single "enclosure member" (e.g., a single piece of fabric over a frame) and the prior art's disclosed netting over a frame was not continuous because the figure's depicted edges in the netting did not align)
- ***Nidec Motor Corporation v. Zhongshan Broad Ocean Motor Co. Ltd***, 851 F.3d 1270, 1274-75 (Fed. Cir. 2017) (reversing anticipation finding made in an IPR proceeding because the claims and specification required that an "IQdr demand signal" in a "rotating frame of reference," but the petitioner only identified signals in a "stationary frame of reference" and the Board is not permitted to find anticipation in view of a missing claim limitation)
- ***In re Chudik***, 851 F.3d 1365, 1372-74 (Fed. Cir. 2017) (reversing the Board's anticipation finding because the claim required that a protruding surface be "arranged to engage" (e.g., contact) a cavity, but this could only happen in the prior art if an element was removed)
- ***Dell Inc. v. Acceleron, LLC***, 818 F.3d 1293, 1298-99 (Fed. Cir. 2016) (affirming the Board's finding of no anticipation because, even though the prior art reference described that the CPU could boot from somewhere on the network, it did not teach booting from the NAS, as required by the claim)
- ***Enfish, LLC v. Microsoft Corp.***, 822 F. 3d 1327, 1342-43 (Fed. Cir. 2016) (reversing a summary judgment granting anticipation because the claim required recited aspects of rows and columns for "a logical table," and thus, the rows and columns needed to be in the same table, and the district court erred in construing the claim too broadly to permit the rows and columns to be from two tables)
- ***Verve, LLC v. Crane Cams, Inc.***, 311 F.3d 1116, 1118, 1121 (Fed. Cir. 2002) (reversing anticipation finding because the prior art reference disclosed a rod that had a uniform diameter along its length (even though the ends had a smaller diameter) but the claims required a rod that had a diameter larger in the middle than towards the ends)
- ***Gen. Elec. Co. v. Nintendo Co.***, 179 F.3d 1350, 1357 (Fed. Cir. 1999) (reversing finding of anticipation where the claims required that a television receive signals from an antenna and then to switch to receiving signals from a video player when the player was turned on because the prior art reference did not expressly disclose the switching and defendant's argument that a POSITA would understand that this switching occurs in televisions was not sufficient to show that the limitation was actually disclosed in the reference)

(Paper 23 at 13-16)

Anticipation

- ***U.S. Well Servs., LLC v. Halliburton Energy Servs., Inc.***, IPR2022-01163, Paper 9 at 12-14, 17, 24 (P.T.A.B. Dec. 20, 2022) (declining to institute IPR under anticipation where the claim required comparing different signals, but the portion of the reference cited by the petitioner only disclosed comparing duplicate signals)
- ***Lenovo (United States) Inc. & Motorola Mobility LLC, v. Theta Ip, LLC***, IPR2023-00697, Paper 32 at 32-34, 37-38 (P.T.A.B. Oct. 16, 2024) (finding that a reference did not anticipate the claimed determining of signal strength of two channels at the same time because the cited portion of the reference disclosed determining the strength of either of two signals, but did not explicitly disclose determining strength of both at the same time)
- ***K-40 Elecs., LLC, v. Escort, Inc.***, IPR2013-00240, Paper 37 at 34 (P.T.A.B. Sept. 29, 2014) (finding no anticipation where the claim required that a receiver receive the same signal continuously, but the portions cited by the petitioner in the reference disclosed identification from multiple sources, and thus, did not disclose a continuously received signal (but later finding the claims anticipated by another reference))
- ***Ex parte Ajay Mahajan and Sumeer Lal***, Appeal 2010008922 at 5 (Dec. 19, 2012) (reversing anticipation rejection because the claims required that two transducers received the same signal, but the alleged reference disclosed two transducers receiving different signals)

(Paper 23 at 13-16)



The Petition Fails to Teach Anticipation

(a) Petitioner fails to track the antecedent basis of “control signal” regardless of construction

(b) Petitioner fails to demonstrate that Tateishi anticipates the properly construed “control signal

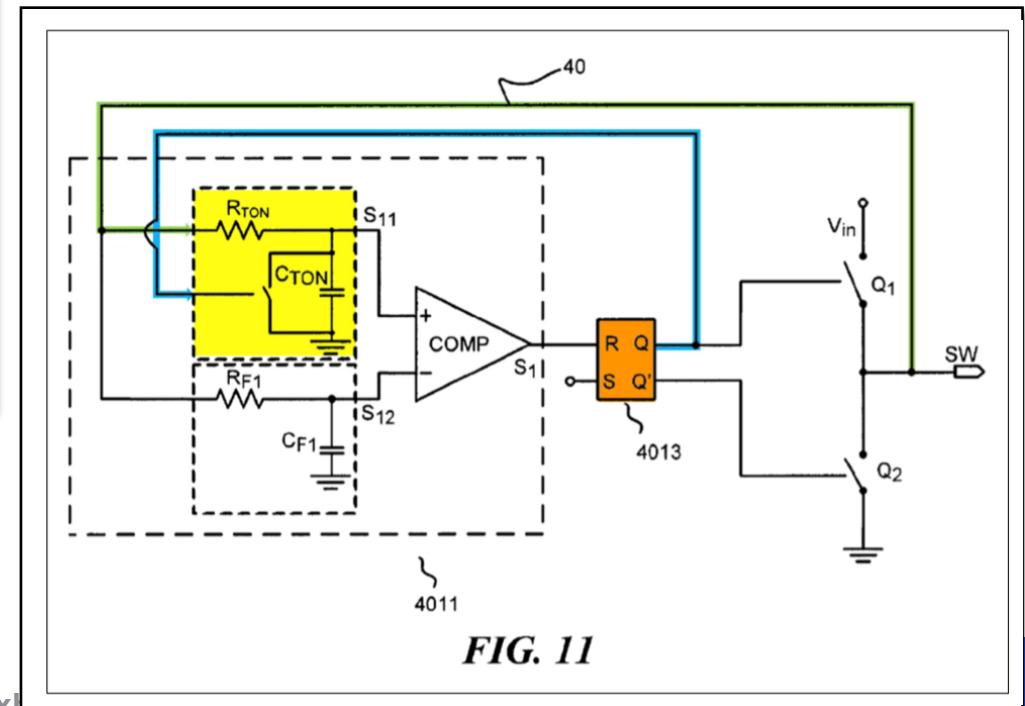
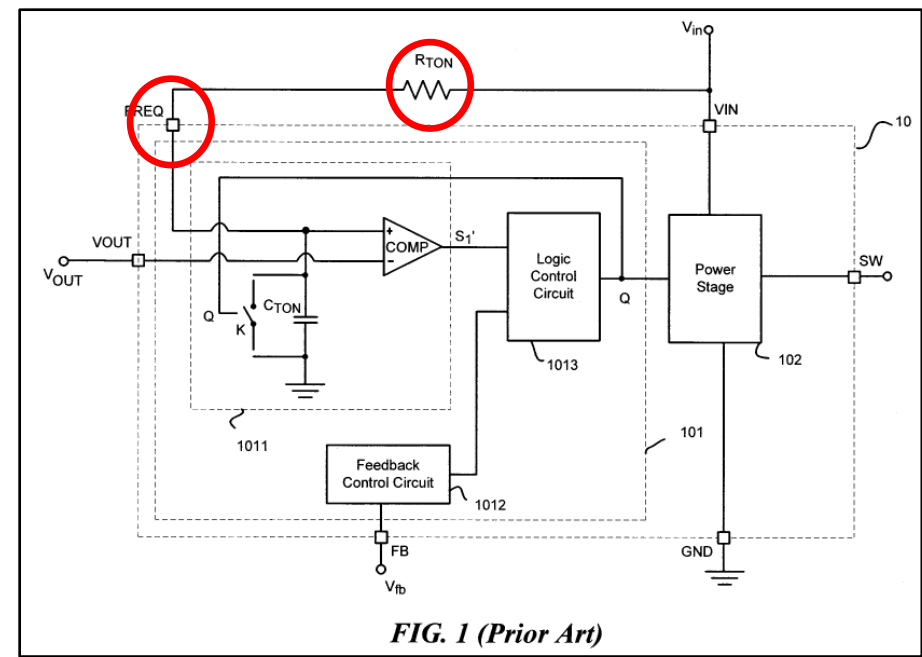
(c) Petitioner fails to demonstrate that Tateishi anticipates the “control signal” under its own construction

The '377 and the Claimed Control Signal

'377 Patent Reduces Chip Size and Cost

The '377 Patent is directed towards “pseudo constant on time control circuit[s] ... [for] step-down regulators.” (EX1001 at 1:12-15; EX2005, ¶ 34.) It provides an on-time generator 4011 that has an input voltage sensing circuit (yellow) that receives a switching signal SW (green) and also a control signal (blue) from the flip-flop 4013 (orange). (EX1001 at 8:18-41; *see also id.* at FIG. 4; EX2005, ¶ 36.) With this structure, the voltage converter does not need extra circuitry that the prior art devices needed (*e.g.*, an output voltage pin VOUT, a frequency setting pin FREQ, and the external frequency setting resistor), which reduces chip size and cost. (EX1001 at 7:65-66, 8:8-17; *see also* EX2005, ¶¶ 34–36 (describing the '377 Patent's discussion of failures in the art needing extra pins).)

(Paper 23 at 4; see *also* EX2005 at ¶ 35)



Claims Require a Control Signal

18. A step-down regulator, comprising:
an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal the on-time generator generates an on-time signal;
a minimum off time generator configured to receive the control signal and to generate a minimum off time signal in accordance with the control signal;
•
•
•
a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal and
a power stage coupled to the output terminal of the flip-flop to receive the control signal wherein based on the control signal the power stage converts an input voltage into the switching signal.

Claims Require a Control Signal

1. A step-down regulator, comprising:
a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:
an on-time generator comprising:
an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive **a control signal** provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the **control signal**, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

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a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates **the control signal**, and

(Paper 23 at 9)

11. A pseudo constant on time control circuit for a step-down regulator, comprising:
an on-time generator comprising:
an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive **a control signal** provided by the pseudo constant on time control circuit, and wherein based on the switching signal and **the control signal** the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

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a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates **the control signal**.

(Paper 23 at 9)



Claims Require a Control Signal

18. A step-down regulator, comprising:

an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal the on-time generator generates an on-time signal;

a minimum off time generator configured to receive the control signal and to generate a minimum off time signal in accordance with the control signal:

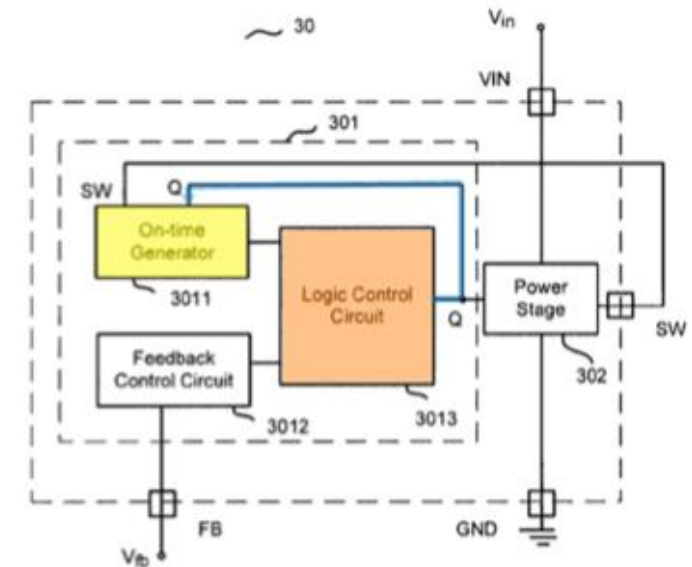
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a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal and

a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal the power stage converts an input voltage into the switching signal.

Control signal generated from—and provided to—specific hardware elements

FIG. 10



(Paper 23 at 11)

(Paper 23 at 10)

(a) Antecedent Basis

“Control Signal” – all the same

18. A step-down regulator, comprising:
an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal wherein based on the switching signal and the control signal the on-time generator generates an on-time signal;
a minimum off time generator configured to receive the control signal and to generate a minimum off time signal in accordance with the control signal;
•
•
•
a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal and
a power stage coupled to the output terminal of the flip-flop to receive the control signal wherein based on the control signal the power stage converts an input voltage into the switching signal.

(Paper 23 at 10)

“Control Signal” – all the same

The Petition identifies several different signals as the “control signal” across various limitations. This is improper because a later identified element—which receives its antecedent basis from an earlier described element—must be the same throughout a claim. *E.g.*, *Salazar v. AT&T Mobility LLC*, 64 F.4th 1311, 1317 (Fed. Cir.), cert. denied, 144 S. Ct. 422, 217 L. Ed. 2d 234 (2023); *Haemonetics Corp. v. Baxter Healthcare Corp.*, 607 F.3d 776, 781–82 (Fed. Cir. 2010) (“Claim 16 states: ‘A centrifugal unit comprising a centrifugal component and a plurality of tubes....’ . . . [I]t unambiguously defines ‘centrifugal unit’ as ‘comprising’ two structural components: a centrifugal component and a plurality of tubes. The claim then further recites, not the centrifugal component and not *a* centrifugal unit, but ‘*the* centrifugal unit’ as ‘having a radius between 25 and 50 mm and a height between 75 and 125% of the radius.’ Reading ‘the centrifugal unit’ in the context of the dimensional limitations to refer exclusively to the vessel, as the district court did, ignores the antecedent basis for ‘the centrifugal unit.’”); *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1356 (Fed. Cir. 1999) (“It is clear from the language of the claim itself that the term ‘a discharge rate’ in clause [b] is referring to the same rate as the term ‘the discharge rate’ in clause [d].”).

“Control Signal” – all the same

6 Q In your opinion, do all instances of the
7 language "control signal" in claim 1 refer to the
8 same signal?

9 MR. DEVKAR: Objection. Form.

10 THE WITNESS: Well, let me ponder that.

11 All right. So the claim introduces the
12 term "control signal" in line 45. It says "to
13 receive a control signal."

14 And then the next time it's referenced, it
15 is in line 47, "the control signal," which is -- the
16 antecedent of that is the "a control signal" that
17 showed up in 45. Therefore, those would be the
18 same.

19 "Output voltage" (reading to self).

20 The next time it shows up, if I'm not
21 missing something, is line 9 where, again, it's "the
22 control signal," which references back to "a control
1 signal" in 45 of column 9.

2 And then in line -- column 10, line 12,
3 again, "the control signal" is mentioned. And it,
4 again, is the -- hearkens back to the "a control
5 signal" that first appears in line 45. So they
6 would all be the same.

(EX2006 at 23:6-24:6)

Petitioner's Expert

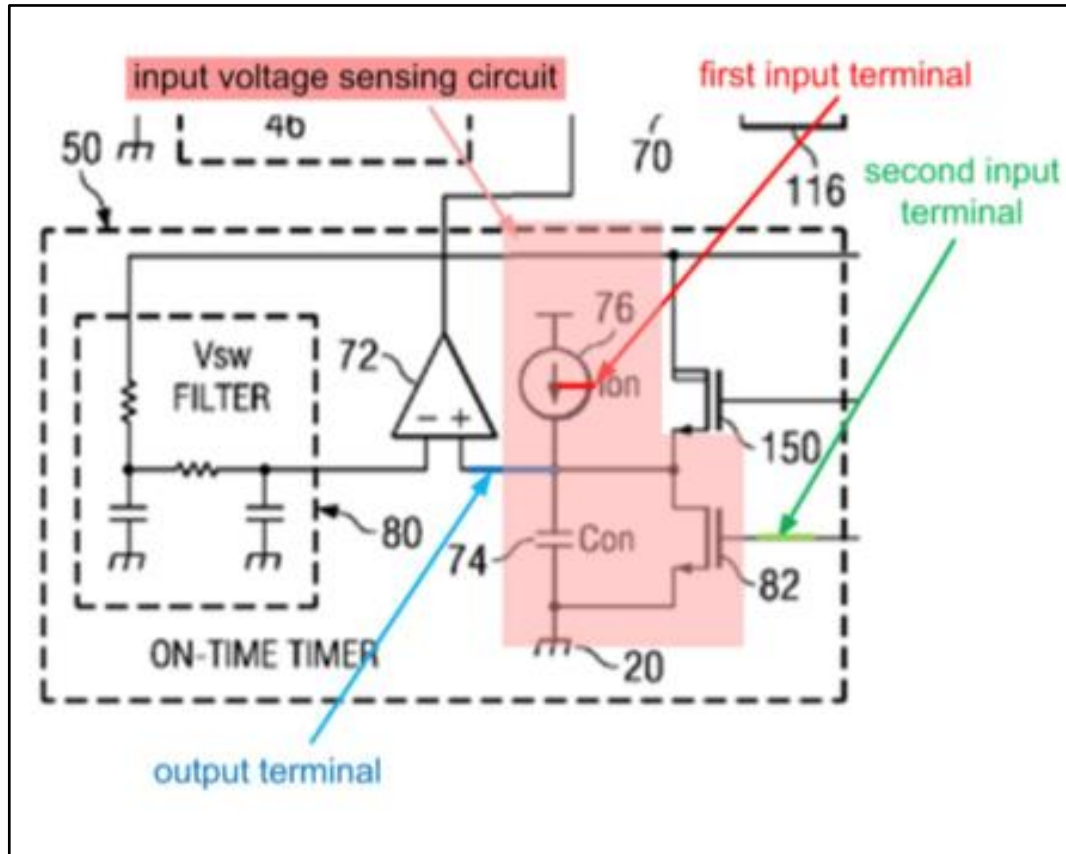
7 Q In your opinion, do all instances of the
8 recited control signal in claim 18 refer to the same
9 signal?
10 A Yeah. Every instance where it says "the
11 control signal," it's -- the antecedent for that is
12 "a control signal" found in line 21, 2, 3, of
13 column 13.

(EX2006 at 26:7-13)

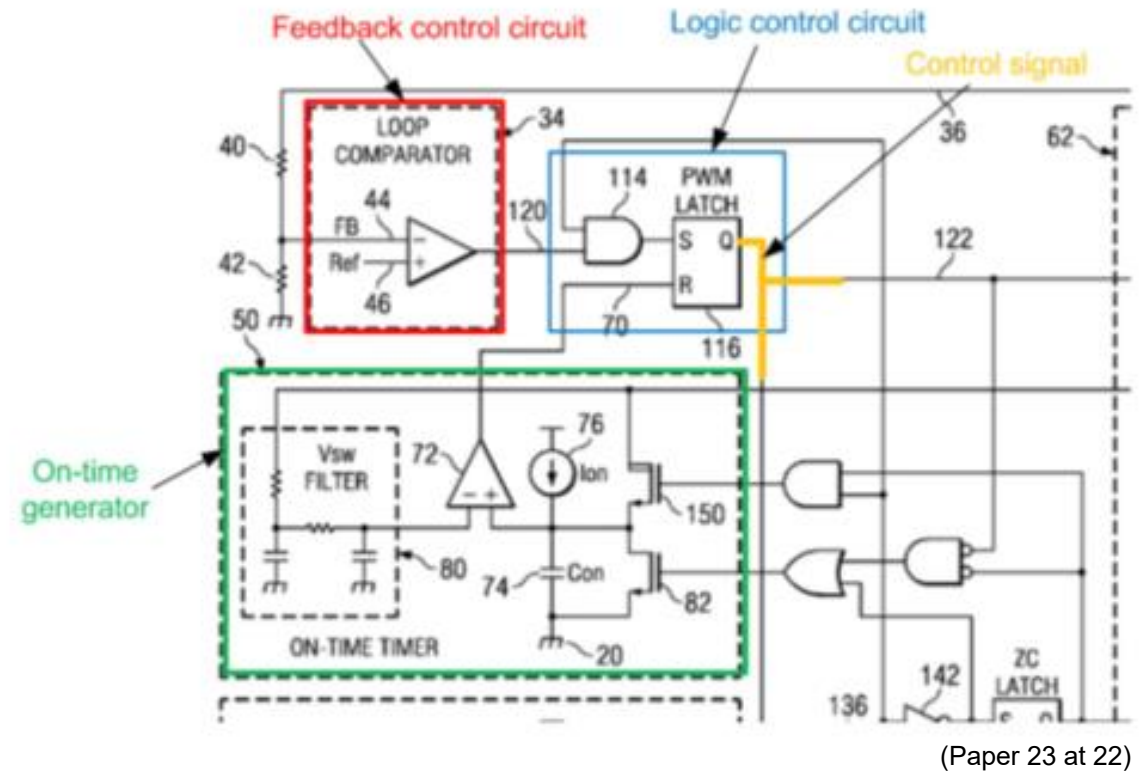
64. The independent claims of the '377 Patent (EX1001) refer to a single “control signal.” For example, independent claim 1 refers to an input voltage sensing circuit that receives the control signal and generates an input voltage sensing signal. (claim 1 at 9:40-50). That control signal is generated by the logic control circuit (claim 1 at 10:9). That same control signal is also an input to the power stage (claim 1 at 10:11) and, based on the control signal, the power stage generates a switching signal (claim 1 at 10:12-13). Independent claim 11 similarly recites that the on-time generator's input voltage sensing circuit receives the control signal and based on the control signal, generates the input voltage sensing signal (claim 11 at 11:44-52). And the logic control circuit generates the control signal (claim 11 at 12:13). Independent claim 18 (the other independent claim) similarly recites that the control signal is an input into the on-time generator, and the on-time generator uses it to generate an on-time signal (claim 18 at 13:21-25). The minimum off time generator receives the control signal and uses it to generate a minimum off time signal (claim 18 at 14:1-4). The flip-flop generates the control signal (claim 18 at 14:18-19), and the power stage receives the control signal and generates the switching signal (claim 18 at 14:21-24). Accordingly, in my opinion, in all of these claims, the term “control signal” must be the same signal throughout each respective claim limitation.

Inconsistent Identification

Petitioner's Identification for 1[B2]



Petitioner's Identification for 1[D]



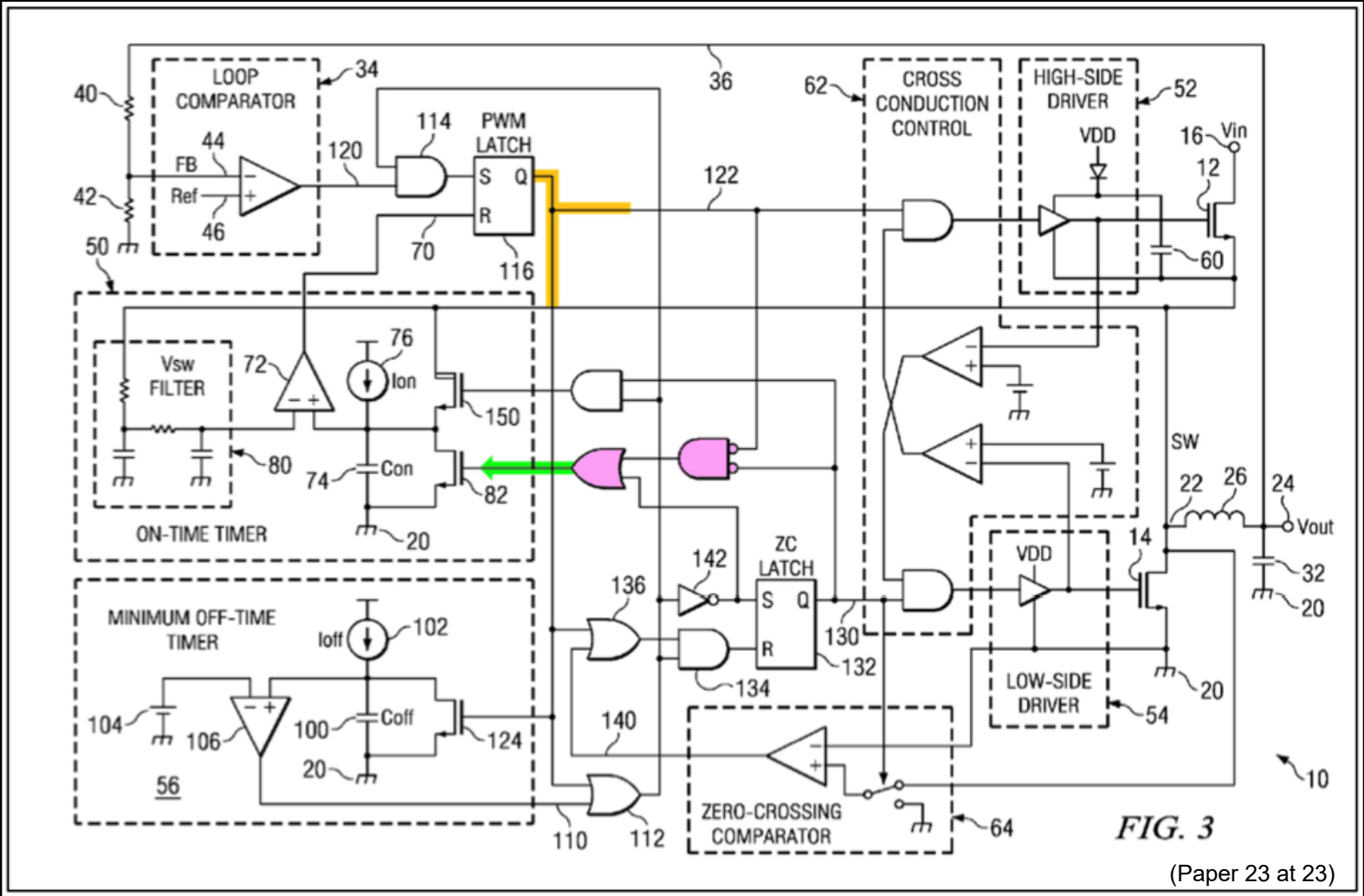
(Paper 23 at 22)

Inconsistent Identification

Not the Same Signal

Petitioner's Identification for 1[D]

Petitioner's Identification for 1[B2]



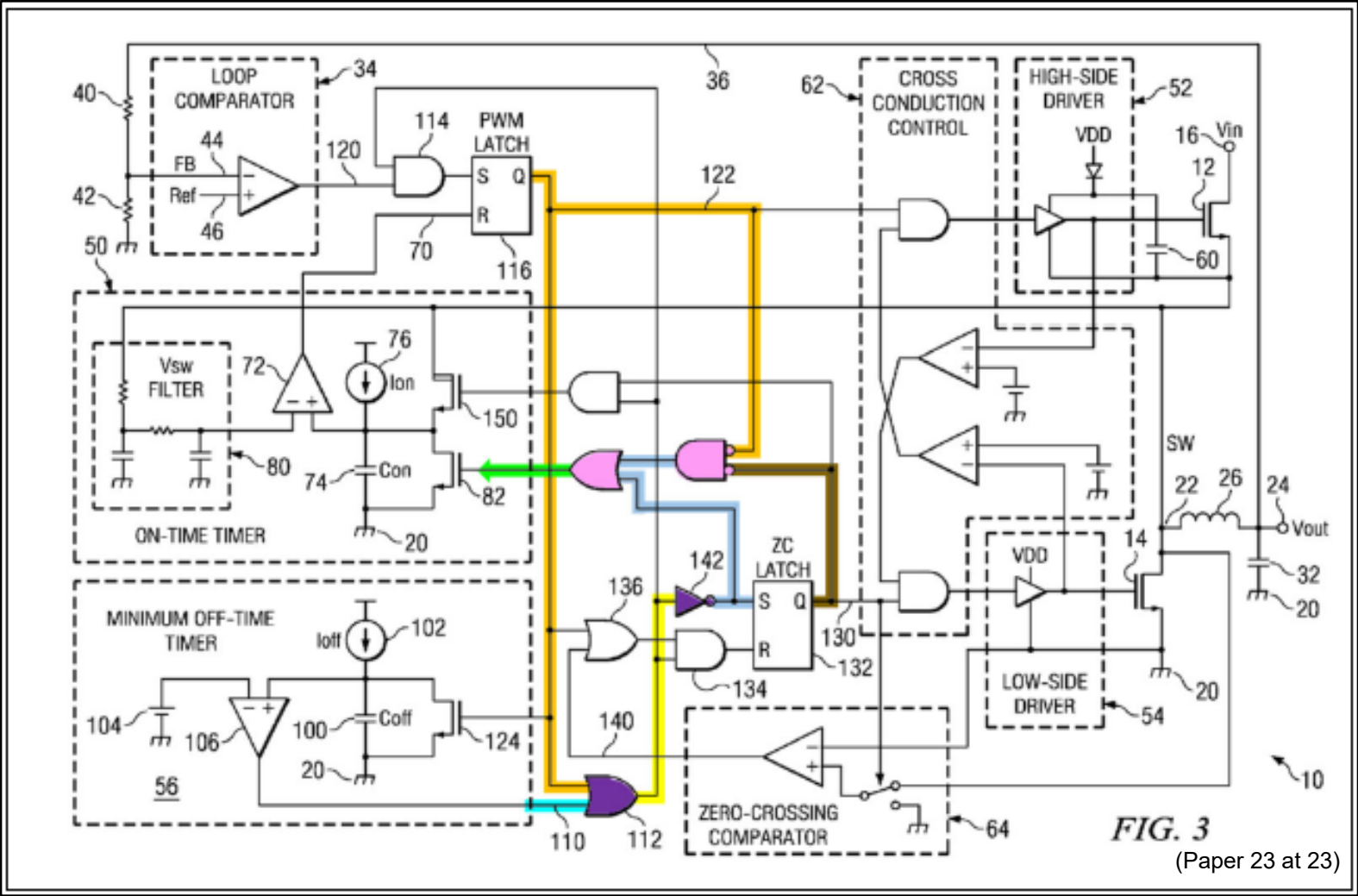
(Paper 23 at 23)

Inconsistent Identification

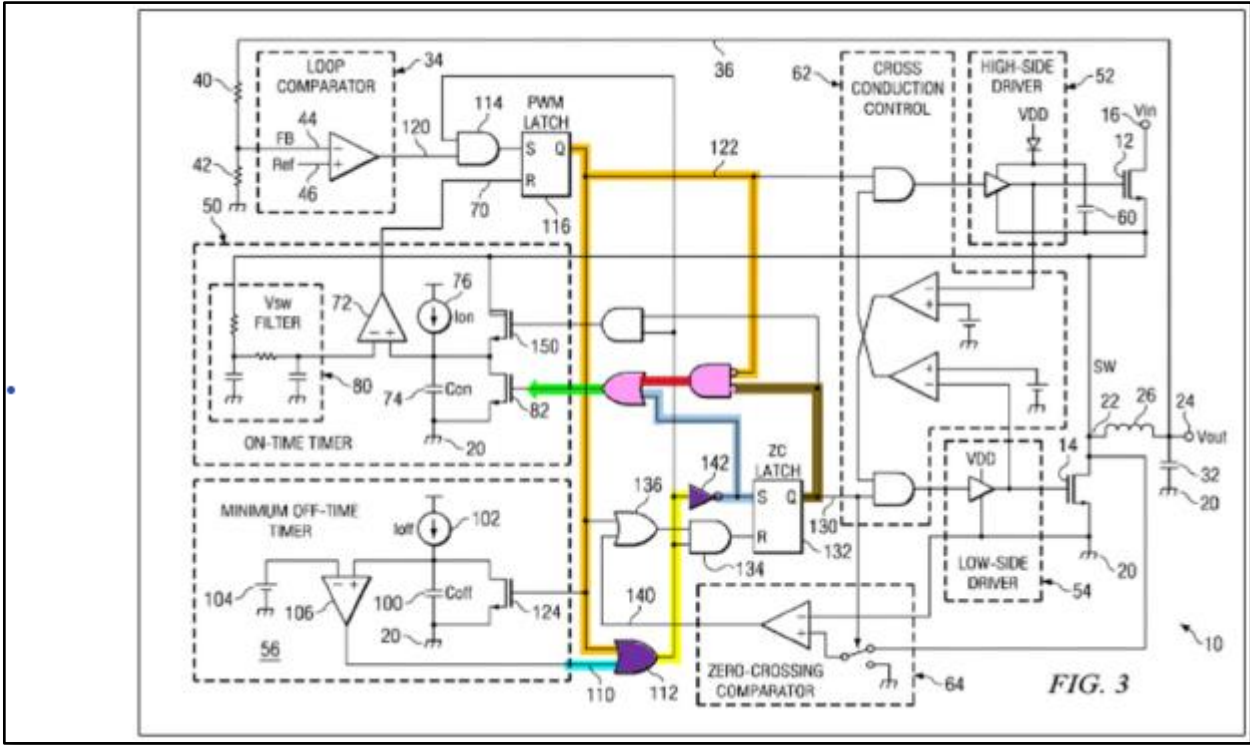
Intervening Logic

Petitioner's Identification for 1[D]

Petitioner's Identification for 1[B2]



Not the Same Signal



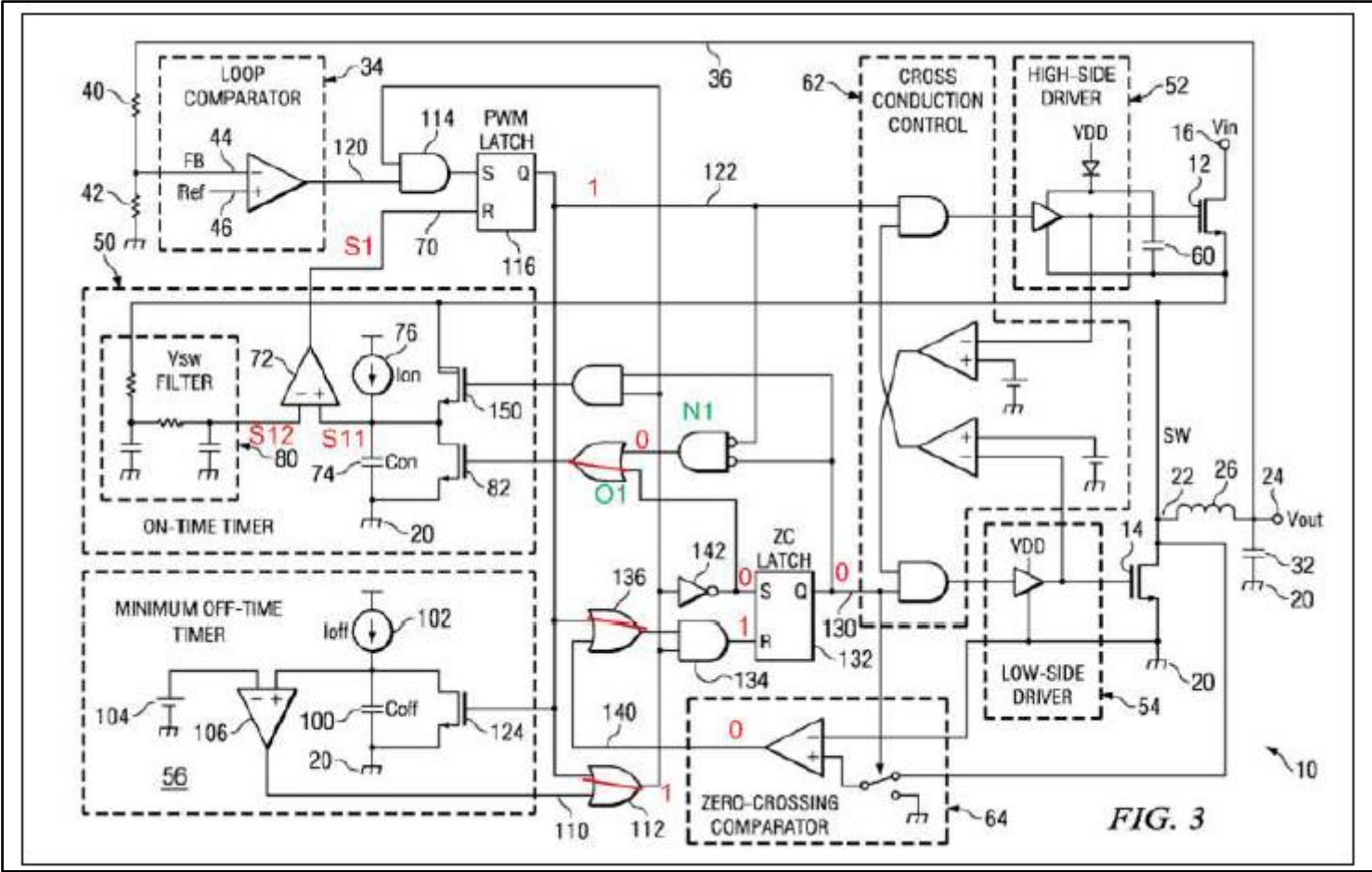
(Paper 23 at 27 (citing EX2005 at ¶ 83))

When Orange (1[D]) is “0”
Green (1[B2]) is “0” or “1”

Orange	Brown	Red	Blue	Green	Aqua	Yellow
0	1*5	0*	1	1	0	0
0	0	1	0*	1	1	1
0	1	0	0	0	1	1
1	0	0	0	0	0*	1
1	1	0	0	0	0*	1
1	0	0	0	0	1*	1

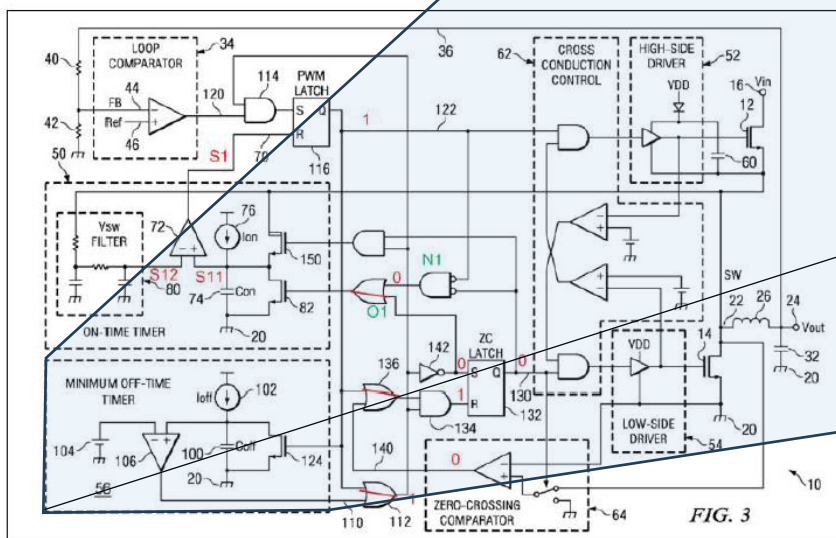
(Paper 23 at 28 (citing EX2005 at ¶ 83))

Petitioner's Logic

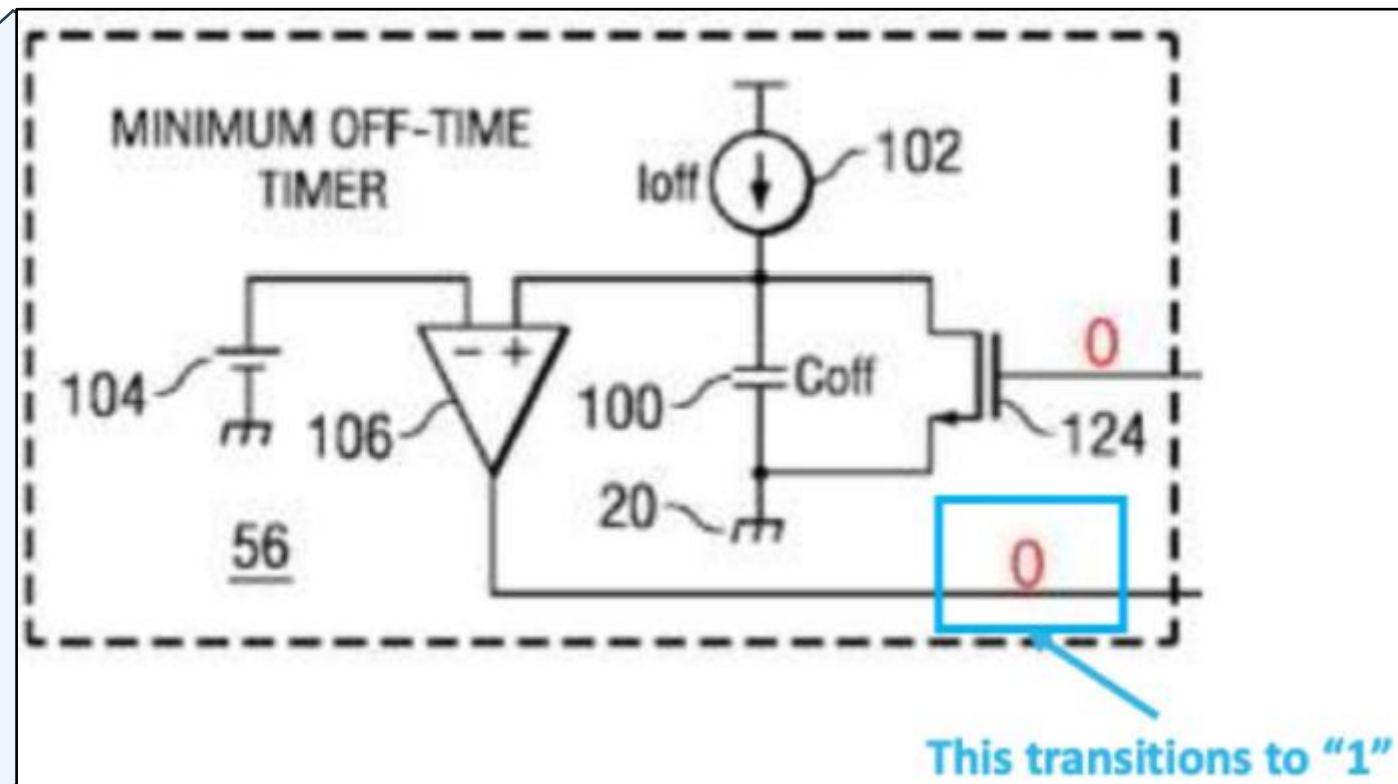


(EX1016 at ¶ 27)

Gap in Petitioner's Logic



(EX1016 at ¶ 27)



(Paper 31 at 6 (Citing EX1016 at ¶ 29))

This also turns off the discharging transistor 124 in the minimum off-time timer 56, allowing the capacitor Coff 100 to be charged by the reference current source 102. This also turns

(EX1005 at 7:58-60)

Gap in Petitioner's Logic

11 Paragraph 38, I can -- I understand your
12 criticism to be that Aqua can be 1 and at other times 0;
13 and Row 6 only considers the situation where Aqua is 1.
14 Is that a fair assessment?

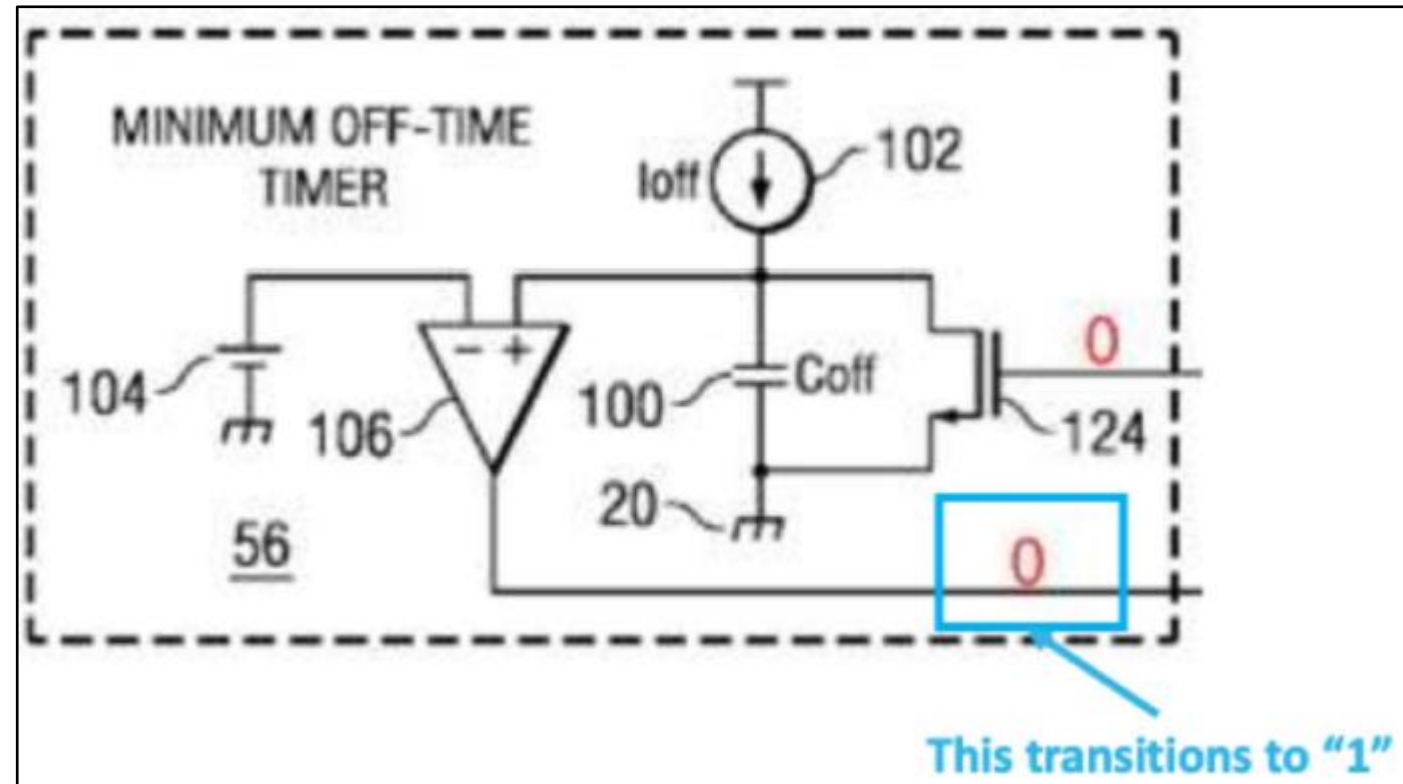
15 A Let me say it another way. With my word, when
16 orange is 1, Transistor 124 is on driving the noninverting
17 input Comparator 106 to 0, which results in the Aqua
18 signal being a 0. So in order for the Aqua signal to be a
19 1, orange must first go to 0; and then sometime later, via
20 the charging of Current Source 102 into Capacitors 100,
21 the noninverting input of 106 rises, causing the
22 comparator to trip, driving the Aqua signal to a 1; but
23 that can't happen when the orange signal is a 1.

(EX2007 at 30:15-23)

4 So when 122 Q output of PWM latch was a
5 0 -- was a 1 and it goes to 0, what happens?

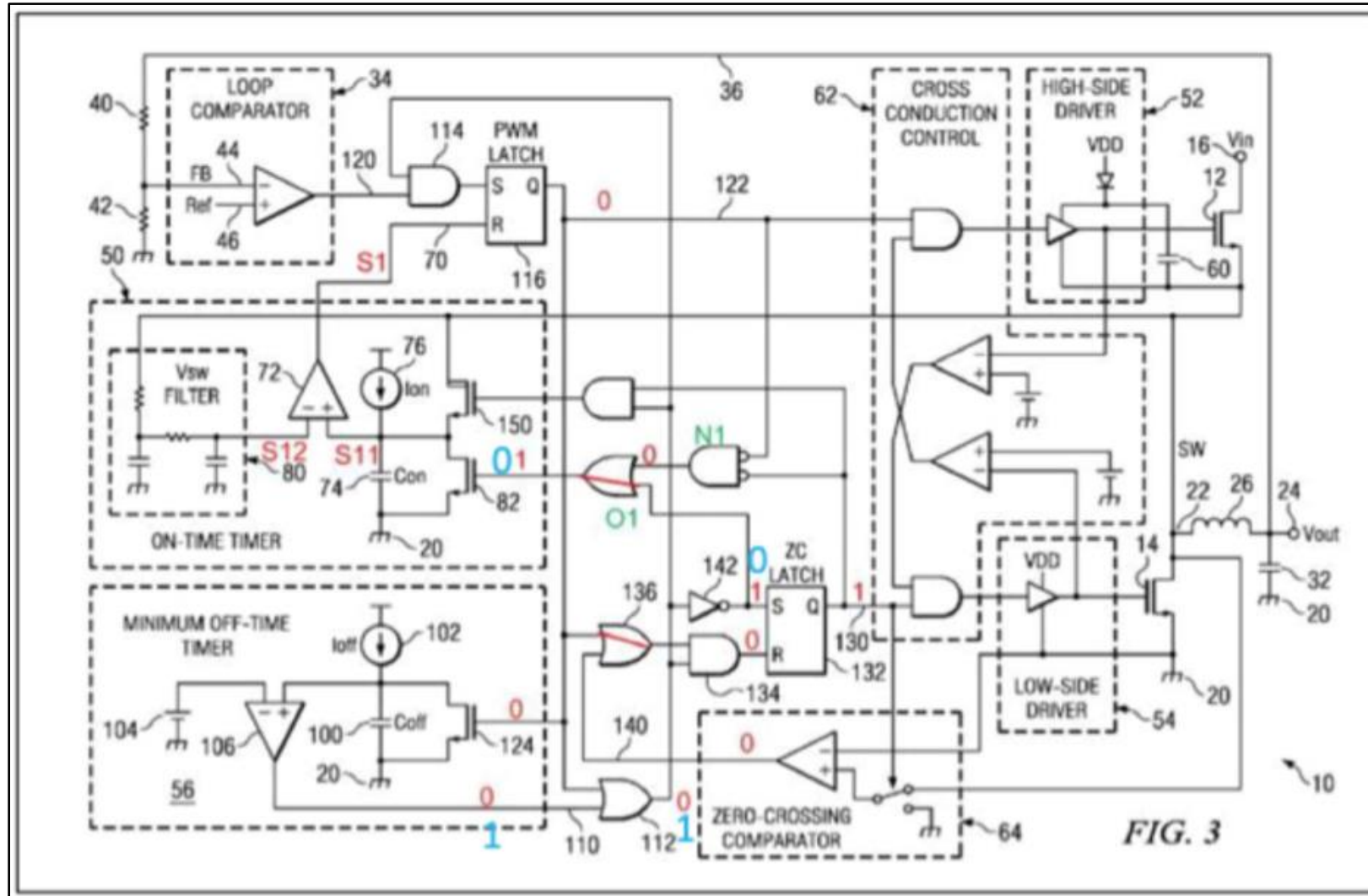
6 Okay. Several things happen. Transistor
7 124 turns off, allowing the current 102 to charge
8 Coff. And so that's just -- set that aside. If I

(EX2006 at 47:4-8)



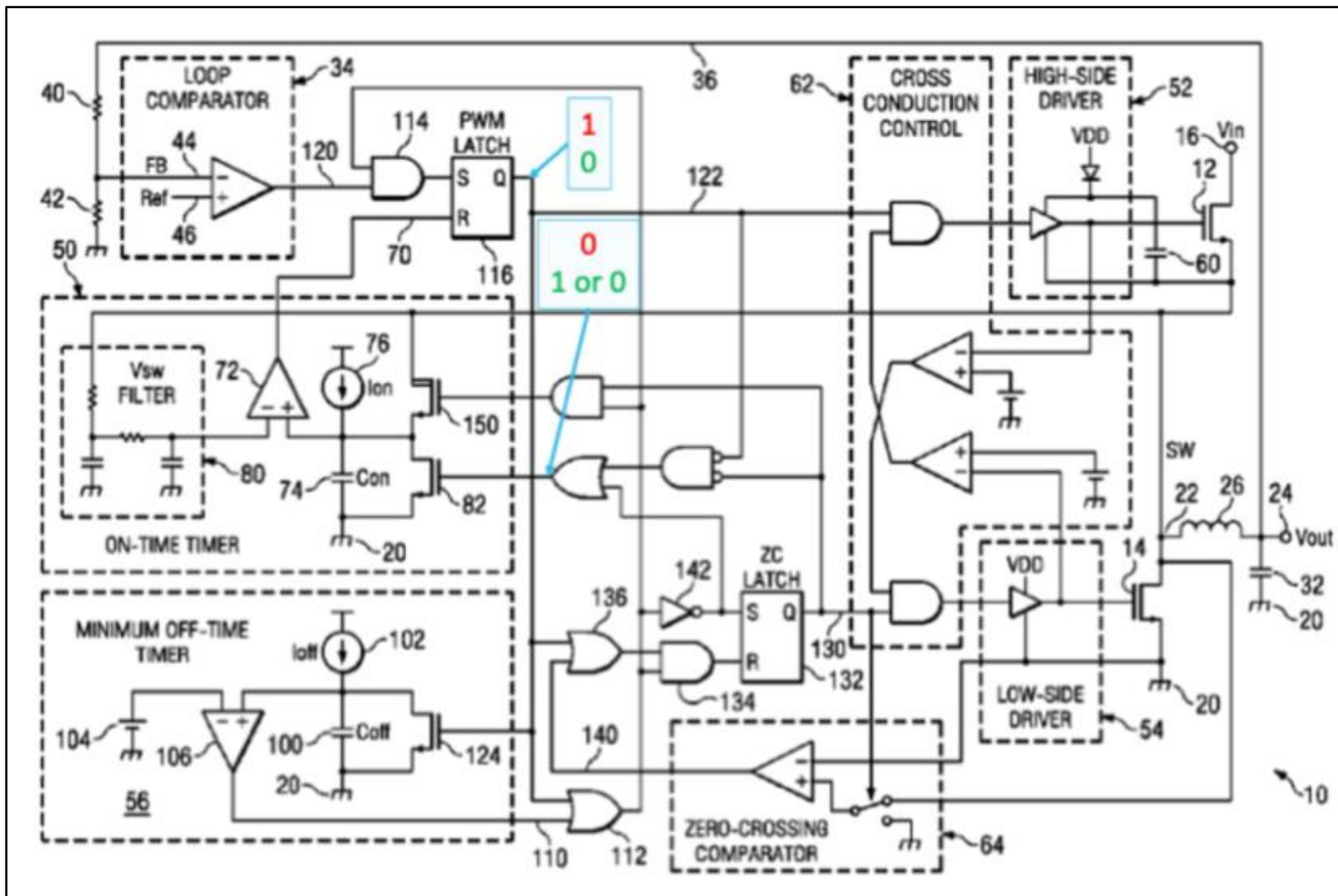
(Paper 31 at 6)

Gap Filled



(Paper 31 at 7)

Not the Same Signal

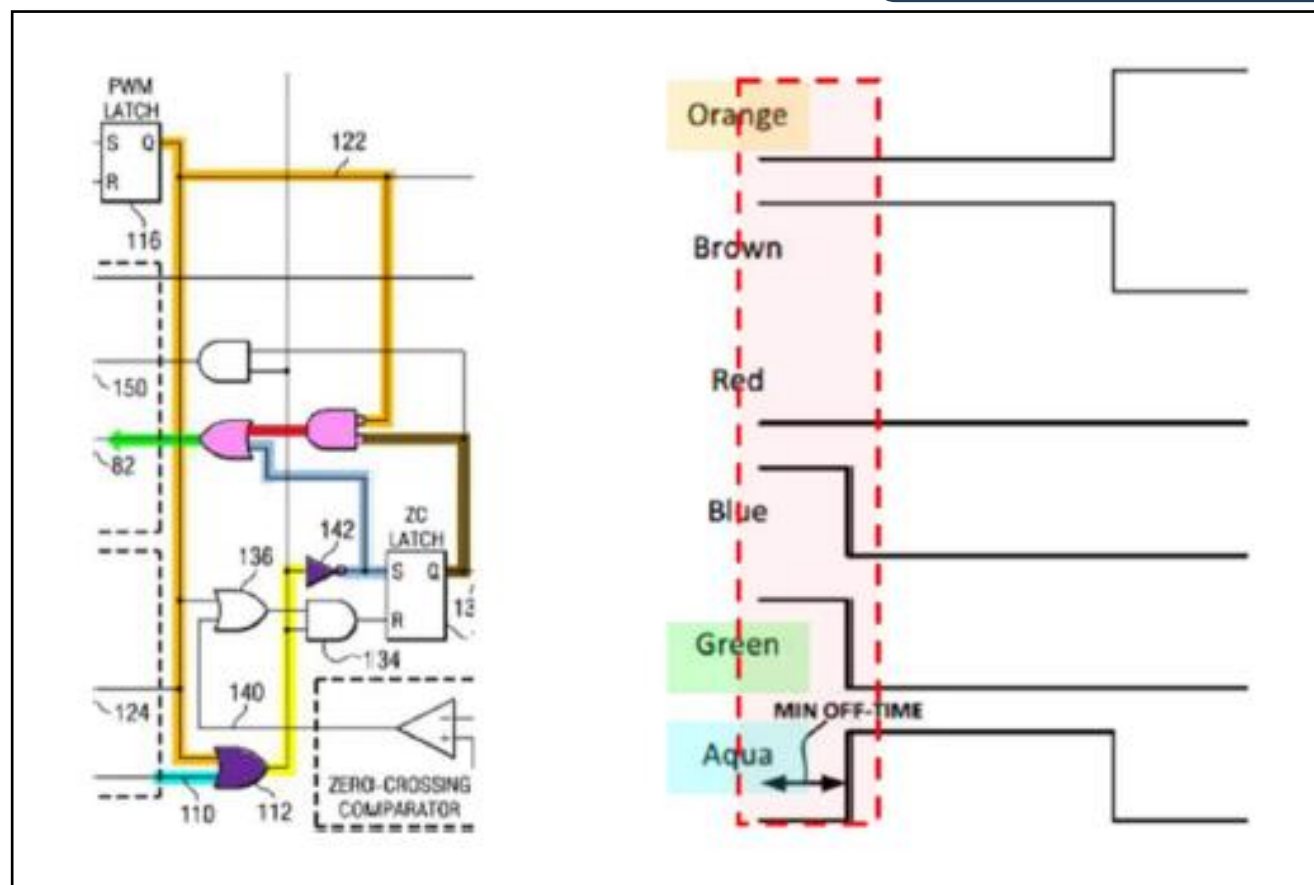


(Paper 31 at 14)

Not the Same Signal

Petitioner's Expert's Timing

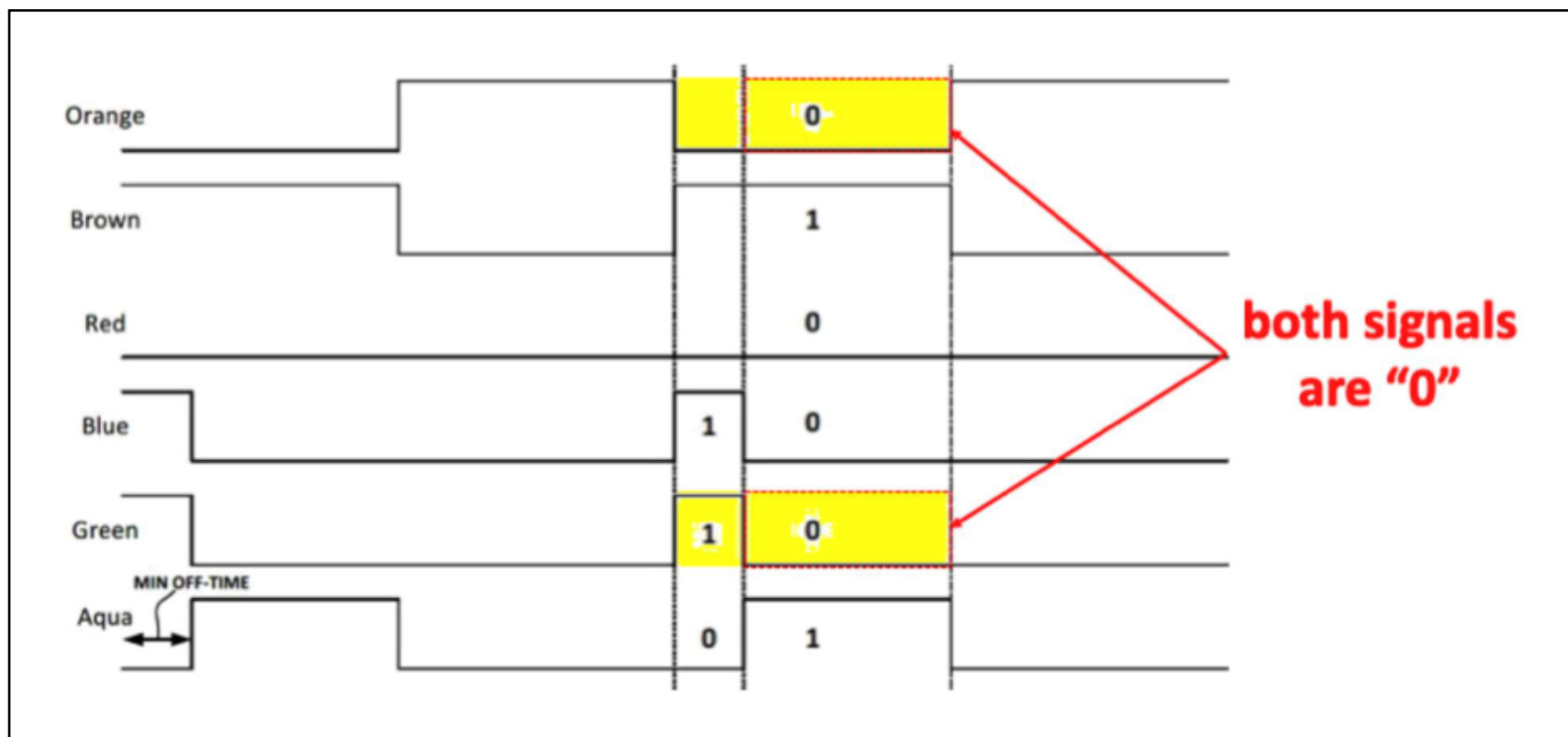
When Orange (1[D]/18[E]) is "0"
Green (1[B2]/18[A]) is "0" or "1"



Not the Same Signal

Petitioner's Expert's Timing

When Orange (1[D]/18[E]) is "0"
Green (1[B2]/18[A]) is "0" or "1"



(Paper 31 at 8 (citing EX1016 at ¶ 34))

Petitioner Did not Consider Zero Crossing

16 Q Okay. And if you could look at paragraph 29
17 where you have a -- a diagram describing PWM latch 0,
18 would there be a scenario where PWM latch outputs a 0 and
19 zero-crossing comparator outputs a 1?

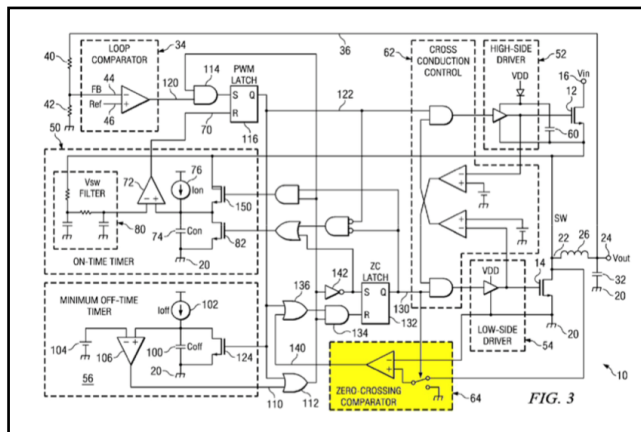
20 A Yes.

(EX2007 at 20:16-20.)

11 Q Okay. How would the zero-crossing comparator
12 being 1 affect the timing diagram that you display on
13 paragraph 34?

14 A I didn't consider that case. I'd have to go back
15 and analyze it under that situation.

(EX2007 at 23:11-15.)



“Control Signal” – Tateishi Fails

18. A step-down regulator, comprising:

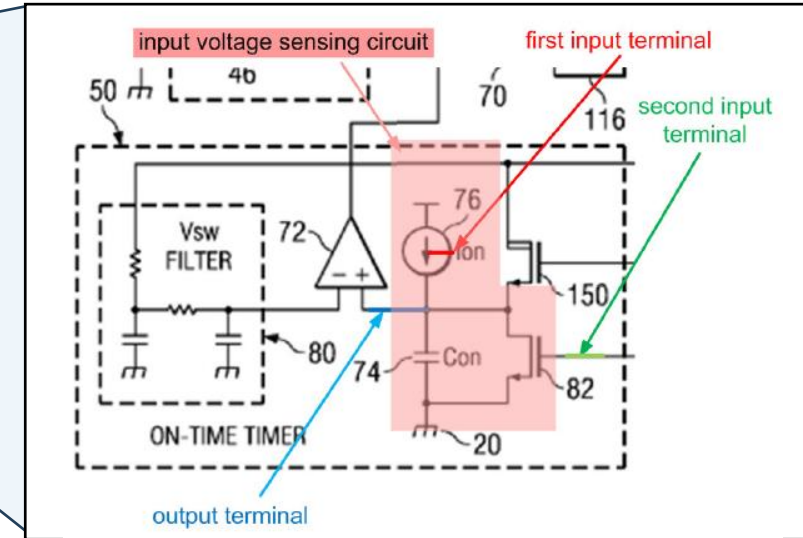
an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal wherein based on the switching signal and the control signal the on-time generator generates an on-time signal;

a minimum off time generator configured to receive the control signal and to generate a minimum off time signal in accordance with the control signal;

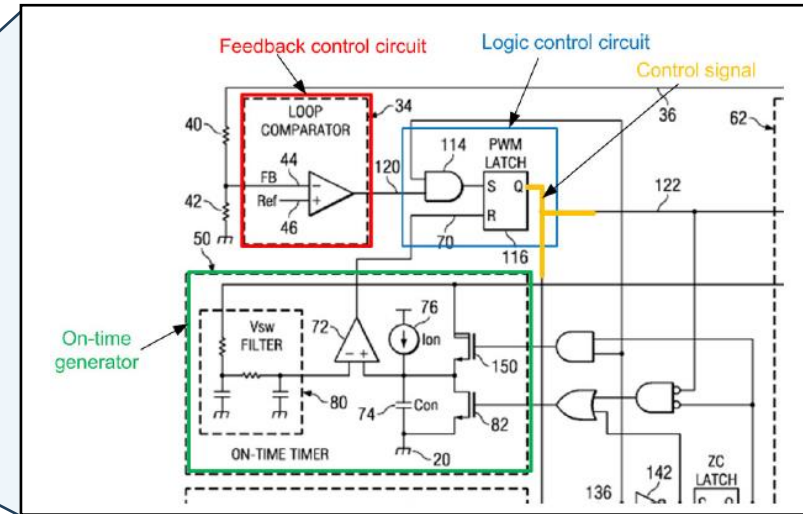
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a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal and

a power stage coupled to the output terminal of the flip-flop to receive the control signal wherein based on the control signal the power stage converts an input voltage into the switching signal.



(Paper 1 at 37, 66)



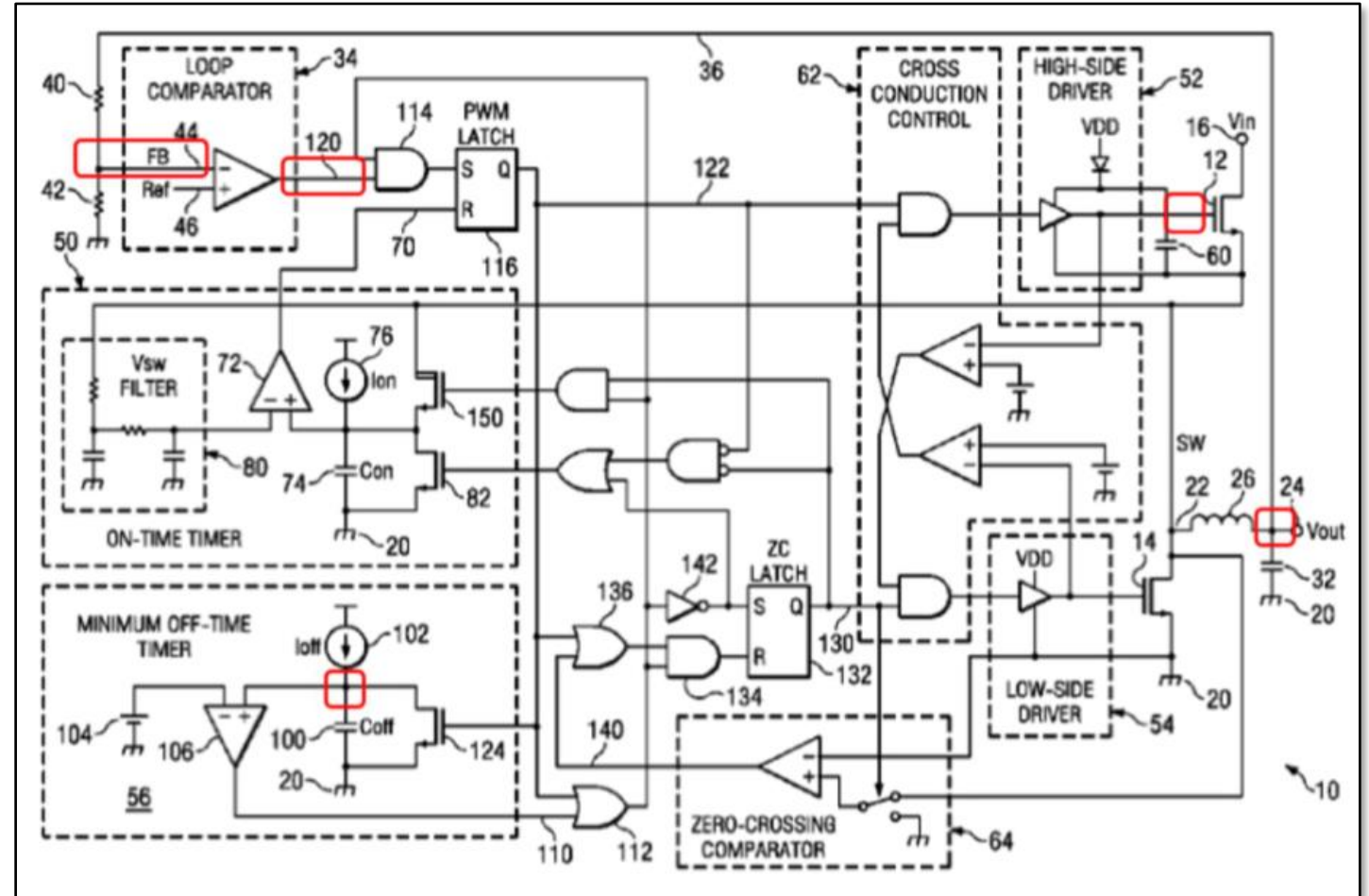
(Paper 1 at 45, 71-72)

(Paper 23 at 10)

Patent Owner's Demonstratives – Exhibit 2009 (Not Evidence)

“Control Signal” – Tateishi Fails

- b. Limitation 18[A]: an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal;
- c. Limitation 18[B]: a minimum off time generator configured to receive the control signal, and to generate a minimum off time signal in accordance with the control signal;
- d. Limitation 18[C]: a comparator configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to receive a reference signal and wherein based on the feedback signal and the reference signal, the comparator generates a comparison signal;
- e. Limitation 18[D]: an and-gate coupled to the comparator and the minimum off time generator to receive the comparison signal, and to receive the minimum off time signal, wherein based on the comparison signal and the minimum off time signal, the and-gate generates an output signal;
- f. Limitation 18[E]: a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal; and
- g. Limitation 18[F]: a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal, the power stage converts an input voltage into the switching signal.



(Paper 31 at 16)

“Control Signal” – Tateishi Fails

18. A step-down regulator, comprising:

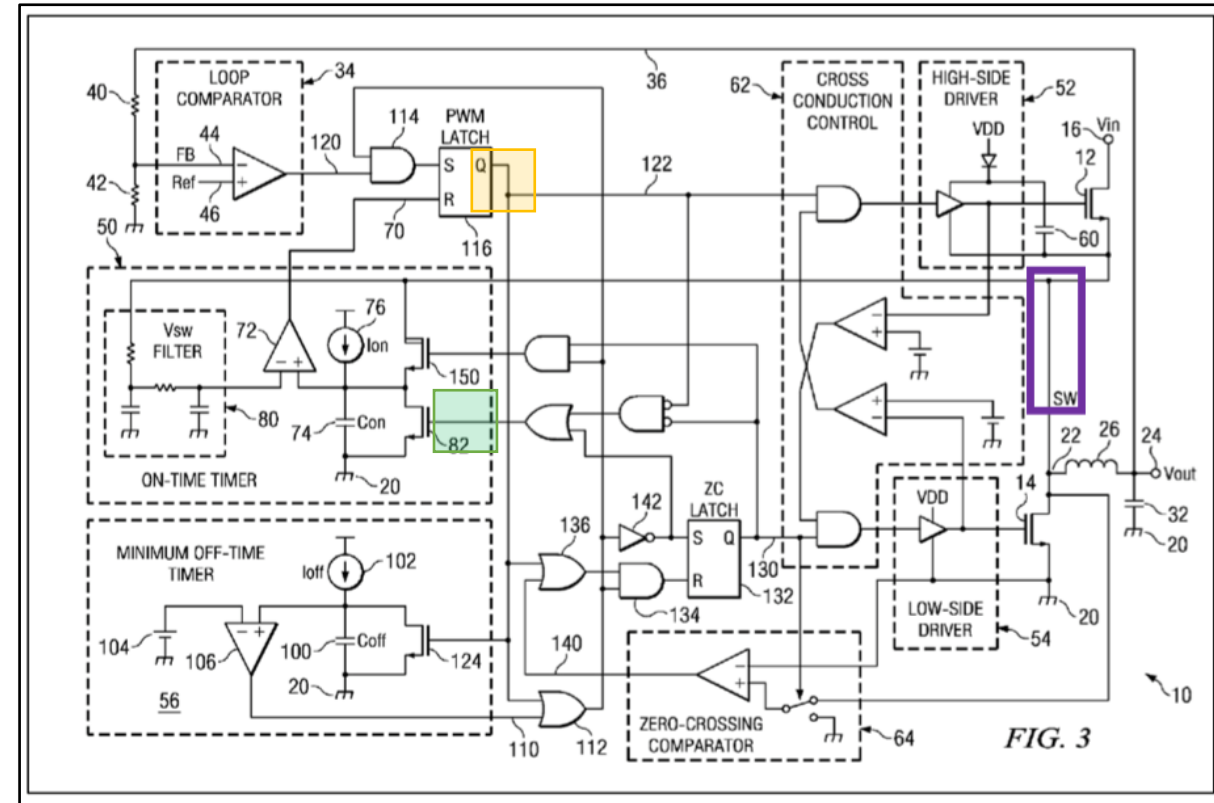
an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal;

a minimum off time generator configured to receive the control signal, and to generate a minimum off time signal in accordance with the control signal;

•
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•

a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal; and

a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal, the power stage converts an input voltage into the switching signal.



(Paper 23 at 27, 31)

Claim Construction

“Control Signal” - “two state signal”

Patent Owner’s Construction

“control signal” is a “logic signal with two distinct states”

(Paper 23 at 7)

Patent Owner’s Construction

The Term “Control Signal” Should be Construed in Accordance With its Plain and Ordinary Meaning as a “Signal Configured to Control a Circuit Component”

(Paper 26 at 6)

Claims Require a Control Signal

18. A step-down regulator, comprising:

an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal the on-time generator generates an on-time signal;

a minimum off time generator configured to receive the control signal and to generate a minimum off time signal in accordance with the control signal;

•
•
•

a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal and

a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal the power stage converts an input voltage into the switching signal.

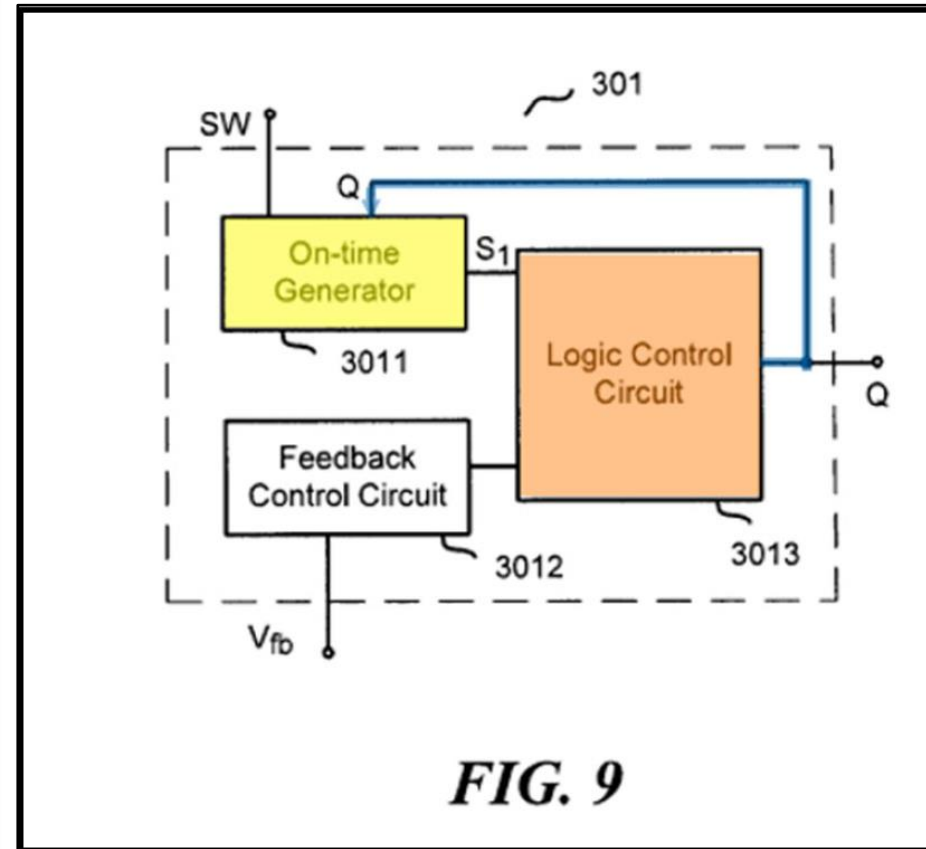


FIG. 9

Logic signal with two distinct states

Petitioner's Expert Agrees

11 Q Back to the claim language. 10 5 through 9
12 states that "the logic control circuit generates a
13 control signal."

14 You see that?

15 A Yes.

16 Q Do you understand the control signal that
17 is generated to be a two-state signal?

18 MR. DEVKAR: Objection. Form.

19 THE WITNESS: Yes.

(EX2006 at 22:11-19)

10 Q If you could look at the control signal in
11 column -- hold on. Let me see -- 14, lines 19 to
12 20. It says:

13 "The flip-flop generates the control
14 signal."

15 A Yep, I see that.

16 Q In your opinion, is the control signal of
17 claim 18 a two-state signal?

18 A Yes.

(EX2006 at 25:10-18)

Logic signal with two distinct states

19 If I understand you correctly, you're
20 stating that the signal Q from the logic control
21 circuit is a two-state signal?

22 MR. DEVKAR: Objection. Form.

1 THE WITNESS: Well, at one point in the
2 patent, which is column 8, starts in line, like,
3 27-ish and goes all the way down mostly to the end
4 of that column.

5 But it says:

6 "The on-time signal S1 resets the
7 flip-flop 4013 to change the control
8 signal Q into a logic low (Q=0). Thus,
9 the high-side switch Q1 is turned off,
10 and the low-side switch Q2 is turned on,
11 the switching signal SW equals to 0."

12 And so that's one instance where it's
13 showing the Q output state with respect to the Q2
14 switch.

15 Earlier, around line 43 it says:

16 "Figure 12 illustrates the waveforms
17 of the step-down regulator 40. As shown
18 in figure 11 and figure 12, when Q=1,
19 the high-side switch Q1 is turned on."

20 So the patent speaks of it in terms of
21 logical values 0 and 1. So -- but that doesn't

(EX2006 at 16:19-17:21)

Petitioner's Expert Agrees

15 Q Is the signal an analog or a digital
16 signal? And this is, again, referring to signal Q
17 of figure 10.

18 MR. DEVKAR: Objection. Form.

19 THE WITNESS: Well, let me see if the '377
20 characterizes itself what the Q value -- what's the
21 nature of the Q.

22 ///

1 BY MR. BOMBACH:

2 Q Please take your time to --

3 A Okay.

4 Q -- as much time as you need.

5 A Okay.

6 So the control signal Q, as I stated a
7 while ago, drives the power stage. And the power
8 stage -- although I don't recall if Q1 and Q2 of the
9 power stage are described as MOSFETs, but at -- or
10 bipolar.

11 But, at any rate, in order to turn on Q1,
12 for example, the volt -- the Q output has to be
13 large enough so that it provides enough turn-on for
14 that output transistor.

15 So, in that sense, you know, you're asking
16 is it an analog or a digital. Typically, when you
17 think about a digital signal, it's -- like in a
18 5-volt system, it's going to be -- the value's going
19 to be 5 volts or ground.

20 Of -- in this case -- so it has two states.

21 Digital signals typically have two states, one of
22 two states.

(EX2006 at 14:15-15:22)

Logic signal with two distinct states

3012 and a logic control circuit 3013. The on-time generator 3011 receives a switching signal SW provided by a step-down regulator and a control signal Q provided by the PCOT control circuit 301, and generates an on-time signal S_1 . The

(EX1001 at 7:44-47)

As shown in FIG. 11, the on-time generator 4011 receives the switching signal SW provided by the step-down regulator 40 and the control signal Q provided by the flip-flop 4013, and

(EX1001 at 8:28-30)

stage 502. The on-time generator 5011 receives a switching signal SW provided by the regulator 50 and a control signal Q provided by the flip-flop 5013, and provides an on-time signal

(EX1001 at 8:66-9:1)

Specification describes a logic signal with two distinct states

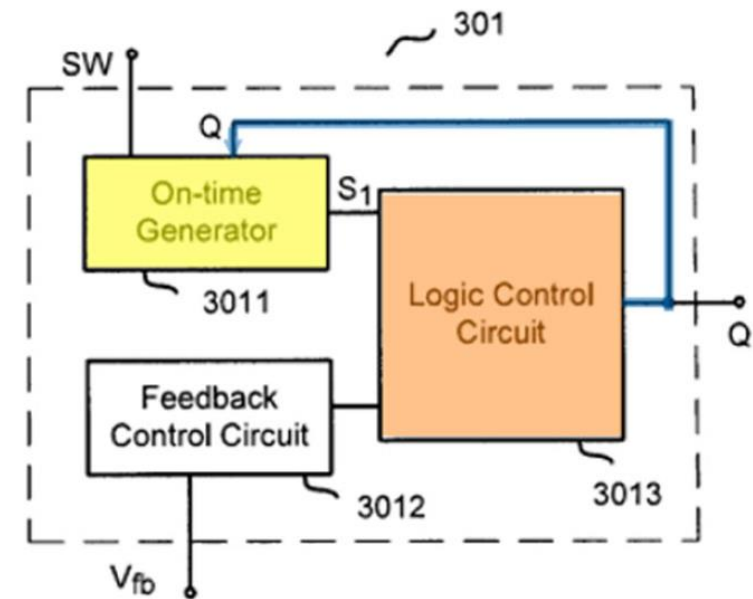
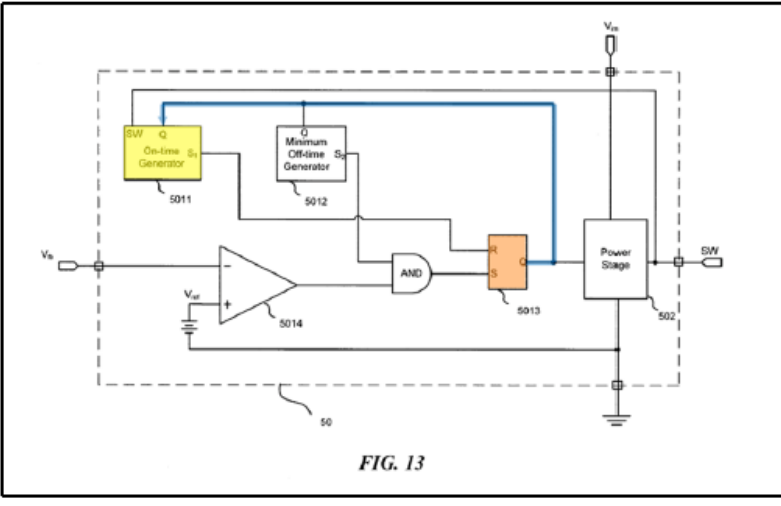
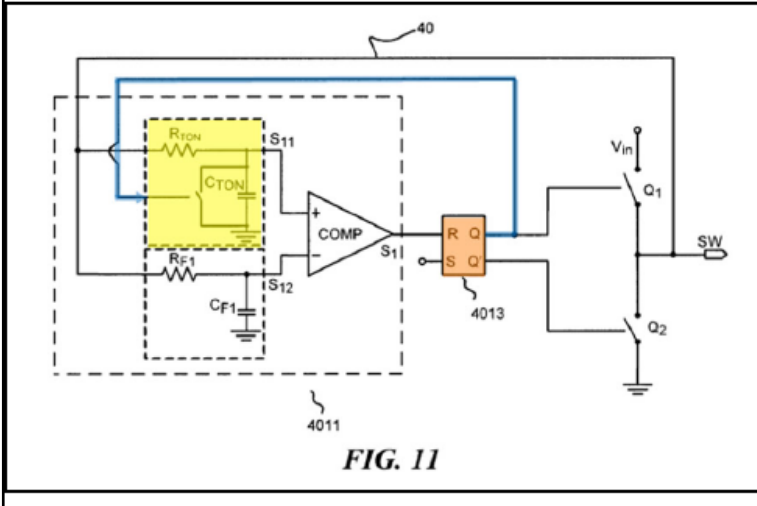
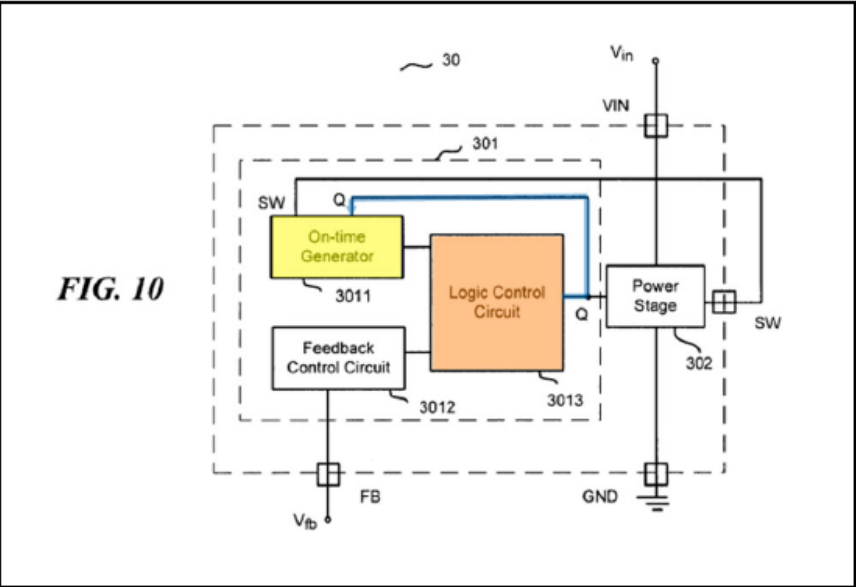
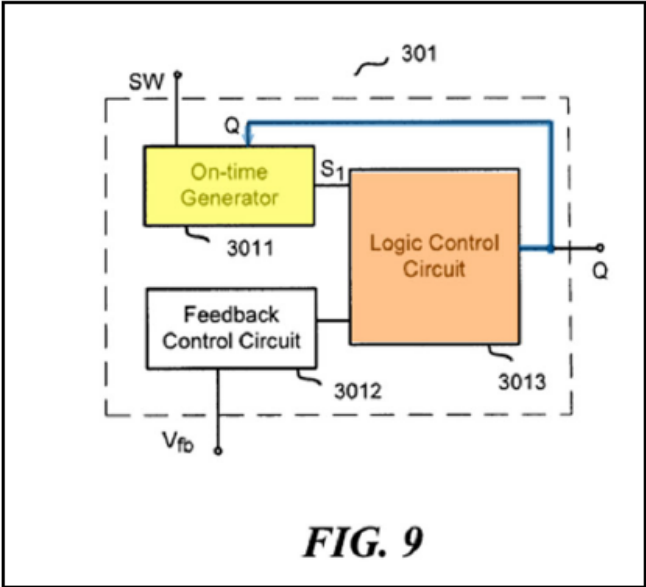


FIG. 9

(Paper 23 at 11 (citing FIG. 9))

Logic signal with two distinct states

All Embodiments



Logic signal with two distinct states

flip-flop 4013. The control signal Q controls the high-side switch Q_1 , and the complementary signal Q' of the control signal Q controls the low-side switch Q_2 . The first terminal of

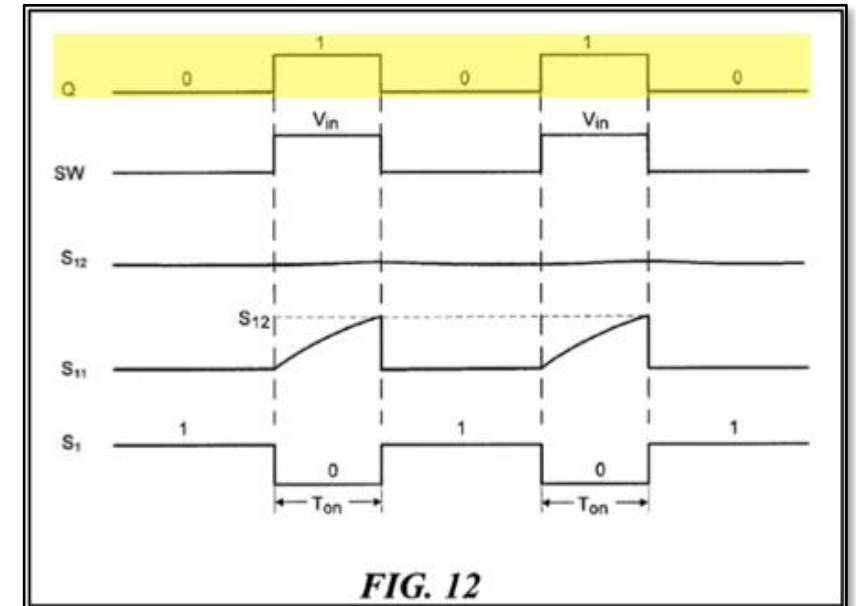
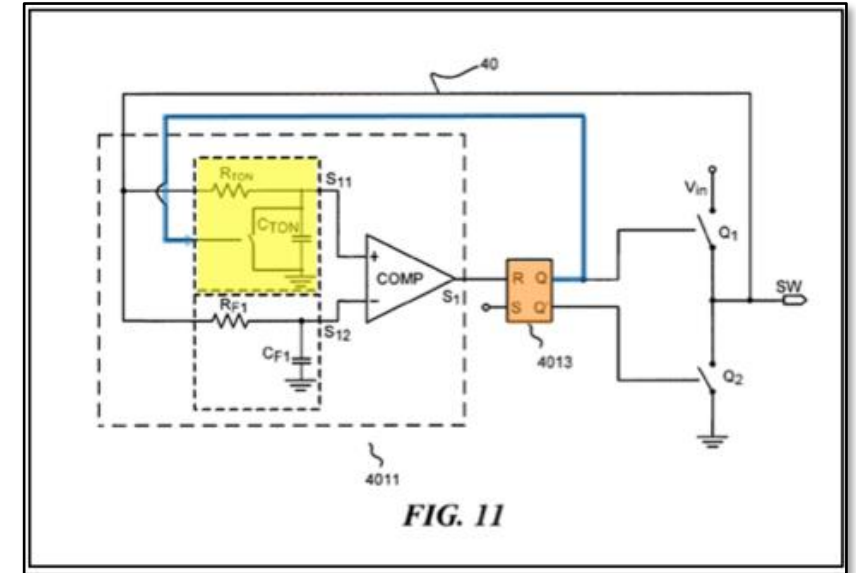
(EX1001 at 8:32-34)

lactor 40 of FIG. 11. As shown in FIG. 11 and FIG. 12, when $Q=1$, the high-side switch Q_1 is turned on, and the switching signal SW equals to the input voltage V_{in} . Meanwhile, the

(EX1001 at 8:43-45)

logical high, that is, $S_1=1$. The on-time signal S_1 resets the flip-flop 4013 to change the control signal Q into logical low ($Q=0$). Thus, the high-side switch Q_1 is turned off, and the low-side switch Q_2 is turned on, the switching signal SW equals to 0. Meanwhile, the switch K is turned on by the

(EX1001 at 8:53-57)



(Paper 23 at 12)

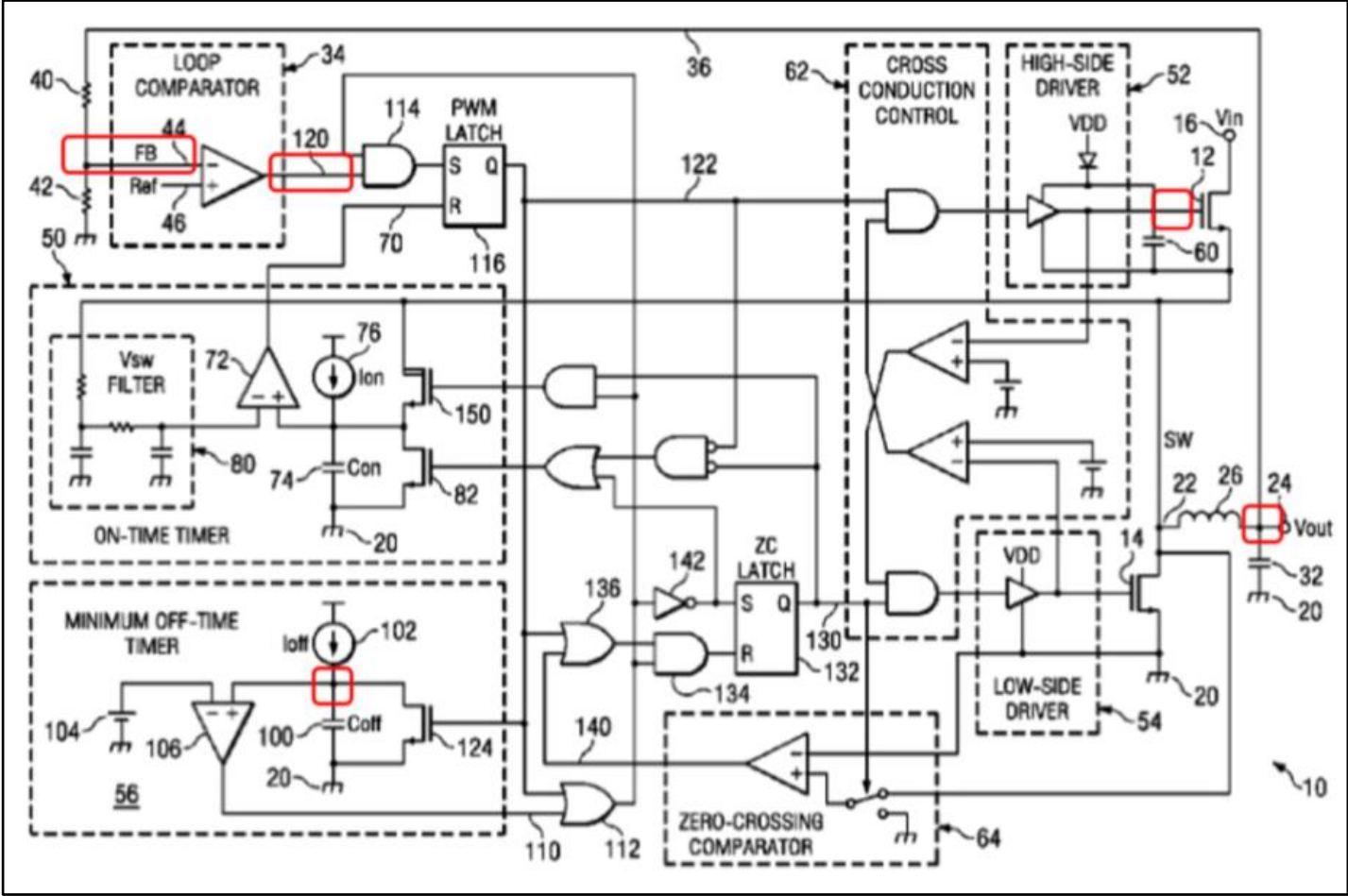
Petitioner's Construction is Wrong

- **Term:** control signal
- **Construction:** signal configured to control a circuit component

(Paper 31 at 12)

18. A step-down regulator, comprising:
an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal the on-time generator generates an on-time signal;
a minimum off time generator configured to receive the control signal and to generate a minimum off time signal in accordance with the control signal;
•
•
•
a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal and
a power stage coupled to the output terminal of the flip-flop to receive the control signal wherein based on the control signal the power stage converts an input voltage into the switching signal.

Petitioner's Application of its Construction



(Paper 31 at 16)

Petitioner's Application of its Construction

21 Q Okay. The output of Endgate 114 -- you consider
22 that to be a control signal?

23 A Well, I mean, in the broadest sense of the
24 construction that I've provided, then -- I guess I could
25 argue that any signal that controls any other device is a
1 control signal -- backing up to your first question about,
2 is 120 a control signal.

3 In the basic construction that I've given, which
4 is a signal configured to control a circuit component, you
5 know, 120, I guess, could be a control signal, as well as
6 the output of the circuit you're talking about, as well as
7 the output of Endgate 114.

(EX2007 at 11:21-12:7)

Petitioner's Expert

4 Q So in -- so would the control signal off of
5 C-off 100 be considered the same control signal going into
6 Transistor 12 under your construction?

7 A I believe so.

8 Q And then if we can look off of the top left of --
9 where it has Loop Comparator 34, which at its negative
10 terminal receives Feedback 44, which is sourced -- if you
11 could see from -- and please correct me if I'm wrong --
12 V-out 24 at the right. Do you see that?

13 A I do.

14 Q Do you consider Feedback 44 to also be a control
15 signal?

16 A Yeah. It controls the output of comparator --
17 well, it's not labeled -- the comparator and the loop
18 comparator circuit. Yes.

19 Q And then would you consider that control signal
20 to be the same control signal going into Transistor 12
21 under your construction of control signal?

22 A Yes.

(EX2007 at 16:4-22)

23 Q Looking at Figure 3 of Exhibit 1001 -- rather
24 1005 -- can you identify two control signals that you
25 would consider to not be the same control signal under
1 your construction of control signal.

2 A Ground would not be a control signal.

3 Q Okay. Any others?

4 A Well, at the -- at the beginning, you asked about
5 VDD or VCC or something; and I can't remember what I said;
6 but, I mean, normally, you wouldn't think of that as a
7 control signal.

8 Q Okay. Any others?

9 A No.

(EX2007 at 16:23-17:9)

Tateishi Fails Under Patent Owner's Construction

“Control Signal” – “logic signal with two distinct states”

18. A step-down regulator, comprising:

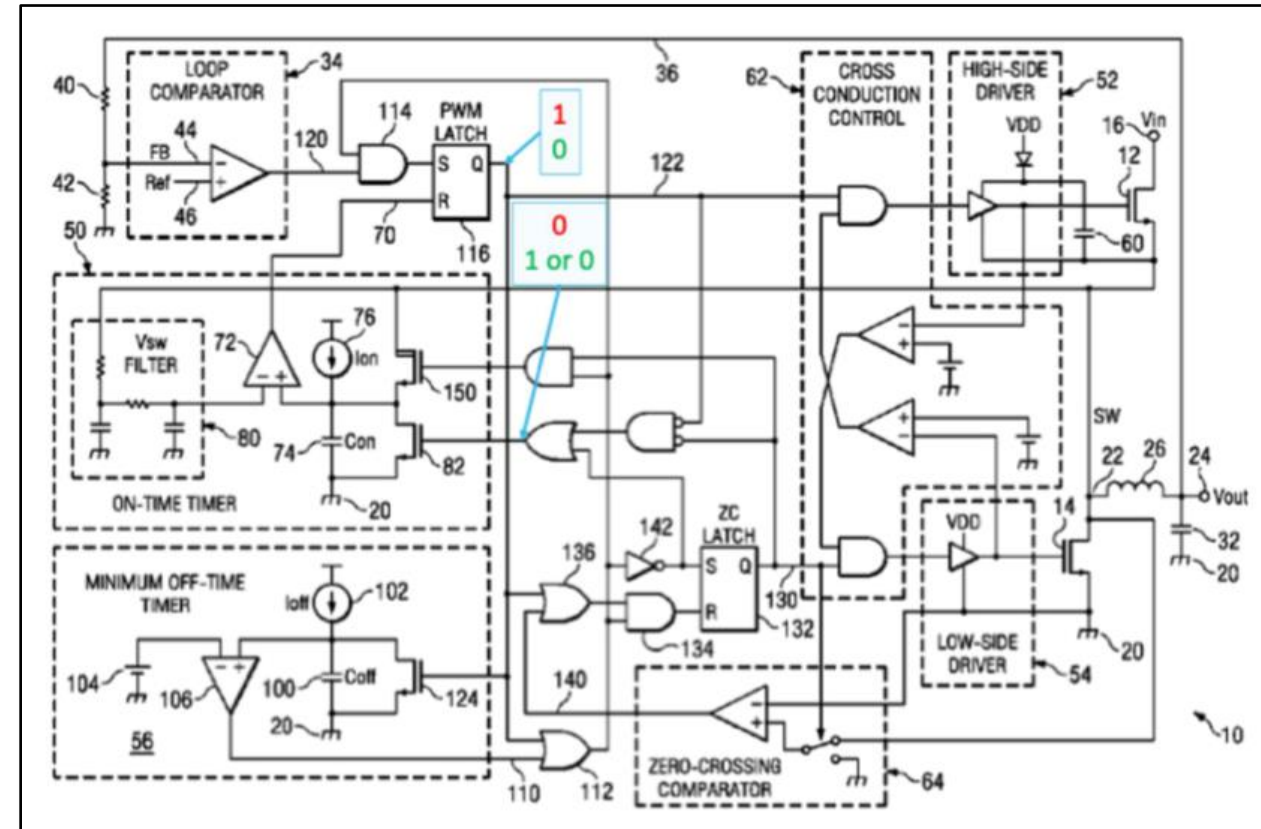
an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal the on-time generator generates an on-time signal;

a minimum off time generator configured to receive the control signal and to generate a minimum off time signal in accordance with the control signal;

•
•
•

a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal and

a power stage coupled to the output terminal of the flip-flop to receive the control signal wherein based on the control signal the power stage converts an input voltage into the switching signal.



Tateishi Fails Under
Petitioner's Construction

“Control Signal” – “signal configured to control a circuit component”

18. A step-down regulator, comprising:

an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal the on-time generator generates an on-time signal;

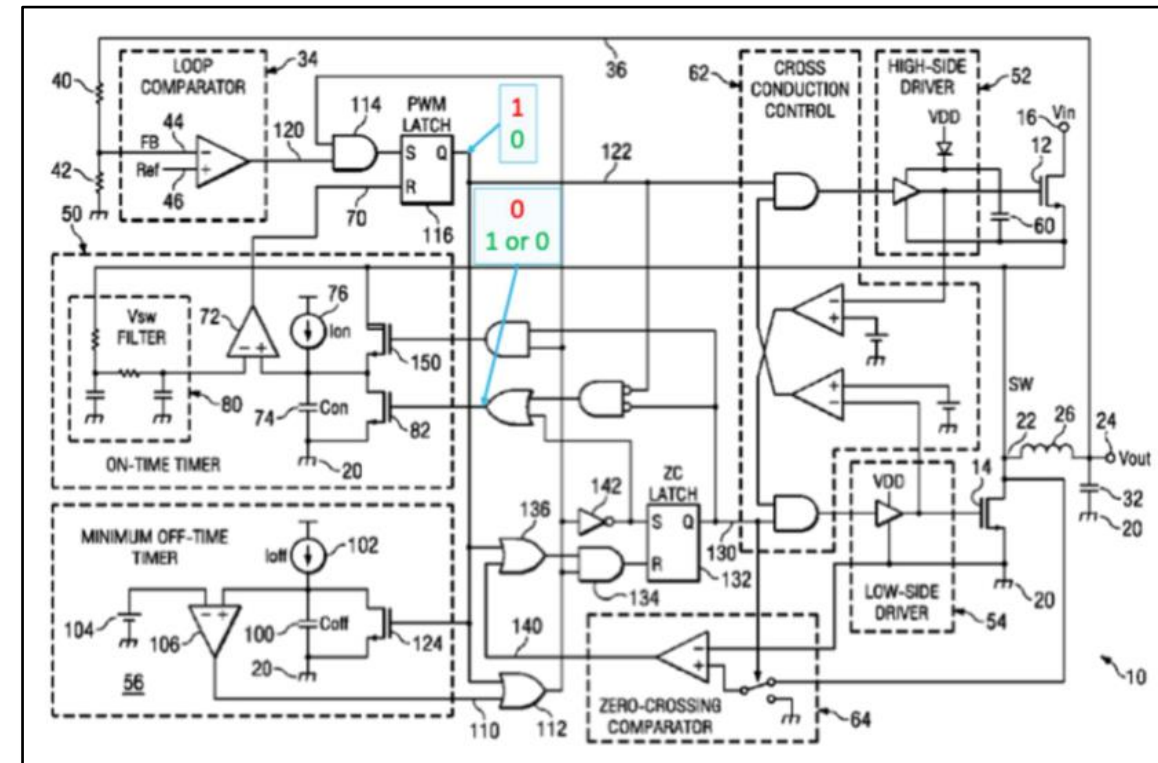
a minimum off time generator configured to receive the control signal and to generate a minimum off time signal in accordance with the control signal:

•
•
•

a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal and

a power stage coupled to the output terminal of the flip-flop to receive the control signal wherein based on the control signal the power stage converts an input voltage into the switching signal.

“a circuit component” is not controlled



“Control Signal” – “signal configured to control a circuit component”

18. A step-down regulator, comprising:

an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal the on-time generator generates an on-time signal;

a minimum off time generator configured to receive the control signal and to generate a minimum off time signal in accordance with the control signal:

•
•
•

a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal and

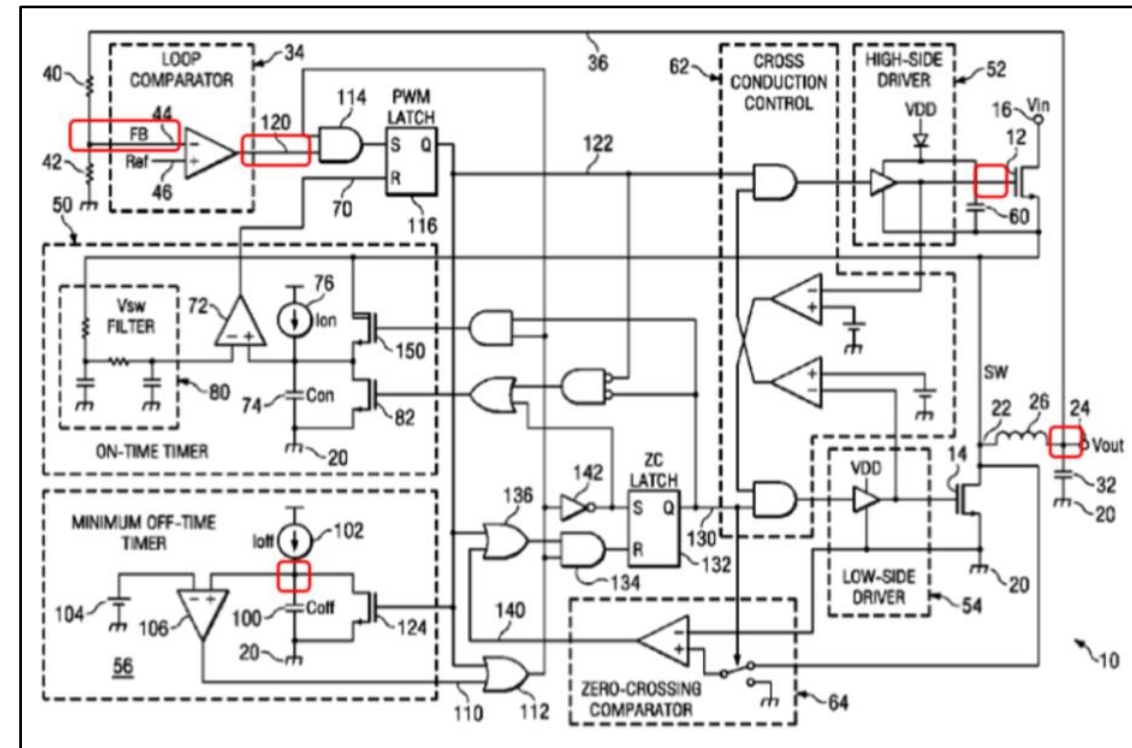
a power stage coupled to the output terminal of the flip-flop to receive the control signal wherein based on the control signal the power stage converts an input voltage into the switching signal.

(Paper 23 at 10)

Petitioner's Allegation, PWM Latch Controls Everything

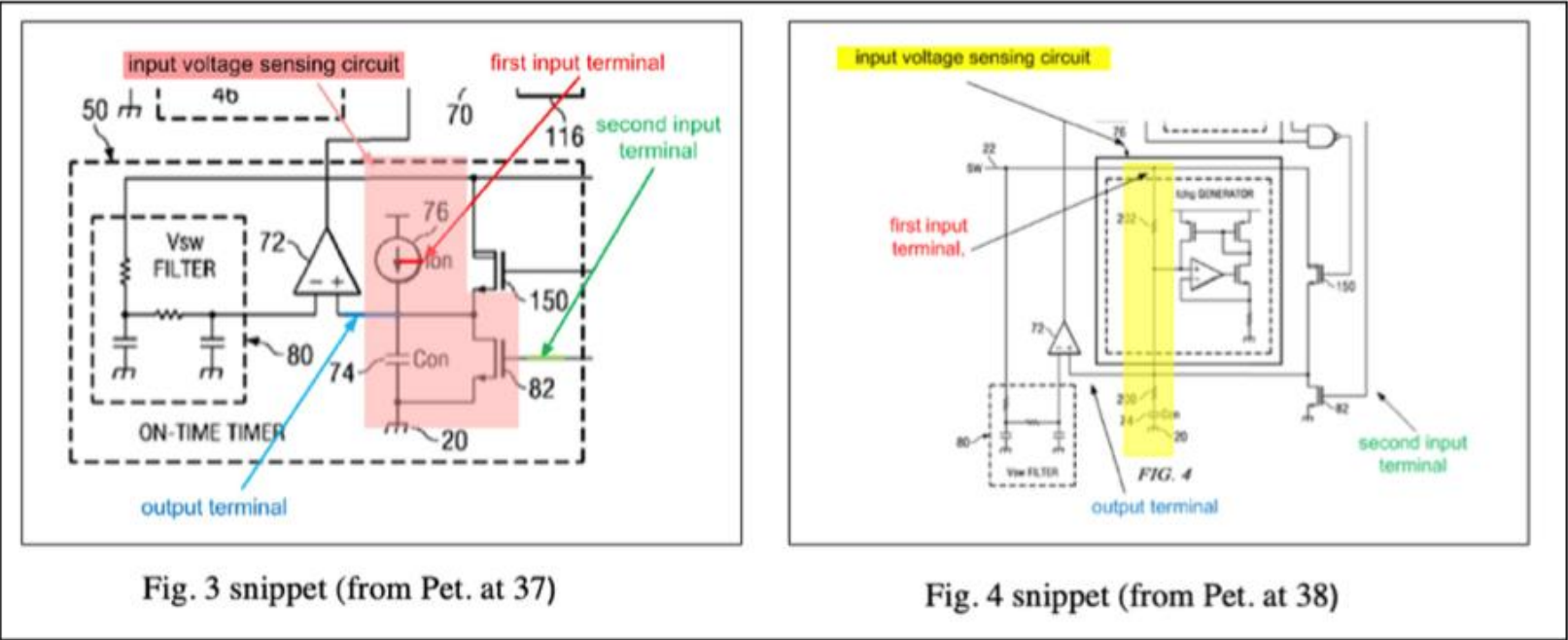
transistor 12 are all the same control signal (annotated in red, below). (*Id.*) In effect, under Petitioner's application, PWM latch generates any signal in the circuit to meet the claim phrase, because any signal is the “control signal.” Under

(Paper 23 at 10)



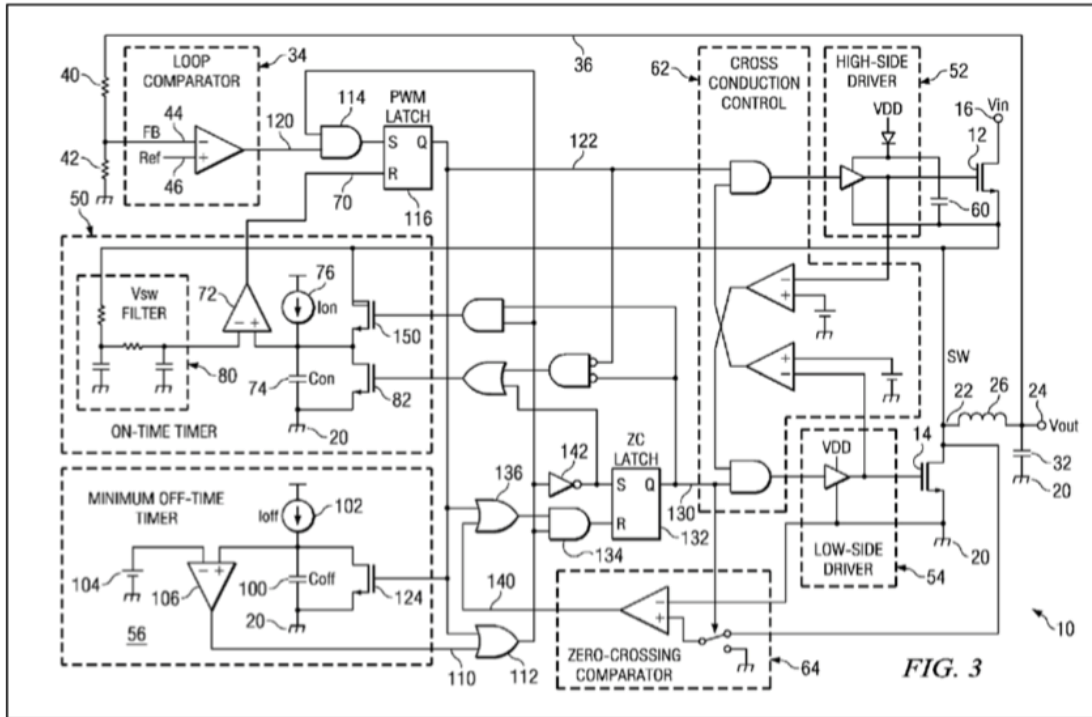
Improper Combination

Petitioner Improperly Combines

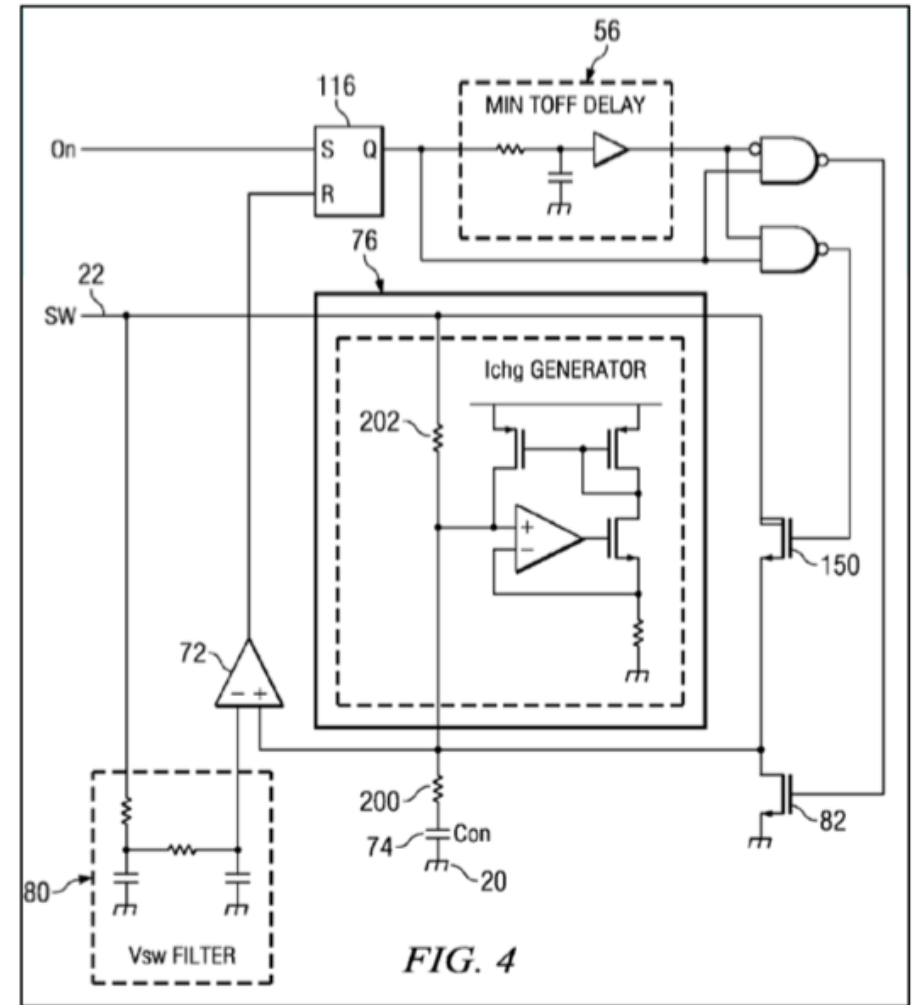


(Paper 23 at 36)

Petitioner Improperly Combines



(EX1001 at FIG. 3; see also Paper 23 at 38-40)



(EX1001 at FIG. 3; see also Paper 23 at 38-40)

[0013] FIG. 4 depicts an example of various portions of another DC to DC buck converter with a pseudo constant switching frequency.

(EX1007 at ¶ 13; see also Paper 23 at 38)

Petitioner's Allegation

Petitioner's Allegation

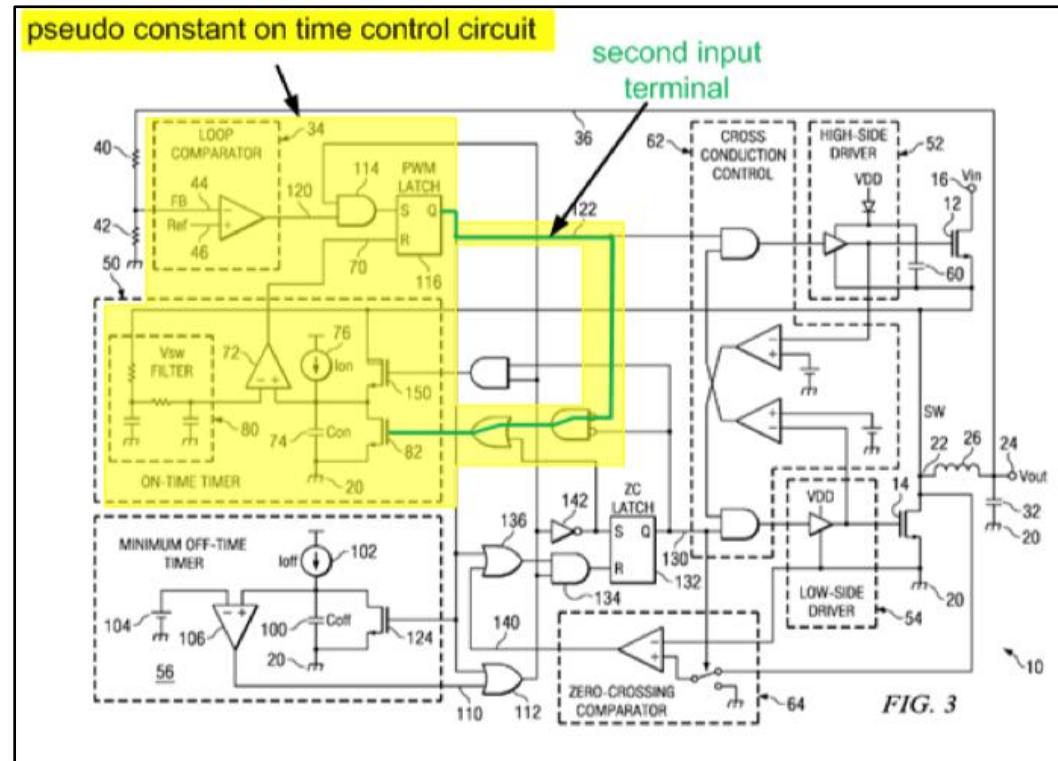
A. Ground 1: Claims 1-4, 9-14, and 17-18 are anticipated by Tateishi

As explained in greater detail in the following paragraphs, the buck-converter circuit disclosed by Tateishi is virtually identical to the recited step-down regulator and includes sub-circuits that are virtually identical to the recited pseudo constant on time control circuit and minimum off time generator.

(Paper 1 at 33)

Petitioner's Allegation – Claim 1

- b. Limitation 1[A]: a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:

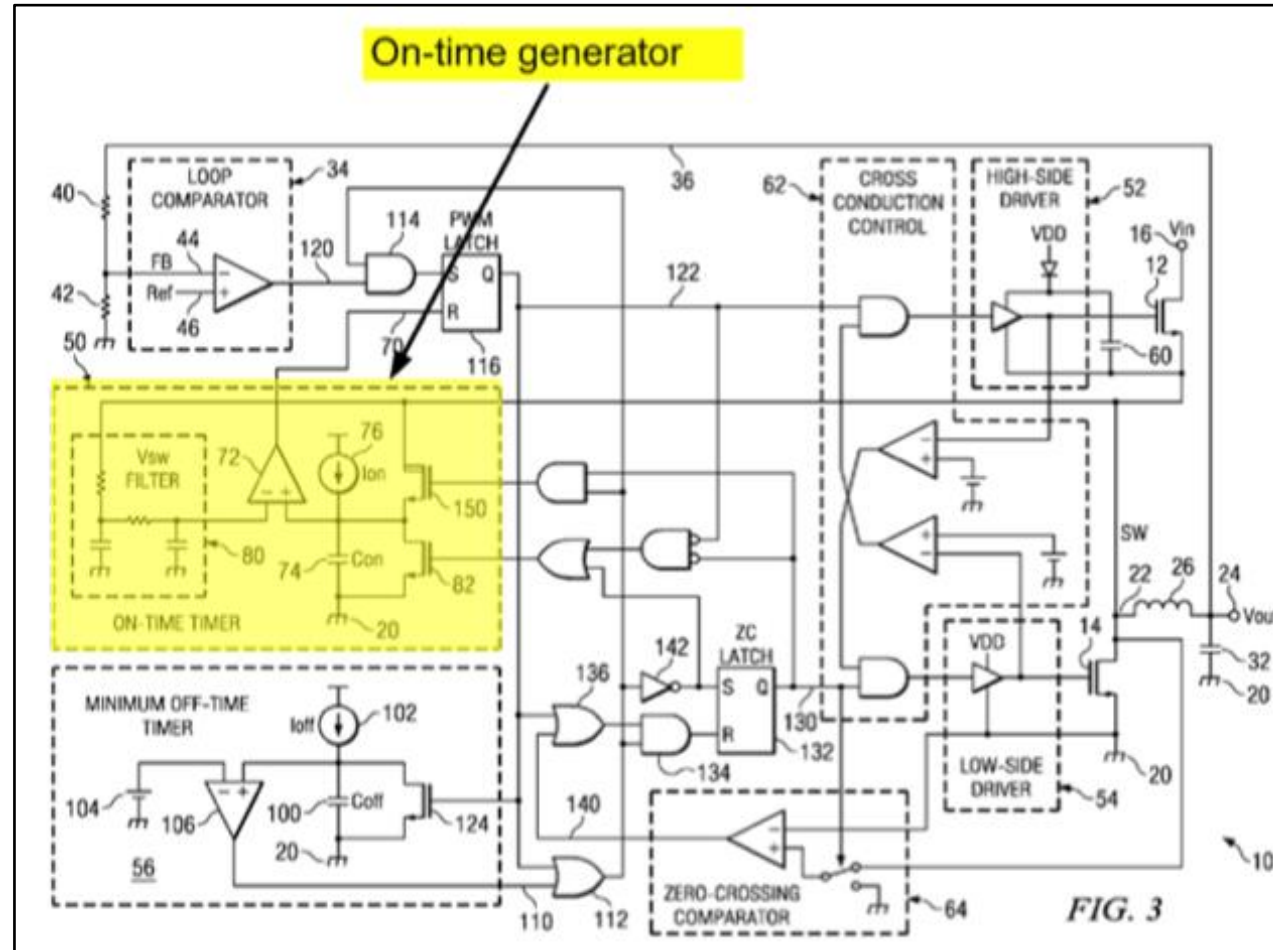


(Paper 1 at 33-34; EX005/7 at FIG. 3)

Patent Owner's Demonstratives – Exhibit 2009 (Not Evidence)

Petitioner's Allegation – Claim 1

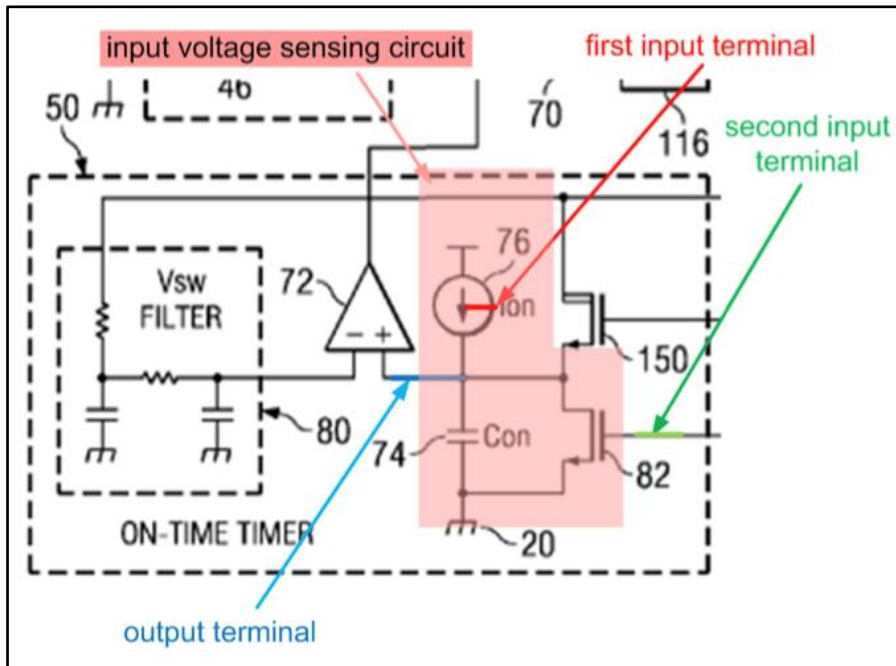
c. Limitation 1[B1]: an on-time generator comprising:



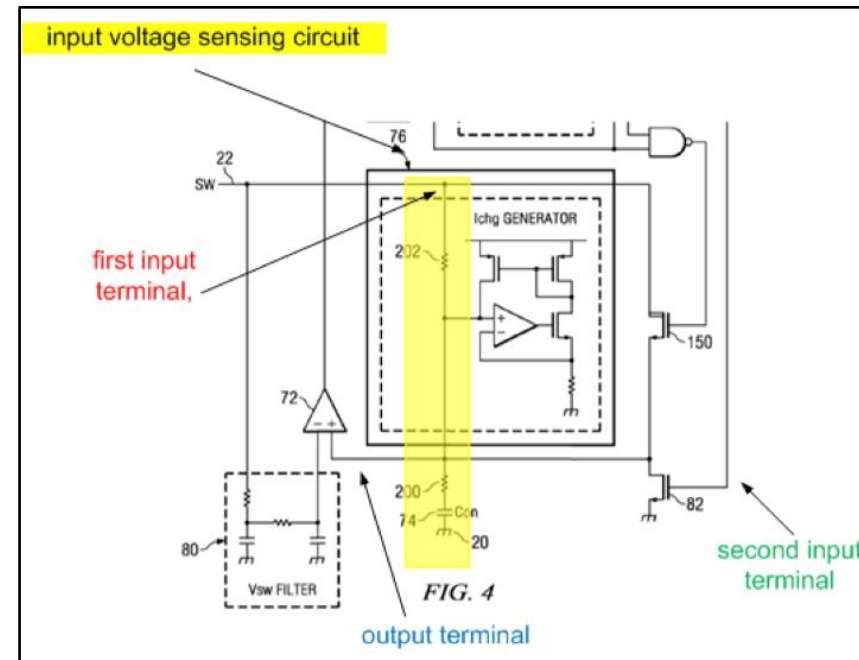
(Paper 1 at 35-36; EX005/7 at FIG. 3)

Petitioner's Allegation – Claim 1

- d. Limitation 1[B2]: an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;



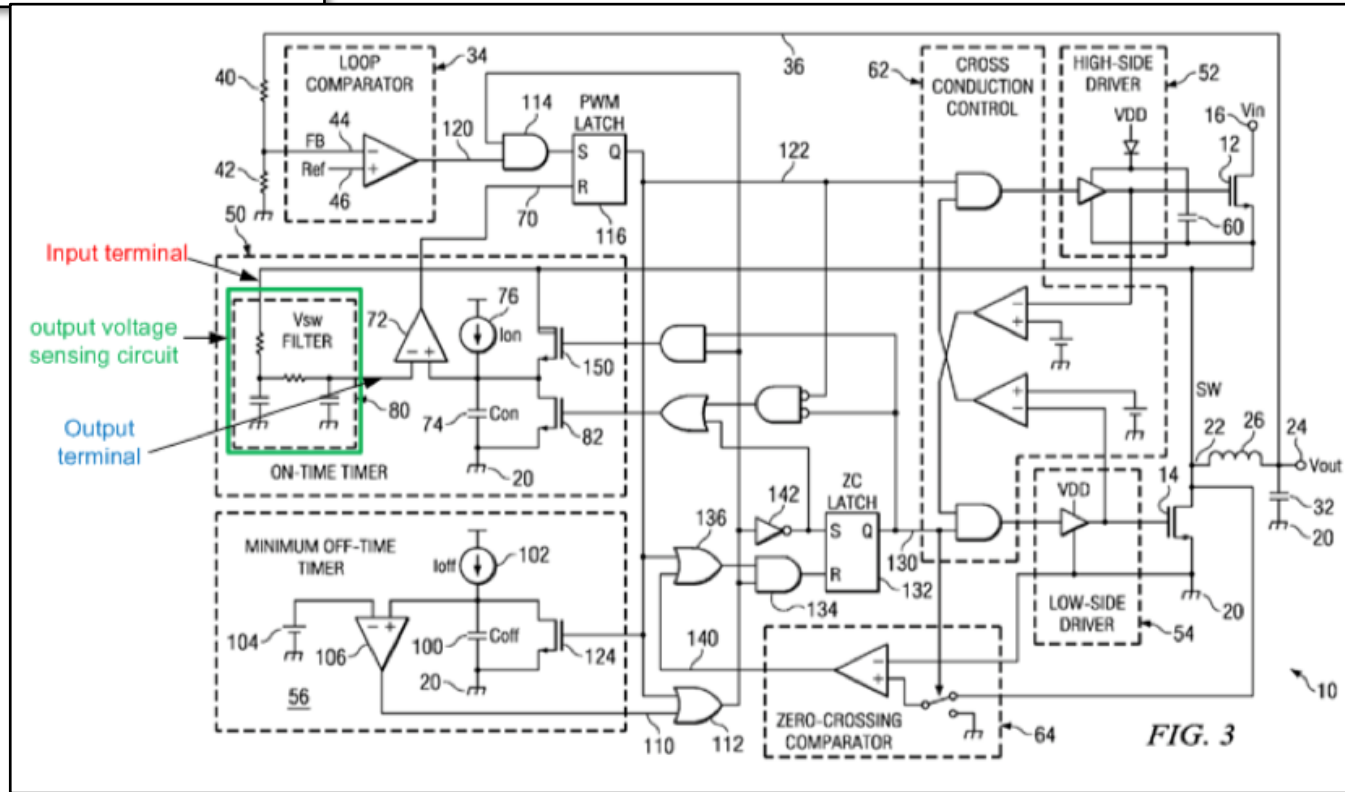
(Paper 1 at 36-39; EX005/7 at FIG. 3)



(Paper 1 at 36-39; EX005/7 at FIG. 4)

Petitioner's Allegation – Claim 1

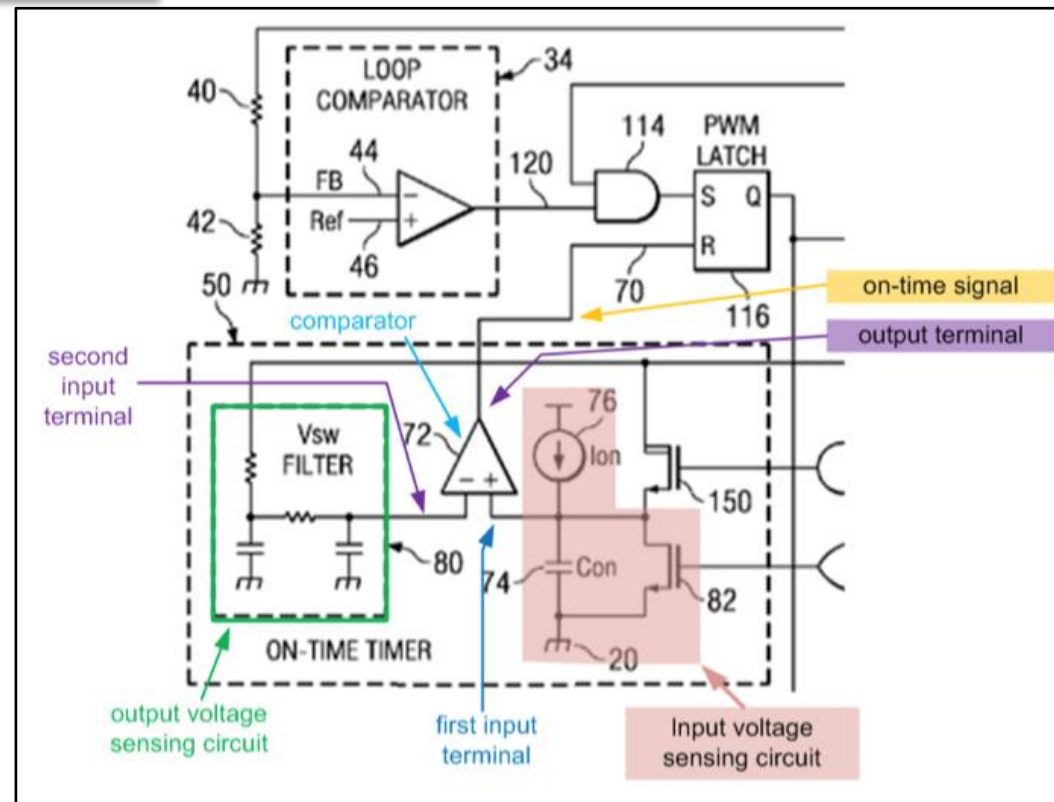
- e. **Limitation 1[B3]: an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and**



(Paper 1 at 36-39; EX005/7 at FIG. 3)

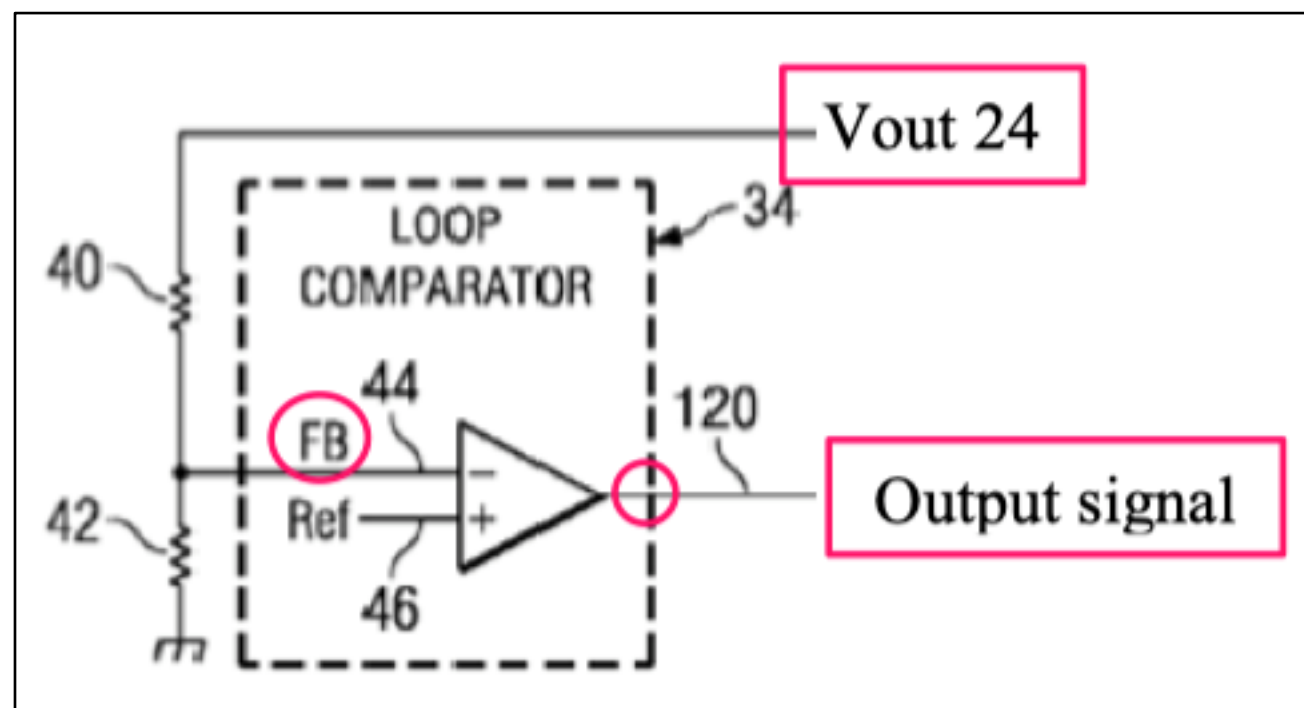
Petitioner's Allegation – Claim 1

- f. Limitation 1|B4|: a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;**



Petitioner's Allegation – Claim 1

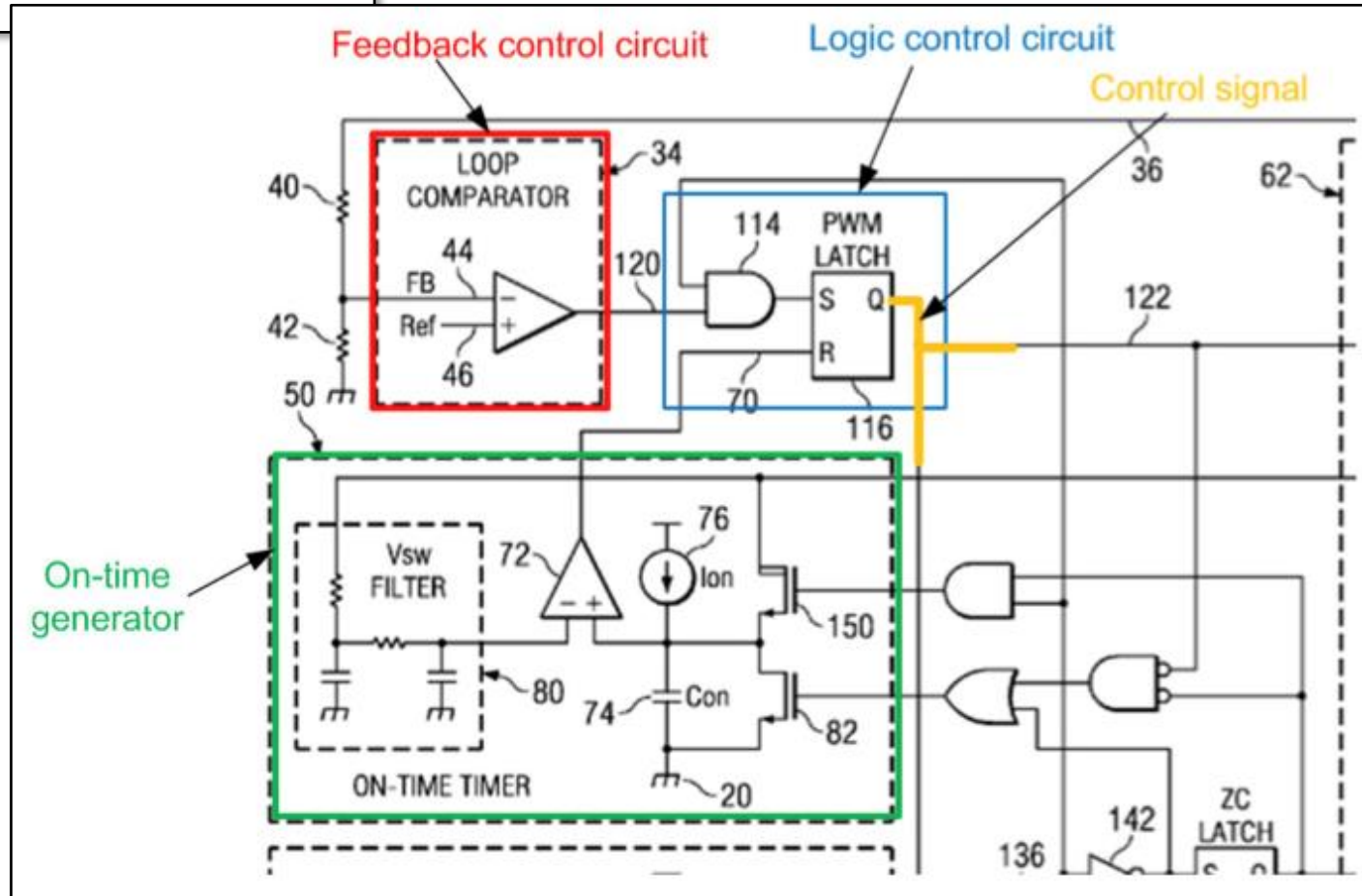
- g. Limitation 1[C]: a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to generate an output signal in accordance with the feedback signal; and



(Paper 1 at 42-43; EX005/7 at FIG. 3)

Petitioner's Allegation – Claim 1

- h. Limitation 1[D]: a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal; and

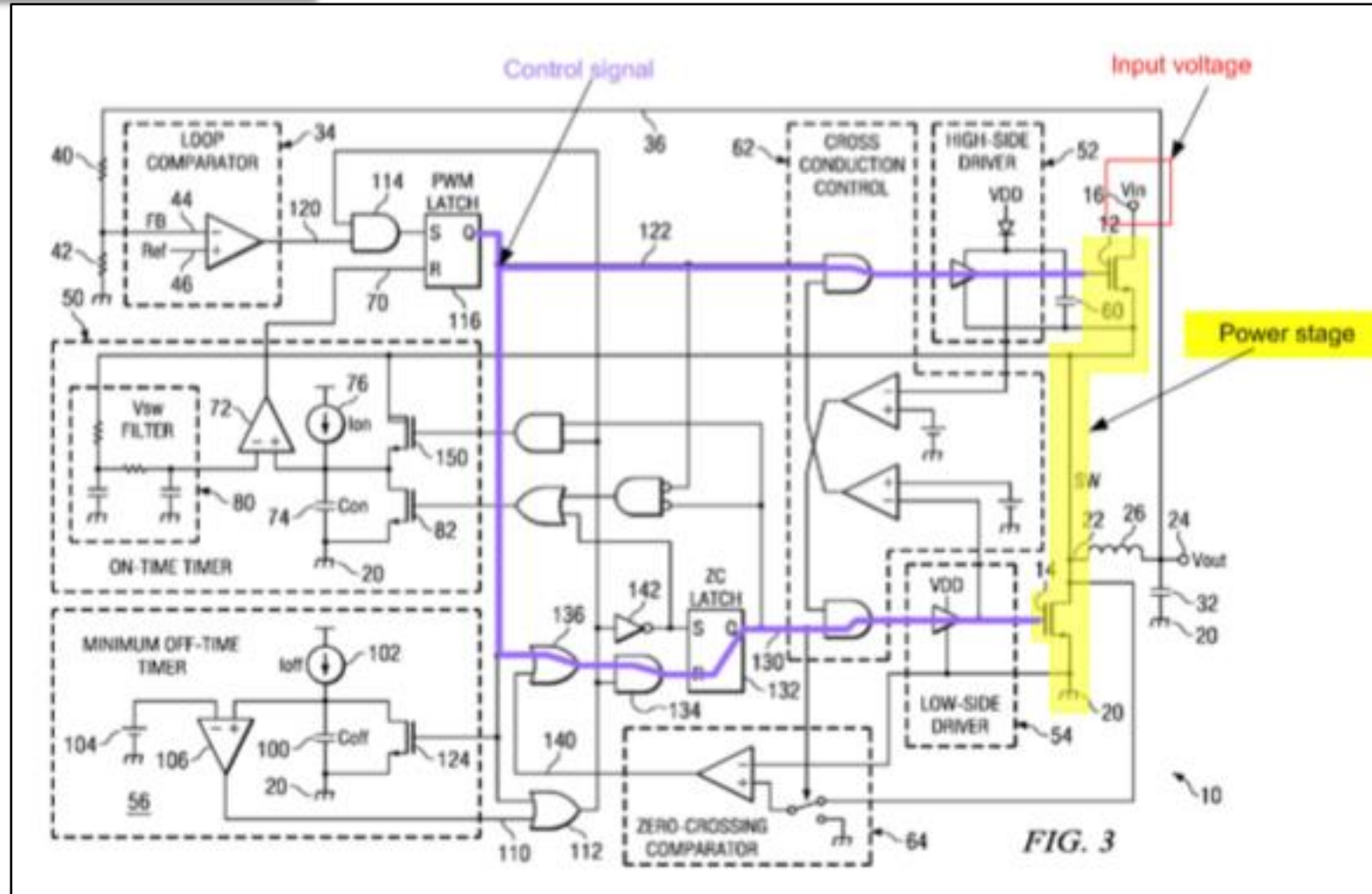


(Paper 1 at 44-47; EX005/7 at FIG. 3)

Patent Owner's Demonstratives – Exhibit 2009 (Not Evidence)

Petitioner's Allegation – Claim 1

- i. Limitation 1[E]: a power stage configured to receive an input voltage and the control signal, wherein based on the input voltage and the control signal, the power stage generates the switching signal.



(Paper 1 at 45-47; EX005/7 at FIG. 3)

Patent Owner's Demonstratives – Exhibit 2009 (Not Evidence)

Petitioner's Allegation – Claim 11

b. Limitation 11[A]: an on-time generator comprising:

Tateishi discloses this limitation. *See, e.g., VII.A.1.c, supra* (incorporated here); EX1003, ¶119.

c. Limitation 11[B1]: an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

Tateishi discloses this limitation. *See, e.g., VII.A.1.d, supra* (incorporated here); EX1003, ¶120.

(Paper 1 at 60-63)

d. Limitation 11[B2]: an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and

Tateishi discloses this limitation. *See, e.g., VII.A.1.e, supra* (incorporated here); EX1003, ¶121.

e. Limitation 11[B3]: a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;

Tateishi discloses this limitation. *See, e.g., VII.A.1.f, supra* (incorporated here); EX1003, ¶122.

f. Limitation 11[C]: a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to generate an output signal in accordance with the feedback signal; and

Tateishi discloses this limitation. *See, e.g., VII.A.1.g, supra* (incorporated here); EX1003, ¶123.

(Paper 1 at 60-63)

g. Limitation 11[D]: a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal.

Tateishi discloses this limitation. *See, e.g., VII.A.1.h, supra* (incorporated here); EX1003, ¶124.

(Paper 1 at 60-63)

Petitioner's Allegation – Claim 18

12. Claim 18

a. Limitation 18[PRE]: A step-down regulator, comprising:

Limitation 18[PRE] recites a step-down regulator. EX1003, ¶136. To the extent the preamble is limiting, Tateishi discloses this limitation. *See, e.g.*, EX1007, ¶5 (“Various apparatuses, methods and systems for a DC to DC converter with a pseudo constant switching frequency are disclosed herein”); EX1003, ¶140. *See also* VII.A.1.a, VII.A.1.b, *supra* (both incorporated here).

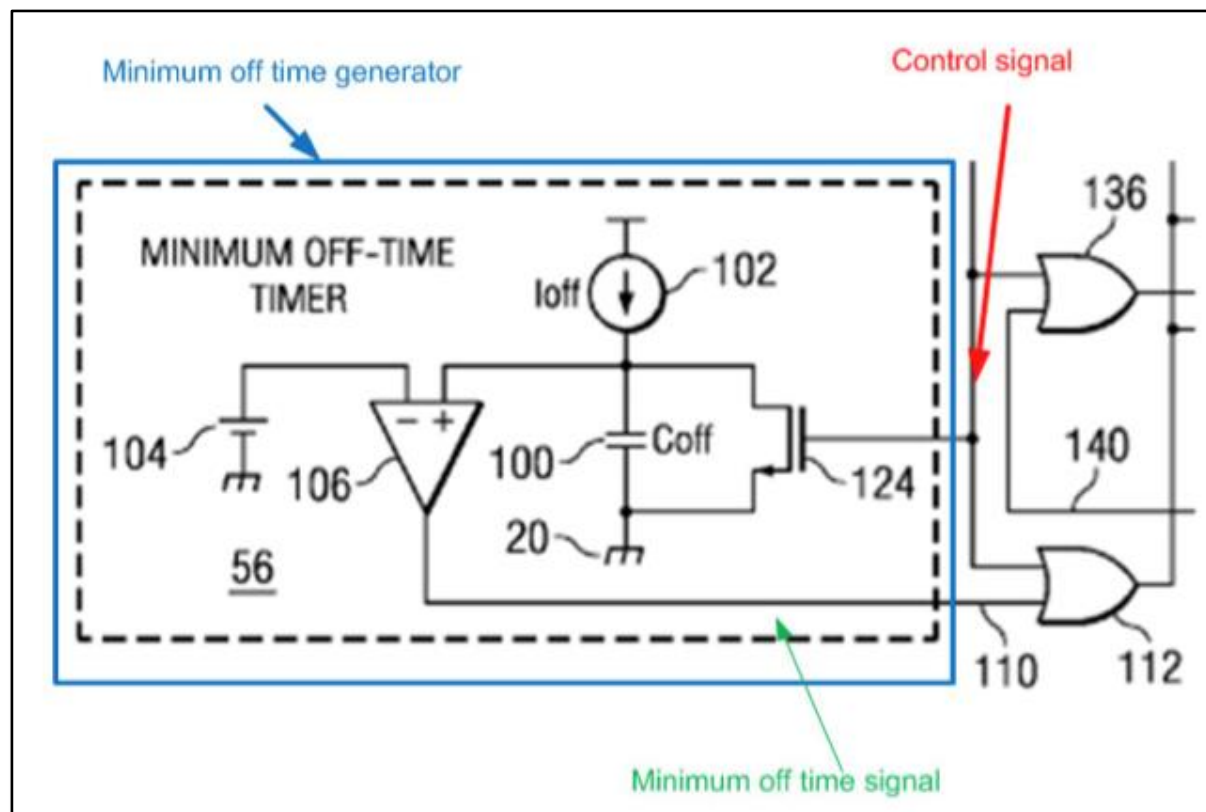
b. Limitation 18[A]: an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal;

Tateishi discloses this limitation. *See, e.g.*, VII.A.1.c, VII.A.1.d, VII.A.1.e, VII.A.1.f, *supra* (all incorporated here); EX1003, ¶137.

(Paper 1 at 66)

Petitioner's Allegation – Claim 18

- c. Limitation 18[B]: a minimum off time generator configured to receive the control signal, and to generate a minimum off time signal in accordance with the control signal;



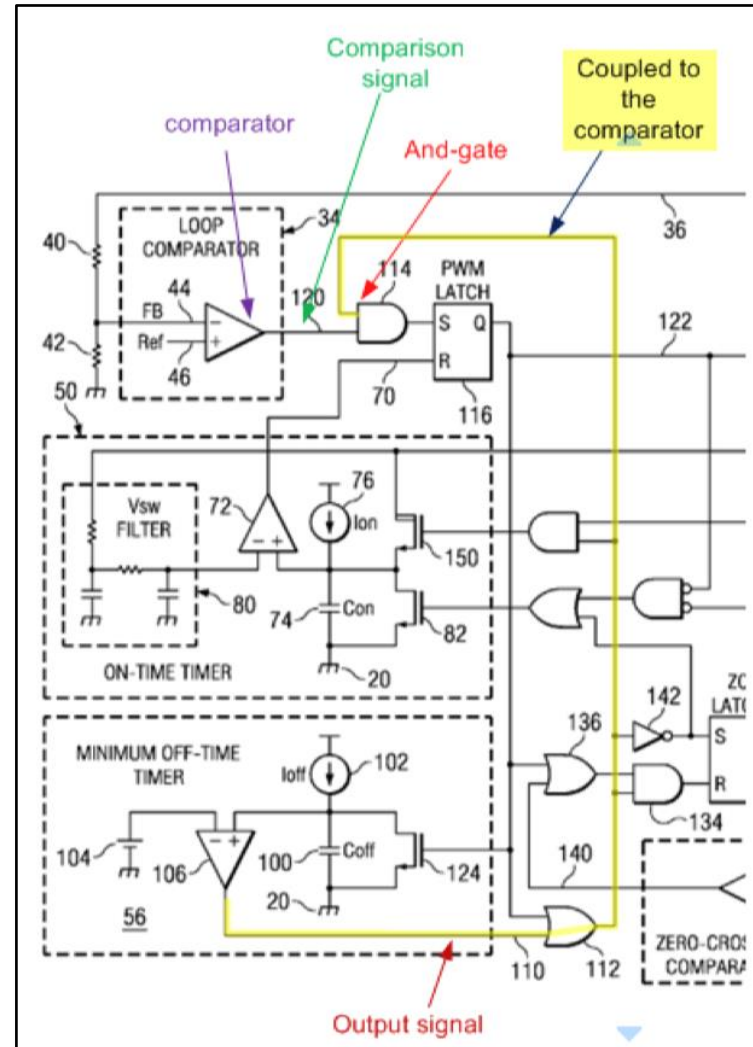
(Paper 1 at 66-68; see also FIG. 3)

Petitioner's Allegation – Claim 18

- d. Limitation 18[C]: a comparator configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to receive a reference signal, and wherein based on the feedback signal and the reference signal, the comparator generates a comparison signal;

Tateishi discloses this limitation. *See, e.g., VII.A.1.g, supra* (incorporated here); EX1003, ¶140.

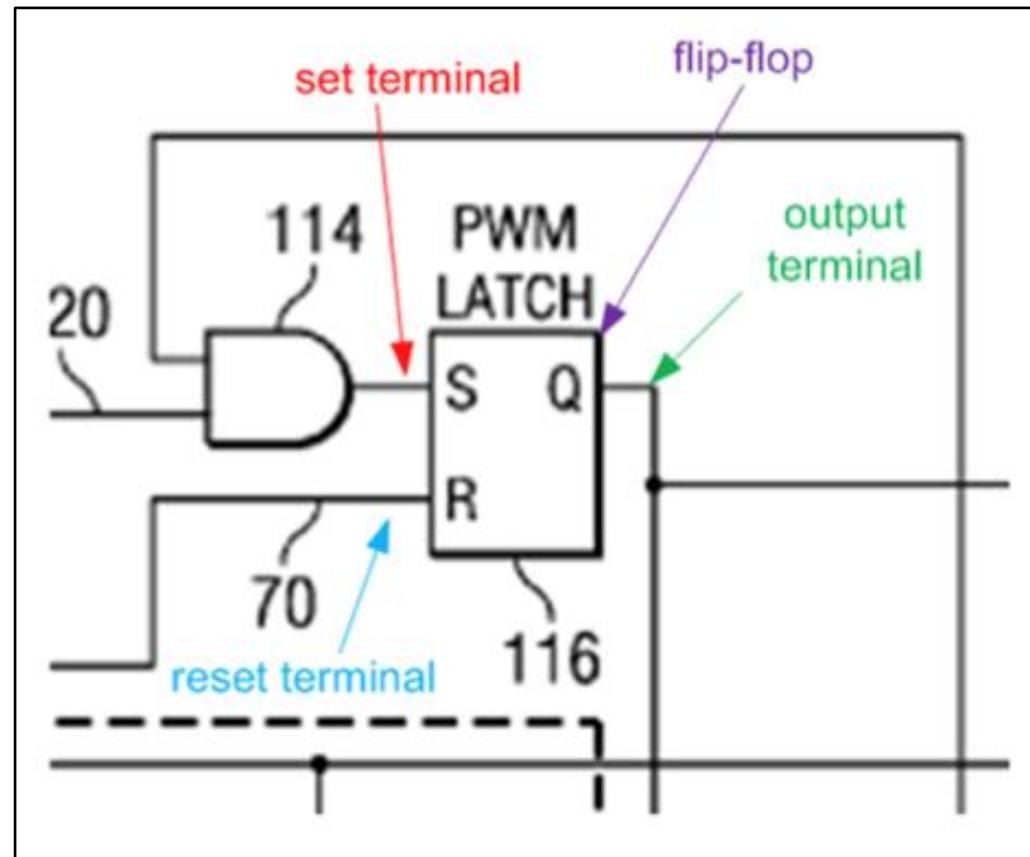
- e. Limitation 18[D]: an and-gate coupled to the comparator and the minimum off time generator to receive the comparison signal, and to receive the minimum off time signal, wherein based on the comparison signal and the minimum off time signal, the and-gate generates an output signal;



(Paper 1 at 68-70; see also FIG. 3)

Petitioner's Allegation – Claim 18

- f. Limitation 18[E]: a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal; and



(Paper 1 at 71-72; see also FIG. 3)

Patent Owner's Demonstratives – Exhibit 2009 (Not Evidence)

Petitioner's Allegation – Claim 18

- g. **Limitation 18[F]: a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal, the power stage converts an input voltage into the switching signal.**

Tateishi discloses this limitation. *See, e.g., VII.A.1.i, supra* (incorporated here); EX1003, ¶145.

(Paper 1 at 72)