



Morgan Lewis

PETITIONER REED SEMICONDUCTOR CORP. DEMONSTRATIVE SLIDES

Reed Semiconductor Corp. v. Monolithic Power Systems, Inc.

IPR2024-01158

U.S. Patent No. 9,041,377

Presenters



Andrew J. Gray, IV
Reg. No. 41,796
Silicon Valley



Annaliese Parker
Admitted *Pro Hac Vice*
Silicon Valley

Morgan Lewis

Petitioner Reed Semiconductor Corp. Exhibit 1022
Demonstrative Exhibit – Not Evidence

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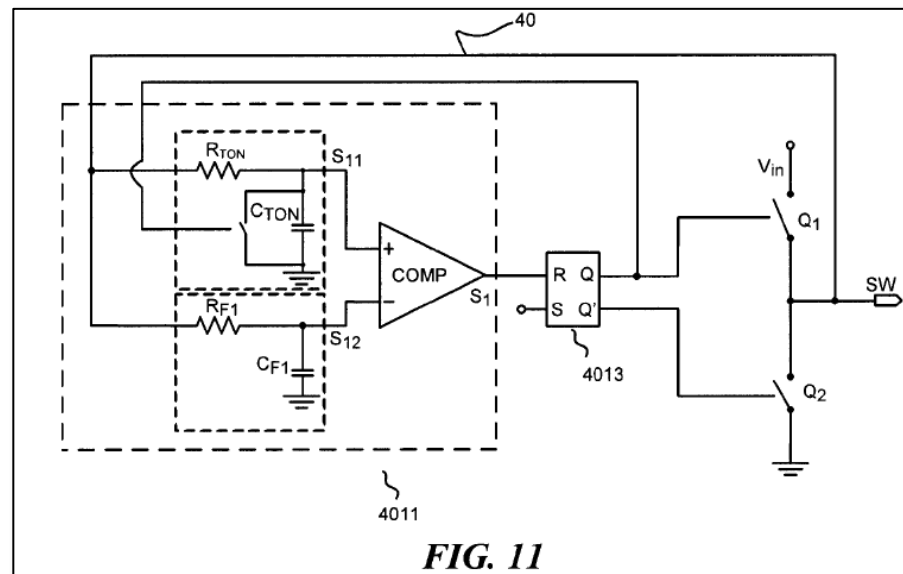
Overview of the '377 Patent

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Overview of the '377 Patent

- The '377 Patent is generally directed to **switch-mode DC-DC voltage converters with pseudo constant-on-time control circuits** for controlling "high-side" and "low-side" switches
- Claims of the '377 patent require:
 - a control signal configured to control an on-time generator, a power stage with high side and low side switches, and a minimum off-time generator

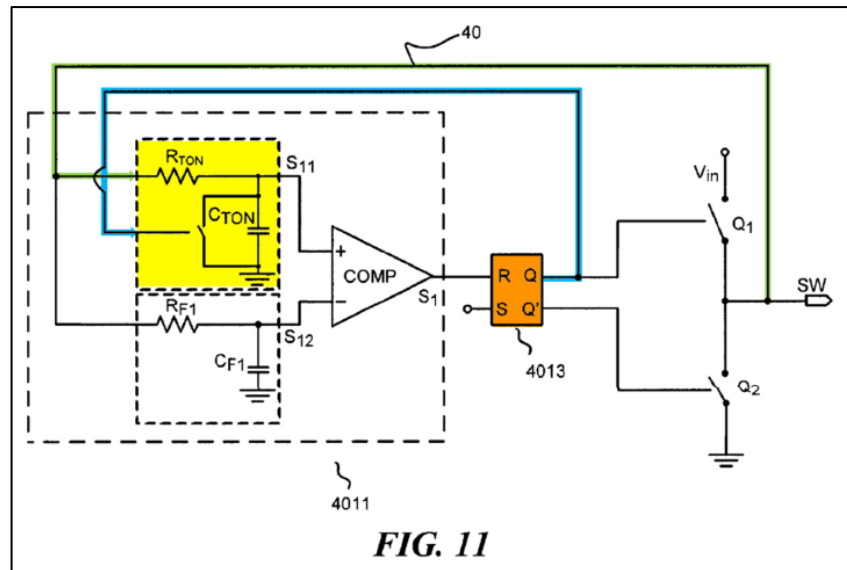


Overview: Disputed Elements of Claim 1

'377 Patent, Claim 1

- A step-down regulator, comprising:
- a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:
 - an on-time generator comprising:
 - an **input voltage sensing circuit** having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a **switching signal** provided by the step-down regulator, **the second input terminal is configured to receive a control signal** provided by the pseudo constant on time control circuit, and wherein based on the **switching signal** and the **control signal**, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;
 - a **logic control circuit** coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, **the logic control circuit generates the control signal**; and
- a **power stage configured to receive** an input voltage and **the control signal**, wherein based on the input voltage and **the control signal**, the power stage generates the switching signal.

'377 Patent, FIG. 11



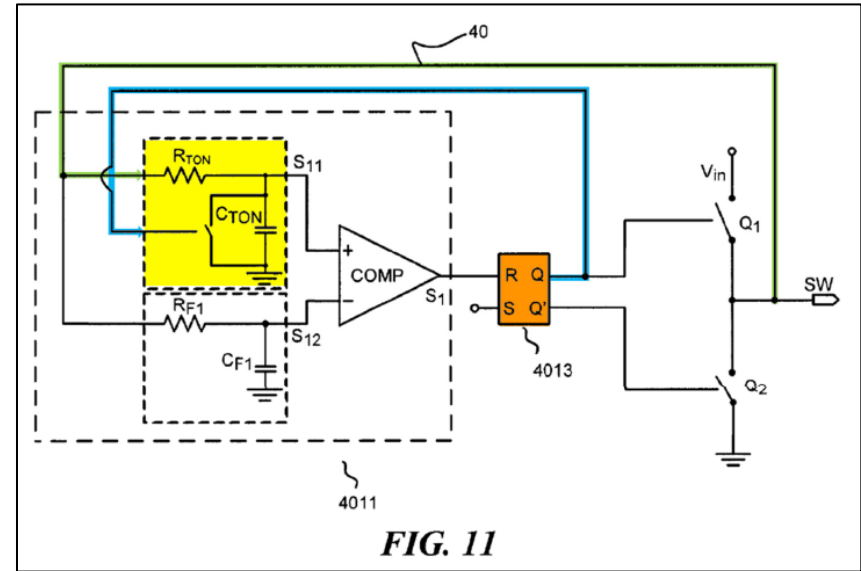
Overview of the Arguments

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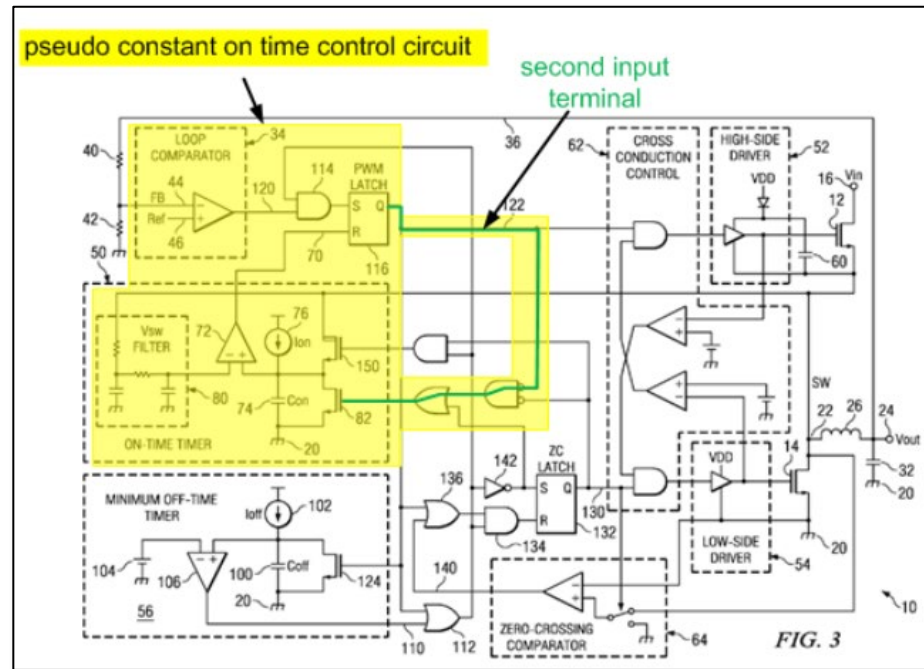
Overview of the Arguments: “Control Signal” requires no construction

“Control Signal” requires no construction and its plain and ordinary meaning is a “**signal configured to control a circuit component.**”



Overview of the Arguments: Tateishi discloses the claimed “Control Signal”

Tateishi's **control signal** (122) controls the “input voltage sensing circuit” and “power stage” recited in the claims.



Claim Construction

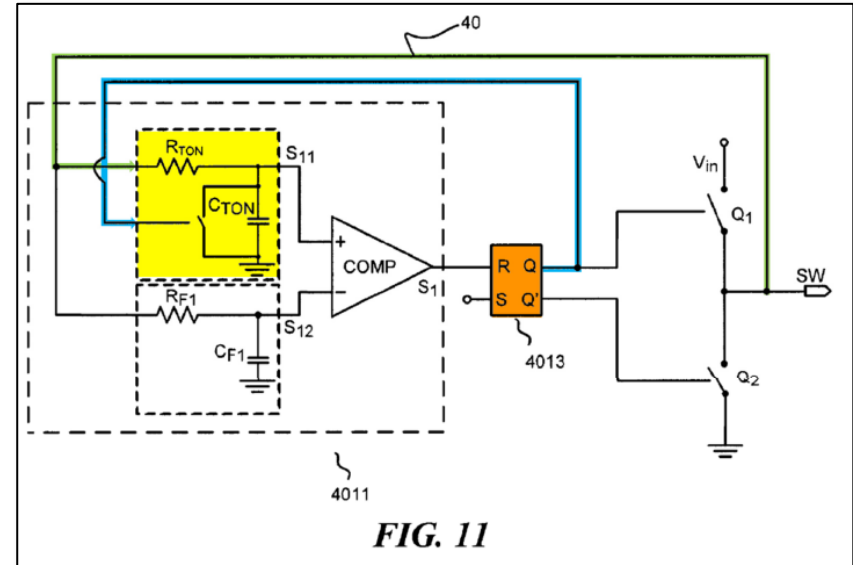


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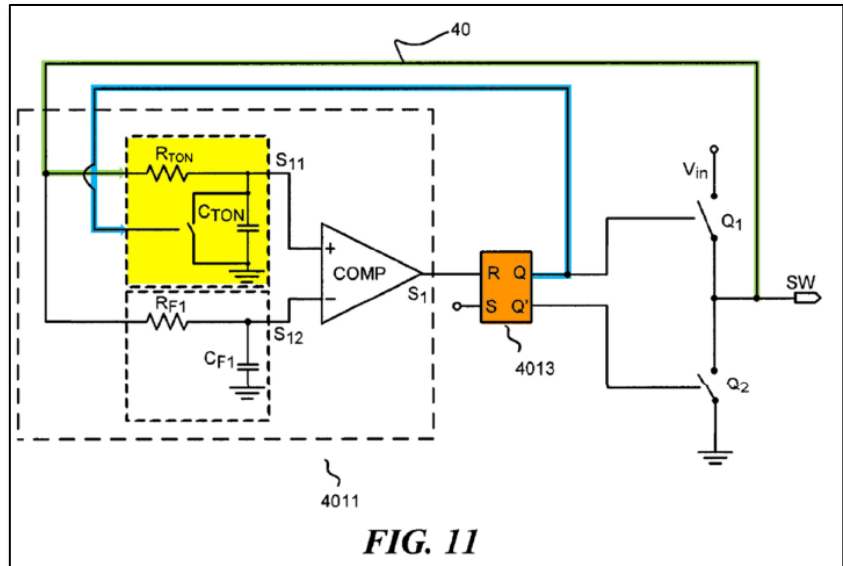
The “control signal” is a “signal configured to control a circuit component”

The control signal requires **no construction** and should be accorded its **plain and ordinary meaning**: a “signal configured to control a circuit component.”



The “control signal” controls the Input Voltage Sensing Circuit and the Power Stage

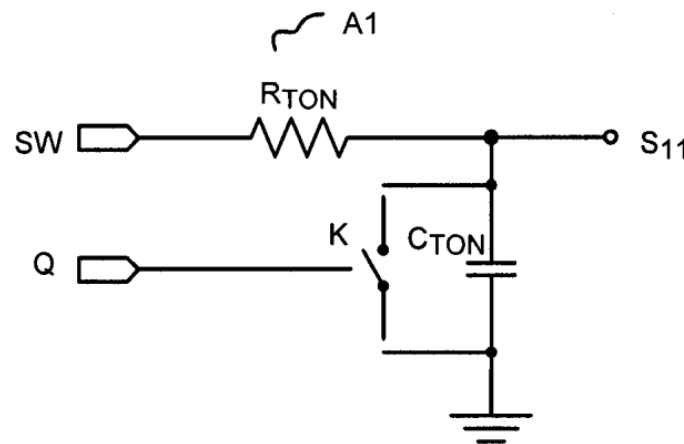
- an on-time generator [4011] comprising:
 - an input voltage sensing circuit [yellow] having . . . a second input terminal . . . , wherein . . . **the second input terminal is configured to receive a control signal**
 - a logic control circuit coupled to the on-time generator . . . **the logic control circuit generates the control signal**
- a power stage configured to receive an input voltage and **the control signal**.



Intrinsic evidence supports Petitioner's construction of "control signal"

- The specification teaches:
- "[t]he switch K is coupled to the capacitor CTON in parallel and controlled by the control signal Q."

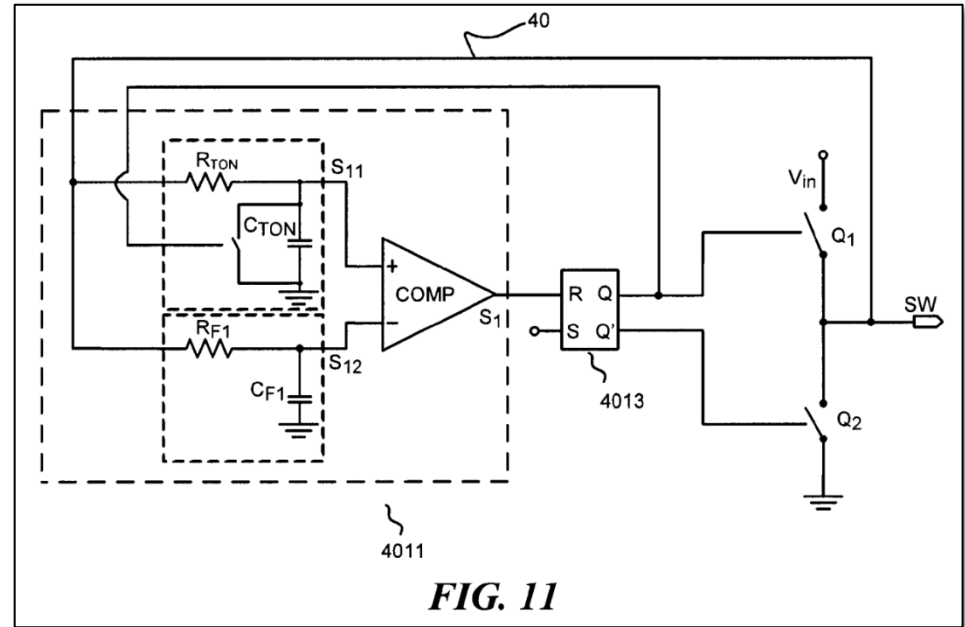
FIG. 4



Paper 26 (Pet. Reply), pp. 8-10; Ex. 1001 ('377 Patent), p. 3, 5:21-23

Intrinsic evidence supports Petitioner's construction of "control signal"

- The specification teaches:
- "[t]he control signal Q controls the high-side switch Q1, and the complementary signal Q' of the control signal Q controls the low-side switch Q2."



Extrinsic evidence supports Petitioner's construction of "control signal"

The Wiley Electrical and Electronics Engineering Dictionary (2004) defines the term "control signal" as "[a] signal utilized to control a device or process.

control signal 1. A signal utilized to control a device or process. In a computer, for instance, such a signal may be an interrupt request. 2. In telecommunications, a signal that transmits control information. For example, a customer picks up a telephone receiver, hears a dial tone, dials a sequence of digits, and then gets a busy signal. All the tones heard are control signals.

Patent Owner Continues to Advance **Narrow Claim Construction** of “Control Signal”

A POSITA would accordingly understand that the claimed **control signal’s** plain and ordinary meaning is **a logic signal with two distinct states.** (EX2005, ¶ 56.)

Patent Owner’s Response

Further, the proper construction of **“control signal”** is **“logic signal with two distinct states,”** which Petitioner’s signal amalgam does not meet. The

Patent Owner’s Surreply

Patent Owners construction of “control signal” deliberately excluding logic gates **is too narrow and unsupported**

- Patent Owner’s construction of control signal seeks to add two unsupported limitations to the claims:

1. The “control signal” **must not pass through any logic gates** from the point of its generation to the point of its ultimate receipt. Paper 6, p. 13.

2. “The **claimed control signal** is, however, **a plain logic 1 or 0.**” Paper 31, p. 9.

Patent Owner agrees that the “control signal” needs to control other circuit elements/components.

- Patent Owner’s expert agrees that “a control signal is a signal that controls other circuit components.” Ex. 1017 (J. McAlexander 7/1/2025 Dep. Tr.), 121:1-4.

Transcript of Joseph McAlexander, III
Conducted on July 1, 2025 121

1 Q So in the context of the '377 patent, you would
2 agree that a control signal is a signal that controls
3 other circuit components, correct?
4 A I would agree with that, yes.

- Patent Owner further asserts “[t]he ‘control signal is a single signal that goes from one control element as control for another.’” Paper 5 (POPR), p. 1.

Paper 5 (POPR), p. 1; Ex. 1017 (J. McAlexander 7/1/2025 Dep. Tr.), 121:1-4

The Board **rejected** Patent Owner's construction of "control signal"

On the present record at this preliminary point in the proceeding and for purposes of this decision, we decline to read the word “logical” into the term “control signal,” we do not construe the claim term as excluding logic gates between the logic control circuit output and the second input terminal of the input voltage sensing circuit, and we do not construe the claims such that the “control signal” must be the exclusively controlling factor of a component.



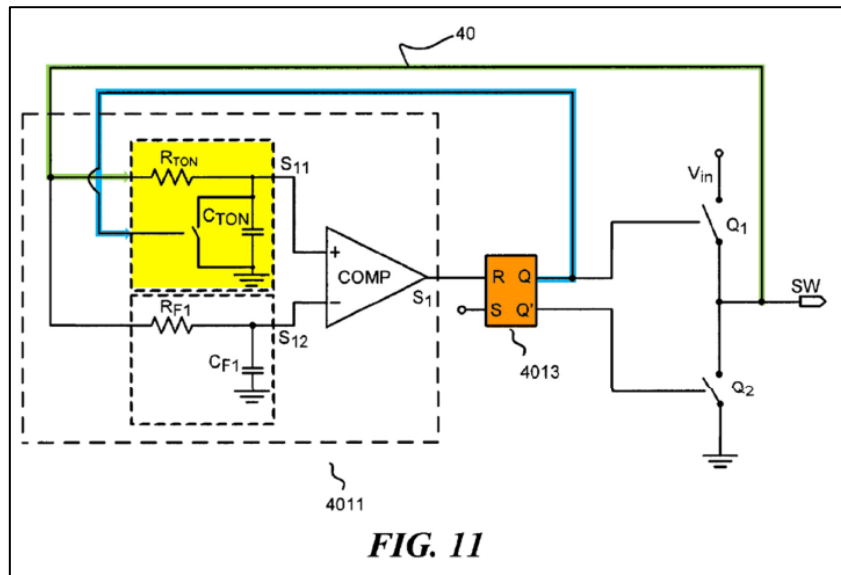
Ground 1: Claims 1-4, 9-14, and 17-18 are anticipated by Tateishi

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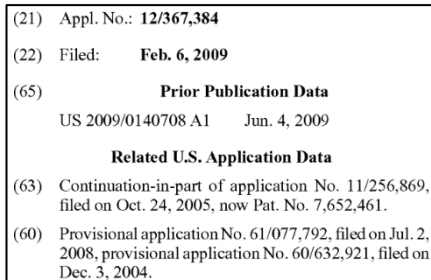
The claims require the “control signal” be generated by the logic control circuit and be received by the power stage and the input voltage sensing circuit

- an on-time generator [4011] comprising:
 - an input voltage sensing circuit [yellow] having . . . a second input terminal . . . , wherein . . . **the second input terminal is configured to receive a control signal**
 - a logic control circuit coupled to the on-time generator . . . **the logic control circuit generates the control signal**
- a power stage configured to receive an input voltage and **the control signal**.



Ex. 1001 ('377 Patent) 9:36-10:13; Paper 5 (POPR), p. 16; Paper 23 (POR), p. 5

- The Tateishi patent ('887 Patent) and the '377 patent teach the same invention
- Tateishi provided the solution 2 years prior to the patent owners



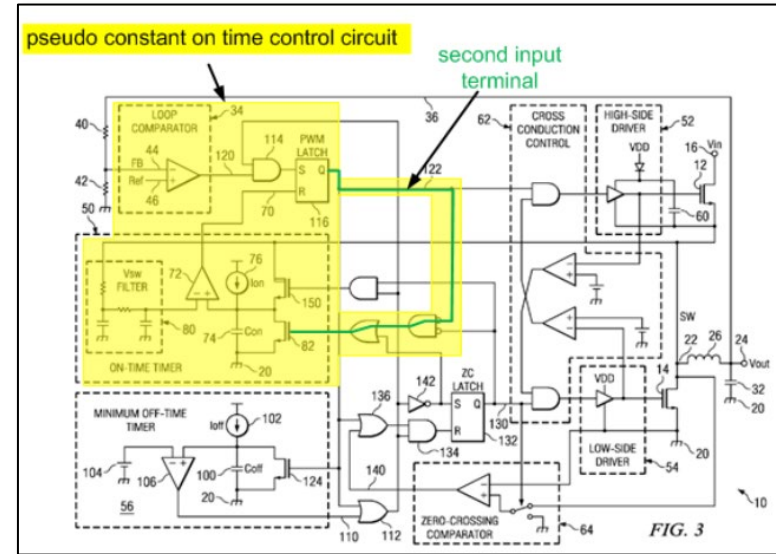
ABSTRACT

Various apparatuses, methods and systems for a DC to DC converter with a pseudo constant switching frequency are disclosed herein. For example, some embodiments provide a DC to DC converter having a switch connected to a switching node to control a voltage of the switching node, and a switching controller that is adapted to turn on and off the switch at a substantially constant frequency based at least in part on the voltage of the switching node. The switching controller includes a modulator connected to a control electrode of the switch and that is adapted to actuate and deactuate the switch, and a first timer that is connected to the switching node and to the modulator. The first timer uses the voltage of the switching node to determine an on-time for the switch.

(21)	Appl. No.:	12/367,384
(22)	Filed:	Feb. 6, 2009
(65)		Prior Publication Data
	US 2009/0140708 A1	Jun. 4, 2009
		Related U.S. Application Data
(63)	Continuation-in-part of application No. 11/256,869, filed on Oct. 24, 2005, now Pat. No. 7,652,461.	
(60)	Provisional application No. 61/077,792, filed on Jul. 2, 2008, provisional application No. 60/632,921, filed on Dec. 3, 2004.	

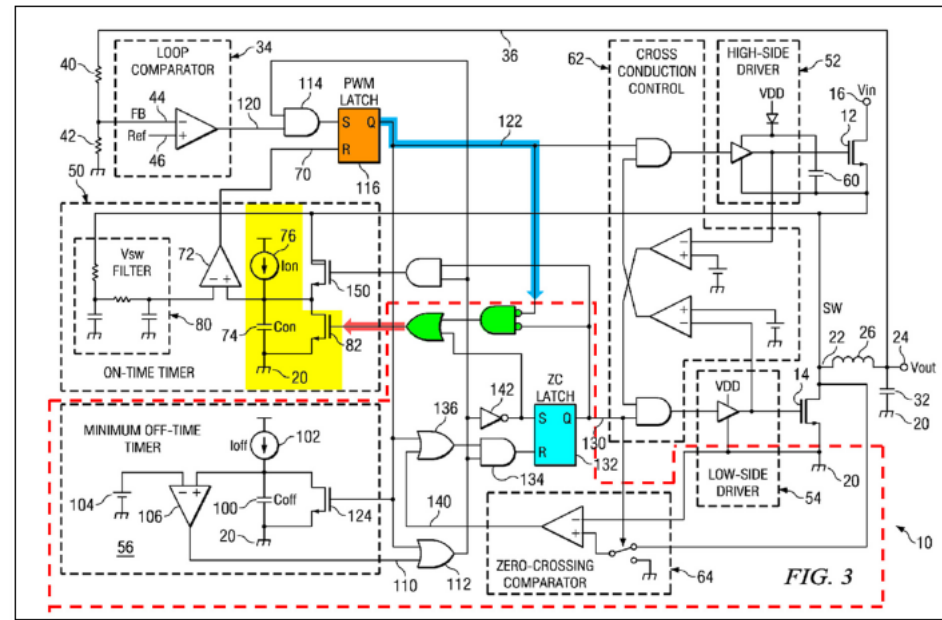
Tateishi Anticipates Claim 1: The “control signal” is received by the “input voltage sensing circuit”

- an on-time generator comprising:
 - an input voltage sensing circuit having . . . a second input terminal . . . , wherein . . . **the second input terminal is configured to receive a control signal**
 - a logic control circuit coupled to the on-time generator . . . **the logic control circuit generates the control signal**
- a power stage configured to receive an input voltage and **the control signal**.



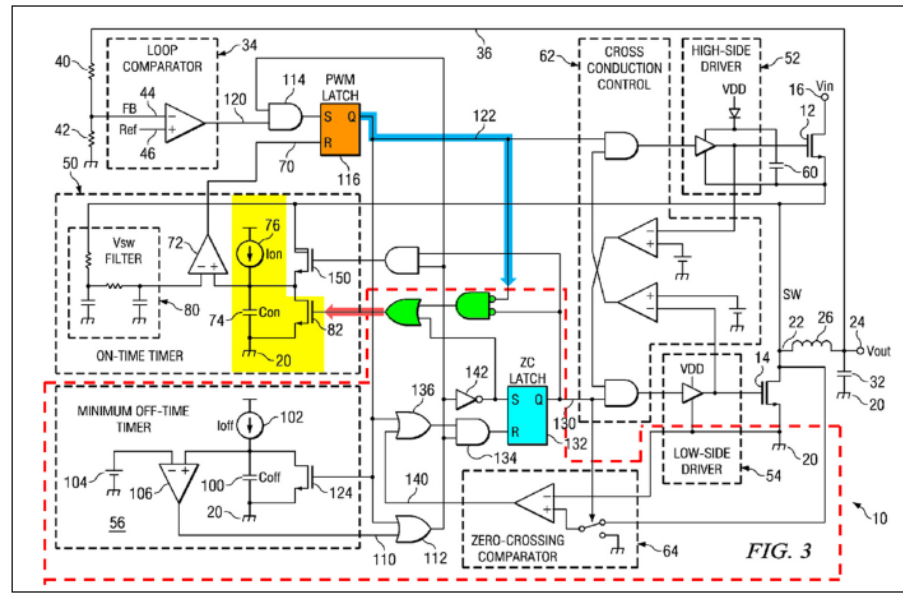
Patent Owner argues the control signal in Tateishi is two different signals

- Patent Owner argues that the control signal is two separate signals (red and blue) because there is logic (green) between the PWM latch 116 and the transistor 82
- Patent Owner argues that the control signal cannot have different logical states between generation of the signal and receipt of the claimed limitation



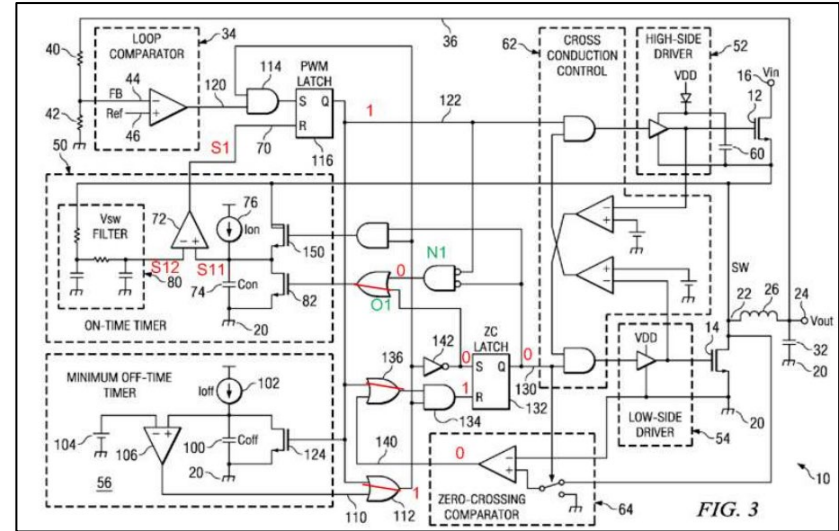
Patent Owner argues the control signal in Tateishi is two different signals

- Patent Owner's analysis is incorrect, improper, narrow, and unsupported.
- When the control function is present, the control signal may pass through intervening logic gates and/or may change logical values along its path and meet the claim limitations. Ex. 1016, p. 8.



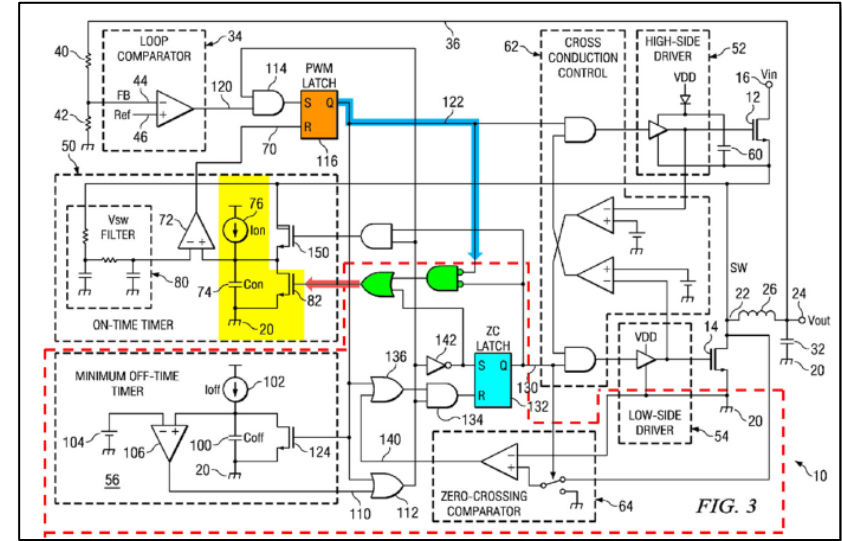
The “control signal” passes through the logic gates to control transistor 82

When the output of the zero-crossing comparator 64 is 0, the control signal 122 controls every logic gate



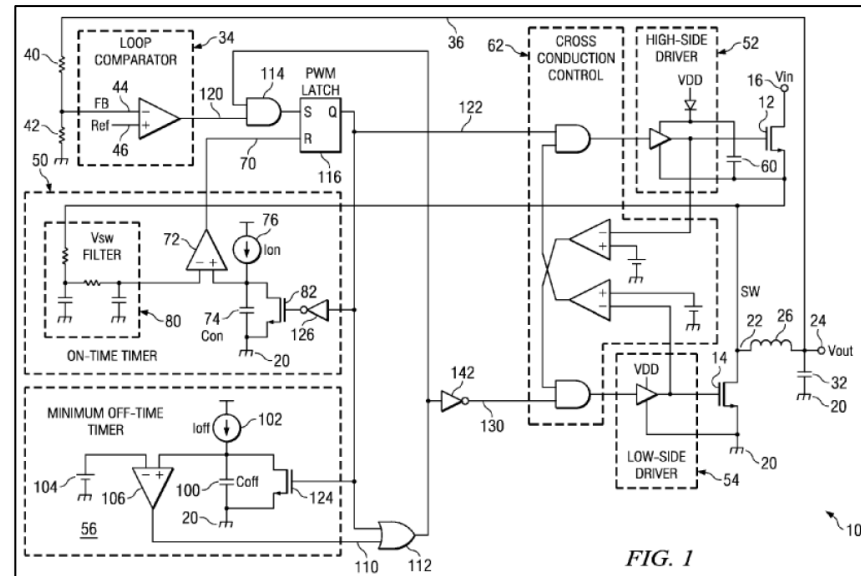
Patent Owner argues the claims require the control signal taught by Tateishi fails because it is not "input" directly into the on-time generator

- This is not required by the claims
 - Claim 1 requires: an input voltage sensing circuit [yellow] having . . . a second input terminal . . . , wherein . . . **the second input terminal is configured to receive a control signal**
- The claims require only that the control signal generated as the Q output of PWM latch 116 be received at the input to transistor 82, which is exactly what Tateishi teaches as shown in FIG. 3.



The Institution Decision discusses how a POSITA would understand a control signal

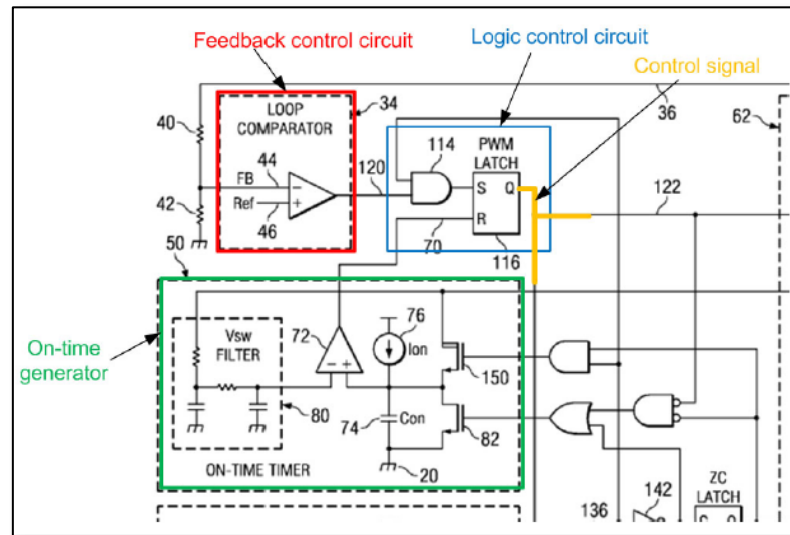
- "Tateishi explains that 'the DC to DC buck converter 10 of FIG. 3 operates in much the same manner as that of FIG. 1.'"
- "Tateishi. . . speaks of output 122 at the Q terminal of SR latch 116 as controlling switch 82 as well as other components without regard to whether the circuit includes logical operators between the two terminals."
- "We [the board] discussed this disclosure of the Figure 1 embodiment merely as potential evidence of how a person of ordinary skill in the art would understand 'a control signal' in the context of a DC to DC buck converter."



The Institution Decision found that Tateishi's control signal is configured to control the input voltage sensing circuit

The “**control signal**” drives the input voltage sensing circuit within the **on-time generator**

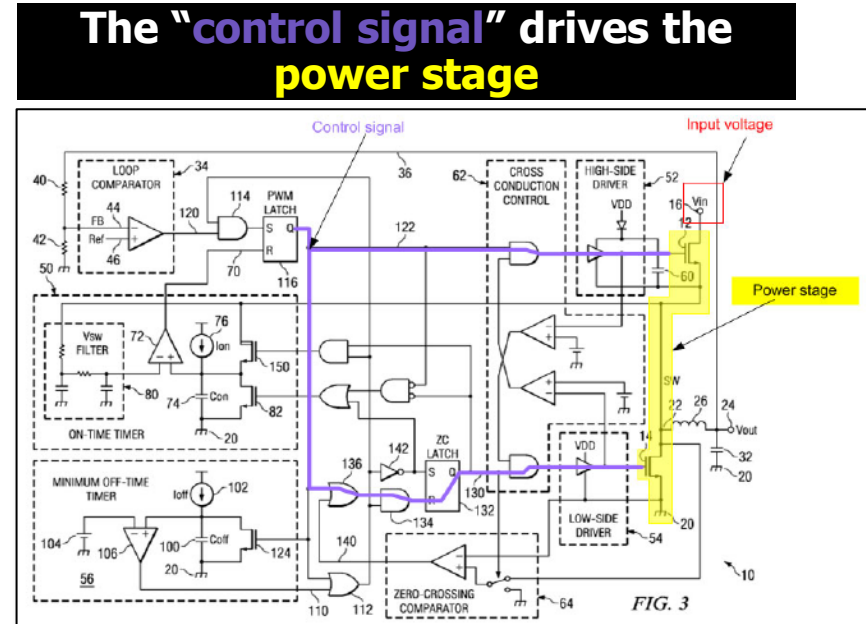
- The control signal “**drives**” the on-time generator and the power stage, both directly and indirectly through logic gates.
- Patent Owner did not dispute this finding by the Board in its Response.



Tateishi FIG. 3

The Institution Decision found that Tateishi's control signal is configured to control the power stage

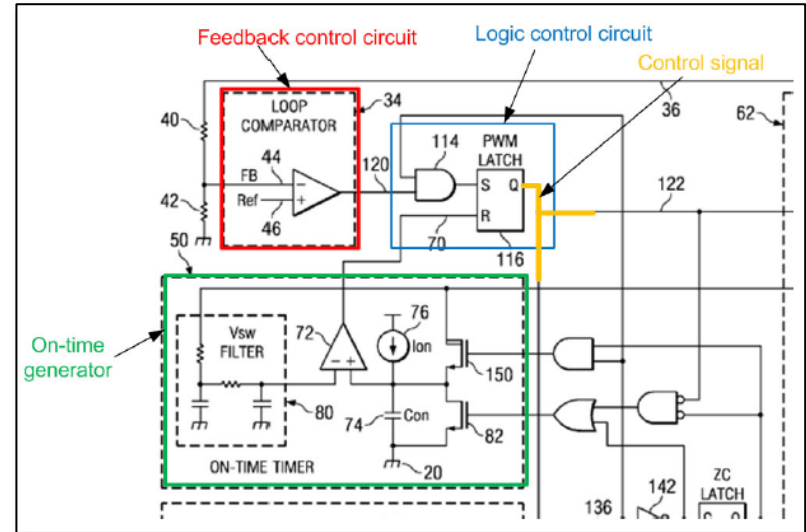
- The control signal “**drives**” the on-time generator and the power stage, both directly and indirectly through logic gates.
- Patent Owner did not dispute this finding by the Board in its Response.



Tateishi FIG. 3

Tateishi's control signal 122 controls the "input voltage sensing circuit" and "power stage" as claimed

- The output 122 drives the discharging transistor 82 in the on-time timer 50 . . . so that during an off-time, the capacitor Con 74 is discharged to ground 20 and during an on-time, the discharging transistor 82 is turned off allowing the capacitor Con 74 to be charged by the current source 76.



Tateishi FIG. 3



Ground 2: Claims 5, 7-8, and 15 are rendered obvious by Tateishi

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Patent Owner failed to respond to and therefore waived Ground 2

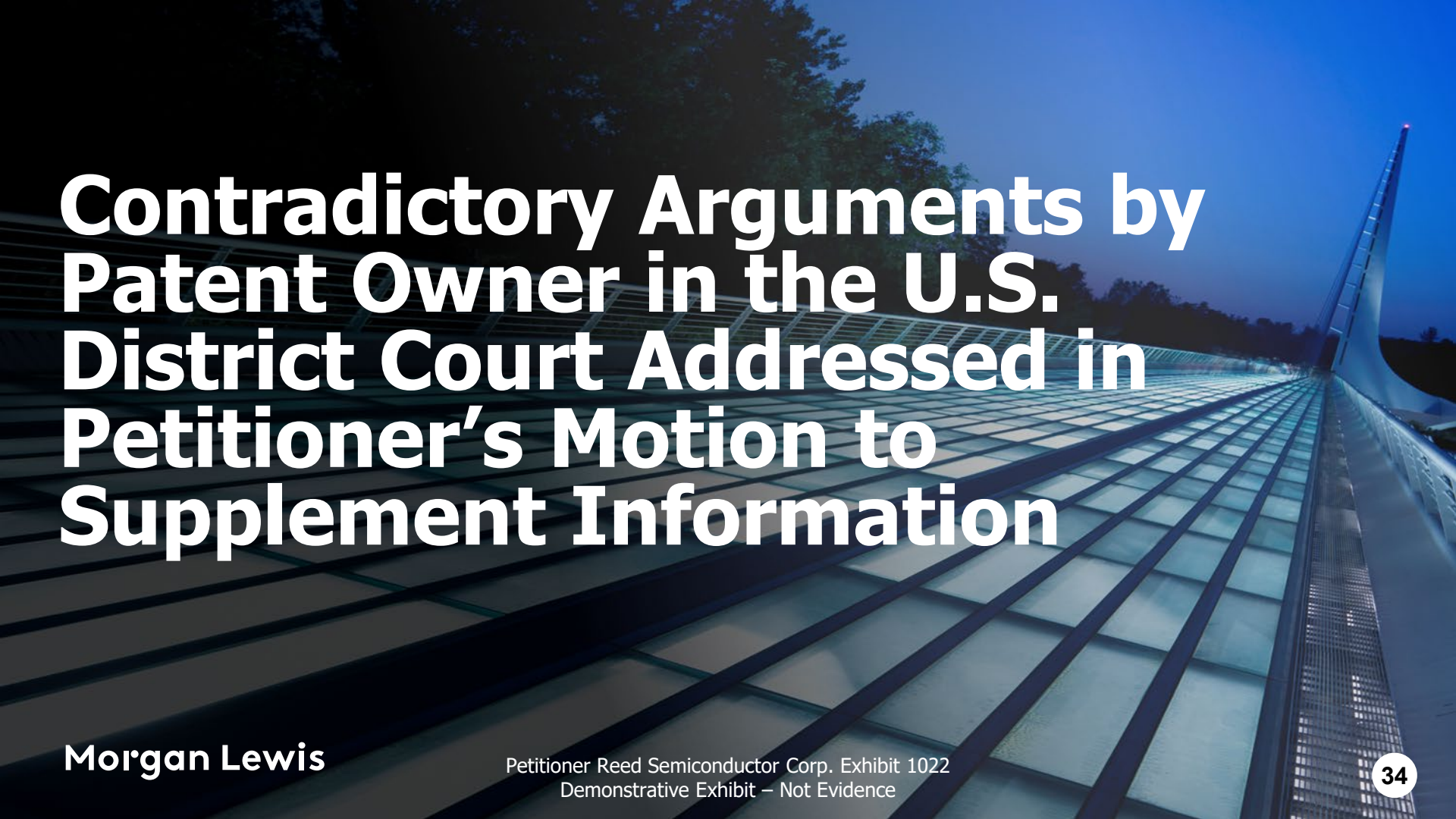
In the Patent Owner Response, Patent Owner states “Ground 2 addresses dependent claims. It does not cure the above-described deficiencies and fails for the same reasons.”



Patent Owner provides no arguments to Ground 2 in their response.



Therefore, Patent Owner **waives arguments** regarding Ground 2.



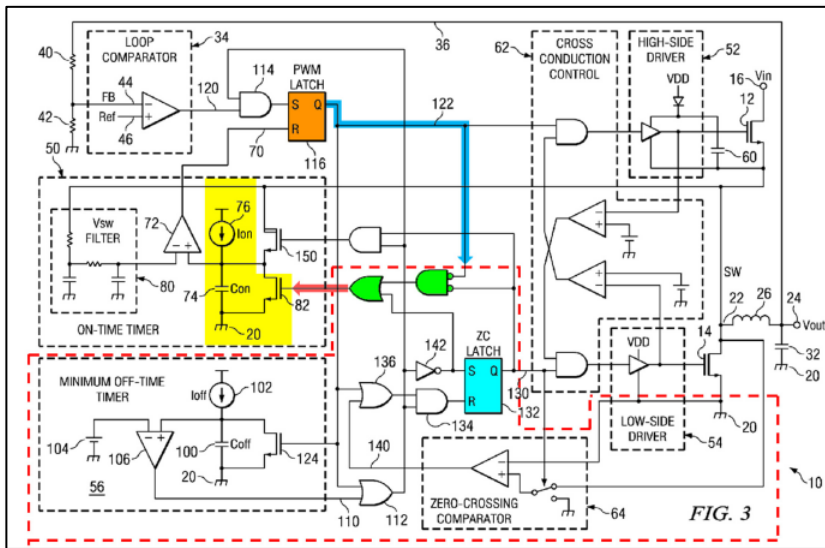
Contradictory Arguments by Patent Owner in the U.S. District Court Addressed in Petitioner's Motion to Supplement Information

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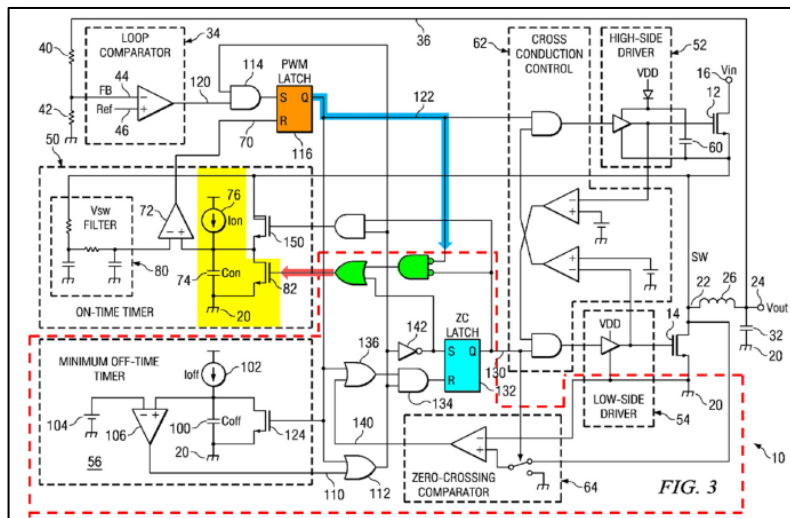
Patent Owner Argues in this IPR that Intervening Logic Interrupts the Control Signal

- Patent Owner argues “[t]he signal of the annotated red and blue arrows above are two different logical signals.”
 - Patent Owner’s Preliminary Response, Paper 5, p. 18; *see also* Patent Owner’s Preliminary Response, Paper 5, EX 2001, ¶¶ 46-47.

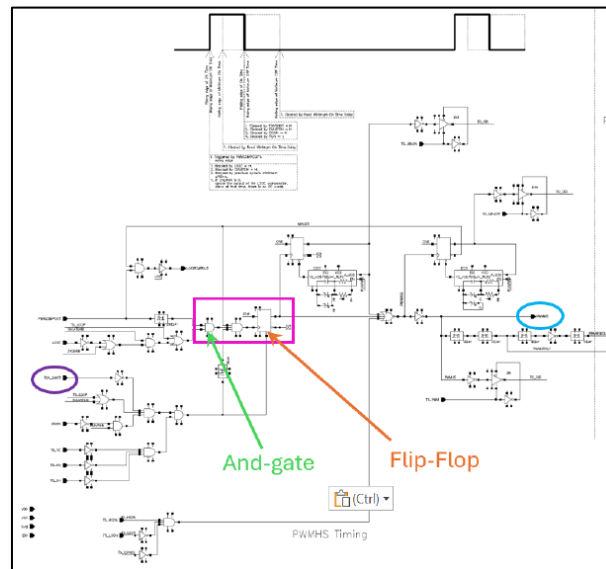


Patent Owner, in U.S. District Court, accepts intervening logic in the “control signal” for their infringement analysis

Tateishi FIG. 3



Reed Accused Product

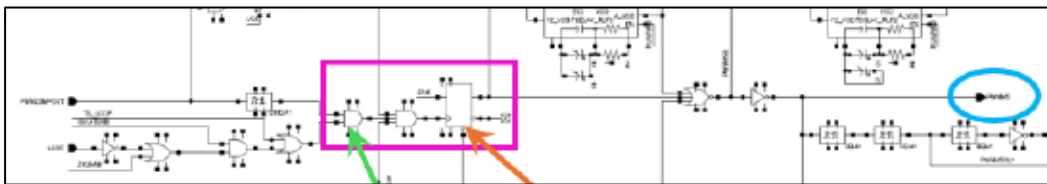


“[T]he flip-flop generates the control signal (e.g., PWMHS/PWMHSB [annotated in blue]).”

Paper 5 (POPR), p. 18; See also Paper 23 (POR) p. 23; EX 1019 at ¶¶ 239, 253

Patent Owner's expert asserts that the control signal can be both a 0 and a 1 and still be the claimed "control signal"

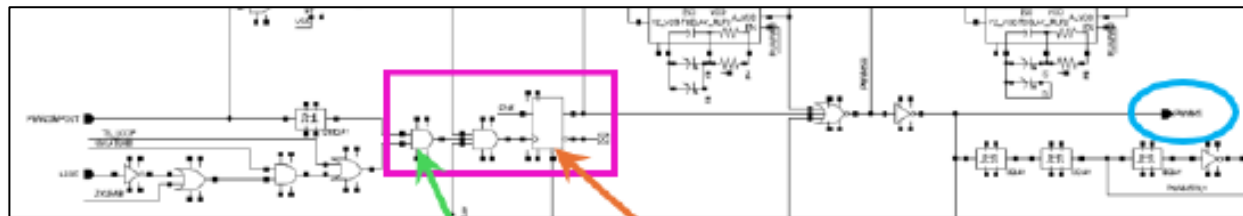
- Q: And the control signal that's generated is not changed by any of the intervening logic, in your opinion; is that correct?
- ...
- A: It is not because when you generate a one on the input, it immediately flips the NOR gate to a zero on the output. So yes, that signal, whatever the flip-flop defines, that is what the PWHMS signal is going to reflect.
- Q: I'm not sure I followed. Did you say that if you generate a one - -
- A: If you generate a one on an input of a NOR gate, it automatically flips to a zero on that output.
- Q: So the one and the zero reflect the same signal, in your opinion?
- A: Yes



Ex. 1020 (J. McAlexander 9/18/2025 Dep. Tr.), 169:20-170:13

Patent Owner's Expert states that the flip flop generates the PWMHS signal, but later states the PWMHS signal is generated after the NOR gate

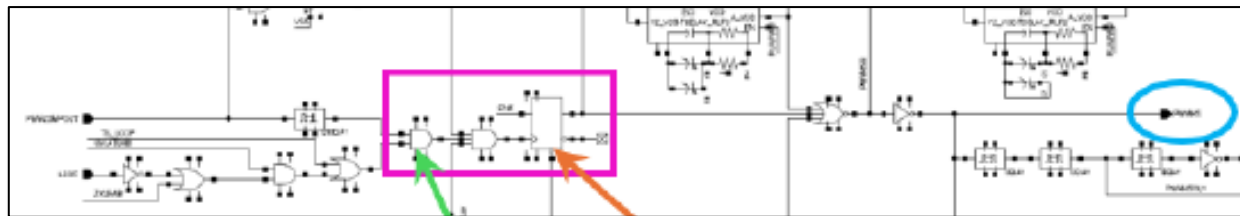
- Q: And so what I'm trying to get at is as the signal that you say is generated by the flip-flop passes through the intervening logic, I'm trying to get your position as to whether it's changed in that intervening logic?
- A: What I'm saying is you are imposing intervening logic. There is nothing that says in the claim that the signal has to be the one that I've defined on the output pin of the flip-flop. It's the flip-flop that generates the signal. And that signal that it generates is PWMHS. I'm not talking about intervening logic or anything. That's the signal that's generated.



Ex. 1020 (J. McAlexander 9/18/2025 Dep. Tr.), 172:6-20

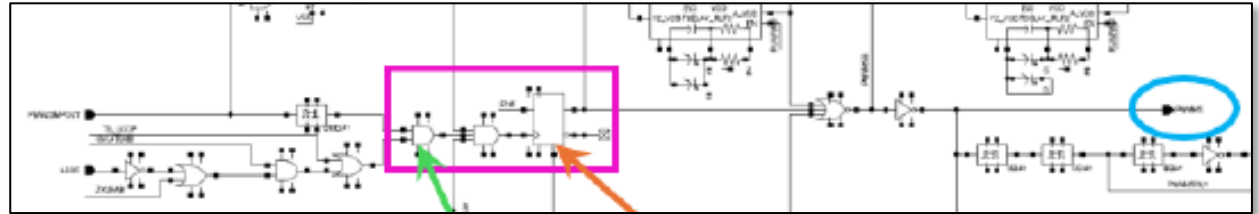
Patent Owner's Expert concedes a precursor is generated by the flop flop prior to generating the PWMHS signal

- Q: At its output, has this flip-flop generated the control signal PWMHS?
- A: I'll use the word precursor. It's generating a precursor that is going to be the PWMHS signal that now has the power to drive that down-stage power circuit.
- Q: But the flip-flop standing alone has not yet generated the control signal at its output, is that your position?
- A: My position is the PWMHS signal is the generated control signal by the flip-flop.



Patent Owner's Expert concedes that the control signal does not need to be generated at the node on the output of the flip flop

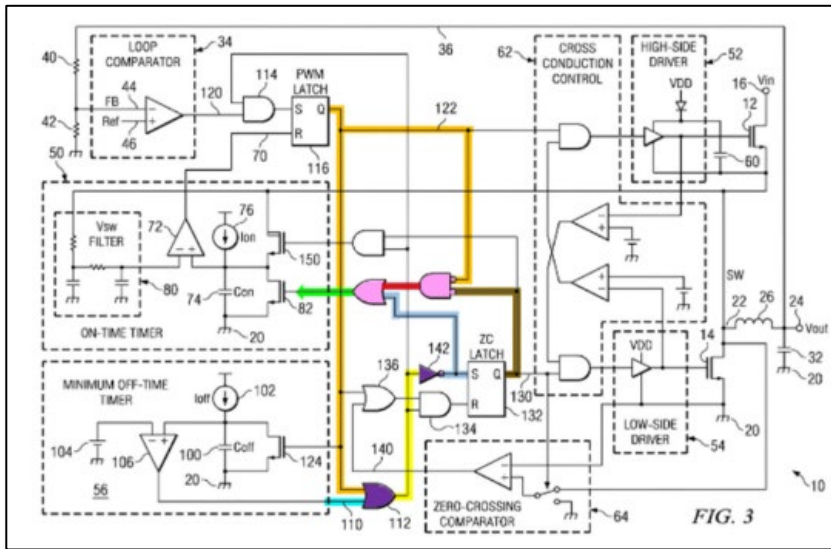
- Q: And in this case it's coupled via a NOR gate?
- A: A NOR gate and an inverter.
- Q: Right, and your position is that NOR gate and that inverter do not change the signal that is output by the flip-flop at its output terminal?
- A: I've never said that. No, I've never said that. That is your surmising that somehow the signal has to be on the output terminal of the flip-flop. There's no restriction in this claim for that at all. There is a flip-flop that has three terminals, including an output terminal, but the only restriction in the claim for the output terminal is that it's coupled to the power stage. And so that's different than the generation of the signal. The signal is not something that's coupled. It's the coupling to the output stage -- excuse me, it's the power stage coupled to the output terminal. The flip-flop is also coupled to receive the control signal but it doesn't have to be literally the node on the output of the flip-flop. And I think that the way I have read this is correct and that's why I pointed to the PWMHS as the signal because that is the signal that's generated by the flip-flop. There's coupling of circuitry as well is required, but that signal that is generated, PWMHS is the signal. That control signal is the control signal that's received by the power stage.
- Q: Is PWMHS the signal that is generated by the flip-flop at its output?
- A: There's nothing in the claim limitation that does what you just said. You just said it generates the control signal at the output. There's nothing in the claim that says that.



Ex. 1020 (J. McAlexander 9/18/2025 Dep. Tr.), 183:7-25, 184:1-12, 14-17

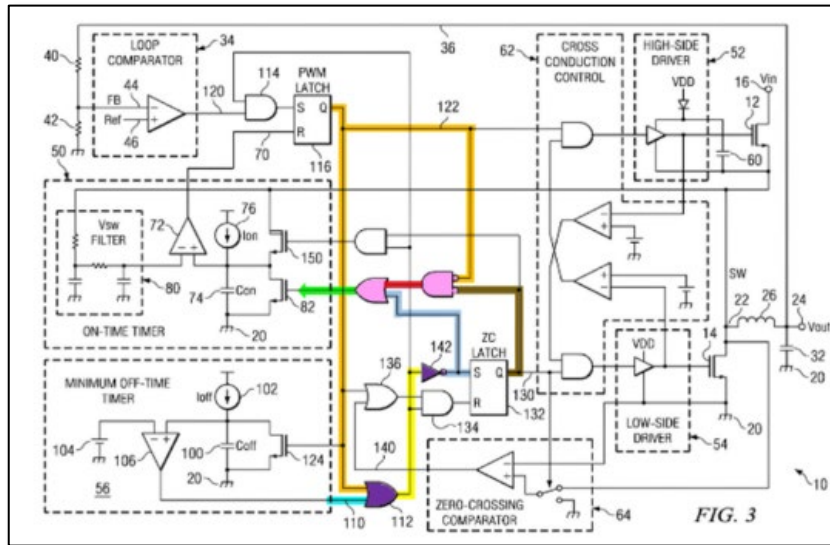
Patent Owner argues in this IPR that combining signals from the ZC latch into the control signal changes the signal

- In their Response, Patent Owner asserts:
- “The logical state of the orange signal does not define the state of the green signal, and there is mismatch in states between the two signals.”

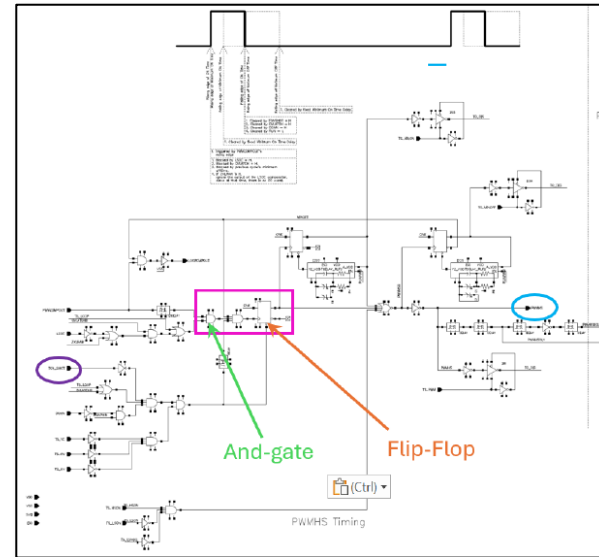


Patent Owner, in U.S. District Court, ignores signals combined into the “control signal” for their infringement analysis

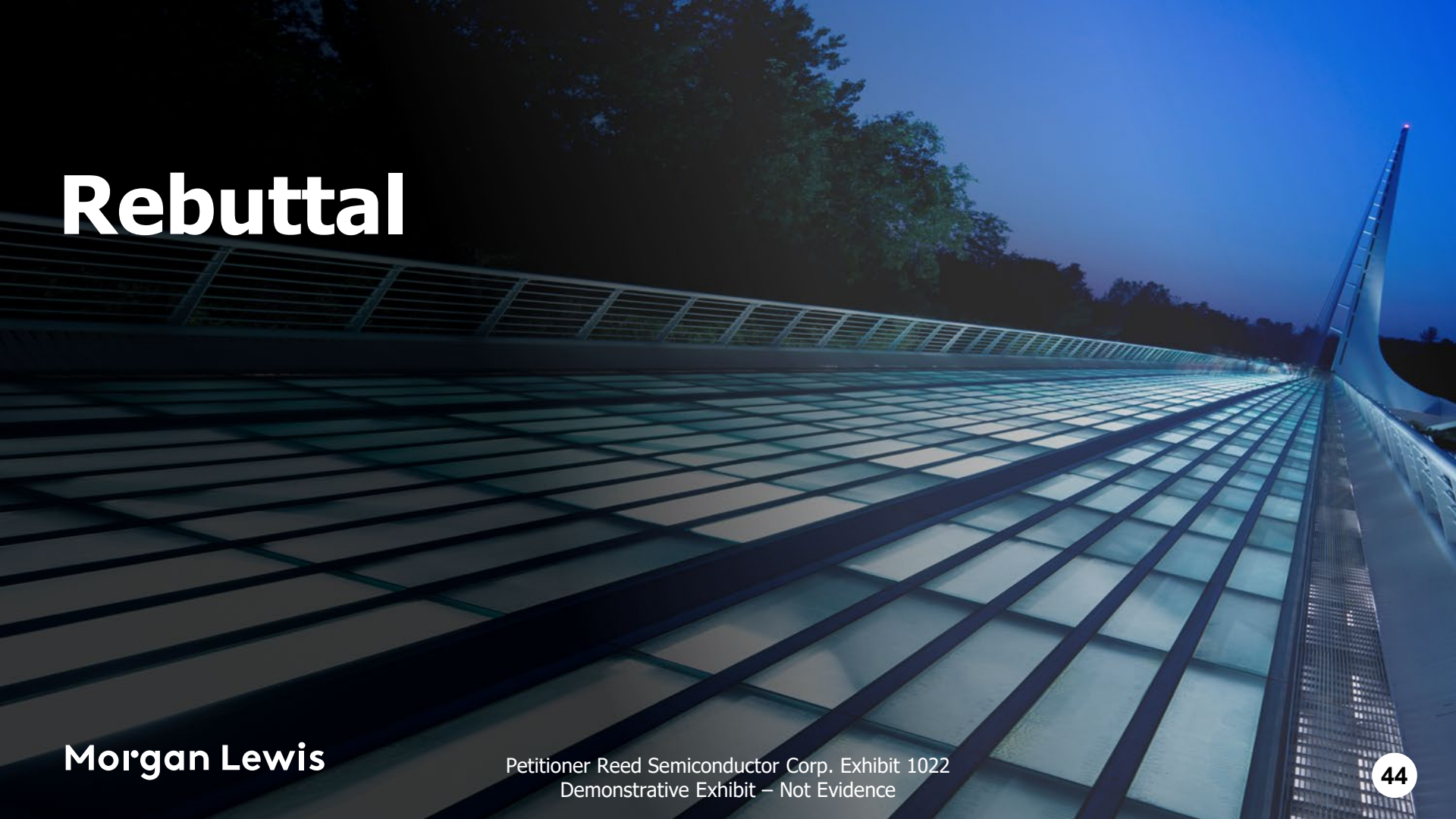
Tateishi FIG. 3



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Rebuttal

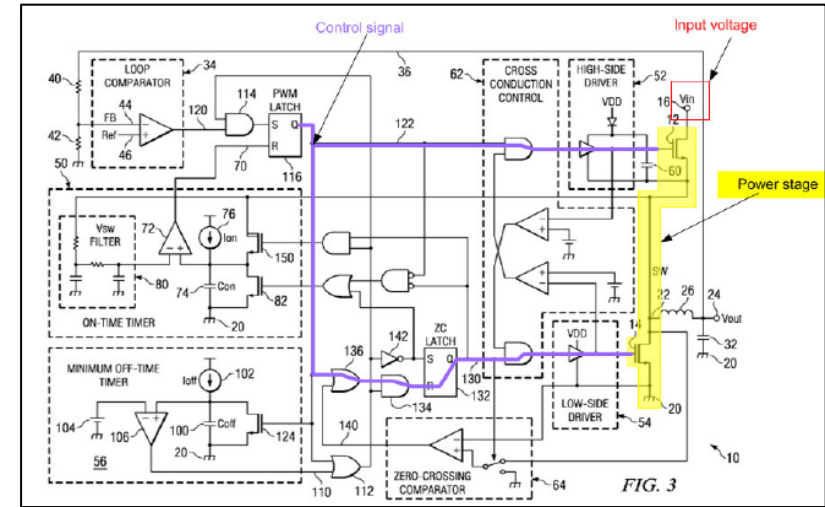


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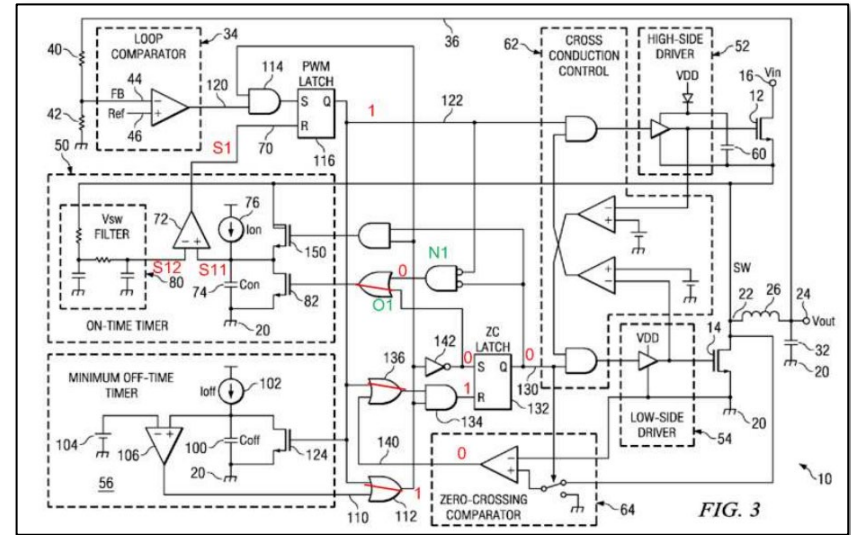
Tateishi Anticipates Claim 1: The “control signal” is received by the “power stage”

- an on-time generator comprising:
 - an input voltage sensing circuit having . . . a second input terminal . . . , wherein . . . **the second input terminal is configured to receive a control signal**
 - a logic control circuit coupled to the on-time generator . . . **the logic control circuit generates the control signal**
- a **power stage** configured to receive an input voltage and **the control signal**.



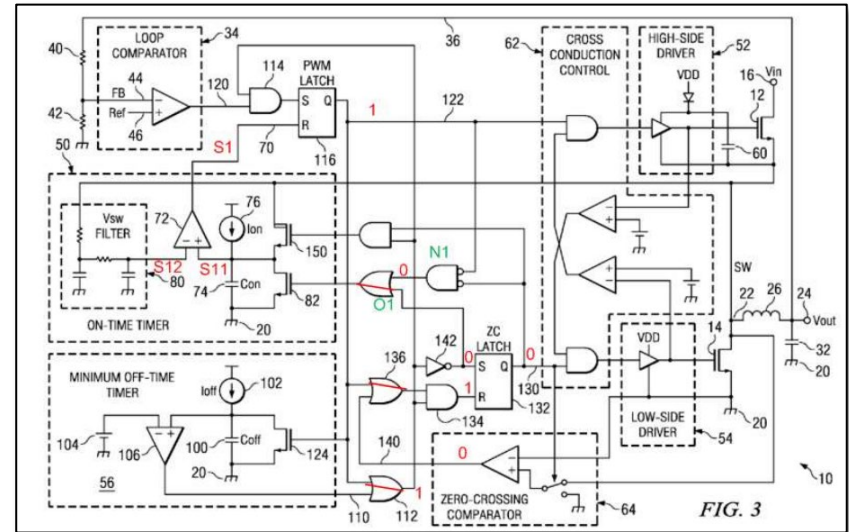
While ZC latch is off (0), a pass through via the logic is created for the control signal

- Patent Owner claims that signals from the ZC latch combined with the control signal generates a new signal
- When the ZC latch is 0 ($S = 0$ and signal 130 = 0), it creates a pass through for the control signal
- When the PWM latch 116 outputs a 1 for the control signal 122, the 1 passes through the AND gate with inverted inputs and the OR gate

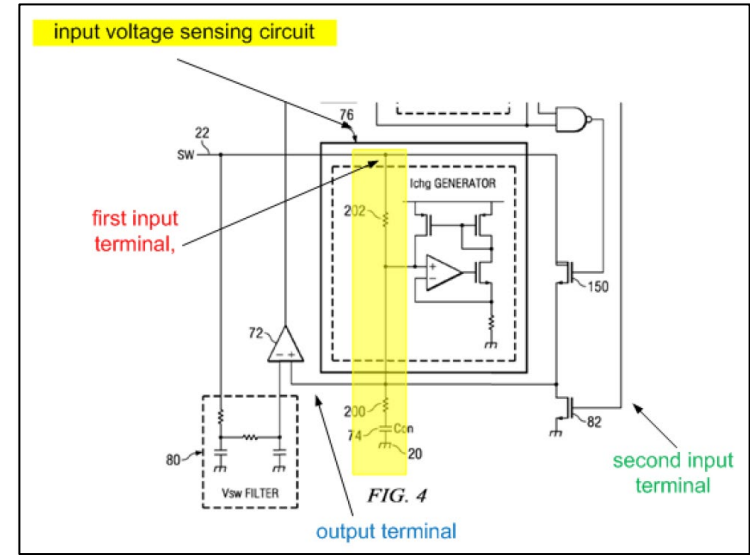
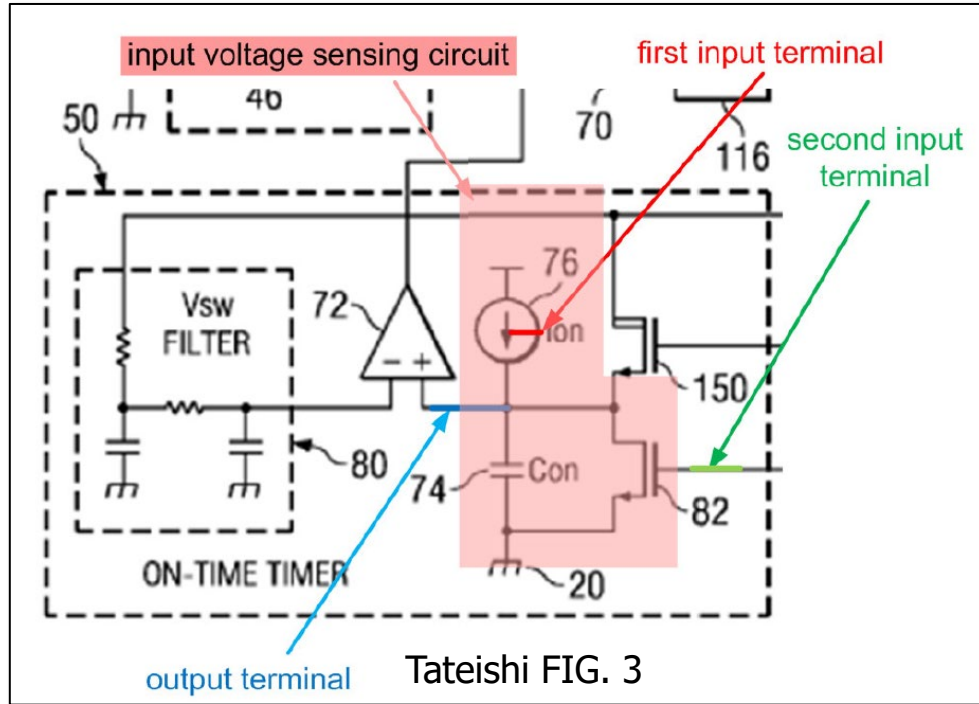


While ZC latch is off (0), a pass through via the logic is created for the control signal

- When the ZC latch is 0 (S = 0 and signal 130 = 0), it creates a pass through for the control signal
- When the PWM latch 116 outputs a 1 for the control signal 122, the 1 passes through the AND gate with inverted inputs and the OR gate



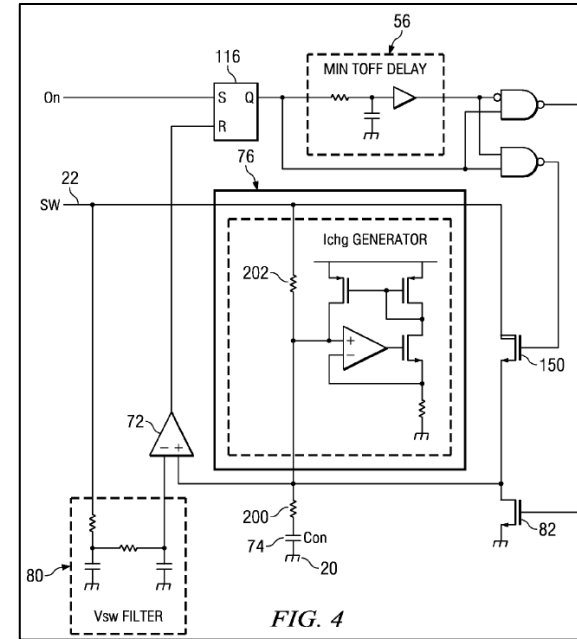
Tateishi's discloses receiving the switching signal



Claims 5, 7-8, and 15 are rendered obvious by Tateishi

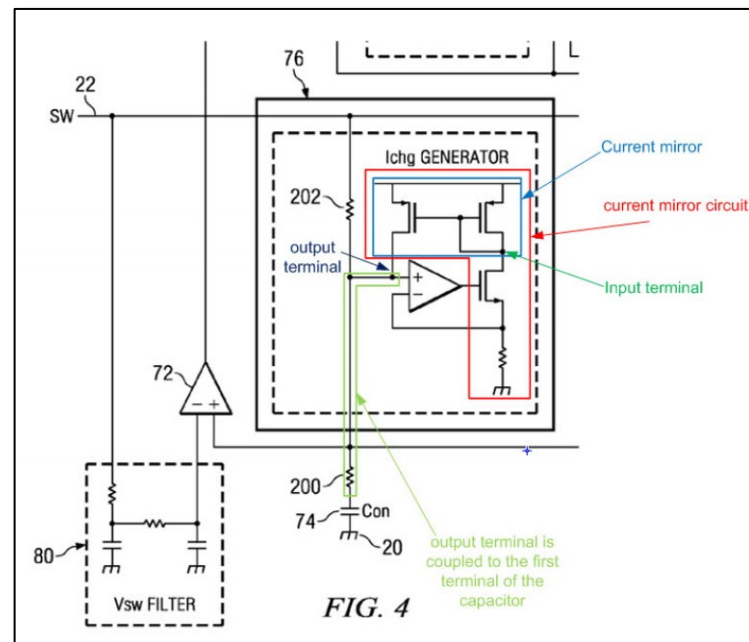
FIG. 4 of Tateishi illustrates an embodiment of a DC to DC buck converter including portions of the on-time timer

FIG. 4 illustrates each claim limitation present in claims 5, 7-8, and 15



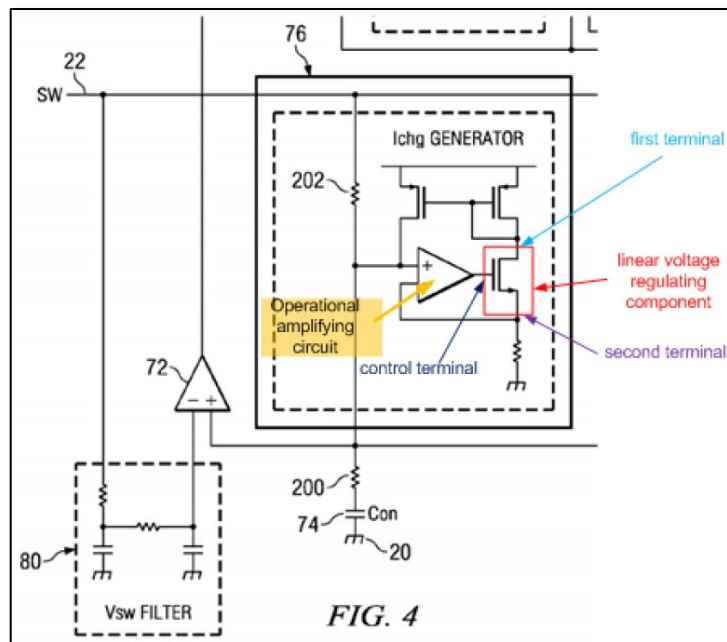
Tateishi Anticipates Claims 5 and 15

- **Claim 5.** The step-down regulator of claim 4, wherein the **current mirror circuit** comprises:
 - a **current mirror** having an **input terminal** and an **output terminal**, wherein the **output terminal** is coupled to the **first terminal of the capacitor** to provide the linear compensation current;
 - a first linear voltage regulating component having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the output terminal of the operational amplifying circuit, the first terminal is coupled to the input terminal of the current mirror; and
 - a second resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first linear voltage regulating component, and the second terminal is grounded, further wherein the first resistor and the second resistor have the same resistance.
- Claim 15 includes features analogous to claim 5.



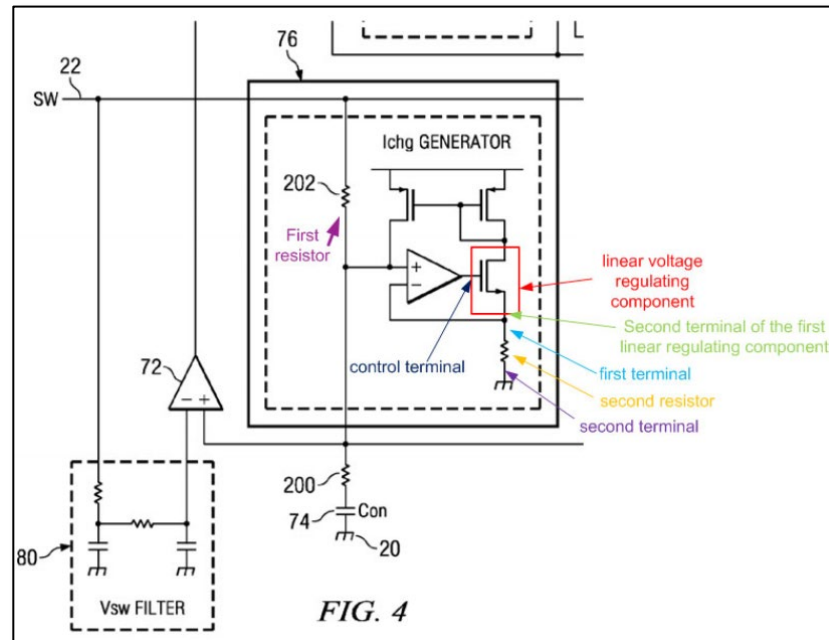
Tateishi Anticipates Claims 5 and 15

- **Claim 5.** The step-down regulator of claim 4, wherein the current mirror circuit comprises:
 - a current mirror having an input terminal and an output terminal, wherein the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current;
 - a first linear voltage regulating component having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the output terminal of the operational amplifying circuit, the first terminal is coupled to the input terminal of the current mirror; and
 - a second resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first linear voltage regulating component, and the second terminal is grounded, further wherein the first resistor and the second resistor have the same resistance.
- Claim 15 includes features analogous to claim 5.



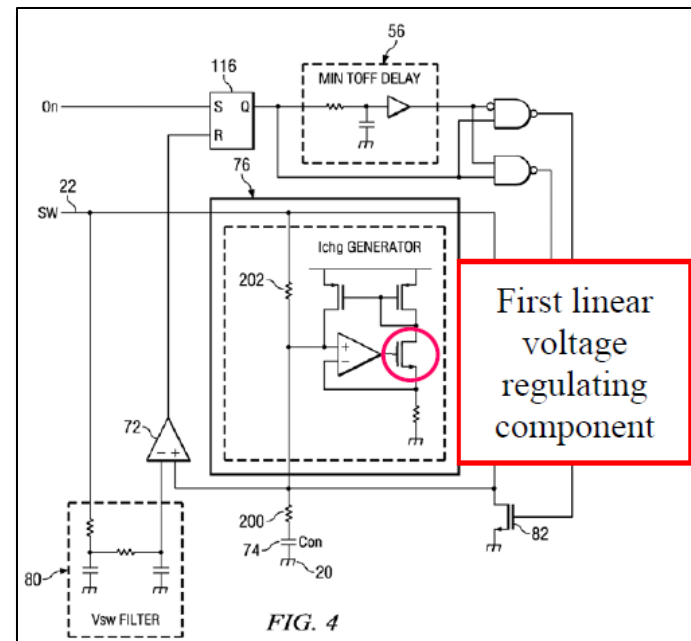
Tateishi Anticipates Claims 5 and 15

- **Claim 5.** The step-down regulator of claim 4, wherein the current mirror circuit comprises:
 - a current mirror having an input terminal and an output terminal, wherein the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current;
 - a first linear voltage regulating component having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the output terminal of the operational amplifying circuit, the first terminal is coupled to the input terminal of the current mirror; and
 - **a second resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first linear voltage regulating component, and the second terminal is grounded, further wherein the first resistor and the second resistor have the same resistance.**
- Claim 15 includes features analogous to claim 5.



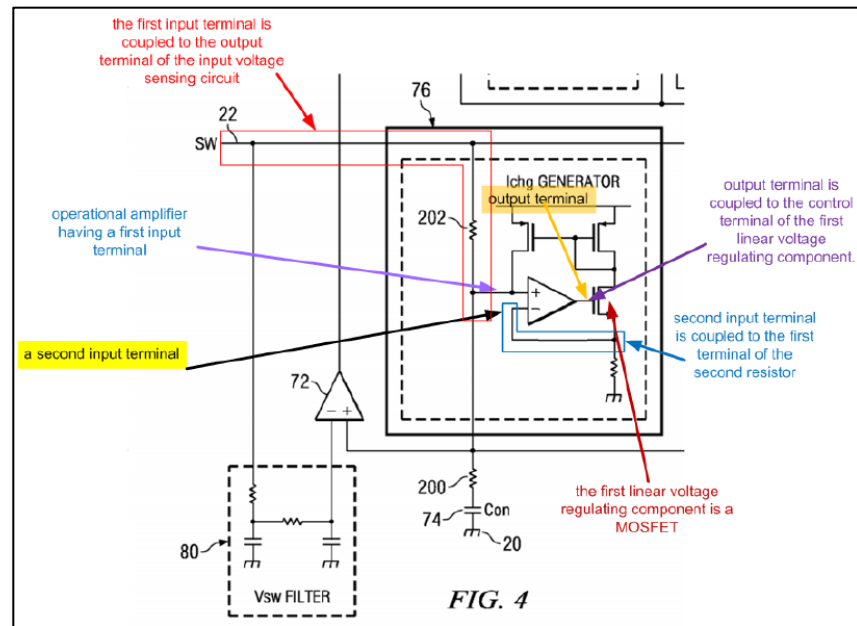
Tateishi Anticipates Claim 7

Claim 7. The step-down regulator of claim 5, wherein the first linear voltage regulating component is a MOSFET or a BJT.



Tateishi Anticipates Claim 8

Claim 8. The step-down regulator of claim 5, wherein the operational amplifying circuit comprises an operational amplifier having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the first terminal of the second resistor, and the output terminal is coupled to the control terminal of the first linear voltage regulating component.



Patent Owner's Proposed Claim Construction of "Control Signal" is Too Narrow

Institution Decision

On the present record at this preliminary point in the proceeding and for purposes of this decision, we decline to read the word "logical" into the term "control signal," we do not construe the claim term as excluding logic gates between the logic control circuit output and the second input terminal of the input voltage sensing circuit, and we do not construe the claims such that the "control signal" must be the exclusively controlling factor of a component.

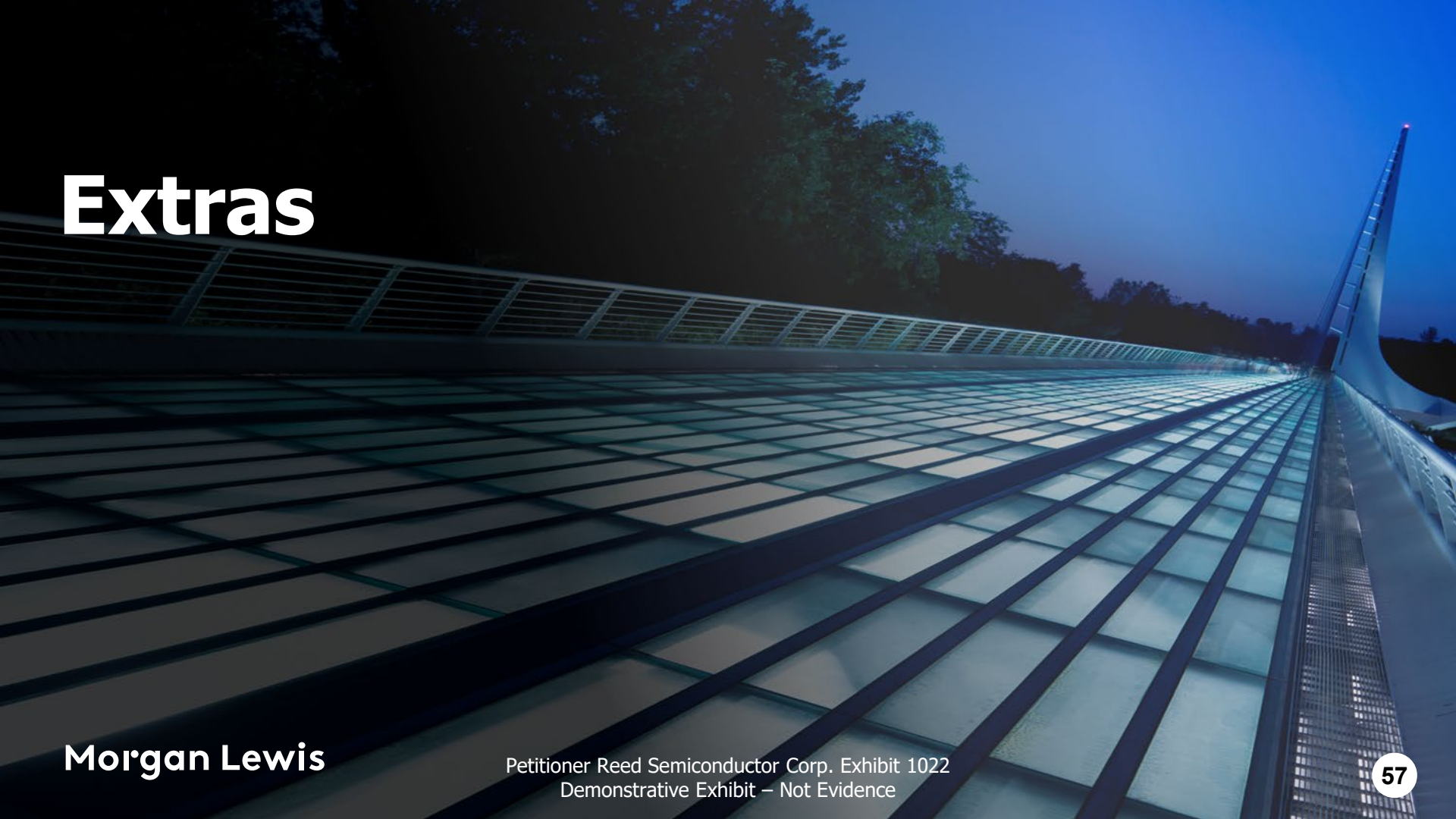
Patent Owner's Response

A POSITA would accordingly understand that the claimed control signal's plain and ordinary meaning is a logic signal with two distinct states. (EX2005, ¶ 56.)

Institution Decision: Patent Owner's construction of "control signal" is too narrow

On the present record at this preliminary point in the proceeding and for purposes of this decision, we decline to read the word "logical" into the term "control signal," we do not construe the claim term as excluding logic gates between the logic control circuit output and the second input terminal of the input voltage sensing circuit, and we do not construe the claims such that the "control signal" must be the exclusively controlling factor of a component.

Extras

A photograph of a modern building's glass and metal facade at dusk. The building features a grid-like pattern of glass panels and dark metal framing. A prominent glass pyramid structure is visible on the right side, illuminated from within. The sky is a deep blue, and trees are visible in the background.

Morgan Lewis

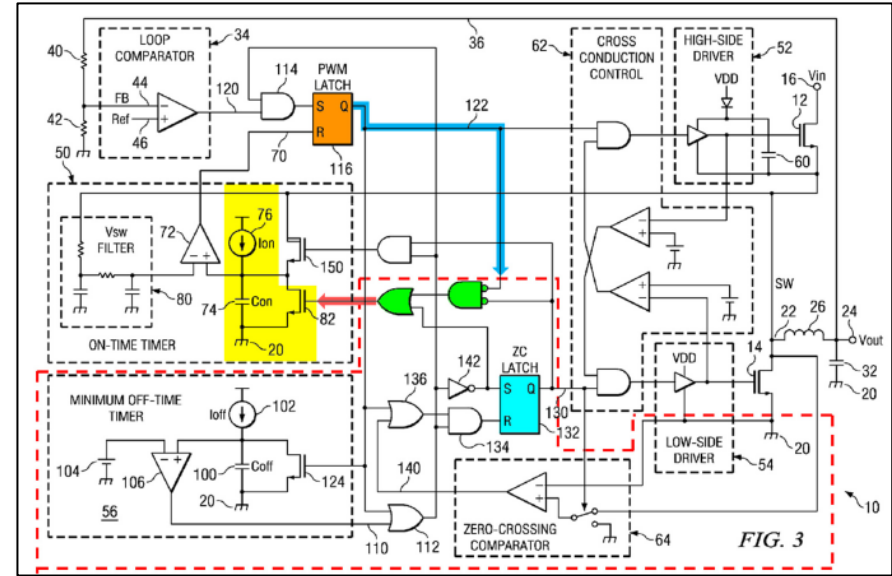
Petitioner Reed Semiconductor Corp. Exhibit 1022
Demonstrative Exhibit – Not Evidence

“Control signal” should be construed in accordance with its plain and ordinary meaning

A control signal is “a signal configured to control a circuit component”

Tateishi's control signal 122 controls the "input voltage sensing circuit" and "power stage" as claimed

- Tateishi teaches that the Q signal output by the PWM latch 116 is the signal that is used to control the on-time generator.
- Tateishi does not disclose any other signal that could be used to control the on-time generator.

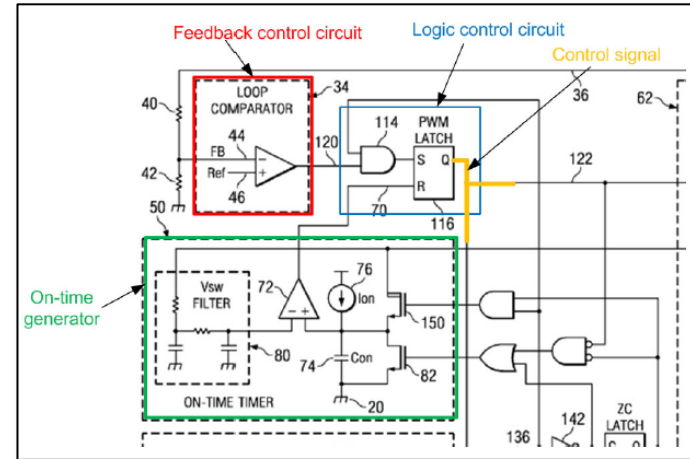
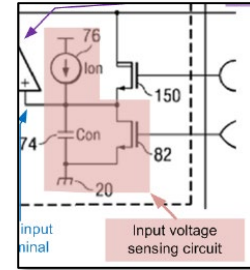


'377 Patent: Claim 1 Excerpts

- A step-down regulator, comprising:
- a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:
 - an on-time generator comprising:
 - an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, **the second input terminal is configured to receive a control signal** provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the **control signal**, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;
 - a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, **the logic control circuit generates the control signal**; and
- **a power stage configured to receive** an input voltage and **the control signal**, wherein based on the input voltage and the control signal, the power stage generates the switching signal.

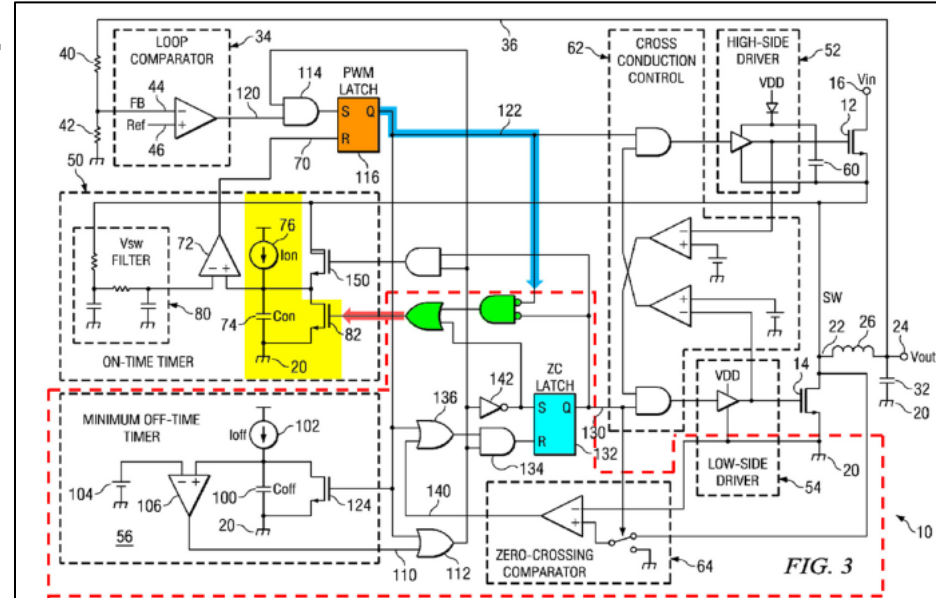
Tateishi Anticipates Claim 1

- an on-time generator comprising:
 - an input voltage sensing circuit having . . . a second input terminal . . . , wherein . . . **the second input terminal is configured to receive a control signal**
 - a logic control circuit coupled to the on-time generator . . . **the logic control circuit generates the control signal**
- a power stage configured to receive an input voltage and **the control signal**.



Tateishi Anticipates Claim 1

- an on-time generator comprising:
 - an **input voltage sensing circuit** having . . .
. . . a second input terminal . . ., wherein . . .
. . . **the second input terminal is configured to receive a control signal**
 - a **logic control circuit** coupled to the on-time generator . . . **the logic control circuit generates the control signal**
- **a power stage configured to receive an input voltage and the control signal.**



Plain and Ordinary Meaning of “Control Signal” Captures Patent Owner’s Construction

Plain and ordinary meaning of “control signal:” a “signal configured to control a circuit component.”

Patent Owner’s Expert Agrees with Plain and Ordinary Meaning of Control Signal

The term “control signal” should be construed in accordance with its plain and ordinary meaning as a “signal configured to control a circuit component” because this construction is consistent with the intrinsic and extrinsic evidence. Indeed,

Transcript of Joseph McAlexander, III
Conducted on July 1, 2025 121

1 Q So in the context of the '377 patent, you would
2 agree that a control signal is a signal that controls
3 other circuit components, correct?
4 A I would agree with that, yes.

Patent Owner's Expert states that the flip flop generates the PWMHS signal, but later states the PWMHS signal is generated after the NOR gate

- Q: When the signal that's generated passes through the NOR gate, is it changed?
- A: Well, again, you're still trying to go back to the other language which is written differently. This language, the two inputs are coupled to receive signals and that flip-flop does have two terminal inputs and an output. But the claim language does not require that's on the output pin, the output node. It just says that the flip-flop has three terminals. But when it comes to the generation, it generates the control signal. And I'm saying the signal that it generates is the one that's over the PWMHS. That is the signal that's generated.

Patent Owner's Expert states that the flip flop generates the PWMHS signal, but later states the PWMHS signal is generated after the NOR gate (cont.)

- Q: And where does that PWMHS signal get generated?
- A: It gets generated in the flip-flop, as I have shown.
- Q: But you disagree that the PWMHS signal generated by the flip-flop passes through any logic before being received by the power stage?
- A: I'm not aware of the PWMHS signal passing through any additional logic before it gets to the power stage, and I'm sitting here looking at the schematic.
- Q: Does the PWMHS signal generated by the flip-flop pass through a NOR gate and an inverter prior to reaching the power stage?
- A: Again, the PWMHS signal is after the NOR gates that you refer to. So no, it doesn't pass through those gates in order to get to the power stage.

Patent Owner **mischaracterizes** the intervening logic as a buffer

- Patent Owner states “[t]he intervening circuitry accused of infringement in the litigation is a buffer . . .” Paper 40, p. 3.
- A buffer in logic is the equivalent of two inverters
- Patent Owner incorrectly assumes that the “the PWMHS signal is a double inversion to the NOR,” is equivalent to a buffer

