UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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REED SEMICONDUCTOR CORP.,

Petitioner,

v.

MONOLITHIC POWER SYSTEMS, INC.,

Patent Owner,

_____

Case No. IPR2024-01158
Patent 9,041,377 B2

_____

PATENT OWNER'S NOTICE OF APPEAL

Via PTAB P-TACTS
Patent Trial and Appeal Board

Via email to efileSO@uspto.gov
Director of the United States Patent and Trademark Office
c/o Office of the Solicitor

Via CM/ECF
United States Court of Appeals for the Federal Circuit

NOTICE OF APPEAL TO THE FEDERAL CIRCUIT

Notice is hereby given, pursuant to 35 U.S.C. §§ 141(c), 142; 35 U.S.C. § 319; 28 U.S.C. § 1295; and 37 C.F.R. §§ 90.2(a), 90.3(a), that Patent Owner Monolithic Power Systems, Inc. ("MPS") hereby appeals to the United States Court of Appeals for the Federal Circuit from the Patent Trial and Appeal Board's Final Written Decision in IPR2024-01158, entered on January 22, 2026 (Paper 49) (the "Final Written Decision") wherein the Board determined All Challenged Claims as Unpatentable in *inter partes* review of U.S. Patent No. 9,041,377 ("the '377 Patent") in IPR2024-01158, attached hereto as Exhibit A, and from all underlying findings, determinations, orders, issues, decisions, rulings, and opinions. This notice is timely under 37 C.F.R. § 90.3(a)(1), having been filed within 63 days after the Final Written Decision.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner further states that the issues on appeal are anticipated to include, but are not limited to:

(1) The Board's conclusion that Claims 1-4, 9-14, 17, and 18 of U.S. Patent No. 9,041,377 have been shown to be unpatentable as anticipated by U.S. Pub. No. 2009/0140708 ("Tateishi");

(2) The Board's conclusion that Claims 5, 7, 8, 15 of U.S. Patent No. 9,041,377 have been shown to be unpatentable as anticipated and obvious by U.S. Tateishi and U.S. Pat. No. 8,476,887 ("Tateishi Patent");

(3) Any Board finding, determination, judgment, or order supporting or related to the Final Written Decision and decided adversely to Patent Owner MPS.

Patent Owner reserves the right to raise on appeal any finding or determination related to the issues listed above and to raise any other issue decided adversely to the Patent Owner in the proceedings underlying the Decision.

Concurrently with this submission, a copy of this Notice of Appeal with the Director of the United States Patent and Trademark Office, and a copy of this Notice of Appeal is being filed electronically with the United States Court of Appeals for the Federal Circuit along with the required docketing fee as set forth in the accompanying Certificates of Filing and Service.

Dated: March 26, 2026

Respectfully submitted,

By: */ Miguel Bombach/*

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CERTIFICATE OF FILING

The undersigned hereby certifies that in addition to being filed electronically through the Patent Trial and Appeal Board's P-TACTS system, a true and correct copy of the foregoing **PATENT OWNER'S NOTICE OF APPEAL OF FINAL WRITTEN DECISION** is also being filed pursuant to 37 C.F.R. § 90.2(a) with the Director of the United States Patent and Trademark Office on March 26, 2026, by electronic mail to efileSO@uspto.gov which is the email address indicated on the U.S. Patent and Trademark Office's web page for the Office of the General Counsel.

I further certify that a true and correct copy of the foregoing **PATENT OWNER"S NOTICE OF APPEAL OF FINAL WRITTEN DECISION** along with the filing fee is being filed via CM/ECF with the Clerk's Office of the United States Court of Appeals for the Federal Circuit on March 26, 2026.

Dated: March 26, 2026

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that on March 26, 2026, a complete and entire copy of the foregoing **PATENT OWNER'S NOTICE OF APPEAL OF FINAL WRITTEN DEICISION with Exhibit A** was electronically served by email, pursuant to 37 C.F.R. 42.6(e) to counsel of record for Petitioner as addressed below:

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The undersigned further certifies that, in addition to being filed electronically through the Patent Trial and Appeal Case Tracking System on March 26, 2026, a true and correct copy of the foregoing **PATENT OWNER'S NOTICE OF APPEAL OF FINAL WRITTEN DECISION with Exhibit A** was served on March 26, 2026, on the Director of the United States Patent and Trademark Office at the following email and mailing address:

Via email efileSO@uspto.gov
Director of the United States Patent and Trademark Office
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Dated: March 26, 2026

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EXHIBIT A

Trials@uspto.gov
571-272-7822

Paper 49
Date: January 22, 2026

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,
Petitioner,

v.

MONOLITHIC POWER SYSTEMS, INC.,
Patent Owner.

IPR2024-01158
Patent 9,041,377 B2

Before JEAN R. HOMERE, KARL D. EASTHOM, and
KEN B. BARRETT, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Reed Semiconductor Corp. ("Petitioner")[1] filed a Petition requesting *inter partes* review of U.S. Patent No. 9,041,377 B2 ("the '377 patent," Ex. 1001). Paper 1 ("Pet."). The Petition challenges the patentability of claims 1–5, 7–15, 17, and 18 of the '377 patent. We instituted an *inter partes* review of all challenged claims on all proposed grounds of unpatentability. Paper 6. Monolithic Power Systems, Inc. ("Patent Owner")[2] filed a Response to the Petition. Paper 23 ("PO Resp."). Petitioner filed a Reply (Paper 26, "Pet. Reply") and Patent Owner filed a Sur-reply (Paper 31, "PO Sur-reply").

An oral hearing was held on October 23, 2025, and a transcript of the hearing is included in the record. Paper 48 ("Tr.").

Patent Owner filed a motion to strike portions of Petitioner's Reply, arguing that "Petitioner's Reply introduces a new anticipation theory based on an embodiment (Figure 1) [of Tateishi] that is different than the [Figure 3] embodiment relied on in the Petition." Paper 27, 1. Petitioner filed an opposition. Paper 28. The Board "preliminarily determine[d] that the Petition did not give notice to Patent Owner (or the Board) that Petitioner is presenting an anticipation theory based on the signal(s) path of Figure 1," but denied Patent Owner's request to strike portions of the Reply. Paper 29,

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[1] Petitioner identifies Reed Semiconductor Corp., Nengda Microelectronics (Shenzen) Co., Ltd., and Nengda Semiconductor Technology (Shenzen) Co., Ltd. as real parties in interest. *See, e.g.*, Pet. 87.
[2] Patent Owner identifies Monolithic Power Systems, Inc. as the real party in interest. Paper 4, 2.

5–6. The Board stated that, "[i]n this case, we are capable of identifying belatedly presented arguments, particularly where Patent Owner has raised the objection, and the exceptional remedy [of striking portions of a brief] is not appropriate," and that, "[i]n reaching a final decision in this proceeding, we will consider only timely presented arguments and will not consider belatedly raised theories or any arguments that exceed the proper scope of the Reply." *Id.* at 6 (citing Patent Trial and Appeal Board's Consolidated Trial Practice Guide 80 (available at https://www.uspto.gov/TrialPracticeGuideConsolidated[3]). At the oral argument, Petitioner confirmed that it is not relying on Tateishi's Figure 1 as an anticipatory reference. *See* Tr. 17:13–19:8.

After the conclusion of the merits briefing authorized in the Scheduling Order, Petitioner moved to submit supplemental information. Paper 37. Petitioner argued in the motion that Patent Owner's witness, Mr. Joseph C. McAlexander III, has taken in the District Court and in this *inter partes* review contradictory positions regarding the meaning of the claim term "control signal" for infringement and patentability purposes. *See id.* at 1–3. Patent Owner filed an opposition to the motion. Paper 40. We granted the motion, stating that "[w]e determine, on the specific facts of this case, that Petitioner has made an adequate showing that the supplemental information reasonably could not have been obtained earlier," and that "it is in the interest of justice for Petitioner to submit the purportedly inconsistent opinions so that we can better assess the credibility of Mr. McAlexander." Paper 43, 5–6. The parties addressed the purported inconsistent opinions at

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[3] The Board recently transitioned to a web-based version of the Trial Practice Guide available at www.uspto.gov/patents/ptab/trial-practice-guide.

oral argument. *See, e.g.*, Tr. 20:1–23:26, 24:11–26:23. The parties declined the opportunity to further brief the issue of the purportedly inconsistent testimony. *See id.* at 49:19–52:22.

This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). For the reasons discussed below, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–5, 7–15, 17, and 18 of the '377 patent are unpatentable.

B. Related Proceedings

Both parties identify, as matters involving or related to the '377 patent, *Monolithic Power Systems, Inc. v. Reed Semiconductor Corp.*, No. 1:24-cv-00165-JFM (D. Del. filed February 8, 2024) and *Monolithic Power Systems, Inc. v. Nengda Microelectronics (Shenzhen) Co. Ltd.*, No. 1:24-cv-00166-JFM (D. Del. filed February 8, 2024). *See, e.g.*, Pet. 87–88; Paper 4, 2.

C. The '377 Patent

The '377 patent "relates generally to switching circuits, and more particularly but not exclusively to a pseudo constant on time control circuit and step-down regulators using it." Ex. 1001, 1:13–16. The '377 patent explains that, in a system using constant-on-time (COT) control techniques, the regulator's switching frequency varies with the output power. *See id.* at 1:20, 1:29–31. "To solve the problem of variable switching frequency in the COT control, pseudo constant on time (PCOT) control is used in step-down regulators." *Id.* at 1:34–36. "In PCOT control, the on time T_{on} of the regulator is proportional to the ratio of the output voltage V_{out} to the input Voltage V_{in}," and "the switching frequency F_{sw} of the step-down regulator remains constant and does not vary with the output power." *Id.* at 1:56–58,

2:8–10. However, some prior art PCOT step-down regulators required an output voltage pin and may have needed a frequency setting pin and/or an external frequency setting resistor, which caused larger package size and higher cost. *Id.* at 2:11–20.

In an embodiment of the '377 patent, "[t]he PCOT control circuit can receive the information of the output voltage V_{out}, without the output voltage pin VOUT, and can also receive the information of the input voltage V_{in}, without the frequency setting pin FREQ and the external frequency setting resistor R_{TON}," and, "[t]hus, when the PCOT control circuit is used in the step-down regulators, the chip size and the cost are both reduced." *Id.* at 7:57–64 (referring to the embodiment of Figure 9).

Figure 2 is reproduced below.

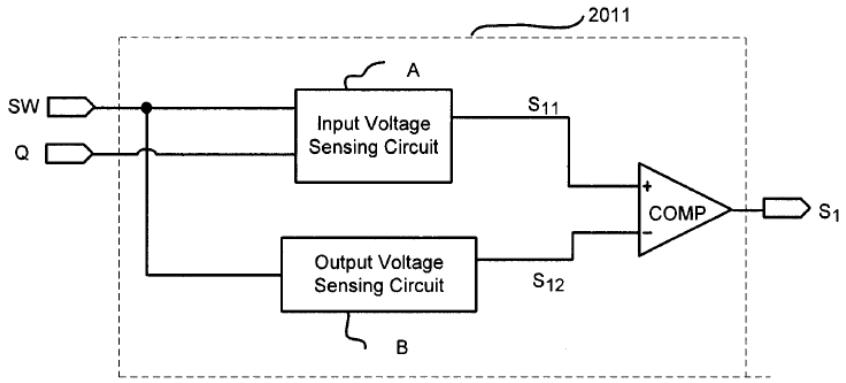

Figure 2 illustrates on-time generator 2011. *Id.* at 4:42.

> [T]he on-time generator 2011 comprises an input voltage sensing circuit A, an output voltage sensing circuit B and a comparator COMP. The input voltage sensing circuit A receives a switching signal SW provided by a stepdown regulator and a control signal Q provided by a PCOT control circuit, and provides an input voltage sensing signal S_{11} to the non-inverting input terminal of the comparator COMP. The output voltage sensing circuit B receives the switching signal SW, and provides an output voltage sensing signal S_{12} to the inverting input terminal of the comparator COMP. The comparator COMP compares the input

> voltage sensing signal S_{11} with the output voltage sensing signal S_{12} to generate an on-time signal S_1.

Id. at 4:46–58.

Figure 3 is reproduced below.

FIG. 3

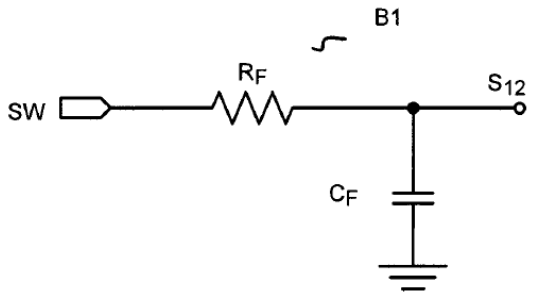

Figure 3 illustrates output voltage sensing circuit B1. *Id.* at 4:59. As shown, this circuit receives, as an input, switching signal SW, and provides output voltage sensing signal S_{12}. *See id.* at 4:61–5:3.

Figure 4 is reproduced below.

FIG. 4

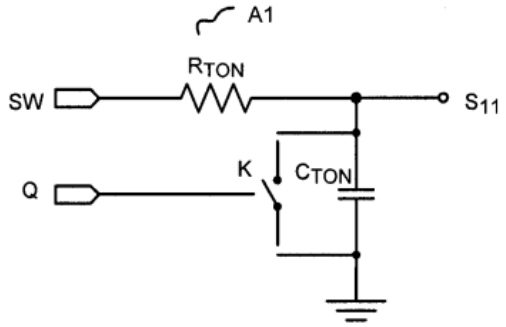

Figure 4 illustrates input voltage sensing circuit A1. *Id.* at 5:14.

> As shown in FIG. 4, the input voltage sensing circuit A1 comprises a resistor R_{TON}, a capacitor C_{TON} and a switch K. The first terminal of the resistor R_{TON} receives the switching signal SW . . . [and one] terminal of the capacitor C_{TON} is coupled to ground. The switch K is coupled to the capacitor C_{TON} in parallel and controlled by the control signal Q. [T]he output terminal of the input voltage sensing circuit A1 . . . provides the input voltage sensing signal S_{11}.

Id. at 5:14–27.

Figure 11 is reproduced below.

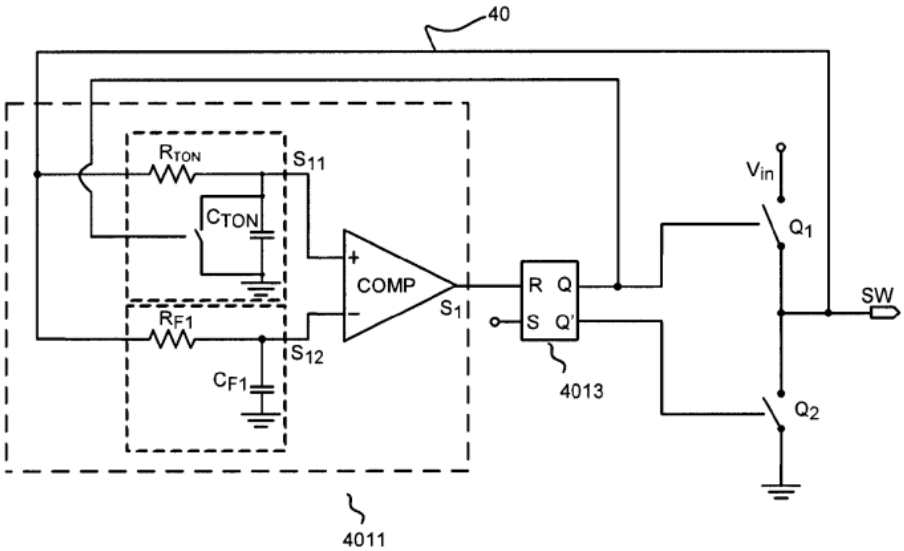

FIG. 11

Figure 11 illustrates a step-down regulator. *Id.* at 8:18.

> As shown in FIG. 11, the step-down regulator 40 comprises an on-time generator 4011, a flip-flop 4013 and a power stage configured by switches Q_1 and Q_2. The on-time generator 4011 comprises the input voltage sensing circuit A1 of FIG. 4 and the output voltage sensing circuit B1 of FIG. 3. . . . [T]he feedback control circuit is not shown in the step-down regulator 40.
>
> As shown in FIG. 11, the on-time generator 4011 receives the switching signal SW provided by the step-down regulator 40 and the control signal Q provided by the flip-flop 4013, and provides an on-time signal S_1 to the reset terminal of the flip-flop 4013. The control signal Q controls the high-side switch Q_1, and the complementary signal Q' of the control signal Q controls the low-side switch Q_2. The first terminal of the high-side switch Q_1 receives the input voltage V_{in}, and the second terminal of high-side switch Q_1 is coupled to the first terminal of the low-side switch Q_2. The second terminal of the low-side switch Q_2 is coupled to ground. The second terminal of the high-side switch Q_1 and the first terminal of the low-side switch Q_2 are configured as the output terminal of the step-down regulator 40 and output the switching signal SW.

Id. at 8:19–41.

As shown in Figure 11 above, comparator COMP is located between flip-flop 4013 and the input voltage sensing and output voltage sensing circuits.

> When the voltage at the non-inverting input terminal of the comparator COMP reaches the output voltage sensing signal S_{12} provided by the output voltage sensing circuit, the on-time signal S_1 becomes logical high, that is, S_1=1. The on-time signal S resets the flip-flop 4013 to change the control signal Q into logical low (Q=0). Thus, the high-side switch Q_1 is turned off, and the low-side switch Q_2 is turned on, the switching signal SW equals to 0. Meanwhile, the switch K [which is coupled to the capacitor C_{TON} in parallel] is turned on by the control signal Q, the capacitor C_{TON} is discharged, and the voltage at the non-inverting input terminal of the comparator COMP decreases rapidly to its initial value.

Id. at 8:49–60; *see id.* at 5:21–22 (describing the location of switch K as labeled in Figure 4).

D. Illustrative Claim

Of the challenged claims of the ’377 patent, claims 1, 11, and 18 are independent claims. Claim 1, reproduced below with bracketed annotations inserted, is illustrative.

> 1. [1Pre] A step-down regulator, comprising:
>
> [1A] a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:
>
> [1B1] an on-time generator comprising:
>
> [1B2] an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal,

the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

[1B3] an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and

[1B4] a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;

[1C] a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to generate an output signal in accordance with the feedback signal; and

[1D] a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal; and

[1E] a power stage configured to receive an input voltage and the control signal, wherein based on the input voltage and the control signal, the power stage generates the switching signal.

Ex. 1001, 9:36–10:13.

E. Evidence

Petitioner relies on the following references:

Name	Reference	Exhibit No.
Tateishi	US 2009/0140708 A1, filed Feb. 6, 2009, published June 4, 2009	1007
Tateishi Patent	US 8,476,887 B2, filed Feb. 6, 2009, issued July 2, 2013[4]	1005

Petitioner also relies on the declarations of Dr. Douglas Holberg (Exs. 1003, 1016) in support of its arguments, and Patent Owner relies on the declarations of Joseph C. McAlexander III, P.E. (Exs. 2001, 2005) in support of its arguments. The parties also rely on other exhibits as discussed below.

F. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §[5]	Reference(s)/Basis
1–4, 9–14, 17, 18	102(b)	Tateishi
1–4, 9–14, 17, 18	102(e)	Tateishi Patent
5, 7, 8, 15	103(a)	Tateishi, Tateishi Patent

[4] The Tateishi Patent issued from the application that was published as the Tateishi reference.

[5] The application that issued as the ’377 patent was filed before the effective date of the Leahy Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), and we apply the pre-AIA versions of 35 U.S.C. §§ 102 and 103.

II. ANALYSIS

A. Principles of Law

Petitioner bears the burden of persuasion to prove unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail, Petitioner must establish by a preponderance of the evidence that the challenged claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987); *see also Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1334 (Fed. Cir. 2008) (to anticipate a patent claim under 35 U.S.C. § 102, "a single prior art reference must expressly or inherently disclose each claim limitation"). Moreover, "[b]ecause the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'" *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). Whether a reference anticipates is assessed from the perspective of one of ordinary skill in the art. *See Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368–69 (Fed. Cir. 2003) ("'[T]he dispositive question regarding anticipation [i]s whether *one skilled in the art* would reasonably understand or infer from the [prior art reference's] teaching' that every claim element was disclosed in

that single reference." (second and third alterations in original) (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991))).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) if present, any objective evidence of obviousness or non-obviousness.[6] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. The Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (quoting *Custom Accessories, Inc. v. Jeffrey–Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986)).

Petitioner contends:

> A person of ordinary skill in the art ("POSITA") in the field of the '377 Patent, as of its earliest possible filing date of June 30, 2011, would have been someone knowledgeable about

[6] The parties have not directed our attention to any objective evidence of obviousness or non-obviousness.

> and familiar with step-down regulator technology that is pertinent to the '377 Patent. A POSITA would have had a bachelor's degree in Electrical Engineering or equivalent training, and approximately two years of experience working in the field of step-down regulators or related technologies. Lack of work experience can be remedied by additional education, and vice versa.

Pet. 27–28 (citing Ex. 1003 ¶¶ 18–19).

Patent Owner contends:

> A person of ordinary skill in the art ("POSITA") in the field of the '377 Patent, as of its priority date of June 30, 2011, would have had a bachelor's degree in Electrical Engineering or equivalent, and approximately two years of experience working the field of power converters, circuit design, device physics, or related technologies. Lack of work experience can be remedied by additional education and vice versa.

PO Resp. 6–7 (citing Ex. 2005 ¶ 32).

We discern no material difference between the parties' definitions. Petitioner's definition is consistent with the level of ordinary skill reflected in the prior art references of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (recognizing that the prior art itself may reflect an appropriate level of skill in the art). For purposes of this decision, we apply Petitioner's definition of the person of ordinary skill in the art. We note, however, that were we to adopt Patent Owner's assessment, the outcome of this Decision would be the same.

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b). In applying that standard, claim terms generally are given their ordinary and

customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). "[W]hile extrinsic evidence can shed useful light on the relevant art, . . . it is less significant than the intrinsic record in determining the legally operative meaning of claim language." *Phillips*, 415 F.3d at 1317 (internal quotation marks omitted).

Control Signal

Independent claim 1, for example, recites, "an input voltage sensing circuit having . . . [a] second input terminal [that] is configured to receive *a control signal* provided by the pseudo constant on time control circuit." Ex. 1001, 9:40–45 (limitation 1B2) (emphasis added). Claim 1 also recites that "the logic control circuit generates *the control signal*." *Id.* at 10:8–9 (limitation 1D) (emphasis added).

Independent claims 11 and 18 contain somewhat similar recitations regarding the "control signal," and the parties treat the independent claims as substantively the same in this regard. *See* Ex. 1001, 11:44–50, 12:11–12, 13:21–23, 14:18–19; *see also* Pet. 61, 63, 66, 72 (Petitioner's contentions, for the corresponding limitations of claims 11 and 18, relying primarily on the contentions for claim 1); PO Resp. 5–6 & 5 n.2 (Patent Owner annotating with color certain terms in claim 1, including "control signal" and stating that "[i]ndependent claims 11 and 18 recite similar limitations."). In

claim 18, the component that generates the "control signal" is labelled "the flip-flop." *See* Ex. 1001, 14:19–20.

Petitioner, characterizing limitation 1D, contends that "the logic control circuit generates the control signal of limitation 1[B2]." Pet. 43–44 (citing Ex. 1003 ¶ 95) (brackets in original). Patent Owner similarly contends that "[t]he claims introduce 'a control signal' [e.g., in the "input voltage sensing circuit" limitation 1B2] . . . and 'the control signal' is thereafter recited as being generated by specific hardware (e.g., a logic control circuit or flip-flop)." PO Resp. 20. Patent Owner asserts that the first occurrence of a "control signal" in the claims' provides antecedent basis for the subsequent recitation of the generated "control signal," and contends that "[t]he 'control signal' must be the same signal throughout each respective claim." *Id.* at 20–21. Thus, the parties agree that, in each independent claim, the two pertinent limitations refer to the same "control signal."

As discussed further below in the context of Petitioner's anticipation ground, Tateishi's circuitry path between the components that Petitioner contends are the output of the "control signal" generator (Q of PWM Latch 116) and the "control signal" receiver (transistor 82) includes logic gates, namely an AND gate with inverting inputs and an OR gate. *See* Pet. 35. The parties' dispute concerns these logic gates.

Petitioner contends that "[t]he term 'control signal' should be construed in accordance with its plain and ordinary meaning as a 'signal configured to control a circuit component.'" Pet. Reply 6; *see also* Pet. 28 (Petitioner contending that, for all claim terms, the "plain meaning should apply.").

Patent Owner contends that a person of ordinary skill in the art "would have understood that the plain and ordinary meaning of the term 'control signal' is a 'logic signal with two distinct states.'" PO Resp. 7 (citing Ex. 2005 ¶ 40); *see also* PO Sur-reply 1 ("The specification and claims describe the control signal as being output by a logic circuit, *e.g.*, a flip flop that outputs only two states, that is used to control other circuits." (referring to the "flip-flop" recited in independent claim 18)). Patent Owner argues that "Petitioner's usage of the term improperly interprets it to mean two signals that have multiple contradictory logic states at the same time." PO Resp. 7 (citing Ex. 2005 ¶ 57).

In the Sur-reply, Patent Owner further discusses this "two distinct state" concept, arguing that:

> Petitioner's identified "control signal" [of Tateishi] does not have two distinct logic states, it has multiple. For example, when [PWM latch output] Q is "1" the input to transistor 82 is "0" and when Q is "0" the input to transistor 82 is "1" or "0" depending on other logic. (EX1016 at ¶ 34.) The proper construction of "control signal," describes a two-state signal and cannot be satisfied with a combination of signals that has at least three states.

PO Sur-reply 13 (coloring omitted).[7] Patent Owner refers to this non-two-state situation as "logical dissimilarity." *Id.* at 15 ("There is a logical

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[7] At the pertinent terminals of the circuits of both the '377 patent and Tateishi, the signal either is a logical high or low value—a 1 or 0—and, thus, all are "two-state" signals. *See, e.g.*, PO Resp. 12 (characterizing Dr. Holberg's testimony that "the patent speaks of it in terms logical values 0 and 1" as an agreement with Patent Owner's position that the Specification of the '377 patent describes "the control signal as a logic signal with two distinct states."); PO Sur-reply 11 (Patent Owner asserting that a two-state signal is a binary signal). It is not clear how Patent Owner's "two-state" argument addresses any dispute in this case.

dissimilarity between the two: when Q is '0' the input to transistor 82 can be either '1' or 0.'").

Patent Owner agrees, at least to some extent, with Petitioner's position that a "control signal" is a signal that controls a circuit component. *See* PO Sur-reply 12 (Patent Owner asserting: "Control is not the real dispute; implicit in Patent Owner's construction—and in context of the claims—is the concept of control. Patent Owner's construction describes 'two distinct states' and, in context of the claims, it provides control to other devices.").

Patent Owner does not contend that the generated and received control signal be the same logical value, 0 or 1, at both terminals, and does not contend that the claim excludes all logic gates or intervening components. *See, e.g.*, Tr. 29:16–18, 30:13–20 (Patent Owner's counsel: "[W]e're not saying just a simple inversion doesn't make the control signal a control signal, so long as there's a state match. . . . If it goes through an inverter, it's still defining the same state. If it's some sort of stepped up step down voltage, if it's filtered, it's still defining . . . the same state. . . . [S]o if it's one here and that's inverted, it's zero. It's still trying to define the same state."); *see also id.* at 25:7–26:16 (Patent Owner arguing that its proposed construction encompasses the circuit path of the device accused of infringing, which has a three-input NOR gate and an inverter); *id.* at 36:18–37:7 (Patent Owner's counsel asserting that the claims do not require a direct connection between the two pertinent terminals).

At oral argument, Patent Owner indicated that it contends that the receiver of the "control signal" must be controlled exclusively by the component that generates the "control signal." *See* Tr. 38:2–10; *see also id.* at 38:15 (Patent Owner's counsel, in response to the question of where that

"exclusively" limitation is in the claim, asserting that, "[i]f there's a logical mismatch, it isn't the exclusive controller."); *id.* at 30:22–31:2 (arguing that the signal value at the receiving terminal cannot be "[c]ontrolled by anything else that adds additional states that creates a mismatch between [the signal at the receiver terminal and the signal at the generating device's terminal]").

To determine the proper construction of "control signal," we first turn to the claim language itself. Claim 1, for example, recites in limitation 1B2, "an input voltage sensing circuit . . . wherein . . . the second input terminal is configured to receive *a control signal* provided by the pseudo constant on time control circuit." Ex. 1001, 9:40–46 (emphasis added). The limitation further recites that, "based on the switching signal and *the control signal*, the input voltage sensing circuit generates [an output signal]." *Id.* at 9:47–50 (emphasis added). Limitation 1D recites that "the logic control circuit generates the *control signal*." *Id.* at 10:8–9 (emphasis added). In independent claim 18, the component that generates the "control signal" is called the "flip-flop." *Id.* at 14:19–20.

Petitioner notes that above-quoted language indicates that the input voltage sensing circuit generates a signal "based on the switching signal and the control signal," and that another limitation recites, "based on the input voltage and the control signal, the power stage generates the switching signal." Pet. Reply 8 (quoting Ex. 1001, 9:47–50, 10:11–13). Petitioner asserts that the parties' witnesses agree that "the control signal is configured to control the 'input voltage sensing circuit' and 'power stage' because their respective outputs are 'based on" the control signal.'" *Id.* (citing Ex. 1016 ¶ 8 (Dr. Holberg testifying that, "[i]n these limitations, the control signal is configured to control the 'input voltage sensing circuit' and 'power stage'

because their respective outputs are 'based on' the control signal.")) (emphasis added); Ex. 1017, 119:14–16 (Mr. McAlexander agreeing that "this claimed control signal controls the power stage to generate the switching signal.")). Patent Owner similarly asserts that the recited "control signal" is a signal that controls another element. *See* PO Sur-reply 12 (Patent Owner asserting: "Control is not the real dispute; implicit in Patent Owner's construction—and in context of the claims—is the concept of control. Patent Owner's construction describes 'two distinct states' and, in context of the claims, it provides control to other devices.").

Patent Owner does not persuasively argue that any aspect of the claim language supports Patent Owner's focus on the state or composition of a logic signal or that supports a narrow reading of the claim as requiring exclusive control by one component (e.g., the logic control circuit of limitation 1D or the flip-flop of limitation 18E). *See, e.g.*, PO Resp. 7–13 (claim construction section of the brief); *id.* at 29–34 (Patent Owner impliedly arguing, without an adequate explanation, that the "based on" language supports its claim construction position); PO Sur-reply 11–13.

We agree with Petitioner that the claim language is consistent with the understanding that the plain and ordinary meaning of "control signal" is a signal configured to control a circuit component.

We next turn to the Specification. As an initial matter, we note that figures of the '377 patent depict the subject circuitry path as not containing any logic gates, for example. *See* PO Resp. 11 (reproducing several figures with the subject path annotated in blue). However, Patent Owner does not contend that the claims are limited to the embodiments in the Specification. *Cf.* Tr. 25:7–26:23 (Patent Owner's counsel arguing that the claim covers

circuits containing logic gates in certain circumstances); *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004) ("[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited.").

Patent Owner argues that the Specification shows that the recited "control signal" generated by the logic control circuit/flip-flop is a logic signal with two distinct states, a logical value of 0 or 1. *See, e.g.*, PO Resp. 10–12. This does not appear to be in dispute and does not help in the analysis of the proper claim construction needed to address the disputed issues.

Petitioner relies on the Specification's description of Figure 4, and specifically the description of the input voltage sensing circuit, which is the receiver of the subject "control signal." *See* Pet. Reply 8–9 (citing Ex. 1001, 5:21–23, Fig. 4; Ex. 1016 ¶¶ 9–11). Petitioner notes that "the specification teaches that '[t]he switch K is coupled to the capacitor C_{TON} in parallel and ***controlled by the control signal Q***' [the subject control signal generated by the logic control circuit/flip-flop]." *Id.* (quoting Ex. 1001, 5:21–23) (alteration in original); *see also id.* at 9 ("As another example, in its description of Figure 11 . . . , the specification teaches that '***[t]he control signal Q controls the high-side switch Q_1***, and the complementary signal Q' of the control signal Q controls the low-side switch Q_2.'" (quoting Ex. 1001, 8:32–34) (alteration in original). We agree with Petitioner that "the specification teaches that the control signal described in the '377 Patent is

configured to 'control' various components of the disclosed circuits," and that the Specification is consistent with Petitioner's proposed construction.

The parties do not direct our attention to any pertinent evidence in the prosecution history. *See, e.g.*, Pet. 26–27 (Petitioner asserting that the applicant, in response to an anticipation rejection, *inter alia*, "amended the claims to incorporate allowable subject matter from claim 2 into claim 1," and subsequently a notice of allowance was issued.).

Lastly, we turn to the extrinsic evidence upon which the parties rely. Petitioner (Pet. Reply 10) relies on a technical dictionary, which defines the term "control signal" as "[a] signal utilized to control a device or process." Ex. 1018 (Wiley Electrical and Electronics Engineering Dictionary), 3. Petitioner argues that, "[l]ike the claim language and specification, this definition also recites a control function and supports Petitioner's construction." Pet. Reply 10. We find that this dictionary definition is consistent with the intrinsic evidence and, as an unbiased pre-litigation source, persuasively indicates that the plain and ordinary meaning of "control signal" is, as Petitioner asserts, a "signal configured to control a circuit component."

Dr. Holberg testifies that the plain and ordinary meaning of "control signal" is a "signal configured to control a circuit component." Ex. 1016 ¶ 13 ("Throughout my years of experience, I and other persons of ordinary skill in the art have used and encountered the term 'control signal' regularly and I and other persons of ordinary skill in the art understand the plain and ordinary meaning of 'control signal' to be a "signal configured to control a circuit component.'"). Mr. McAlexander agrees that, "in the context of the

'377 patent, . . . a control signal is a signal that controls other circuit components." Ex. 1017, 121:1–4; *see* Pet. Reply 6 (citing same).

Dr. Holberg further opines that:

> Under Petitioner's proposed construction, the claimed control signal may be impacted by other functionality of the circuit in performing its primary function of controlling the high-side and low-side switches. The control signal may pass through intervening logic gates and/or may change logical values along its path (i.e., from 0 to 1, from 1 to 0). But if the control function is present, and meets the other requirements recited in the claims, then that signal constitutes a "control signal."

Ex. 1016 ¶ 16 (cited at Pet. Reply 13).

Patent Owner argues Dr. Holbert's testimony shows that that Petitioner's application of its proposed construction renders "control signal" superfluous. PO Sur-reply 15–16; *see also id.* at 12–13. Patent Owner argues:

> Dr. Holberg testified that any signal—or combination of signals—within Figure 3 [of Tateishi] can be *the same control signal* (except for voltage power and ground). For instance, he testified that the positive input to comparator 106, the feedback signal 44, signal 120, Vout 24, and the input to transistor 12 are all *the same control signal* . . . . (*Id.*) In effect, under Petitioner's application, PWM latch generates any signal in the circuit to meet the claim phrase, because any signal is the "control signal." Under Petitioner's application, any signal in a device can satisfy claim 18's "the flip flop generates the control signal" and "an on-time generator configured to receive . . . a control signal," rendering this phrase meaningless.

Id. at 15–16 (citing Ex. 2007, 10:1–6, 11:21–13:8, 13:20–25, 16:4–17:9) (emphasis added; last alteration in original); *see also id.* at 10. This is an incorrect characterization, and the cited testimony supports Petitioner's position. Dr. Holberg was not, as Patent Owner asserts, testifying that each listed item is the *same* control signal, and was not testifying that all of those

items are the specifically recited "control signal," e.g., that generated by the logic control circuit of limitation 1E or the flip-flop of limitation 18E. *See* Ex. 2007, 10:1–6, 11:21–13:8, 13:20–25, 16:4–17:9. Rather, Dr. Holberg testified that those items would each be considered a "control signal" under the plain and ordinary meaning because "it affects any of the downstream circuitry." *Id.* at 9:13–10:6. This testimony is consistent with Petitioner's proposed claim construction.

Mr. McAlexander, in the claim construction section of his Supplement Declaration filed in support of Patent Owner's Response, states his agreement with Patent Owner's position that term "control signal" is a "logic signal with two distinct states." Ex. 2005 ¶ 40. Mr. McAlexander then explains that two states are a logic low (0) and a logic high (1), and opines that the control signal would be a digital signal not be an analog signal. *See id.* ¶¶ 41–57; *id.* ¶ 55 (Mr. McAlexander testifying that "Dr. Holberg also confirmed that the control signal would not be an analog signal according to the specification."). For example, Mr. McAlexander testifies:

> A POSITA would understand that such a "control signal" would be a digital signal with two states in order to control this claimed functionality. For example, the control signal could turn the high and low side switches off and on, meaning that it should have a logical high or low state (e.g., a '1' or '0') to control the turning on and off of the switches in the power stage.

Id. ¶ 47; *see also, e.g.*, *id.* ¶ 53 ("Figure 12 [of the '377 patent] is a timing diagram for Figure 11 and states that the control signal Q can have a value of 0 or 1 (*e.g.*, discrete logic states)."). We do not view this as inconsistent with Petitioner's proposed construction or Dr. Holberg's testimony about the understanding of a person of ordinary skill regarding the meaning of "control signal."

After considering the parties' arguments and evidence, we determine that Patent Owner has not offered persuasive evidence that a person of ordinary skill in the art reading the claims in light of the Specification would understand the plain and ordinary meaning of "control signal" to be as narrow as Patent Owner proposes. We do not construe the claims such that the "control signal" must be the exclusively controlling factor of a component, as Patent Owner urges. Petitioner's position, on the other hand, is consistent with the evidence of record.

We construe "control signal" as having its plain and ordinary meaning, namely a signal configured to control a circuit component.

D. The Asserted Anticipation of Claims 1–4, 9–14, 17, and 18 by Tateishi

Petitioner asserts that claims 1–4, 9–14, 17, and 18 of the '377 patent are anticipated by Tateishi under the pre-AIA version of 35 U.S.C. § 102(b). *See* Pet. 23–24; *id.* at 33–47 (addressing claim 1). Patent Owner argues that the Petition "fails to demonstrate the claimed 'control signal' as described in the claims." PO Resp. 13; *see also id.* at 18–34. Patent Owner also argues that Petitioner's contentions regarding the "switching signal" of limitation 1B2 involve the combination of several embodiments, and argues that this is inconsistent with an anticipation analysis. *See* PO Resp. 34–41.

1. Tateishi (Ex. 1007)

Tateishi is a United States Patent Application Publication titled, "DC to DC Converter with Pseudo Constant Switching Frequency." Ex. 1007, codes (12), (19), (54). Tateishi discloses that "[t]he switching frequency is controlled by a switching controller in the DC to DC converters based upon feedback from the switching node, without a direct connection to the output node." *Id.* ¶ 17. "The use of feedback from the switching node to establish

the pseudo constant switching frequency avoids the need to provide a pin on the integrated circuit for direct feedback from the output node at the far end of the external filtering components." *Id.*

Figure 3 of Tateishi is reproduced below.

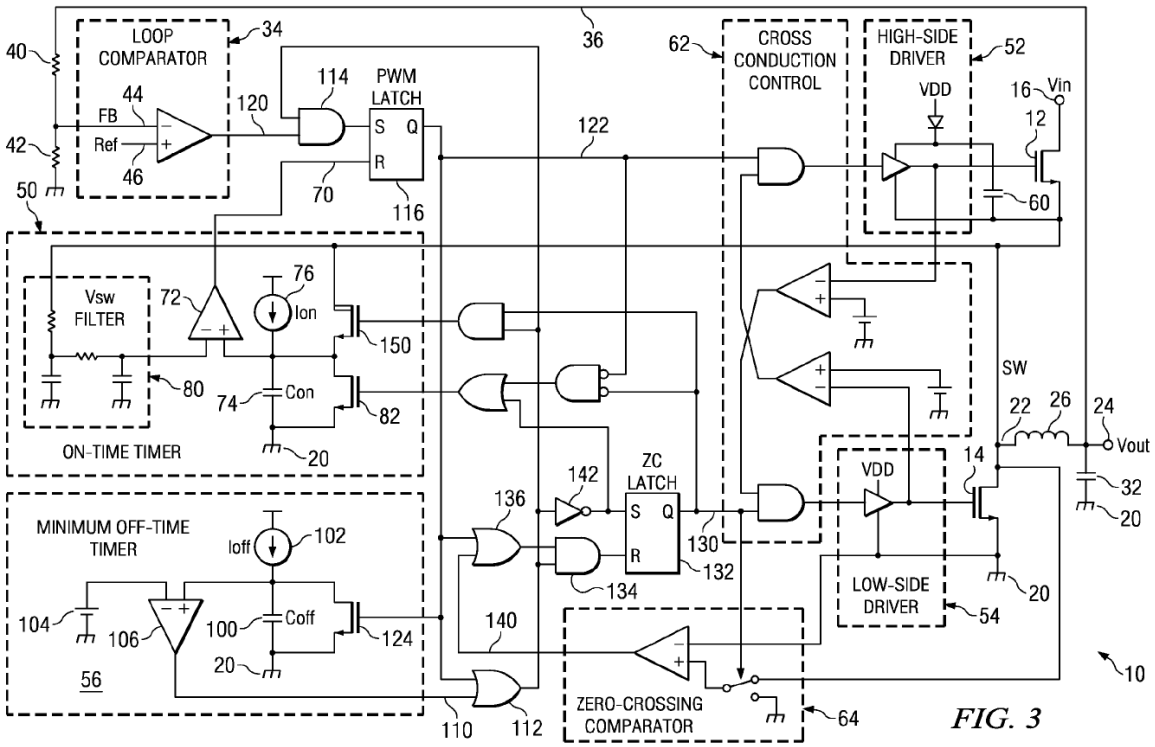

FIG. 3

Figure 3 "depicts an example of a DC to DC buck converter with a pseudo constant switching frequency that takes into consideration off-time low side switch voltage." *Id.* ¶ 12.

"A high side switch 12 and a low side switch 14 are connected in series between an input Vin 16 and ground 20, with a switching node 22 between the high side switch 12 and the low side switch 14." *Id.* ¶ 18. "An output Vout 24 is connected to the switching node 22 through an output filter." *Id.*

> The DC to DC buck converter 10 of FIG. 1[8] establishes a pseudo constant switching frequency for the switching node 22 based on feedback from the switching node 22 rather than from the output Vout 24. During an on-time, the high side switch 12 is turned on and the low side switch 14 is turned off, allowing current to flow from the input Vin 16 to the output Vout 24 through the inductor 26. During an off time, the low side switch 14 is turned on and the high side switch 12 is turned off. . . . A loop comparator 34 in the DC to DC buck converter 10 begins each on-time based on a feedback signal 36 from the output Vout 24. . . . When the divided feedback voltage 44 falls below a reference voltage 46, the loop comparator 34 starts the on-time. An on-time timer 50 ends the on-time after a period calculated to maintain a substantially constant switching frequency, or pseudo constant frequency.

Id. ¶ 19.

> When the off-state is initiated by the on-time timer 50, the discharging transistor 82 is turned on and the capacitor Con 74 is discharged to ground 20. After the minimum off-time, which is generated by the minimum off-time timer 56, the discharging transistor 82 is turned off and a precharging transistor 150 is turned on to precharge the capacitor Con 74. . . . The comparator 72 in the on-time timer 50 generates a pulse on the on-time termination signal 70 and terminates the on-time when the voltage on the capacitor Con 74 reaches (Vout+Vdcr).

Id. ¶ 59.

Tateishi, in the context of the Figure 1 embodiment, discusses the role of the SR latch 116 in the on time and off time operations.

> [A]fter the minimum off-time timer 56 has measured the minimum off time and when the loop comparator 34 detects that the voltage at the output Vout 24 has fallen below a reference

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[8] Much of Tateishi's descriptions are of the Figure 1 embodiment, but the Figure 3 embodiment uses many of the same element numbers and "[t]he DC to DC buck converter 10 of FIG. 3 operates in much the same manner as that of FIG.1." Ex. 1007 ¶ 58.

> voltage 46, the Set input of the SR latch 116 is asserted to begin an on-time. The output 122 of the SR latch 116 is thus asserted, turning on the high side switch 12 and turning off the low side switch 14. The output 122 of the SR latch 116 also drives a discharging transistor 124 in the minimum off-time timer 56, discharging the capacitor Coff 100 to ground 20 when the on-time begins. The output 122 also drives the discharging transistor 82 in the on-time timer 50 through an inverter 126 [of the Figure 1 embodiment], so that during an off-time, the capacitor Con 74 is discharged to ground 20 and during an on-time, the discharging transistor 82 is turned off allowing the capacitor Con 74 to be charged by the current source 76.

Id. ¶ 51.

Tateishi's disclosures are discussed further below in the context of the parties' contentions.

2. The Asserted Anticipation of Independent Claim 1 by Tateishi

a. [1Pre] A step-down regulator, comprising:

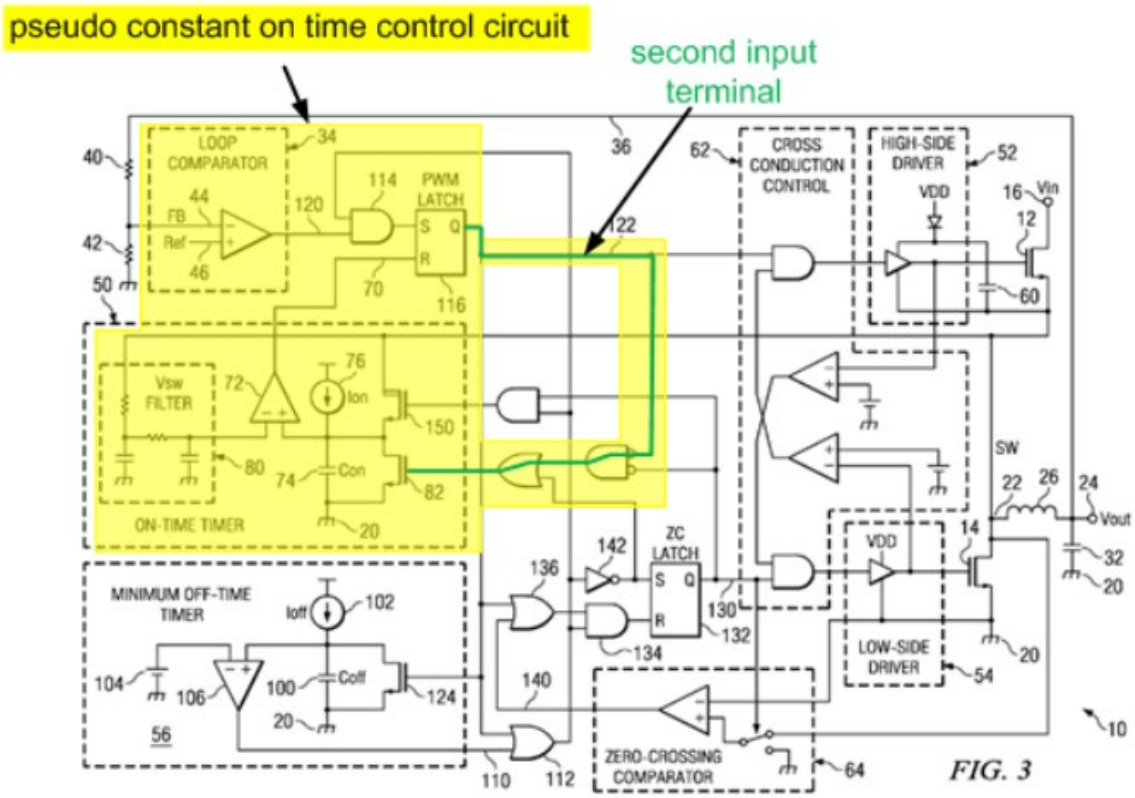
Petitioner contends that, to the extent the preamble is limiting, Tateishi discloses a step-down regulator, namely, "a DC-DC buck converter that receives an input voltage and regulates it down to a lower output voltage." Pet. 33 (citing Ex. 1007 ¶¶ 5, 18, Figs. 1, 3; Ex. 1003 ¶ 81). Patent Owner does not raise any arguments regarding this contention.

Without determining whether the preamble is limiting, we have reviewed Petitioner's arguments and the underlying evidence, and we find that Petitioner has shown by a preponderance of the evidence that Tateishi discloses the subject matter of the preamble.

b. [1A] a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:

The recited pseudo constant on time control circuit comprises multiple components, which are discussed further below. *See* Ex. 1001, 9:37–10:9. Petitioner contends that "Tateishi discloses a loop comparator 34, an on-time

timer 50, and other circuitry that generates signals that control the on-time of the buck converter according to 'a pseudo on-time generation algorithm.'" Pet. 34 (citing Ex. 1007 ¶¶ 45–48; Ex. 1003 ¶¶ 83–88). Petitioner utilizes an annotated version of Tateishi's Figure 3, reproduced below, to visually depict its contentions as to the recited pseudo constant on time control circuit.



Id. at 35. Above is Petitioner's annotated version of Tateishi's Figure 3 with yellow shading over, *inter alia*, on-time timer 50, loop comparator 34, and SR latch 116, and a green line from SR latch 116 to discharging transistor 82. *See* Ex. 1007 ¶ 51.[9]

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[9] The arrow for the green label "second input terminal" is located other than intended by Petitioner. *See* Pet. 37 (the arrow for the same label pointing to a point near discharging transistor 82); Ex. 1003 ¶ 87 (Dr. Holberg's

Patent Owner does not raise any arguments regarding these contentions other than as to whether the green line corresponds to the "control signal" of limitations 1B2 and 1D, which are discussed below. *See, e.g.*, PO Resp. 22.

We have reviewed Petitioner's arguments and the underlying evidence, and we find that Petitioner has shown by a preponderance of the evidence that Tateishi discloses the limitation 1A.

c. [1B1] an on-time generator comprising:

Petitioner contends that Tateishi's on-time timer 50 is the recited "on-time generator." Pet. 35–36 (citing Ex. 1007 ¶¶ 21, 45, Fig. 3; Ex. 1003 ¶ 83). Petitioner's annotated version of Tateishi's Figure 3, reflecting this contention, is reproduced below.

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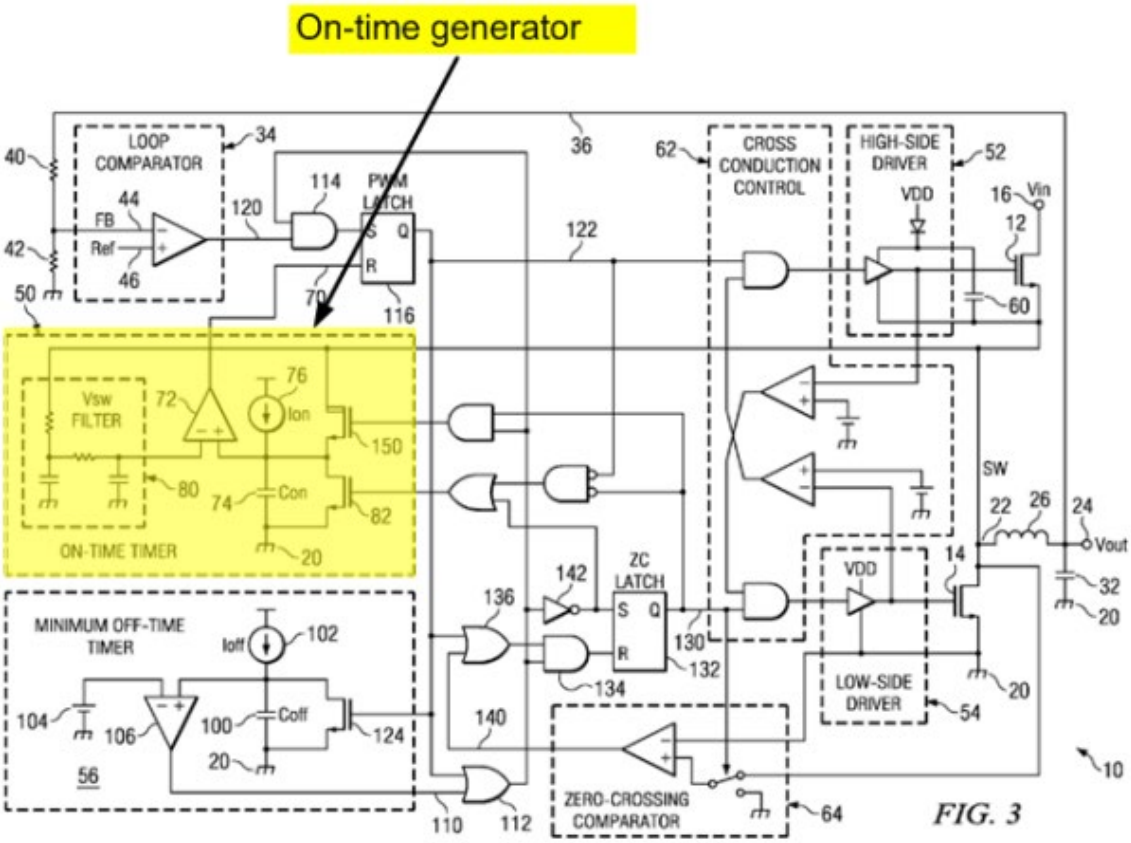
declaration with an annotated figure similar to that above with the arrow pointing to the input of discharging transistor 82).



Id. at 36. Above is Tateishi's Figure 3 with on-time timer 50 shaded yellow.

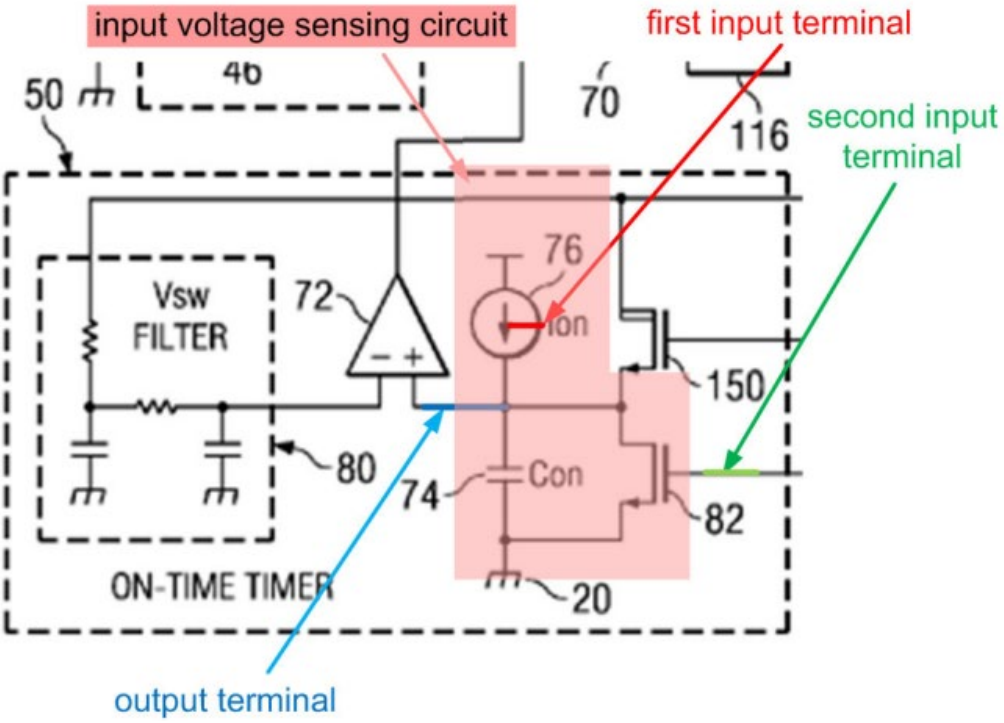
Patent Owner does not raise any arguments regarding this contention. However, Patent Owner, as discussed below, does present arguments regarding the input voltage sensing circuit recited in limitation 1B2 and which is part of the on-time timer.

We have reviewed Petitioner's arguments and the underlying evidence, and we find that Petitioner has shown by a preponderance of the evidence that Tateishi discloses an on-time generator.

d. [1B2] an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

Limitation 1B2 recites an input voltage sensing circuit having two input terminals—a first input terminal configured to receive a switching signal and a second input terminal configured to receive a control signal provided by the pseudo constant on time control circuit. Patent Owner disputes Petitioner's contentions as to both of those input terminals. *See, e.g.*, PO Resp. 13, 34.

Petitioner contends that Tateishi discloses the recited input voltage sensing circuit having the recited two input terminals and the output terminal. Pet. 36–39 (citing, *inter alia*, Ex. 1003 ¶¶ 84–87). According to Petitioner, "Tateishi discloses the on-time timer 50 comprising a capacitor Con 74, a discharging transistor 82 driven by the control signal 122, and a current source 76 that provides a charging current proportional to the input voltage of the power stage at input Vin 16." *Id.* at 37 (citing Ex. 1007 ¶¶ 32, 52, Fig. 3; Ex. 1003 ¶ 85). Petitioner's annotated version of a portion of Tateishi's Figure 3 is reproduced below.



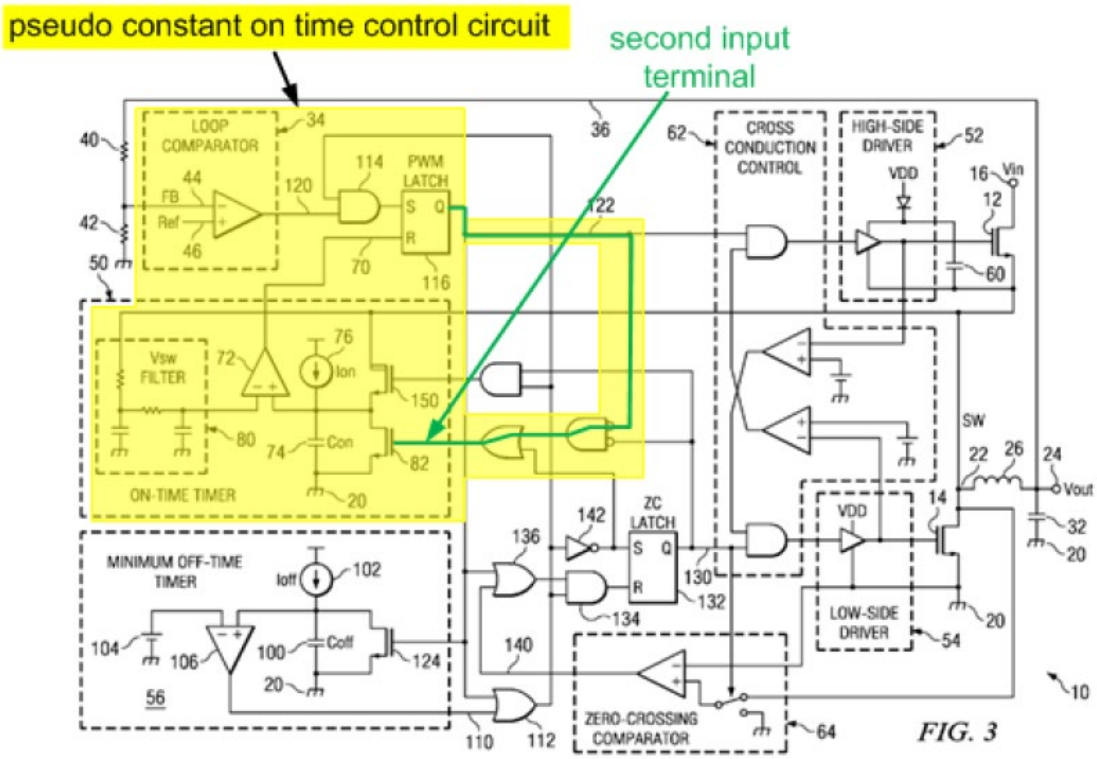
Pet. 37. Above is Petitioner's annotated version of the portion of Tateishi's Figure 3[10] depicting on-time timer 50, with capacitor Con 74, discharging transistor 82, and current source 76 shaded red and identified as the input voltage sensing circuit. *See* Ex. 1007 ¶ 52. Petitioner identifies the recited "first input terminal" as being in current source 76 (red), "second input terminal" at discharging transistor 82 (green), and "output terminal" as the connection to comparator 72 (blue). Petitioner further contends that "Tateishi discloses several example embodiments of current source 76, including those illustrated in Figs. 2 and 4," and that the embodiments of

[10] As mentioned above, during the trial there was some question as to whether the Petition includes a theory that Tateishi's Figure 1 embodiment is an anticipatory disclosure. *See, e.g.*, Paper 29 (Order on Patent Owner's Motion to Strike summarizing the dispute). At oral argument, Petitioner confirmed that it is not relying on the embodiment of Figure 1 as an anticipatory disclosure. *See* Tr. 17:13–19:8.

Figures 2 and 4 receive voltage from switching node SW 22 and "output a current that is proportional to the voltage of the switching node 22 (which, during the on-time, is connected to the input voltage, Vin)." Pet. 38 (citing Ex. 1007 ¶¶ 50, 62, Figs. 2, 4; Ex. 1003 ¶¶ 85–86).

As mentioned, this limitation 1B2 recites that "the second input terminal [of the input voltage sensing circuit] is configured to receive *a control signal*" and limitation 1D recites that "the logic control circuit generates *the control signal*." Ex. 1001, 9:44–45, 10:8–9 (emphasis added). In this regard, Petitioner contends that "Tateishi discloses . . . a discharging transistor 82 driven [at the second input terminal] by the control signal 122." Pet. 37 (citing Ex. 1007 ¶¶ 32, 52, Fig. 3; Ex. 1003 ¶ 85). Petitioner also contends that PWM SR latch 116 (mapped to the "logic control circuit" of limitation 1D) produces the control signal of this limitation 1B2. *Id.* at 45 (citing Ex. 1003 ¶ 96).

In support, Dr. Holberg testifies that "[t]he second input terminal [the input voltage sensing circuit] receives its input from PWM latch 116," and that "[t]he on-time timer 50 comprises . . . . a discharging transistor 82 driven by the control signal 122 (produced by SR latch 116)." Ex. 1003 ¶¶ 85, 87; *see also id.* ¶ 75 ("The on-time circuit 50 receives the control signal 122 . . ." (citing Ex. 1007 ¶¶ 19, 33)). Dr. Holberg provides an annotated version of Figure 3, reproduced below. *Id.* ¶ 87.



Id. Above is Dr. Holberg's annotated version of Figure 3 with, *inter alia*, loop comparator 34, PWM SR latch 116, and on-time timer 50 shaded yellow. The green line in the annotated figure above depicts Dr. Holberg's opinion as to how output 122 of the SR latch 116 and the input to discharging transistor 82 is the "control signal" of limitations 1B2 and 1D. *See id.* ¶¶ 87–88, 96.

Control Signal

Patent Owner argues that Petitioner, for limitation 1B2 and 1D, improperly is identifying separate signals as the recited "control signal." *See* PO Resp. 21 (citing Ex. 2005 ¶¶ 66–68); *see also id.* at 18 ("Petitioner's analysis of the 'control signal' in the Petition across claim phrases fails to track the control signal's antecedent basis."). Specifically, Patent Owner argues that "[t]he signals identified by Petitioner for **1[B2]** and **1[D]** are two entirely different signals" because "these two signals are separated by two

logic gates, an OR gate and an inverting AND gate." *Id.* at 22 (citing Ex. 2005 ¶¶ 69–76). Patent Owner further argues that "a POSITA would understand that the separating logic makes them different logical signals." *Id.* (citing Ex. 2005 ¶¶ 70–72). Patent Owner also argues that "those [Or and AND] gates have—as their inputs—other signals from other logic that affects their output," and "[t]his other logic further demonstrates that Petitioner's two identified signals are not the same 'control signal.'" *Id.* at 23 (citing Ex. 2005 ¶¶ 73–76).

Patent Owner additionally argues that, even if "two distinctly different logic signals" can be the same "control signal," Petitioner's analysis still fails. *Id.* at 26. Patent Owner argues that:

> Petitioner's analysis, in order to hold, would require that the signals identified be logically consistent, i.e., its 1[D] signal would need to be logically consistent in some manner with the signal identified in 1[B2]. Petitioner would need—but failed—to demonstrate that its identified signal is a logic signal with two distinct states.
>
> The signals identified by Petitioner have logic states that are inconsistent; the identified control signal is, *e.g.*, '0' while another part of it can be either '1' or '0' depending on other logic of the circuit. (EX2005, ¶ 78.) There is a breakdown in any sense of cohesive control the alleged control signal would have and Petitioner failed to identify a logic signal with two distinct states.

Id.

Patent Owner's argument, as we understand it, is that the signal generated at PWM SR Latch 116 is not the same "control signal" received by transistor 82 because there are scenarios in which the signal state at transistor 82 is affected, and therefore controlled, by components other than the PWM SR Latch. *See* PO Resp. 26–29; *see id.* at 29 ("In other words, the value of Coff and the load provide logical signals that affect the control of

switch 82; it is not controlled via the . . . signal [from the PWM Latch].”). Specifically, Patent Owner argues that, at certain times, the zero-crossing comparator (including the ZR latch) or the minimum off-time timer control transistor 82. *See id.* at 28–29.

Similarly, Patent Owner notes that two limitations each recite that a particular signal is generated “based on [another particular signal] and the control signal,” and argues that Petitioner has failed to show both limitations are satisfied because Petitioner relies on two different “control signals.” *See id.* at 29–34 (referring to limitations 1B2 and 1E); *see also id.* at 18–19; *see also* Ex. 1001, 10:11–13 (limitation 1E reciting “based on the input voltage and the control signal, the power stage generates the switching signal.”). For this argument, Patent Owner asserts that the signal received at transistor 82 (the subject of limitation 1B2 and which Patent Owner colors green in its briefs) is not the same as the signal received at the power stage (the subject of limitation 1E and which Patent Owner colors orange). *See* PO Resp. 32–33 (“[T]he orange signal itself is an input to the identified ‘power stage’ (yellow) which generates a ‘switching signal’ (purple box). . . . The green signal is not an input to the power stage, and the power stage does not generate the “switching signal” based on the green signal along with the ‘input voltage.’”).

Patent Owner’s arguments are based on a claim construction with which we do not agree for the reasons discussed above in the claim construction section.

Dr. Holberg persuasively testifies that Tateishi’s signal 122—the output Q of the PWM Latch (mapped to the output signal of the logic control circuit/flip-flop)—controls transistor 82 (the input of which is mapped to the

recited received signal) when the zero-crossing comparator is not triggered[11] and when the output 110 of the minimum off-time timer 56 is a logical 0. Ex. 1016 ¶¶ 24–31. Dr. Holberg further testifies that, accordingly, Tateishi discloses the "control signal" recited in both limitations 1B2 and 1D, namely the signal Q generated by the logic control circuit and the signal input to transistor 82. *See id.* ¶¶ 30–31.

Patent Owner asserts that Dr. Holberg's presumptions are incorrect but Patent Owner is referring to a different scenario, where minimum off-time timer signal 110 is a logical 1, rather than a 0 as in Dr. Holberg's declaration. *See* PO Sur-reply 5 (impliedly arguing, without a pinpoint citation, that Dr. Holberg "confirmed" the incorrect presumptions in his deposition). Patent Owner's argument is, in effect, that there are times during operation of Tateishi's device when the minimum off-time timer also controls transistor 82. *See id.* at 5–8; *see also* Tr. 37:8–15 (Patent Owner asserting that, in practice, the zero-crossing latch and the minimum off-time timer override the output from the PWM latch/flip-flop). This does not appear to be in dispute, and does not detract from the PWM Latch signal being a "control signal" under our claim construction, as set forth above.

We determine that Petitioner has demonstrated by a preponderance of the evidence that Tateishi discloses the "control signal" recited in limitations 1B2 and 1D of independent claim 1.

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[11] We disagree with Patent Owner's assertion that Dr. Holberg was testifying about a hypothetical situation where the zero-crossing comparator is "eliminate[d]" or "disabled." *See* PO Sur-reply 9.

Switching Signal

This limitation 1B2 recites "an input voltage sensing circuit . . . wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator." Ex. 1001, 9:40–44.

As mentioned above, Petitioner contends that the recited "first input terminal" is in Tateishi's current source 76. *See* Pet. 37. Tateishi's Figure 3 does not show the input to current source 76, and thus does not depict the terminal as receiving the recited switching signal. Ex. 1007, Fig. 3. In that regard, Petitioner further contends that Tateishi discloses, in Figures 2 and 4, example embodiments of current source 76 and contends that those examples do disclose the switching signal as the input. *See* Pet. 38–39 (citing, *inter alia*, Ex. 1007 ¶¶ 50, 62, Figs. 2, 4; Ex. 1003 ¶ 85).

Patent Owner argues that Petitioner "modifies and combines several embodiments within Tateishi in a way that should be presented under an obviousness analysis," rather than in an anticipation ground. PO Resp. 19; *see also id.* at 34–41. We do not agree with Patent Owner's argument.

Tateishi states that "[o]ne example of a current source 76 that produces an output 84 proportional to (Vin-Von1) is illustrated in FIG. 2." Ex. 1007 ¶ 50. Tateishi also discloses an embodiment of current source 76 in Figure 4. *Id.* ¶ 62, Fig. 4.

Petitioner persuasively argues that "Figure 3 illustrates current source 76 using the generic symbol for an 'ideal current source,' while Figures 2 and 4 each show the detailed circuitry inside of current source 76," and that, "[n]otwithstanding these differing levels of detail, current source 76 refers to the same element in all three figures, as evidenced by the fact that the inventor used the same reference numeral in all three figures." Pet. Reply 21 (citing Ex. 1016 ¶ 40; *Ex parte Grabelsky*, Appeal No. 2012-

004212, 2015 WL 252852, at *2–3 (PTAB. Jan. 16, 2015) ("U.S. patent application disclosures apply identical reference characters to only an invention's 'same' features." (quoting 37 C.F.R. § 1.84(p)(4))). We also find persuasive and credible Dr. Holberg's opinion that "POSITAs would have understood that current source 76 refers to the same element in each of Tateishi's Figures 2, 3, and 4." Ex. 1016 ¶ 40; *see, e.g.*, *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1341 (Fed. Cir. 2016) ("[A] reference can anticipate a claim even if it does not expressly spell out all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would at once envisage the claimed arrangement or combination." (alterations and internal quotations omitted)).

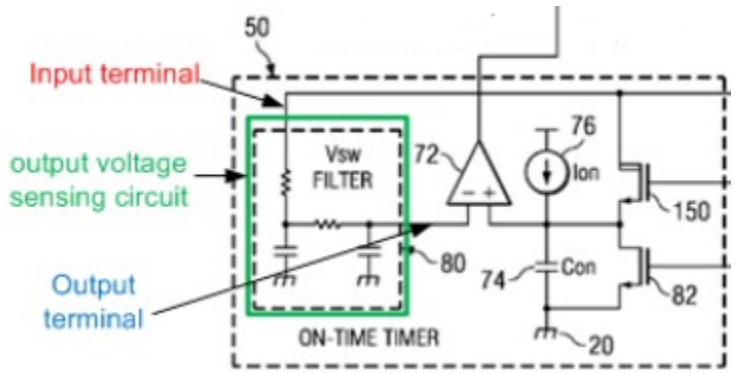
We determine that Petitioner, in relying on Figures 2, 3, and 4, has articulated a proper anticipation ground, and did not, as Patent Owner urges, resort to an obviousness ground.

We determine that Petitioner has demonstrated by a preponderance of the evidence that Tateishi discloses this limitation 1B2.

> *e. [1B3] an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and*

Petitioner contends that "Tateishi discloses an output voltage sensing circuit having an input terminal configured to receive the switching signal (SW) and generating an output voltage sensing signal based on the switching signal (low-pass filtered/averaged switching-node voltage) at an output terminal of low-pass filter 80." Pet. 40 (citing Ex. 1003 ¶¶ 89–91); *see also id.* at 39 (citing Ex. 1007 ¶¶ 49, 52, Figs. 1, 3; Ex. 1003 ¶ 89). Petitioner

utilizes an annotated version of a portion of Tateishi's Figure 3, reproduced below, to visually depict its contentions as to the recited output voltage sensing circuit.



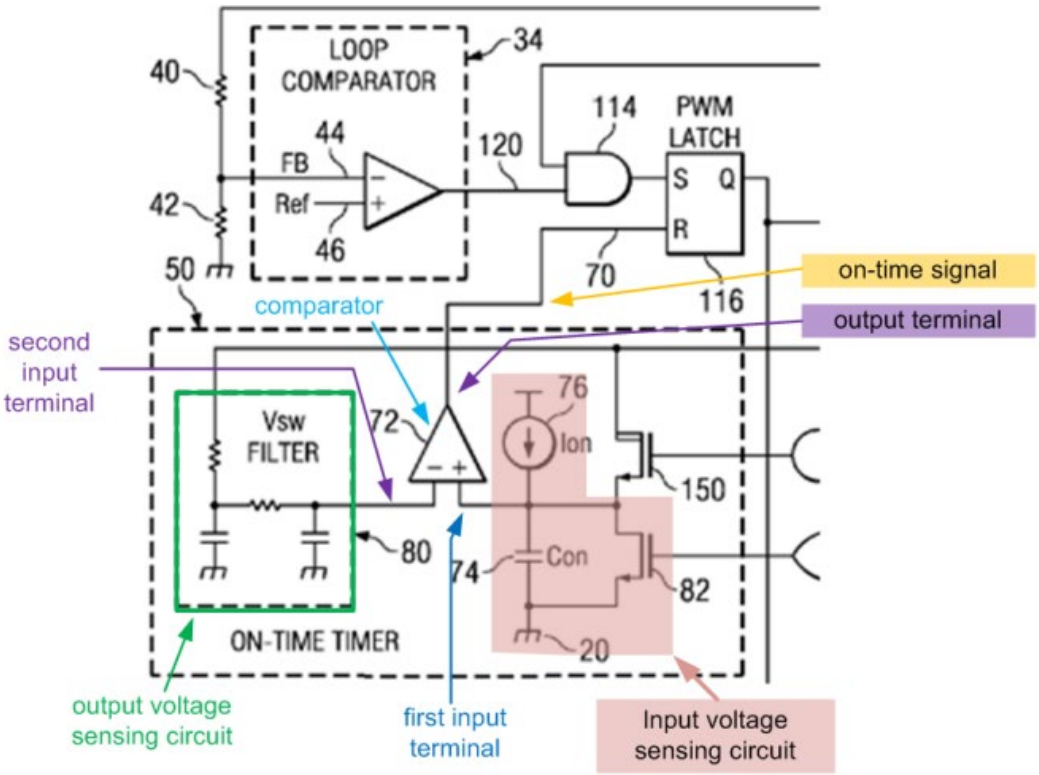
Pet. 40. Above is a cropped and cleaned up portion of Petitioner's annotated version of Tateishi's Figure 3, that depicts on-time timer 50 with Petitioner's annotations identifying Vsw (switching node voltage) filter 80 as the recited "output voltage sensing circuit" (green) with an input terminal (red) and an output terminal (blue). *See* Ex. 1007 ¶¶ 33, 44.

Patent Owner does not raise any arguments regarding these contentions.

We have reviewed Petitioner's arguments and the underlying evidence, and we find that Petitioner has shown by a preponderance of the evidence that Tateishi discloses this limitation 1B3.

f. [1B4] a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;

Petitioner contends that Tateishi discloses this limitation, and provides the annotated portion of Figure 3 reproduced below to illustrate its contentions. Pet. 41–42 (citing Ex. 1003 ¶¶ 92–93; Ex. 1007 ¶¶ 33, 49).



Id. at 42. Above is an annotated portion of Tateishi's Figure 3 reflecting Petitioner's contention that "Tateishi's comparator 72 [light blue] receives the output voltage sensing signal from Vsw filter 50 [output sensing circuit (green) received at the comparator's second input terminal (purple)],

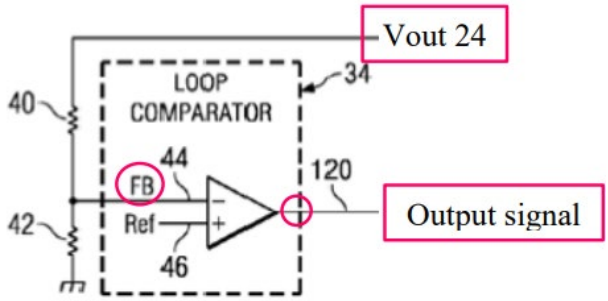
receives the input voltage sensing signal [at the comparator's second input terminal (purple)] from capacitor Con 74 [a portion of input voltage sensing circuit (pink)], and, based on those inputs, generates on-time termination signal 70 [yellow]," at the comparator's output terminal (purple).

Patent Owner does not raise any arguments regarding these contentions.

We have reviewed Petitioner's arguments and the underlying evidence, and we find that Petitioner has shown by a preponderance of the evidence that Tateishi discloses this limitation 1B4.

> *g. [1C] a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to generate an output signal in accordance with the feedback signal; and*

Petitioner contends that Tateishi's loop comparator 34 is the recited feedback control circuit, and provides the annotated portion of Figure 3 below. Pet. 42–43 (citing Ex. 1003 ¶ 94; Ex. 1007 ¶ 19, Figs. 1, 3).



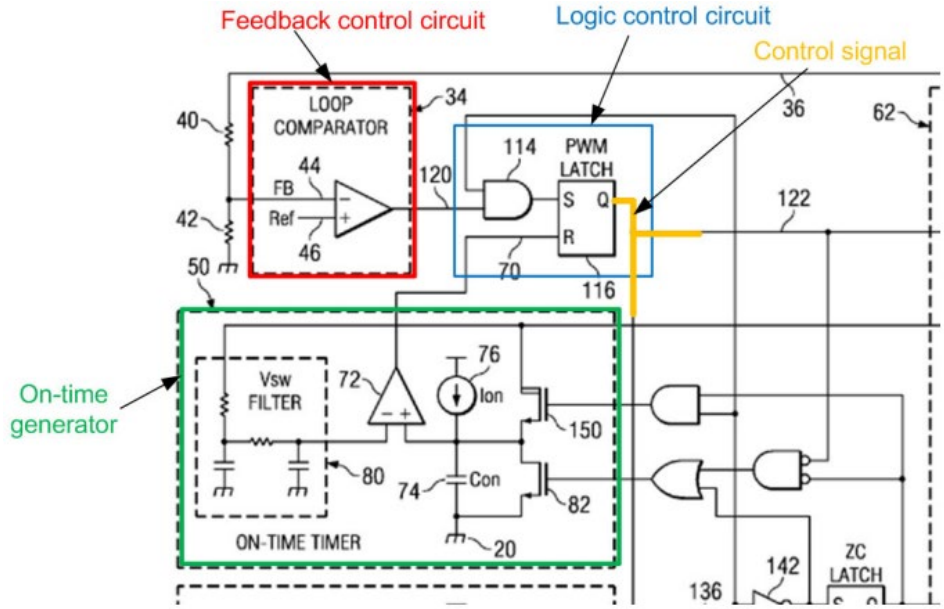
Id. at 43. Above is a portion of Figure 3 depicting loop comparator 34 with Petitoner's labels of an output signal (output signal 120) and Vout 24 as the feedback signal FB. *See* Ex. 1007 ¶ 51. Petitioner further contends that "[a] POSITA would understand that the output (FB) of the voltage divider is proportional to (i.e., representative of) the output voltage." Pet. 43 (citing Ex. 1003 ¶ 94).

Patent Owner does not raise any arguments regarding these contentions.

We have reviewed Petitioner's arguments and the underlying evidence, and we find that Petitioner has shown by a preponderance of the evidence that Tateishi discloses this limitations 1C.

> *h. [1D] a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal; and*

Petitioner contends that "Tateishi (in particular, Tateishi's PWM SR latch 116–possibly in combination with AND gate 114) discloses this limitation." Pet. 44 (citing Ex. 1007 ¶¶ 51, 52, Figs. 1, 3; Ex. 1003 ¶ 95). Petitioner provides an annotated portion of Tateishi's Figure 3, reproduced below.



Id. at 45. Above is Petitioner's annotated version of a portion of Tateishi's Figure 3 with PWM SR latch 116 and AND gate 114 identified as the logic control circuit (blue), loop comparator 34 identified as the feedback control

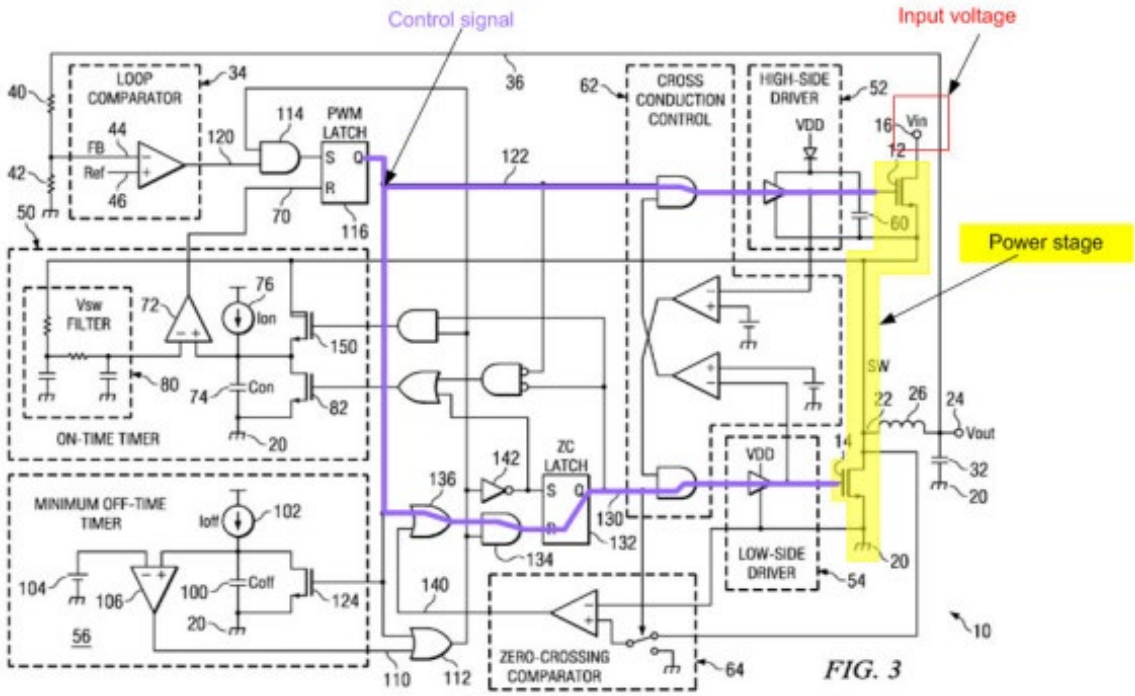
circuit (red), and on-time timer 50 identified as the on-time generator (green). Petitioner contends that "Tateishi's PWM SR latch 116 is coupled to the output 120 of the loop comparator 34 (through AND gate 114) to receive the output signal of limitation 1[C], and Tateishi's PWM SR latch 116 is coupled to the output of comparator 72 to receive the on-time signal of limitation 1[B4], and—based on these signals—Tateishi's PWM SR latch 116 produces the control signal 122 of limitation 1[B2]." *Id.* (citing Ex. 1003 ¶ 96) (brackets in original).

Patent Owner argues that the output 122 of PWM SR latch 116—mapped to the generated "control signal" of this limitation 1D—is not the same "control signal" of limitation 1B2. *See, e.g.*, PO Resp. 19–26. We do not agree with Patent Owner's arguments for the reasons discussed above in the context of claim construction and of the input voltage sensing circuit (limitation 1B2).

We determine that Petitioner has demonstrated by a preponderance of the evidence that Tateishi discloses limitation 1D, the logic control circuit.

i. [1E] a power stage configured to receive an input voltage and the control signal, wherein based on the input voltage and the control signal, the power stage generates the switching signal.

Petitioner contends that Tateishi discloses this limitation. Pet. 45–47. According to Petitioner, "[i]n particular, Tateishi discloses a cross-conduction circuit that receives the control signal 122 produced by PWM SR latch 116, high-side and low-side switch drivers (52, 54) and high-side and low-side power switches (12, 14) configured to perform synchronous rectification." *Id.* at 46 (citing Ex. 1007, Figs. 1, 3; Ex. 1003 ¶ 97). Petitioner provides the annotated version of Tateishi's Figure 3 reproduced below.



Id. Above is Petitioner's annotated version of Tateishi's Figure 3 with output 122 of the SR latch 116 in purple, input voltage Vin 16 in red, and, shaded in yellow and labeled "Power stage," high side switch 12, low side switch 14, ground 20, with switching node 22 between the high side switch 12 and the low side switch 14. *See* Ex. 1007 ¶ 18.

Patent Owner does not raise any arguments regarding these contentions beyond the unpersuasive arguments discussed above regarding Petitioner's purportedly inconsistent mapping of "control signal." *See* PO Resp. 29–34 (arguing that the "control signal" received by the "input voltage sensing circuit" of limitation 1B2 is not the same "control signal" received by the "power stage" of limitation 1E).

We have reviewed Petitioner's arguments and the underlying evidence, and we find that Petitioner has shown by a preponderance of the evidence that Tateishi discloses this limitations 1E.

j. Conclusion as to Independent Claim 1

Having considered the parties' arguments and evidence, we determine that Petitioner has shown by a preponderance of the evidence that claim 1 is anticipated by Tateishi.

3. The Asserted Anticipation of Independent Claims 11 and 18 by Tateishi

Petitioner contends that independent claims 11 and 18 are anticipated by Tateishi. Pet. 60–63, 66–72. Petitioner, with the support of Dr. Holberg's testimony and relying on many of the contentions made for independent claim 1, addresses the limitations of these claims. *See id.*

Patent Owner does not present arguments beyond those regarding independent claim 1 and discussed above. *See, e.g.*, PO Resp. 26 ("Claims 11 and 18 suffer from the same problem and are also not anticipated by Tateishi."); *id.* at 34 ("Claims 11 and 18 have similar language and the Petition suffers from the same deficiencies."); *id.* at 34–41 (arguing independent claims 1, 11, and 18 together). We acknowledge that Patent Owner's Sur-reply focuses its discussion on independent claim 18, rather than independent claim 1, but we discern no substantively different arguments. *See, e.g.*, PO Sur-reply 3 n.1 ("Claim 11 is substantively similar to claim 1. . . . Claims 18 is referenced in more detail herein, but the arguments are equally as applicable to claims 1 and 11."); *see also* PO Resp. 5 n.2 (Patent Owner, when quoting independent claim 1, stating that "Independent claims 11 and 18 recite similar limitations.").

Having considered the parties' arguments and evidence, we determine that Petitioner has shown by a preponderance of the evidence that Tateishi anticipates independent claims 11 and 18.

4. The Asserted Anticipation of Dependent Claims 2–4, 9, 10, 12–14, and 17 by Tateishi

The remaining claims in this ground, claims 2–4, 9, 10, 12–14, and 17, depend directly or indirectly from one of the independent claims also challenged in this ground. Petitioner, with the support of Dr. Holberg's testimony, addresses the limitations of these claims. *See* Pet. 47–60, 63–66. For these claims, Patent Owner does not present arguments beyond those regarding the independent claims and discussed above. *See, e.g.*, PO Resp. 1–4 (Introduction section summarizing the arguments).

Having considered the parties' arguments and evidence, we determine that Petitioner has shown by a preponderance of the evidence that Tateishi anticipates dependent claims 2–4, 9, 10, 12–14, and 17.

E. The Asserted Anticipation of Claims 1–4, 9–14, 17, and 18 by the Tateishi Patent

We understand Petitioner to argue, in the alternative to the ground based on the Tateishi application publication (Ex. 1007), that the Tateishi Patent (Ex. 1005) also anticipates claims 1–4, 9–14, 17, and 18. *See* Pet. 23–24 ("The Tateishi Patent is also prior art under (pre-AIA) §102(e)"; identifying Ground 1 as anticipation "under §102 by Tateishi and/or the Tateishi Patent"). However, we are unable to locate in the Petition or Petitioner's Reply a discussion of or citation to the Tateishi Patent other than under the Petitioner's heading "Identification of Challenge and Relief Requested" on pages 23 and 24 of the Petition. *Cf. id.* at i–x (Table of Contents identifying a section of the Petition discussing the Tateishi (Application) anticipation ground but not a section discussing a Tateishi Patent anticipation ground). Although the issued patent may be substantively identical to the published application, Petitioner does not assert

that, and we decline to compare the documents to determine whether that is the case. In light of Petitioner's silence on the alternative ground, Petitioner has not demonstrated by a preponderance of the evidence that the Tateishi Patent anticipates 1–4, 9–14, 17, and 18.

F. The Asserted Obviousness of Claims 5, 7, 8, and 15 over Tateishi and/or the Tateishi Patent

Petitioner asserts that claims 5, 7, 8, and 15 of the '377 patent would have been "obvious under §103 by Tateishi and/or the Tateishi Patent." Pet. 24 (table of the grounds); *but see id.* at 72 (heading identifying only Tateishi as the relied-on reference); *see also id.* at 72–82 (discussing the alleged obviousness of the claims challenged in this ground). Because the discussion of the ground does not mention the Tateishi Patent, we understand Ground 2 to be a single-reference obviousness challenge based on Tateishi (Exhibit 1007) alone.

Petitioner, with the support of Dr. Holberg's testimony, addresses the limitations of these claims and offers reasoning why the claimed subject matter would have been obvious. *See* Pet. 72–82. For these claims, Patent Owner does not present arguments beyond those regarding the independent claims and discussed above. *See* PO Resp. 41 ("Ground 2 addresses dependent claims. It does not cure the above-described deficiencies and fails for the same reasons.").

Having considered the parties' arguments and evidence, we determine that Petitioner has shown by a preponderance of the evidence that dependent claims 5, 7, 8, and 15 would have been obvious over Tateishi.

III. CONCLUSION[12]

Petitioner has shown by a preponderance of the evidence that claims 1–4, 9–14, 17, and 18 are anticipated by Tateishi and that claims 5, 7, 8, 15 would have been obvious over Tateishi.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–4, 9–14, 17, 18	102(b)	Tateishi	1–4, 9–14, 17, 18	
1–4, 9–14, 17, 18	102(e)	Tateishi Patent		1–4, 9–14, 17, 18
5, 7, 8, 15	103(a)	Tateishi, Tateishi Patent	5, 7, 8, 15	
Overall Outcome			1–5, 7–15, 17, 18	

IV. ORDER

For the foregoing reasons, it is

ORDERED that claims 1–5, 7–15, 17, and 18 of the ’377 patent have been proven to be unpatentable;

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[12] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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