

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.,
Petitioner,

v.

PICTIVA DISPLAYS INTERNATIONAL LTD.,
Patent Owner.

Case No. IPR2024-01187
Patent No. 9,257,492

**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO.
9,257,492 UNDER 35 U.S.C. §§ 311–319 AND 37 C.F.R. § 42.100 *et seq.***

TABLE OF CONTENTS

Contents

I.	INTRODUCTION	1
II.	STANDING, MANDATORY NOTICES AND FEE AUTHORIZATION	2
III.	SUMMARY OF CHALLENGE	4
IV.	OVERVIEW OF THE '492 PATENT	6
	A. Prosecution History	8
V.	LEVEL OF ORDINARY SKILL	9
VI.	CLAIM CONSTRUCTION	9
VII.	OVERVIEW OF PRIOR ART	9
	A. Ingle (Ex.1004, Ex.1005)	9
	B. Hasei (Ex.1006, Ex.1007)	12
	C. Hanamura (Ex.1008)	14
	D. Egitto (Ex.1013)	16
VIII.	APPLICATION OF PRIOR ART TO THE CHALLENGED CLAIMS	17
	A. Ground I: Claims 1, 2, 8-11, and 16 Are Obvious Over Ingle in view of Hasei.....	17
	1. Motivation to Combine Ingle and Hasei.....	18
	a) Ingle contemplates forming an optoelectronic assembly using a conventional process, like that of Hasei.....	18
	b) Both Ingle and Hasei teach forming an OLED device using structured application of layers, and Ingle teaches a substrate suitable for this purpose.....	21

2.	Independent Claim 10	26
3.	Dependent Claim 11: “The method as claimed in claim 10, wherein before the optically functional layer is applied, the second electrically conductive layer is removed in the component region and the optically functional layer is applied to the first electrically conductive layer in the component region.”	39
4.	Independent Claim 1	42
5.	Dependent Claim 2: “The method as claimed in claim 1, wherein a first electrode of a capacitor is formed by the first contact region between the dielectric and the substrate and a second electrode of a capacitor is formed by the electrode layer on a side of the dielectric facing away from the first contact region.”	45
6.	Dependent Claim 8: “The method as claimed in claim 1, wherein the dielectric is applied by a printing method.”	46
7.	Dependent Claim 9: “The method as claimed in claim 1, wherein the dielectric firstly is applied in a structured fashion to the second electrically conductive layer in such a way that it adjoins the first trench, and wherein then the dielectric is heated in such a way that it deforms and encapsulates edges and/or side surfaces of the first and second electrically conductive layers in the first trench.”	46
8.	Independent Claim 16	48
B.	Ground II: Claims 1, 2, 8, and 16 Are Obvious Based on Hanamura	50
1.	Independent Claim 1	50
2.	Dependent Claim 2: “The method as claimed in claim 1, wherein a first electrode of a capacitor is formed by the first contact region between the dielectric and the substrate and a second electrode of a capacitor is formed by the electrode layer on a side of the dielectric facing away from the first contact region.”	56

3.	Dependent Claim 8: “The method as claimed in claim 1, wherein the dielectric is applied by a printing method.”	58
4.	Independent Claim 16	58
C.	Ground III: Claims 3, 5, and 6 Are Obvious Based on Hanamura in view of Egitto	60
1.	Dependent Claim 3: “The method as claimed in claim 1, wherein before the dielectric is applied, a second trench and at least one third trench are formed, which delimit a resistance region, which comprises a part of the first and second electrically conductive layers and which has a taper in a direction parallel to the electrically conductive layers and which leads into the first contact region on a first side of the taper.	60
2.	Dependent Claim 5: “The method as claimed in claim 3, wherein the resistance region is formed such that it forms a third contact region on a second side of the taper and thus forms a resistor that is electrically connected in series with the capacitor.”	68
3.	Dependent Claim 6: “The method as claimed in claim 2, wherein a plurality of capacitors and/or resistors are formed electrically in parallel with one another and/or electrically in series one after another.”	69
IX.	DISCRETIONARY DENIAL IS INAPPROPRIATE UNDER <i>FINTIV</i>	70
X.	CONCLUSION.....	72

TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 9,257,492
1002	File History for U.S. Patent No. 9,257,492
1003	Declaration of Alex Kattamis, Ph.D.
1004	World Intellectual Property Organization Published Application No. 2011/036089 A1 (Ingle)
1005	Certified English Translation of World Intellectual Property Organization Published Application No. 2011/036089 A1 (Ingle)
1006	Japanese Patent Application Publication No. JP 2003-317610 (Hasei)
1007	Certified English Translation of Japanese Patent Application No. JP 2003-317610 (Hasei)
1008	U.S. Patent No. 5,691,877 (Hanamura)
1009	LEFT BLANK
1010	U.S. Patent No. 7,817,117
1011	LEFT BLANK
1012	LEFT BLANK
1013	U.S. Patent Publication No. 2009/0178271 (Egitto)
1014	James L. Sanford and Frank R. Libsch, <i>TFT AMOLED Pixel Circuits and Driving Methods</i> , 4.2 SID 03 Digest 10-12 (2003)
1015	Reiji Hattori et al., <i>Current-Writing Active-Matrix Circuit for Organic Light-Emitting Diode Display Using aSi:H Thin-Film-Transistors</i> , IEICE Trans. Electron., Vol.e83-C, No. 5 (May 2000)
1016	U.S. Patent No. 3,997,411 (Muenz)
1017	James W. Nilsson and Susan A. Riedel, <i>Electric Circuits</i> , Addison-Wesley Publishing Co. (5th ed. 1996)
1018	Alan B. Grebene, <i>Bipolar And MOS Analog Integrated Circuit Design</i> , John Wiley & Sons (1983)
1019	IEEE 100, <i>The Authoritative Dictionary of IEEE Standards Terms</i> (7th ed. Dec. 2000)
1020	Jiun-Haw Lee et al., <i>Introduction To Flat Panel Displays</i> , John Wiley & Sons (2008)

Petition for *Inter Partes* Review of U.S. Patent No. 9,257,492

Exhibit No.	Description
1021	Robert A. Street, <i>Technology and Applications of Amorphous Silicon in Materials Science</i> , Vol. 37 (2000)
1022	Gary S. May and Costas J. Spanos, <i>Fundamentals of Semiconductor Manufacturing and Process Control</i> (2006)
1023	Bruce E. Kahn, <i>Printing Methods for Printed Electronics</i> , Soc’y For Imagin Sci. & Tech.: NIP24 and Digital Fabrication 15-20 (2008), https://doi.org/10.2352/ISSN.2169-4451.2008.24.1.art00005_1
1024	Ana C. Arias et al., <i>Materials and Applications for Large Area Electronics: Solution-Based Approaches</i> , 110 Chemical Reviews 3-24 (2010)
1025	Docket Control Order, <i>Pictiva Displays International Ltd. v. Samsung Elec. Co., Ltd.</i> , No. 2:23-cv-00495, Dkt. #40 (E.D. Tex. Apr. 17, 2024)

I. INTRODUCTION

Samsung Display Co., Ltd. (“Petitioner”) petitions for *inter partes* review (“IPR”) seeking cancellation of claims 1-3, 5, 6, 8-11, and 16 (the “Challenged Claims”) of U.S. Patent No. 9,257,492 (Ex.1001, “’492 patent”), nominally assigned to Pictiva Displays International Ltd.

The Challenged Claims are directed to a passive electronic component (e.g., a capacitor), a method for producing a passive electronic component, and a method for producing an optoelectronic assembly that comprises both a passive electronic component and an optoelectronic component (e.g., an organic light emitting diode (“OLED”)). According to the claimed methods, both the dielectric layer and electrically conductive electrode layer are formed “in a structured fashion.”

The inventor of the ’492 patent, Andrew Ingle, disclosed the majority of the alleged invention more than two years earlier, in a PCT application that published on March 31, 2011. Like the ’492 patent, PCT Application Publication No. WO 2011/036089 A1 (“Ingle”) disclosed “a method for producing an electronic component and an electronic component,” including a capacitor and an OLED. Ingle, 1:8-9, 6:3-7. And like the ’492 patent, Ingle disclosed that layers could be deposited in a structured fashion, including through the aid of self-assembling monolayers and printing processes. *See id.*, 6:19-24, 15:26-35. Similarly, prior art Japanese Patent Application Publication No. JP 2003-317610 (“Hasei”) already

taught the use of inkjet printing to selectively deposit electrodes and thereby avoid the drawbacks of conventional photolithographic processes. The combination of Ingle and Hasei renders obvious all the limitations of claims 1, 2, 8-11, and 16, as shown in Ground I.

Beyond the inventor himself, U.S. Patent No. 5,691,877 (“Hanamura”), issued well before the ’492 patent, taught and/or suggested the same method for producing electronic assemblies including both capacitors and resistors. Meanwhile, U.S. Patent Publication No. 2009/0178271 (“Egitto”) disclosed how to manipulate the shape and size of resistor materials to control their overall resistance. Hanamura renders obvious all the limitations of claims 1, 2, 8, and 16, as shown in Ground II. The combination of Hanamura and Egitto renders obvious all the limitations of claims 3, 5, and 6, as shown in Ground III.

II. STANDING, MANDATORY NOTICES AND FEE AUTHORIZATION

Grounds for Standing: Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the ’492 patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the ’492 patent on the ground identified in this petition.

Real Party-in-Interest: Petitioner identifies Samsung Display Co., Ltd., Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. as real parties-in-interest.

Related Matters: Patent Owner has asserted the '492 patent in litigation against Samsung Electronics Co. Ltd. and Samsung Electronics America, Inc. in *Pictiva Displays International Ltd. v. Samsung Electronics Co., Ltd.*, Case No. 2:23-cv-00495 (E.D. Tex.) and *Pictiva Displays International Ltd. v. Samsung Electronics Co., Ltd.*, Case No. 2:24-cv-00532 (E.D. Tex.).

Lead and Back-Up Counsel: Petitioner designates Scott C. Weidenfeller (Reg. No. 54,531, SWeidenfeller@cov.com) as lead counsel, of Covington & Burling LLP, One CityCenter, 850 Tenth Street, NW, Washington, DC 20001 (postal and hand delivery), telephone: (202) 662-6000, facsimile: (202) 662-6291.

Petitioner designates David A. Garr (Reg. No. 74,932, dgarr@cov.com) as back-up counsel, of Covington & Burling LLP, One CityCenter, 850 Tenth Street, NW, Washington, DC 20001 (postal and hand delivery), telephone: (202) 662-6000, facsimile: (202) 662-6291.

Service Information: Service information is provided in the designation of counsel above. Petitioner consents to service of all documents via electronic mail at the email addresses above and at SDC-Pictiva-IPR@cov.com.

Fee Authorization: The Office is authorized to charge all fees due in connection with this proceeding to Deposit Account No. 60-3160.

III. SUMMARY OF CHALLENGE

Petitioner requests IPR based on the following grounds:

- **Ground I:** Claims 1, 2, 8-11, and 16 are obvious over Ingle in view of Hasei;
- **Ground II:** Claims 1, 2, 8, and 16 are obvious over Hanamura; and
- **Ground III:** Claims 3, 5, and 6 are obvious over Hanamura in view of Egitto.

The '492 patent is a U.S. national stage application of PCT Application No. PCT/EP2013/067348, filed August 20, 2013, and claims priority to a foreign application filed September 27, 2012. Petitioner's challenge is based on the following references, which are available as prior art under 35 U.S.C. § 102 (AIA)¹ as shown in the following table:

¹ The application for the '492 patent was filed after March 16, 2013, but claims priority to a German patent application filed prior to March 16, 2013. During prosecution, the application was "examined under the first inventor to file provisions of the AIA." Ex.1002, 471. Accordingly, it is treated as such herein. Nevertheless, as shown, the references relied upon qualify as prior art, and render obvious the Challenged Claims, under both the AIA and pre-AIA conditions for patentability.

Exhibit	Reference	Date(s)	Availability as Prior Art	
			Pre-AIA	AIA
Ex.1004 (certified translation provided as Ex.1005)	WO 2011/036089 A1 (Ingle)	Filed Sept. 16, 2010; Published Mar. 31, 2011	§§ 102(a), (b)	§ 102(a)
Ex.1006 (certified translation provided as Ex.1007)	Japanese Publication Application No. JP2003-317610 (Hasei)	Filed Apr. 18, 2002; Published Nov. 7, 2003	§§ 102(a), (b)	§ 102(a)
Ex.1008	U.S. Patent No. 5,691,877 (Hanamura)	Filed Feb. 16, 1996; Issued Nov. 25, 1997	§§ 102(a), (b), (e)	§ 102(a)
Ex.1013	U.S. Patent Publication No. 2009/0178271 (Egitto)	Filed Jan. 16, 2008; Published July 16, 2009	§§ 102(a), (b), (e)	§ 102(a)

The Examiner did not rely upon any of these prior art references during prosecution, nor did the Examiner consider any of the combinations of prior art references presented by the Grounds herein.² The supporting declaration of Alex Kattamis, Ph.D. (Ex.1003) was also not before the examiner. Accordingly, the

² Two relatives of Ingle, a German relative, DE 102009060066, and a U.S. relative, U.S. Patent Publication No. 2012/0267147, were provided during prosecution; however, neither was relied upon by the Examiner. Ex.1002 (File History), 289, 332.

obviousness grounds and arguments in this Petition are not the same (or substantially the same) as those previously presented to the Office.

IV. OVERVIEW OF THE '492 PATENT

The '492 patent is directed to “a method for producing a passive electronic component and/or a method for producing an optoelectronic assembly[.]” *See, e.g.*, '492 patent, 1:41-46. The claimed methods include forming layers of electrically-conductive and dielectric (insulating) materials on a substrate. These layers can be arranged to produce a passive electronic component, such as a capacitor or resistor. *See, e.g., id.*, 8:22-24. They can also be used in producing an optoelectronic assembly, which may include, for example, one or more passive electronic components and one or more optoelectronic components. *See, e.g., id.*, 8:29-52.

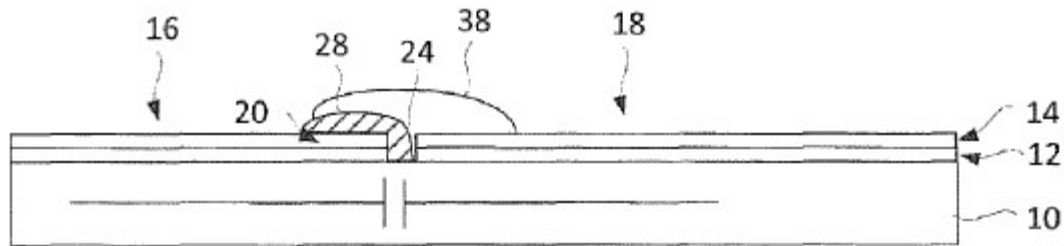
The '492 patent alleges benefits of applying layers “in a structured fashion,” as compared to applying layers “without structure” and later structuring the layers using known methods like photolithography. For example, in its “Background,” the '492 patent states that: “Suitable insulators or dielectrics such as light-sensitive resists” are conventionally “applied *without structure* in a planar fashion to metal layers,” after which photolithography masks are used to selectively remove the resist from particular regions, “as a result of which the resist layer is structured.” *Id.*, 1:27-

37.³ This conventional approach, according to the '492 patent, is “usually very expensive and complex.” *Id.*

To purportedly simplify and/or lower cost of production, the '492 patent states that “the dielectric and/or the electrode layer and/or subsequently [*sic*] further layers or materials” may be “*applied in a structured fashion . . . for example by printing, for example inkjet printing or screen printing, by blade coating and/or by deposition with the aid of SAMs (self-assembling monolayers) and the like.*” *Id.*, 1:66-2:19. The '492 patent states that, through this approach, “the desired structure is already formed during the application of the corresponding layer,” and “[t]he area to be coated is thus coated only in partial regions dependent on the desired structure.” *Id.*, 1:66-2:4.

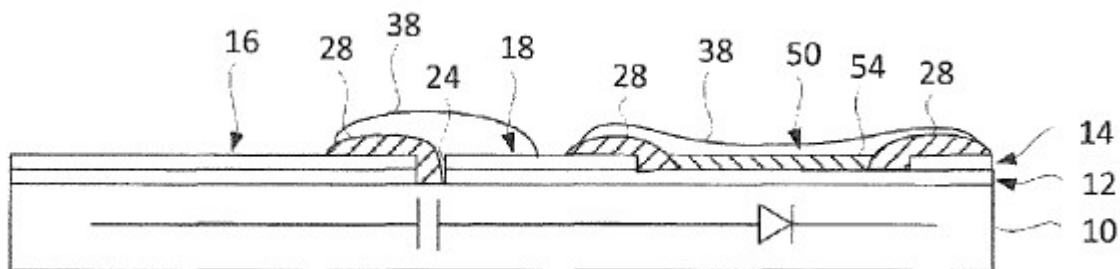
An exemplary result of the '492 patent's method for producing a passive electronic component is depicted in Figure 7, which “shows the substrate 10 and the first and second electrically conductive layers 12, 14 with the dielectric 28, wherein an electrode layer 38 is applied in a structured fashion on the dielectric 28 and a part of the second contact region 18.” *Id.*, 12:27-31. The passive component of Figure 7 “can form a capacitor, for example.” *Id.*, 12:40-42.

³ All emphasis added except where otherwise noted.



Id., Fig. 7.

An exemplary result of the '492 patent's method for producing an optoelectronic assembly that combines a passive electronic component and an optoelectronic component is depicted in Figure 16. Figure 16 shows a passive electronic component, *i.e.*, a capacitor like that of Figure 7, in combination with an optoelectronic component, *i.e.*, an OLED comprising "an organically functional layer 54 . . . formed in the component region 50." *Id.*, 14:31-34.



Id., Fig. 16.

The '492 patent includes three independent claims (claims 1, 10, 16) and fifteen dependent claims (claims 2-9, 11-15, 17-18).

A. Prosecution History

The prosecution history for the '492 patent is relatively short; the '492 patent received a first action allowance. The Examiner's reasons for allowance merely

stated that “[t]he prior art of record neither anticipates nor renders obvious all the limitations in the base claims 1, 10, and 16.” Ex.1002 (File History), 324-26.

V. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) for the ’492 patent would have had a bachelor’s degree in Electrical Engineering, Physics, or a comparable field of study, and at least three years of research or industrial experience with semiconductor (organic or inorganic) optoelectronic devices and/or lighting or displays. Ex.1003, ¶46. An individual with additional education could have less research or industrial experience and vice-versa. *Id.*

VI. CLAIM CONSTRUCTION

Claims in an IPR are construed in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history. 37 C.F.R. § 42.100(b); *see Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). Petitioner does not believe that any specialized constructions are necessary for this petition.

VII. OVERVIEW OF PRIOR ART

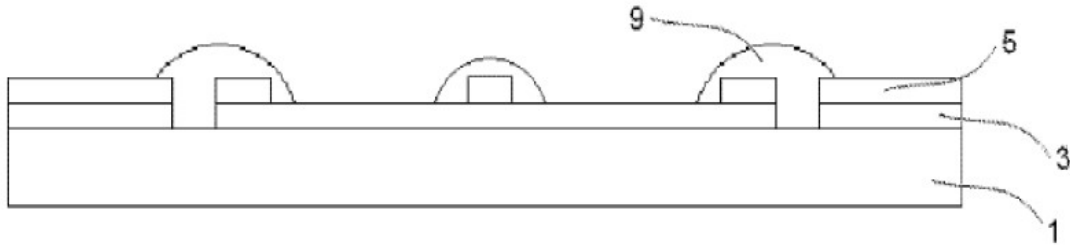
A. Ingle (Ex.1004, Ex.1005)

PCT Application Publication No. WO 2011/036089 A1 (“Ingle”), the primary reference in Ground I, names as an inventor the sole-named inventor of the ’492 patent, Andrew Ingle. Ingle was published on March 31, 2011, more than one year before the ’492 patent’s September 27, 2012, foreign priority date.

Similar to the '492 patent, Ingle “relates to a method for producing an electronic component and an electronic component.” Ingle, 1:8-9. Ingle’s method, like that of the '492 patent, forms components like “a capacitor” and “an organic electronic component, such as an organic light-emitting diode.” *Id.*, 6:3-7. Like the '492 patent, Ingle discloses application of layers in a structured fashion, *e.g.*, “[o]ne task of [Ingle’s] invention is to provide an improved method of producing an electronic component . . . in which the insulator *is only applied to certain areas of* an electrically conductive layer.” Ingle, 1:22-25. Like the '492 patent, Ingle teaches that structured application of layers may “be done by applying the first and second electrically conductive layers or parts thereof to the substrate, for example by printing, by deposition with the aid of SAMs (self-assembling monolayers) and the like.” *Id.*, 6:19-24; *see also* 15:26-35 (“Suitable printing processes include . . . screen printing, inkjet printing, flexographic printing and the like.”). Ingle alleges the same benefits of this approach as the later-filed '492 patent: “[t]he method according to [Ingle’s] invention is usually free of photolithographic steps and can therefore be used as a cost-effective method for producing an electronic component, such as an organic light-emitting diode.” *Id.*, 18:7-10.

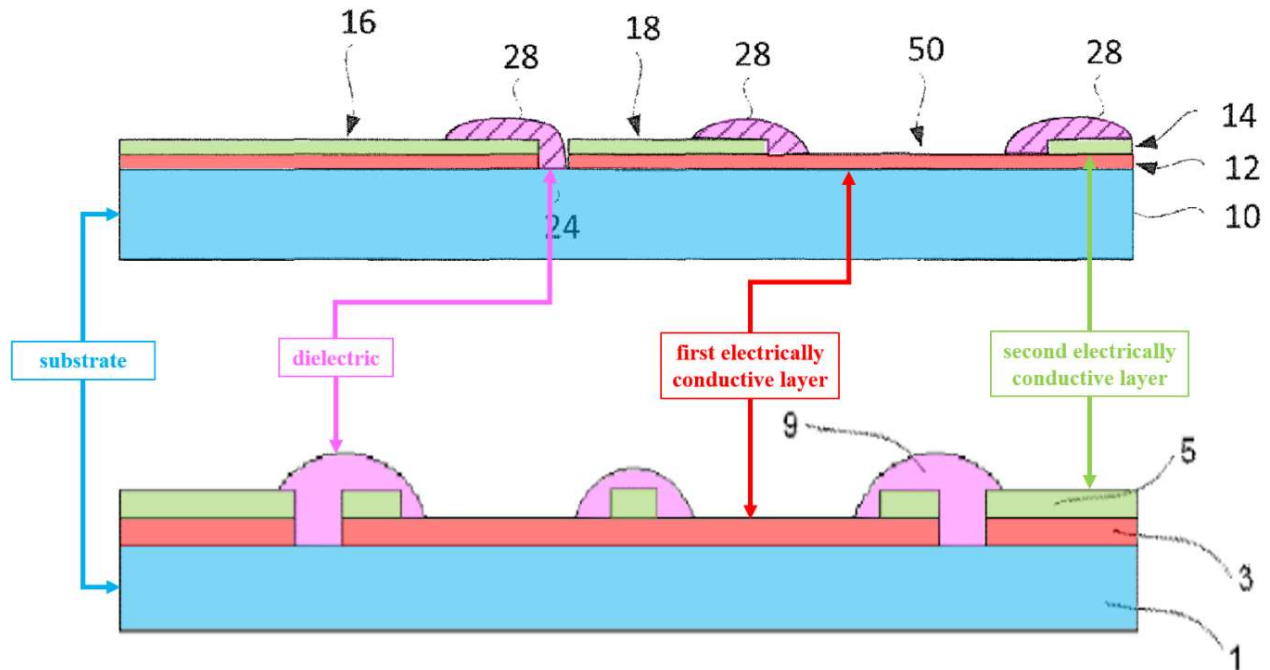
Ingle describes its claimed method as “suitable for producing an electronic component having at least one first electrode region and a second electrode region, which are separated from one another by an insulator and each have at least a partial

layer of a first electrically conductive material,” as shown in, for example, in its Figure 1I (reproduced below). *Id.*, 2:2-7.



Id., Fig. 1I.

A comparison of Fig. 1I of Ingle with Figure 15 of the '492 patent (below) shows that the devices in both share the same base structure that can be used to form, among other things, “a capacitor” and “an organic electronic component, such as an organic light-emitting diode.” *Id.*, 6:3-7. After detailing how to build the base structure depicted in its Figure 1I, Ingle teaches that “an OLED, can now be produced on the substrate layer . . . using a conventional process.” *Id.*, 21:34-36.



'492 patent Fig. 15 (annotated, top); Ingle Fig. 1I (annotated, bottom).

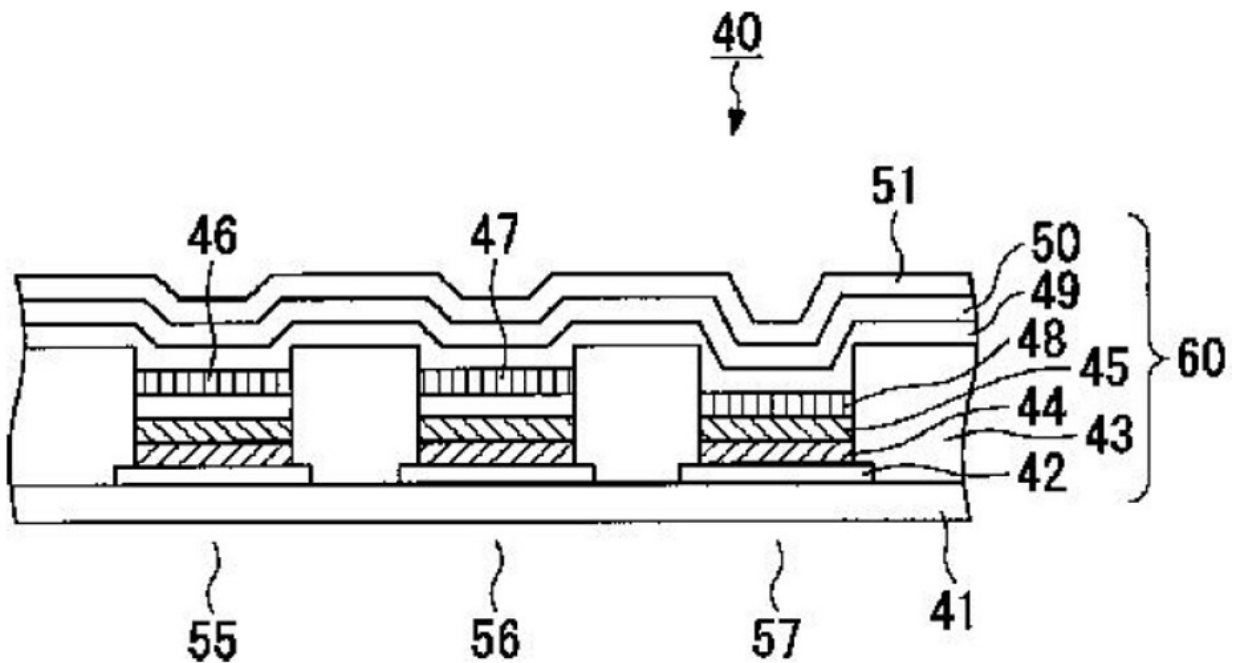
B. Hasei (Ex.1006, Ex.1007)

Japanese Patent Application Publication No. JP 2003-317610 ("Hasei") published in November 2003, *i.e.*, almost a decade before the '492 patent's claimed priority date. As detailed below, Hasei illustrates the "conventional process" for forming the OLED contemplated in Ingle (*see* Ingle, 21:34-36), and accordingly serves as a secondary reference in Ground I.

Like Ingle and the '492 patent, Hasei teaches structured application of layers. For example, Hasei notes that "the conventional method of providing a conductive pattern requires a photomask to be used in the photolithography process, which lengthens the manufacturing process and requires that a photomask be made each

time the model of the conductive pattern is changed.” Hasei, ¶3. Hasei teaches a method that deposits material using “an inkjet head of a droplet discharging device,” *i.e.*, “inkjet device,” to *only* the desired locations on a substrate. *Id.*, ¶15. Through Hasei’s approach, “there is no need to create a photomask, so the manufacturing time required for forming a conductive pattern of a transparent electrode or the like can be shortened, and manufacturing costs can be reduced.” *Id.*, ¶5.

Furthermore, like Ingle and the ’492 patent, Hasei’s structured application of layers is for making an electro-optical device. For example, Hasei’s Figure 3 illustrates “a cross-sectional view depicting an example of an organic EL device manufactured using [Hasei’s] method for manufacturing an electrode wiring pattern.” *Id.*, ¶31.



Id., Fig. 3.

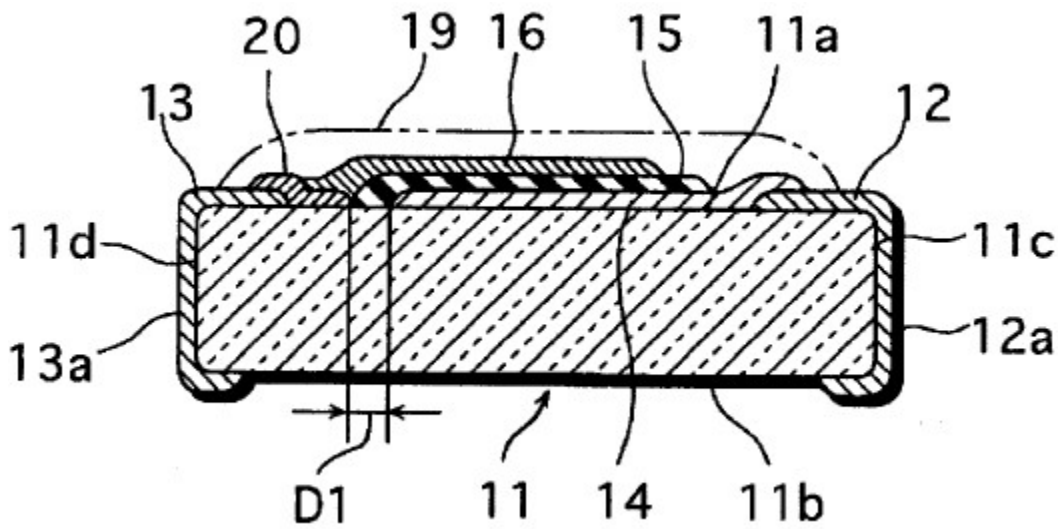
As shown above, Hasei's Figure 3 "includes a substrate (light transmitting layer) 41 capable of transmitting light, an organic EL element (light emitting element) 60 formed on one surface of the substrate 41, sandwiched between a pair of a negative electrode (electrode) 50 and a positive electrode (transparent electrode) 42, and which includes light emitting layers 46, 47, 48 made of an organic electroluminescent material and a hole injection layer 44," a "protective layer 51 for protecting the organic EL element 60," *Id.*, ¶32, and "thin film 49," which "is an electron transport layer or an electron injection layer." *Id.*, ¶38. The "negative electrode 50 is a metal electrode" that "may be formed by the droplet discharging method." *Id.*, ¶37.

C. Hanamura (Ex.1008)

U.S. Patent No. 5,691,877 ("Hanamura") issued in 1997, well before the '492 patent's claimed priority date of September 27, 2012. Hanamura discloses the '492 patent's technique for forming a capacitor and a resistor and serves as the primary reference in Grounds II and III.

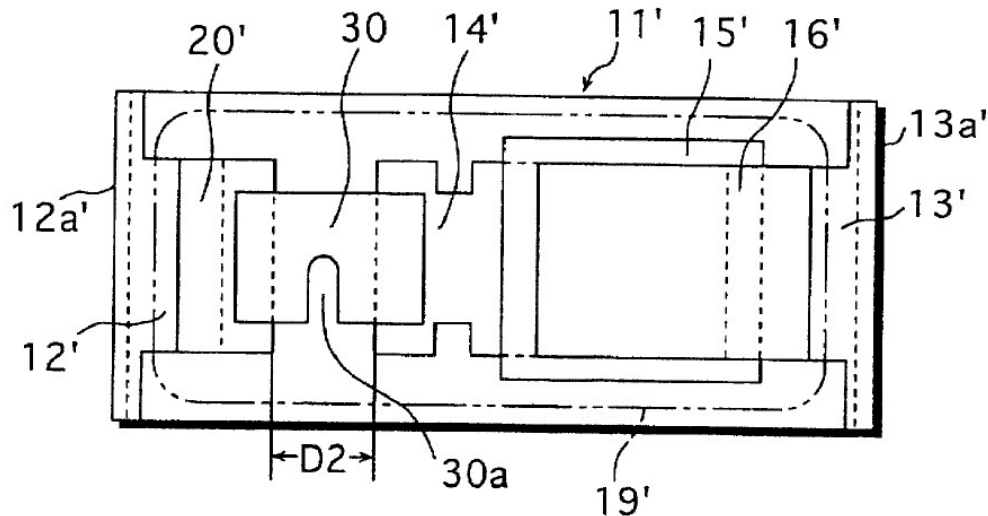
For example, Hanamura discloses "a chip type thick film capacitor wherein a capacitor element is formed on an insulating chip substrate." Hanamura, 1:6-10. Hanamura notes that successive screen printing of two metal layers—the first to form electrode leads and the second to form a first capacitor electrode—causes the two metal layers to come into electrical conduction with one another, thereby

shorting the electrodes of the capacitor and rendering the device inoperative. *Id.*, 1:49-59. Hanamura solves this problem by forming a first capacitor electrode and an auxiliary electrode in a single screen-printing step. *See, e.g., id.*, 5:52-62. As shown in Hanamura's Figure 1 (reproduced below), Hanamura's first capacitor electrode 14 and auxiliary electrode 20 are separated by predetermined spacing "D1," which prevents the two from shorting. *Id.* This space is subsequently filled with a dielectric layer 15, like the trench in the '492 patent.



Id., Fig. 1.

Hanamura further teaches a method of manufacturing a resistor in conjunction with a capacitor. *See Id.*, 1:6-10 (disclosing a "chip type thick film capacitor which incorporates a resistor to work as a composite device."). Similar to the '492 patent, Hanamura "reliably adjust[s]" resistance of the device by adjusting the dimensions of a resistor layer 30. *See, id.*, 2:39-41, 6:50-58, 7:34-39. As illustrated in

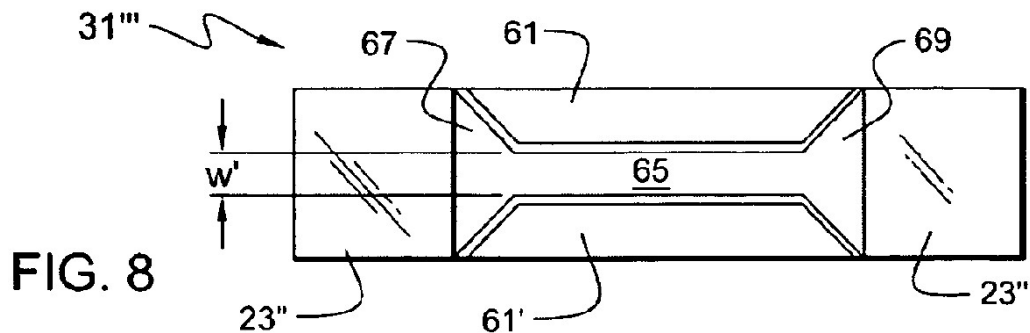


D. Egitto (Ex.1013)

For example, Egitto “provid[es] resistors for circuitized substrates such as printed circuit boards, chip carriers and the like.” Egitto, ¶1. Egitto explains that “it is often necessary to adjust the resistance of the film resistors in the circuit.” *Id.*, ¶5. Like Hanamura, Egitto teaches that, “[t]o increase the resistance of a film resistor, the resistor [can be] ‘trimmed’, often by forming a slot across the electrical current

path in the resistor and to make the effective width of the resistor (and the current path there-through) smaller and thereby increasing resistance.” *Id.*

Figure 8 of Egitto (reproduced below) illustrates a pattern that may be formed in the resistor material according to Egitto’s teachings. *See Id.*, ¶52. Egitto discloses that a laser may be used to form isolated parts 61 and 61’, thereby creating a remaining portion of the resistor material 65 with “a rectangular shape with substantially triangular ends 67 and 69.” *Id.*, ¶¶82-83.



Id., Fig. 8.

VIII. APPLICATION OF PRIOR ART TO THE CHALLENGED CLAIMS

A. Ground I: Claims 1, 2, 8-11, and 16 Are Obvious Over Ingle in view of Hasei

Independent claim 1 of the '492 patent is directed to a method of producing a passive electronic component (*e.g.*, a capacitor); independent claim 16 is directed to the passive electronic component itself. Independent claim 10 is directed to a method of producing an optoelectronic assembly that includes both a passive electronic component (like in claims 1 and 16) and an optoelectronic component (*e.g.*, OLED).

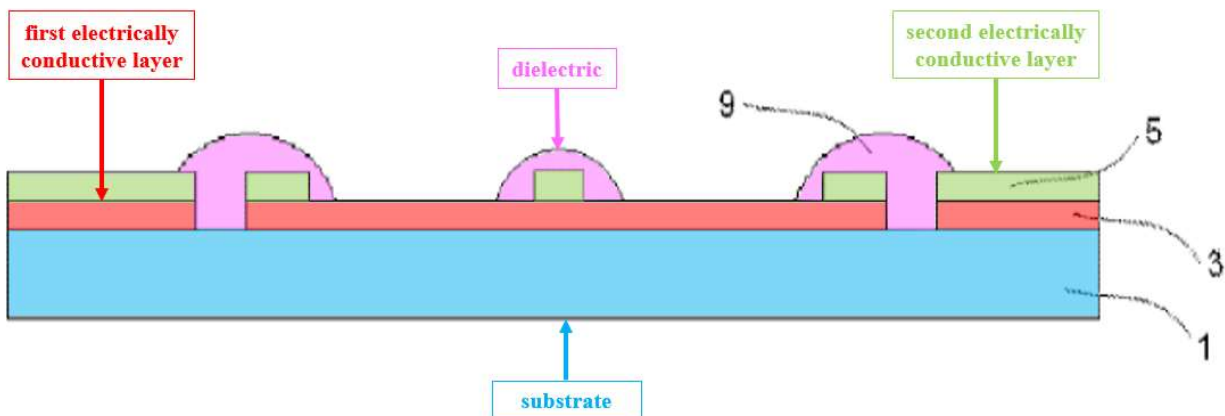
As the method of producing the passive electronic component is subsumed within the method of producing the optoelectronic assembly, the limitation-by-limitation analysis in this Ground addresses Independent claim 10 first.

1. Motivation to Combine Ingle and Hasei

A POSITA would have been motivated to combine Ingle and Hasei. Ex.1003, ¶¶108-25.

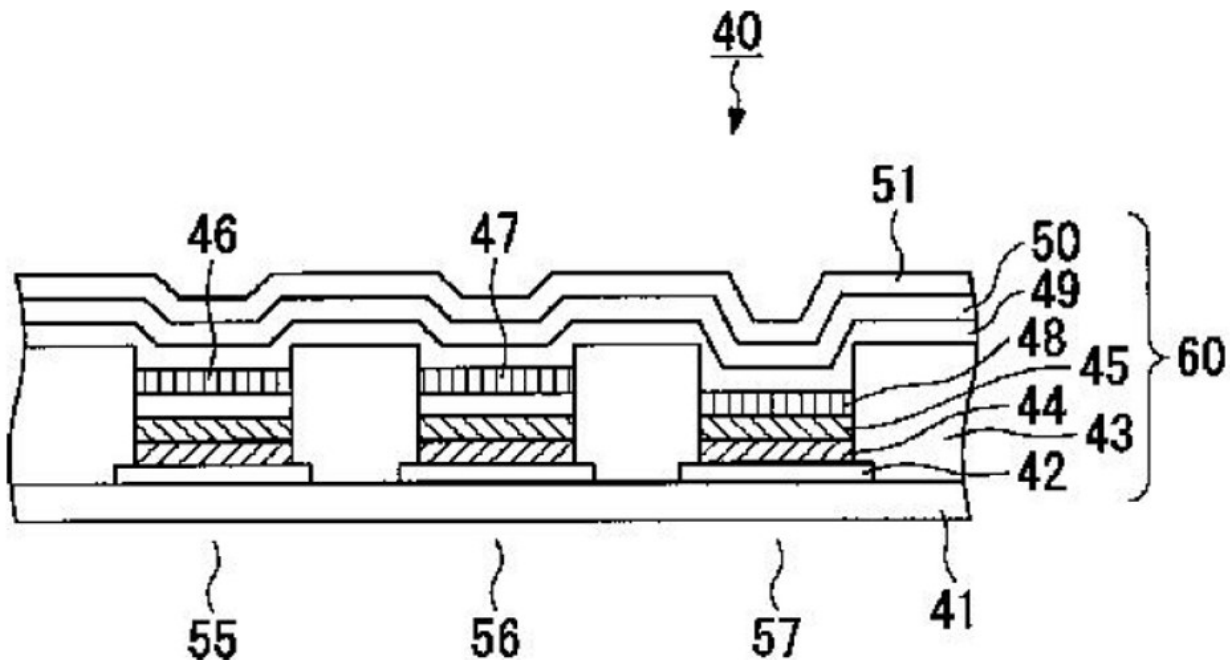
a) Ingle contemplates forming an optoelectronic assembly using a conventional process, like that of Hasei.

Ingle discloses “the preparation of a substrate for producing an electronic component using the method according to [its] present invention.” Ingle, 19:3-5. Ingle depicts this base structure in Figure 1I. *See* Ex.1003, ¶109.



Ingle, Fig. 1I (annotated). *See* Ex.1003, ¶109. Ingle explains that, once the base structure is prepared, “[t]he electronic component, for example an OLED, can [then] be produced on the substrate layer . . . using a conventional process.” Ingle, 21:34-36. *See* Ex.1003, ¶110.

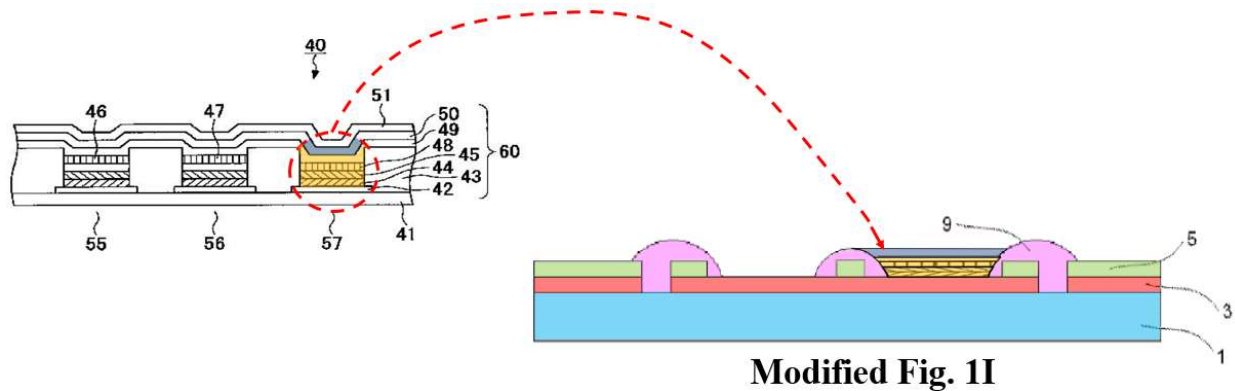
Hasei discloses such a conventional process for forming an OLED. As discussed (*supra* §VII.B), Hasei discloses “an organic EL element (light emitting element) 60 formed on one surface of [a] substrate 41, sandwiched between a pair of a negative electrode (electrode 50) and a positive electrode (transparent electrode) 42, and which includes light emitting layers 46, 47, 48 made of organic electroluminescent material and a hole injection layer 44,” as shown in Figure 3. Hasei, ¶32.



Hasei, Fig. 3. *See* Ex.1003, ¶¶111-12.

It would have been obvious to a POSITA to form Hasei’s OLED on Ingle’s base structure, as depicted below. Doing so would have been nothing more than combining prior art elements according to known methods and applying a known technique to improve a similar device in the same way to obtain predictable results.

KSR Int'l., Co. v. Teleflex Inc., 550 U.S. 398, 401 (2007). A POSITA would have had a reasonable expectation of success in making such a combination, considering the similarities between the teachings of Ingle and Hasei, and Ingle's direction to incorporate an OLED on Ingle's base structure. Ex.1003, ¶112.



Hasei, Fig. 3 (upper-left, annotated); Ingle, Fig. 11 (lower-right, annotated, modified). See Ex.1003, ¶112.

Hasei's OLED is bottom-emitting—*i.e.*, light shines from the electroluminescent layer through the substrate. Hasei, ¶33; see Ex.1003, ¶¶113-14. Accordingly, Hasei teaches that “the material forming the substrate 41 may be a transparent or semi-transparent material that can transmit light, such as transparent glass, quartz, sapphire, or a transparent synthetic resin,” Hasei, ¶33, and that “[t]he positive electrode 42 is a transparent electrode made of indium tin oxide or the like.” *Id.*, ¶34.

Ingle similarly contemplates a structure that would facilitate a bottom-emitting OLED. Ingle teaches that “[t]he substrate may be a transparent” layer that

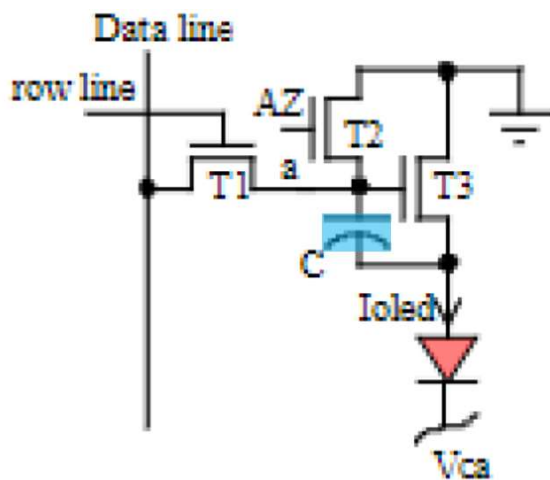
comprises “glass, quartz, [or] sapphire.” Ingle, 5:3-8. Further, Ingle’s “first electrically conductive layer may be a transparent” layer comprising “a transparent conductive oxide (TCO), e.g. indium-doped tin oxide (ITO).” *Id.*, 3:30-35. Accordingly, a POSITA would have reasonably expected that Ingle’s base structure for a conventional OLED would readily accommodate Hasei’s OLED. *See* Ex.1003, ¶115.

A POSITA would also expect success as Hasei and Ingle utilize similar materials to form light-emitting layers. For example, Ingle explains that its “functional layer” “can be radiation-emitting layers, such as *fluorescent and/or phosphorescent emitter layers*.” Ingle, 5:32-36. Similarly, Hasei discloses that its “light emitting layers 46, 47, and 48 can be formed from . . . light emitting materials such as various *fluorescent and phosphorescent materials*.” Hasei, ¶37; Ex.1003, ¶¶116-19.

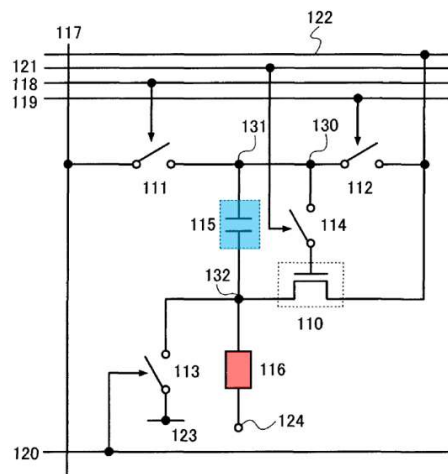
b) Both Ingle and Hasei teach forming an OLED device using structured application of layers, and Ingle teaches a substrate suitable for this purpose.

A POSITA would recognize the electronic components contemplated in Ingle—e.g., “a capacitor” and “an organic electronic component, such as an organic light-emitting diode” (Ingle, 6:3-7)—as conventional components of an optoelectronic assembly. Ex.1003, ¶¶120-121. A POSITA would understand that such OLED devices typically require passive circuit components, and that placing

capacitors in close proximity (or directly connected) to optically functional layers are a conventional way to form such devices. Ex.1003, ¶¶101-07; 120-22. For instance, pixel circuits were already widely used in OLED mobile phone screens as of the '492 patent, Ex.1003, ¶123, and it was well understood that such circuits (as shown below) rely on OLEDs in conjunction with common passive components like transistors and capacitors. *Id.*, ¶101-07.



Ex.1014, Fig. 6 (annotated)



Ex.1010, Fig. 1 (annotated)

See Ex.1003, ¶¶106-07.

Accordingly, a POSITA attempting to produce an optoelectronic assembly would know that an OLED may be connected to a capacitor. Ex.1003, ¶106. The POSITA would readily recognize Ingle's base structure as suitable for this purpose, particularly in light of Ingle's disclosure that its "electronic component" could be "a capacitor" or "an organic electronic component, such as an organic light-emitting diode." Ingle, 6:3-7; *see also* Ex.1003, ¶121.

Ingle discloses that a capacitor may be built at the separation area 7, *i.e.*, the location of the trench. *See* Ingle, 20:1-7 (“As shown in Fig. 1D, laser ablation then takes place which produces a separation area 7 or a trench in the second electrically conduction layer 5 and the first electrically conductive layer 3. The separation area 7 represents the subsequent electrical insulation between the cathode and the anode of the electric component.”). A POSITA would recognize that a capacitor could be formed on Ingle’s base structure (*e.g.*, Ingle’s Fig. 1D) simply by adding a second electrode (*i.e.*, cathode) on top of the leftmost portion of insulator 9 (pink) at the location of the trench, as illustrated below. *See* Ex.1003, ¶¶124-25. This would form a capacitor (brown dashed box), comprising a first electrode (region to the left of capacitor), an insulator (pink), and the added second electrode (grey). The second electrode would be in contact with the first electrically conductive layer 3 (red), such that the capacitor (brown dashed box) is in direct electrical contact with the OLED (purple dashed box), consistent with conventional pixel circuits (as described above).

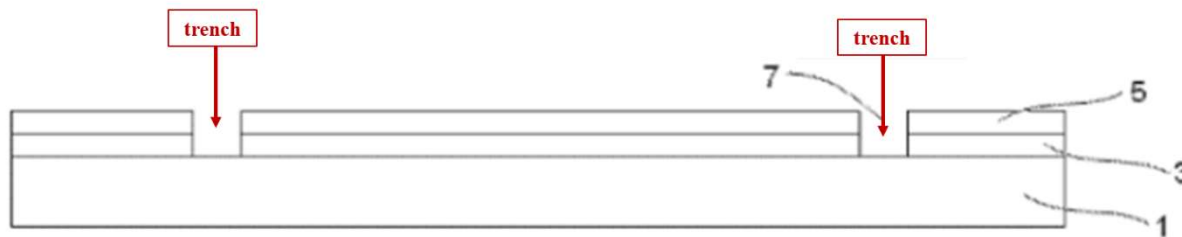
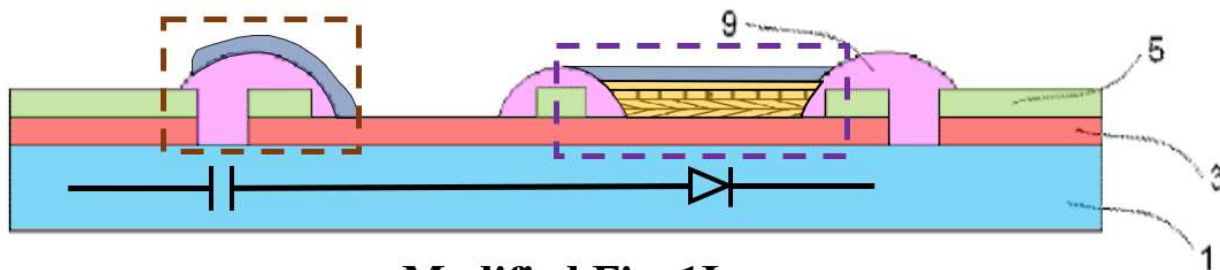


Fig. 1D

Ingle, Fig. 1D (annotated).



Modified Fig. 1I

Ingle, Fig. 1I (annotated, modified). *See* Ex.1003, ¶129.

Ingle leaves open how to finish forming a capacitor on its base structure, *i.e.*, how to apply the cathode. Nonetheless, given Ingle’s emphasis on applying layers in a structured manner, it would have been obvious to a POSITA to apply the capacitor’s cathode in such manner. For example, Ingle touts that its method “is usually free of photolithographic steps” (Ingle, 18:7-10), and that “each layer of the component can be applied individually and, if necessary, structured according to desire or purpose.” *Id.*, 7:20-24. Hasei similarly advocates for a structured application process, *e.g.*, using a droplet discharge device like an inkjet printer,

rather than photolithography. *See, e.g.*, Hasei, ¶¶14-15, 37. Hasei explains that using such a method, the electrode material “is discharged only onto the portion of the substrate where the conductive pattern is to be formed,” and thus wastage of electrode material is “significantly reduced.” *Id.*, ¶¶5, 7. Hasei further teaches that, because there is no need to create a photomask, “the manufacturing time required for forming a conductive pattern . . . can be shortened.” *Id.*

The OLED’s cathode would likewise be applied in a structured fashion. *See, e.g.*, Hasei, ¶ 37 (“The negative electrode 50 may be formed by the droplet discharging method.”). Thus, a POSITA would read Ingle and Hasei as teaching that the cathode of *each of* the OLED and the capacitor could be formed without photolithography. *See* Ingle, 18:7-10 (disclosed method “is usually free of photolithographic steps”).

Furthermore, a POSITA would recognize that this approach could allow both cathodes to be formed during the same manufacturing step. *See* Ex.1003, ¶170. A POSITA would have a reasonable expectation of success considering Hasei’s disclosures that structured application allows material to be “discharged only onto the portion of the substrate where the conductive pattern is to be formed.” Hasei, ¶¶5, 7; *see also* Ingle, 15:19-24 (applying “material at specific points by means of a printing process [makes it] possible to reduce or eliminate the risk of errors caused by incorrect alignment of the photolithographic system.”). Thus, using Hasei’s inkjet

printing method would have been nothing more than applying a known method of structured application, *e.g.*, droplet discharge, to improve a similar device, *e.g.*, the OLED and capacitor of Ingle, to obtain predictable results, *e.g.*, a manufacturing process free from photolithography. Ex.1003, ¶¶168-170.

Accordingly, it would have been obvious for a POSITA to build an optoelectronic assembly comprising a capacitor and OLED based on the teachings of Ingle in view of Hasei. As discussed below, the combination of Ingle in view of Hasei teaches or suggests each and every limitation of claims 1, 2, 8-11, and 16 of the '492 patent.

2. Independent Claim 10

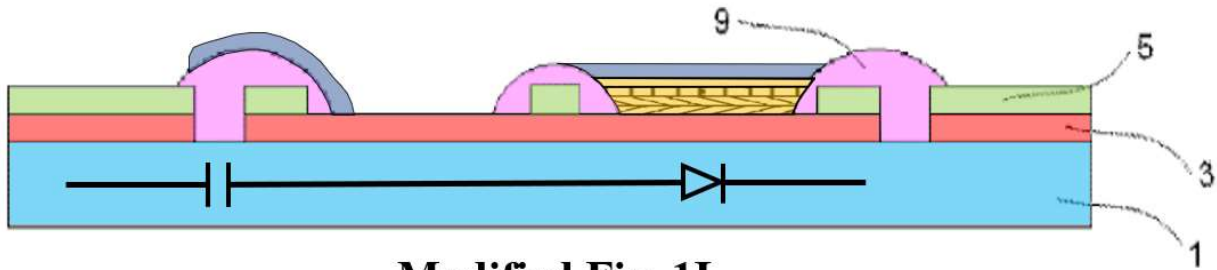
a) Element 10[Pre]: “A method for producing an optoelectronic assembly, comprising:”

To the extent the preamble is limiting, Ingle in view of Hasei renders it obvious. Ex.1003, ¶¶126-30.

The '492 patent explains that “[a]n optoelectronic assembly may include for example a passive electronic component and one, two or more optoelectronic components,” which may be an organic light emitting diode. '492 patent, 8:29-31, 36-42.

Ingle describes building both optoelectronic and passive components on a substrate. Ex.1003, ¶128.

As discussed in Section VIII.A.1, it would have been obvious based on the disclosures of Ingle and Hasei to build an optoelectronic assembly including both a capacitor and an OLED, as shown in the modified Figure 1I below.



Modified Fig. 1I

Ingle, Fig. 1I (annotated, modified). *See* Ex.1003, ¶129.

Accordingly Ingle in view of Hasei renders obvious the preamble.

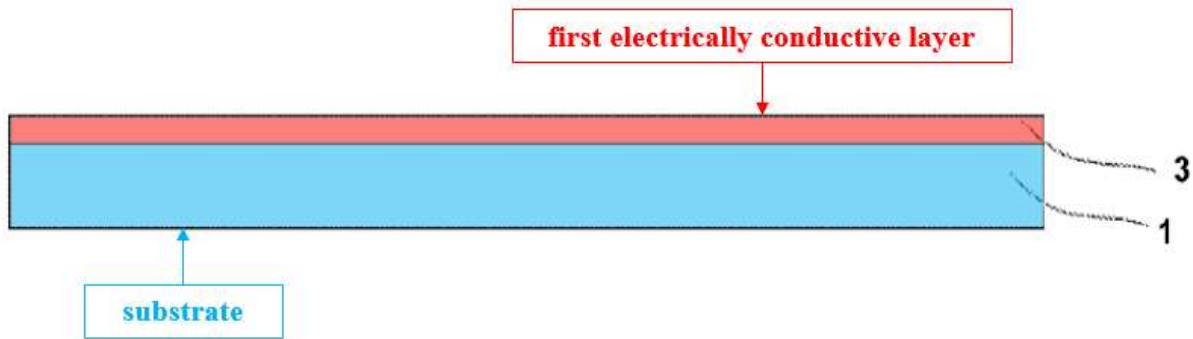
b) Element 10[a]: “forming a passive electronic component, the passive electronic component, comprising:”

Ingle teaches or suggests this element. Ex.1003, ¶¶131-34. Ingle discloses “a method for producing an electronic component.” Ingle, 1:7-8. In particular, the method can be used to form “a capacitor,” *id.*, 6:3-7, which is a passive electronic component. Ex.1003, ¶132; *see also* ’492 patent 2:20-21 (“A passive electronic component can be for example a capacitor.”). As discussed above, it would have been obvious to use Ingle’s method to form the capacitor in an OLED driving circuit.

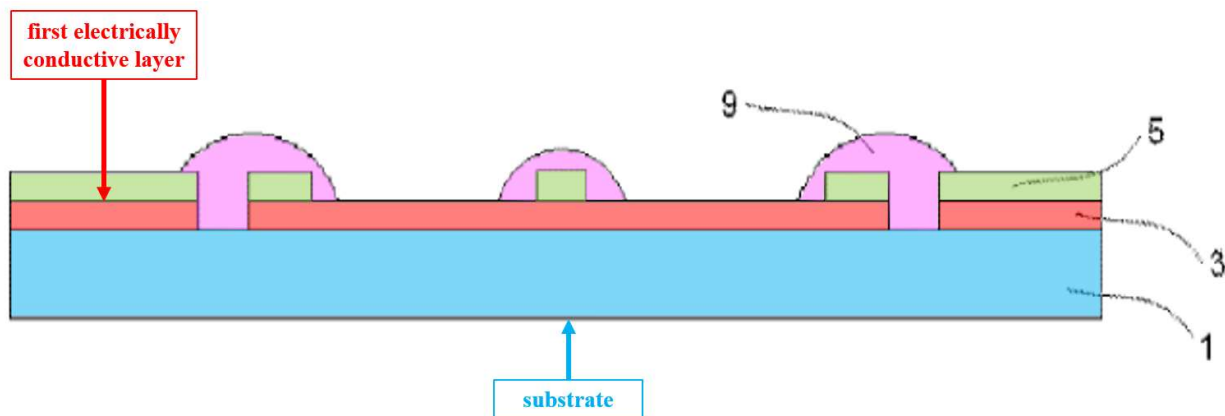
See supra § VIII.A.1.

c) **Element 10[b]: “a first electrically conductive layer on a substrate,”**

Ingle teaches or suggests this element. Ex.1003, ¶¶135-38. As shown in the annotated figure, below, Ingle’s method begins “with extensive coating of the substrate layer 1 with a first electrically conductive layer 3.” Ingle, 19:14-16; *see also id.*, 3:26-30 (the “first electrically conductive layer ... is deposited directly on the substrate layer.”).



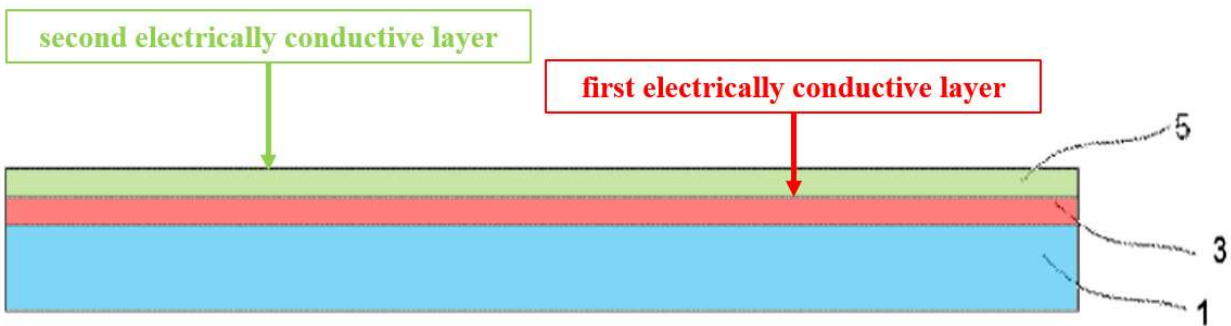
Id., Fig. 1B (annotated). As shown in Figure 1I, the first electrically conductive layer (red) is part of the final base structure on which the rest of the assembly is built.



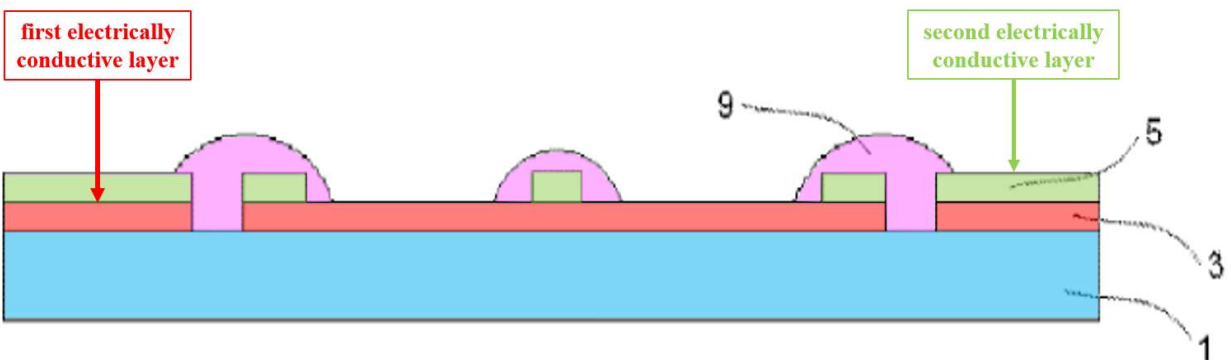
Id., Fig. 1I (annotated). The first electrically conductive layer is therefore part of the final electronic component. Ex.1003, ¶129.

d) Element 10[c]: “a second electrically conductive layer on the first electrically conductive layer,”

Ingle teaches or suggests this element. Ex.1003, ¶¶135-38. As illustrated in Figure 1C, below, Ingle teaches that “the first electrically conductive layer 3 is coated extensively with a second electrically conductive layer 5.” Ingle, 19:29-31.



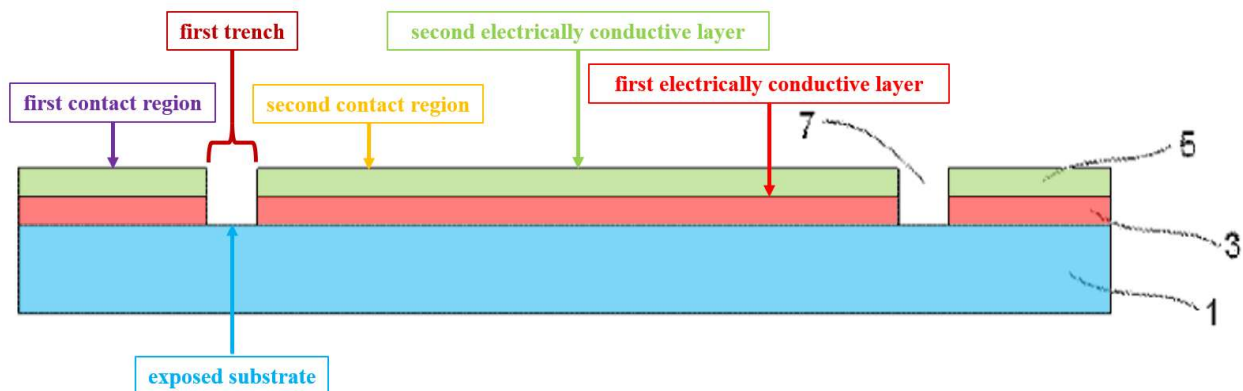
Id., Fig. 1C (annotated). As shown in Figure 1I, the second electrically conductive layer (green) is part of the final base structure on which the rest of the assembly is built. Ex.1003, ¶129.



Id., Fig. 1I (annotated).

- e) **Element 10[d]: “a first trench formed in the first and second electrically conductive layers, wherein the first trench separates a first contact region from a second contact region,”**

Ingle teaches or suggests this element. Ex.1003, ¶¶144-53. Ingle teaches that a “trench” or “gap” is formed in the first and second electrically conductive layers. Ingle, 8:30-9:9. This creates a “separation region” between what Ingle calls the “first electrode region” and the “second electrode region.” *Id.* This “trench” may be formed by laser ablation. *Id.*, 20:2-5. Figure 1D, below, shows that several such trenches may be formed, enabling multiple electronic components to be produced on the same substrate.

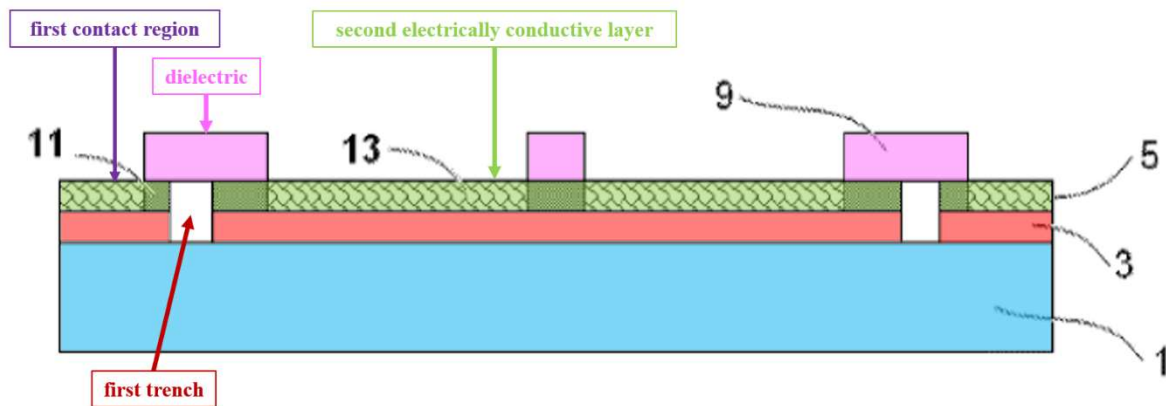


Ingle, Fig. 1D (annotated). Ex.1003, ¶147.

Ingle’s “second electrode region” and “first electrode region” are the claimed “first contact region” and “second contact region,” respectively. Ex.1003, ¶¶148-153.

- f) **Element 10[e]: “a dielectric, which is applied in a structured fashion to the second electrically conductive layer in the first contact region and at least partly on the substrate in the first trench such that the dielectric electrically insulates the first contact region from the second contact region, and”**

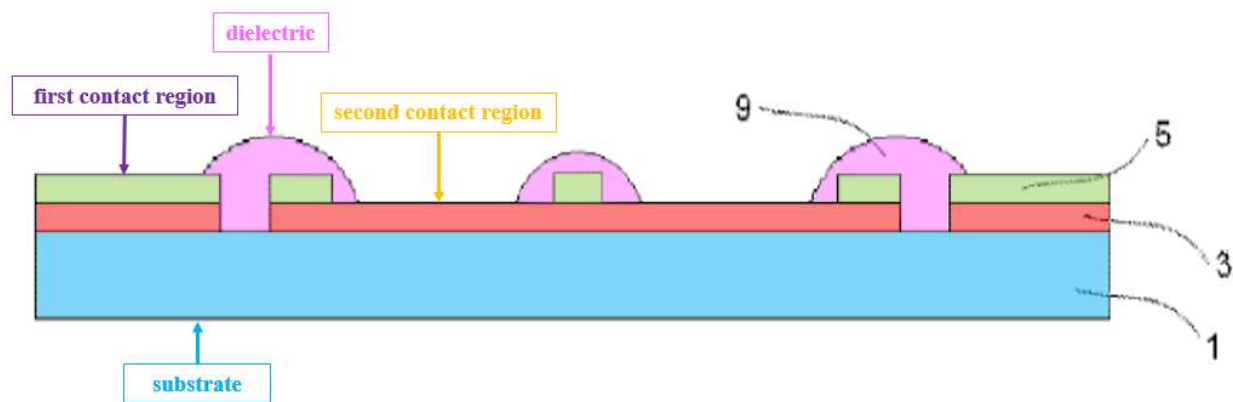
Ingle teaches or suggests this element. Ex.1003, ¶¶154-60. As illustrated in Ingle’s Fig. 1E (reproduced below), Ingle discloses that “an insulator 9 is applied to the second electrically conductive layer 5 in a structured manner.” Ingle, 20:9-11. As shown, the insulator is applied in the first contact region.



Ingle, Fig. 1E (annotated). Ex.1003, ¶155.

Ingle next discloses that its insulator is applied at least partly on the substrate in the first trench. For example, Ingle teaches that “[t]he substrate 1 or the insulator 9 is then heated directly such that the insulator 9 softens (reflow) and flows over the open edges of the second electrically conductive layer 5 and the first electrically conductive layer 3,” as shown in Figure 1I. Ingle, 21:27-30. *See*, Ingle, 20:20-22

(“The insulator 9 should be selected so that it can be softened by subsequent treatment and brought into a flowable state.”); Ex.1003, ¶156. As shown in Figure 1I below, Ingle’s insulator 9 is applied at least partially to the substrate (blue) in the first trench such that it electrically insulates the first contact region from the second contact region. See Ex.1003, ¶157.



Ingle, Fig. 1I (annotated). See Ex.1003, ¶157.

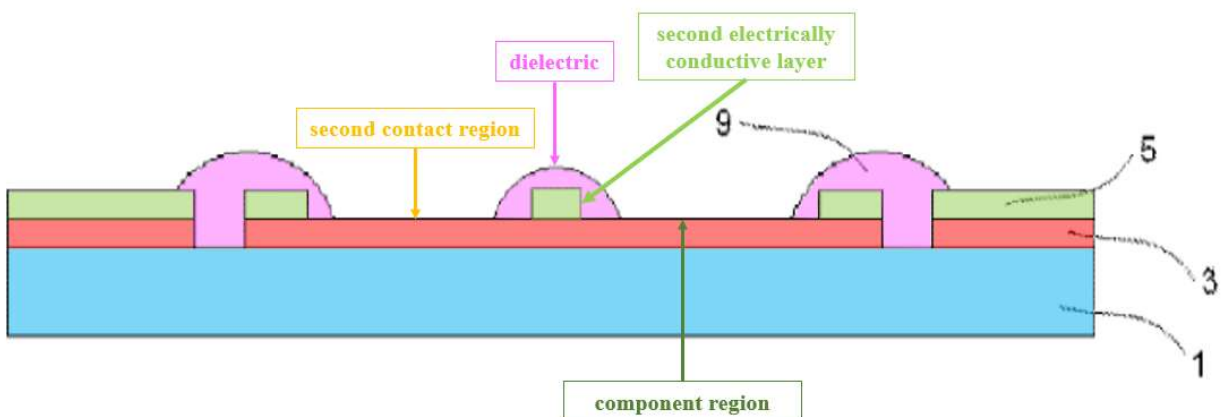
A POSITA would understand that Ingle’s “insulator” is the claimed “dielectric.” Ex.1003, ¶158. For example, Ingle discloses that the “insulator” may be a “coating agent,” such as a “polymer.” Ingle, 3:20-22. The ’492 patent likewise states that “[t]he dielectric can be a covering or a coating agent, for example a polymer and/or a resist.” ’492 patent, 3:16-17. Likewise, Ingle describes an “insulator” as “an insulating substance which is applied in such a way that it prevents a current flow between the first electrode region and the second electrode region.” Ingle, 3:16-19. Using nearly identical language, the ’492 patent describes a “dielectric” as “an electrically insulating substance applied in such a way that it

prevents a current flow between two electrically conductive regions,” ’492 patent, 3:8-10. Accordingly, Ingle teaches selecting an insulator from among the same materials that the ’492 patent contemplates using as a dielectric. *Id.*; *see also* Ex.1003, ¶159-60. Indeed, use of insulating materials as dielectrics was so widespread as of the ’492 patent that publications concerning semiconductor fabrication (*e.g.*, the ’492 patent) used the terms “insulator” and “dielectric” interchangeably. *See, e.g.*, ’492 patent, 3:8-10 (defining “dielectric” as “an electrically insulating substance . . .”); Hanamura, 7:6-9 (“a dielectric layer 15 is formed . . . by printing a pasty **insulating or dielectric material** with the use of a fourth screen 24’.”); *see also* Ex.1003, ¶160.

Accordingly, Ingle at least renders obvious applying a dielectric in a structured fashion to the second electrically conductive layer in the first contact region and at least partially to the substrate in the first trench such that the dielectric electrically insulates the first contact region from the second contact region. *See* Ex.1003, ¶154-60.

- g) **Element 10[g]: “applying the dielectric in a structured fashion to the second layer such that the dielectric demarcates a component region for forming an optoelectronic component relative to the second contact region,”⁴**

Ingle teaches or suggests this element. Ingle discloses applying the dielectric in a structured fashion to the second layer, as discussed in the preceding section. *See supra* §VIII.A.2.f. As shown in Figure 1I, the dielectric (pink) demarcates a component region for forming an optoelectronic component relative to the second contact region. Ex.1003, ¶¶172-73.



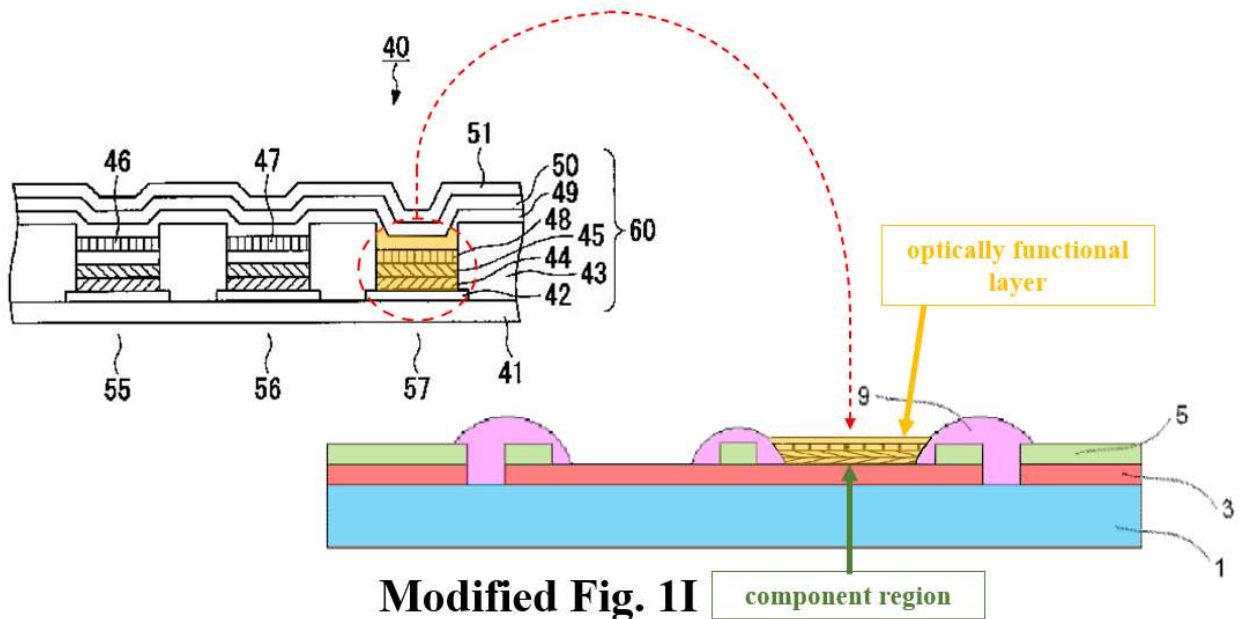
Ingle, Fig. 1I (annotated). *See* Ex.1003, ¶173.

⁴ Claim element 10[g] is directed to the application of the dielectric, whereas claim element 10[f] is directed to an electrode applied in a structured fashion to the dielectric. For ease of review, claim element 10[g] is addressed prior to claim element 10[f].

h) Element 10[h]: “forming an optically functional layer in the component region, and”

This element would have been obvious to a POSITA based on Ingle in view of Hasei. Ex.1003, ¶¶174-80. As explained above, Ingle instructs a POSITA to form a conventional OLED on Ingle’s base structure. *See supra* §VIII.A.1; Ingle, 21:34-22:5 (“conventional process” for forming an OLED on a substrate comprises “vapor-deposit[ing] onto the substrate layer in subsequent processing steps” “the semiconducting, light-emitting organic layers and the second electrode layer, for example a cathode layer.”); *see also* Ex.1003, ¶175. Likewise, Hasei discloses a conventional OLED comprising three pixels (red (55), green (56), and blue (57)) that include “light emitting layers 46, 47, 48 made of organic electroluminescent material,” Hasei, ¶[0032], that “can be formed from ... light emitting materials such as various fluorescent and phosphorescent materials,” Hasei, ¶[0037]. Each of Hasei’s light emitting layers are an optically functional layer. *See* ’492 patent, 4:66-5:3 (“optically functional layers can be for example radiation emitting layers, such as fluorescent and/or phosphorescent emitter layers, for example those of components which emit electromagnetic radiation, for example LEDs or OLEDs.”); Ex.1003, ¶¶176-78.

As explained above and depicted below, it would have been obvious for a POSITA to place Hasei’s OLED, including its optically functional layer, on Ingle’s base structure in the component region. *See* Ex.1003, ¶179.



Hasei, Fig. 3 (upper-left, annotated); Ingle, Fig. 1I (lower-right, annotated, modified); Ex.1003, ¶179. Accordingly, Ingle in view of Hasei renders obvious forming an optically functional layer in the component region. *See* Ex.1003, ¶180.

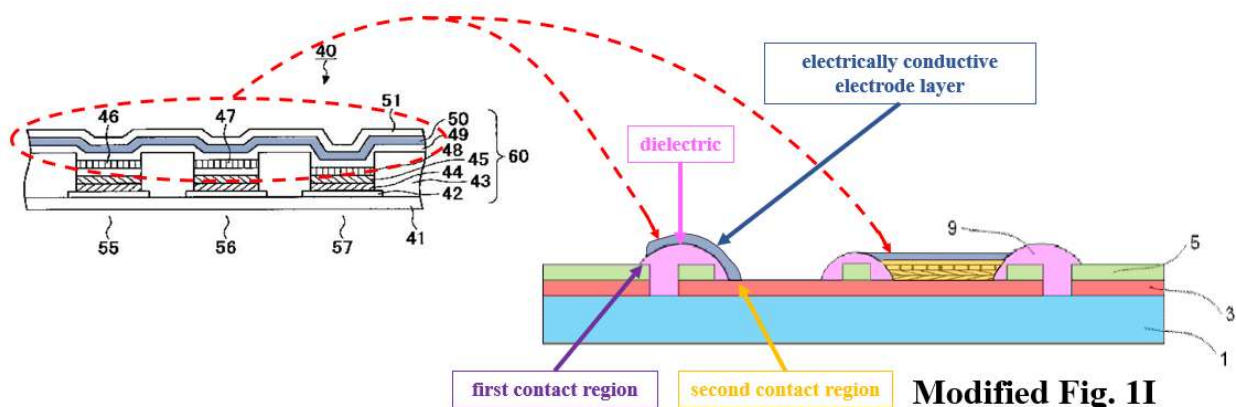
- i) **Element 10[f]: “an electrically conductive electrode layer, which is applied in a structured fashion to the dielectric above the first contact region and to the second contact region,”**

This element would have been obvious to a POSITA based on Ingle in view of Hasei. Ex.1003, ¶¶161-71. As explained above, it would have been obvious for a POSITA to form an electrode above the left-side dielectric in Ingle’s base structure using Hasei’s droplet discharge method to form a capacitor connected to the OLED. *See supra* VIII.A.1; Ex.1003, ¶162. A POSITA would readily understand that Ingle’s capacitor could be completed on Ingle’s base structure by applying an electrode above the dielectric in the first contact region, Ex.1003, ¶162, and Ingle informs the

POSITA to apply the electrode in a structured fashion. *See, e.g.*, Ingle, 7:20-24, 18:7-10; *see also* Ex.1003, ¶162.

Hasei similarly teaches applying the cathode in a structured fashion. In particular, Hasei deposits material using “an inkjet head of a droplet discharging device,” *i.e.*, “inkjet device” (Hasei, ¶15), and so “the electrode material is discharged only onto the portion of the substrate where the conductive pattern is to be formed.” *Id.*, ¶5. Similarly, the ’492 patent contemplates applying materials “in a structured fashion . . . for example by printing, for example inkjet printing.” ’492 patent, 1:66-2:19 (“applying in a structured fashion’ means . . . that the desired structure is already formed during the application of the corresponding layer” and “[t]he area to be coated is thus coated only in partial regions dependent on the desired structure.”); Ex.1003, ¶163-65.

As shown in the figures below, the electrically conductive layer (grey) is applied to the dielectric (pink) above the first contact region and to the second contact region. *See* Ex.1003, ¶166.



Hasei, Fig. 3 (left, annotated); Ingle, Fig. 1I, (right, annotated, modified). *See* Ex.1003, ¶166. A POSITA would understand that the degree to which both the dielectric (pink) and the electrically conductive layer (grey) extend over the first contact region may be adjusted to fine tune the capacitance of the capacitor. *See* Ex.1003, ¶167-70.

Accordingly, Ingle in view of Hasei renders obvious applying an electrically conductive electrode layer in a structured fashion to the dielectric above the first contact region and to the second contact region. *See* Ex.1003, ¶171.

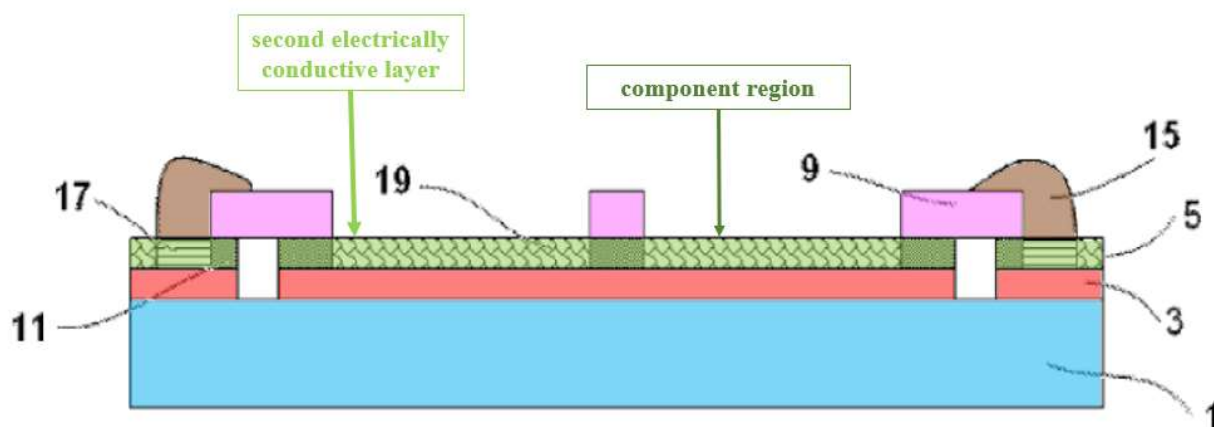
j) Element 10[i]: “applying the electrode layer in a structured fashion such that a part of the electrode layer covers the optically functional layer.”

This element would have been obvious to a POSITA based on Ingle in view of Hasei. Ex.1003, ¶¶181-84. For example, Ingle teaches that an OLED may be produced on a substrate by “vapor-deposit[ing] onto the substrate layer in subsequent processing steps” “the semiconducting, light-emitting organic layers and the second electrode layer, for example a cathode layer.” Ingle, 21:34-22:5; *see also* Ex.1003, ¶182. Further, as explained above, it would have been obvious for a POSITA to apply the electrode layer 50 disclosed in Hasei to Ingle using Hasei’s droplet discharge method, recognizing that this technique applies the electrode in a structured fashion. *See supra* §§VIII.A.2.i, VIII.A.1; Ex.1003, ¶183-84. Accordingly, as shown below, Ingle in view of Hasei discloses applying the



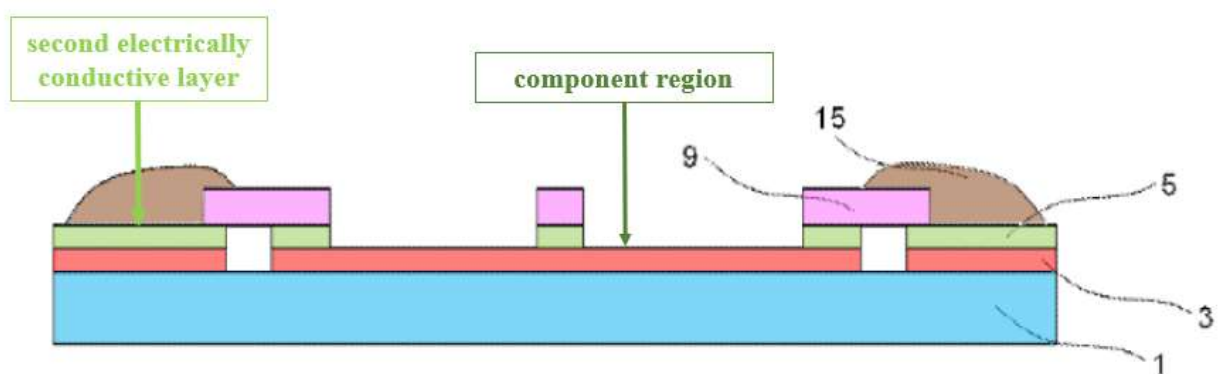
3. Dependent Claim 11: “The method as claimed in claim 10, wherein before the optically functional layer is applied, the second electrically conductive layer is removed in the component region and the optically functional layer is applied to the first electrically conductive layer in the component region.”

39

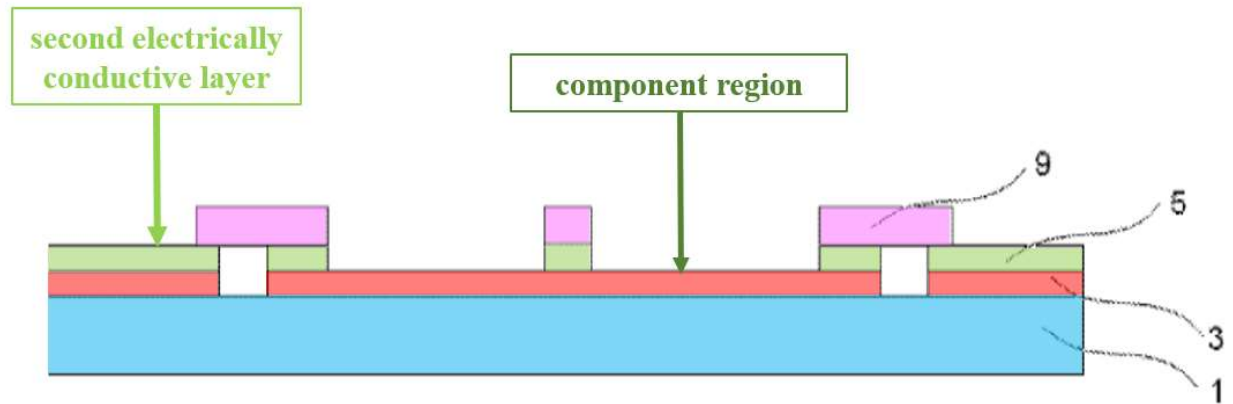


Ingle, Fig. 1F (annotated). *See* Ex.1003, ¶186.

Ingle discloses that “the next step is to remove the second electrically conductive material from the second electrically conductive layer 5,” as shown in Figure 1G. Ingle, 21:14-16.

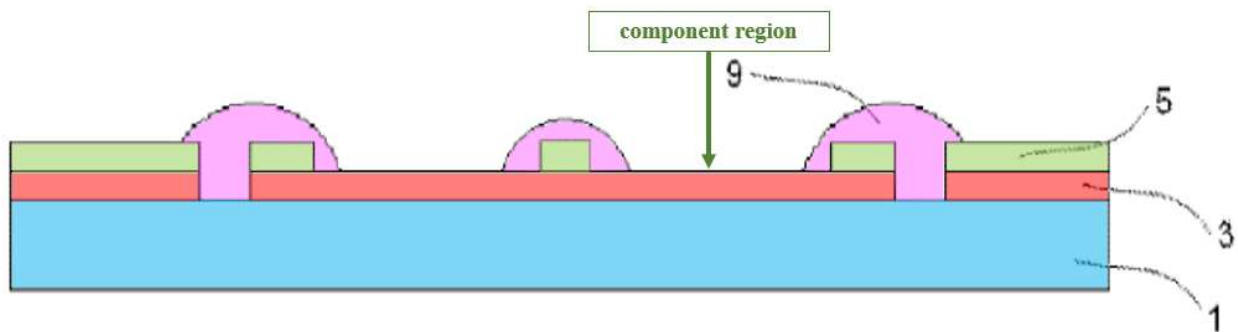


Ingle, Fig. 1G (annotated). *See* Ex.1003, ¶187. Ingle next discloses that “[i]n step I), the protective material 15 ... is removed using a solvent,” as shown in Figure 1H. Ingle, 21:23-25.

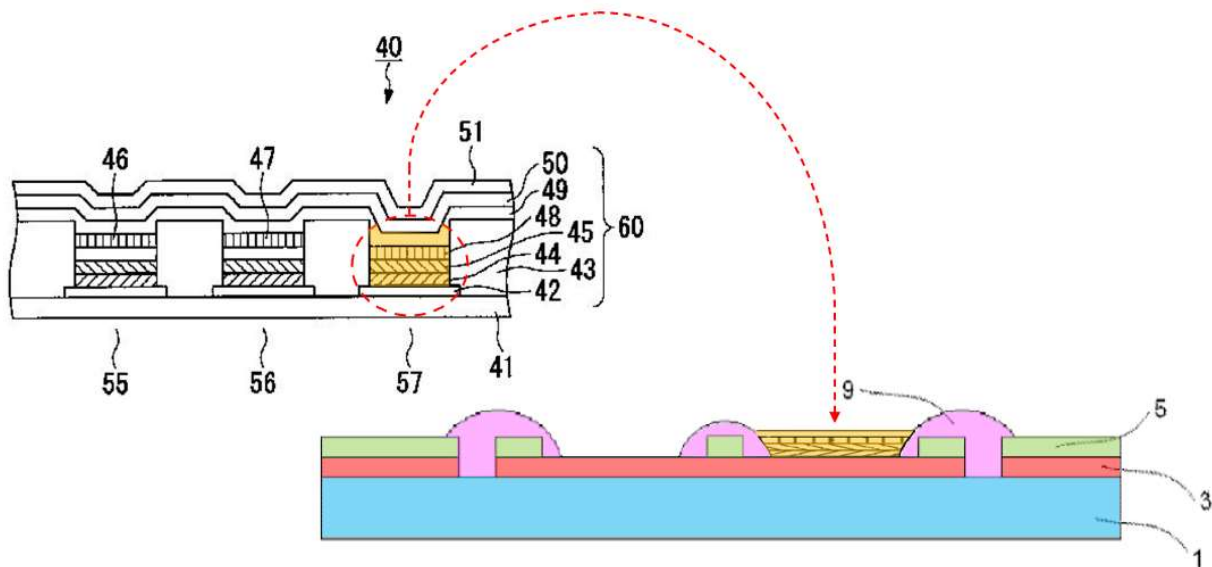


Ingle, Fig. 1H (annotated). *See* Ex.1003, ¶188. Next, Ingle discloses that “the insulator 9 is then heated,” forming the structure shown in Figure 1I. Ingle, 21:27-32. *See supra* §§VIII.A.2.f and VIII.A.2.g.

As shown in Figure 1I, the second electrically conductive layer has been removed in the component region before the optically functional layer has been applied. *See* Ex.1003, ¶¶189-90.



Ingle, Fig. 1I (annotated). *See* Ex.1003, ¶190. As discussed in Section §VIII.A.1, it would have been obvious to then incorporate the OLED from Hasei by applying the optically functional layer to the first electrically conductive layer in the component region, as shown in the modified Figure 1I below. *See* §VIII.A.2.h.



Modified Fig. 1I

Hasei, Fig. 3 (upper-left, annotated); Ingle, Fig. 1I (lower-right, annotated, modified). *See* Ex.1003, ¶191.

Accordingly, as shown in Figures 1F through 1I, Ingle in view of Hasei renders obvious that before the optically functional layer is applied, the second electrically conductive layer is removed in the component region and the optically functional layer is applied to the first electrically conductive layer in the component region. *See* Ex.1003, ¶192.

4. Independent Claim 1

As evident from the below, Claim 1 of the '492 patent is directed to a subset of the method of Claim 10. Accordingly, the below discussion largely references arguments presented in Section VIII.A.2.

a) Element 1[Pre]: “A method for producing a passive electronic component, comprising:”

To the extent the preamble is limiting, Ingle teaches or suggests it for the same reasons described with respect to element 10[a] above. *See supra* §VIII.A.2.b; *see also* Ex.1003, ¶193.

b) Element 1[a]: “forming a first electrically conductive layer on a substrate,”

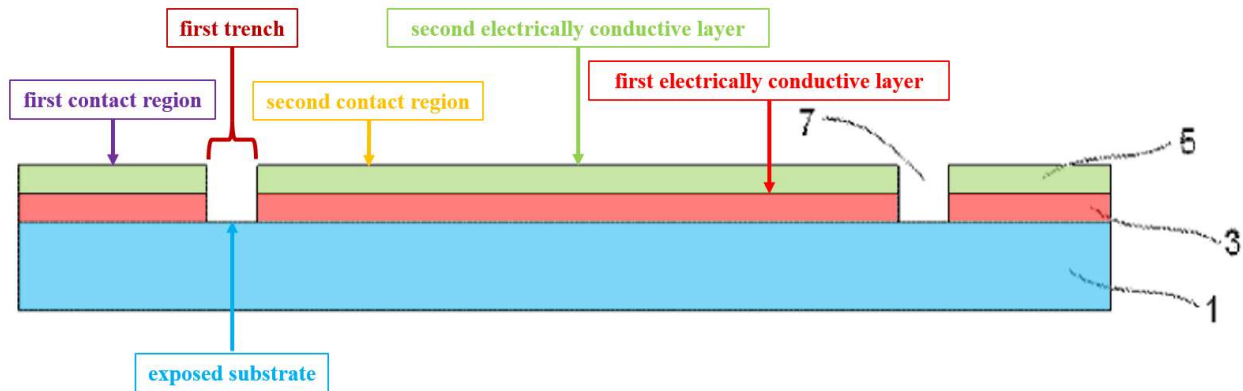
Ingle teaches or suggests this element for the same reasons described with respect to element 10[b] above. *See supra* §VIII.A.2.c; *see also* Ex.1003, ¶194.

c) Element 1[b]: “forming a second electrically conductive layer on the first electrically conductive layer,”

Ingle teaches or suggests this element for the same reasons described with respect to element 10[c] above. *See supra* §VIII.A.2.d; *see also* Ex.1003, ¶195.

d) Element 1[c]: “forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region,”

Ingle teaches or suggests this element for the same reasons described with respect to element 10[d] above. *See supra* §VIII.A.2.e; *see also* Ex.1003, ¶196. As shown in Ingle’s Fig. 1D (reproduced below), Ingle’s first trench is formed through laser ablation and the substrate is exposed in the trench. Ingle, 20:2-5; *see also* Ex.1003, ¶196.



Ingle, Fig. 1D (annotated). Ex.1003, ¶196.

- e) **Element 1[d]: “applying a dielectric in a structured fashion to the second electrically conductive layer in the first contact region and at least partly to the substrate in the first trench such that the dielectric electrically insulates the first contact region from the second contact region, and”**

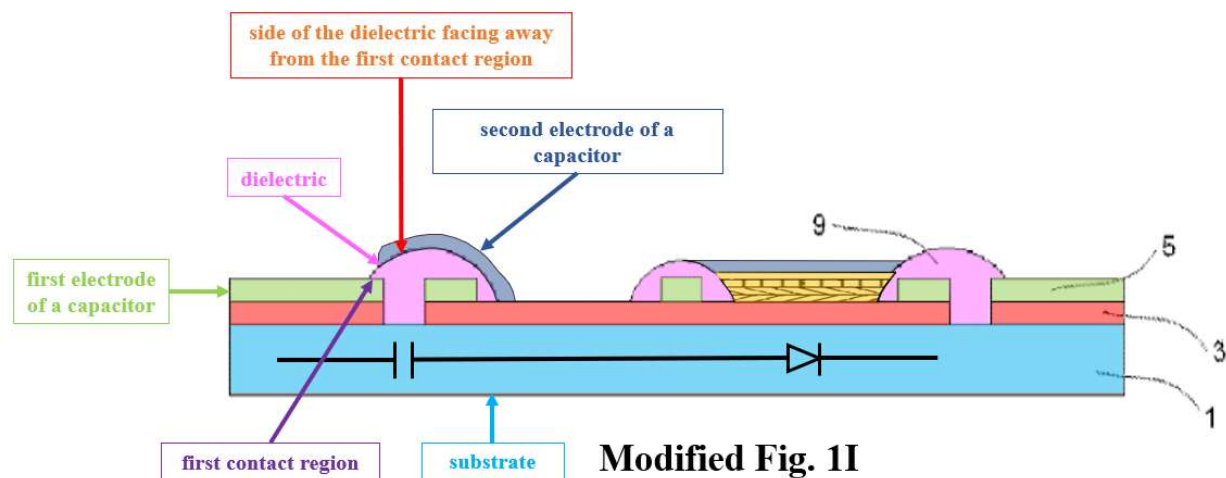
Ingle teaches or suggests this element for the same reasons described with respect to element 10[e] above. *See supra* §VIII.A.2.f; *see also* Ex.1003, ¶197.

- f) **Element 1[e]: “applying an electrically conductive electrode layer in a structured fashion to the dielectric above the first contact region and to the second contact region.”**

This element would have been obvious based on Ingle in view of Hasei for the same reasons described with respect to element 10[f] above. *See supra* §VIII.A.2.i; *see also* Ex.1003, ¶198.

5. **Dependent Claim 2: “The method as claimed in claim 1, wherein a first electrode of a capacitor is formed by the first contact region between the dielectric and the substrate and a second electrode of a capacitor is formed by the electrode layer on a side of the dielectric facing away from the first contact region.”**

Claim 2 would have been obvious based on Ingle in view of Hasei. Ex.1003, ¶¶199-202. As explained above, it would have been obvious for a POSITA to form an electrode above the left-side dielectric in Ingle’s base structure using Hasei’s droplet discharge method, or Ingle’s vapor-deposition method, in order to form a capacitor in series with the OLED. *See supra* VIII.A.1; Ex.1003, ¶200. As shown below, Ingle in view of Hasei discloses that a first electrode of a capacitor (green) is formed by the first contact region between the dielectric (pink) and the substrate (blue) and a second electrode of a capacitor (grey) is formed by the electrode layer on a side of the dielectric facing away from the first contact region. *See* Ex.1003, ¶¶200-01.



Ingle, Fig. 1I, (annotated, modified). *See* Ex.1003, ¶201.

6. Dependent Claim 8: “The method as claimed in claim 1, wherein the dielectric is applied by a printing method.”

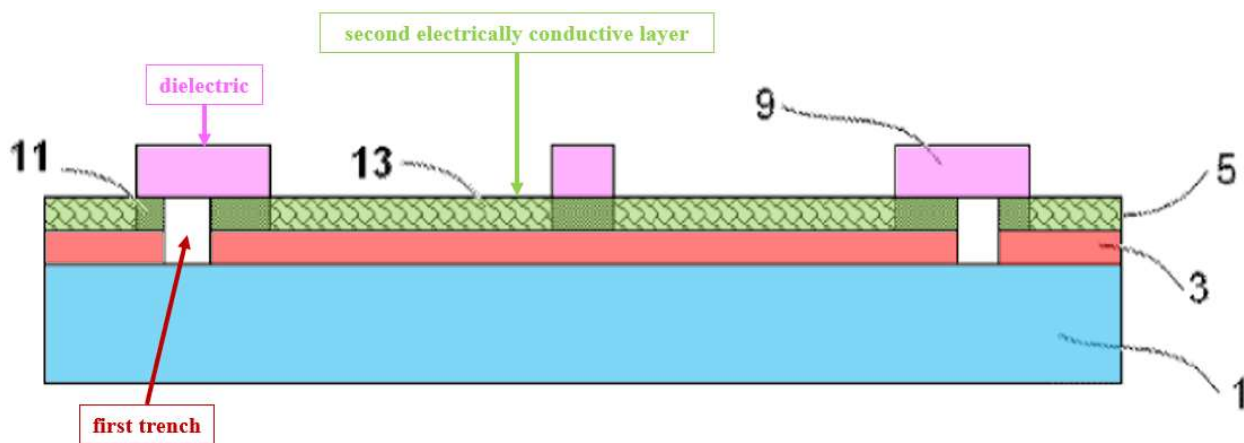
Claim 8 would have been obvious to a POSITA based on Ingle in view of Hasei. Ex. 1003, ¶¶203-05.

Ingle discloses that its insulator 9 “may be applied ... by means of a printing process, such as screen printing, inkjet printing, or flexographic printing.” Ingle, 20:17-20. A POSITA would recognize screen printing, inkjet printing, or flexographic printing as printing methods. *See* Ex.1003, ¶204; *see also* ’492 patent, 4:10-15 (“In various embodiments, the dielectric is applied by a printing method.... The printing method may include for example inkjet printing or screen printing”). Further, as discussed (*supra* §VIII.A.2.f; Ex.1003, ¶¶154-60), the POSITA would recognize Ingle’s insulator 9 as the ’492 patent’s claimed dielectric. Accordingly, Ingle renders obvious that the dielectric is applied by a printing method. *See* Ex.1003, ¶¶203-05.

7. Dependent Claim 9: “The method as claimed in claim 1, wherein the dielectric firstly is applied in a structured fashion to the second electrically conductive layer in such a way that it adjoins the first trench, and wherein then the dielectric is heated in such a way that it deforms and encapsulates edges and/or side surfaces of the first and second electrically conductive layers in the first trench.”

Claim 9 would have been obvious to a POSITA based on Ingle in view of Hasei. Ex.1003, ¶¶206-11.

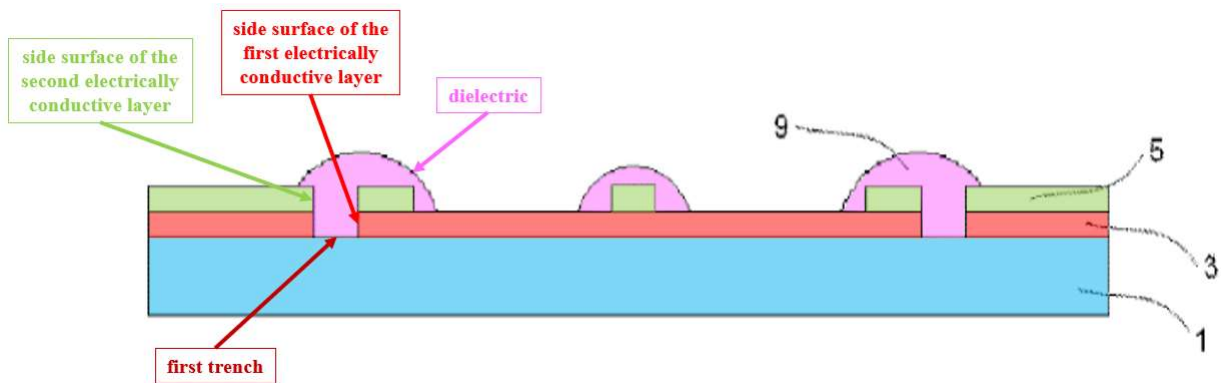
Ingle discloses applying a dielectric in a structured fashion to the second electrically conductive layer and adjoining the first trench. For example, Ingle discloses that “insulator 9 is applied to the second electrically conductive layer 5 in a structured manner,” as shown in Figure 1E. Ingle, 20:9-11. *See supra* §VIII.A.2.f). A POSITA would recognize Ingle’s insulator 9 as a dielectric. *See, e.g., supra* §VIII.A.2.f; Ex.1003, ¶207-08.



Ingle, Fig. 1E (annotated). *See* Ex.1003, 208. Further, as shown in Figure 1E above, the insulator 9 (pink) “adjoins the first trench.” *See* Ex.1003, ¶209; ’492 patent, 4:25-28.

Ingle discloses heating the dielectric so that it deforms and encapsulates edges / side surfaces of the first and second electrically conductive layers in the first trench. For example, Ingle discloses that “[t]he substrate 1 or the insulator 9 is then heated directly such that the insulator 9 softens (reflow) and flows over the open edges of the second electrically conductive layer 5 and the first electrically conductive layer

3,” as shown in Figure 1I. Ingle, 21:27-30; *see, id.*, 20:20-22 (“The insulator 9 should be selected so that it can be softened by subsequent treatment and brought into a flowable state.”); Ex.1003, ¶210. As shown in Figure 1I below, the dielectric (pink) encapsulates edges and/or side surfaces of the first and second electrically conductive layers (red and green, respectively) in the first trench.



Ingle, Fig. 1I (annotated). *See* Ex.1003, ¶210.

8. Independent Claim 16

Claim 16 of the '492 patent is directed to a passive electronic component that may be formed using the method of Claim 1, which in turn is directed to a subset of the method of Claim 10. Accordingly, the below discussion largely references arguments presented in Section VIII.A.2.

a) Element 16[Pre]: “A passive electronic component, comprising:”

To the extent the preamble is limiting, Ingle teaches or suggests it for the same reasons described with respect to element 10[a] above. *See supra* §VIII.A.2.b; Ex.1003, ¶212.

- b) **Element 16[a]: “a first electrically conductive layer on a substrate,”**

Ingle teaches or suggests this element for the same reasons described with respect to element 10[b] above. *See supra* §VIII.A.2.c; Ex.1003, ¶213.

- c) **Element 16[b]: “a second electrically conductive layer on the first electrically conductive layer,”**

Ingle teaches or suggests this element for the same reasons described with respect to element 10[c] above. *See supra* §VIII.A.2.d; Ex.1003, ¶214.

- d) **Element 16[c]: “a first trench in the first and second electrically conductive layers, wherein the first trench separates a first contact region from a second contact region,”**

Ingle teaches or suggests this element for the same reasons described with respect to element 10[d] above. *See supra* §VIII.A.2.e; Ex.1003, ¶215.

- e) **Element 16[d]: “a dielectric, which is applied in a structured fashion on the second electrically conductive layer in the first contact region and at least partly on the substrate in the first trench such that said dielectric electrically insulates the first contact region from the second contact region, and”**

Ingle teaches or suggests this element for the same reasons described with respect to element 10[e] above. *See supra* §VIII.A.2.f; Ex.1003, ¶216.

- f) Element 16[e]: “an electrically conductive electrode layer, which is applied in a structured fashion on the dielectric above the first contact region and at least partly on the second contact region.”**

Ingle in view of Hasei teaches or suggests this element for the same reasons described with respect to element 10[f] above. *See supra* §VIII.A.2.i; Ex.1003, ¶217. Applying the electrode “to the second contact region” (as in element 10[f]) satisfies the requirement in element 16[e] that the electrode be applied “at least partly on the second contact region.” Ex.1003, ¶217.

B. Ground II: Claims 1, 2, 8, and 16 Are Obvious Based on Hanamura

Hanamura discloses a chip type thick film capacitor, illustrated in its Figure 1, and a method of making the same. Hanamura teaches or suggests all elements of claims 1, 2, 6, 8, and 16 of the '492 patent, as discussed below. *See also* Ex.1003, ¶218.

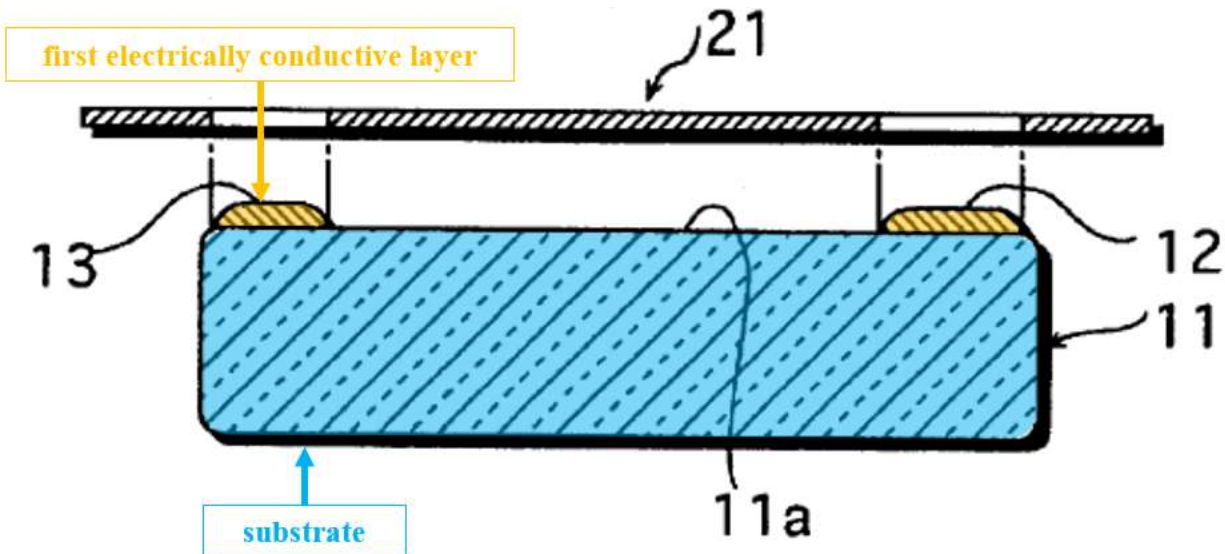
1. Independent Claim 1

- a) Element 1[pre]: “A method for producing a passive electronic component, comprising:”**

To the extent the preamble is limiting, Hanamura teaches or suggests it. Ex.1003, ¶¶219-22. Hanamura discloses a “method of advantageously making a chip type thick film capacitor.” Hanamura, 1:8-12. *See id.*, 5:23-24 (“The chip type capacitor according to the first embodiment may be manufactured in the following manner.”). A capacitor is a passive electronic component. Ex.1003, ¶220-22; *see also* '492 patent, 2:20-23.

b) Element 1[a]: “forming a first electrically conductive layer on a substrate,”

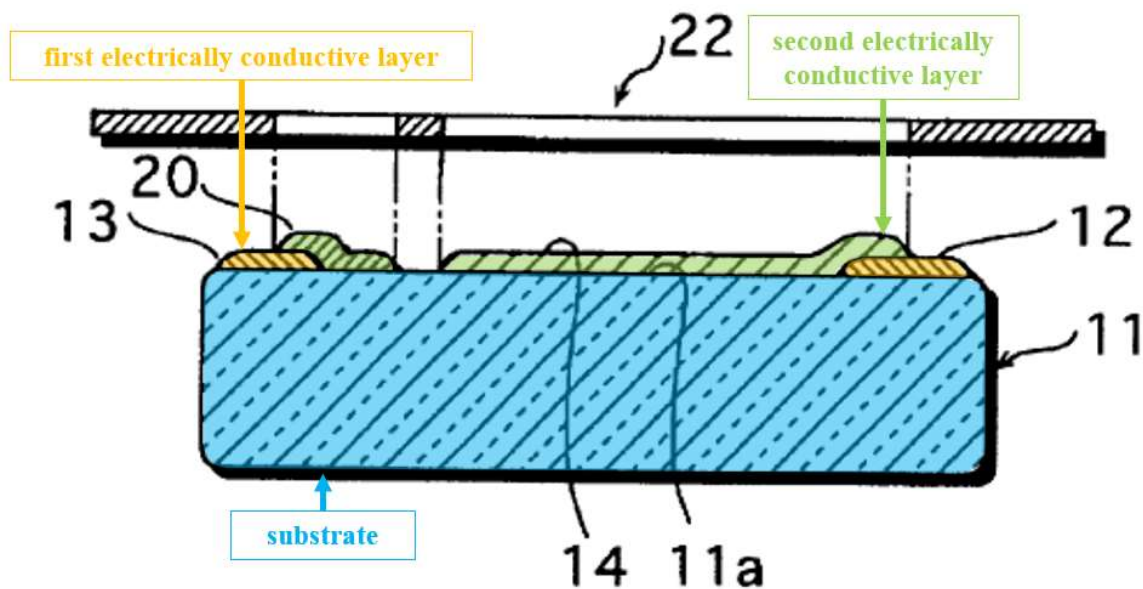
Hanamura teaches or suggests this element. Ex.1003, ¶¶223-28. Hanamura discloses “a first lead electrode 12 and a second lead electrode 13 are formed simultaneously on the head surface 11a of an insulating chip 11 by printing an electrically conductive paste,” as shown in Figure 3. Hanamura, 5:25-28. A POSITA would recognize Hanamura’s electrodes 12 and 13, deposited simultaneously, as the ’492 patent’s claimed “first electrically conductive layer.” Ex.1003, ¶224. The “insulating chip 11” in Hanamura “serv[es] as a substrate.” Hanamura, 2:45-48. Ex.1003, ¶225-26. Accordingly, as shown in Figure 3, Hanamura’s First Embodiment discloses forming a first electrically conductive layer (yellow) on a substrate (blue). See Ex.1003, ¶226-27.



Hanamura, Fig. 3. See Ex.1003, ¶227.

c) Element 1[b]: “forming a second electrically conductive layer on the first electrically conductive layer,”

Hanamura teaches or suggests this element. Ex.1003, ¶¶229-31. Hanamura discloses that “a first capacitor electrode 14 and an auxiliary electrode 20 are formed simultaneously on the head surface 11a of the chip 11 by printing an electrically conductive paste,” as shown in Hanamura’s Figure 4 (reproduced below). Hanamura, 5:29-32. As depicted, the second electrically conductive layer (electrodes 14 and 20, both shown in green) is formed on the first electrically conductive layer (electrodes 12 and 13, both shown in yellow). *See also id.*, 4:56-57 (the “first capacitor electrode 14 [is] partially overlapping the first lead electrode 12”). Accordingly, Hanamura discloses forming a second electrically conductive layer (green) on the first electrically conductive layer (yellow). *See* Ex.1003, ¶230.

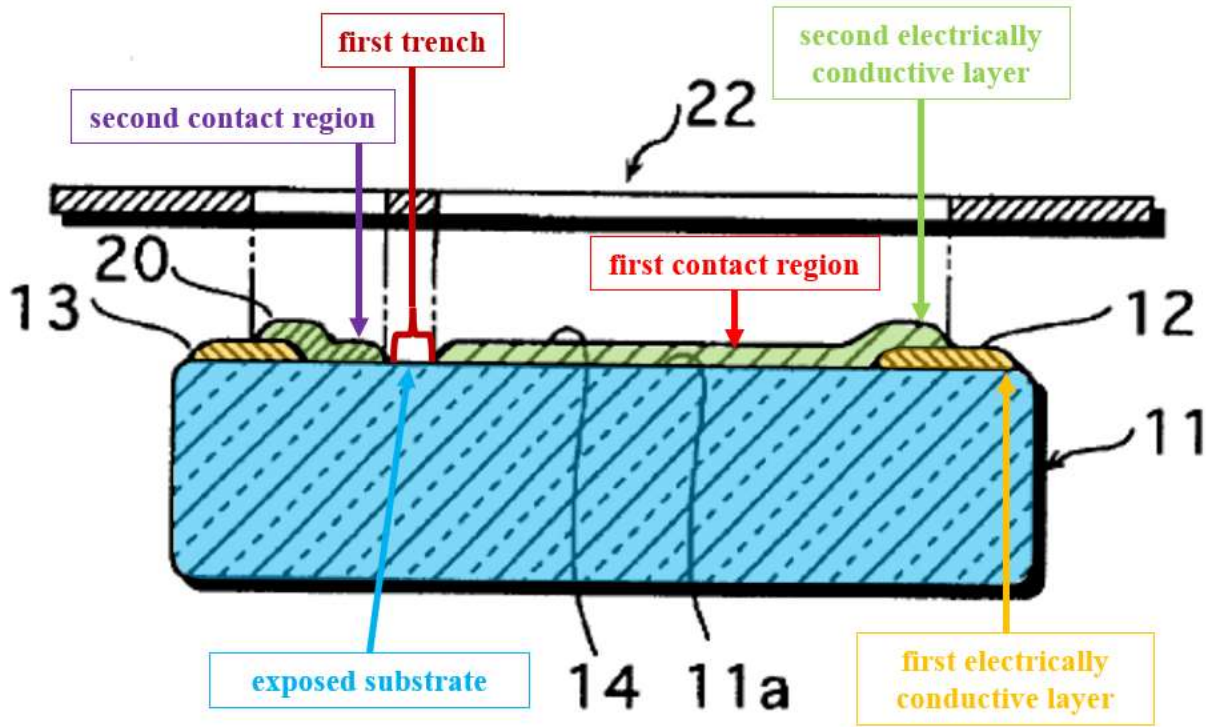


Hanamura, Figure 4. *See* Ex.1003, ¶230.

- d) **Element 1[c]: “forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region,”**

Hanamura teaches or suggests this element. Ex.1003, ¶¶232-35. Hanamura discloses a first trench. For example, Hanamura teaches that the “first capacitor electrode 14 and the auxiliary electrode 20 are formed simultaneously on the head surface 11a of the chip 11 by using the second screen 22, as shown in FIG. 4.” Hanamura, 5:52-55; Ex.1003, ¶233. By doing so, a “predetermined spacing D1 is reliably provided between the first capacitor electrode 14 and the auxiliary electrode 20 even if the second screen 22 positionally deviates slightly relative to the previously formed lead electrodes 12, 13.” Hanamura, 5:55-59; Ex. 1003, ¶233.

As shown in Figure 4 (reproduced below), using Hanamura’s method, a first trench (dark red brackets) is formed in the first and second electrically conductive layers (yellow and green, respectively) such that the substrate (blue) is exposed in the first trench, and wherein the first trench separates a first contact region (red label) from a second contact region (purple label). *See* Ex.1003, ¶234.

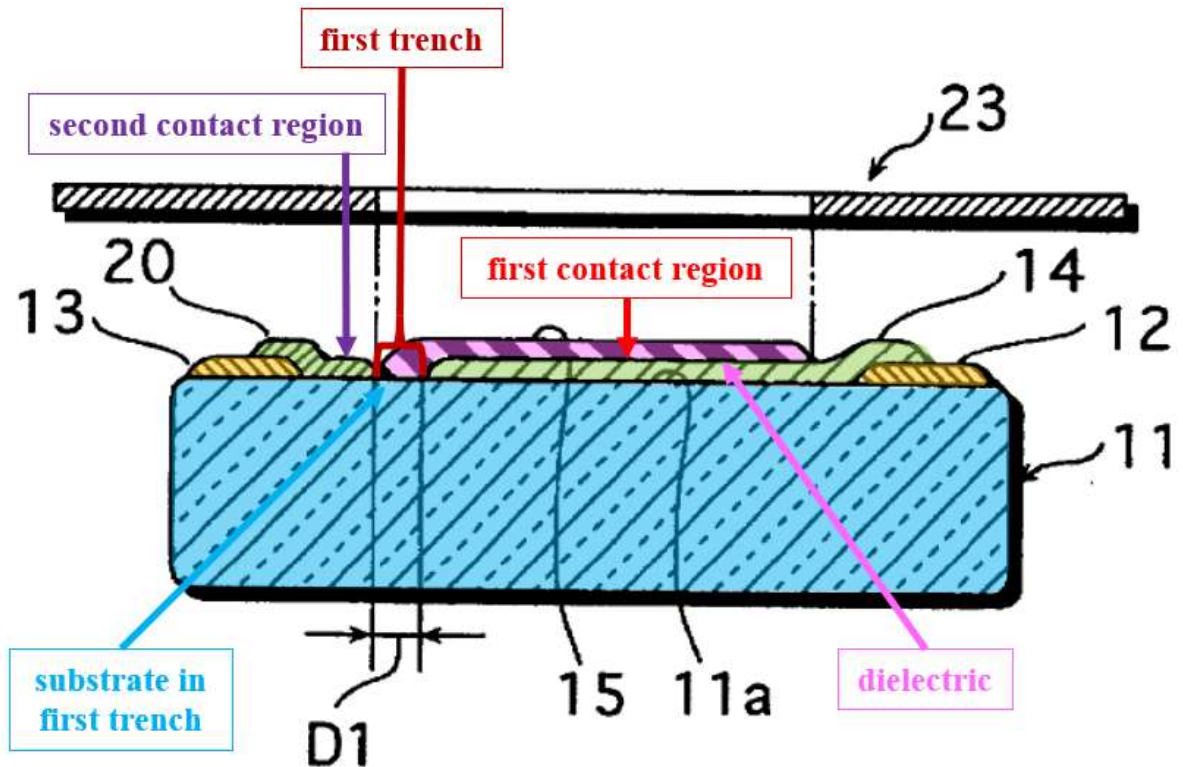


Hanamura, Fig. 4. *See* Ex.1003 ¶234.

- e) **Element 1[d]: “applying a dielectric in a structured fashion to the second electrically conductive layer in the first contact region and at least partly to the substrate in the first trench such that the dielectric electrically insulates the first contact region from the second contact region, and”**

Hanamura teaches or suggests this element. Ex. 1003, ¶¶236-40. Hanamura discloses that “a dielectric layer 15 is formed on the first capacitor electrode 14 by printing a pasty insulating or dielectric material with use of a third screen 23,” as shown in Figure 5 (reproduced below). Hanamura, 5:33-36. Hanamura’s dielectric layer 15 is thus applied in a structured fashion, *i.e.*, screen printing. *See* Ex.1003, ¶237-39. Further, as shown in Figure 5, the dielectric layer 15 (pink) is applied to

the second electrically conductive layer (green) in the first contact region and at least partly to the substrate (blue) in the first trench such that the dielectric electrically insulates the first contact region from the second contact region. *See* Ex.1003, ¶239.

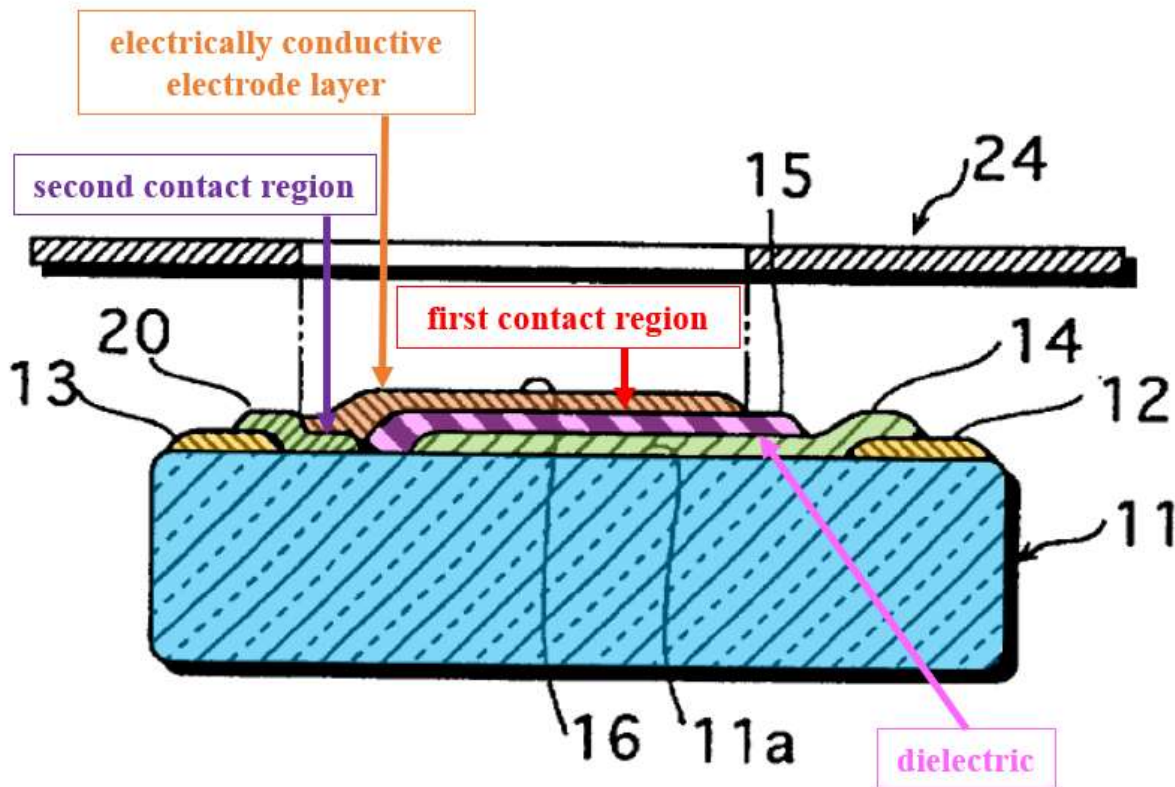


Hanamura, Fig. 5 (annotated). *See* Ex.1003, ¶239.

- f) **Element 1[e]: “applying an electrically conductive electrode layer in a structured fashion to the dielectric above the first contact region and to the second contact region.”**

Hanamura teaches or suggests this element. Ex.1003, ¶¶241-44. Hanamura discloses that “a second capacitor electrode 16 is formed on the dielectric layer 15 by printing an electrically conductive paste with the use of a fourth screen 24,” as shown in Hanamura’s Figure 6 (reproduced below). Hanamura, 5:37-39; *see also*

Ex.1003, ¶242. Hanamura's second capacitor electrode 16 is thus applied in a structured fashion, *i.e.*, screen printing. *See* Ex.1003, ¶243 As shown in Figure 6, the capacitor electrode 16 is applied to the dielectric above the first contact region (red label) and to the second contact region (purple label). *See* Ex.1003, ¶243.

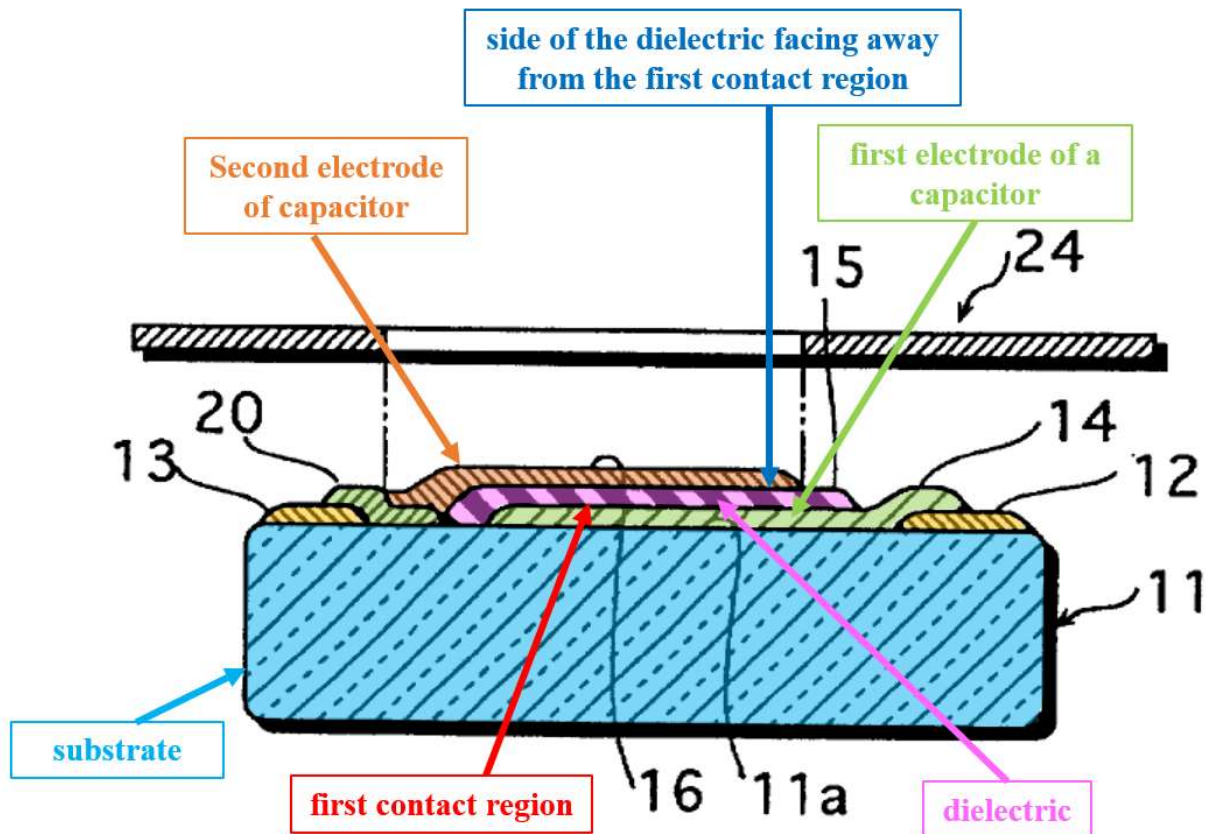


Hanamura, Fig. 6 (annotated). *See* Ex.1003, ¶243.

2. **Dependent Claim 2:** “The method as claimed in claim 1, wherein a first electrode of a capacitor is formed by the first contact region between the dielectric and the substrate and a second electrode of a capacitor is formed by the electrode layer on a side of the dielectric facing away from the first contact region.”

Hanamura teaches or suggests this claim. Ex.1003, ¶¶245-48. Hanamura discloses that “a first capacitor electrode 14” is “formed ... on the head surface 11a,”

and that “a dielectric layer 15 is formed on the first capacitor electrode 14,” and that “a second capacitor electrode 16 is formed on the dielectric layer 15,” as shown in Hanamura’s Figures 4-6. Hanamura, 5:29-40. Ex. 1003, ¶246. Accordingly, as shown in Figure 6 (reproduced below), Hanamura at least renders obvious that a first electrode of a capacitor (green) is formed by the first contact region between the dielectric (pink) and the substrate (light blue) and a second electrode of a capacitor (orange) is formed by the electrode layer on a side of the dielectric facing away from the first contact region. See Ex.1003, ¶247.



Hanamura, Fig. 1 (annotated). See Ex.1003, ¶247.

3. Dependent Claim 8: “The method as claimed in claim 1, wherein the dielectric is applied by a printing method.”

Hanamura teaches or suggests this claim. Ex.1003, ¶¶249-50. Hanamura discloses that the “dielectric layer 15 is formed on the first capacitor 14 by printing a pasty insulating or dielectric material with the use of a third screen.” Hanamura, 5:33-36. *See* Ex.1003, ¶249-50.

4. Independent Claim 16

a) Element 16[Pre]: “A passive electronic component, comprising:”

To the extent the preamble is limiting, Hanamura teaches or suggests it for the same reasons described with respect to element 1[pre] above. *See supra* §VIII.B.1.a); Ex.1003, ¶251.

b) Element 16[a]: “a first electrically conductive layer on a substrate,”

Hanamura teaches or suggests this element for the same reasons described with respect to element 1[a] above. *See supra* §VIII.B.1.b); Ex.1003, ¶252.

c) Element 16[b]: “a second electrically conductive layer on the first electrically conductive layer,”

Hanamura teaches or suggests this element for the same reasons described with respect to element 1[b] above. *See supra* §VIII.B.1.c); Ex.1003, ¶253.

- d) **Element 16[c]: “a first trench in the first and second electrically conductive layers, wherein the first trench separates a first contact region from a second contact region,”**

Hanamura teaches or suggests this element for the same reasons described with respect to element 1[c] above. *See supra* §VIII.B.1.d); Ex.1003, ¶254.

- e) **Element 16[d]: “a dielectric, which is applied in a structured fashion on the second electrically conductive layer in the first contact region and at least partly on the substrate in the first trench such that said dielectric electrically insulates the first contact region from the second contact region, and”**

Hanamura teaches or suggests this element for the same reasons described with respect to element 1[d] above. *See supra* §VIII.B.1.e); Ex.1003, ¶255.

- f) **Element 16[e]: “an electrically conductive electrode layer, which is applied in a structured fashion on the dielectric above the first contact region and at least partly on the second contact region.”**

Hanamura teaches or suggests this element for the same reasons described with respect to element 1[e] above. *See supra* §VIII.B.1.f). Applying the electrode “to the second contact region” (as in element 1[e]) satisfies the requirement in element 16[e] that the electrode be applied “at least partly on the second contact region.” Ex.1003, ¶256.

C. Ground III: Claims 3, 5, and 6 Are Obvious Based on Hanamura in view of Egitto

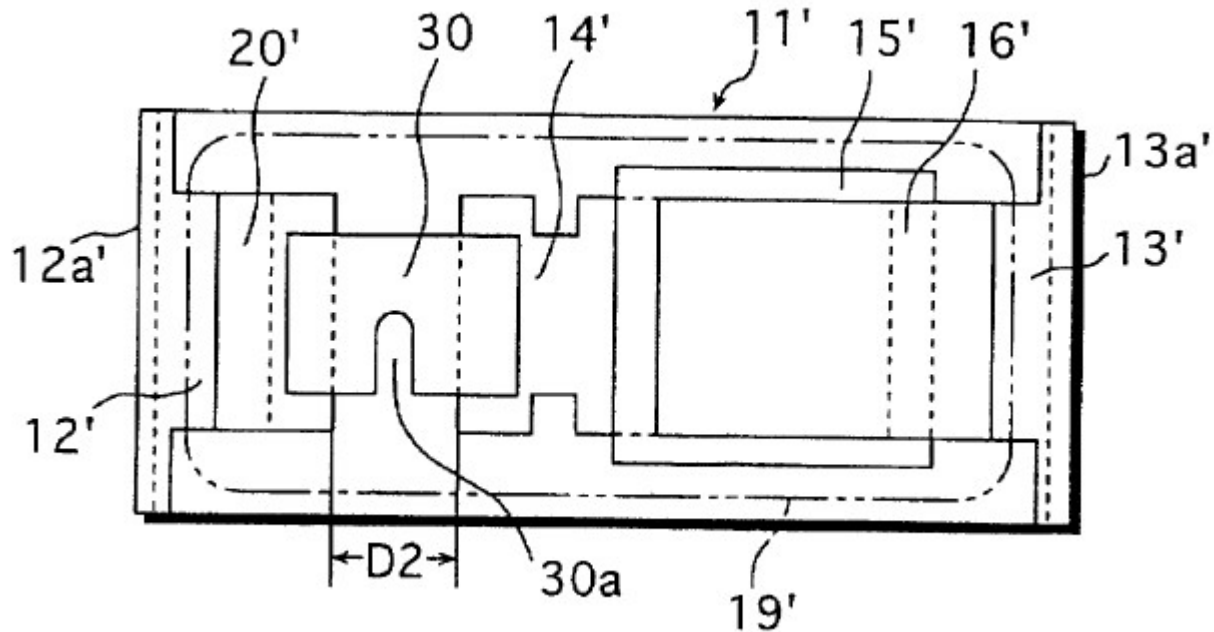
The '492 patent's dependent claims 3, 5, and 6 require a resistor (or resistance region) with certain characteristics. *See* '492 patent, cls. 3, 5, 6. As detailed below, Hanamura in view of Egitto renders obvious these dependent claims.

- 1. Dependent Claim 3: “The method as claimed in claim 1, wherein before the dielectric is applied, a second trench and at least one third trench are formed, which delimit a resistance region, which comprises a part of the first and second electrically conductive layers and which has a taper in a direction parallel to the electrically conductive layers and which leads into the first contact region on a first side of the taper.**

Claim 3 would have been obvious to a POSITA based on Hanamura in view of Egitto. Ex.1003, ¶¶273-80.

As discussed above, the first embodiment of Hanamura renders obvious the method of claim 1 for producing a passive electronic component, *e.g.*, a capacitor. Hanamura in view of Egitto renders obvious the claimed second and third trench that delimit a resistance region. For example, Hanamura discloses that “[a]nother object of [its] present invention is to provide a chip type thick film capacitor which additionally incorporates a resistor having a reliably adjusted resistance.” Hanamura, 2:39-40; Ex.1003, ¶257. Hanamura provides an example of such a structure in its second embodiment. Hanamura, 5:63-7:39. Hanamura teaches that the resistance of the device can be “reliably adjusted” by adjusting the dimensions of a resistor layer

30, *id.*, 6:50-58, as well as by trimming a groove 30a to change the overall shape of the layer, *id.*, 7:34-39, as shown in Figure 8 below.



Hanamura, Fig. 8. *See* Ex.1003, ¶¶257-60.

A POSITA would have been motivated to add a resistor to Hanamura's first embodiment because Hanamura teaches that the resistor can "control the rate of electric charging and discharging of the capacitor." Hanamura, 6:55-58. A POSITA would recognize that such a resistor could be created by incorporating a resistor layer to Hanamura's first embodiment, or alternatively, by forming trenches in the first and second electrically conductive layers already present in the embodiment. *See* Ex.1003, ¶261. A POSITA would recognize that the latter approach would save at least one manufacturing step, as there would be no need to deposit a separate layer as is shown in Figure 11. *See* Ex.1003, ¶262.

Doing so would have been nothing more than applying a known technique to improve a similar device in the same way to obtain predictable results. *KSR*, 550 U.S. at 401; Ex. 1003, ¶263. POSITAs have understood since at least 1975 that a resistor can be formed “in series with [a] capacitor ... by etching away” electrode layers connected to the capacitor. *See, e.g.*, Ex.1016 (U.S. Patent No. 3,997,411 (“Muenz”)), 4:39-52; Ex.1003, ¶¶263-64. For example, Muenz describes a method for the production of a thin film electric circuit having a conductor path and at least one capacitor and/or one resistor. *See* Ex.1016, Abstract. As shown in Figure 11 below, Muenz describes a similar configuration to that of the ’492 patent, wherein a capacitor is built over the side of a trench formed between two contact regions (the tantalum-aluminum layers 2’, 3 form one electrode of the capacitor, while the nickel-chromium-gold layer 9, 10 form the opposite electrode). *See, e.g.*, Ex.1016, 4:30-34; *see also* Ex.1003, ¶265. As shown in Figure 12, Muenz describes two resistors, R1 and R2, in series with a capacitor, C. Resistor R1 “merges directly into the layer[] 2,” the electrically conductive tantalum-aluminum layer connected to the electrode of the capacitor C1. *Id.*, 4:53-65.

Fig. 11

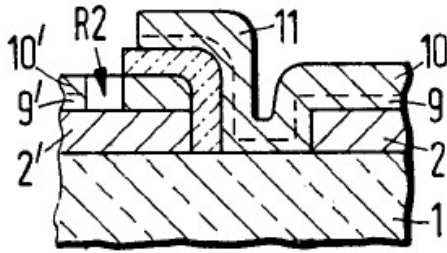
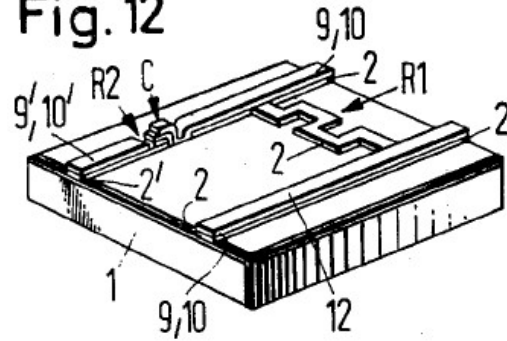


Fig. 12

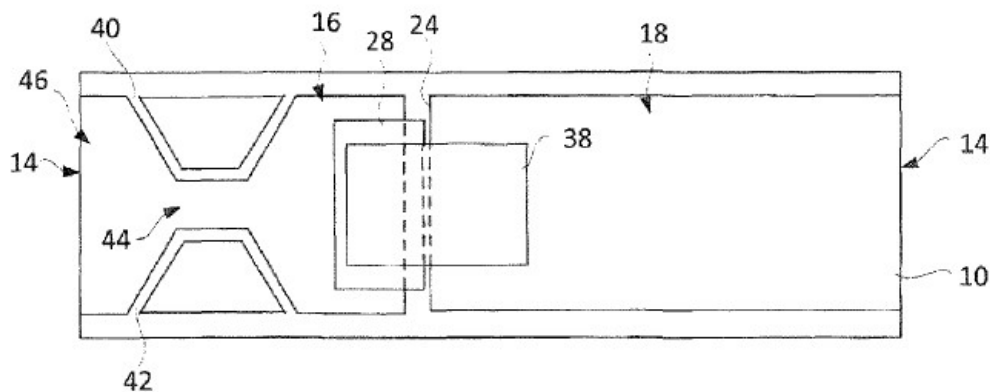


Muenz, Figs. 11, 12; Ex.1003, ¶265.

A POSITA would have had a reasonable expectation of success in forming a resistor in Hanamura's first and second electrically conductive layers shown in its first embodiment. *See* Ex.1003, ¶¶265-67. As explained in Egitto, the resistance “*R*” across a material, is calculated by the well-known equation $R = rl/A$, where “*r*” is the resistivity of the material, “*l*” is the material's length, and “*A*” is the cross sectional area. Egitto, ¶¶69-73. Ex.1003, ¶267-68 Accordingly, the resistance of a material or set of materials is directly dictated by the shape of that material(s), and can be altered through corresponding changes to the dimensions of the material(s). Both Hanamura and Egitto apply this principle. *See, e.g.*, Hanamura, 6:55-58 (“The resistance of the resistor layer 30 may be adjusted by a trimming groove 30a (see Fig. 8) of the resistor layer 30,”); Egitto, ¶81 (“[S]elected ones of the remaining resistors may be etched to different widths, thus providing difference resistance values.”).

The claim requires that the resistance region have a particular design, *i.e.*, that a second trench and at least one third trench are formed, which delimit the resistance region, and which cause the resistance region to have taper in a direction parallel to the electrically conductive layers. Such a design is shown, for example, in Figure 9 of the '492 patent, reproduced below (showing second trench 40, third trench 42, and resistance region 44).

Fig. 9

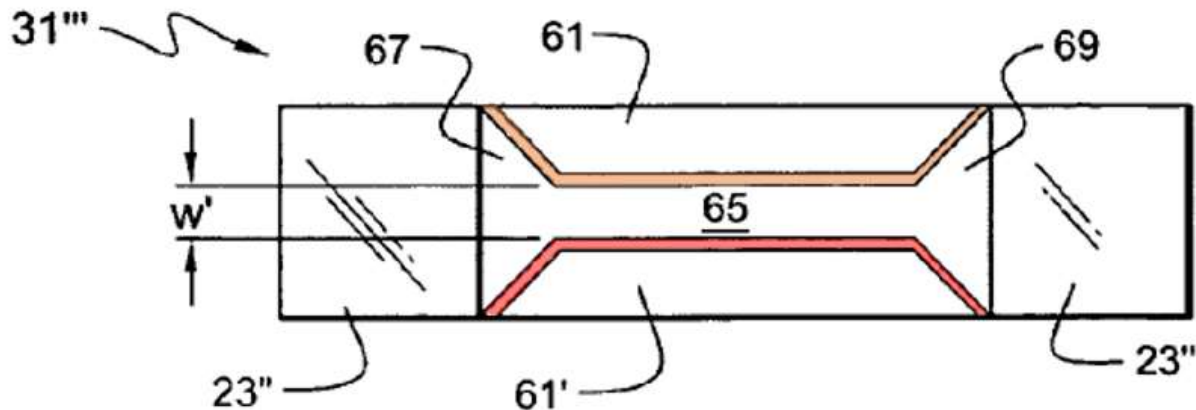


'492 patent, Fig. 9.

This is nothing more than a design choice, one that would in any event have been obvious based on *Egitto*. Ex.1003, ¶276-78.

As previously discussed, *Egitto* relates to providing resistors for circuitized substrates and is focused on adjusting the resistance of thin film resistors in a circuit. *Egitto* teaches that “[t]o increase the resistance of a film resistor, the resistor [can be] ‘trimmed’, often by forming a slot across the electrical current path in the resistor and to make the effective width of the resistor (and the current path there-through)

smaller and thereby increasing resistance.” Egitto, ¶5. Egitto’s Figure 8 discloses a “representative pattern[],” which is materially the same design claimed in the ’492 patent. Ex.1003, ¶279.



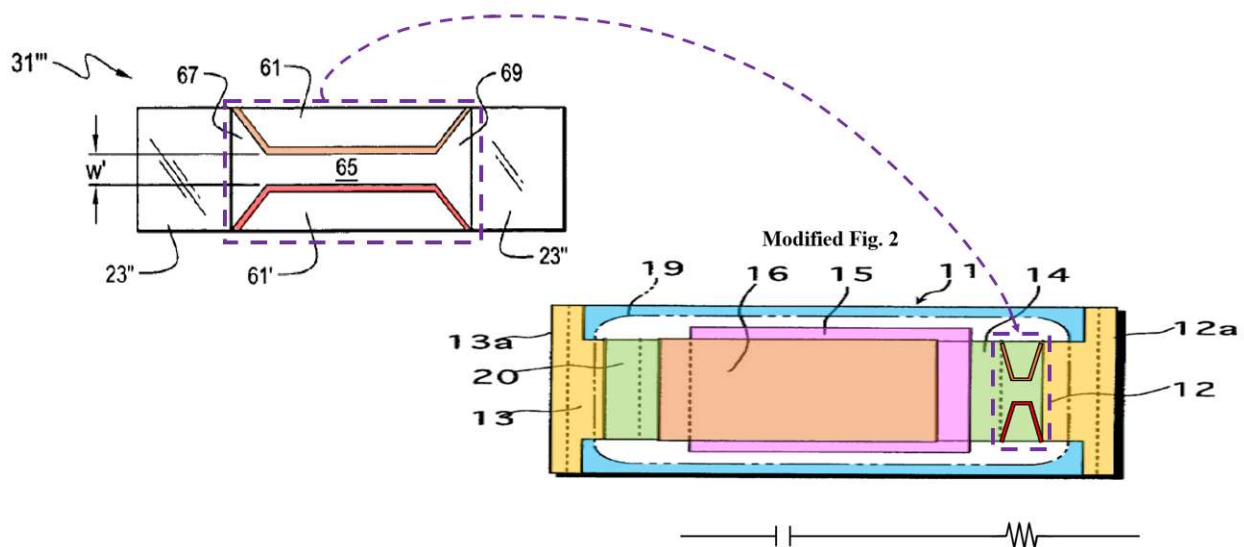
Egitto, Fig. 8 (annotated).

Egitto teaches that the resistor material can be etched away to form “isolated parts 61 and 61’,” which are “substantially trapezoidal, meaning that the center, remaining material (65) has a rectangular shape with substantially triangular ends 67 and 69.” See Egitto, ¶82. Egitto discloses that the etching process is “preferably accomplished using a laser.” *Id.*, ¶83. As shown above, the process involves creating two trenches (orange and red), creating a taper in a direction parallel to the resistor material. Ex.1003, ¶280.

Using the design from Egitto in the electrically conductive layers of Hanamura would involve nothing more than applying a known technique to a known device ready for improvement to yield predictable results. Ex.1003, ¶¶281-85.

Hanamura already disclosed the concept of trimming a groove 30A in its resistor material. *See* Hanamura, 6:50-58. Egitto teaches a specific method of forming the groove 30A, i.e., using a laser, and a specific design. As discussed above, the result would be predictable as resistance is based on a well-known formula linked to the resistivity and dimensions of the material. There would have been an expectation of success for the same reason, and because Egitto taught that its method “enables the circuit designer to alter the resulting resistance by selectively removing ... material and leaving a desired, precise width thereof remaining as the current path.” Egitto, ¶82.

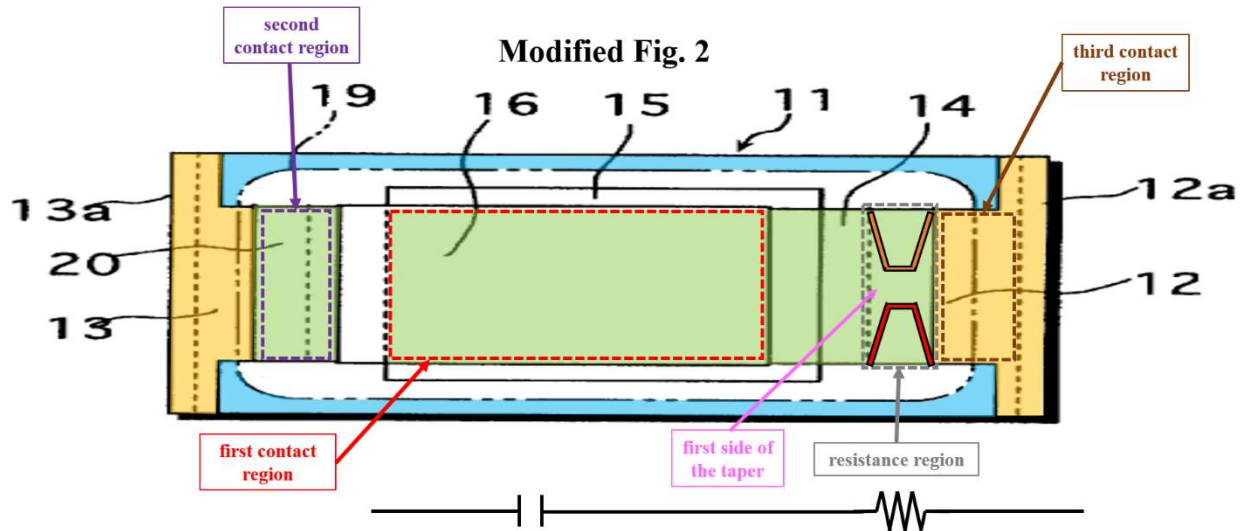
The resulting modification to Hanamura is shown in modified Figure 2 below, where the resistor design from Egitto has been placed into Hanamura’s first embodiment.



Egitto, Fig. 8 (top-left, annotated); Hanamura, Fig. 2 (bottom-right, annotated, modified). *See* Ex.1003, ¶286.

The above combination renders obvious the '492 patent's claim 3. Hanamura forms its first and second electrically conductive layers prior to applying its dielectric. *See, e.g.*, Hanamura Fig. 3 (forming first electrically conductive layer), Fig. 4 (forming second electrically conductive layer), Fig. 5 (forming dielectric layer). Accordingly, if the second and third trenches are formed via the deposition of the electrically conductive layers (as is done for the first trench), the resistance region necessarily would be formed before the dielectric is applied. *See* Ex.1003, ¶287-88. Alternatively, it would have been obvious to a POSITA to etch the trenches prior to applying the dielectric in order to avoid damaging later-deposited layers. *See* Ex.1003, ¶289.

As shown in the modified Figure 2 below, the second and third trenches (orange and red) delimit a resistance region (grey box) that comprises a part of the first and second electrically conductive layers, and which has a taper in a direction parallel to the electrically conductive layers (yellow and green, respectively) and which leads into the first contact region (red box) on a first side of the taper. *See* Ex.1003, ¶290.

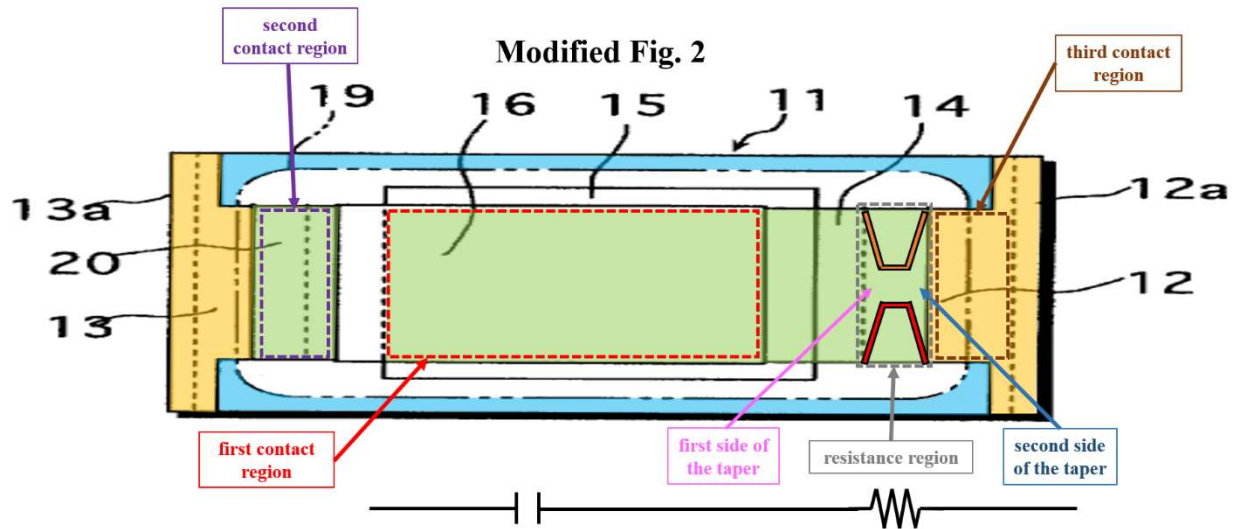


Hanamura, Fig. 2 (annotated, modified). See Ex.1003, ¶290.

2. **Dependent Claim 5:** “The method as claimed in claim 3, wherein the resistance region is formed such that it forms a third contact region on a second side of the taper and thus forms a resistor that is electrically connected in series with the capacitor.”

Claim 5 would have been obvious to a POSITA based on Hanamura in view of Egitto. Ex.1003, ¶¶291-93.

As explained above, it would have been obvious to modify Hanamura to include a resistance region with the design disclosed in Egitto. See *supra* §**Error! Reference source not found.**; Ex.1003, ¶292. As shown below, adding such a resistance region forms a third contact region (brown box) on a second side of the taper and thus forms a resistor that is electrically connected in series with the capacitor.

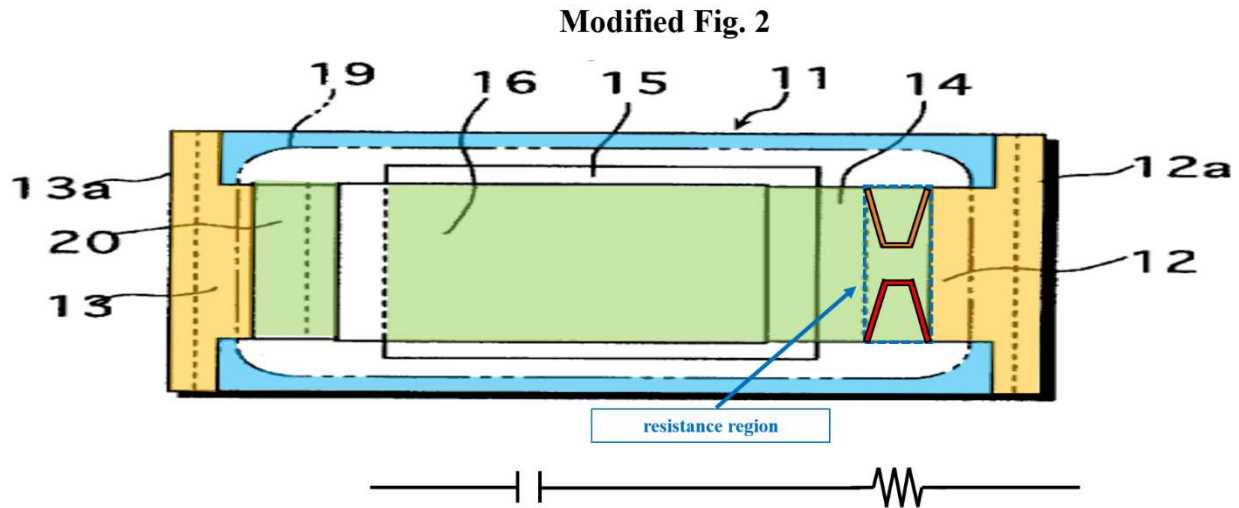


Hanamura, Fig. 2 (annotated, modified). *See* Ex.1003, ¶292.

3. Dependent Claim 6: “The method as claimed in claim 2, wherein a plurality of capacitors and/or resistors are formed electrically in parallel with one another and/or electrically in series one after another.”

Claim 6 would have been obvious to a POSITA based on Hanamura in view of Egitto. Ex.1003, ¶¶294-97.

As explained above, it would have been obvious to modify Hanamura to include a resistance region with the design disclosed in Egitto. *See supra* §**Error! Reference source not found.**; Ex.1003, ¶295. As shown below, adding such a resistance region results in a capacitor that is formed electrically in series with a resistor. *See* Ex.1003,¶295.



Hanamura, Fig. 2 (annotated, modified). *See* Ex.1003, ¶295. Accordingly, Hanamura in view of Egitto discloses a plurality of capacitors and resistors that are formed electrically in parallel with one another and/or electrically in series one after another. *See* Ex.1003, ¶296.

IX. DISCRETIONARY DENIAL IS INAPPROPRIATE UNDER *FINTIV*

The Board should decline to exercise its discretion to deny institution under 35 U.S.C. § 314(a) and *Apple Inc. v. Fintiv, Inc.*, IPR2020-0019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential). While the '492 patent has been asserted in *Pictiva Displays International Ltd. v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:23-cv-00495 (E.D. Tex.) (the “-495 matter”) and *Pictiva Displays International Ltd. v. Samsung Electronics Co., Ltd.*, Case No. 2:24-cv-00532 (E.D. Tex.) (the “-532 matter”), those cases remain in a very early stage.

With respect to Pictiva's most recent assertion of the '492 patent against Samsung Electronics and Samsung Electronics America in the -532 matter, the Complaint was recently filed on July 12, 2024 (Pictiva sued those entities together with Key Patent Innovations Limited). An Answer has not yet been filed, no scheduling order has been issued, and no discovery has taken place, as the case is just underway.

In the -495 matter, in which Pictiva previously sued the same two Defendants, infringement contentions were served on March 11, 2024. The court issued its initial scheduling order on April 17, 2024, scheduling a trial for August 2025. *See* Ex.1025 (Docket Control Order).

Accordingly, the parties have made no material investments in the parallel litigations. Discovery has only just begun in the -495 matter; the deadline to substantially complete document production is December 24, 2024. No depositions have taken place, and the claim construction process has not begun. Additionally, this Petition is being filed less than five months after service of infringement contentions in the -495 matter and less than a month after the filing of the Complaint in the -532 matter, demonstrating that Petitioner has acted with diligence in preparing its patent challenge. Finally, Patent Owner will need to narrow the asserted claims in advance of any trial, *see* Ex. 1025 at 1, and Petitioner has challenged claims not asserted by Patent Owner, such that a trial could not resolve all of Petitioner's

claim challenges. Discretionary denial is further inappropriate because this Petition presents compelling evidence of unpatentability, for the reasons discussed in Section §VIII, above.

X. CONCLUSION

Petitioner respectfully requests *inter partes* review and cancellation of claims 1-3, 5, 6, 8-11, and 16 of the '492 patent.

Date: July 26, 2024

Respectfully submitted,

By / Scott C. Weidenfeller /
Scott C. Weidenfeller
Registration No.: 54,531
COVINGTON & BURLING LLP
One CityCenter, 850 Tenth Street, NW
Washington, DC 20001

David A. Garr
Registration No.: 74,932
COVINGTON & BURLING LLP
One CityCenter, 850 Tenth Street, NW
Washington, DC 20001

CERTIFICATION UNDER 37 C.F.R. § 42.24(D)

I certify that the foregoing complies with the type-volume limitation of 37 C.F.R. § 42.24 and contains 11,785 words based on the word count indicated by the word-processing system used to prepare the paper, and excluding those portions exempted by § 42.24(a).

Date: July 26, 2024

/ Scott C. Weidenfeller /
Scott C. Weidenfeller (Reg. No. 54,531)

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6 and 42.105, I hereby certify that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,257,492 under U.S.C. §§ 311–319 and 37 C.F.R. § 42.100 *et seq.*, together with its supporting exhibits, and Power of Attorney was served by Federal Express for Saturday delivery, a means at least as fast and reliable as Priority Mail Express®, on the following correspondence address of record for patent owner:

Botos Churchill IP Law LLP
430 Mountain Avenue, Suite 401
New Providence, NJ 07974
Customer # 175540

A courtesy copy was also sent patent owner's litigation counsel:

Samuel F. Baxter
Jennifer L. Truelove
MCKOOL SMITH, P.C.
104 East Houston Street Suite 300
Marshall, TX 75670
sbaxter@mckoolsmith.com
jtruelove@mckoolsmith.com

Philip Warrick
IRELL & MANELLA LLP
750 17th Street NW, Suite 850
Washington, DC 20006
pwarrick@irell.com

Jason G. Sheasby
Annita Zhong, PhD
IRELL & MANELLA LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, CA 90067
jsheasby@irell.com
hzhong@irell.com

Rebecca Carson
Jie Gao
IRELL & MANELLA LLP
840 Newport Center Drive, Suite 400
Newport Beach, CA 92660
rcarson@irell.com
jgao@irell.com

Date: July 26, 2024

/ Scott C. Weidenfeller /
Scott C. Weidenfeller (Reg. No. 54,531)