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Analog Integrated
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BIPOLAR AND MOS ANALOG INTEGRATED CIRCUIT DESIGN

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PREFACE

The contents and organization of this book are primarily aimed at the practicing engineer in the field of solid-state electronics. It is intended as a valuable reference for the IC designer and user alike. For the analog IC designer, it provides rigorous design guidelines and examples, while for the user, it offers a detailed analysis of various classes of analog circuits, points out their design philosophy, capabilities, and limitations, and presents application examples and guidelines.

It is intended to be an easy and smooth reading book on a rapidly evolving, high-technology subject. To this end, the lengthy and detailed mathematical treatment of the subject matter is minimized. Long derivations of device or circuit equations are avoided whenever possible; instead, the emphasis is placed on the end result, and the basic design philosophy leading up to it, with a clear understanding of the underlying assumptions and trade-offs. Whenever possible, each new design idea or concept is also demonstrated with a practical example.

The advent of integrated circuit technology has altered many of the established circuit design techniques and principles. This is particularly evident in the field of analog integrated circuits where the designer is faced with a new set of design constraints and ground rules. In writing this book, it is my intention to educate the practicing electronics engineer in the fundamental design principles, capabilities, and applications of monolithic analog circuits. However, the subject matter is treated rigorously and from a fundamental viewpoint, to make this book suitable as a text for graduate study in semiconductor circuits.

This book is an updated sequel to an earlier book by the author, *Analog Integrated Circuit Design* (published by Van Nostrand Reinhold, 1972) which covered the analog IC design technology of the 1960's. Since then, many significant changes have occurred in the world of microelectronics. Perhaps the most important of these has been the "microprocessor revolution," which has resulted in a truly revolutionary growth of digital signal-processing techniques. In turn, this has led to a rapid evolution and advancement of analog circuit methods, particularly in the areas that interface with digital techniques and technologies. As a result, complete LSI systems have evolved which combine complex analog and digital functions on the same chip.

A great deal of this development has been possible by extending the capabilities of MOS devices and process technology to cover analog functions. Consequently, analog IC design using MOS technology has rapidly evolved into a major area of growth. These developments of recent years are profoundly reflected in the contents and the organization of this book.

In the preparation of the text, it is assumed that the reader is familiar with the basic theory and principles of solid-state devices. Therefore, the solid-state device theory, which is already well covered elsewhere in the literature, is reviewed only briefly, and almost all of the space is devoted to circuit approaches unique to monolithic integrated circuits. Hybrid integrated circuits, which represent an area of overlap between discrete and monolithic circuits, are not covered explicitly.

The text of the book is comprised of fifteen chapters which follow a logical sequence in the form of three "sections." The first section of the book, comprised of Chapters 1–3, reviews the basic "tools" of analog IC design and fabrication, namely, process technology, IC components, and techniques for placing these components on the chip, that is, the chip layout. These chapters are intended to familiarize the designer with the physical structures, advantages, and limitations of monolithic components. This knowledge is imperative to an analog IC design engineer since a successful design is one that efficiently utilizes the advantages of monolithic devices while avoiding their shortcomings.

The second section of the text, made up of Chapters 4–6, covers the basic "building blocks," or subcircuits, of analog IC design. One important chapter in this section, Chapter 6, deals with the use of MOS technology in analog or combined analog/digital LSI design. All the subcircuits covered in this section serve as essential building blocks of the complex IC designs that are covered in the remainder of the book.

The third and main section of the book, comprised of Chapters 7–15, covers the entire field of analog integrated circuits by dividing them into functional categories and then examining each category separately. Thus, for example, circuit classes such as operational amplifiers, multipliers, oscillators, phase-locked loops, filters, and data conversion circuits are examined separately. In this section, particular emphasis is given to the recent developments in the field of analog circuits, particularly in the areas of switched-capacitor filters, switching regulators, voltage-controlled oscillators, high-resolution data conversion circuits, and the precision reference circuitry associated with them.

Part of the material in this book is patterned after a sequence of graduate level courses in integrated electronics which I taught at Santa Clara University. Therefore, when preceded by courses on solid-state circuits and semiconductor electronics, this book will be well suited for a senior or graduate level course.

I am grateful to many people who have contributed directly or indirectly to the preparation of this book. In particular, I would like to thank my wife, Karen, who has been a constant source of encouragement for me during the long years of effort that have gone into this book. I would also like to extend my appreciation to many colleagues and associates in the IC industry for their assistance and guidance in the

organization and technical accuracy of the text. I am particularly grateful to the management of Exar Integrated Systems, Inc., for providing me the time to work on this book, and to Ms. Sue Wooldridge who has patiently typed and retyped the draft of the manuscript several times over.

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BIPOLAR AND MOS ANALOG INTEGRATED CIRCUIT DESIGN

CHAPTER THREE

PASSIVE COMPONENTS: DIODES, RESISTORS, CAPACITORS

Monolithic IC processes are designed and developed around active devices. In order to fabricate a number of active and passive devices simultaneously, with the same set of processes, a number of design and performance compromises have to be made. This, in turn, results in the limited sizes and kinds of passive components available in monolithic form. Certain passive components, such as inductors, are not compatible with microminiaturization. The resistors and capacitors are available only with poor absolute-value tolerances, and only over a relatively narrow range of values. The diodes are limited to those available from the p - n junctions used in basic active device structures.

In spite of the limitations on their sizes or absolute-value tolerances, passive components in integrated circuits still enjoy some of the basic advantages of monolithic structures, such as close matching and close thermal tracking. In many cases, by proper choice of the available components and imaginative circuit design approaches, it is possible to overcome the limitations of monolithic components. The circuit techniques used for this purpose are covered in the following chapters. However, before starting an actual design problem, it is imperative that the IC designer should know the basic choices of passive component types and values available. In going from a discrete circuit design to its integrated counterpart, the economics of design often become “inverted.” In the discrete or nonintegrated circuits, cost and complexity can be related to the number of active devices needed. In the monolithic case, it is usually the requirements on the absolute values, or the sizes of the passive components, which can make the design a difficult or uneconomical one.

The purpose of this chapter is to familiarize the designer with the important features of passive components, namely, diodes, resistors, and capacitors. Whenever applicable, comparisons between different types and classes of components are presented in either graphic or tabular form for quick reference.

PART I: INTEGRATED DIODES

3.1. JUNCTION DIODES

Any one of the semiconductor junctions forming the monolithic circuit structure can be used as a junction diode. Figure 3.1 shows the diodes associated with the basic integrated *npn* transistor. D_{BE} and D_{BC} represent the diodes formed by the base-emitter and the base-collector junctions, D_{SS} is the collector-substrate diode in junction-isolated circuits. The resistors r_b and r_{cs} represent the parasitic bulk resistances between the device terminals and the actual diode junctions. Also shown, by dashed lines, is the parasitic *pnp* transistor formed by the base and collector regions of the *npn* transistor and the *p*-type substrate which was described earlier (see Section 2.1).

The collector-substrate diode D_{SS} is not practical for circuit applications since its anode (i.e., the substrate) is common to the entire circuit and must be permanently reverse biased. The collector-base diode D_{BC} must be used with care. If it is forward biased, the parasitic *pnp* transistor is activated. However, the current gain of this transistor is reduced significantly by the presence of the n^+ -type buried layer.

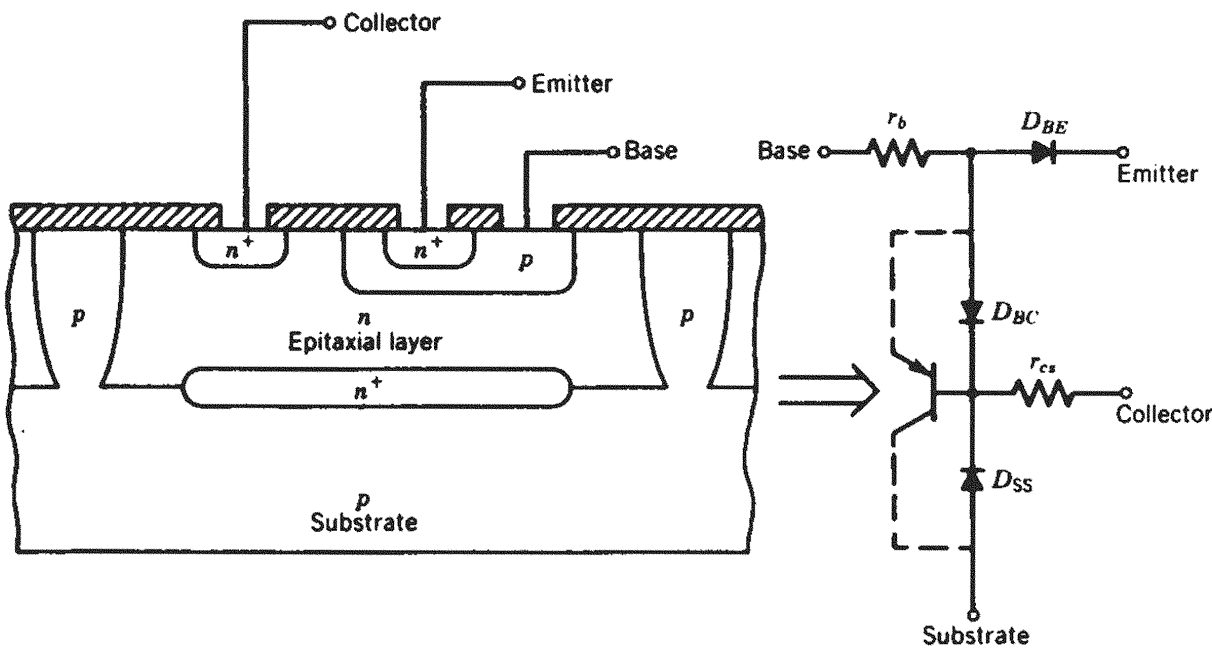


FIGURE 3.1. Possible junction diodes available in integrated *npn* transistor structures.

The diode current I_D is exponentially related to the voltage V_D applied across the junction diode as

$$I_D = I_S \left[\exp\left(\frac{V_D}{V_T} - 1\right) \right] \quad (3.1)$$

where $V_T = kT/q$ is the thermal voltage. I_S is the reverse saturation current, and is proportional to the diode junction area.

Note that this equation is the same as that described earlier in connection with the transistor base-emitter characteristics [see Eq. (2.2).] For a typical integrated diode, the forward I_D and V_D characteristics predicted by Eq. (3.1) are valid over six orders of magnitude in current. For a 1-mil² base-emitter junction area, this range covers current values of 10 nA to 10 mA. At high current densities, due to high-level injection effects, the diode forward characteristics can be approximated as

$$I_D \approx \exp\left(\frac{V_D}{2V_T}\right) \quad (3.2)$$

The dynamic diode forward conductance g_d can be evaluated by differentiating Eq. (3.1) with respect to V_D , that is,

$$g_d = \frac{1}{r_d} = \frac{\partial I_D}{\partial V_D} = \frac{I_D}{V_T} \quad (3.3)$$

Similarly, the diode voltage drop V_D at any given current level can be written as

$$V_D = V_T \ln\left(\frac{I_D}{I_S}\right) \quad (3.4)$$

For forward-current levels greater than 10 μ A, typical values of V_D are in the range of 0.5–0.7 V, neglecting bulk resistances.

The forward diode voltage V_D shows a strong but highly predictable dependence upon temperature. For the case of the base-emitter diode, which is the most commonly utilized diode connection, the temperature coefficient of V_D falls within the narrow range of -1.8 to -2.2 mV per $^{\circ}$ C. This temperature coefficient also shows a weak but predictable dependence on the current density through the diode, as illustrated in Figure 3.2. As a rule of thumb, a base-emitter diode with a 1-sq. mil (625 μ m²) junction area, biased at $I_D = 60$ μ A, corresponds to the -2.0 -mV/ $^{\circ}$ C drift point in the figure.

The semiconductor junctions which make up the *npn* bipolar transistor can be interconnected as a diode in any one of the five possible configurations listed below:

1. Base-emitter junction with the collector left open.
2. Base-emitter junction with the collector short-circuited to base.
3. Base-collector junction with the emitter open.

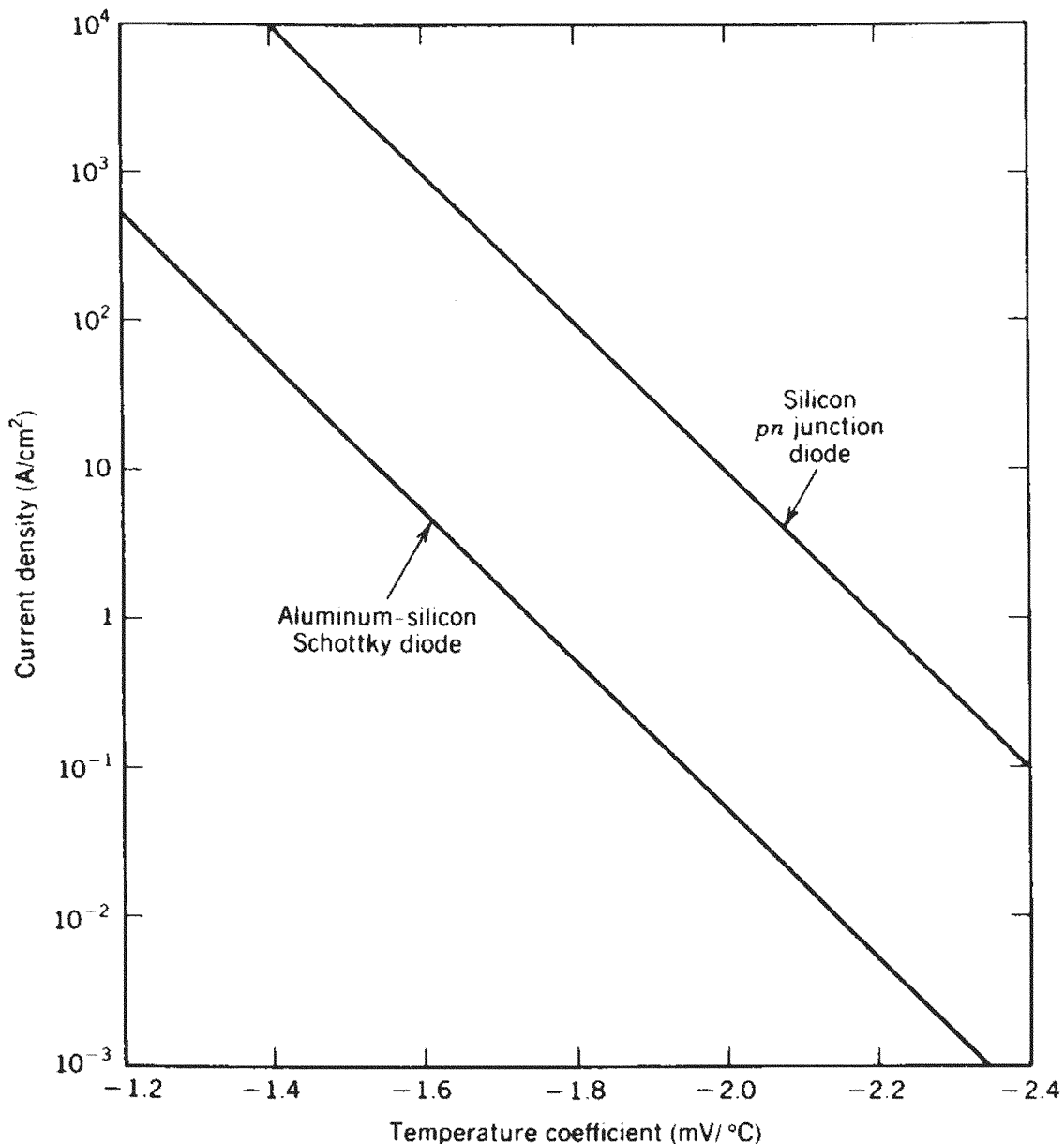


FIGURE 3.2. Temperature coefficient of forward diode voltage V_D for junction and Schottky diodes as a function of current density.⁽²⁾

4. Base-collector junction with the emitter short-circuited to base.
5. Base-emitter and base-collector junctions in parallel.

Figure 3.3 gives a relative comparison of each of these diode connections with respect to the parasitics and the breakdown characteristics associated with each configuration. The series bulk resistances associated with a given diode structure are, in general, the most significant parasitics. With respect to the bulk resistances, diode connection 2 has a distinct advantage over the other configurations since, in this connection, any parasitic resistance in the base or terminal of the device appears divided by β of the transistor.

All the diode-connected transistor configurations, which include the base-emitter junction, have low reverse breakdown voltages (typically 6–8 V). The diode configurations which utilize the collector-base junction under forward

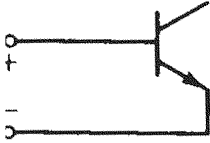
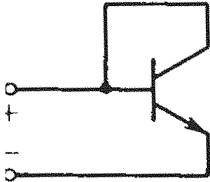
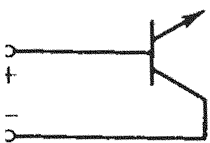
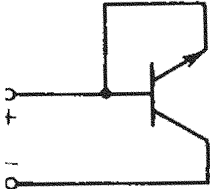
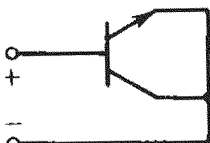
Diode Connection	Series Resistance	Reverse Breakdown	Parasitic <i>pnp</i> Action	Storage Time ($I_d = 2\text{ mA}$)
	Low ($\approx r_b$)	Low (6–8 V)	No	High ($\approx 60\text{ nsec}$)
	Low ($\approx r_b/\beta$)	Low (6–8 V)	No	Low ($\approx 15\text{ nsec}$)
	High ($\approx r_b + r_{cs}$)	High ($>40\text{ V}$)	Yes	High ($\approx 80\text{ nsec}$)
	High ($\approx r_b + r_{cs}$)	High ($>30\text{ V}$)	Yes	High ($\approx 50\text{ nsec}$)
	High ($\approx r_b + r_{cs}$)	Low (6–8 V)	Yes	High ($\approx 100\text{ nsec}$)

FIGURE 3.3. A comparison of practical diode connections for an *npn* transistor.

bias can have parasitic *pnp* action between the base, collector, and substrate regions (see Fig. 3.1)

Diode connection 2 in Figure 3.3 combines two desirable electrical properties: low series resistance and no parasitic *pnp* action to the substrate. Therefore, it is the most commonly used configuration for integrated circuits, as long as its low breakdown voltage does not present a problem.

Effect of Bulk Resistance. Figure 3.4 shows the actual equivalent circuit of the preferred base–emitter diode connection. The transistor is assumed to be ideal, and the parasitic resistances r_b and r_{cs} are identified separately. If the transistor is in its active region, the parasitic base resistance r_b appears reduced by the β of the transistor, and the collector series resistance r_{cs} is masked by the high dynamic impedance of the transistor collector. However, if the voltage drop

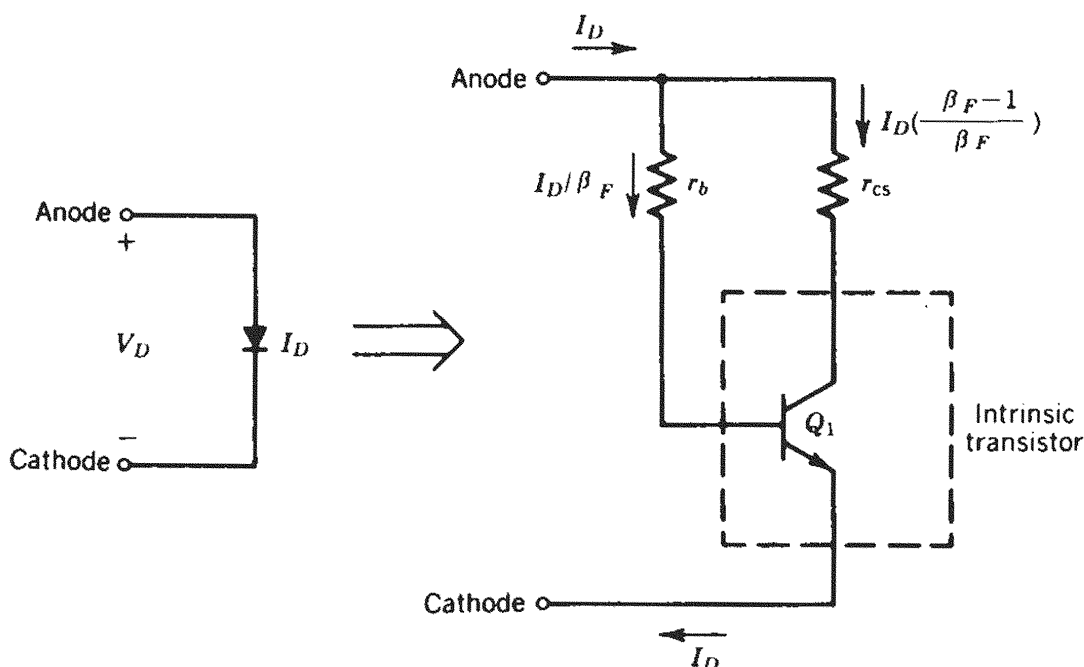


FIGURE 3.4. Effects of parasitic bulk resistances on diode-connected *n*pn transistor. (Note that excessive voltage drop across r_{cs} can cause Q_1 to saturate.)

across r_{cs} is sufficiently high, that is, when $I_D r_{cs} \geq 0.5$ V, it may cause the transistor collector–base junction to be forward biased and Q_1 to go into saturation. When this happens, the diode characteristics deteriorate because β of the transistor is reduced, and the parasitic *pnp* transistor of Figure 3.1 is activated and causes a part of I_D to be shunted to the substrate. For example, in a small-area diode, with $r_{cs} \approx 100 \Omega$, such a parasitic action may start at current levels as low as 5 mA.

Circuit Layout. Figure 3.5 shows the plane view and the crosssection of a diode-connected transistor. Note that this is basically the same as the small-signal *n-p-n* transistor structure of Figure 2.4, with the n^+ -type collector contact region and the collector metal overlapping with the base contact. This is done to reduce the overall device geometry and the collector series resistance, since the collector–base breakdown voltage is of no consideration.

In many circuit applications, most diodes do not share a common anode; thus, they must be placed in separate isolation tubs. In some applications, several junction diodes are used with a common anode, but separate cathodes. In such cases, the multiple-emitter transistor structure of Figure 2.21 can be used, with its collector short-circuited to the base to reduce the chip area.

3.2. SCHOTTKY DIODES

When a metal and a semiconductor material are brought in contact, an electrostatic barrier is formed at the interface, which causes the metal–semiconductor interface to have rectifying properties. In the case of silicon, such a rectifying

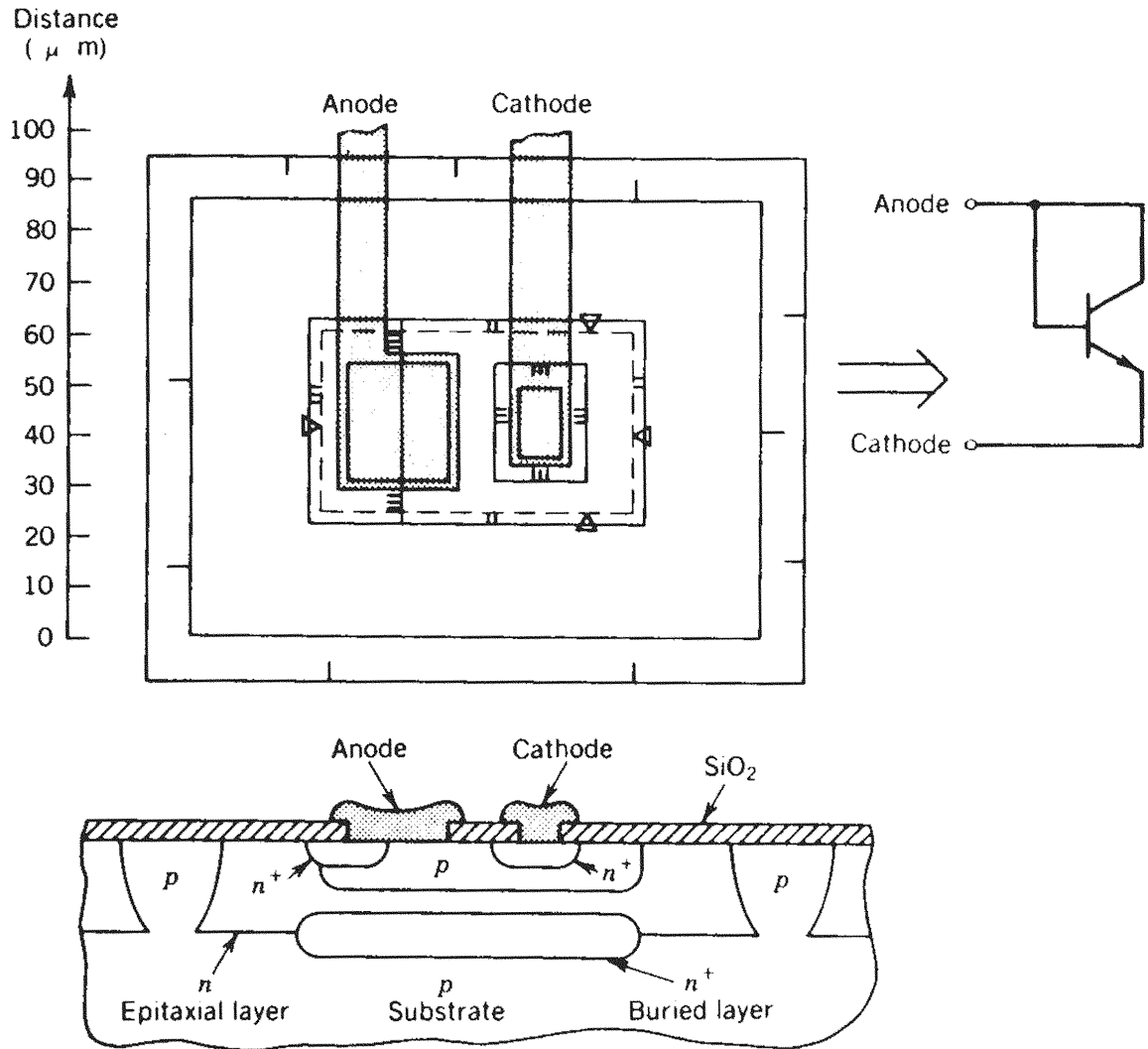


FIGURE 3.5. Lateral dimensions and device cross-section of a typical diode-connected *n*pn transistor. (See Fig. 2.4 for coding of mask layers.)

junction, called a Schottky diode, is formed when a metal such as aluminum is placed in contact with a lightly doped *n*-type silicon ($N_D \leq 10^{17}$ atoms/cm³).⁽¹⁾ In such a diode, the metal serves as the anode and the high-resistivity *n*-type semiconductor region serves as the cathode. Thus, the Schottky diode is forward biased (i.e., conducting) when its metal side is biased positive with respect to the semiconductor side. Schottky diodes can be fabricated with various combinations of metals, such as platinum–silicide (Pt₅Si₂) or aluminum.

The most commonly used Schottky diodes in analog IC design are the aluminum–silicon type diodes. These diodes can be fabricated simultaneously with ohmic contacts by using conventional aluminum evaporation or sputtering techniques. The nature of the resulting silicon–aluminum contact (i.e., ohmic or rectifying) is determined by the resistivity of the semiconductor region which is in direct contact with the metal. Thus, for example, a Schottky diode is formed by simply bringing aluminum in contact with a lightly doped ($N_D < 10^{17}$ atoms/cm³) *n*-type epitaxial region, as shown in Figure 3.6. The polarity of the resulting diode is also indicated. In the simple aluminum–silicon Schottky diode structure of Figure 3.6, the aluminum layer is made to overlap the contact region

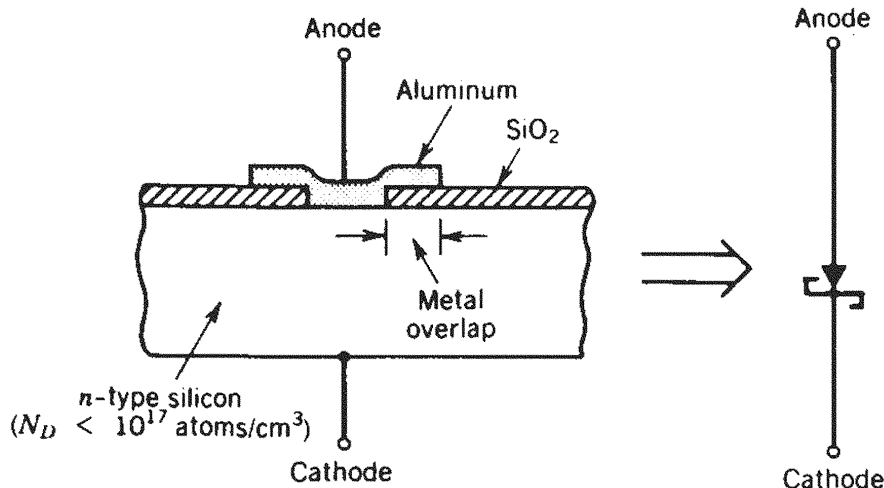


FIGURE 3.6. Cross section of an aluminum-silicon Schottky diode.

by a small amount (typically $\approx 4\text{--}6\ \mu\text{m}$) to serve as a field plate and to reduce the reverse leakage current of the device along the device periphery. This effect is similar to that described in Figure 2.17.

Compared to conventional p - n junction diodes, Schottky diode characteristics have the following significant features:

1. In Schottky diodes, the current flow is by majority carriers, rather than by minority carrier diffusion. Thus, their switching speeds are not limited by the storage time delays and are much faster than those of junction diodes.
2. For a given diode area and the forward-current level, Schottky diodes have a much smaller forward-voltage drop V_F . (For a typical forward current of $10\ \mu\text{A}$, $V_F \approx 0.25\ \text{V}$ for a Schottky diode and $\approx 0.55\ \text{V}$ for a comparable p - n junction diode.)

Because of these advantages, Schottky diodes find a very wide range of application in digital circuits. However, they are also useful in analog circuit applications, particularly in those applications requiring combined linear and digital functions, as a means of “clamping” the collector-base voltage of n pn transistors to keep them from saturating.

Electrical Characteristics. The forward-voltage drop V_F across a Schottky diode depends on the barrier potential ψ_n between the metal and the silicon. In the case of aluminum on n -type silicon, ψ_n is approximately equal to $0.69\ \text{V}$. The forward voltage V_F is related to the forward current I_F as⁽²⁾

$$V_F = \psi_n + V_T \ln\left(\frac{I_F}{I_o}\right) \quad (3.5)$$

where $V_T (= kT/q)$ is the thermal voltage. I_o is the reverse saturation current

given as

$$I_o = RAT^2 \quad (3.6)$$

where R = Richardson constant (≈ 120 Amperes per $\text{cm}^2 \text{ } ^\circ\text{K}^2$).

T = temperature ($^\circ\text{K}$)

A = diode junction area in cm^2

The forward current–voltage characteristics for an aluminum–silicon Schottky diode, given by Eq. (3.5), are valid over approximately five orders of magnitude in current densities I_F/A of from 0.1 mA/cm^2 to 10 A/cm^2 , neglecting the bulk resistance of the silicon.

The temperature coefficient of an aluminum–silicon Schottky diode decreases with increasing temperature, and can be approximated as

$$\frac{dV_F}{dT} \approx -1.76 + 0.086 \ln \left(\frac{I_F}{A} \right) \quad (3.7)$$

where I_F/A is in A/cm^2 . This temperature dependence of V_F is compared in Figure 3.2 with that of a comparable p - n diode.

The reverse breakdown of a Schottky diode varies inversely with the square root of the semiconductor impurity concentration. With a $2.5 \text{ } \Omega/\text{cm}$ n -type epitaxial layer, typical measured reverse breakdown values are in the range of 40–50 V.

Schottky Clamped Transistors. The most common application of Schottky diodes in IC design is the clamping of the n - p - n transistor base–collector junction to keep the transistor out of saturation and, thus, improve its switching speed by reducing the minority carrier charge storage in the base region. This is done by connecting a Schottky diode between the base and the collector regions of the transistor, with the anode (i.e., the metal part) connected to the base.

Figure 3.7 shows the layout and the cross section of such a Schottky clamped n pn transistor structure. The Schottky diode is formed by simply making direct contact to the n -type epitaxial region with aluminum, without putting a heavily doped n^+ diffusion region at the metal–silicon interface. This is normally done by simply extending the base contact window into the n -type collector region, and covering it with an overlapping aluminum layer. As a result, the part of the aluminum making contact to the p -type base forms an ohmic contact, whereas the aluminum touching the n -type epitaxial layer forms a Schottky diode. The resulting transistor and diode combination is shown in Figure 3.7b, where D_s is the Schottky diode. Note that the normal collector and emitter contacts, which have the heavily doped n^+ -type regions in contact with aluminum, are unaffected by this structure.

In the circuit application of the Schottky clamped n pn transistor, as the collector voltage drops below that of the base, the Schottky diode D_s of Figure 3.7b starts conducting and cuts off the base current. With this configuration, the

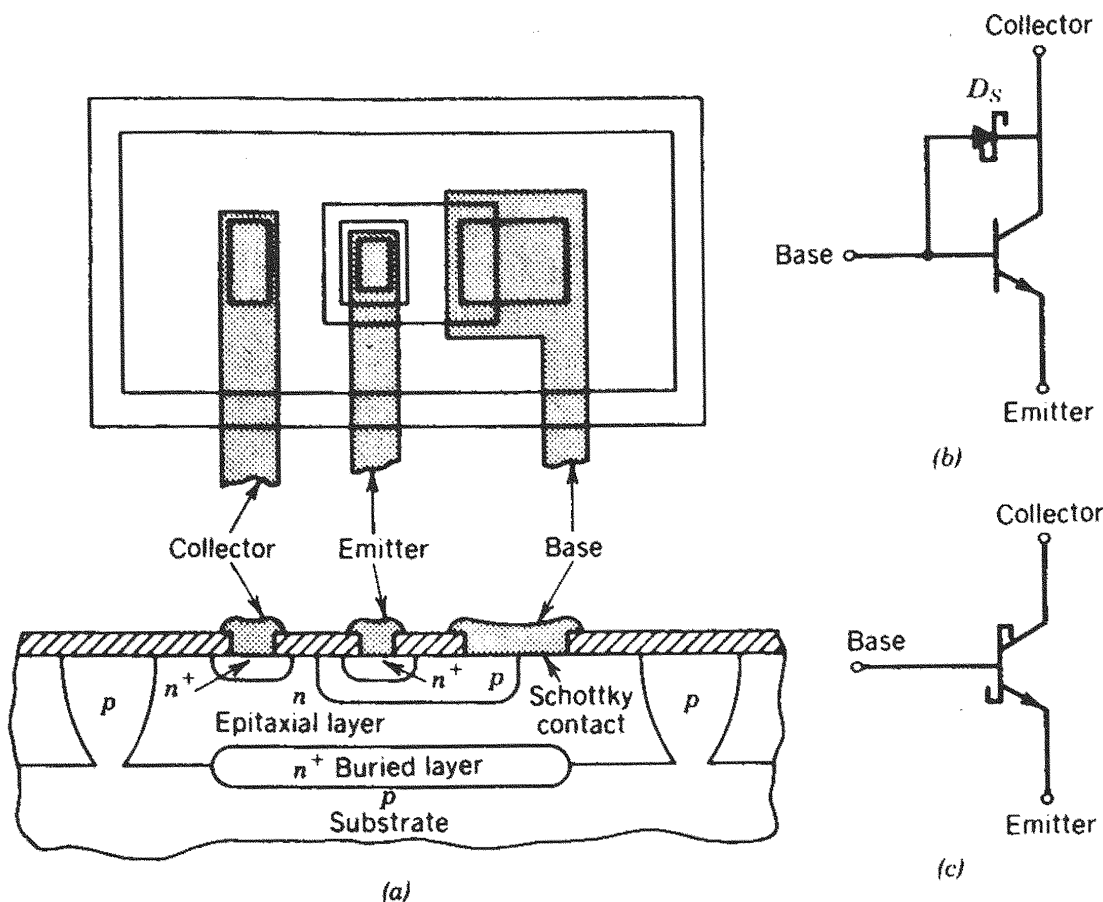


FIGURE 3.7. Schottky clamped npn transistor: (a) typical device layout; (b) electrical equivalent; (c) device symbol.

collector–base voltage cannot drop below $V_{BE} - V_F$, or approximately 0.4–0.45 V at room temperature.

In designing Schottky clamped transistors, a word of caution is in order. The forward voltage V_F is a function of the diode area. Thus, if the transistor to be clamped is operating at high collector currents, then the area of the Schottky clamp diode must be increased in order to maintain a low value of V_F .

Typical applications of Schottky clamped transistors are at the output stages of high-speed analog circuits, such as comparators or oscillators, where large signal swings are required with minimum switching delays.

3.3. ZENER DIODES

The avalanche breakdown of a reverse-biased p - n junction can often be used as a voltage reference or for dc level shift purposes. Although the actual breakdown mechanism of semiconductor junctions encountered in IC fabrication is *avalanche* breakdown, rather than the so-called *Zener breakdown*, it is customary to use the term Zener diode to describe this phenomenon.

As discussed earlier, the three basic junctions available in a monolithic integrated circuit are the emitter–base, the base–collector, and the collector–isolation junctions. The reverse breakdown voltage associated with the

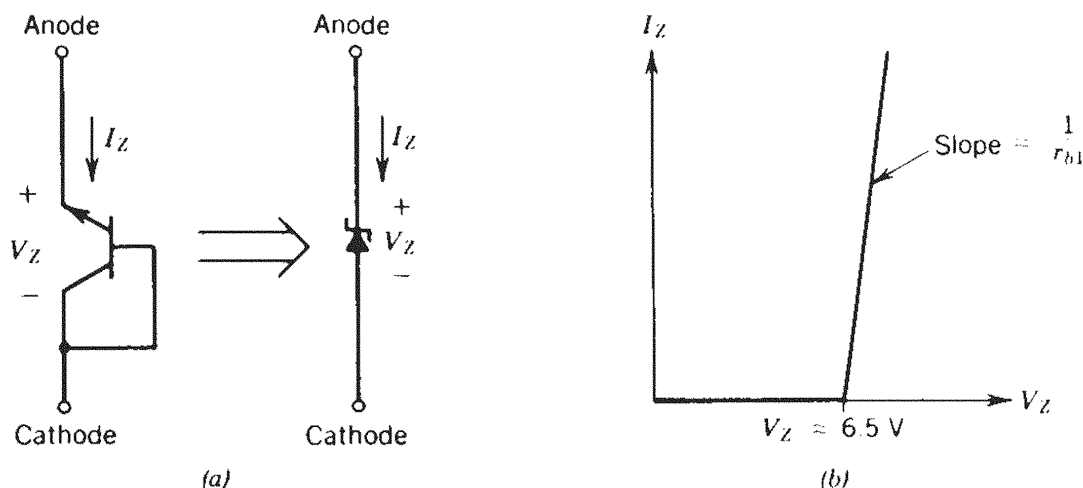


FIGURE 3.8. *npn* transistor base-emitter junction as a Zener diode: (a) Circuit connection and device symbol; (b) current-voltage characteristics.

latter two of these junctions is usually in excess of the power supply voltage, which renders them useless for Zener diode applications. Thus, the base-emitter junction, which has a reverse breakdown voltage BV_{EBO} in the range of 6–8 V, is the most commonly used Zener diode connection. For this purpose, either one of diode configurations 1 and 2 of Figure 3.3 can be used. In general, diode configuration 2 is preferred, since this connection provides a predictable *dc* bias for the *npn* collector region, rather than letting it remain open-circuited, which in turn may lead to parasitic transistor action.

Figure 3.8 shows the basic transistor connection for Zener diode applications, along with its current-voltage characteristics. The breakdown voltage V_Z is equal to the base-emitter breakdown BV_{EBO} . For the case of devices fabricated with the basic bipolar IC processes, this breakdown voltage falls within the narrow range of 6–8 V. The breakdown resistance of the base-emitter Zener is approximately equal to the bulk base resistance r_{b1} of the *npn* transistor (see Fig. 2.14). The typical circuit layout for the Zener-connected *npn* transistor is the same as that of the diode-connected transistor of Figure 3.5, with the emitter biased *positive* with respect to the base region.

The junction breakdown voltage exhibits a temperature coefficient which is positive and increases with increasing breakdown voltage, as shown in Figure 3.9. At very low breakdown voltages, that is, below 5 V, where both sides of the junction are very heavily doped, the true Zener breakdown effect, namely, the carriers tunneling through the junction depletion layer, dominates, and the temperature coefficient of the breakdown changes sign.

The breakdown voltage of the base-emitter junction falls into the rather narrow voltage range of 6–8 V and, thus, exhibits a positive temperature coefficient of +2 to +4 mV/°C.

Temperature Compensation of Zener Diodes. Since the temperature coefficients of the diode forward voltage V_D and the base-emitter breakdown voltage BV_{EB} are of opposite polarity, it is possible to compensate partially the thermal

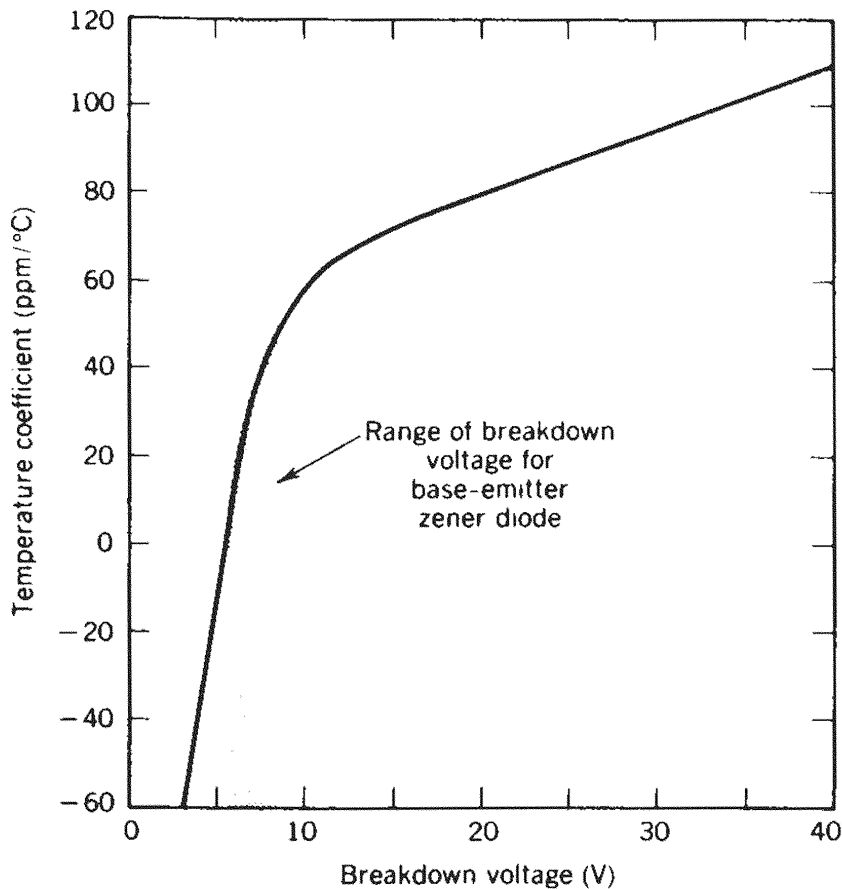


FIGURE 3.9. Temperature coefficient of breakdown voltage.

drift of an avalanche breakdown diode by connecting a forward-biased diode in series with it. The resultant composite diode has a breakdown voltage of $V_D + BV_{EB}$, with a significantly reduced temperature coefficient. In a monolithic circuit, this partial compensation can be obtained with a minimum increase of chip area by connecting two transistors back to back in diode connection 2, as shown in Figure 3.10. Since both transistors now have their collector and base

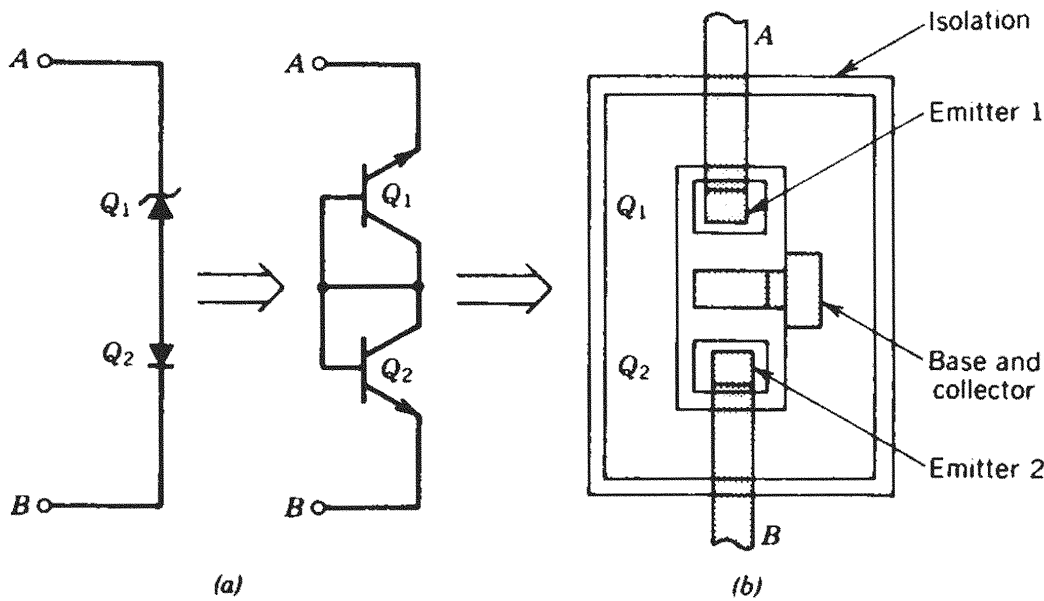


FIGURE 3.10. Temperature-compensated zener diode: (a) Circuit connection and (b) layout.

regions in common, they can be designed as a single transistor with two separate emitters, as shown in the figure.

Buried-Zener Structures. In the base-emitter junction, the breakdown takes place at the surface of the device, where the doping level of the junction is at a maximum. This makes the actual breakdown voltage difficult to predict and subject to long-term drift, due to surface irregularities and contamination. To avoid this problem, several Zener diode structures have been developed which confine the breakdown mechanism to *below* the surface of the device. Because the actual breakdown takes place in the subsurface region, these Zener diodes are often called *buried Zeners*.

Figure 3.11 shows the simplest buried-Zener structure compatible with bipolar IC fabrication steps. This is the so-called *isolation Zener*, which is formed by placing an n^+ emitter diffusion over a p -type isolation region, such that n^+ completely overlaps the isolation region. Such a Zener diode has its p side permanently grounded, since it is formed by the isolation of the p -type substrate common to the entire circuit. The typical breakdown voltage of the isolation Zener diode is of the order of $5.4 \pm 0.4 \text{ V}$, depending on the impurity profile

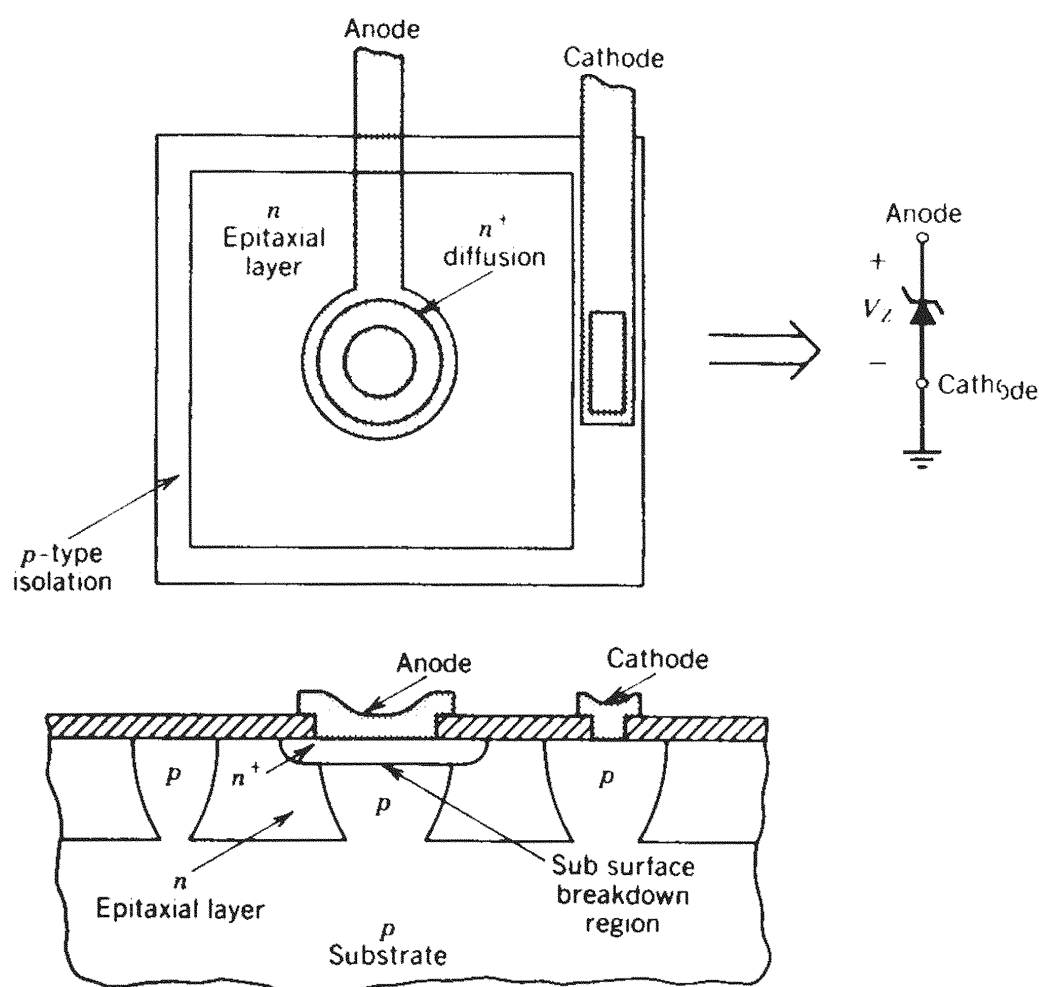


FIGURE 3.11. Layout and cross section of a buried-Zener structure using n^+ emitter and p^+ isolation diffusions. (Note: $V_Z \approx 5.4 \pm 0.4 \text{ V}$.)

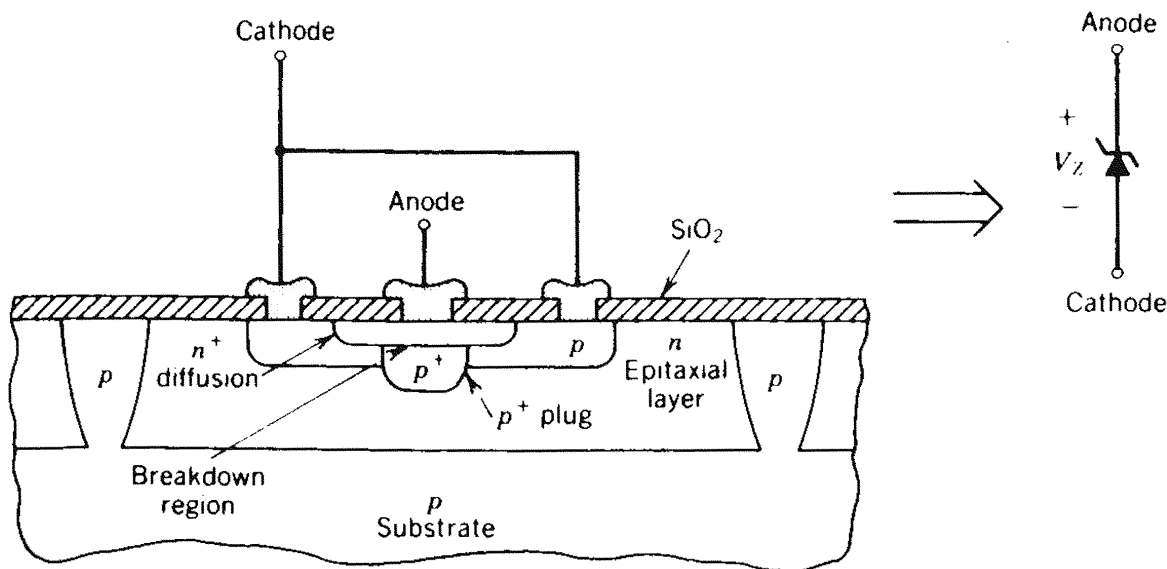


FIGURE 3.12. Buried-zener structure using *p*⁺ plug diffusion.⁽³⁾

of the isolation region. Its temperature coefficient is in the range of +1 to +2 mV/°C. Note that in the device layout of Figure 3.11, a circular geometry is used to avoid localized breakdown of the device at its corners. This layout technique is often used in designing Zener diodes whose breakdown voltages must be reasonably well controlled.

Figures 3.12 and 3.13 show alternate buried-Zener structures compatible with bipolar IC processing steps. In each case, a circular device layout is assumed. In the device structure of Figure 3.12, an additional deep *p*⁺ diffusion, called *p*⁺ plug, is used prior to the *p*-type base and the *n*⁺ emitter diffusions. The *n*⁺ diffusion completely covers the *p*⁺ plug diffusion. The resulting diode breaks down where the dopant concentration is the greatest, that is, at the intersection of the *p*⁺ and *n*⁺ diffusions. The normal *p*-type base diffusion is then used to make contact to the *p*⁺-type region (i.e., the cathode) of the Zener diode. Surface

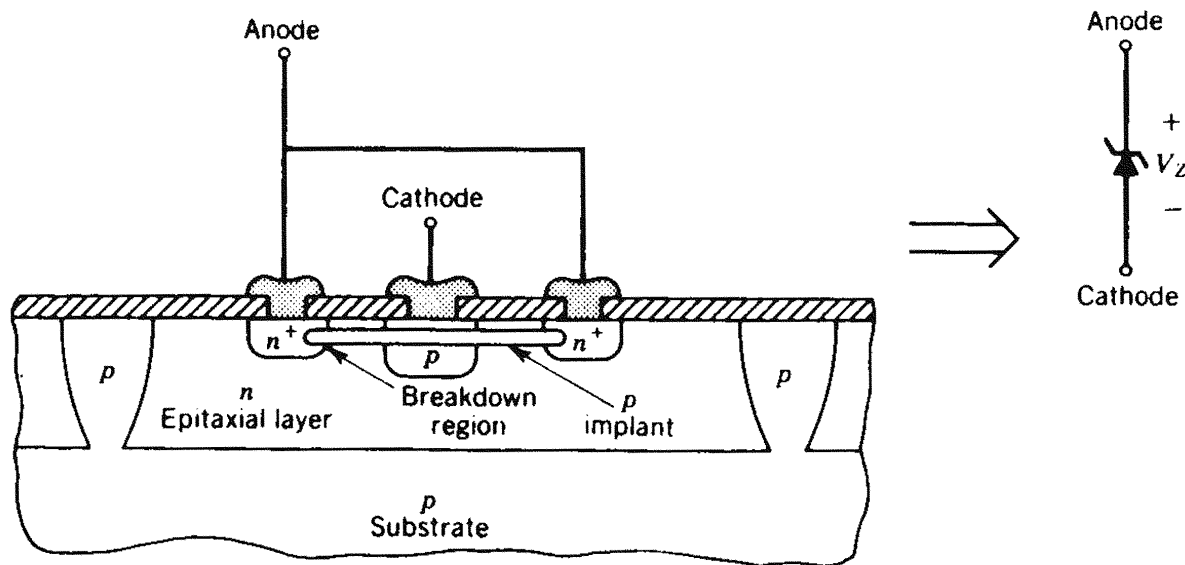


FIGURE 3.13. Ion-implanted buried-zener structure.⁽⁴⁾

breakdown between the p -type base and the n^+ emitter diffusions does not occur since this breakdown voltage is higher than the p^+-n^+ junction breakdown. This type of buried-Zener structure exhibits a typical breakdown voltage of 6.3 V, with a production tolerance of ± 200 mV.⁽³⁾

An alternate buried-Zener structure is the ion-implanted subsurface Zener diode of Figure 3.13. In this case, first the p -type and the n^+ -type regions are diffused during the base and the emitter diffusion cycles. Then a heavily doped p^+ -type layer is implanted over the area indicated in the figure. This p^+ implant overlaps the p^+ -type base diffusion and touches the n^+ ring surrounding it. Since the implanted p^+ -type layer has its maximum impurity concentration *below* the surface, the breakdown occurs along the n^+-p^+ junction below the device surface, with the n^+ and p diffusions serving as the anode and the cathode contacts for the device.⁽⁴⁾ With this technique, it is possible to control the absolute value of the breakdown voltage to within ± 100 mV under production environment.

PART II: INTEGRATED RESISTORS

Two general classes of resistors are available in monolithic circuits: semiconductor and thin film. The semiconductor resistors in turn can be categorized into the following four groups, based on their physical structure:

1. Diffused resistors.
2. Pinched resistors.
3. Epitaxial resistors.
4. Ion-implanted resistors.

Semiconductor resistors are, by far, the most commonly used monolithic resistor structures. With the exception of ion-implanted resistors, they can be fabricated simultaneously with the rest of the circuit elements, without requiring extra processing steps. However, they are, in general, nonideal circuit components, with rather loose tolerances, and by discrete component standards, they have poor temperature and frequency characteristics. The thin-film resistors, on the other hand, offer superior electrical characteristics at the expense of additional processing steps and may be “trimmed,” or adjusted, to a specific tolerance after the deposition step.

The electrical parameter that is most often used in characterizing integrated resistors is the *sheet resistance*. In the case of a uniform sample of resistive material having length L , width W , and thickness T , as shown in Figure 3.14, the total resistance R of the resistor can be written as

$$R = \frac{\rho L}{TW} \quad (3.8)$$

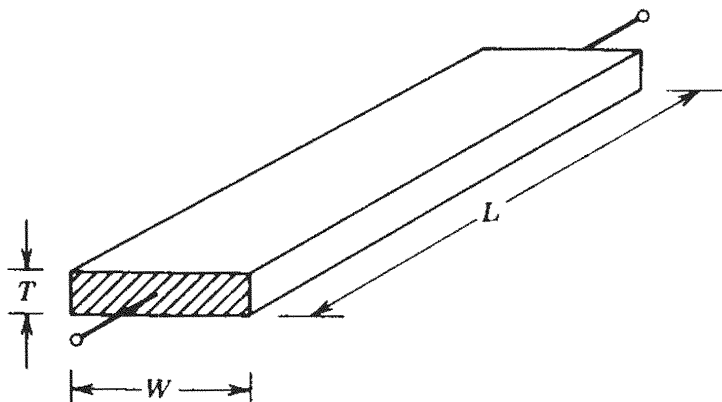


FIGURE 3.14. Calculation of sheet resistance for a uniform sample of resistive material.

where ρ (ohm/cm) is the resistivity of the material. For actual design and layout considerations, it is more convenient to define the parameter R_s (ohms), called *sheet resistance*.

$$R_s = \frac{\rho}{T} \quad (3.9)$$

In physical terms, the sheet resistance corresponds to the resistance of one “unit square” of the material with $L = W$. For this reason, the value of R_s is often stated in ohms per square ($\Omega/\square$). Once the value of sheet resistance is given, the total value of the resistor is determined only by its length-to-width ratio, namely,

$$R = R_s \frac{L}{W} \quad (3.10)$$

For example, if one were to make a 1-k Ω resistor using a material with $R_s = 100 \Omega/\square$, one would design it to have a length-to-width ratio of 10 between the end contacts.

3.4. DIFFUSED RESISTORS

A diffused resistor structure is formed by the bulk resistance of a diffused semiconductor region. In forming a monolithic resistor, either of the two basic diffusion cycles, that is, the base or the emitter diffusion, can be utilized. The *p*-type diffused resistor, which is fabricated using the base diffusion cycle of the *npn* transistor, is the most commonly used resistor structure.

Figure 3.15 shows a typical geometry and the cross section of a *p*-type diffused resistor obtained using the *npn* base-diffusion step. In circuit applications of such a resistor structure, it is necessary that the *p-n* junction outlining the resistor should, at all times, be reverse biased to confine the current flow to the volume of silicon defined by the resistor geometry. The total resistor value R is given as

$$R = \frac{\bar{\rho}}{x_j} \frac{L}{W} = R_s \frac{L}{W} \quad (3.11)$$

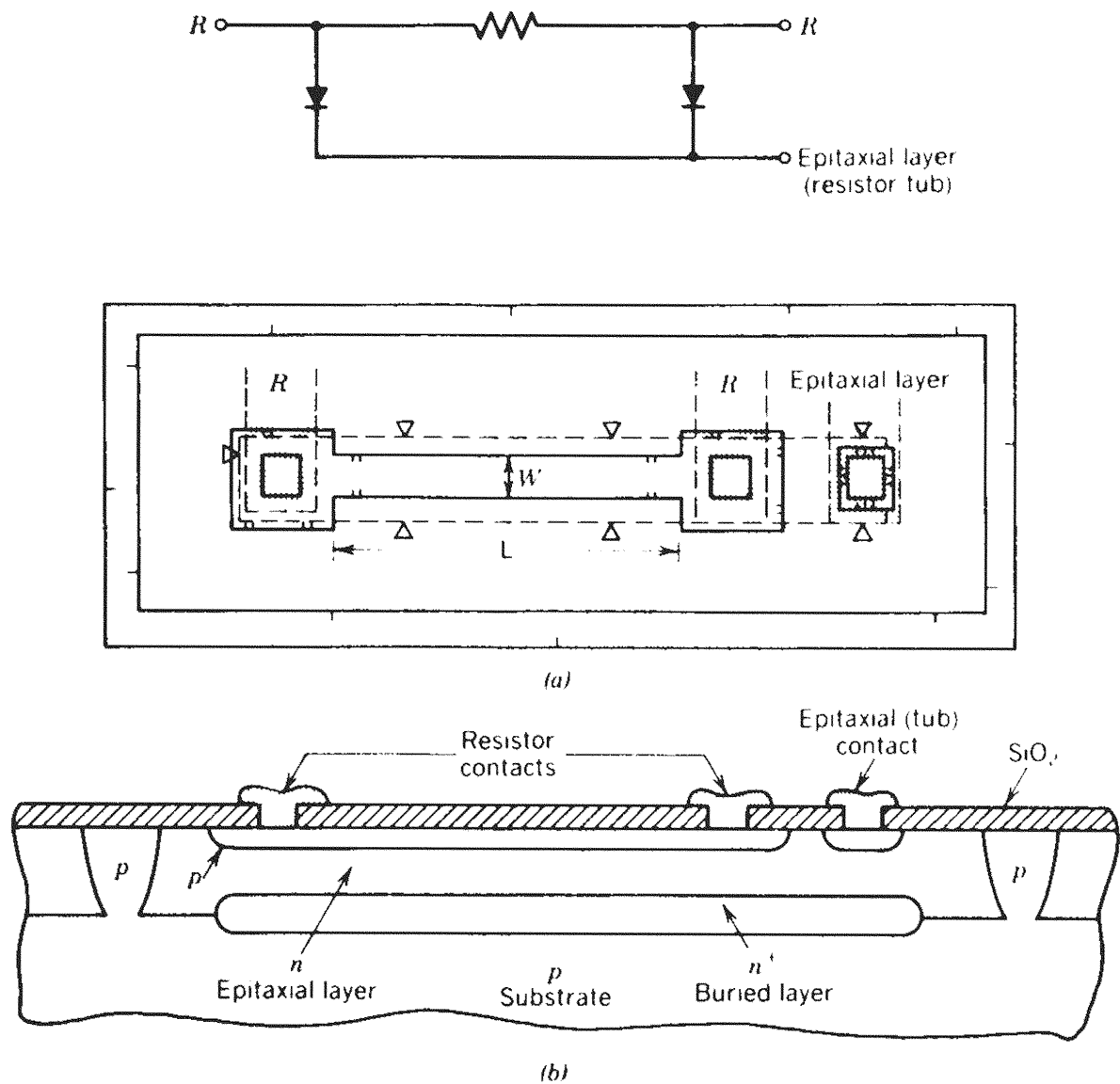


FIGURE 3.15. p-Type base-diffused resistor (see Fig. 2.4 for coding of mask layers): (a) Typical device layout; (b) Cross section.

where x_j is the junction depth of the diffused resistor, and $\bar{\rho}$ is the *average* resistivity of the diffused layer. In a diffused resistor, due to nonuniform impurity distribution, the average resistivity $\bar{\rho}$ is difficult to calculate analytically. In the literature, detailed tables of $\bar{\rho}$ are available for various impurity profiles and background concentrations.⁽⁵⁾

For the case of base-diffusion profiles commonly used in analog IC fabrication, the available values of R_s are typically in the range of 60–250 $\Omega/\square$, with the most common range of values being between 130 and 200 $\Omega/\square$.

The sheet resistance R_s has a positive temperature coefficient due to the decrease of carrier mobility with temperature. Figure 3.16 shows the typical temperature dependence of R_s for a p-type diffused resistor. As will be described in later chapters, this strong temperature dependence of R_s is one of the dominant thermal drift sources in a monolithic circuit. At high current levels, localized self-heating of the resistor can cause the current–voltage characteristics to be nonlinear. To avoid this effect, it is good design practice to limit the power

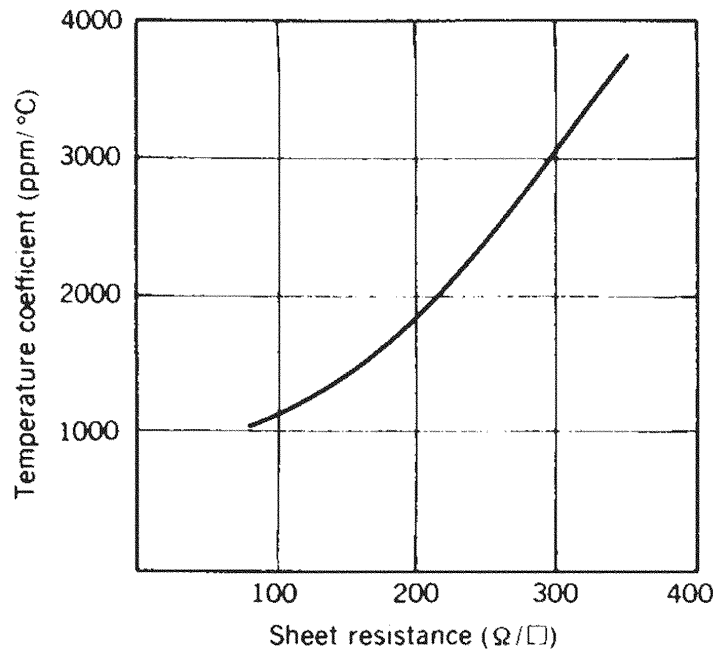


FIGURE 3.16. Typical temperature coefficient of *p*-type diffused resistor as a function of sheet resistance.

dissipation of a diffused resistor to less than 3 mW per square mil of junction area.

Side-Diffusion Effects

In calculating the value of a diffused resistor from its mask dimensions *L* and *W*, it is also necessary to take into account the side diffusion of impurities under the oxide window of width *W*. Figure 3.17 shows the cross section of a diffused resistor taken transverse to the direction of current flow. Note that the effective cross-sectional area of the resistor is *increased* due to the side diffusion of the impurities under the oxide window, shown as the shaded areas in the figure. The effect of side diffusion can be taken into consideration by defining an *effective width* *W_{eff}* for the resistor, instead of the actual diffusion window width *W* where *W_{eff}* ≥ *W*, when calculating the resistor length. Figure 3.18 gives the approxi-

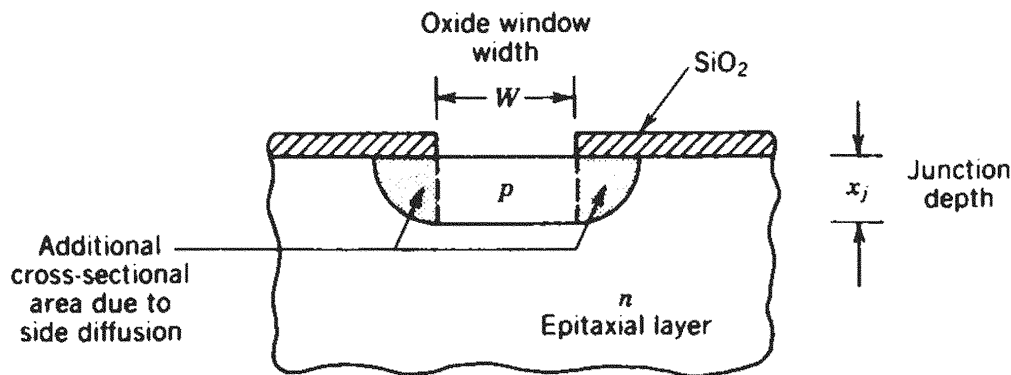


FIGURE 3.17. Transverse cross section of diffused resistor, showing the effects of side diffusion.

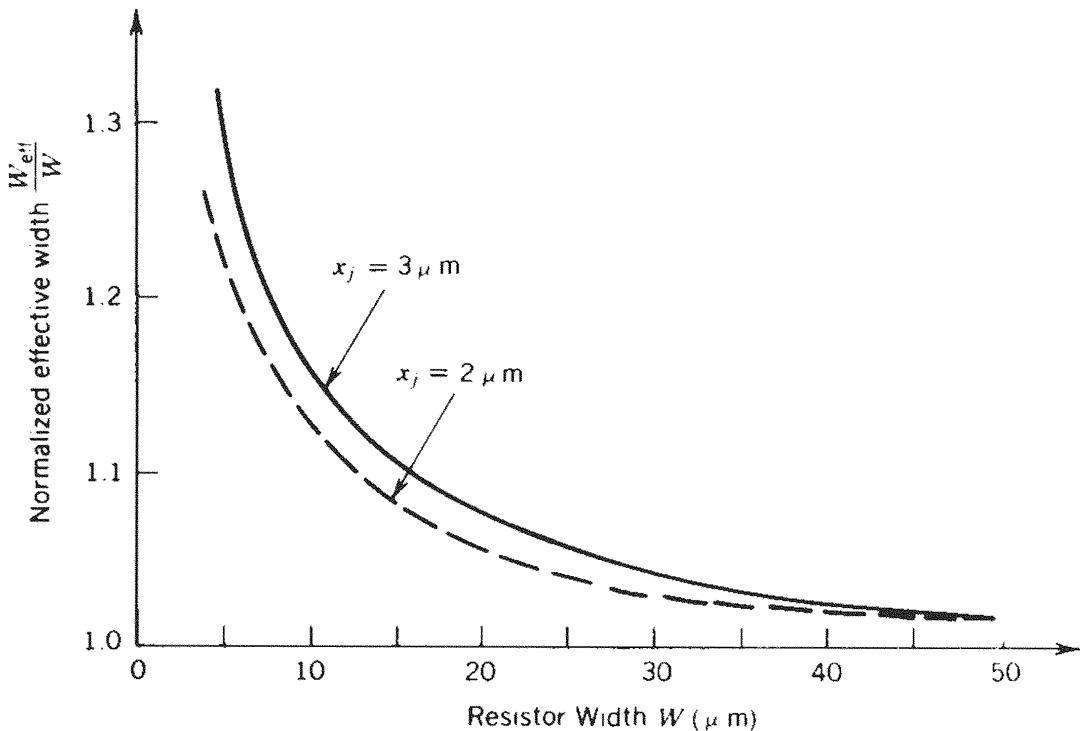


FIGURE 3.18. Effective width of a resistor, including side-diffusion effects.

mate value of W_{eff} as a function of the window width. Note that the side-diffusion effects are particularly significant for narrow resistor widths (i.e., $W \leq 10 \mu m$) and deeper junctions.

Resistor Layout and Tolerances

To obtain a given resistor L/W ratio, with efficient use of the chip area, often requires that the resistor follow a folded or zigzag structure. This can be achieved by making square or round bends in the lateral layout of the resistor, as shown in Figure 3.19. The equivalent values of the L/W ratios for such bends (measured between lines *A* and *B*) are also shown. The inner separation in the resistor fold, shown as the distance k in the figure, is set by the side-diffusion effects (see Fig. 3.17) and is normally no less than 10μ . The lower limit of resistor width W is set by the masking tolerances and is approximately $5\text{--}7 \mu m$ for production circuits. The best matching of resistor values is obtained for the values of W in excess of $20 \mu m$, where the effects of side diffusion or masking irregularities are reduced.

The end points of diffused resistors are normally widened to make sufficient room for ohmic contacts. This often results in an irregular resistor shape near the contact area. Figure 3.20 shows some of the typical diffused resistor endings and their contribution to the total resistor value in terms of *equivalent squares*.⁽⁶⁾

The absolute-value tolerance of diffused resistors is dependent on two factors: (1) control of sheet resistivity and (2) masking tolerances and irregularities. The typical range of sheet resistivity tolerance is approximately $\pm 20\%$ in the production environment. The masking tolerance is primarily due to the *edge*

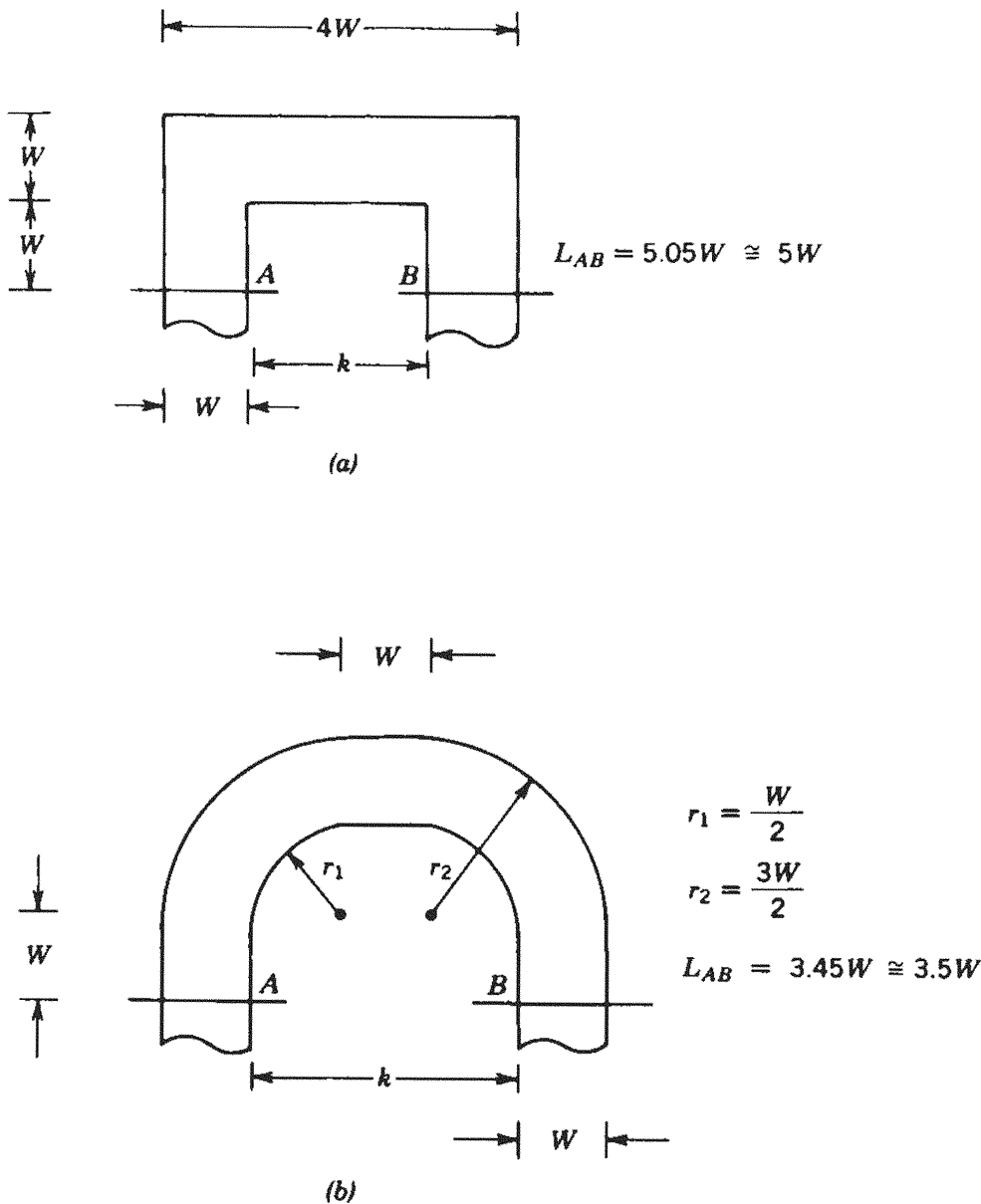


FIGURE 3.19. Calculation of effective resistor length around square and round corners.

definition of the resistor pattern, and is typically of the order of $\pm 0.5 \mu\text{m}$ for each edge of the resistor. Table 3.1 gives a summary of some of the absolute-value tolerances associated with various resistor widths. Note that for resistor widths beyond $5 \mu\text{m}$, control of the sheet resistance is the dominant factor in determining the absolute-value tolerance.

The matching of diffused resistors, and the tracking of component values over temperature, are excellent for identical devices located side by side on the chip layout. The matching characteristics are primarily limited by random mask irregularities; thus, they improve as the resistor width is increased.

In practice, the typical range of resistor values which can be obtained from a sheet resistance R_s is

$$0.1 R_s \leq R \leq 10^3 R_s \tag{3.12}$$

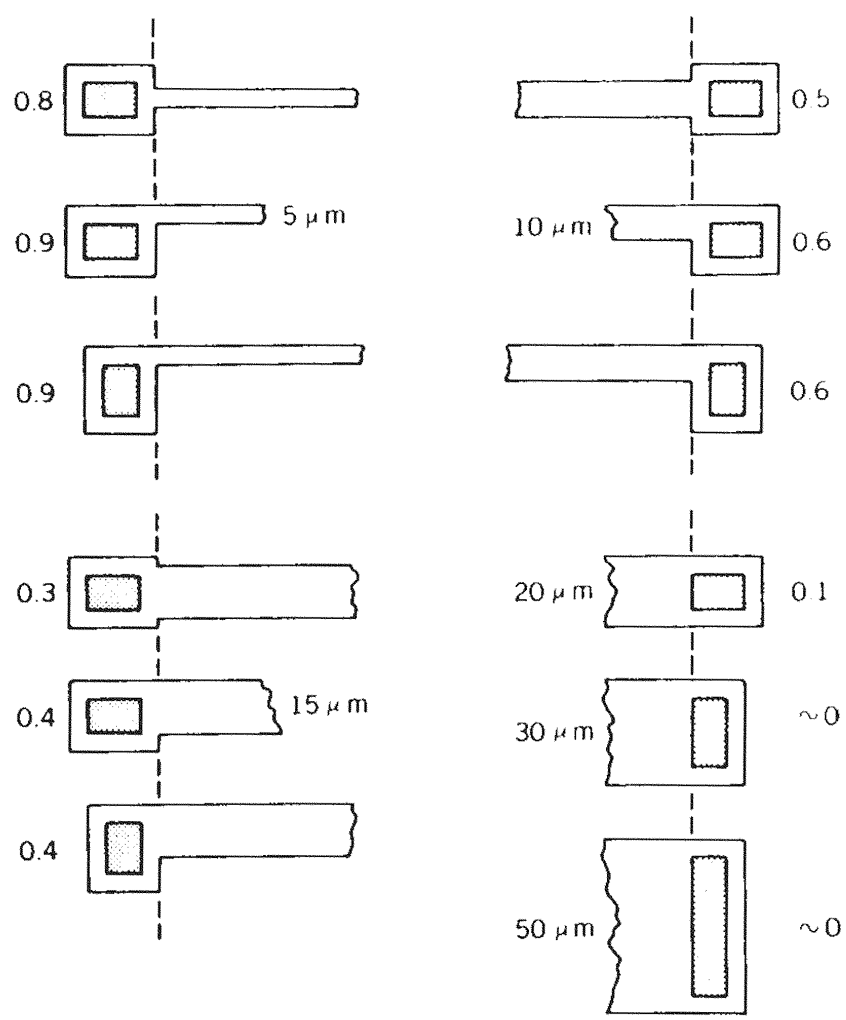


FIGURE 3.20. Resistance contributions of diffused resistor endings. (Units in equivalent squares.)^a

TABLE 3.1. Electrical Characteristics of *p*-Type Diffused Resistors

Sheet resistivity range	100–200 Ω/□
Temperature coefficient	+1500– +2000 ppm/°C
Absolute-value tolerance ^a	
5-μm wide	± 30%
10-μm wide	± 22%
50-μm wide	± 20%
Matching tolerance of identical resistors ^a	
5-μm wide	± 3%
10-μm wide	± 1.2%
25-μm wide	± 0.8%
50-μm wide	± 0.2%

^aIn tolerance distributions, sigma limit is assumed.

In the lower end of this range, the practical limit is set by the contact resistances associated with the resistor contact windows. The practical limit at the upper end is set by the available chip area.

n^+ Diffused Resistors

A low-value resistor can be obtained by using the heavily doped n^+ emitter diffusion of an $n p n$ bipolar transistor. Figures 3.21 and 3.22 show two such resistor structures commonly used in analog IC design. The sheet resistance R_s of n^+ diffusion is normally in the range of $2\text{--}10\ \Omega/\square$, with a typical temperature coefficient of $+2000\ \text{ppm}/^\circ\text{C}$.

The key advantage of n^+ resistors is the low value of R_s , which makes them feasible for the design of resistors in the range of $1\text{--}100\ \Omega$. Such low-value resistors are useful for output short-circuit protection or overload shut-down circuitry in amplifiers and regulators. They also find application as crossunders, or *underpasses*, in circuit interconnections to simplify the layout of the integrated circuit interconnection pattern.

The basic n^+ resistor structure of Figure 3.21 is obtained by putting an n^+ diffusion layer on top of the n -type epitaxial region. Since the epitaxial layer is of much higher resistivity, the resistance between the resistor terminals is almost totally determined by the n^+ diffused layer. The advantage of this device structure is its high breakdown voltage, which is equal to the collector–isolation breakdown. Its disadvantage is that each n^+ resistor would require a separate isolation pocket.

The n^+ resistor structure of Figure 3.22 is imbedded within the p -type base-diffused island. In such a resistor structure, it is necessary that the p -type island be reverse biased with respect to the n^+ -type region at all times. It is also

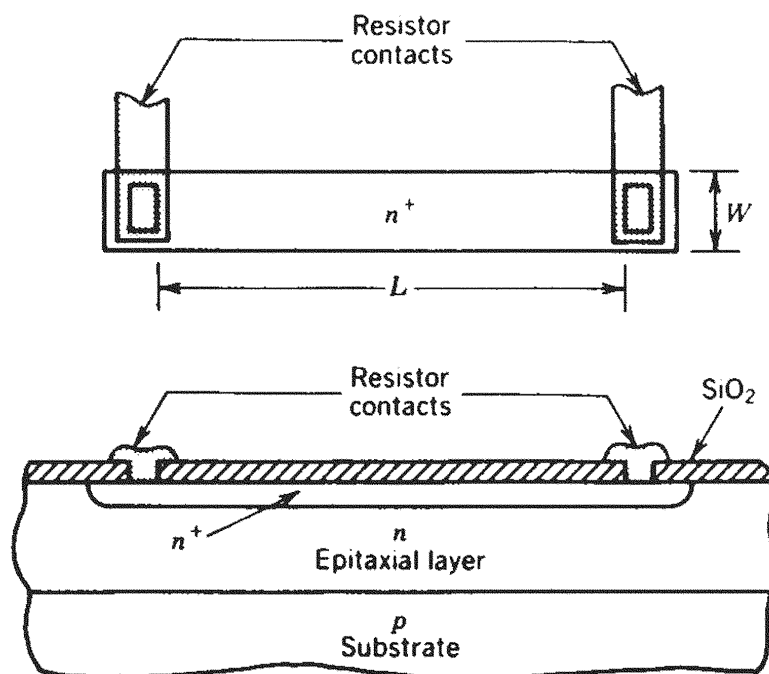


FIGURE 3.21. Top view and cross section of n^+ diffused resistor in epitaxial tub.

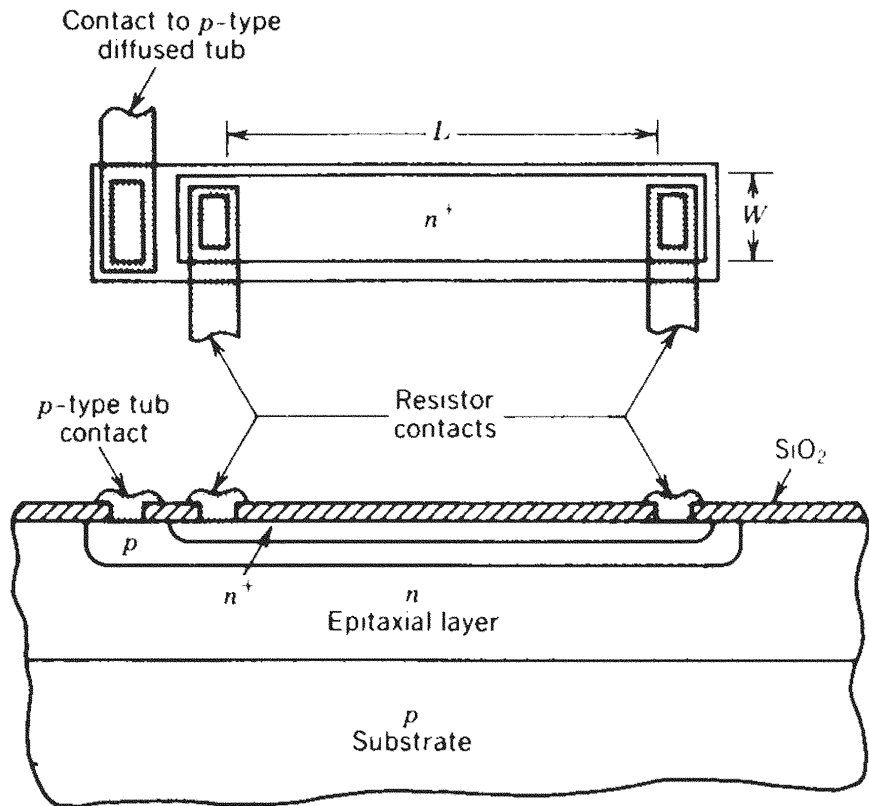


FIGURE 3.22. Top view and cross section of n^+ diffused resistor in p -type diffused tub.

important that the p -type island be either short-circuited or reverse biased relative to the n -type epitaxial region to avoid parasitic npn transistor action. The advantage of the n^+ resistor structure of Figure 3.22 is that several such resistors can be placed in the same isolation tub or in the same p -type island and, thus, save on the chip area. Its disadvantage is the low breakdown voltage (≈ 6.5 V) between the n^+ resistor and the p -type base diffusion.

Frequency Response

The diffused resistor structure has a distributed capacitance associated with it, due to the reverse-biased p - n junction which surrounds it. Figure 3.23 shows the high-frequency equivalent circuit of a diffused resistor of total value R_1 , which has a distributed capacitance C_1 associated with it. In the case of p -type diffused resistors formed by base diffusion, this capacitance is equivalent to C_{CO} of Table

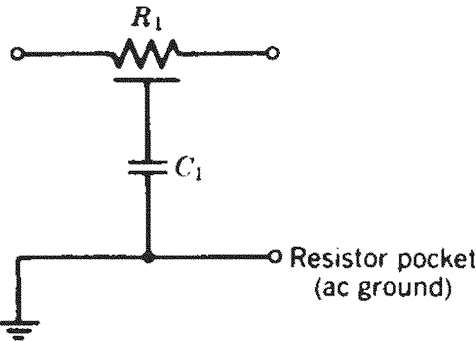


FIGURE 3.23. High-frequency equivalent circuit of diffused resistor.

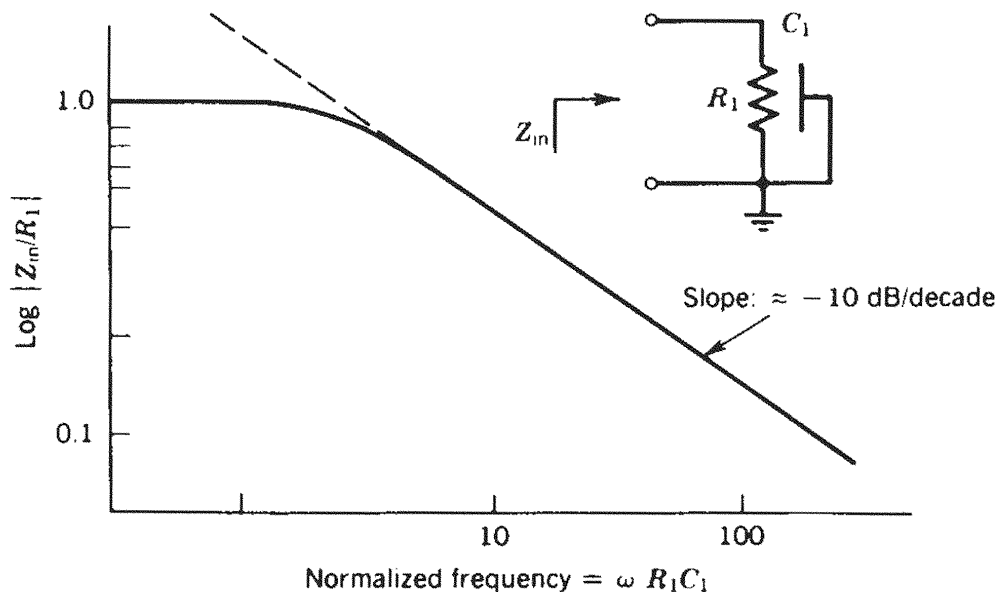


FIGURE 3.24. Normalized frequency response of diffused resistor.

2.2 per unit area of the junction, calculated under appropriate bias conditions. In the case of n^+ diffused resistors fabricated with the emitter diffusion, the junction capacitance per unit area is equal to C_{JE0} for the device structure of Figure 3.21, and C_{CS0} for the device of Figure 3.22, calculated under appropriate reverse-bias conditions.

At high frequencies, the net effect of the distributed capacitance C_1 is to shunt the ac signal to ground and cause excessive phase lag. Figure 3.24 shows the typical frequency response of a diffused resistor in terms of the magnitude of its driving-point impedance. Assuming that the capacitance C_1 is uniformly distributed along R_1 , one can show that the magnitude of the driving-point impedance Z_{in} is down by approximately 3 dB at a frequency f_1 given as

$$f_1 \approx \frac{1}{3R_1C_1} \tag{3.13}$$

Replacing the total resistor and capacitor values by the sheet resistance R_s and the capacitance C_o per unit area of the junction, Eq. (3.13) can be written as

$$f_1 \approx \frac{1}{3R_sC_oL^2} \tag{3.14}$$

Note that f_1 decreases as the square of the resistor length. For a typical 10-k Ω diffused resistor structure ($R_s = 200 \Omega$, $L = 50 \text{ mil}$, $W = 0.5 \text{ mil}$), f_1 is approximately 10 MHz.

3.5. PINCHED RESISTORS

The sheet resistivity of a semiconductor region can be increased by reducing its effective cross-sectional area. In a pinched resistor structure, this technique is used to obtain a high-value of sheet resistance from the ordinary base-diffused

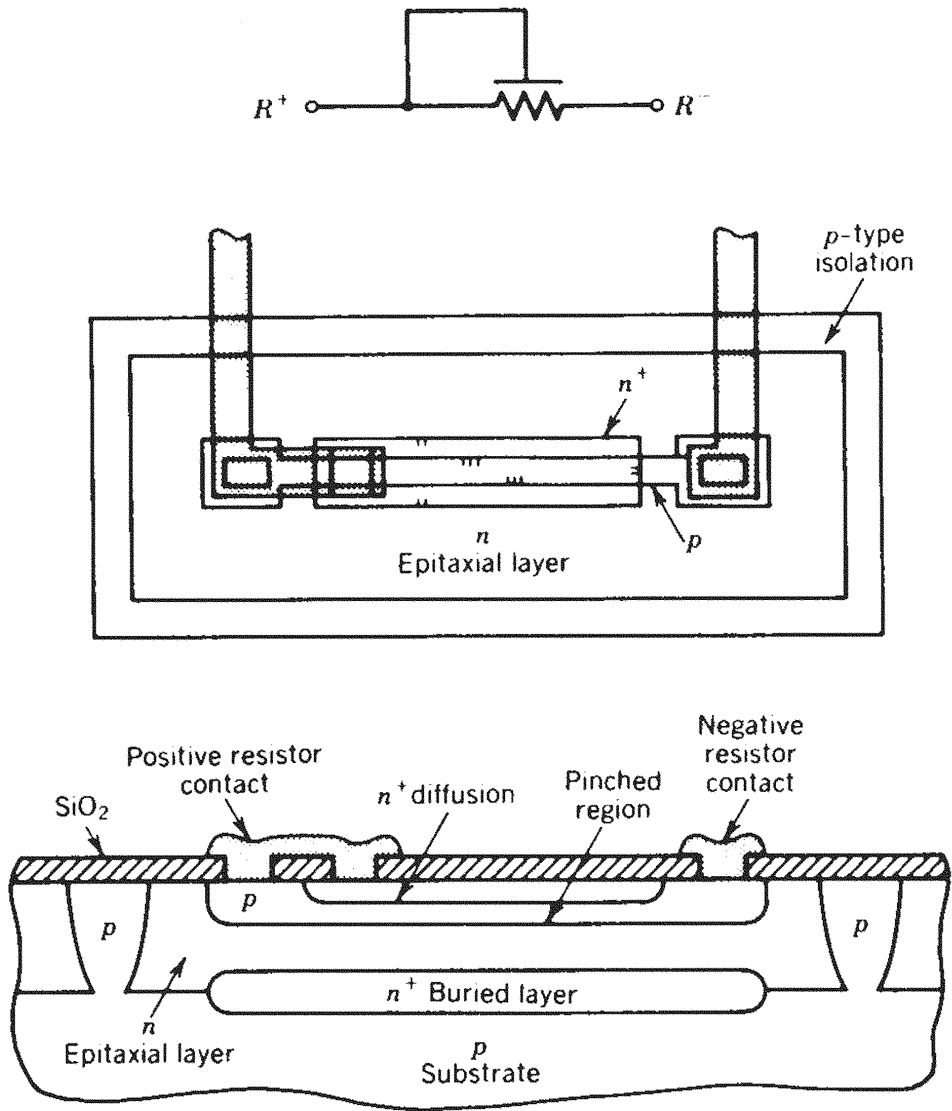


FIGURE 3.25. Layout and cross section of pinched resistor.

resistor. Figure 3.25 shows such a resistor structure formed by placing an n^+ emitter diffusion over the p -type diffused resistor. The emitter diffusion greatly reduces the effective cross-sectional area of the p -type resistor and consequently raises its sheet resistivity. Since the effective area of the resistor is pinched by the n^+ diffusion, such a resistor structure is called a *pinched resistor*.

The sheet resistance R_s of a pinched resistor can be expressed as

$$R_s = \frac{\rho}{x_b - x_e} = \frac{\rho}{W_B} \tag{3.15}$$

where x_b and x_e are the depths of the base and emitter diffusions. The average resistivity $\bar{\rho}$ for the effective cross section of the resistor can be calculated from the knowledge of the diffusion profiles. It should be noted that the effective depth of such a pinched resistor structure is equal to W_B , the $n p n$ transistor base width. Typical values of R_s of a pinched resistor are in the range of 2–10 $\text{k}\Omega/\square$.

It is important that the surrounding epitaxial region be biased within the

breakdown region of the resistor. Therefore, it is very rarely possible to place a base-emitter pinched resistor in an island common with other resistors.

Figure 3.26 shows the circuit designation and the current-voltage characteristics for a pinched resistor. Normally, the n^- and n^+ -type regions surrounding the pinched resistor are short-circuited and connected to the resistor terminal, which is maintained at a more positive potential than the rest of the resistor structure. Such a connection, as shown in Figure 3.26a, ensures that all the junctions forming the resistor are reverse biased. The current-voltage characteristics of the pinched resistor are linear only for small voltage drops across the resistor. In this range of operation, the device behaves as a linear resistor, with the sheet resistivity R_s given by Eq. (3.15). Application of a higher dc voltage results in an increase of the reverse bias between the p -type resistor body and the surrounding n -type island. This reverse bias between causes the junction depletion layer to extend into the resistor and pinch the effective resistor cross section, in a manner similar to the case of a FET. Consequently, for increasing

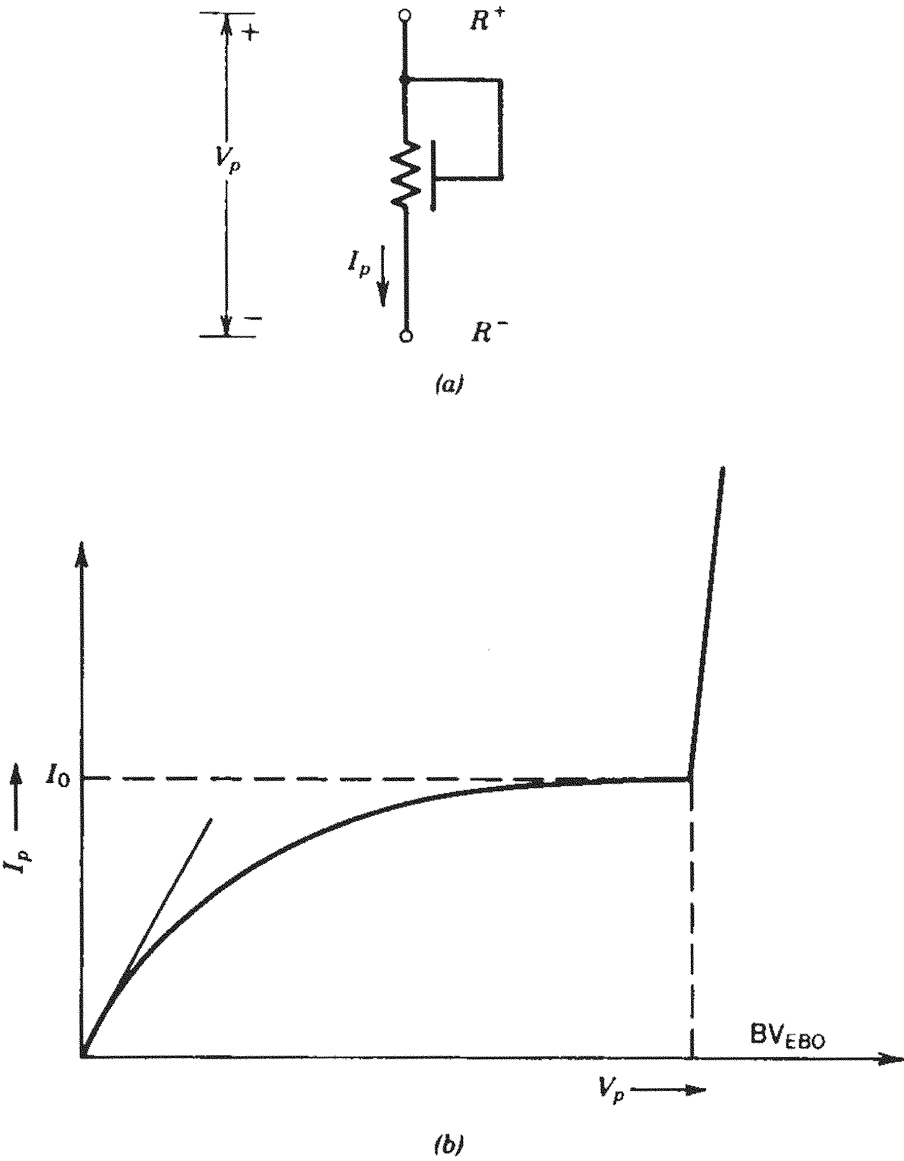


FIGURE 3.26. Pinched resistor. (a) Electrical symbol. (b) Current-voltage characteristics.

voltages, the pinched resistor current I_p tends to saturate to a constant value I_o , as shown in Figure 3.26b. Since the top portion of the pinched resistor is comprised of the heavily doped emitter diffusion, the resistor exhibits a low breakdown voltage, equal to the transistor emitter–base breakdown BV_{EBO} (typically 6–8 V).

The sheet resistance of the pinched resistor structure exhibits a strong temperature coefficient of the order of +3000 to +5000 ppm/°C. The saturation current I_o is also strongly temperature dependent. Its temperature coefficient is almost identical to that of the sheet resistance, but opposite in polarity. Absolute values of the pinched resistors are difficult to control in fabrication. Typical absolute-value tolerances associated with R_s and I_o are in the range of –50 to +80%. However, the matching and tracking of identical pinched resistor structures on the same chip can be held to within $\pm 6\%$. Since the effective thickness of the pinched resistor is the same as the base width of the *npn* transistor, the variations in the absolute values of the pinched resistor tend to track the transistor β variations.

When using pinched resistors, a word of caution is in order. The pinched resistor is a nonlinear element. Thus, tapping a pinched resistor will *not* produce a voltage ratio proportional to the geometric aspect ratio, since the two halves of the resistor will not be biased equally.

3.6. EPITAXIAL RESISTORS

The bulk resistance of the *n*-type epitaxial layer can be used in some applications to form a noncritical high-value resistor. This can be done by using a structure as shown in Figure 3.27. The resulting structure, known as an *epitaxial resistor*. Its sheet resistance can be expressed as:

$$R_s = \frac{\rho_e}{d} \quad (3.16)$$

where ρ_e is the resistivity, and d is the thickness of the epitaxial layer. For a 5 Ω cm epitaxial layer of 10- μ m thickness, this results in a sheet resistivity of approximately 5 k Ω /□.

Since the epitaxial resistor is formed by the epi–isolation junction, its breakdown voltage is also substantially higher than that of the diffused resistor structure. The sidewalls of the epitaxial resistor are formed by the deep isolation diffusion which diffuses sideways as well as downward during the diffusion cycles. When calculating the effective cross section of the epitaxial resistor, the side-diffusion effects should be taken into consideration. Figure 3.28 shows the transverse cross section of a 30- μ m wide epitaxial resistor, fabricated on a 10- μ m thick epitaxial layer, to indicate the significance of the isolation side diffusion on the effective cross section of the resistor. Note that the actual cross section is approximately 35% of the ideal cross section implied by the isolation mask pattern.

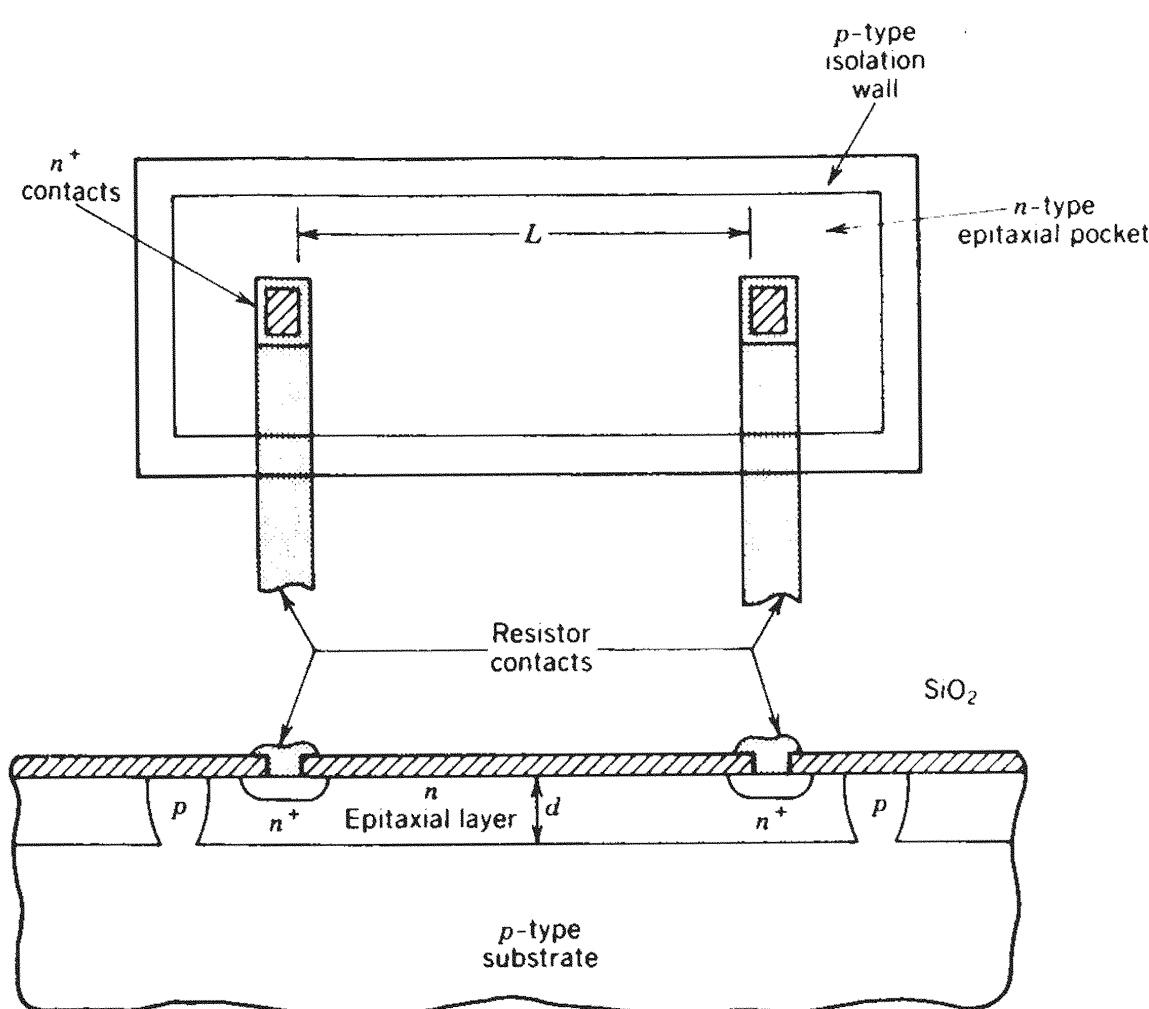


FIGURE 3.27. Layout and cross section of epitaxial resistor.

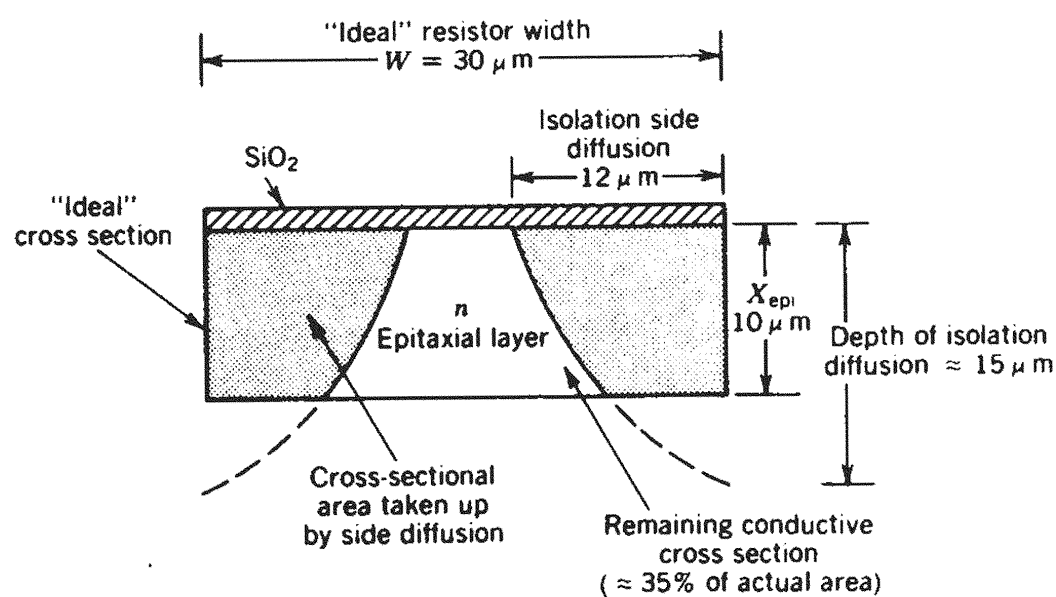


FIGURE 3.28. Transverse cross section of epitaxial resistor showing the effects of isolation side diffusion.

The temperature coefficient of the epitaxial resistor is significantly higher than that of the diffused resistor, due to the strong temperature dependence of mobility at low impurity concentrations. Typical values of the bulk resistor temperature coefficients are in the range of +3500 to +5000 ppm/°C for epitaxial layers of 1–5Ω cm.

The absolute-value tolerances for an epitaxial resistor are quite loose, due to relatively poor control of the epitaxial resistivity ($\pm 20\%$) and the epitaxial layer thickness ($\pm 10\%$). Thus, the practical absolute-value tolerance for a bulk resistor is typically $\pm 30\%$ for resistor widths of 75 μm or more. This tolerance degrades further for narrower resistor structures, due to the side-diffusion effects of the isolation wall illustrated in Figure 3.28.

Epitaxial Pinched Resistors

The conductive cross section of an epitaxial resistor can be reduced further by providing a “blanket” of *p*-type base diffusion over it. The resulting device structure, which is called an epitaxial pinched resistor, is shown in Figure 3.29.

In the case of the epitaxial pinched resistor, the body of the resistor is formed by the *n*-type epitaxial region surrounded on all sides by the *p*-type substrate,

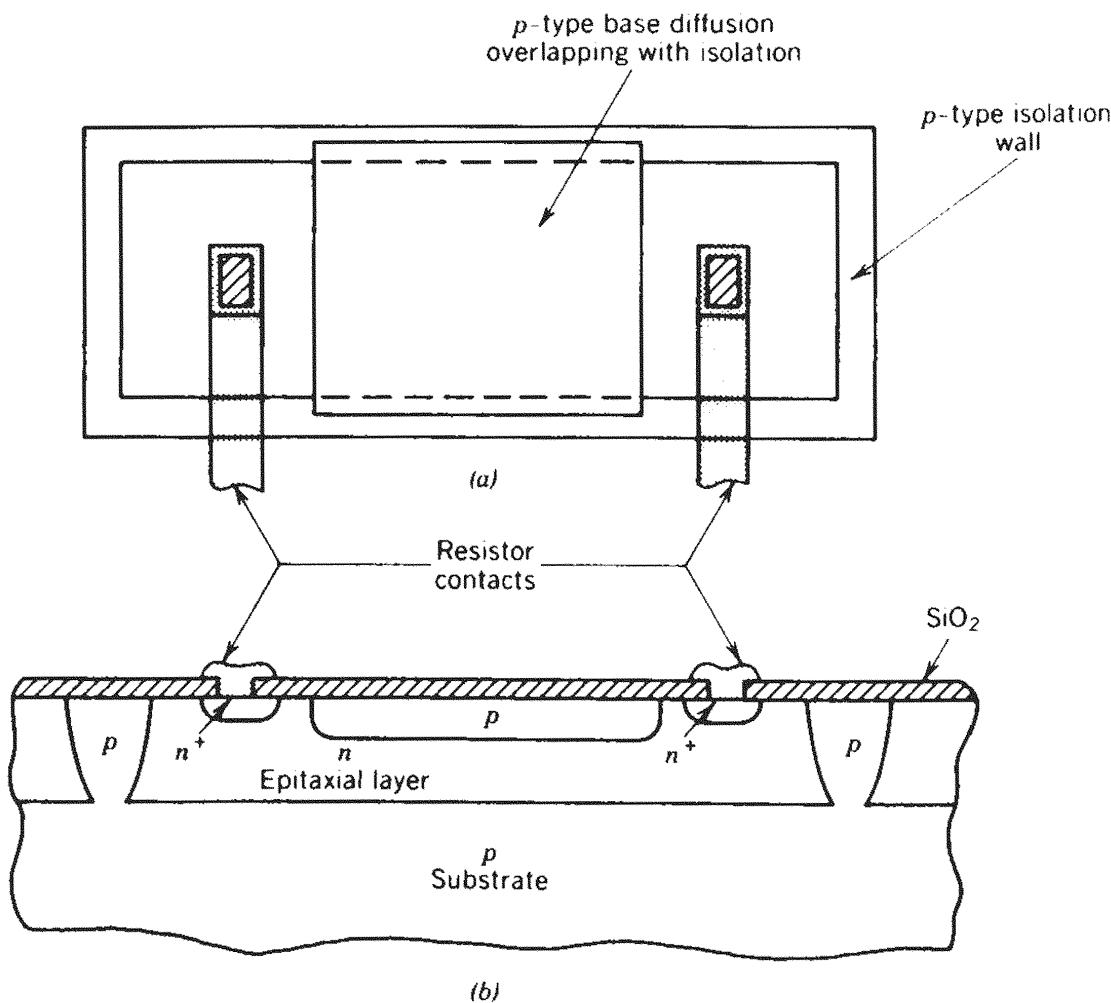


FIGURE 3.29. Epitaxial pinched resistor: (a) Device layout; (b) cross section.

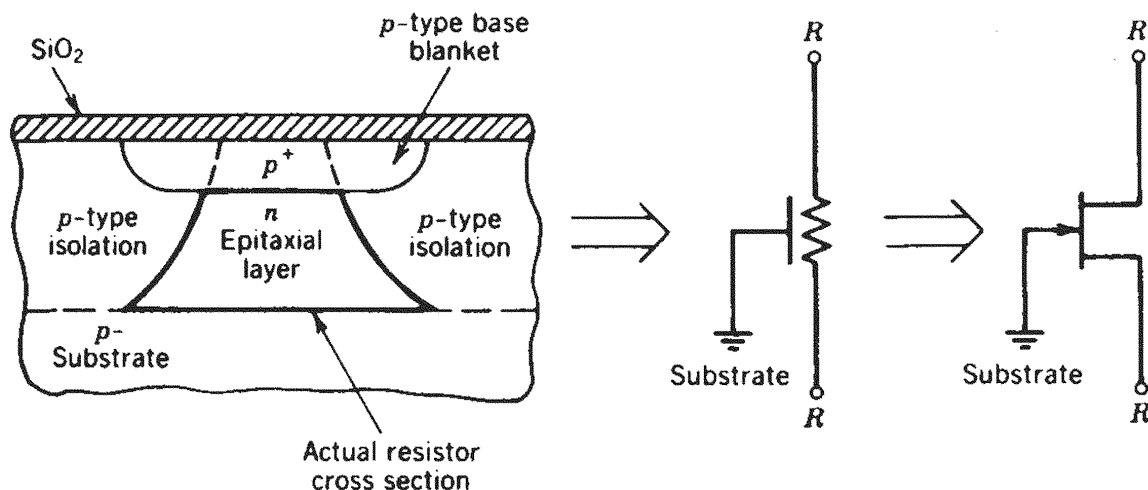


FIGURE 3.30. Effective cross section and electrical equivalent of epitaxial pinched resistor.

isolation, and base diffusion. The sheet resistivity of the resulting device can be expressed as

$$R_s = \frac{\rho_e}{d - x_b} \quad (3.17)$$

where x_b is the depth of the base diffusion, and ρ_e and d are the resistivity and the thickness of the epitaxial layer. For resistivity ranges available in analog circuits, the values of R_s for an epitaxial pinched resistor are in the range of 4–8 k Ω with a temperature coefficient of approximately +4000 ppm/°C.

The epitaxial pinched resistor provides an alternate method of obtaining high-value resistors, without the breakdown limitation of the base-diffused pinched resistor. Its breakdown voltage is basically equal to the base–collector breakdown BV_{CBO} of the n - p - n transistor. The absolute-value and matching tolerances associated with the epitaxial pinched resistor are somewhat poorer than those of the epitaxial unpinched resistor; they are comparable to those of the basic base-diffused pinched resistor.

Figure 3.30 shows the effective cross section of an epitaxial pinched resistor and its electrical equivalent. Note that similar to the case of the normal epitaxial resistor, the epitaxial pinched resistor cross-sectional area is also strongly dependent on the side diffusion of the isolation walls. It is basically an n -channel JFET structure, with the isolation walls, p -type substrate and the p -type base diffusion all together serving as the gate region. Thus, it exhibits nonlinear current–voltage characteristics, similar to an n -channel JFET, with a pinch-off voltage V_p in the range of 25–40 V, depending on the epitaxial layer resistivity and thickness.

3.7. ION-IMPLANTED RESISTORS

Ion-implantation techniques can be utilized to form resistor structures on the semiconductor surface. The fundamental principles of ion-implantation tech-

nology were briefly described in Chapter 1 (see Section 1.7) and are well covered in the literature.⁽⁷⁾ With this technique the impurities are introduced into the silicon lattice by bombarding the wafer surface with high-energy ions.

The implanted ions lie within a very shallow layer (typically on the order of 0.1–0.8 μm) along the silicon surface. Thus, for similar doping levels, the implanted layers yield a sheet resistivity which is roughly 10–20 times higher than a correspondingly doped diffused layer of 2–4- μm thickness.

In fabricating ion-implanted resistors, normally boron-implanted p -type resistor structures are used. For defining resistor geometries, either a thick oxide or an unremoved photoresist layer can be used as a mask. The sheet resistance of the implanted resistor is *inversely* proportional to the implantation dose, that is, the total number of boron atoms implanted per unit area of the resistor surface.

Figure 3.31 shows the planar layout and the cross section of a p -type ion-implanted resistor. Due to the shallow depth of the ion-implanted resistor, it is difficult to obtain a good ohmic contact to the implanted region. Therefore, p -type diffused beds are used at the contact areas of the resistor, as shown. Unlike diffused resistors, ion-implanted resistors are not influenced by the side-diffusion effects. Thus, the true length and width of an implanted resistor is defined accurately by the window size of the ion-implantation mask.

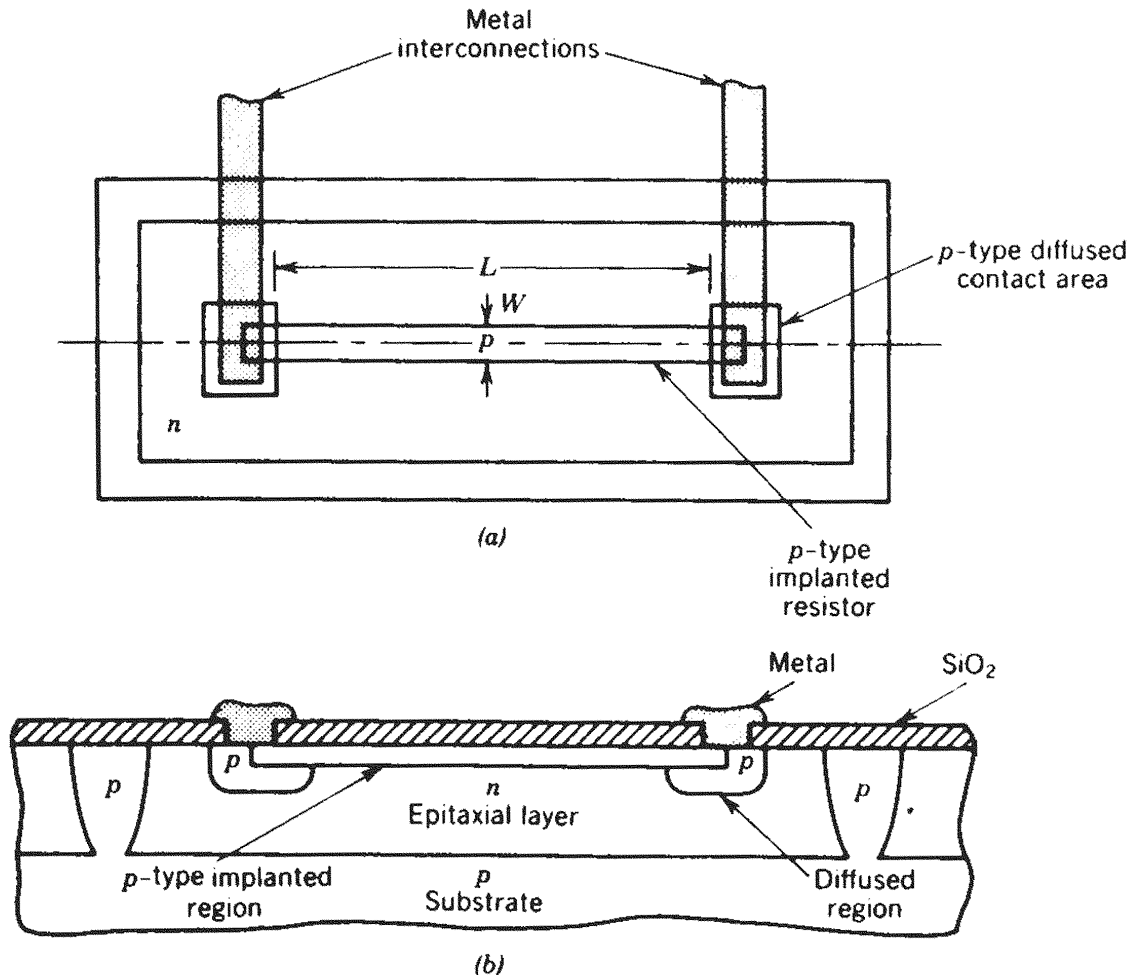


FIGURE 3.31. Lateral geometry and cross section of p -type ion-implanted resistor.

The final value of the sheet resistance is also affected by the post implant annealing time and temperature, since this heat treatment determines the electrical activity of the implanted dopant atoms. By proper choice of the implantation dose and annealing temperatures, sheet resistivity ranges of $0.1\text{--}20\text{ k}\Omega/\square$ can be obtained. Both the implantation dose and the post implant anneal cycles can be very accurately controlled to approximately $\pm 5\%$, and a uniformity or matching tolerance of $\pm 1\%$ can be obtained across the wafer for resistor widths $\geq 25\text{ }\mu\text{m}$. The main contributor to the matching error is, in general, the edge definition of the masking step, rather than the uniformity of the ion implant.

After the implantation step, the implanted impurities can be either partially or totally activated by the post implant heat treatment. The choice of this step profoundly affects the resistor characteristics, as described below:

1. *Partial Activation.* In this process, the wafer is annealed at a low temperature (typically 10–20 min at $500\text{--}600^\circ\text{C}$) and only a small fraction (i.e., 50% or less) of the implanted impurities are electrically activated. Thus, for a given implant dose, one can obtain a range of R_S values by simply controlling the annealing time and temperature.
2. *Total Activation.* In this process, the wafer is heat treated at an elevated temperature (typically 10–20 min at 900°C) to activate virtually all of the implanted impurities, and only the implant dose is used to control the value of R_S .

The advantage of partial activation is that it results in a lower temperature coefficient of R_S , typically in the range of $+100\text{--}+600\text{ ppm}/^\circ\text{C}$. However, its disadvantage is poor thermal noise characteristics of the resistor and poor long-term stability. For this reason, in most high-volume production processes, the total activation technique is preferred.

The practical values of R_S obtained by the total activation process is in the $1\text{--}10\text{ k}\Omega/\square$ range, with the most commonly used range of values being $2\text{--}4\text{ k}\Omega/\square$. The temperature coefficient of fully activated ion-implanted resistors is relatively high, typically on the order of $1500\text{--}4000\text{ ppm}/^\circ\text{C}$, depending on the value of R_S , as shown in Figure 3.32.

The implanted resistors may also exhibit JFET-like characteristics, that is, become nonlinear, as the voltage across the resistor is increased, due to the pinching off of the resistor cross section by the depletion layer of the $p\text{--}n$ junction around the resistor. Thus, the resistor may exhibit a voltage dependence and appear to have a higher value than nominal, as the voltage across it increases.

Figure 3.33 shows the typical voltage dependence of a $1.5\text{ k}\Omega/\square$ p -type implanted resistor, as a function of applied voltage, for various values of resistor width W . Note that the voltage dependence is much more pronounced for narrow resistors (i.e., $W \leq 15\text{ }\mu\text{m}$) than for wider ones, due to the additional pinch-off effect along the resistor edge.

The voltage dependence is also a very strong function of the implant dose, as shown in Figure 3.34. For low-implant doses of $3 \times 10^{13}\text{ atoms}/\text{cm}^2$ or less,

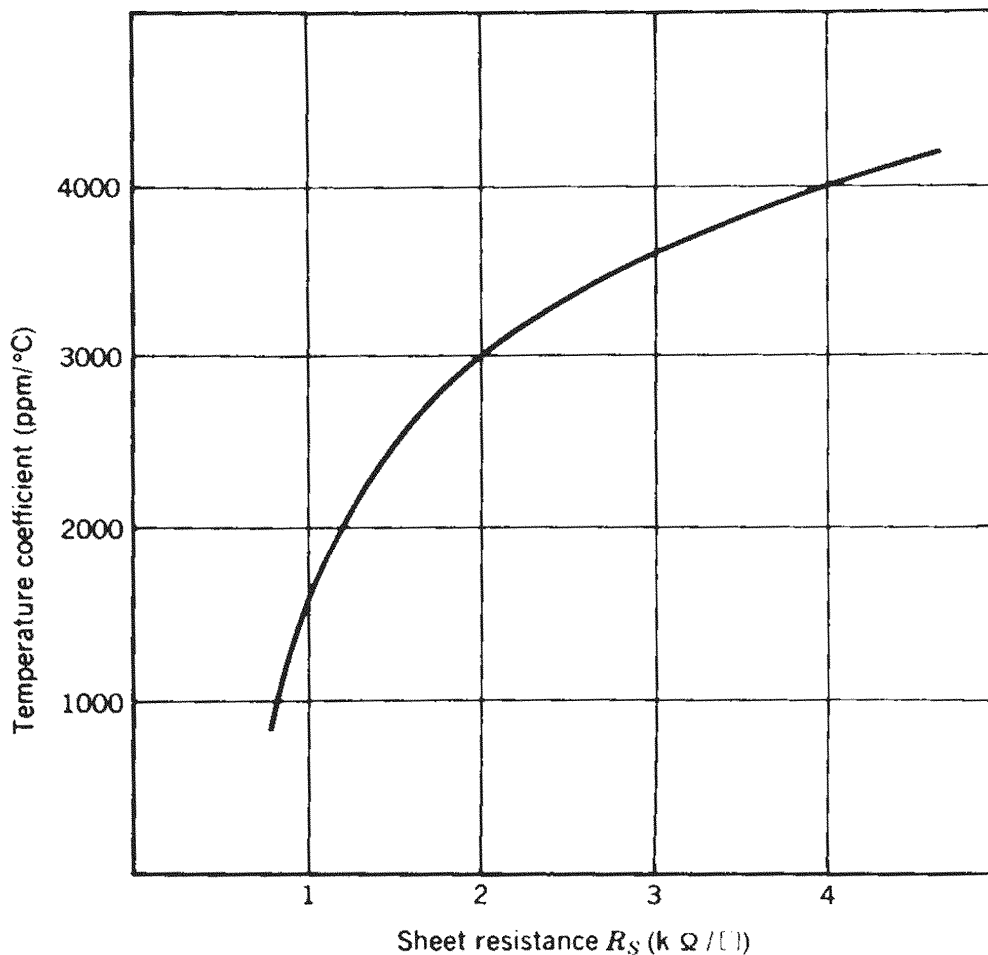


FIGURE 3.32. Average temperature coefficient of *p*-type ion-implanted resistor as a function of sheet resistance. (All impurities are activated.)

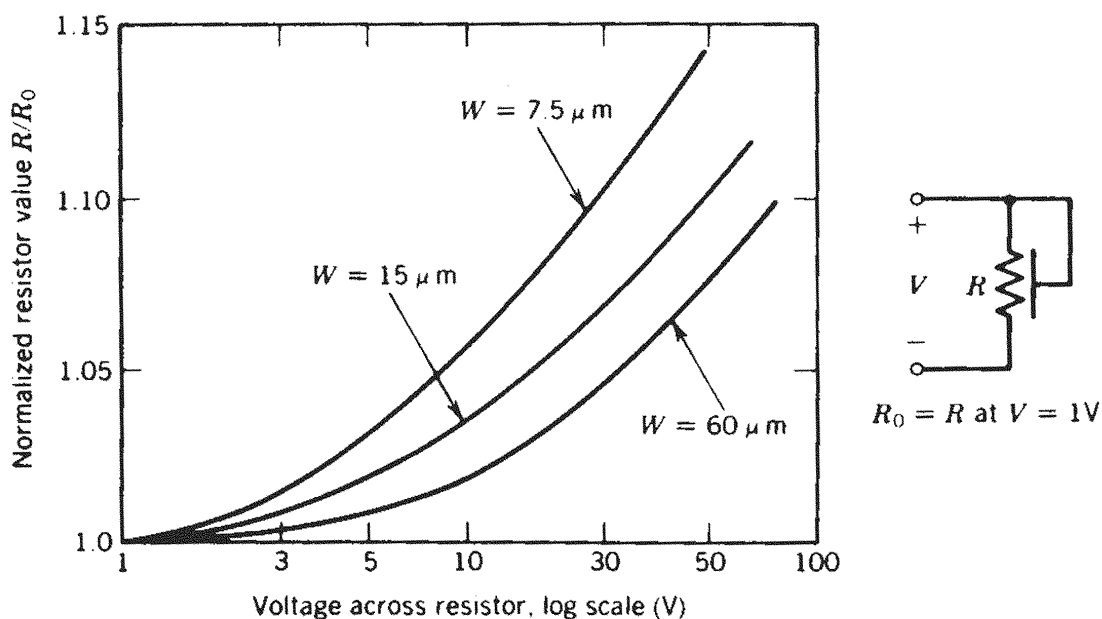


FIGURE 3.33. Voltage dependence of resistor value for boron-implanted $1.5\text{-}k\Omega/\square$ resistor as a function of resistor width.

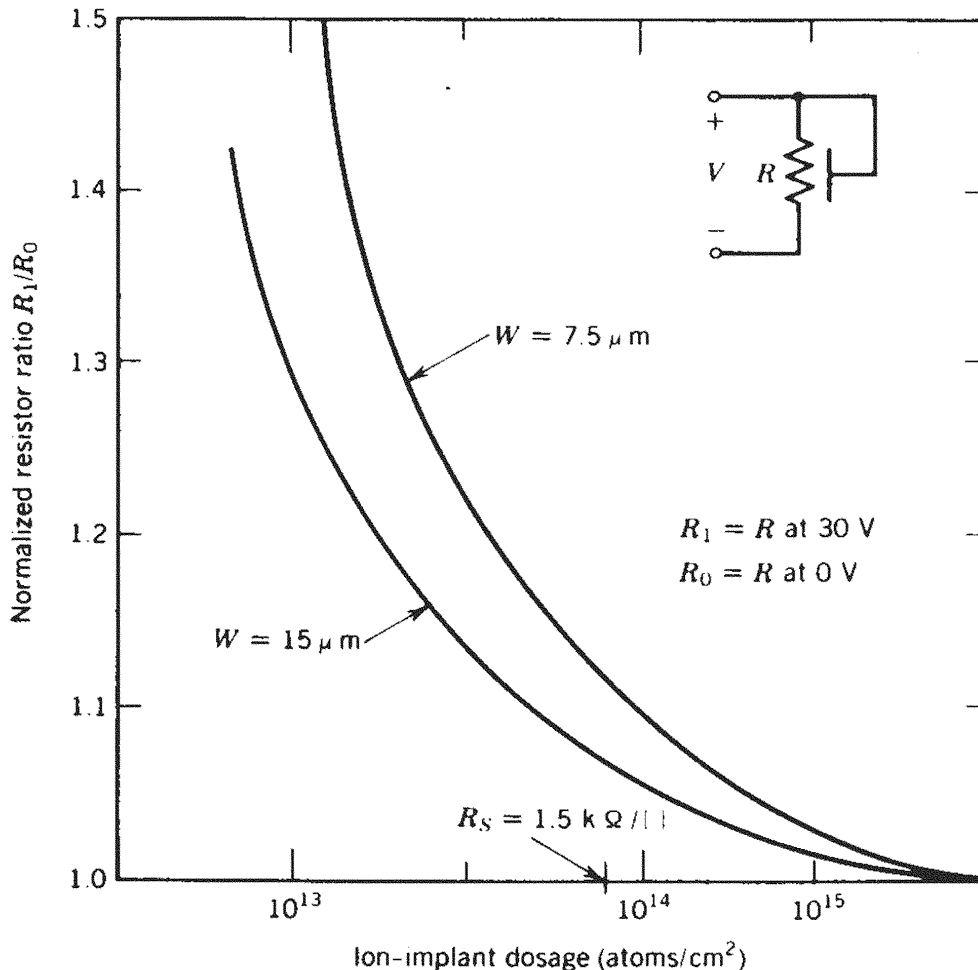


FIGURE 3.34. Dependence of voltage coefficient of resistance on ion-implant dosage for 100-keV boron implant. (All impurities are fully activated.)

which corresponds to $R_S \geq 5 \text{ k}\Omega/\square$, this voltage dependence may become very strong and may lead to complete pinching off of the resistor, causing it to behave as a constant-current source.

3.8. THIN-FILM RESISTORS

Using the film deposition techniques in Chapter 1, resistive thin-film layers can be deposited and patterned on the silicon surface. Compared with the ordinary base-diffused resistors, thin films offer the following advantages:

1. Low temperature coefficient.
2. Tighter absolute-value control by additional trimming steps.
3. Wide choice of sheet resistances.
4. Low stray capacitance.

The main disadvantage of thin-film resistors is the additional process steps required in their fabrication. In some cases, in addition to the basic deposition

TABLE 3.2. Typical Characteristics of Thin-Film Resistors

Resistor Type	R_s ($\Omega/\square$)	Temperature Coefficient (ppm/ $^{\circ}\text{C}$)	Absolute Tolerance without Trim ^a	Matching Tolerance (25- μm wide) ^a
Ta	10–1000	± 100	$\pm 5\%$	$\pm 1\%$
Ni–Cr	40–400	± 100	$\pm 5\%$	$\pm 1\%$
SnO ₂	80–4000	0–1500	$\pm 8\%$	$\pm 2\%$
CrSiO	30–2500	± 50 – ± 150	$\pm 10\%$	$\pm 2\%$

^aSigma limit is assumed.

and patterning steps, an additional SiO₂ deposition is necessary to stabilize the resistor structure by sealing it off from an ambient atmosphere.

The most commonly used thin-film resistors in integrated circuits are tantalum, nickel–chromium (Ni–Cr), cermet (CrSiO), and tin oxide (SnO₂). Table 3.2 gives a summary of the basic properties of each of these thin-film resistors. Of the four listed in the table, Ta and Ni–Cr films are by far the most widely used.

In the circuit layout of thin-film resistors, zigzag geometries with sharp corners are avoided since these etch poorly during the resistor masking step. Instead, a circular fold, as shown in Figure 3.19*b*, is preferred. An alternative way of eliminating sharp corners in thin-film resistors is to layout a number of parallel strips which can then be connected in series by aluminum interconnections at each end of the strips. The thin-film resistors should also be laid out over a smooth region of the surface oxide layer, with no steps or sudden changes of the oxide layer.

3.9. TRIMMING OF RESISTORS

In a number of applications for precision analog circuits, such as converters or precision voltage references, the absolute-value tolerances associated with semiconductor or thin-film resistors are not acceptable. In those cases, additional steps must be taken to “trim” the resistor, after its fabrication, to meet a given absolute-value tolerance. Some of these methods will be outlined in this section.

Adjustment and Trimming of Semiconductor Resistors

The semiconductor resistors, such as the diffused, pinched, epitaxial, or ion-implanted types discussed earlier, cannot be adjusted, once fabricated. One possible exception to this is the case of partially activated ion-implanted resistors which can have their values lowered by additional heat treatment.

A permanent design change, or iteration, in the value of a diffused resistor requires the change and the retooling of one or more mask layers. In such cases,

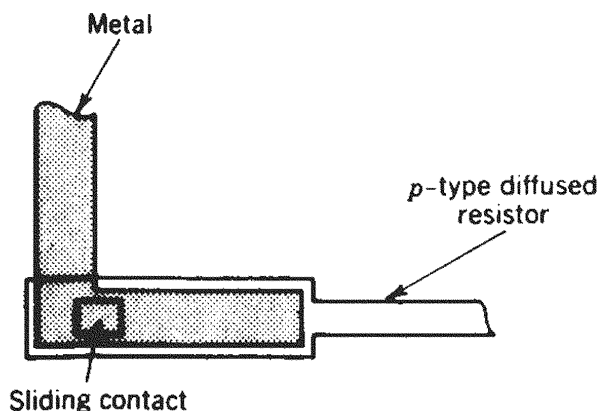


FIGURE 3.35. Resistor end section layout with sliding contact option.

where a possible change is anticipated, the so-called *sliding contact* method illustrated in Figure 3.35 can be used. This is done by providing a large end-area for the resistor, which is then covered by a metal layer. Then if a design change is needed, the value of the resistor can be changed by sliding, or relocating, the contact window. Such a sliding contact method requires only one mask change, and does not affect the diffusion-related mask layers.

Although the semiconductor resistors cannot be directly adjusted, their values can be indirectly trimmed by open- or short-circuiting various prearranged taps on the resistor, usually at the wafer probing stage. This can be done by any of the following methods.

Zener Zapping. This method uses the selective short-circuiting of base-emitter Zener diodes across the resistor taps. When a large current, typically on the order of 200–300 mA, is passed through a small-area Zener diode, the localized power dissipation at the junction reaches such a level that the junction is permanently destroyed. In addition, the metal in the contact window melts and gets swept under the oxide layer and across the silicon surface over the junction. This narrow link of metal fuses into silicon and provides a permanent short circuit across the Zener diode, as shown in Figure 3.36. In the industry jargon, this process is called *Zener zapping*, and can be used for providing a short circuit across one or more of the prearranged resistor taps, as shown in Figure 3.37.⁽⁸⁾ The zapping of the selected Zener diode is done by applying a current and voltage pulse across the selected trim pads during the wafer probing stage. The unzapped Zener diodes remain as open circuits, providing that the voltage drop across their shunting resistor tabs is below the Zener breakdown voltage.

Fusible Links. This technique uses narrow fuse links between prearranged resistor taps. These links initially short-circuit all the taps together, but they can be selectively open-circuited by burning them out. When an excessive amount of current is passed through them, they behave as “fuses” and burn out to form a permanent open circuit. The fuse sections can be made either with narrow and thin aluminum strips ($\approx 5\ \mu\text{m}$ wide and $1000\ \text{\AA}$ thick) or with Ni-Cr resistor segments. Figure 3.38 illustrates how various resistor taps can be open-circuited

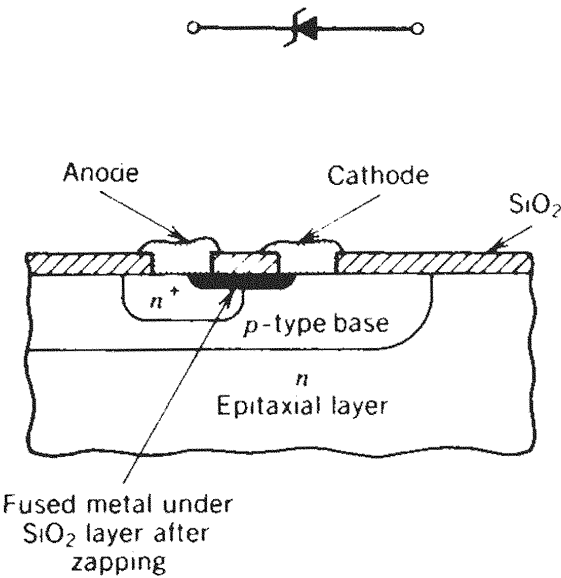


FIGURE 3.36. Cross section of a short-circuited Zener diode after zapping operation.⁽⁸⁾

by selectively blowing such fuse links. Similar to Zener zapping, the blowing of the fuse links is normally done at the wafer probing stage.

Laser Trimming. In this method, a laser beam is used to cut through selected metal links which connect the prearranged resistor taps, as shown in Figure 3.39. Laser trimming is also performed at the wafer probing stage, and is more accurate and reliable than the fusible link technique, since it produces a clean break in the metal link.⁽⁹⁾

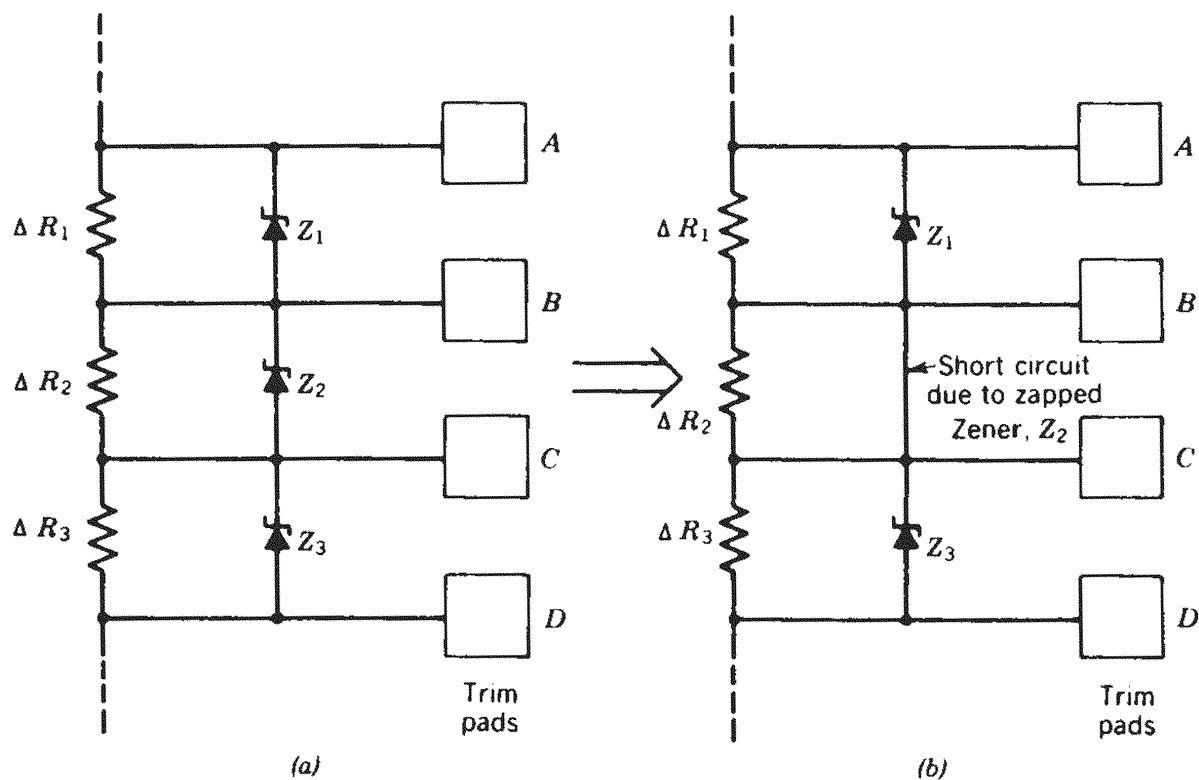


FIGURE 3.37. Resistor trimming by Zener zapping: (a) Before trim and (b) after trim, with Z_2 zapped.

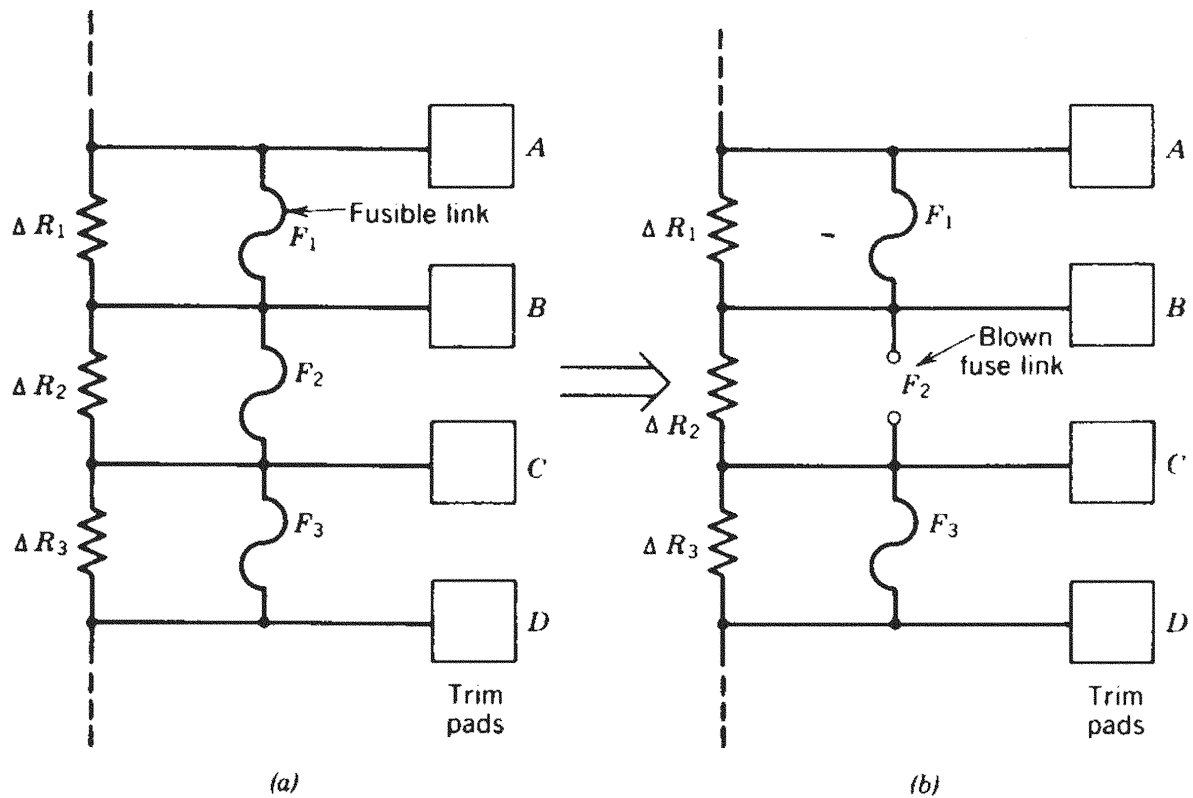


FIGURE 3.38. Resistor trimming by blowing fuse links: (a) Before trim and (b) after trim.

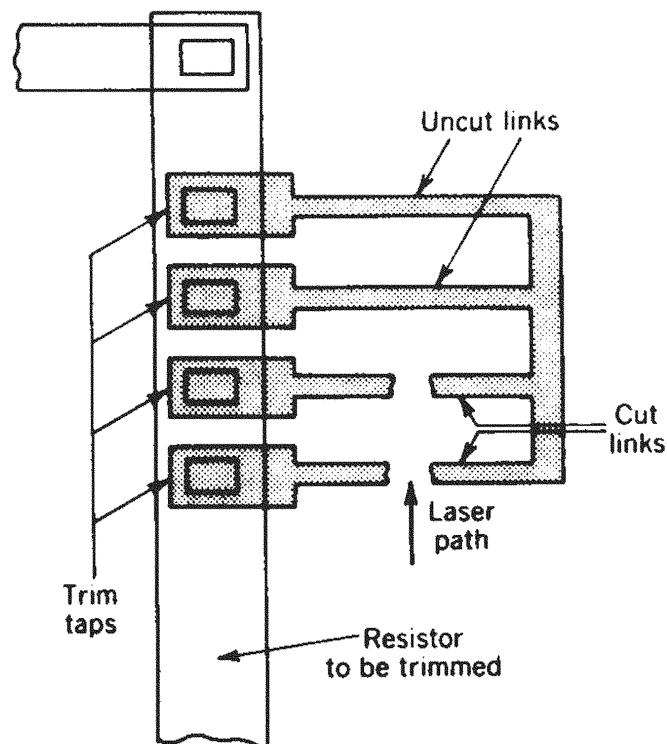


FIGURE 3.39. Laser trimming of resistor by selective cutting of metal links.

Trimming of Thin-Film Resistors. After deposition, the absolute-value tolerances of thin-film resistors can be trimmed to within 1–0.01% of the desired value by means of one of the following methods:

1. *Oxidation.* By heating certain resistor films in an oxidizing atmosphere, some of the material on the film surface can be converted to a nonconductive oxide layer, which increases the total resistor value. This method is generally used for tantalum.
2. *Annealing.* Most thin-film materials exhibit a coarse grain structure after deposition. A subsequent heat treatment, or annealing cycle, causes the grain structure to reorient itself in a more dense fashion and causes the sheet resistance to be lowered. Annealing can be done locally by applying power to the resistor, or by heating it with a laser beam. However, it should be noted that since annealing changes the material structure of the thin film, it also affects the temperature coefficient of the resistor and the tracking of the resistor values over the temperature.
3. *Laser Trimming.* By selectively evaporating a small portion of the thin-film resistor, its effective resistance can be increased. This is normally done by cutting an L-shaped groove into the resistor, as shown in Figure 3.40, by means of a finely focused laser beam (spot size $\leq 1 \mu\text{m}$). This is normally done with an automated test system, while the resistance is continuously monitored. The initial cut is made perpendicular to the direction of current flow. As the resistance approaches the desired value, the direction of the beam is moved parallel to the length of the resistor for fine adjustment of the resistor value. For accurate trimming, relatively wide resistor geometries ($W \geq 50 \mu\text{m}$) are needed. Although laser trimming is an accurate technique for fabricating precision thin-film resistors on monolithic chips, it is a relatively slow and costly step since each precision resistor must be aligned and trimmed individually.

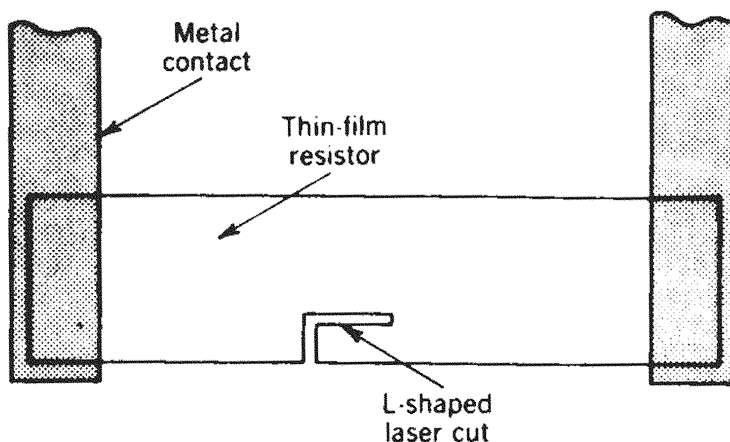


FIGURE 3.40. Trimming of thin-film resistor with L-shaped laser cut.

PART III: INTEGRATED CAPACITORS

The most fundamental limitation on integrated capacitors is size. A general expression for the capacitance of a parallel-plate capacitor can be written as

$$C = C_o A \quad (3.18)$$

where C_o is the capacitance per unit area, and A is the area of one of the plates. The value of C_o is restricted to a narrow range (typically on the order of $0.05\text{--}0.5\text{pF/mil}^2$) due to the type of dielectric materials available in monolithic circuits and their voltage breakdown properties. Thus, the chip area requirement increases quite rapidly with the required capacitor value. As a rule of thumb, for every $3\text{--}5\text{ pF}$ of capacitance value, an amount of chip area equivalent to an isolated small-signal *npn* transistor is used up. Since the practical chip size of a monolithic circuit is dictated by yield considerations, this puts an upper limit on the value of capacitance that can be economically fabricated in monolithic form.

There are two basic classes of capacitor structures available in monolithic circuits: junction and MOS (or oxide) capacitors. The properties of each of these capacitor types are discussed below.

3.10. JUNCTION CAPACITORS

Application of a reverse bias across a semiconductor junction results in the formation of a depletion layer which is devoid of mobile carriers. Figure 3.41 shows an idealized illustration of such a depletion layer formed across a reverse-biased junction. This structure closely simulates a parallel-plate capacitor with an area equal to the total junction area, and with the two plates of the capacitor being separated by the total depletion layer width x . The depletion layer width can be related to the total voltage V , across the junction (i.e., the applied voltage *plus* the built-in potential) by the solution of the one-dimensional Poisson equation.

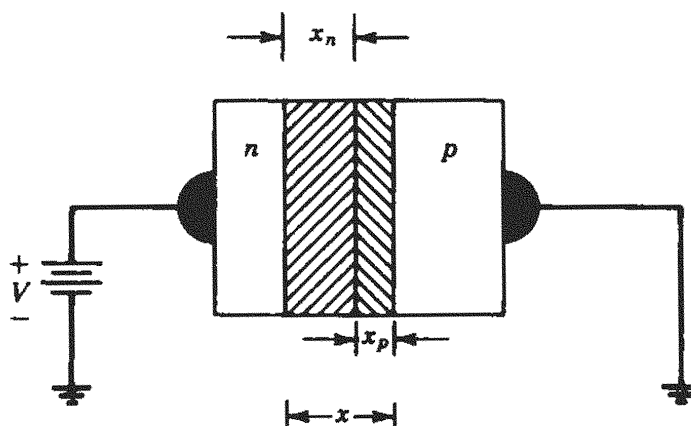


FIGURE 3.41. Idealized illustration of *p-n* junction depletion layer under reverse bias.

tion.⁽¹⁾ It can be shown that the overall charge neutrality conditions require that an equal number of positive and negative charges be depleted on either side of the junction. This implies that the depletion layer tends to spread more into the more lightly doped side of the junction. For a step-junction structure, with uniform impurity concentrations of N_A and N_D atoms/cm³ on the p and n sides of the junction, the total depletion layer width can be related to the total voltage V_i as

$$V_i = V + \psi_o = \frac{q}{2\epsilon} \frac{N_A N_D}{N_A + N_D} x^2 \quad (3.19)$$

where V is the externally applied reverse bias, and ψ_o is the built-in junction potential which depends on the impurity concentration on either side of the junction, and is given by (Eq. 2.31).

The dielectric constant ϵ can be expressed as

$$\epsilon = \epsilon_r \epsilon_o \quad (3.20)$$

where ϵ_o = permittivity of free space ($= 8.85 \times 10^{-14}$ F/cm)

ϵ_r = relative dielectric constant of the insulating material ($= 12$ for silicon)

Thus, in the case of junction capacitors in silicon, $\epsilon = 1.04 \times 10^{-12}$ F/cm. For a step junction, the charge neutrality condition also requires that the total charges on each side of the junction be equal, that is,

$$N_A x_p = N_D x_n \quad (3.21)$$

Since the capacitance per unit area of a parallel-plate capacitor with a plate separation x is given as

$$C_o = \frac{\epsilon}{x} \quad (3.22)$$

the capacitance per unit area of the junction can be related to the total reverse bias V_i across the junction, from Eqs. (3.21) and (3.22), as

$$C_o = \sqrt{\frac{q\epsilon}{2V_i} \frac{N_A N_D}{N_A + N_D}} \quad (3.23)$$

With most junctions, the impurity level on one side of the junction is much higher than that on the other. This is particularly true if one side of the junction, say, the p side, is formed by diffusion into the uniform n background, as is the case with the base-collector junction of the $n p n$ transistor. In such a case, one can still invoke the step-junction approximation with $N_A \gg N_D$. Then Eq. (3.23) reduces to

$$C_o = \sqrt{\frac{q\epsilon N_D}{2V_i}} = \frac{C_{xo}}{\sqrt{1 + V/\psi_o}} \quad (3.24)$$

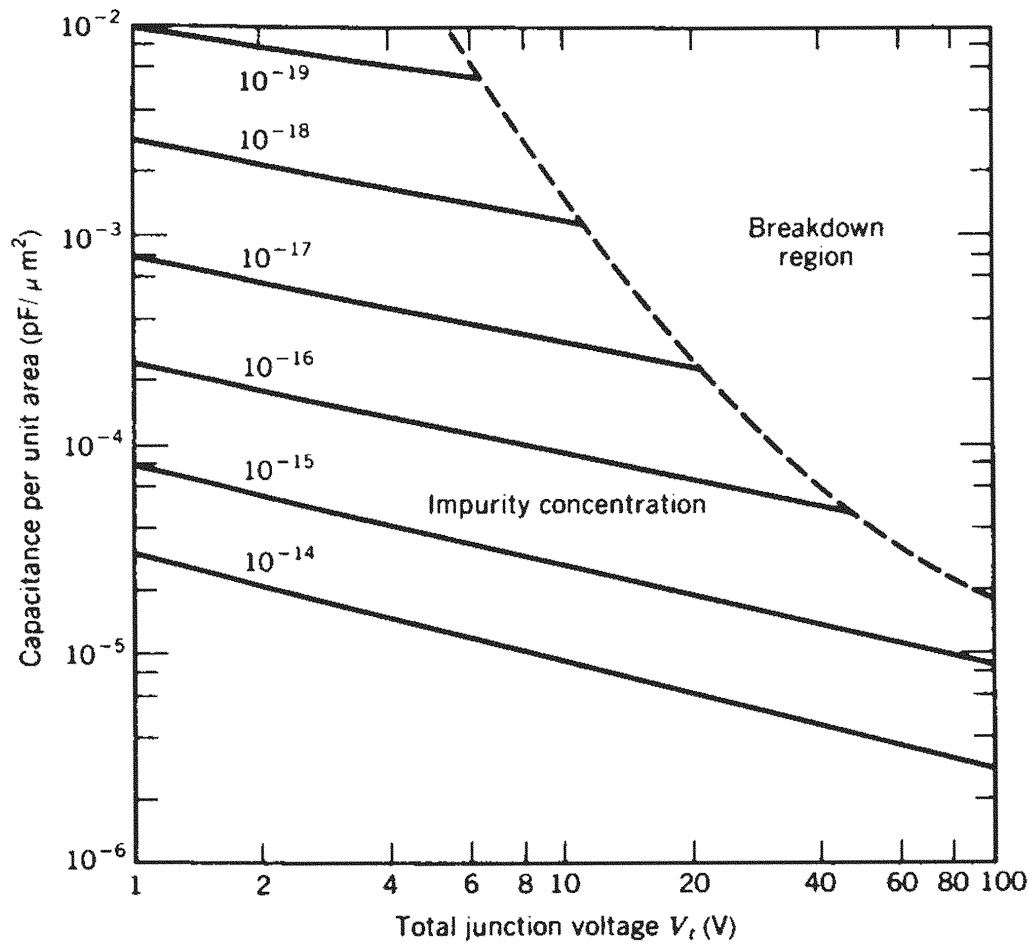


FIGURE 3.42. Capacitance per unit area versus junction voltage for a step junction. (Note: Impurity concentration shown corresponds to more lightly doped side of junction.)

where C_{x0} is the capacitance per unit area of the junction with zero applied bias (i.e., $V = 0$ and $V_t = \psi_o$).

Figure 3.42 shows the capacitance per unit area as a function of the total junction voltage for a step junction, for different values of impurity concentration on the lighter doped side. In general, the voltage dependence of the junction capacitances which can be fabricated with the monolithic IC processes can be described by a generalized version of Eq. (3.24) as

$$C_o = \frac{C_{x0}}{(1 + V/\psi_o)^n} \tag{3.25}$$

where the exponent n is equal to $\frac{1}{2}$ for a step junction, and $\frac{1}{3}$ for a linearly graded junction. For most semiconductor junctions, either the step or the linearly graded junction approximation holds very closely. A detailed family of capacitance versus voltage curves is available in the literature.⁽¹¹⁾

In a planar epitaxial integrated circuit, there are three separate junctions which can be used as capacitors. As shown in Figure 3.43, these are the base-emitter, the base-collector, and the collector-substrate capacitances associated with the integrated *npn* bipolar structure. Also shown is the resultant interconnection of these three capacitors, along with the ideal diodes in shunt

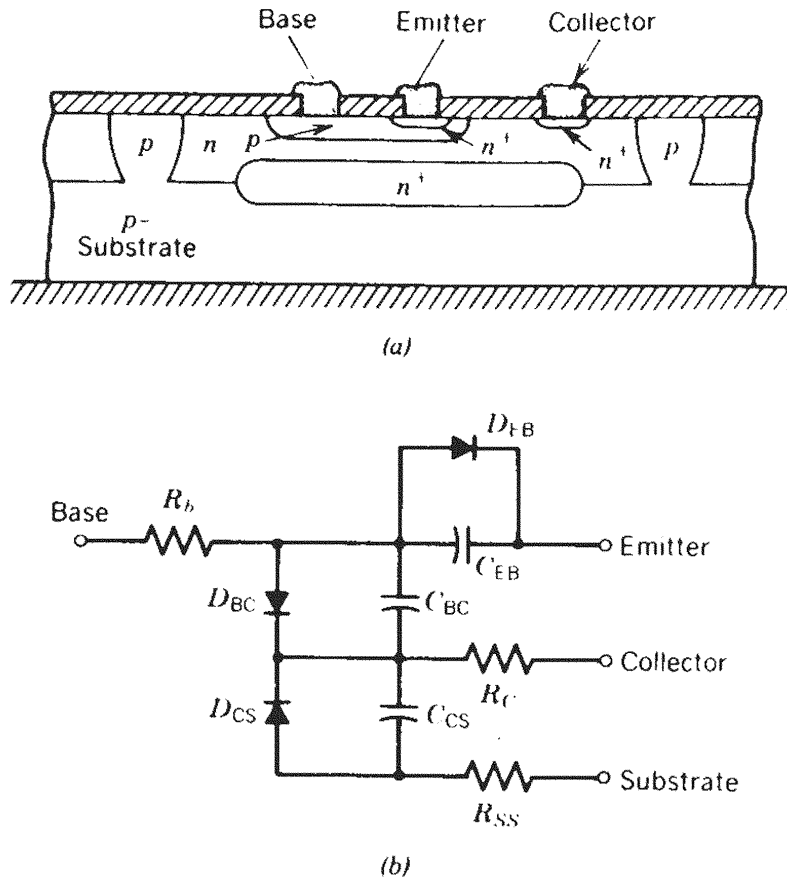


FIGURE 3.43. Junction capacitances in bipolar integrated circuits: (a) Physical device structure; (b) Equivalent circuit of junction capacitances.

with them, to indicate the bias polarity requirements for each capacitor. Note that each capacitance also has a finite bulk resistance in series with it.

With reference to Figure 3.43, the collector–substrate capacitance C_{CS} has only a very limited application since one of its terminals, the substrate, is common to the rest of the circuit and represents an ac ground point. However, C_{CS} is an inherent part of the device structure, and is always present in any junction isolated structure. The remaining capacitances, C_{EB} and C_{BC} , can be eliminated when not needed by omitting the emitter or the base diffusion.

The emitter–base junction offers the highest capacitance per unit area; however, its low reverse breakdown voltage ($\approx 6.5\text{ V}$) limits its use in some applications. The base–collector capacitance finds a wider range of applications than C_{EB} because of its high breakdown voltage (typically $\approx 50\text{ V}$). However, its performance is hampered by the collector series resistance R_C and the shunt C_{CS} to ground. An n^+ -type buried layer can be used to reduce R_C . However, this causes approximately a 30% increase in the value of C_{CS} by increasing the impurity concentration at the epi–substrate interface.

In order to utilize C_{BC} efficiently for ac coupling purposes, it is necessary that the C_{BC}/C_{CS} ratio be kept as high as possible. This can be done by choosing the reverse bias across the collector–substrate junction. In this manner, C_{BC}/C_{CS} ratios in the range of 3–10 are feasible. In the case of dielectrically isolated

integrated circuits (see Fig. 1.14), such bias precautions are not necessary since C_{CS} is negligible.

Table 2.2 gives a summary of the typical junction capacitances associated with each of the three basic junctions available in bipolar monolithic IC structures for various commonly used fabrication processes.

3.11. MOS CAPACITORS

MOS or oxide capacitors are formed by using a thin oxide layer as a dielectric between two conducting surfaces. Normally, the low-resistivity semiconductor region below the oxide layer serves as one plate of the capacitor, and the aluminum deposited over the oxide forms the second plate. Figure 3.44 shows the cross section and a typical layout for such a capacitor structure.

Normally, n^+ emitter diffusion is used as one plate of the capacitor because of its low sheet resistance. During the fabrication process, once the emitter diffusion is made, a special capacitor mask is applied to grow a well-controlled thin SiO_2 layer over the selected portion of the n^+ diffusion. The thickness of this

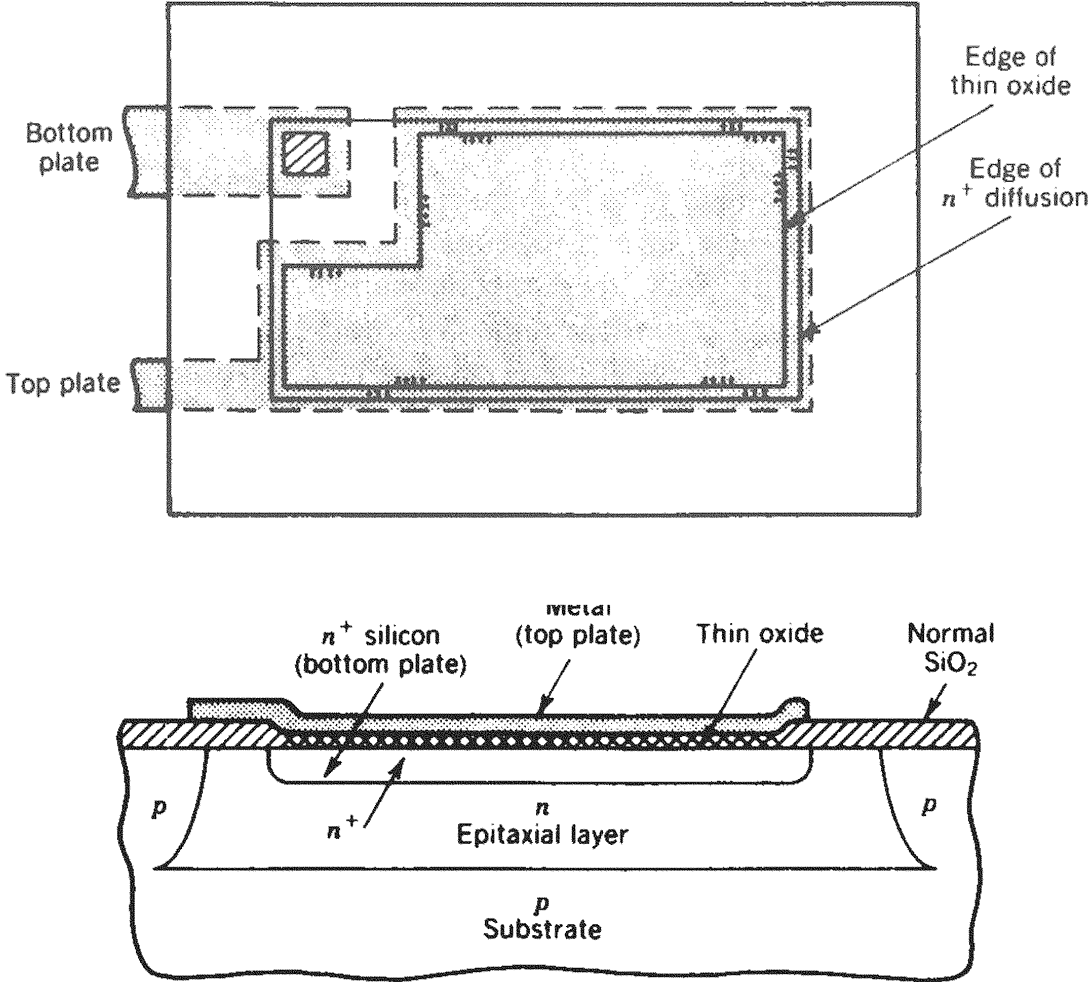


FIGURE 3.44. Typical layout and cross section of MOS capacitor.

SiO₂ layer, which is in the range of 1000–2000 Å, serves as the dielectric thickness of the parallel-plate capacitor. Finally, an aluminum layer is deposited over the thin oxide region, slightly overlapping the oxide, to form the complete capacitor structure.

The resulting capacitor structure has a capacitance per unit area C_o given as

$$C_o = \frac{\epsilon}{t_{ox}} = \frac{\epsilon_r \epsilon_o}{t_{ox}} \tag{3.26}$$

where t_{ox} is the thickness and ϵ_r is the relative dielectric constant of SiO₂. Typical values of ϵ_r are in the range of 2.7–4.2, depending on the growth rate and the purity of the SiO₂ layer.

In certain applications, Si₃N₄ rather than SiO₂ may be used as a dielectric, because of its higher relative dielectric constant ($\epsilon_r \approx 4\text{--}9$), in order to increase the value of C_o . In the case of Si₃N₄, a dielectric thickness of 500–1000 Å is normally used. The lower limit of oxide or nitride thickness is normally set by yield, process control, and breakdown voltage requirements. Normally, Si₃N₄ is not used alone, but in conjunction with an SiO₂ layer to form a two-layer dielectric, thus enhancing breakdown and long-term reliability characteristics of the capacitor.

Figure 3.45 shows the equivalent circuit of the MOS capacitor illustrated in Figure 3.44, in terms of the inherent device parasitics. The resistor R_s represents the access resistance to the bottom plate (i.e., the n -type layer) and is typically of the order of several ohms. C_{cs} is the capacitance of the epitaxial layer-substrate junction, and D_{cs} is the reverse-biased collector-substrate diode. In order to reduce the parasitic effects of C_{cs} , the MOS capacitor is normally fabricated without an n -type buried layer under it.

Unlike their junction counterparts, MOS capacitors can operate with either positive- or negative-polarity voltage applied across the capacitor, and the capacitance value is not voltage dependent. However, MOS capacitors fail by the breakdown of the dielectric layer, when their voltage rating is exceeded. This breakdown is an irreversible (i.e., destructive) failure mechanism, which results

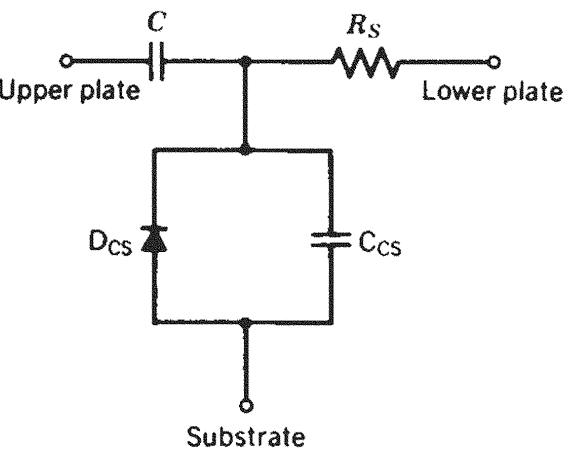


FIGURE 3.45. Electrical equivalent circuit of MOS capacitor.

TABLE 3.3. Typical Characteristics of MOS Capacitors

Device Parameter	Dielectric Material	
	SiO ₂	Si ₃ N ₄
Capacitance (pF/mil ²)	0.25–0.4	0.5–1.0
Relative dielectric constant	2.7–4.2	3.5–9
Breakdown voltage (V)	50–100	50–100
Absolute tolerance (%)	±20	±20
Matching tolerance (%) ^a	±1	±1
Temperature coefficient (ppm/°C)	±20	+4 to +10
Q at 10 MHz	25–80	20–100

^aThe matching tolerance can be reduced to as low as 0.1% by careful device layout.

in a permanent short circuit across the capacitor. Therefore, additional care must be taken in the use of MOS capacitors in the circuit, to provide overvoltage protection in a manner similar to the gate protection of conventional MOS transistors.

Table 3.3 gives a summary of the electrical characteristics of MOS capacitors, using either SiO₂ or Si₃N₄ as the dielectric material. The absolute-value tolerance is normally set by the control of the dielectric oxide or nitride layer thickness. MOS capacitors offer excellent matching characteristics, typically on the order of ± 1%. By careful layout of the capacitor geometry, this matching tolerance can be improved to ± 0.1%.⁽¹²⁾ This feature makes MOS capacitors extremely useful as precision building blocks in D/A converters and switched-capacitor filters, which are described in Chapters 13 and 14.

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