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R.A. Street (Ed.)

Technology and Applications of Amorphous Silicon



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Robert A. Street (Ed.)

Technology and Applications of Amorphous Silicon

With 279 Figures and 20 Tables



Springer

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Preface

Hydrogenated amorphous silicon (a-Si:H) has become an established material in semiconductor technology, led by photovoltaic and active matrix display applications. The primary attribute of the technology is its large area capability, which provides applications that are otherwise unavailable. The extraordinary ability to make devices on one-meter glass plates or long rolls of metal foil is outside the scope of traditional semiconductor manufacturing. A-Si:H exhibits the full range of semiconducting properties, although with lower speed and current compared with single crystal silicon, and the most important devices are thin film transistors and photodiodes. The plasma deposition technology along with the amorphous structure provide a wide set of compatible materials that allows diversity in device design and considerable band gap engineering. For example, a triple solar cell structure (Chap. 6) has 10–12 distinct layers, each specifically optimized to its role.

The book describes both established and emerging applications. Active matrix addressing is ideally suited to a-Si:H thin film transistors, and is applied to liquid crystal displays (Chap. 2), and image sensor arrays (Chap. 4). Such arrays are made with > 10 million distinct a-Si:H devices, a number which compares respectably with any silicon IC. The arrays are embedded in electronic and optical systems, and the chapters describe how the devices interact with the external systems to fulfill their role.

One focus of the emerging technology is the development of novel devices with complex layered structures. Examples are integrated color sensors (Chap. 7) and large area position sensors (Chap. 8). Another focus is the integration of laser recrystallized polycrystalline silicon into the technology (Chap. 3). Polysilicon adds flexibility to the large area technology since, in addition to co-existing with a-Si:H devices on the same array, parts of an individual a-Si:H device, such as the TFT contacts, can be selectively recrystallized. Finally, some revolutionary approaches to the manufacture of devices using printing technology are described in Chap. 5. The expanding range of device options makes the future of a-Si:H and large area electronics look very promising.

As editor I would like to thank the authors for their excellent contributions to this book. I am grateful to the Xerox Palo Alto Research Center for their

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support of the project, and to many colleagues with whom it has been a pleasure to work on this subject.

Palo Alto, 1999

Bob Street

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3 Laser Crystallization for Polycrystalline Silicon Device Applications

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Abstract. Pulsed excimer-laser processing of amorphous silicon on non-crystalline substrates is an important processing technology for large-area polysilicon electronics, such as flat-panel displays and two-dimensional imaging arrays. The technique allows for the creation of CMOS polysilicon on glass substrates, the integration of polysilicon silicon and amorphous devices on the same glass substrate, and the fabrication of self-aligned amorphous silicon thin-film transistors via laser doping. Materials studies show that laser-crystallized polysilicon contains larger grains with fewer defects than polysilicon prepared by other techniques and exhibits large lateral grain growth in a narrow range of excimer laser energy density, with a corresponding peak in the electron mobility. This interesting materials phenomenon provides the opportunity to create excellent polysilicon for device applications, using an appropriate region of parameter space to avoid a non-uniform grain-size distribution and large surface roughness. Also, laser-processing enhancements, such as laser doping and fabrication of self-aligned transistors, provide additional tools to fabricate unique devices. These materials and device processing issues are described, and the device results are presented. For the devices, emphasis is placed on homogeneity and stability as well as on important performance parameters, such as thin-film transistor mobility and leakage currents.

3.1 Introduction

Over the last decade, interest in polycrystalline-silicon (poly-Si) devices has been driven largely by the rapid growth of large area electronic systems, specifically, flat-panel active-matrix displays and two-dimensional imagers [3.1–21]. Currently, amorphous silicon (a-Si) is the semiconductor used in the electronics of these large area systems, since it can readily be deposited on large glass substrates and processed into thin film transistors at low temperatures. By low temperature is meant below about 600°C which is a typical softening point of the glass substrates used for the large-area systems. This can be increased somewhat for the newer glasses, such as Corning 1737, which has a softening point of 660°C [3.22]. In any case, the separation point between high and low temperature processing is in the vicinity of 600°C, and we will use it to specify the dividing point between the two regions with the understanding that this value is approximate and may be increased somewhat as the substrates improve.

Processing of a-Si is compatible with this low-temperature glass but its low speed and low current carrying capability limit it to pixel switch applications. The driver circuits such as, shift registers, multiplexers, and amplifiers, require the faster performance of crystalline silicon. These circuits are currently external to the flat panel array and require costly packaging to assemble. Polycrystalline silicon has an electron mobility that is several orders of magnitude larger than that of amorphous silicon, typically $\approx 100 \text{ cm}^2/\text{Vs}$ versus $< 1 \text{ cm}^2/\text{Vs}$. This allows poly-Si to be applicable to the peripheral drive circuitry which requires higher speeds and/or higher current carrying capability than amorphous silicon can provide. In addition, poly-Si provides CMOS capability that is missing for a-Si due to its poor p-type device performance. Poly-Si CMOS allows the fabrication of low power-consumption circuits. As a result, poly-Si can provide the functionality and performance necessary for low-power driver circuits that can be fabricated on the glass panel. This architecture reduces the number of external connections, as illustrated in Fig. 3.1, and thereby the packaging costs.

To create the polycrystalline silicon, a variety of techniques have been employed, ranging from direct deposition of poly-Si to laser crystallization of deposited a-Si precursors. The former typically requires temperatures in excess of 600°C to obtain good electronic grade material. As a result, this technique is limited to wafer-sized fused-silica substrates for applications in smaller electronic systems such as projection displays. To be compatible with the glass substrate, the two crystallization processes are thermal crystallization in the solid phase or laser crystallization from the melt [3.17]. The latter is the focus here since excimer-laser crystallization of amorphous silicon is a preferable processing technique, as described in Sect. 3.2.

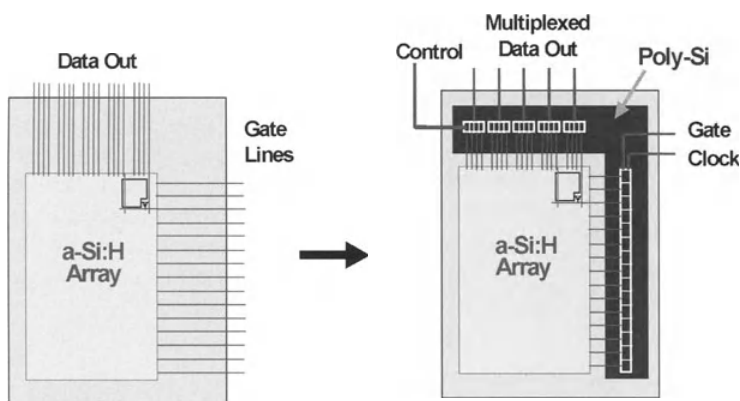


Fig. 3.1. An illustration of the simplified packaging allowed by poly-Si peripheral circuits on an amorphous Si large-area array [3.15]

For a viable laser crystallization process, high quality poly-Si has to be formed over the entire area of the glass plate or edge regions for peripheral circuits. Poly-Si is rich in defects, primarily associated with the grain boundaries. These defects create charge-trapping centers that limit the electrical transport through the material and degrade other device parameters as well [3.23]. Nonetheless, device-grade material can and has been made using laser crystallization and devices with excellent characteristics have been fabricated. The homogeneity of this material and the devices, however, has been problematic [3.25]. The grain size and trap-state density depend strongly on the crystallization and other processing parameters. Any variations in grain size, surface topography, interface structure, and the like translate into variations in the device parameters. Obtaining device-grade material and achieving homogeneity for large-area poly-Si electronic circuits is a major focus of this chapter.

Section 3.2 describes the crystallization process and the properties of the resulting poly-Si material. Emphasis here is placed on excimer-laser crystallized poly-Si. Laser doping of the poly-Si is also discussed. Section 3.3 describes the fabrication and the characteristics of poly-Si thin film transistors (TFTs). Section 3.4 presents a hybrid amorphous and poly-Si processing technique and describes its advantages and the circuit results. Section 3.5 concludes this chapter with a brief discussion of applications of poly-Si.

3.2 Laser Processing of Polysilicon

3.2.1 Polysilicon

Until recently, the primary application of polysilicon was in gate electrodes for metal-oxide-semiconductor (MOS) transistors in integrated circuits [3.23, 24]. Now with the rapid growth of large-area electronics and its need for higher performance devices than provided by a-Si, poly-Si is finding another major application. Currently, several of the major display manufacturers have prototype poly-Si display fabrication facilities and have plans to scale these up to mass production capacities of order 100,000 panels per month. These are large-area displays, e.g., 12.1 in, on glass, requiring low temperature processing. This activity is distinct from the smaller-sized projection displays that are currently fabricated on 4 in fused silica substrates by standard high-temperature processing techniques. There is also interest in reducing the processing temperature even further to well below 600°C so that flexible and less expensive substrates such as plastics can be used [3.26].

Growth of Polysilicon. Poly-Si can be prepared by direct deposition onto a substrate or by crystallization of an amorphous Si precursor. The poly-Si prepared by direct deposition exhibits a columnar structure and small grains. As a result, its electrical properties are poor, with low mobilities, typically

about $5 \text{ cm}^2/\text{Vs}$ [3.13]. Crystallization of a-Si precursors, either by solid phase crystallization or by laser crystallization, yields better poly-Si with higher mobilities.

The deposition of the precursor Si films is most often done by chemical vapor deposition (CVD) from silane gas (SiH_4), although sputtered a-Si has also been studied. Two CVD techniques are used: low-pressure chemical vapor deposition (LPCVD) at temperatures near 600°C ($550\text{--}700^\circ\text{C}$) and plasma enhanced chemical vapor deposition (PECVD) at temperatures near 250°C . For LPCVD, the Si deposited in the upper part of the temperature range is polycrystalline, whereas that in the lower part of the range is amorphous. The temperature at which the transition from amorphous to crystalline occurs can be lowered by reducing the silane partial pressure and also by using disilane rather than silane [3.27]. A fully amorphous film is preferred for the precursors since any poly-Si grains present in the starting film provide a large number of nucleation sites for subsequent grain growth during the crystallization of the remainder of the film. This yields poly-Si with smaller grains and a corresponding lower mobility than poly-Si crystallized from fully amorphous precursors.

Films prepared by standard PECVD deposition are amorphous although microcrystalline silicon can be obtained by reducing the silane partial pressure and increasing that of hydrogen gas. PECVD a-Si:H can be used as a poly-Si precursor, but it contains large amounts of hydrogen, about 10 at. % for electronic grade a-Si:H. Since the hydrogen evolves during the crystallization process, it complicates the crystallization but is not a serious barrier. Typically an extra dehydrogenation step is required before PECVD a-Si:H is crystallized. For solid-phase crystallization the dehydrogenation and crystallization anneals can be combined. For laser crystallization, a dehydrogenation anneal or a laser heating at low laser fluences is used to remove the bulk of the H before a high-laser-fluence crystallization step. This avoids film ablation and cracking caused by the rapid evolution of the H during laser crystallization.

Crystallization of LPCVD or PECVD a-Si films on glass substrates is achieved either by solid-phase crystallization (SPC) at temperatures near 600°C or by laser heating. The former technique (SPC) became of interest for TFT work when it was determined that the field effect mobility was an order of magnitude larger than for as-deposited poly-Si, i.e., about 40 rather than $5 \text{ cm}^2/\text{Vs}$ [3.28]. But due to the low temperatures (below $\approx 600^\circ\text{C}$) required by the glass substrates, the thermal-anneal times are too long for a viable manufacturing process. In addition, extra steps of high-dose Si implants [3.29] are often required for the LPCVD-deposited precursors to ensure a fully amorphous starting material for the best grain growth. In addition, the grain structure for thermally crystallized poly-Si is inferior to that of laser crystallized films, as seen in Fig. 3.2 [3.30, 31]. The laser-processed film has large, columnar grains, which have few intra-granular defects. The thermally



Fig. 3.2a,b. TEM cross section of two low-temperature processed poly-Si films on glass, providing a comparison of typical grains from (a) an excimer laser-crystallized film and (b) a thermally-crystallized film [3.31]

crystallized poly-Si, on the other hand, has smaller grains with a variety of intra-granular defects, mainly threading dislocations and stacking faults. These comparisons with laser processing have led to the decline in interest in SPC for poly-Si device fabrication. The current procedure of choice is laser crystallization and so is the process discussed in detail below.

Electrical Properties of Polysilicon. Before discussing laser crystallization, we briefly describe the electrical properties and defects in poly-Si. Although its electrical properties are superior to those of a-Si, grain boundary effects diminish its performance compared with that of single-crystal silicon. The grain boundaries disrupt the periodic structure of the crystallites, presenting discontinuities that restrict the current flow. In addition, they contain broken and strained Si-Si bonds that create trapping states that lie within the Si bandgap. These traps diminish all the important TFT parameters, namely, the mobility and subthreshold slope are lowered, the threshold voltage and leakage current are increased, and the stability is diminished.

The effects of these traps and barriers at the grain boundaries on the conductivity and mobility have been thoroughly studied for doped poly-Si [3.23]. The variation in the mobility of the carriers at room temperature as a function of doping level is shown in Fig. 3.3 [3.32]. The remarkable feature in these data is the minimum in the mobility that is not seen in single-crystal Si. This minimum is due to the effects of the poly-Si grain boundaries. As carriers are introduced into the poly-Si through doping, the free carriers become trapped at defect sites at the grain boundaries and are depleted from the grains. This causes the height of the electronic barrier at the grain boundaries, V_B , to increase with doping level as more charge is localized there. In addition, these carriers are immobilized by the traps at the grain boundaries and are lost to the conduction process. The barrier height increases with doping concen-

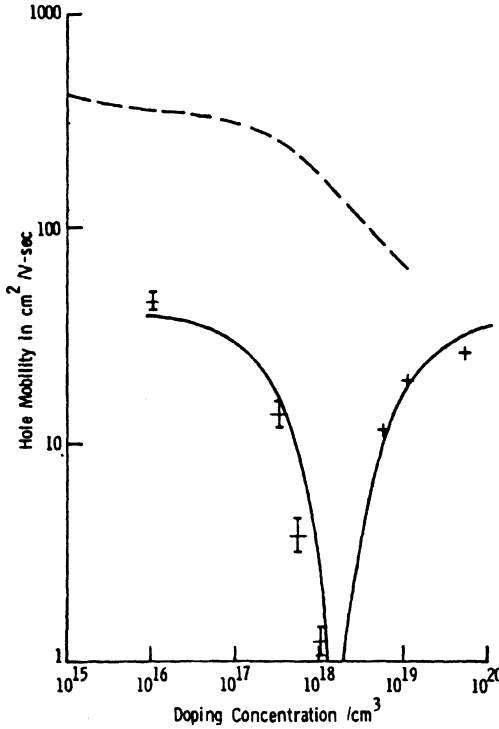


Fig. 3.3. The variation in the room-temperature Hall mobility of the carriers as a function of B doping level in polysilicon (data points) compared with that in single-crystal silicon (*dashed line*) from Seto [3.32]. The *solid line* is the theoretical calculation for poly-Si described by the model of Fig. 3.4

tration, N_d , until all the traps, of density N_T , are filled. For $N_d > N_T$, the additional carriers added by doping screen the trapped charge with the result that the barrier height drops with increasing doping concentration. This is shown schematically in Fig. 3.4 for a one-dimensional model with grains of length L [3.23].

In this model V_B is maximum at a carrier concentration of $N_d = Q_T/L$, where Q_T is the number of traps per unit area of grain boundary. The grain boundary is assumed to be of negligible thickness compared with L . When the carrier concentration is sufficient to fill all the traps, i.e., $N_d > Q_T/L$, then V_B decreases with increasing carrier concentration according to

$$V_B = qQ_T^2/8\epsilon N_d, \quad (3.1)$$

where q is the electronic charge and ϵ is the dielectric constant of poly-Si. From Fig. 3.4 and (3.1), it is evident that one requires large grains (large L) with few defects (small Q_T) for optimal electrical properties of the poly-Si. As a result, the efforts at producing good quality poly-Si have concentrated

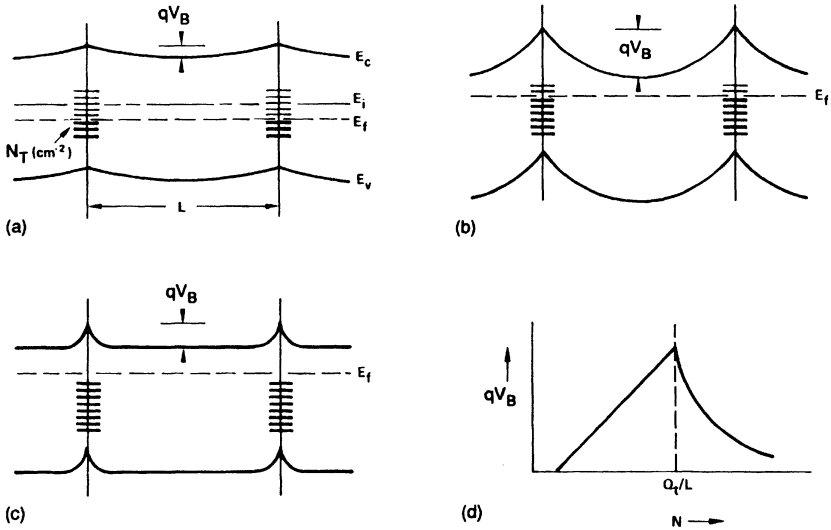


Fig. 3.4a–d. Schematic representation of the height of the electronic barrier, qV_B , at the grain boundaries. As shown in (d), it increases with doping level as more charge is localized there, reaches a maximum at the critical concentration, $N_d = Q_T/L$, and then decreases. Shown also are the energy diagrams for dopant concentrations (a) below, (b) at, and (c) above the critical concentration [3.23]

on these two aspects of the material: (1) creating large-grain poly-Si through growth and re-growth techniques, such as, laser crystallization, and (2) defect reduction through growth and passivation techniques.

Passivation of Defects in Polysilicon. Defect reduction is an important step in the production of device quality poly-Si for TFT applications [3.33]. Creating large-grain material is helpful in this regard, but passivation has the largest effect. Passivating the trap states reduces the deleterious effects of the grain boundaries since, once passivated, they no longer provide active levels within the bandgap to act as traps, thereby reducing Q_T . Since the grain boundary traps are associated with dangling or strained bonds, terminating or modifying them with hydrogen as in the case of a-Si:H and the Si-SiO₂ interface can passivate them. H passivation reduces the number of trap states, as shown in Fig. 3.5 [3.34] for laser-crystallized poly-Si. The dangling-bond spin density varies from 1 to $6.7 \times 10^{18}/\text{cm}^3$ in as-crystallized poly-Si for the different processing conditions used. The minimum in each of the curves corresponds to a maximum in the grain size as a function of laser fluence. This defect concentration is reduced by at least an order of magnitude for each of these poly-Si films by hydrogen passivation. The as-passivated spin density is about $1 \times 10^{17}/\text{cm}^3$ for all the films, independent of the starting defect concentration. This is a saturation value and is not lowered further by

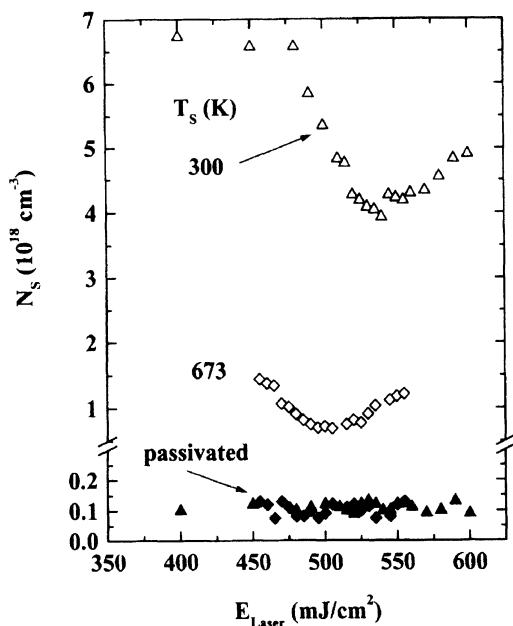


Fig. 3.5. Defect concentration from ESR measurements for laser crystallized poly-Si as a function of laser fluence before (*open symbols*) and after passivation (*solid symbols*). The triangles and diamonds represent data from samples crystallized at two different substrate temperatures (300 K and 673 K, respectively). The minimum in each of these curves corresponds to a maximum in the grain size. Hydrogenation was achieved by exposing the samples to monatomic hydrogen at 350 K for 2 h [3.34]

additional hydrogenation. A similar saturation level of defects of $10^{17}/\text{cm}^3$ is obtained for as-deposited poly-Si when optimized hydrogenation conditions are used [3.35]. This hydrogen passivation process reduces the number of traps, thereby reducing the number of trapped carriers. This causes a lowering of the grain boundary barrier height, V_B , and a corresponding improvement in conductivity and mobility. As a result, hydrogen passivation is a vital step in the production of poly-Si devices with good electrical properties as discussed in Sect. 3.3.

3.2.2 Laser Crystallization

Crystallization of a-Si using continuous wave lasers has been studied extensively in the past [3.36], but is incompatible with low-temperature substrates, since the film and substrate temperatures are heated to well above 600°C . A pulsed laser, on the other hand, provides the means of melting the Si film rapidly enough [3.37] that a low-temperature substrate is not damaged. Using UV light is also advantageous since it is highly absorbed in the Si film rather

than the substrate. As a result, the most commonly used laser crystallization technique for a-Si on glass is performed with pulsed rare-gas halogen excimer lasers.

Excimer Laser. The short wavelength, high intensity, and short pulse length characteristics of the excimer laser make it a favorable tool for crystallizing amorphous silicon on glass substrates [3.38]. The short wavelength in the ultraviolet (308 nm for a XeCl excimer) ensures that the high laser energy is absorbed in the thin silicon film and not the substrate. For example, the absorption depth in silicon is about 7 nm for a XeCl excimer radiation, compared with a typical film thickness of order 100 nm. Also the reflectivity of Si in the UV varies only slightly with temperature and phase. The reflectivity at 308 nm is $\approx 60\%$ for crystalline Si and $\approx 70\%$ for liquid Si. As a result, there is no complication due to a large and discontinuous changes in the energy being absorbed by the film while it heats up and melts, as is the case of IR laser crystallization.

The short excimer laser pulse length of 20–200 ns, ensures that the silicon film is heated rapidly above the melting point and solidifies quickly, with the heat flowing to the unheated substrate. Typical solidification times are on the order of 100 ns [3.10] and are sufficiently short that low melting point substrates, such as glass, do not have time to flow. Thus excimer-laser crystallization does not melt the substrate and can therefore be used to produce poly-Si on glass, as well as other temperature sensitive materials such as plastic. In addition, it is well suited, due its spatial selectivity, to producing hybrid amorphous and poly-Si material and/or devices in neighboring regions of the same glass substrate. Due to the rapid heat up and cool down of this process, neighboring material and devices maintain their integrity while selected regions are being crystallized. This provides significant simplifications in circuit design, fabrication and packaging for large area electronic devices. With peripheral poly-Si electronics, such as shift registers and multiplexers, the number of external lines that have to be attached to the plate is substantially reduced, along with the packaging costs.

The raw excimer laser beam is spatially non-uniform and rounded. Since the grain growth depends strongly on the laser fluence, a uniform beam is required [3.39–41]. The sought-after beam profile is a top hat or a mesa with steep slopes. To this end, the beam is homogenized using a homogenizer that creates a more uniform beam with a top-hat beam profile. But for currently available excimer lasers and optical systems, the beam is inhomogeneous despite the homogenizer. The homogenizer averages out some spatial variations and creates a top-hat beam profile, but it also produces many interfering plane waves. The interference results in variations in the beam intensity that, for currently used optics, has a spatial frequency of order 10 μm microns, comparable to device dimensions. So even for the best

currently available optical system, non-uniformities exist in the beam profile and these can translate into inhomogeneities in the laser-crystallized silicon.

One method to diminish the inhomogeneity further is to expose each point of the amorphous silicon to multiple shots while the beam is scanned over the film in steps that are smaller than the beam size [3.7, 40, 41]. This multiple-shot crystallization provides a partial averaging of the beam inhomogeneities, but the final pulse at each point is expected to imprint any beam inhomogeneities into the poly-Si.

Heat Flow Analysis. The rapid heating of the film by the laser pulse and its subsequent rapid cool down are described by the heat diffusion equation [3.10, 13]. In one-dimension,

$$\rho C_p (\delta T / \delta t) = \delta / \delta z [\kappa (\delta T / \delta z)] + \alpha I(z, t), \quad (3.2)$$

where z is the distance into the film and substrate. $I(z, t)$ is the energy deposited in a unit area of Si per unit time by the excimer laser, given by,

$$I(z, t) = I_0(t) (1 - R) \exp(-\alpha z), \quad (3.3)$$

where ρ , C_p , and κ are the film and substrate parameters, density, specific heat, and thermal conductivity, respectively. They are each functions of temperature, T , and can differ substantially for the film and substrate. R and α are the optical reflectivity and optical absorption coefficient of the Si film and are functions of temperature and laser wavelength.

Numerical solutions of this heat-flow equation for the case of a thin a-Si film on a glass or fused silica substrate with temperature dependent parameters (specific heat, thermal conductivity, density, and reflectivity) provides useful information and insight into the heating and melting during laser crystallization. A function of interest from these numerical calculations is the temperature profile (temperature versus depth and time) for a given laser pulse. If the laser pulse is ideal with a top-hat shaped spatial profile and a square temporal shape, two parameters, the energy density and the pulse duration, provide a complete description. These two parameters serve as approximate descriptors for pulses of an actual laser beam shape that is typically an asymmetric Gaussian in time and a rounded mesa in space. Some programs, such as LIMP [3.42], provide calculation results using the actual beam temporal profile, $I_0(t)$, as an input function. LIMP is a one-dimensional simulation so it does not take into account lateral heat flow through the silicon between the melted and unmelted areas or the spatial non-uniformities of the beam profile. Nonetheless, it and similar routines provide useful information on the heating and melting process.

Figure 3.6 shows the results of such a model calculation for the case of an actual asymmetric XeCl excimer laser pulse whose full width at half maximum is about 20 ns and whose fluence is approximately 550 mJ/cm². The film is 100 nm of LPCVD a-Si on a fused silica substrate. The film melts

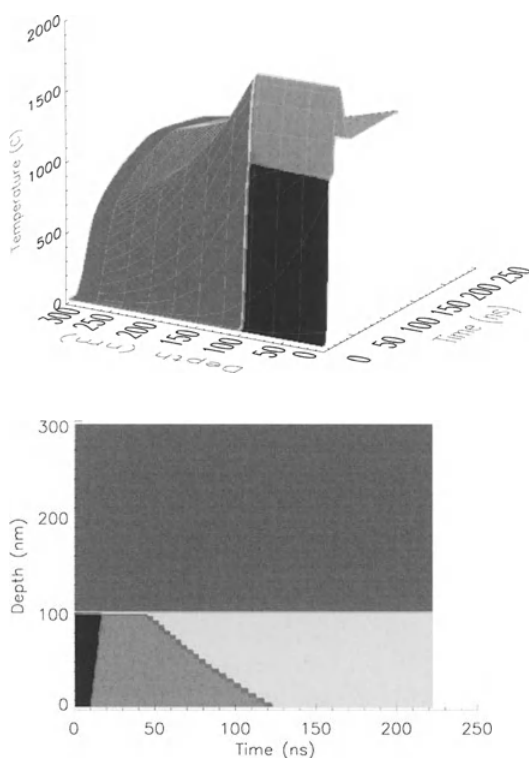


Fig. 3.6. Model calculations using the one-dimensional heat-flow equations for the case of 100 nm of a-Si on a fused silica substrate irradiated by a XeCl excimer laser pulse, 20 ns wide and about 550 mJ/cm^2 in intensity (*black* = a-Si; *gray* = liquid Si; *light gray* = poly-Si; *dark gray* = fused silica substrate)

during the pulse, is superheated well above the melting point of Si, remains molten at the interface for ≈ 30 ns, and solidifies completely in an additional ≈ 70 ns, with a melt-front velocity of $\approx 0.7 \text{ m/s}$. It should be noted that the surface region of the substrate is also heated to above the melting point of Si, thereby exceeding the softening point of glass and even that of quartz. Due, however, to the brevity of this high-temperature state, the substrate material does not have sufficient time to flow and become distorted under normal processing conditions. Extreme superheating can, however, damage the substrate interface, as discussed below.

This value of 550 mJ/cm^2 used in the calculation of Fig. 3.6 is well above the melt-through value for this case of a 20 ns pulse and a 100 nm thick film. The model calculations show that the surface melts at $\approx 100 \text{ mJ/cm}^2$ and the film melts all the way through at $\approx 300 \text{ mJ/cm}^2$. It should be mentioned that the specific laser fluence at which the various phenomena, such as melt

through, occur depends also on the pulse duration and shape. Using (3.2) and (3.3) for the case of a square laser pulse of duration τ , one can derive the threshold energy density to raise the film surface to the melting point to be [3.13]

$$F_T = (T_m - T_0)\rho C_P(\pi D\tau)^{1/2}/2(1 - R), \quad (3.4)$$

where T_m is the melting temperature, T_0 is the film temperature before irradiation, and D is the thermal diffusion coefficient in the film, $D = \kappa/\rho C_P$. This expression shows that the threshold fluence for surface melting varies as $\sqrt{\tau}$ for a square pulse. The expression is different for other pulse shapes, but this result shows the basic variation in F_T with the temporal shape and width of the pulse. In this article we will quote specific values for the fluence at which various phenomena occur. It will be understood that these fluence values are only appropriate for the specific pulse shape and duration used in the measurements, as well as for a given spatial variation.

3.2.3 Grain Growth

Both LPCVD amorphous Si (containing little or no hydrogen) and PECVD a-Si:H (containing about 10 at. % H) have been processed successfully using laser crystallization. In the latter case, the H has to be removed either by a thermal anneal or by a stepped increase in laser exposure [3.39, 46, 47]. In both cases a remarkable phenomenon occurs in the grain growth as a function of laser energy density. During the laser crystallization process, large grains, which can be as large as 100 times the film thickness, can form [3.40–45]. Large lateral grain growth occurs in a very narrow range of laser fluences about a characteristic value, F_p [3.15, 49]. This critical fluence depends on the characteristics of the laser pulse (wavelength, shape, and pulse length) and the film thickness and the thermal properties of the substrate. For example, it is approximately 550 mJ/cm² for an asymmetric Gaussian beam with a full-width at half-maximum of 20 ns and for 100 nm of Si on glass or quartz [3.15]. F_p is one of the three characteristic fluence values that separate the grain growth into four regimes. The other two characteristic fluences are the surface-melt threshold fluence and the melt-through fluence. For the asymmetric Gaussian beam above and for 100 nm of Si on glass, these two fluences are ≈ 100 mJ/cm² and ≈ 300 mJ/cm², respectively, and $F_p \approx 550$ mJ/cm².

At laser fluences below 300 mJ/cm², partial melting occurs and the average grain size is small and heterogeneous, as seen in Fig. 3.7. Below the surface-melt threshold fluence, about 100 mJ/cm², only sample heating occurs and little or no crystallization results (Fig. 3.7a). Above the surface-melt threshold fluence, partial melting of the film occurs. In this case, the grains are larger in the surface region where the primary melt occurs and smaller near the interface where explosive crystallization happens, as seen in Fig. 3.7b–d.

The phenomenon of explosive crystallization has been well studied [3.50–53]. Briefly, explosive crystallization occurs when a rapidly moving (> 10 m/s)

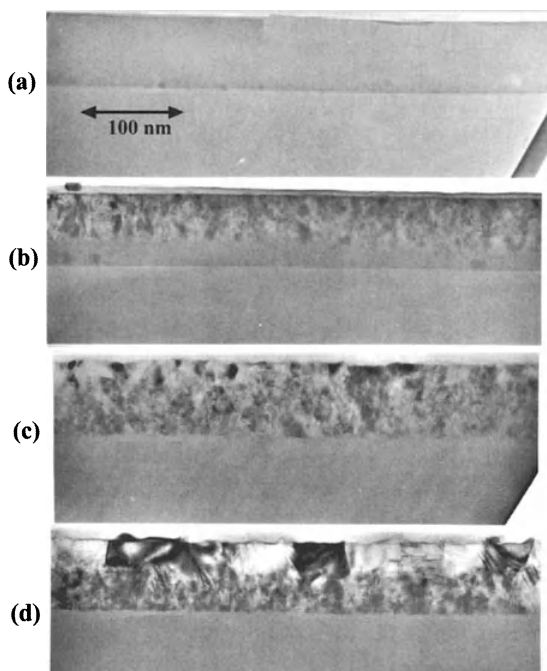


Fig. 3.7a–d. Cross sectional TEM images of 100 nm of laser-crystallized silicon on quartz, showing the heterogeneous structure of the film for laser fluences below the melt-through value. The laser fluences are (a) just below the surface-melt threshold of $\approx 100 \text{ mJ/cm}^2$, (b) 150 mJ/cm^2 , (c) 200 mJ/cm^2 , and (d) 250 mJ/cm^2 , below the melt-through value of $\approx 300 \text{ mJ/cm}^2$. The small-grain material near the interface has been created by explosive crystallization

molten layer propagates through the film, resulting in fine-grain poly-Si. Due to the lower melting temperature of a-Si with respect to that of crystalline Si ($\approx 1400 \text{ K}$ versus 1687 K), the primary melt created at the surface of the film by the absorbed laser pulse is supercooled and, therefore, solidifies into poly-Si. The latent heat released during this solidification heats the underlying a-Si at the interface between the solidifying-liquid and the a-Si solid below. This heat is sufficient to melt a layer of the underlying a-Si due to the larger latent heat of fusion for crystalline Si (1800 J/g versus $\approx 1300 \text{ J/g}$ for a-Si). This thin molten layer is supercooled and, therefore, highly unstable. It solidifies and the process repeats, creating another thin molten layer below that propagates downward into the a-Si film at high velocity, greater than 10 m/s . The rapid cooling and solidification of the Si causes the fine-grain structure.

Above the melt-through threshold ($\approx 300 \text{ mJ/cm}^2$), complete melting of the film occurs. The grains become homogeneous in size throughout the depth

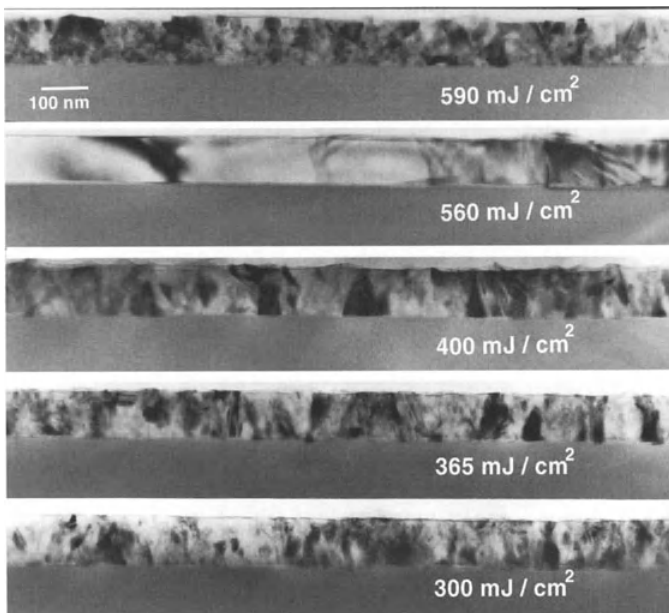


Fig. 3.8. Cross sectional TEM images of 100 nm of silicon on quartz, laser crystallized with 100 laser shots per point for laser fluences above the melt-through value of about 300 mJ/cm² [3.15]

of the film; they have a columnar morphology; and their lateral extent is comparable to the film thickness, as seen in Fig. 3.8 [3.15]. The grain size increases only gradually with increasing fluence. In the vicinity of F_p (≈ 550 mJ/cm²), a rapid increase in the lateral grain size occurs. Grains as large as several microns, or about 100 times the film thickness, can result. Above this peak fluence, the average grain size drops and a heterogeneous mixture of large and small grains is often observed.

Figures 3.9 and 3.10 further document the development of the large grains for the case of a scanned laser beam that is strongly overlapped so that each point of the film is exposed to multiple-laser shots [3.15]. Figure 3.9 shows the laser fluence dependence of the Si (111) X-ray peak intensity, the average grain size from the X-ray results, and the Hall electron mobility for phosphorous-doped material (about 1 at. % P). The peak in the X-ray intensity, observed in the vicinity of 550 mJ/cm², is also evident in the average grain size extracted from the X-ray data and in the Hall mobility measurements. The maximum mobility occurs for the largest grain size, as is to be expected from the discussion above, i.e., due to the fact that the grain boundaries present a dominant scattering mechanism for the carriers in poly-Si.

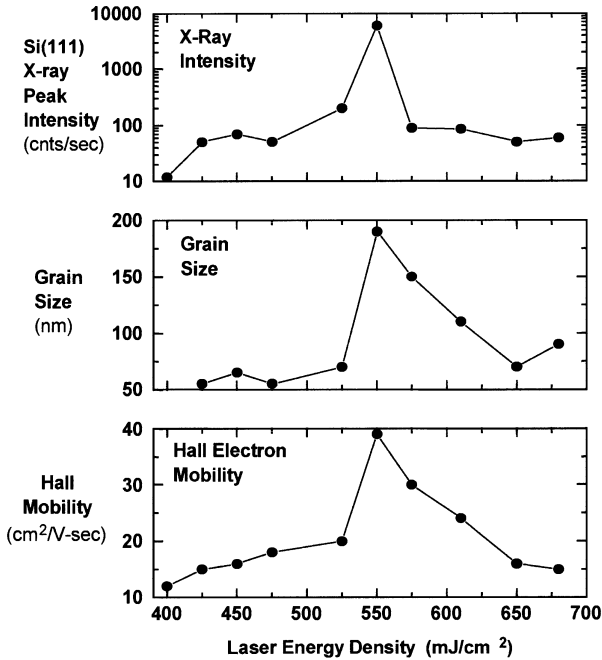


Fig. 3.9. The laser fluence dependence of the Si (111) X-ray peak intensity, the average grain size from the X-ray results, and the Hall electron mobility for phosphorous-doped material, using 100 shots per point for a 100 nm thick a-Si starting film on fused silica substrates [3.15]

The full extent of the grain growth is evident in the TEM cross-sections and planar views of Fig. 3.10 where the peak in the grain size near $F_p \approx 550 \text{ mJ/cm}^2$ is seen directly. Note the large grains in the vicinity of F_p and the smaller grains above and below this laser energy density. The planar views of Fig. 3.10 show that the grains in material crystallized near F_p are greater than a micron in lateral extent, much larger than the film thickness of 100 nm. Note also the narrowness of the region of large lateral grain growth. As is evident in Fig. 3.10, a change in fluence of only 5% above or below F_p leaves the large grain region and creates smaller grains of order of 100 nm, approximately the sample thickness.

This increase in grain size with fluence can be understood in terms of seeded growth from the liquid phase. In the low fluence regime, the film is only partially melted and the amorphous Si below the melt undergoes explosive crystallization that yields fine grain material [3.50–53], as discussed above. The melted portion of the film re-grows vertically into larger grain material, with nucleation sites presumably provided by the material below the primary melt. The two-layer structure of the larger-grain re-grown melt

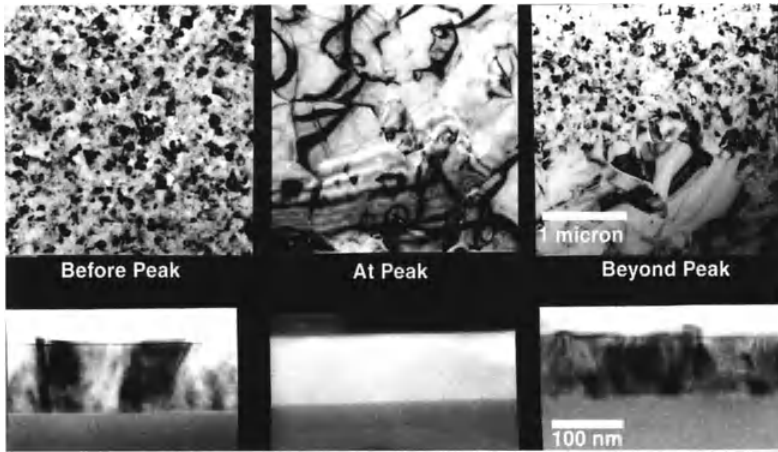


Fig. 3.10. TEM cross sections and planar views of 100 nm of Si laser crystallized below (530 mJ/cm^2), at (550 mJ/cm^2), and above (570 mJ/cm^2) the laser fluence for large lateral grain growth [3.15]

and the finer-grain explosive crystallization layer are readily seen in Fig. 3.7. The fraction of the film that is melted increases with increasing laser fluence. At the melt-through threshold, the entire film is melted and a smaller number of nucleation sites exist. These sites nucleate the grains that grow from the substrate to the surface, yielding poly-Si with a columnar morphology. If the nucleation sites are associated with regions of crystalline order or with actual crystallites at the interface, then the heating provided by the increasing laser energy would be expected to destroy more of these nucleation sites at the film/substrate interface. The decrease in the nucleation site density reduces the number of competing crystals and thereby allows for larger lateral grain growth during solidification and growth from the sparse nucleation sites. At F_p the areal density of nucleation sites has reached a minimum, allowing for a maximum in the grain size [3.41]. The grain growth at this point is still limited since heat loss to the substrate leads to supercooling and the formation of additional nucleation sites [3.44]. The results on 100 nm thick films indicate that the grain size limit several microns.

Beyond F_p , the decrease in grain size at the higher energies can be attributed to a dramatic increase in the number of nucleation sites during the rapid cooling of the molten film. One mechanism is the creation of small grain material by homogeneous nucleation from a supercooled melt [3.43, 44]. It is assumed that all the nuclei at the film-substrate interface have been destroyed at these high laser fluences. For grain growth to begin, nucleation of crystals has to occur. But for these thin films, the cooling rate is high so that supercooling of the melt can result before nucleation. If this supercooling is sufficiently large, i.e., of order 500°C , then copious nucleation can

occur, resulting in small-grain material. In fact, if the cooling rate is even more rapid, exceeding about 10^{10} K/s, then crystallization is suppressed and amorphization occurs [3.50, 54, 55]. It turns out, however, that for pulsed laser crystallization of a-Si on fused silica substrates, this high cooling rate can only be achieved for films thinner than about 24 nm [3.56]. Films 24 nm or thinner can be quenched into the amorphous state, whereas thicker films are either a mixture of a-Si and poly-Si or fully polycrystalline.

In addition to homogeneous nucleation from a supercooled melt, another possible nucleation source in this high fluence regime is the creation of nuclei at the substrate due to substrate damage [3.45, 57]. A roughening of the interface is observed in the TEM cross sections of Fig. 3.10 for the above-peak region for a multiple-shot crystallization. That substrate damage can occur is reasonable since one-dimensional heat flow calculations indicate that the silicon/substrate interface can approach 2000°C at these laser energy densities (Fig. 3.6). Both mechanisms can provide numerous nucleation sites, resulting in the frustration of large lateral grain growth and the production of smaller grain material. For device fabrication, this small-grain material above the peak is undesirable so that crystallization below and near the peak is recommended.

3.2.4 Surface Roughening

Surface roughening also occurs in thin silicon films upon crystallization. Surface roughness in laser crystallized poly-Si has been attributed to the differences in the latent heat and thermal conductivity between polycrystalline and amorphous Si [3.9], to hydrogen evolution in PECVD Si [3.58], to optical interference effects, and to the freezing of capillary waves excited in the molten silicon [3.49]. For the latter model, the volume increase of silicon upon freezing (liquid: 2.53 gm/cm^3 ; solid: 2.30 g/cm^3) can drive the denser liquid silicon toward grain boundaries. This grain boundary region is the last to freeze, and the extra silicon accumulated there is frozen into elevated structures, enhancing the roughness. This effect is most pronounced in the laser fluence regime of large lateral grain growth, i.e., near 550 mJ/cm^2 for 100 nm thick films. The micrographs of Fig. 3.11 show the hillocks formed at the grain boundaries at this fluence. The elevations at the grain boundaries of this large grain material are separated by about $1.5\text{ }\mu\text{m}$ and can be as high as the film thickness.

Atomic force microscopy (AFM) yield results consistent with these TEM data. Fig. 3.12a shows a $5 \times 5\text{ }\mu\text{m}^2$ area of a film crystallized by a single laser shot at $\approx 550\text{ mJ/cm}^2$. The image shows the boundary region between large lateral grains (right) and fine grains crystallized from the supercooled melt (left). The fine grain area has a roughness on the order of 6 nm rms (root-mean-square). The large grain region has a much larger roughness of about 40 nm rms. The areas also show ridges at grain boundaries and hillocks up to 140 nm high at points of confluence for several or more grains. Figure 3.12b

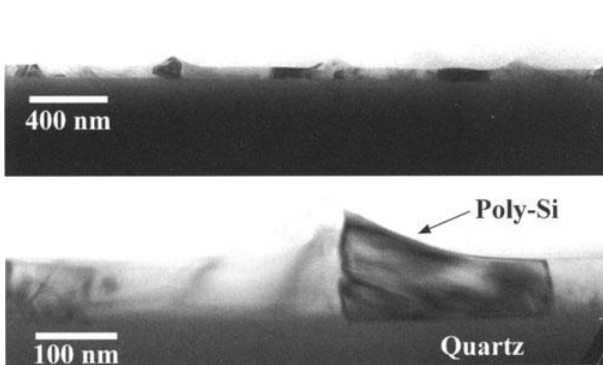


Fig. 3.11. TEM micrographs of 100 nm thick films laser crystallized at 550 mJ/cm^2 , showing the hillocks formed at the grain boundaries [3.49]

shows a $5 \times 5 \mu\text{m}^2$ area of a film crystallized with 100 shots at $\approx 510 \text{ mJ/cm}^2$. The surface is substantially smoother ($< 4 \text{ nm rms}$) and the grains have intra-granular ridges and hillocks. The morphologies are consistent with the large grains in the single shot sample having grown from a single, small nucleus, and the large grains in the multi-shot sample having developed from a distributed nucleus or multiple coherent nuclei (i.e. a partially melted grain). These AFM results show that the rms roughness increases by about an order of magnitude for material crystallized at the fluence of the peak. This large roughness occurs over a very narrow range of laser energy densities, a full width at half maximum of only 30 mJ/cm^2 or a mere 5% of the center fluence. This is the very narrow range of large lateral grain growth discussed above and is a problematic region for device fabrication, since roughness is known to be detrimental to carrier transport [3.59]. As discussed below on Sect. 3.3.2, the adjustment of the processing parameters to avoid this regime yields excellent material and devices with good parameters and uniformity.

3.2.5 Laser Doping

Excimer laser processing provides other unique capabilities in the device-fabrication process, one of which is the doping of the TFT source/drain contacts. The traditional doping process for crystalline silicon is ion implantation, which requires a subsequent thermal process to anneal out the ion damage and to activate the carriers. For low-temperature poly-Si, this is the maximum process temperature, approaching 600°C [3.18]. Recently, it has been realized that laser doping has the potential of simplifying this process and avoiding any high-temperature processing steps [3.10, 60–65]. It provides the possibility of creating self-aligned and short-channel TFTs, as well as lowering the processing temperature. For a-Si TFTs, this process has the added advantage that both crystallization and doping of the S/D contacts

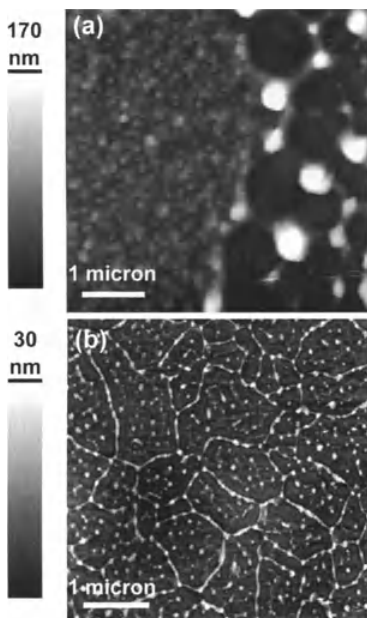


Fig. 3.12. (a) AFM image of the surface of poly-Si crystallized by a single laser shot at $\approx 550 \text{ mJ/cm}^2$. The left half has supercooled to produce small grains, while the right half has undergone large lateral grain growth, forming $\approx 1 \mu\text{m}$ grains and large hillocks. (b) AFM image of 100 shot crystallization at $\approx 510 \text{ mJ/cm}^2$. Ridges and hillocks occur both within and between the grains. In each figure the light regions are the high points [3.49]

can be performed in a single step. Due to the short excimer-laser pulse length, the silicon melts and solidifies in times on the order of 100 ns. These times are, however, sufficiently long to allow for the diffusion of dopant impurities throughout the molten regions of the film. The diffusion length for P in molten Si for this typical laser-processed melt time of 100 ns is about 70 nm, comparable to the film thickness. As a result, the laser crystallization process can be augmented by including a laser doping procedure, thereby reducing the number of process steps in the fabrication of thin-film poly-Si devices. The current laser process for thin-film poly-Si devices involves the laser crystallization of an amorphous silicon film, followed by ion implantation for the source and drain contacts. The implantation step requires a subsequent activation anneal, which, for time considerations, has to be performed as near as possible to the softening temperature of the glass substrate. Laser doping has the potential of simplifying this process and avoiding any high temperature steps. Since the entire process is compatible with low-temperature glass substrates as well as other temperature sensitive materials, the laser crystal-

lization/doping procedure can also be used to produce hybrid amorphous and poly-Si material and/or devices in neighboring regions of the same substrate.

In the laser doping process, a laser pulse briefly melts a surface layer in a doping region, allowing the dopant species to be introduced into the molten material [3.10]. When the molten layer solidifies, the dopant species are distributed and electrically activated in the layer. The source of the dopant atoms can be either a deposited layer, such as a heavily phosphorous-doped or boron-doped amorphous silicon layer [3.65] or a dopant-containing spun-on glass [3.10, 63], or a gas containing the dopant species, such as PF_5 or BF_3 [3.60–62, 64], at the silicon surface. In each case the laser melts the silicon film and the dopant atoms diffuse into the molten region. In the solid-source doping case, the doping source is melted along with the silicon. In the case of gas immersion laser doping (GILD), pyrolysis occurs to disassociate the molecules before dopant diffusion proceeds. This process is illustrated schematically in Fig. 3.13 for the case of a gas-phase dopant source used to dope a silicon wafer [3.66]. An Al mask is patterned and used to shield regions of the Si wafer where doping is not to occur. This is the process appropriate for TFT device fabrication where only the source and drain regions are doped and the channel region remains undoped, being protected by the mask.

Dopant Distribution. Figure 3.14 shows the boron dopant depth profiles measured by secondary ion mass spectrometry (SIMS) for samples doped at three different laser energy densities [3.66, 67]. These data reveal that the doping level and doping depth are both controlled by the laser melting process. Since the boron diffusion coefficient in molten Si is about $\approx 10^{-4} \text{ cm}^2/\text{s}$, which is very fast compared with the solid phase diffusion rate ($\approx 10^{-11} \text{ cm}^2/\text{s}$), the dopant diffusion occurs primarily in the liquid phase. A higher laser doping energy results in a longer melt duration and deeper melting depth which leads to a higher doping level and deeper doping depth. During the solidification, the solid/liquid interface is moving toward the surface and the dopants are diffusing in the opposite direction. The overall effect is that the doping is slightly shallower than the melting depth.

The melt time can be measured directly using the transient reflectivity of a HeNe probe laser (wavelength = 633 nm) during the laser doping process. Since molten Si is a metal, silicon's reflectivity increases by about a factor of about 2 upon melting, from 40% to about 70% at 633 nm. This provides a direct measure of the total melt time. The melt times can be related to the melt depth using heat flow calculations of the type discussed above in Sect. 3.2.2. Good agreement is found between the calculated melt depth and the doping depth measured by SIMS, as in Fig. 3.14 [3.66]. It should be mentioned that the actual dopant profiles are sharper than the measured SIMS profiles due to the finite depth resolution of SIMS from ion mixing. So the doping depth corresponds to the point at which the SIMS concentration deviates from a constant slope. Also with increasing laser energy, the melt

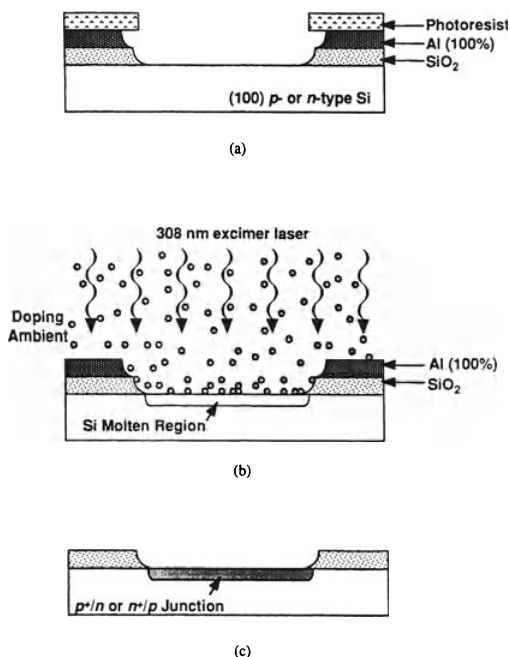


Fig. 3.13a-c. Schematic of the laser doping process for the case of a gas-phase dopant source used to dope a Si wafer. A photomasking step, (a), is required to create a mask, an Al reflector in this example. This defines the regions to be doped by the laser (b). The mask is removed to yield a doped region adjacent to an undoped region, (c), as in a source/drain contact for a TFT [3.66]

duration increases, allowing more dopants to be incorporated in the silicon film.

The results above are for a silicon wafer, but similar results apply for a-Si or poly-Si films on a glass substrate. Figure 3.15 shows the SIMS profiles for 100 nm of poly-Si on quartz, doped with phosphorous by the GILD process using PF_5 gas [64]. This figure shows the P profiles for a laser fluence of 560 mJ/cm^2 , above the melt-through threshold, which from heat flow calculations is about 480 mJ/cm^2 . There is a flat concentration profile throughout the thickness of the film except for a small drop near the substrate, which is pronounced at a low number of laser shots. On the other hand, at 365 mJ/cm^2 , below the melt-through threshold, the phosphorous concentration profiles are not flat throughout the film, as shown in Fig. 3.16. The concentration is seen to fall off at about one decade per 20 nm beyond a depth of 40 nm. This is the approximate instrumental resolution for the SIMS sputtering conditions that were used. So, in fact, the SIMS profile is consistent with a dopant profile that is essentially constant to a depth of about 40 nm (the melt depth at 365 mJ/cm^2), where it falls to the background level of

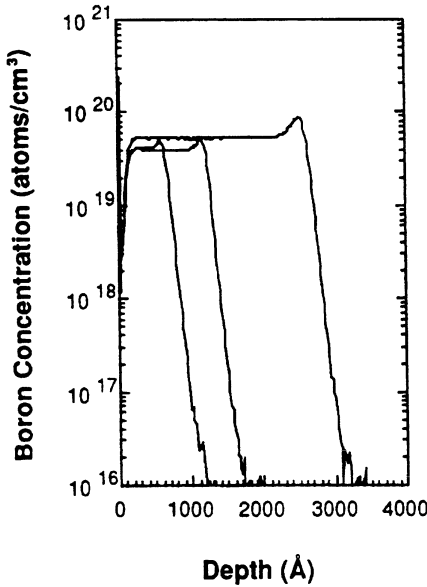


Fig. 3.14. Boron doping profiles in GILD-doped Si wafers from SIMS measurements for increasing laser fluence from left to right of approximately 760, 930, and 1280 mJ/cm² [3.67]

10¹⁸/cm³. Heat flow simulations that agree with the total integrated concentrations are shown in Fig. 3.16. The difference in sharpness of the profiles is due to the finite SIMS resolution.

Electrical Properties. The electrical properties of the laser-doped films are determined using conductivity and Hall effect measurements. Typical results on the sheet resistance versus number of laser shots are shown in Fig. 3.17 [64] for several laser energy densities and for the same experimental conditions of Fig. 3.15 and Fig. 3.16. A typical sheet resistance needed for the source and drain contacts in a poly-Si TFT is about 1000 Ω/□. So these results indicate that approximately 100 shots are required to achieve this value as long as the laser energy density exceeds 400 mJ/cm² for these 100 nm thick films on quartz. For 1000 shots, resistances below 30 Ω/□ are achieved. For lower laser fluences, less efficient doping occurs due to the shorter melt time and a corresponding smaller incorporation time.

The carrier concentration, extracted from Hall measurements, rises almost linearly with shots for the GILD process at a rate of about 2×10^{18} /cm³ per pulse [3.64], equivalent to a phosphorous dose of 2×10^{13} /cm² per pulse. Thus about 100 shots are required to achieve an ion-implantation dose of 2×10^{15} /cm², typical of that used for poly-Si source and drain contacts.

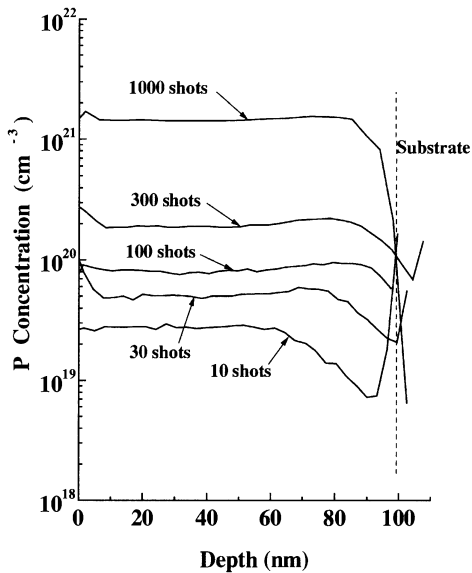


Fig. 3.15. SIMS data showing phosphorous depth profiles in 100 nm thick Si films on quartz substrates, laser doped at a fluence of 560 mJ/cm^2 , above the melt-through threshold, with differing numbers of laser shots [3.64]

The variation of carrier concentration with laser fluence is small and only substantial at low shot densities and laser fluences below 400 mJ/cm^2 . Similar results have been obtained in the case of B for p-type doping.

For GILD, a large number of pulses are required to achieve high doping levels. In fact, the P dopant rate of $2 \times 10^{13}/\text{cm}^2/\text{pulse}$ is two orders of magnitude less than the number of Si surface sites available for a dopant gas molecule to adsorb. As a result, more pulses are required to compensate for the low efficiency per pulse. To dope throughout the entire film thickness, high laser fluences are needed. However, high fluence and large number of shots are the conditions under which film ablation often occurs. To avoid ablation and still heavily dope throughout the film thickness, a two-step GILD doping procedure has been used. In addition, solid source doping yields high dopant levels with only a few laser shots [3.10]. The solid-source doping procedure, however, requires an additional deposition step. This extra step is simplified by using spun-on-glass as the dopant source. Nonetheless, deposited solid sources provide an efficient source of dopants and thereby may be a more appropriate procedure for realizing laser doping for the fabrication of devices with fewer laser shots.

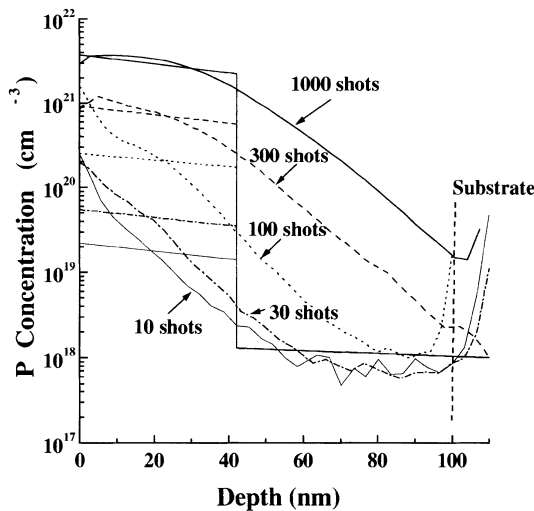


Fig. 3.16. SIMS data showing phosphorous depth profiles in 100 nm thick Si films, laser doped at a fluence of 365 mJ/cm², below the melt-through threshold, with differing numbers of laser shots. Heat flow simulations that agree with the total integrated concentrations are also shown. The difference in profiles sharpness is due to the SIMS resolution [3.64]

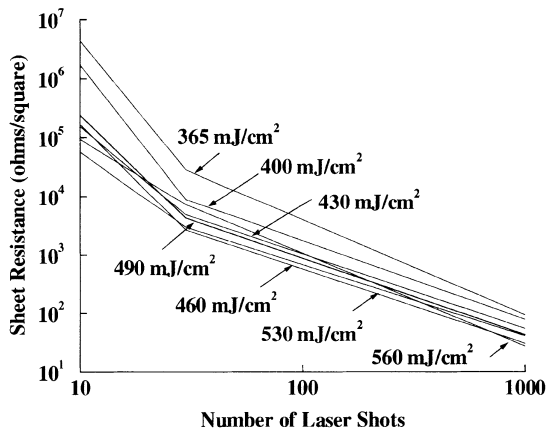


Fig. 3.17. Resistance of poly-Si, laser doped with P by the GILD process at several laser fluences [3.64]

3.3 Low-Temperature Poly-Si Devices

Three classes of laser processed device are discussed. First, self-aligned a-Si TFTs are devices that have low parasitic capacitance between the source/drain

and the gate. These devices are fabricated using laser doping of the source and drain contacts and are described in Sect. 3.3.1. Second, CMOS poly-Si TFTs enable low power-consuming circuits. Such devices are required for any high-performance circuits such as the peripheral drivers. CMOS poly-Si is discussed in Sect. 3.3.2. Third are hybrid a-Si/poly-Si devices and circuits, which take advantage of the low leakage currents of a-Si and the faster performance of poly-Si, and are described in Sect. 3.4.

The main challenges in applying the laser crystallization technique in high-volume manufacturing of TFTs are; (1) improving the uniformity of all the device performance parameters over a large area, (2) reducing the TFT leakage currents to satisfy the requirements for pixel switching, and (3) improving the device stability to ensure reliable circuit performance over the period of operation. In this section, low-temperature poly-Si device fabrication and the issues of device performance, including uniformity, leakage current and stability, are discussed.

3.3.1 Device Fabrication

Device Architectures. Common poly-Si TFT architectures include top-gate co-planar, top-gate staggered, and bottom-gate staggered structures, as shown in Fig. 3.18. A major advantage of the co-planar structure, Fig. 3.18a, is that the source/drain contacts are self-aligned with respect to the channel region which minimizes the parasitic capacitance of the TFT. The smaller parasitic capacitance results in a smaller feed-through voltage on the pixel electrode arrays for display applications, reducing image flicker and sticking. For imagers, the smaller capacitance leads to better signal-to-noise ratios. The self-aligned structure also lends itself to scaling down the channel dimensions to improve the pixel aperture ratio for display or imaging applications.

An advantage of the staggered structures (Fig. 3.18b,c) is the reduction in the electric field in the drain region. Since the source/drain contacts are made on opposite sides of the channel layer relative to the gate, the electric field near the drain region is smaller than in the coplanar structure, resulting in reduced field-dependent leakage currents and a reduced kink effect. The field dependence of the leakage current are discussed in Sect. 3.3.3. The bottom-gate staggered structure, which is not self-aligned using conventional processing, can be made self-aligned using laser doping, as discussed below.

Due to the features of the laser-crystallized poly-Si described previously, the performance characteristics of the top- and the bottom-gate TFTs are quite different. The critical channel region in the top-gate TFTs is the surface layer of the Si film. Since the top layer of the poly-Si film exhibits larger grains and a smaller number of intra-granular defects, the top-gate TFTs usually have higher mobility than that of bottom-gate TFTs. However, as described in Sect. 3.2.4, the surface roughness due to the large lateral grain growth can result in diminished and non-uniform device performance for the top-gate TFTs.

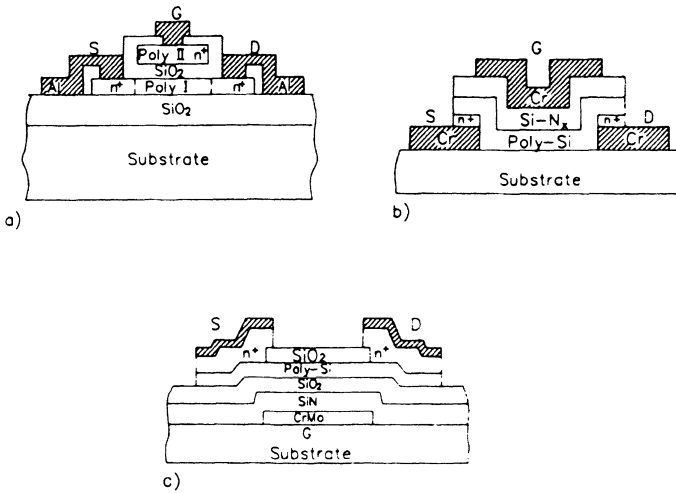


Fig. 3.18a–c. Cross sections of the various poly-Si TFT architectures: (a) top-gate coplanar, (b) top-gate staggered, and (c) bottom-gate staggered structures [3.13]

An advantage of the bottom-gate TFT is that the problem of the surface roughness is avoided. Their main disadvantage, however, is their relatively low mobility, due, in part, to the relatively high defect density near the bottom layer of the Si film, the TFT channel. Also, the laser processing energy density is limited by the thermal sensitivity of the gate insulator. The laser crystallization is performed on an a-Si film that has been deposited on the gate insulator. This structure is sensitive to heating from the laser processing which can damage the gate insulator, as indicated in Fig. 3.10. A lower laser energy density is required to avoid this damage to the gate insulator. As a result, the maximum electron field-effect mobility that has been obtained for bottom-gate TFTs is less than that for top-gate structures [3.86].

Process Flow. A typical process flow for the fabrication of top-gate, coplanar poly-Si TFTs is shown in Fig. 3.19. After the deposition of a buffer oxide on the glass substrate, a thin silicon layer, ≈ 100 nm thick, is deposited either by LPCVD or PECVD. Laser annealing using either a scanning beam or a large-area, non-scanned beam, then crystallizes the film. After crystallization, a CVD oxide, ≈ 100 nm thick, is deposited, followed by a polysilicon gate deposition of thickness ≈ 350 nm. After gate definition, either a phosphorus ion implant or a boron implant is performed to make the source and drain regions of the n-MOS or p-MOS devices, respectively. Typical implant conditions are $2 \times 10^{15} \text{ cm}^{-2}$ and 80 keV for phosphorus and $2 \times 10^{15} \text{ cm}^{-2}$ and 30 keV for boron. A 600°C furnace anneal is used to activate the source drain implants. This is the highest temperature step in the fabrication pro-

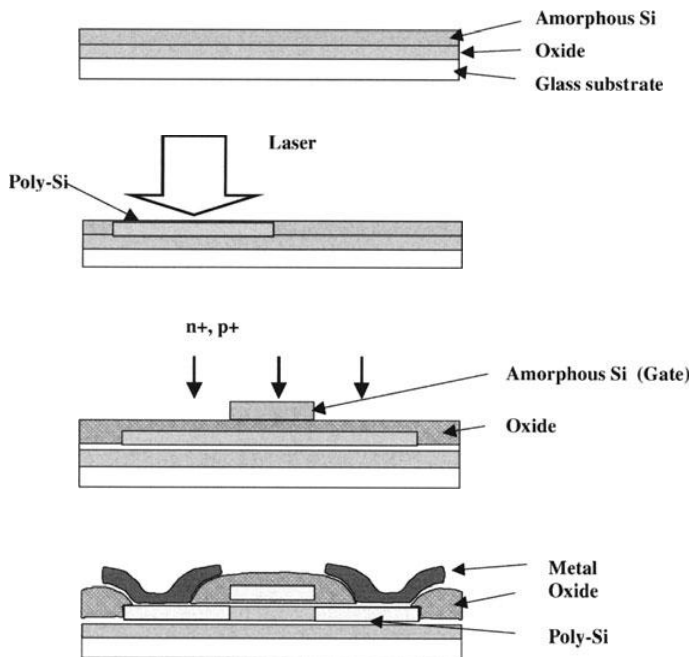


Fig. 3.19. Fabrication steps for top-gate, coplanar poly-Si TFTs [3.18]

cess. The devices then must be hydrogenated. Typically several hours in a plasma hydrogenation system at 350°C is necessary. A crossover isolation oxide can then be deposited and contacts etched to the source, drain and gate of the TFT. Then metal is deposited and patterned to form interconnects for the completed device. Using this fabrication procedure produces, TFTs are made with excellent device characteristics, as presented in Sect. 3.3.2.

As mentioned above, the 600°C furnace anneal for the dopant activation is the highest-temperature step in the poly-Si TFT fabrication process. This activation anneal can be eliminated by using laser doping rather than ion implantation for doping the source/drain contacts. This doping procedure is described in Sect. 3.2.5. It has yielded excellent devices for several different processes and device structures and has been studied by a number of groups.

Self-Aligned a-Si TFTs. Laser doping can be used to fabricate self-aligned, bottom gate a-Si TFTs. As shown in Fig. 3.18, bottom-gate structures, such as the conventional bottom-gate a-Si:H TFT, are not self-aligned. In the a-Si TFT case, depositing phosphorous-doped a-Si:H with subsequent patterning forms the source/drain contacts. Since it is difficult to selectively etch doped a-Si over the intrinsic a-Si, a top passivation island is utilized as the etch-stop to form the source/drain electrode. As a result, there is significant overlap

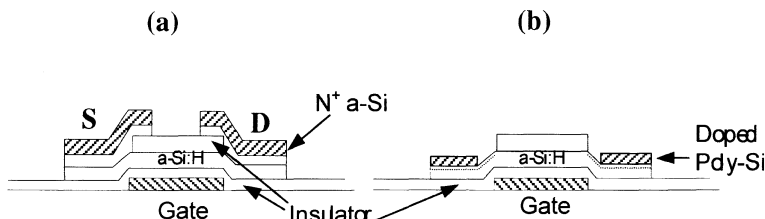


Fig. 3.20a,b. Device structures of bottom-gate a-Si:H TFTs (a) with the conventional doped a-Si source/drain contacts and (b) with laser-doped source/drain contacts [3.18]

of the source/drain electrodes with the channel region, causing additional parasitic capacitance between the gate and the source/drain. In addition, the non-self-aligned structure limits the scaling down of the channel dimension, which affects the pixel fill factor. Using laser doping, bottom-gate TFTs with a self-aligned geometry can be fabricated, as shown in Fig. 3.20 for the case of the conventional a-Si:H TFT structure. This structure reduces the parasitic capacitance and lowers the contact resistance. A factor of 20 lower contact resistance of the laser-doped source/drain has been achieved. This has also enabled a-Si TFTs with short-channel lengths down to $1\ \mu\text{m}$ and with reasonable performance to be made [3.19].

3.3.2 CMOS Device Performance

The various device parameters of interest are determined from the measured transfer characteristics of the transistor, the source-drain current, I_{sd} , as a function of the gate voltage, V_g , for various source-drain voltages, V_{sd} . The parameters of interest are the on-off ratio and the leakage current, the threshold voltage, the field effect mobility, and the subthreshold slope. Also, the uniformity in these parameters across the wafer or plate is important for any circuit applications. Transfer curves for a top-gate poly-Si TFT fabricated in the manner described in Fig. 3.19 are shown in Fig. 3.21, for an n-MOS TFT with channel width/length ratio (W/L) of $50\ \mu\text{m}/15\ \mu\text{m}$. A laser energy density of $500\ \text{mJ}/\text{cm}^2$ and 5 shots was applied to the $50\ \text{nm}$ LPCVD silicon channel layer. The device has a high on-off ratio (nearly 10^8), a threshold voltage less than $2\ \text{V}$, a field effect mobility greater than $150\ \text{cm}^2/\text{Vs}$, and a leakage current of $0.3\ \text{pA}/\mu\text{m}$ at $10\ \text{V}$ drain bias. In addition, the transistor turns on abruptly, having a subthreshold slope of better than $0.3\ \text{V}$ per decade of source-drain current. These excellent device characteristics indicate that the laser-crystallized material is also of high quality. The device parameters are discussed further below and in subsequent sections.

Subthreshold Slope. The subthreshold slope, S , parameterizes how abruptly the transistor turns on. It is degraded by defects that trap charge in the

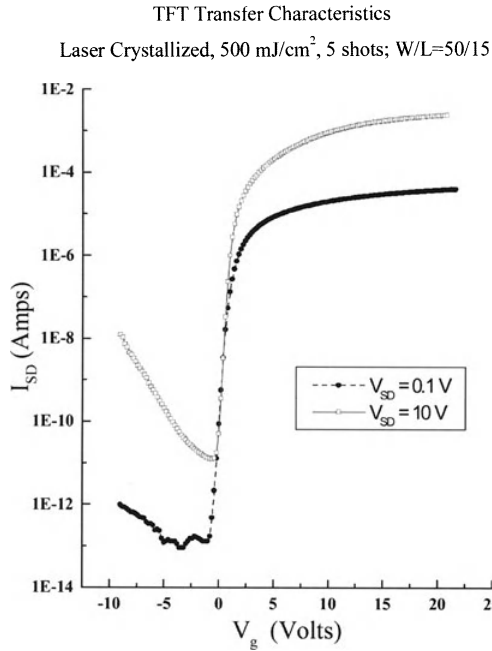


Fig. 3.21. n-MOS TFT device transfer characteristic with channel $W/L = 50/15$ for a laser energy density of 500 mJ/cm² and 5 shots applied to a 50 nm LPCVD silicon channel layer. Curves for two different source-drain voltages are shown [3.18]

space charge region of the transistor. For a single-crystal MOSFET, $S \approx (1 + C_D/C_g)$, where C_g is the gate capacitance and C_D is the space charge capacitance, which varies as the square root of the space charge density, $\sqrt{N_{SC}}$. As a result, S increases as the square root of N_{SC} [3.13]. It is about 0.16 V/decade for a MOSFET with a substrate doping level of 10¹⁶/cm³ and a gate oxide thickness of 150 nm.

The value of 0.3 V/decade for the poly-Si TFT of Fig. 3.21 corresponds to a larger space charge density of order 10¹⁷/cm³, due to the large number of trapping states at the grain boundaries and intra-granular defects, as discussed in Sect. 3.2. It is also consistent with the number of dangling bond defects determined from ESR measurements after hydrogenation, as shown in Fig. 3.15. The value before hydrogenation is even larger by a factor of about 50, corresponding to a poorer $S \approx 1$ V/decade. The dramatic effect of hydrogenation on N_{SC} that is shown in Fig. 3.15 is also evident in the reduction in S shown in Fig. 3.22, from 1.24 V/decade before hydrogenation to 0.24 V/decade after hydrogenation. These TFTs were hydrogenated in a hydrogen plasma for 8 h at 350°C. Also, the dramatic improvement in the leakage current by 4 orders of the magnitude and in the threshold voltage is

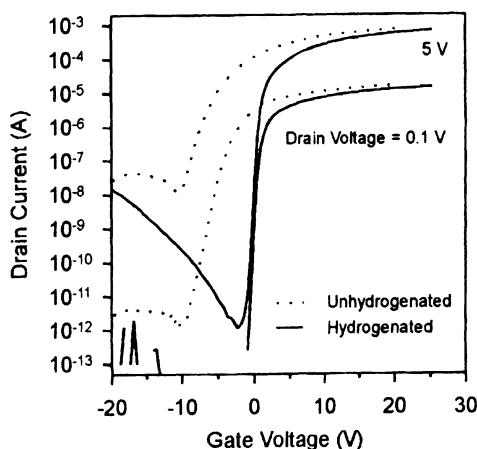


Fig. 3.22. $I_{sd} - V_g$ characteristics for a TFT with $W = 10\ \mu\text{m}$ and $L = 10\ \mu\text{m}$, showing the dramatic performance improvement obtained from hydrogenation in the leakage current, threshold voltage, and subthreshold slope. The subthreshold slope improves from 1.24 V/decade to 0.24 V/decade, the leakage current improves by four orders of magnitude, and the threshold voltage improves from $-10.3\ \text{V}$ to $-0.2\ \text{V}$ [3.21]

readily apparent in these data. Hydrogenation is evidently an important step in fabricating TFTs with good parameters, as discussed further in Sect. 3.3.3 below.

Mobility. A striking feature of the laser crystallization process is the formation of large grains in a narrow range of the laser energy density, as described in Sect. 3.2.3. This feature affects the TFT mobility and uniformity. Below the critical value, F_p , the TFT mobility increases gradually with laser energy density. This improvement in the TFT performance is due to the reduction of the intra-grain defects and the small and gradual increase in grain size. Near the region of the critical fluence, the same region for producing the maximum grain size, the TFT mobility increases abruptly and reaches a maximum value due to the large lateral grain growth. When the laser energy density is above the critical value, the TFT mobility decreases and the distribution of the TFT performance becomes non-uniform, as does the grain size.

Figures 3.23 and 3.24 show plots of mobility versus laser energy density. The data are for various numbers of laser shots for n-MOS and p-MOS transistors fabricated as described in Sect. 3.3.1 and Fig. 3.19. For both n-type and p-type transistors, the mobility peaks near $500\ \text{mJ}/\text{cm}^2$. This peak in mobility corresponds to the peak in the grain size for the experimental conditions of these measurements, namely 50 nm thick films (both LPCVD and PECVD) and a SOPRA XeCl laser with a 160 ns pulse width. Beyond this peak there

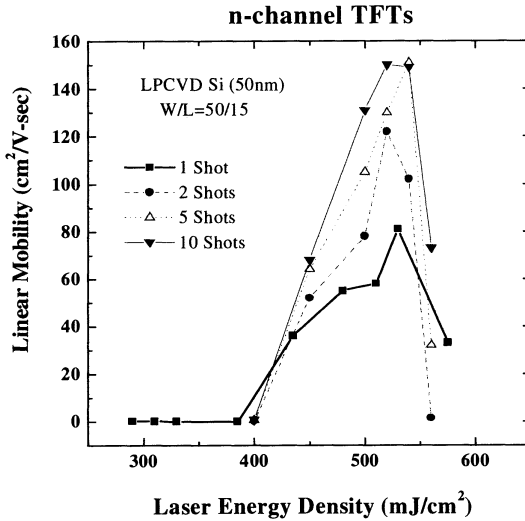


Fig. 3.23. Field effect mobility for top-gate, n-MOS TFTs as a function of laser energy density. Data are presented for various numbers of laser shots for n-MOS transistors fabricated in 50 nm thick LPCVD silicon [3.18]

is a sharp drop in mobility as the grain size drops and the ablation threshold is approached. Multiple shot annealing improves device performance, with most of the improvement seen in the first five laser shots. This corresponds to an increase in grain size and grain quality with the number of pulses.

Uniformity. Although devices with excellent characteristics have been obtained, the uniformity of the devices has been problematic [3.7, 9, 15]. Any variation in grain size, surface topography, interface structure, and the like translates into variations in the device parameters. This nonuniformity can be significant in the overlap regions for scanned laser crystallization [3.15] and is alleviated by either heating the substrate to temperatures of about 400°C during crystallization [3.7] or using a small pitch scan, i.e., one with step size much less than the beam dimension [3.9]. The inhomogeneity is lessened by these approaches but is not eliminated. The root cause is the distribution in grain size and surface roughness created by portions of the laser beam that have fluences near the fluence of the grain size peak, F_p . The sharpness of the large lateral grain growth regime exacerbates this effect since small variations in the beam intensity, either spatially in the beam profile or temporally from shot to shot, can create rough, large-grain regions in an otherwise smooth, uniform film.

In the regions with roughened surfaces, the TFT mobility drops and the threshold voltage increases. Roughness is known to be detrimental to carrier transport [3.59] and therefore creates these undesirable device characteristics.

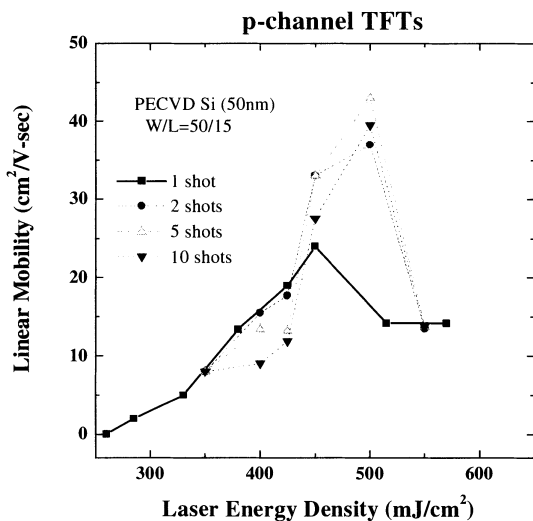


Fig. 3.24. Field effect mobility for top-gate TFTs versus laser energy density for p-MOS devices fabricated in 50 nm PECVD silicon [3.18]

Overall, as much as a 50% variation in mobility can be observed [3.15], far too big for any large area electronic applications. This is a worse case scenario that can be alleviated by crystallizing below the fluence of large grain growth. Good uniformity can be obtained by keeping the beam fluence below F_p [3.17]. The fluence must be sufficiently below F_p so that all artifacts such as interference fringes and beam fluctuations will not carry the fluence above F_p . There is a trade-off, however. As the fluence decreases, so do the grain size and the mobility. Yet the distribution in mobility over the devices on the plate will also decrease. It is a matter of creating a few spectacular devices with a wide variation versus creating all good devices with good parameters in a narrow distribution. The good devices are what are desired in large-area electronics and can readily be achieved by keeping the beam fluence below F_p .

Alternative methods to improve the device uniformity by controlling the grain size distribution have been proposed. These include seeded grain growth [3.68] and a controlled heat flow process [3.69]. In the seeded grain growth method, crystalline seeds are generated in a defined pattern to match the design of the devices. In the controlled heat flow process, the lateral heat flow is manipulated by patterning of materials with different thermal conductivity or by thermal isolation of the device region. Bottom-gate TFTs with maximum mobility of $600 \text{ cm}^2/\text{Vs}$ have been fabricated in laser crystallized poly-Si films over a SiO_2 membrane [3.70]. Using the thermal-isolation, membrane structure, large grains of several tens of microns have been generated in a pre-defined pattern, as shown in Fig. 3.25.

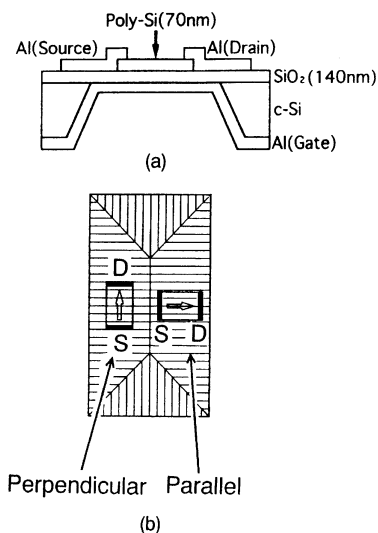


Fig. 3.25a,b. Schematics of bottom gate TFTs fabricated on a membrane, (a) cross section, and (b) top view [3.70]. Due to the lateral heat flow pattern, there are dominant orientations of the grain boundaries. Two kinds of TFTs were fabricated with the channel length parallel or perpendicular to the grain boundaries respectively. The TFT field effect mobility of the TFT with the channel length parallel to the grain boundaries is twice as that with the channel length perpendicular to the grain boundaries

Various methods for reducing the surface roughness to improve performance and uniformity have been proposed. Multiple laser irradiation is as an efficient way to reduce the surface roughness [3.12]. A laser crystallization process using two different fluence values is also reported to alleviate the surface roughness by re-planarization, yielding a small roughness of about $\pm 5\%$ [3.9]. In addition to modifying the laser process, a chemical-mechanical polishing has been proposed to improve the device performance for the top-gate poly-Si TFTs [3.71].

For the bottom-gate TFTs, the effect of the surface roughness is less detrimental to the device performance compared with that of the top-gate TFTs. The device uniformity may be improved by combining multiple irradiation with a lowering of the laser energy density below the critical value and by choosing the bottom-gate TFT structure. Figure 3.26 shows results from an experiment to obtain uniform TFT characteristics with a process compatible with a-Si TFTs. A 4 mm wide beam with an energy density of $\approx 75\%$ of the critical value crystallized a swath of Si film that was fabricated into an array of bottom-gate TFTs. The mobility has an acceptable 10% variation over the 4 mm width of the beam then deviates substantially at the beam edges. By increasing the laser fluence to the critical energy value, the TFT mobility can be increased substantially. However, some of the TFTs exhibit large gate leakage due to damage to the gate insulator.

3.3.3 Device Leakage Currents

The leakage current requirements for the poly-Si TFTs in the peripheral driver circuits of active matrix arrays are not as stringent as that for the

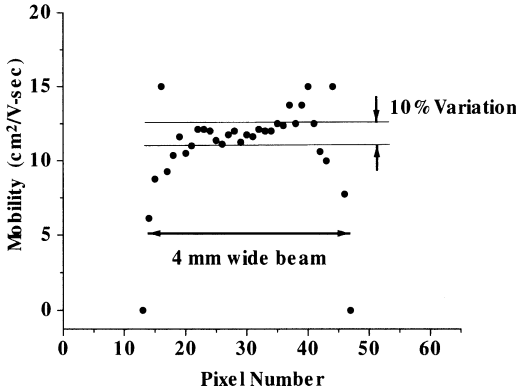


Fig. 3.26. Transistor mobility as a function of position for bottom-gate TFTs fabricated on a glass wafer and crystallized by a 4 mm wide beam [3.15]

pixel switches. A major challenges for poly-Si pixel switch is to achieve a sufficiently low leakage current to prevent the pixel from losing charge during a frame time. The allowed maximum leakage current can be estimated as,

$$I_{\text{Leak}} < \eta Q / \tau_{\text{fr}} , \quad (3.5)$$

where τ_{fr} is the frame time (33 ms for a video rate), η is the quality factor for the application (the percentage of charge-loss allowable), and Q is the charge stored on the pixel capacitor. The maximum charge stored in the pixel depends on the storage capacitor and the operation voltage:

$$Q = C_{\text{store}} V_{\text{op}}, \quad C_{\text{store}} = \frac{\varepsilon A}{d} . \quad (3.6)$$

For a display array with a pixel size of $100 \times 100 \mu\text{m}^2$, the pixel capacitance from (3.6) is about 0.25 pF. Under an operating voltage of 10 V and a quality factor of 2%, the maximum leakage current for the pixel switch is about 1.5 pA. The restrictions on the leakage current are more stringent when the pixel size is smaller or the operating voltage is lower. For imaging applications the frame time is often much larger (≈ 1 s) requiring a much smaller value of the leakage current allowable for the pixel switches.

Poly-Si TFTs exhibit higher off-state (leakage) currents compared with a-Si:H TFTs or single crystalline MOSFETs. Under a gate-off condition, the leakage current exhibits an exponential dependence on the bias on the gate and the drain. In addition, the leakage current is asymmetric in most cases when source and drain are reversed, due to an asymmetric spatial distribution of the defects in the channel, as discussed below. Figure 3.27 illustrates the difference in the leakage current when the source and drain are reversed, while the on-state behavior is unchanged [3.72].

The field-dependent leakage current in poly-Si TFTs originates from intra-grain and grain boundary defects or traps. Several authors have proposed

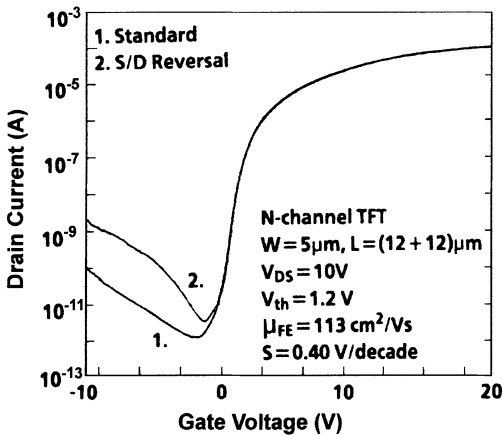


Fig. 3.27. Leakage current characteristics of a dual gate *n*-channel TFT with reversed source/drain connections [3.72]

models for the leakage current, most of which are based on field-emission or field-enhanced tunneling at trap sites in the high-field region near the drain [3.73–75]. Various experimental results show that the leakage current is a direct consequence of the high drain field in the poly-Si. The leakage current may vary from device to device depending on the spatial location of the defect as well as the energy of the traps in the poly-Si bandgap [3.75]. For example, when the traps are near the edge of the gate, where the electric field is relatively low, the leakage current is low. As the traps move further from the gate edge toward the source, the leakage current at first rises as the traps cross the peak channel electric field, and then decrease as they move nearer to the source.

Currently, the most efficient method to reduce the leakage current is to incorporate hydrogen into the TFT channel layer to passivate the trap states. The hydrogenation methods include exposure to a hydrogen plasma at an elevated temperature [3.73], hydrogen ion implantation followed by thermal activation of hydrogen [3.76], and deposition of a thin hydrogenated silicon nitride film followed by thermal anneal to drive hydrogen from the nitride film into the silicon channel [3.77]. Figure 3.22 shows the effects of hydrogenation on the leakage current reduction. After 8 h of hydrogenation at 350°C, the leakage current is reduced by 4 orders of the magnitude. In addition to hydrogenation, fluorine passivation and ammonium plasma passivation are also reported to effect leakage current reduction [3.78, 79].

Reducing the electric field strength along the channel in the drain depletion region can minimize the TFT leakage current. The field can be reduced by offsetting the source/drain contacts where a space of order a few microns is introduced between the source/drain regions and the channel region defined by the gate. The field can also be reduced by introducing lightly doped

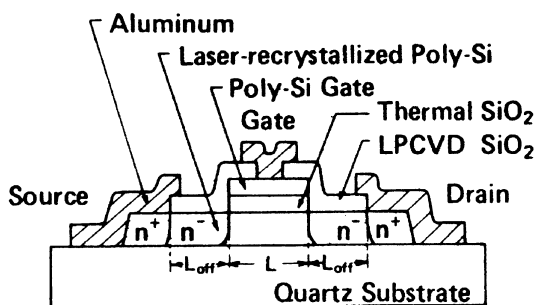


Fig. 3.28. Schematic cross-sectional view of a lightly doped source/drain structure for leakage current reduction [3.80]

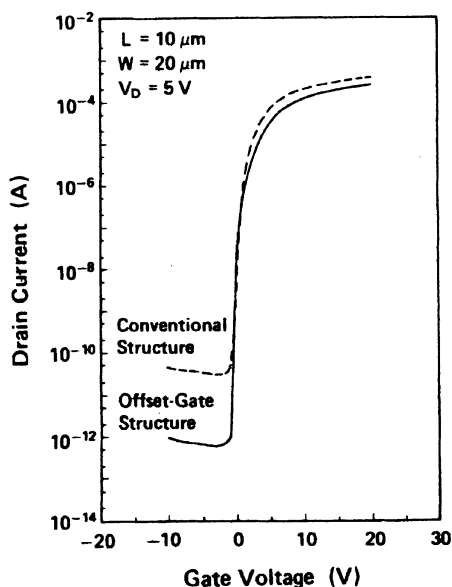


Fig. 3.29. Subthreshold current characteristics in a conventional poly-Si TFT and an offset-gate-structure poly-Si TFT [3.80]

source and drain regions, as shown in Fig. 3.28. In this case, the lightly doped regions were formed by phosphorus implantation with a dose of $10^{12}/\text{cm}^2$, compared with a dose of $10^{15}/\text{cm}^2$ for the n^+ contacts. Figure 3.29 shows a comparison of the leakage current between a conventional top-gate poly-Si TFT and a TFT with the source/drain-offset structure. The offset-structure TFT has a leakage current reduction of one to two orders of magnitude [3.80]. Although the source/drain-offset structure increases the device contact resistance, the on-state current reduction is insignificant as long as the design of the offset region is appropriate.

3.3.4 Device Stability

The stability of poly-Si TFTs is of importance for large area electronic applications, especially for the driver circuitry where the drive currents and frequencies are high. The various types of poly-Si TFT degradation occur under a combination of gate and drain bias stress. The degradation includes any or all of the following: an increase in the leakage current, a shift in the threshold voltage, a decrease in the on-current, and a hysteresis in the on-current. The first two are the most troublesome. Most degradation occurs when a device is stressed in the “on-state”. Unlike single-crystal silicon, which degrades due to hot-carrier effects, poly-Si TFTs can degrade significantly when the device is in the on-state with a high channel current flowing, even when the source-drain bias is low [3.81]. In this case, both the threshold voltage and the leakage current increase. In addition, stressing using ac stress conditions leads to a more severe performance loss than comparable steady-state, dc stress conditions.

Several mechanisms have been proposed to account for the instability [3.82–84]. Hack et al. [3.82] proposed that changes in the characteristics of stressed poly-Si TFTs are caused by the generation of defects in the poly-Si in response to changes in the free carrier densities. There are two types of the stress-related defects, each with a different position within the energy bandgap. Stressing in the TFT linear operation region ($V_g > V_{sd}$) produces defects around or below midgap. The defects generated are distributed symmetrically spatially from source to drain, causing a threshold voltage shift. Degradation under saturation conditions ($V_g < V_{sd}$) results in additional defects being created higher up in the bandgap. These defects are in the high field region near the drain, which causes asymmetric device behavior. The origins of both types of defects are related to weak silicon bonds. These stress-induced defects are metastable since annealing of these devices at about 300°C will eliminate the defects and restore the device performance to its original state.

Fonash et al., [3.84] have described a reversible passivation/depassivation stress phenomenon. After an on-state stress with V_{sd} of 20 V, the device exhibits a lower leakage current when measured with the source/drain voltage polarity reversed relative to its polarity used for stressing. The same device was then subjected to a second on-state stress with the source/drain stress voltage reversed. The leakage current after this stress was lower when measured with the source/drain polarity the same as that of the first stress voltage (Fig. 3.30). Since the poly-Si devices, which were not hydrogenated, do not exhibit this behavior, the authors attribute this phenomenon to hydrogen release or capture at defects and positively charged hydrogen motion in the stress electric field.

The high field related instability may be reduced by the same methods used in the leakage reduction described in Sect. 3.3.3. For example, the device degradation for the staggered TFT structure, which has a lower field near the

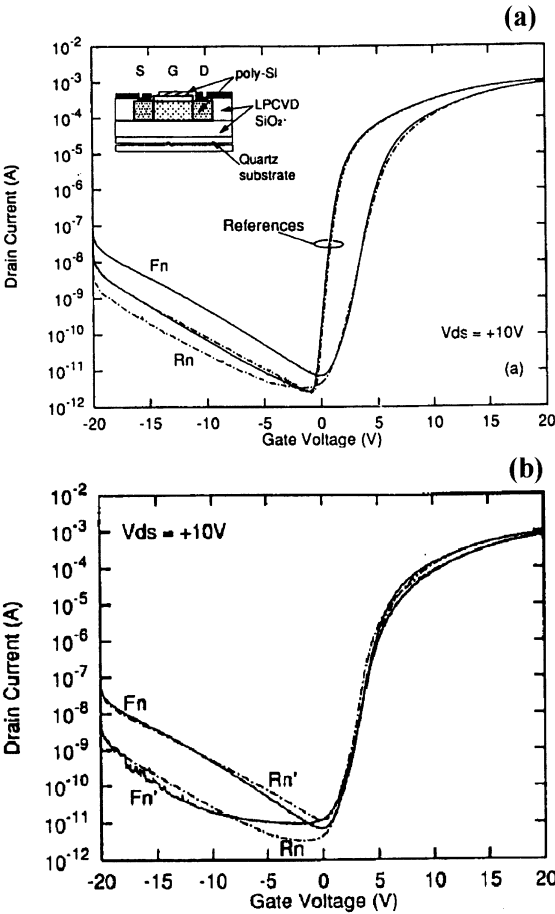


Fig. 3.30a,b. Device performance under on-state stress with (a) forward and then (b) reverse source/drain bias of 20 V. F_n and F_n' are measured for the first and second stresses with the source/drain connected with the same polarity as that of the stress voltage. R_n and R_n' are measured for the first and second stresses with the source/drain polarity reversed relative to that of the stress [3.84]

drain, is less severe compared with that of the planar structure. Figure 3.31a shows the stress effect of a double, bottom-gate staggered poly-Si TFT made by laser crystallization. The stress was performed under linear conditions for 4 h. There is a small positive shift of the threshold voltage. The other types of degradation, i.e., changes in leakage current, on-current, and hysteresis in the on-current, are not observed. Figure 3.31b shows the results of device degradation under a stress of high drain bias, where the hysteresis in the

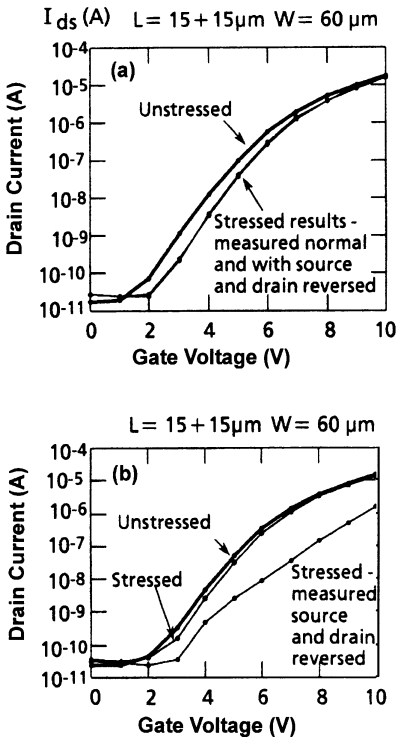


Fig. 3.31a,b. Transfer characteristics for an unstressed TFT and a TFT stressed for 4 h with (a) $V_g = 15 \text{ V}$ and $V_{sd} = 10 \text{ V}$ and (b) $V_g = 10 \text{ V}$ and $V_{sd} = 15 \text{ V}$ [3.85]

on-current is observed. Overall, the degradation of this device is much less than that of the device with single gate and planar structure.

In general, poly-Si TFTs have better stability under stress than a-Si TFTs. With proper defect passivation, such as hydrogenation, the change in the device properties for poly-Si TFTs are sufficiently small that they can be used for various integrated circuit applications.

3.4 Integration of a-Si and Poly-Si TFTs

A-Si:H thin film transistors possess low off-state currents, making them ideal pixel switches in large area arrays. However, the carrier mobility of a-Si:H is too low for high-speed peripheral driver circuits so that current technology relies on connecting the a-Si:H arrays to external high-speed, crystalline-silicon circuits. In contrast, the fabrication of large-area arrays with poly-Si pixel switches and peripheral drivers requires poly-Si TFTs to have uniform performance and low off-state currents. The alternative discussed here is a hybrid system combining a-Si and poly-Si TFTs as illustrated in Fig. 3.1.

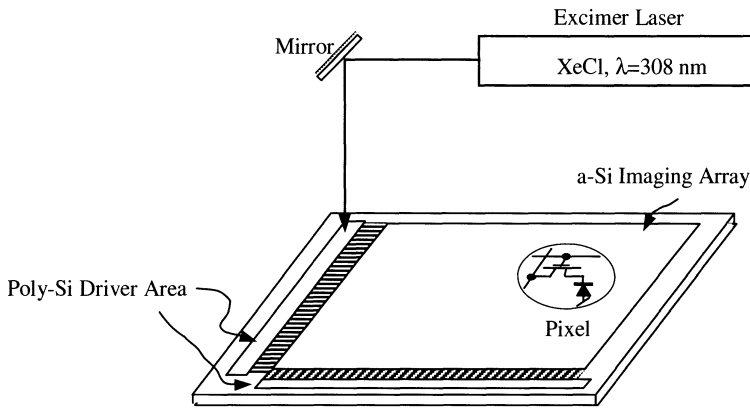


Fig. 3.32. Schematic of a laser crystallization system for converting a-Si:H material to poly-Si films for the drive circuits in the peripheral areas of an imaging array

The hybrid approach utilizes the low leakage current a-Si:H TFTs to fulfill the requirements for the pixel switches and high-mobility poly-Si for the peripheral circuits. Poly-Si devices have the high mobility needed for peripheral drive circuitry, and the requirements on the TFT off-state currents are not as stringent as for the pixel switches. In addition, since the area of the peripheral circuits is generally smaller than the laser beam width (Fig. 3.32), uniformity of the poly-Si TFTs is easier to achieve with a one-dimensional laser scan for the crystallization process than for a two-dimensional scan to crystallize the entire plate. This approach reduces the number of external connections and thereby lowers the packaging costs of large-area electronics. The cost advantage is more pronounced for high-resolution arrays when the pitch of the pixels becomes less than the current bonding pitch for the peripheral circuits, about 100 μm .

3.4.1 Development of Hybrid a-Si and Poly-Si Devices

Integration of a-Si and poly-Si TFTs relies on simple modifications of the existing a-Si device fabrication process. The attempt has been focused on selective laser crystallization of a-Si:H in order to have the same process steps for most of the fabrication of a-Si and poly-Si TFTs. An early study by Sera et al. in 1989 [3.3] demonstrated the principle of a staggered top-gate TFT structure. Figure 3.33 describes the fabrication process. In general, a top-gate poly-Si TFT has a higher mobility compared with that of a bottom-gate TFT, as described in Sect. 3.3.1. However, the performance of a top-gate a-Si TFT is inferior to that of the bottom-gate a-Si:H TFTs [3.86]. The mobility of the top-gate a-Si:H TFT [3.1] is about 0.2 cm^2/Vs , which is much less than that of a conventional bottom-gate a-Si:H TFT, $\approx 1 \text{ cm}^2/\text{Vs}$.

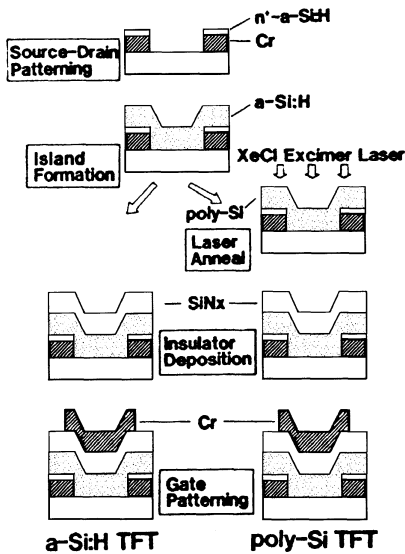


Fig. 3.33. Fabrication process for top-gate a-Si:H and poly-Si TFTs using the selective excimer laser annealing method [3.3]

This work on the top-gate TFTs showed that the inverse staggered (bottom-gate) TFT structure is more suitable for the integration of a-Si and poly-Si devices. An early demonstration of the monolithic fabrication of bottom-gate hybrid a-Si:H and poly-Si TFTs was reported by Shimizu et al. in 1990 [3.6]. The Si film is grown by the CVD process, and the poly-Si material is created by selective pulsed laser crystallization. The fabrication procedure is shown in Fig. 3.34. The discrete a-Si:H and poly-Si TFTs have field effect mobilities of 1.3 and $60 \text{ cm}^2/\text{Vs}$, respectively. A demonstration liquid crystal display with a-Si:H pixel switches and poly-Si peripheral circuits was reported by Tanaka in 1993 [3.87], with circuit diagram as shown Fig. 3.35. The poly-Si TFTs connect each output terminal of the driver IC to two drain lines in the pixel array to reduce the number of driver ICs by one half. This work shows the simplicity of the fabrication with an all n-type TFT design.

The major technical difficulties of monolithic fabrication of both a-Si and poly-Si TFTs on the same low temperature substrate are achieving selective laser crystallization, and control of the TFT threshold voltage. Selective laser crystallization of PECVD a-Si:H has to deal with the problem of hydrogen evolution from the hydrogenated a-Si:H film. The threshold voltage issue is related to an appropriate gate insulator for both a-Si and poly-Si TFTs. Both issues are addressed in the following section.

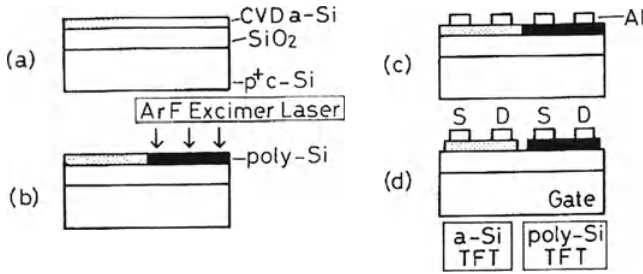


Fig. 3.34a-d. Fabrication flowchart for the on-chip bottom-gate a-Si and poly-Si TFTs with selective laser crystallization process. (a) deposition of CVD a-Si film, (b) local crystallization by an excimer laser, (c) TFT source and drain patterning, and (d) TFT island formation [3.6]

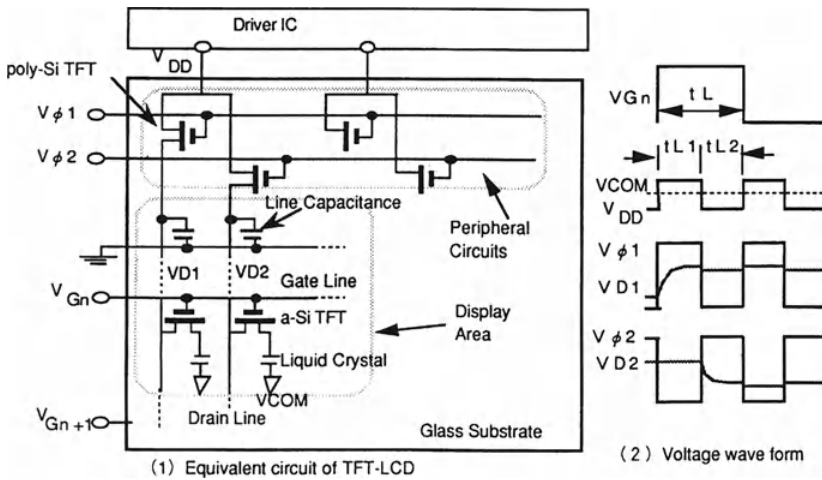


Fig. 3.35. Schematic of the poly-Si peripheral circuitry used to reduce the number of driver ICs in a display [3.87]

3.4.2 Hybrid Materials Processing

To maintain high performance a-Si TFTs, a low temperature PECVD process is used to deposit a-Si:H films for the fabrication of the hybrid a-Si and poly-Si devices. The low-temperature PECVD a-Si:H films contain a large amount of atomic hydrogen, typically 10 at. % which passivates Si dangling bonds and determines the electronic properties of the a-Si:H [3.88].

Whereas H is essential for good electrical performance of a-Si devices, it is problematic for a poly-Si precursor since it causes film ablation and cracking during laser crystallization due to the rapid hydrogen out-diffusion. To prevent this explosive H evolution, a 450°C furnace anneal for several

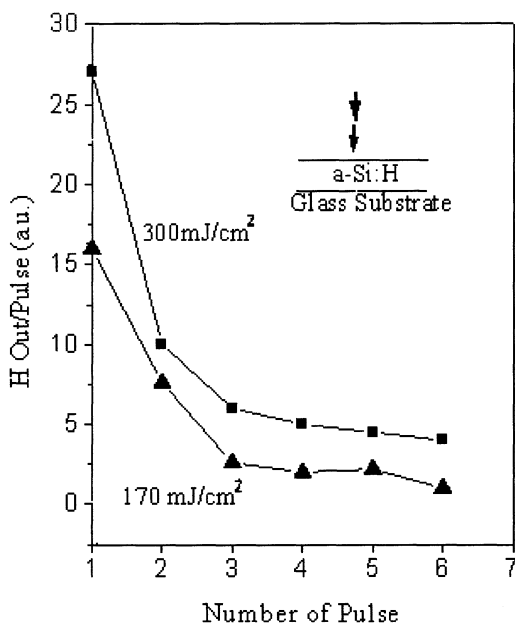


Fig. 3.36. Hydrogen out-diffusion per laser pulse as a function of the number of the laser pulses. The a-Si:H sample was first irradiated by a excimer laser at 170 mJ/cm² with a number of pulses. The same sample was then irradiated by the laser at a higher energy density (300 mJ/cm²) [3.90]

hours is usually required to remove most of the H from the a-Si:H films prior to laser crystallization. This anneal makes it impossible to fabricate high quality a-Si devices because of the significant loss in H in the amorphous devices at 450°C.

There have been several approaches to make high quality materials for both a-Si and poly-Si devices on the same substrate. Shimizu et al. [3.6] describe an approach in which a-Si deposition is carried out at 450°C using disilane, resulting in a smaller amount of H (3 at. %) in the material. Because of the small hydrogen content in the starting material, the laser ablation is avoided during selective crystallization. This small amount of hydrogen, however, is detrimental to the a-Si TFT performance. In order to achieve high performance, a crucial hydrogenation procedure had to be performed on both a-Si and poly-Si devices.

An alternative approach is reported by Aoyama et al. [3.89]. In their work, the precursor for the poly-Si film is a 40-nm thick hydrogenated a-Si:H. The thin a-Si:H film allows thorough laser crystallization without hydrogen induced film ablation. A restriction in this process, however, is a limit on the laser energy density to a value below that required to get a large poly-Si grains.

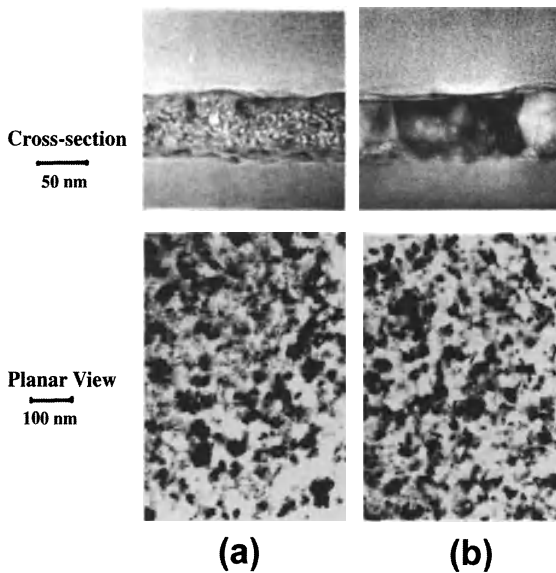


Fig. 3.37a,b. TEM cross sections and planar views of samples after laser dehydrogenation at (a) 150 mJ/cm^2 and (b) 300 mJ/cm^2 [3.90]

The hydrogen out-diffusion from a-Si:H is also controlled by careful choice of the laser fluence [3.90]. Pulsed laser crystallization of a-Si:H films with moderate thickness (40–100 nm) can be performed by a series of laser exposures with increasing laser energy density. One scheme is to have the laser beam shaped as a staircase in space [3.56]. With this beam profile, the a-Si:H film receives laser irradiations with a gradual increase in energy density as the beam is scanned. Another approach is to use three laser irradiations with increasing laser energy density [3.90]. Figure 3.36 shows the experimental data on the amount of hydrogen that out-diffuses for different laser fluences and number of laser shots.

During a pulsed laser irradiation, hydrogen diffuses rapidly in the molten silicon layer. In the three-step process, the laser energy density of the first irradiation is chosen to be slightly above the Si surface-melting threshold. The hydrogen atoms near the surface are removed during a multiple-shot irradiation at this low energy density. The second laser energy density is chosen to be near the melt-through fluence, which depends on the various factors discussed in Sect. 3.2.2 and includes the film thickness. This irradiation removes most of the hydrogen remaining in the film. The final scan at higher laser fluence produces poly-Si films with large grains.

Figure 3.37 shows cross-sectional and planar-view TEM images of the films processed by the three-step process. After the first laser scan, the film is partially converted to microcrystalline Si with fine grains (Fig. 3.37a). The

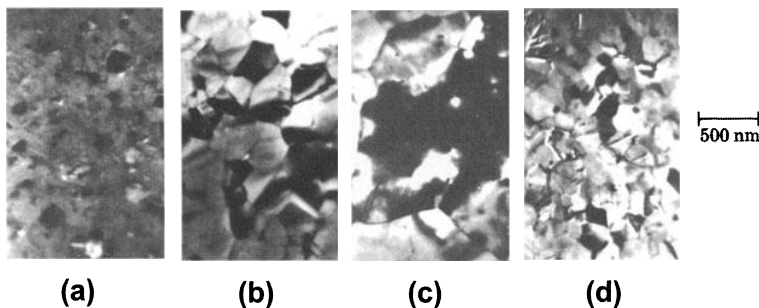


Fig. 3.38a–d. TEM planar views of poly-Si films produced by the three-step laser processing of PECVD a-Si:H. The laser energy densities for the third and final step were (a) 425 mJ/cm^2 , (b) 445 mJ/cm^2 , (c) 465 mJ/cm^2 , and (d) 485 mJ/cm^2 [3.47]

second scan at an energy density near the melt-through threshold produces columnar poly-Si grains (Fig. 3.37b). The average grain size, however, is small. The desired film crystallinity is mainly determined by a third and final scan.

Figure 3.38 shows the film crystallinity from samples processed by the three-step laser crystallization process at various laser energy densities for the last step. The behavior of the average grain size versus the laser fluence is similar to that for laser crystallization of LPCVD deposited Si films described in Sects. 3.2.2 and 3.2.3. The grain size increases with increasing laser energy density up to a peak value of a few microns. The grain size then decreases with further increases in the laser energy density. The transistor field effect mobility is correlated with this grain size. At the optimized grain size, however, the film suffers from damage at the interface between the Si film and the gate insulator below. The damage results in non-uniform device performance and a significant leakage current through the gate insulator. Uniform device performance is obtained by choosing a laser energy density near to, but below, the critical value.

3.4.3 Device Fabrication and Performance

Figure 3.39 illustrates the monolithic fabrication process for making a-Si and poly-Si bottom-gate TFTs on the same substrate. The process starts with the gate electrode patterning, followed by PECVD deposition of a dual dielectric of Si_3N_4 and SiO_2 and a-Si:H. Selective laser dehydrogenation/crystallization is then performed. The film is hydrogenated after the crystallization process to passivate the defects in the poly-Si film. The source/drain contacts are made from deposited, doped a-Si:H, followed by metal deposition and patterning.

The dual dielectric gate insulator is used to optimize the threshold voltage simultaneously for both a-Si and poly-Si TFTs. The TFT threshold voltage depends on the fixed charge in the dielectric film, the defect density, the dop-

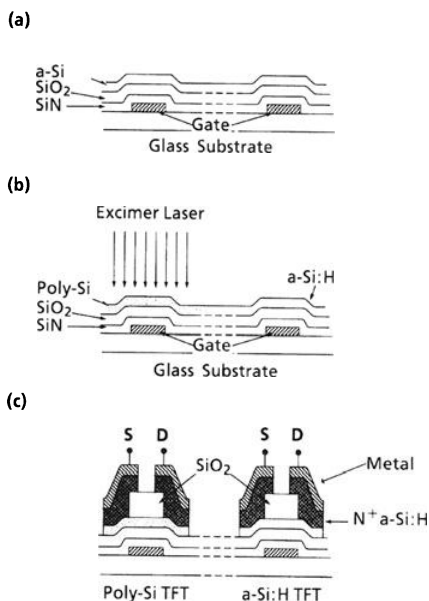


Fig. 3.39a–c. Fabrication process for hybrid a-Si and poly-Si TFTs; (a) PECVD deposition of the gate insulator and an a-Si:H film; (b) selective laser dehydrogenation and crystallization; (c) the final device structure with source and drain contacts [3.48]

ing level in the Si film, and the work function of the gate electrode. a-Si:H TFTs show superior performance with a silicon nitride (SiN) gate insulator over that for a SiO₂ gate insulator. According to the defect pool model [3.91], the superior performance of a-Si TFTs with a nitride gate insulator is attributed to the positive fixed charge in the nitride dielectric. The positive charge pulls the Fermi level up in the band gap, causing a redistribution of the defect density of states. This lowers the defect densities located above midgap in the a-Si:H. Therefore, the threshold voltage is small and positive for SiN. However, the threshold voltage of poly-Si TFTs is just the reverse; namely, it is large and negative with a SiN gate insulator and is small and positive for a SiO₂ gate insulator. Figure 3.40 describes the general behavior of a-Si and poly-Si TFTs with nitride or oxide as the gate insulator.

Large-area display and imaging applications require small and positive threshold voltages for a-Si pixel switches and poly-Si TFTs in the peripheral circuits. A simple approach to obtain small and positive threshold voltages for both a-Si and poly-Si TFTs is to combine SiN and SiO₂ for the gate insulator. Figure 3.41 shows simulation results of the transfer characteristics of poly-Si TFTs with various film thickness of nitride and oxide, keeping the total dielectric film thickness at 100 nm. In this simulation, a uniform

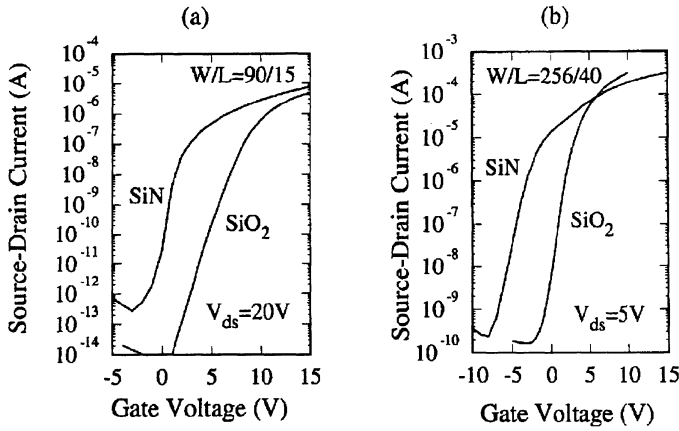


Fig. 3.40a,b. Transfer characteristics of (a) a-Si TFTs and (b) poly-Si TFTs with nitride and oxide as the gate insulator, at the specified device width-to-length ratio (W/L) and source-drain voltage, V_{ds} [3.47]

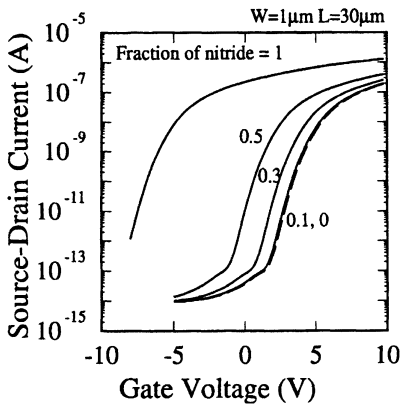


Fig. 3.41. Simulated transfer characteristics of poly-Si TFTs with a dual dielectric of nitride and oxide. The total dielectric thickness is 100 nm [3.47]

density of fixed charge is introduced into each layer of the two-layer gate dielectric. It is assumed that the fixed charge density in nitride is $+4 \times 10^{17}$ charges/cm³ while it is -10^{17} charges/cm³ in the oxide. The two-dimensional device simulator is based on one specifically developed for modeling a-Si TFTs wherein the defects and grain boundaries are treated as a spatially uniform density of localized states in the band gap. The effective density of states spectrum for poly-Si has been obtained by fitting the model to both the low drain bias transfer data as well as to the activation energy of the channel conductance as a function of gate bias. This set of calculations demonstrates

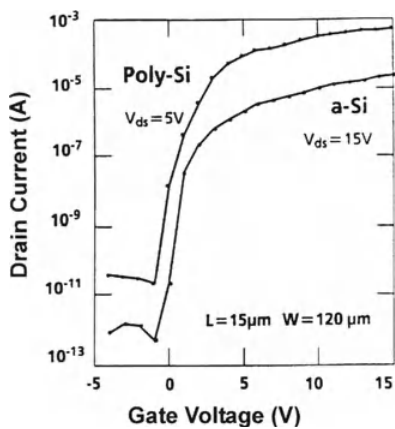


Fig. 3.42. Transfer characteristics of an a-Si and poly-Si TFTs fabricated on the same substrate by the selective laser de-hydrogenation and crystallization process and with a dual dielectric [3.47]

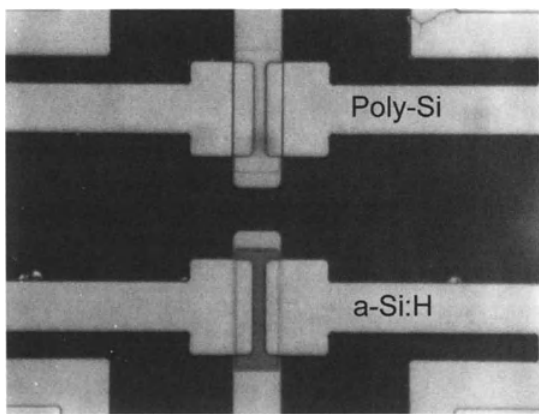


Fig. 3.43. Optical microscope photograph of an a-Si TFT and a poly-Si TFT built side by side by a monolithic fabrication process. The distance between the two devices is about 10 μm [3.92]

that the threshold voltage can be controlled by adjusting the film thickness of the oxide and nitride.

Figure 3.42 shows the transfer characteristics from a-Si and poly-Si TFTs fabricated on the same glass substrate. The gate insulator consists of a dual-layer oxide and nitride dielectric. The performance of the poly-Si TFTs are uniform, although the mobility is lower than the maximum of about

100 cm²/Vs that one is able to obtain with a monolithic fabrication process. The a-Si TFT exhibits a low leakage current of less than 1 fA/μm under a drain bias of 10 V, which is sufficiently low for the pixel switch.

With proper light shielding during the laser crystallization process, an a-Si TFT and a poly-Si TFT can be made side by side. Digital or analog circuits may utilize the low mobility and low leakage currents in a-Si for hybrid circuits. The minimum device separation is determined by the lateral thermal diffusion. Figure 3.43 shows a photograph of an a-Si and a poly-Si TFT built side-by-side with a separation of about 10 μm [3.47].

3.5 Conclusion

Materials studies show that laser-crystallized polysilicon contains larger grains with fewer defects than polysilicon prepared by other techniques. This is of particular significance for devices since large grains and few defects imply improved performance, such as higher electron mobility and lower leakage current for thin-film transistors. As a result, laser processing yields good devices and also allows for the creation of CMOS polysilicon on glass substrates, the integration of polysilicon silicon and amorphous devices on the same glass substrate, and the fabrication of self-aligned amorphous silicon thin-film transistors via laser doping. Thus, this processing technique provides a wide range of opportunities for large-area polysilicon electronics. One of the attractive areas is in the application to active matrix liquid crystal displays. The high carrier mobility of poly-Si TFTs allows the dimensions of the pixel switches to be scaled down. This leads to an improvement in the pixel aperture ratio and, therefore, to a brighter and lower-power display. The smaller size and improved performance of poly-Si TFTs also make them suitable for projection displays and high definition displays. The construction of CMOS poly-Si drive circuitry on the glass substrate reduces the number of off-substrate connections, leading to greater reliability, lower cost, and compact construction. With more than 20 years of development invested in low temperature poly-Si technology, new products, such as camera view-finders and small poly-Si displays, are now available in the market place.

Another application area of poly-Si devices on glass is in the combination of amorphous silicon photo sensors with poly-Si pixel switches and drive circuitry for large-area imaging. Similar to display applications, poly-Si TFTs improve the pixel fill factor (aperture ratio) and the packaging for flat panel imagers. In addition, the availability of both n-channel and p-channel TFTs enables digital and analogue circuit design. For example, with the high drive power of CMOS poly-Si TFTs, pixel amplifiers can be built to improve the imaging signal-to-noise ratio.

Other applications of low temperature poly-Si TFTs include printers, smart sensors, memory devices, and neural networks. Considerable development in manufacturing yield, device uniformity and stability, and device leak-

age current is still required to fully realize all these applications. Nonetheless, several major display manufacturers have prototype poly-Si display fabrication facilities and have plans to scale these up to mass production capacities in the near future.

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4 Large Area Image Sensor Arrays

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Abstract. The development of large area 2-dimensional amorphous silicon image sensor arrays has taken nearly ten years. At the time of writing, these devices are being introduced into the market for digital X-ray imaging applications such as medical radiography and non-destructive testing. This chapter describes the arrays, the range of applications and why the amorphous silicon technology is well matched to the particular needs of X-ray imaging.

4.1 Introduction

Amorphous silicon 2-dimensional (2-d) image sensor arrays owe their development to earlier research on linear image sensors and to the processing technology developed for active matrix addressed liquid crystal displays. Active matrix addressing of LCDs using amorphous silicon thin film transistors (TFT) was first proposed by LeComber et al. in 1979 [4.1], and was demonstrated by the same group in 1981 [4.2], although the idea of matrix addressing is considerably older. Shortly afterwards, a number of groups applied the matrix addressing technique to linear image sensors, combining the TFTs with amorphous silicon sensors to make arrays for scanners and FAX machines [4.3–5]. The linear sensors use the same addressing structures as is used in the 2-d arrays, but configured as a single line of sensors. The first sensors were Schottky barrier devices, but the better performance of p-i-n photodiodes soon became apparent.

The processing technology to create 1-d and 2-d matrix addressed arrays for scanning and display was also created in the early 1980's and has since been greatly refined due to the rapid development of the AMLCD market for lap-top computer displays. The sensor arrays use the same processing technology, and made the transition from 1-d to 2-d arrays of increasing size starting at the end of the 1980's [4.6].

This chapter begins with a description of the important devices – the photodiodes and TFTs – that make up the sensor arrays, and goes on to describe the arrays, the electronic systems that provide the control and readout, and the various applications in medicine, non-destructive testing, scientific imaging and document capture.

4.2 Devices

Thin film transistors, p-i-n diodes and photoconductors are the active devices in most image sensor arrays. The structure and properties of the key amorphous silicon devices are described before going on to discuss the arrays. Further information about photodiodes is contained in Chap. 7 on color sensors and Chap. 8 on position sensors, and closely related p-i-n devices are used in the solar cells described in Chap. 6. This chapter focuses on those properties that are of importance to the image sensors.

4.2.1 P-i-n Photodiodes

The ideal photosensor has a high sensitivity to illumination and negligible dark current. Either a photoconductor or a photodiode structure can be used, the distinction being that the photoconductor has ohmic electrical contacts while the photodiode has rectifying contacts, either a doped layer or a metal Schottky barrier. The merit of the photoconductor is that gain may be achieved, resulting in high photocurrent, although at the expense of a long response time. On the other hand, photodiodes exhibit exceptionally low leakage currents. Avalanche gain is a desirable property for high sensitivity photodiodes but has not been reported in a-Si:H, although it is observed in amorphous selenium [4.7].

The a-Si:H p-i-n photodiode is used as the light detector in image sensor arrays primarily to take advantage of its high quantum efficiency, low reverse bias leakage current and thin film structure. The diode is also used instead of the TFT as the switching element in some arrays, because of its good rectifying properties. The photodiode design is illustrated in Fig. 4.1 and consists of very thin p-doped and n-doped layers with a thicker undoped (i) layer in between. The doped layers provide rectifying contacts but do not contribute to the light sensitivity because doping causes a high density of charged dangling bond defects in a-Si:H – positive in n-type material and negative in p-type material [4.8]. The minority carrier lifetime in doped a-Si:H is therefore so small that most holes generated in the n-layer and electrons in the p-layer recombine before they can cross the reverse bias junction. On the other hand, the high defect density results in a very small depletion width, so that a doped layer thickness of 100 Å or less is sufficient to form the junction.

Incident light which is absorbed in the doped layer reduces the sensitivity to short wavelength illumination. Hence, particular care is needed to minimize such absorption if high sensitivity to blue light is required. Microcrystalline silicon or a-Si:C:H both have a lower absorption than a-Si:H and are often used in solar cells to enhance blue sensitivity [4.9]. This approach also works for sensor arrays, but has not been widely implemented because the extra blue sensitivity has not yet proved to be sufficiently important.

In many sensor arrays, the p-i-n photodiodes are etched to isolate the sensor from the neighboring pixels, as in the structure shown in Fig. 4.1. The

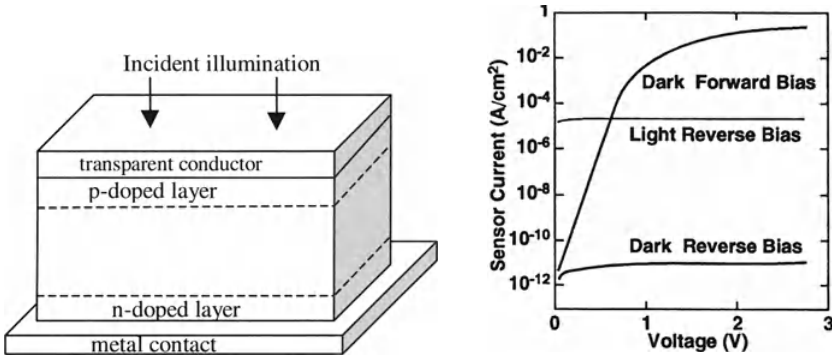


Fig. 4.1. Illustration of the structure of an a-Si:H p-i-n photodiode (*left*), and the forward and reverse bias electrical characteristics (*right*)

exposure of the edge of the diode can affect the leakage current, as is described shortly, particularly when the sensor area is small. The diode requires metal contacts on both top and bottom because the thin doped layers are not sufficiently conductive by themselves. For example, a 100 Å thick p-type a-Si:H layer has a sheet resistance of $10^{11} \Omega/\square$, and even the more conductive n-type layer is only $10^8 \Omega/\square$. A transparent conductor is required for the illuminated surface and indium tin oxide is commonly used.

The basic electrical characteristics of a p-i-n photodiode are shown in Fig. 4.1. The exponentially increasing forward bias current is typical of a diode, as is the low reverse bias current. The large increase in reverse current under illumination is the basis for its use as a light sensor.

The Sensor Photocurrent. Absorption of light in the sensor generates electron-hole pairs in the i-layer. The charges separate under the action of the electric field and cause a current to flow in the external circuit. The electric field includes the internal built-in potential and the applied reverse bias. The photocurrent, I_{PH} , resulting from a light flux, G_L , is given by

$$I_{PH} = G_L \eta_{QE}(V, \lambda) . \quad (4.1)$$

The quantum efficiency $\eta_{QE}(V, \lambda)$ comprises a wavelength-dependent absorption that generates electron-hole pairs, and a bias-dependent charge collection efficiency. In the absence of photoconductive or avalanche gain the quantum efficiency is always less than unity.

A typical quantum efficiency spectrum is shown in Fig. 4.2. The decrease at long wavelength is due to the low absorption coefficient of a-Si:H below the band gap energy, and the short wavelength decrease mostly arises from absorption in the upper doped layer and perhaps the transparent conductor. The peak quantum efficiency of 80–95% in optimized diodes occurs in the range 500–600 nm. The interference fringes seen in Fig. 4.2 are due to

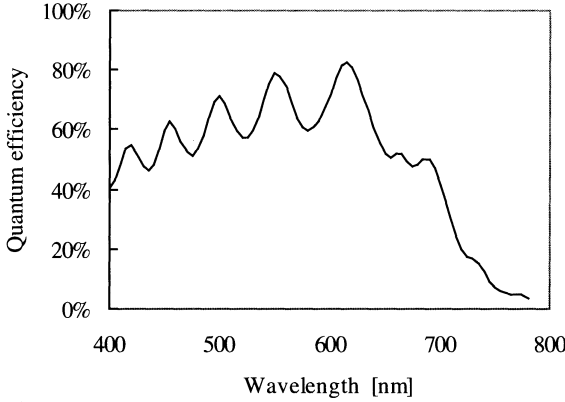


Fig. 4.2. Typical quantum efficiency spectrum of a p-i-n photo-diode with an ITO contact

the thin transparent overlayers to the photodiode, and the choice of materials and thickness can be designed as an antireflection coating for a selected wavelength range.

The charge collection efficiency depends on the applied bias and on the carrier recombination lifetimes. Dangling bond defects act as traps and limit the carrier lifetime, τ , such that the mean free path, L , of a carrier with drift mobility, μ , in a uniform applied electric field, F , is,

$$L = \mu\tau F . \quad (4.2)$$

Trapping will occur with high probability when L is smaller than the thickness of the sample. Hence, the collection efficiency is increased by large values of $\mu\tau$ and a high applied bias. In a device of thickness, t_F , the fraction, P , of charge that is collected is given by the Hecht formula,

$$P = \frac{\mu\tau F}{t_F} [1 - \exp(-t_F/\mu\tau F)] \approx 1 - \frac{t_F}{2\mu\tau F} , \quad (4.3)$$

where the approximation on the right applies when $\mu\tau$ is large [4.10].

The values of $\mu\tau$ are usually different for electrons and holes and depend on the density of traps, N_D , and the capture cross-section, σ , as [4.8],

$$\mu\tau = \frac{\text{const}}{\sigma N_D} . \quad (4.4)$$

Neutral dangling bonds in undoped a-Si:H can trap both electrons and holes, but the cross section for holes is greater, so that $\mu\tau$ is correspondingly 5–10 times smaller than for electrons. The high density of charged defects in doped a-Si:H strongly trap minority carriers. In low defect density a-Si:H, typical values are $(\mu\tau)_{\text{electron}} = 3 \times 10^{-7} \text{ cm}^2/\text{V}$ and $(\mu\tau)_{\text{hole}} = 5 \times 10^{-8} \text{ cm}^2/\text{V}$ [4.8].

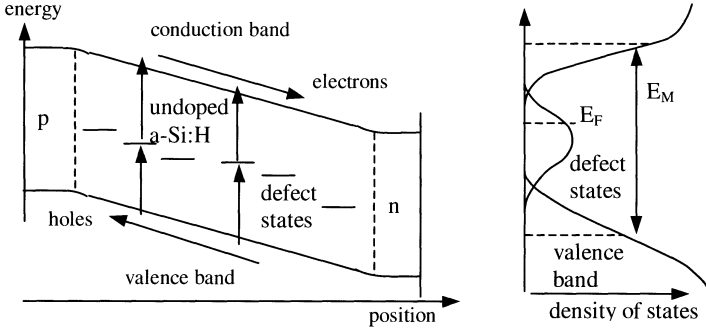


Fig. 4.3. *Left:* band model for bulk thermal generation through defect states in the band gap. *Right:* density of states model for amorphous silicon

Reverse Bias Dark Current. The photodiode reverse bias dark current may have components from the bulk, the doped contacts or the exposed diode perimeter. In optimized devices the bulk current dominates and is attributed to the thermal generation of electrons and holes via mid-gap defect states, as illustrated in Fig. 4.3 [4.11, 12]. Electrons are thermally excited from the valence band to empty or singly occupied defect states, and are later excited from these states to the conduction band, resulting in electron-hole pairs which are collected by the applied field. The equilibrium excitation rates of electrons and holes must be equal, which ensures that the dominant contribution is from states at the middle of the band gap. The thermal generation current, J_{th} , is given by [4.11],

$$J_{th} = eN(E)kT\omega_0 \exp(-E_M/2kT) vol. , \quad (4.5)$$

where $N(E)$ is the density of defect states in the middle of the gap, E_M is the mobility gap energy, $vol.$ is the volume of the sample, and unity collection efficiency is assumed for the generated charge.

Equation (4.5) predicts that the current is thermally activated with half the mobility gap energy and experiments indeed find an activation energy of about 0.85–0.9 eV, in support of this model (see Fig. 4.4). This activation energy causes the current to increase by an order of magnitude with a temperature increase of 20°C near room temperature. Thus, the leakage current of an image sensor array may be reduced by modest cooling, but the array will not operate well at elevated temperature.

The absolute magnitude of the current is also consistent with the thermal generation model. Figure 4.4 shows the reverse current at room temperature after the application of a field. The current decreases to a steady state value of $1\text{--}2 \times 10^{-11}$ A/cm², which is consistent with a midgap defect density of 10^{16} cm⁻³eV⁻¹ and a mobility gap of 1.8 eV in (4.5), both of which are within the accepted range for amorphous silicon [4.8]. The slow increase of the steady state current with applied field is most probably explained by a field lowering

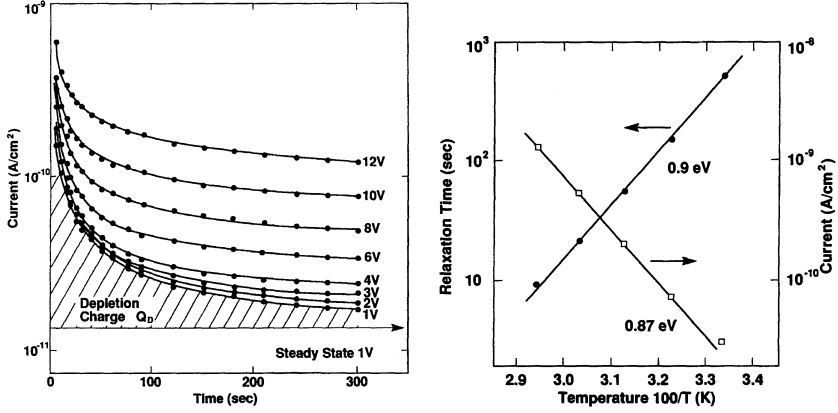


Fig. 4.4. *Left:* Measurements of the room temperature thermal generation current, showing the transient decay after the bias is applied. *Right:* Temperature dependence of the current and relaxation time showing an activation energy of about half the band gap

of the excitation energy [4.12]. The room temperature leakage current in a typical device is indeed remarkably small – the data in Fig. 4.4 indicates a current below 2×10^{-15} A in a photodiode of size $100 \times 100 \mu\text{m}$.

Figure 4.4 also shows that the current is larger when the field is first applied and decreases quite slowly to the steady state value. The excess current is explained by the depletion of charge from mid-gap defect states [4.11]. Undoped a-Si:H is slightly n-type, with its Fermi energy above the middle of the band gap (Fig. 4.3). After the bias is applied, the occupied states above mid-gap are depleted of charge, and depletion continues until the steady state thermal generation is established. The amount of depletion charge is approximately,

$$Q = eN(E)\Delta E \text{ vol.} \cong 1.6 \times 10^{-8} \text{ C/cm}^2, \quad (4.6)$$

where ΔE is the position of the equilibrium Fermi energy above mid-gap, estimated to be 0.1 eV, and the diode thickness is $1 \mu\text{m}$. The estimated depletion charge is consistent with the measured decay and the slow decay time is due to the low excitation probability from mid-gap states, and the thermal activation energy of the relaxation time is also consistent with this explanation.

The exposed periphery of the photodiode provides a different source of leakage current which is particularly significant in small devices. In the presence of both bulk and peripheral components, the total current in a square diode of edge length d_S , is given by,

$$I_{\text{total}} = I_B d_S^2 + 4I_P d_S, \quad (4.7)$$

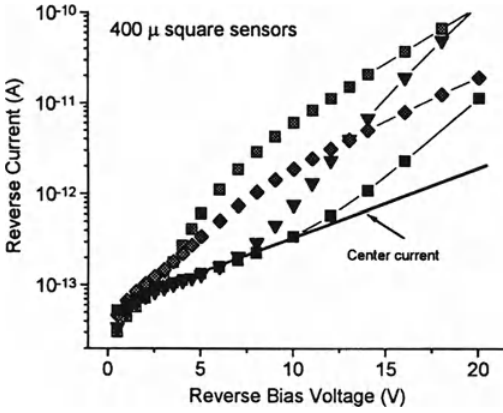


Fig. 4.5. Examples of the bias dependence of p-i-n photodiodes. The variation is largely due to peripheral currents, while the bulk leakage current is similar in each device

where I_B (cm^{-2}) and I_P (cm^{-1}) are the bulk and peripheral conductance. The peripheral current increasingly dominates when d_S is sufficiently small, and the different dependence on the pixel size allows an easy experimental method to determine the relative magnitude of the two components.

Figure 4.5 illustrates the bias dependence of the reverse current in sensors of size $400 \times 400 \mu\text{m}$ [4.13]. The group of samples exhibits much variability in the current when the bias is large. Measurements with different pixel sizes confirm that the excess current is due to the peripheral contribution and that the bulk current follows the line indicated. The mechanism of peripheral current is not definitely identified, but is probably related to band bending at the a-Si:H surface. The different edge leakage currents are no doubt explained by the process variations in the etching and passivation during fabrication of the device. Unpassivated sensors are very sensitive to the ambient atmosphere and generally have larger edge leakage currents.

The Forward Current. The characteristics of the photodiode are completed by the forward bias current which is illustrated in Fig. 4.6 [4.14]. Although photodiode sensors operate in reverse bias, the forward current characteristics are a useful tool for understanding the device, and a high forward current is needed for diode addressed arrays. The p-i-n device exhibits diode behavior with a current increasing exponentially with bias, V ;

$$I_F = I_0 \exp(eV/nkT). \quad (4.8)$$

The ideality factor, n , is generally 1.3–1.5, depending on the thickness, deposition conditions and quality of the contacts [4.15]. Schottky diodes using Pt or Pd contacts instead of the p-type contact follow a similar form except that the current is larger and the ideality factor is close to unity.

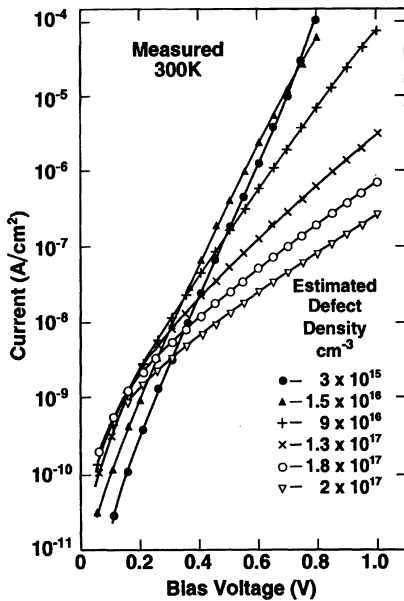


Fig. 4.6. Examples of the forward bias characteristics of an a-Si:H p-i-n diode, showing the effects of a high defect density in the undoped layer

The departure from the exponential slope at larger bias is due to a series resistance, which can originate in the bulk a-Si:H material if the device is thick or defective, or in the contacts, which are often thin films of significant resistance. Figure 4.6 illustrates the effect of high defect density in the undoped layer.

Semiconductor theory attributes an ideality factor $n = 1$ to thermionic emission and $n = 2$ to a generation-recombination mechanism [4.16]. The relative contribution of the two mechanisms depends on the height of the barrier and the density of recombination centers. The thermionic emission rate decreases with a larger barrier height, while generation-recombination increases with defect density. A-Si:H diodes with high work function metal contacts such as Pt or Pd, exhibit thermionic emission [4.17]. However, the p-type contact has a large enough barrier to suppress thermionic emission in favor of the generation-recombination mechanism. Modeling studies show that even though the ideality factor is < 2 , there is essentially no contribution from thermionic emission and the intermediate value of n is entirely due to the distribution of localized states in a-Si:H, particularly the band tails [4.14]. Furthermore, the fact that the reverse current of the p-i-n device is due to thermal generation is obviously consistent with the identification of recombination-generation as the forward current mechanism.

Current Stability. The signal of interest in an image sensor is the difference between the photocurrent and the dark current. An image acquired in the dark is subtracted from the measured image to correct for any leakage current or other fixed signals. The long term stability of the dark current therefore determines whether the correction data can be obtained only once or whether it must be obtained frequently to reflect a time-varying current. Clearly, current stability is less important when the dark current is small, and therefore low leakage devices are desirable.

There are several potential sources of instability in a-Si:H photodiodes. Prolonged illumination of amorphous silicon is well known to cause a reversible metastable defect generation process, known as the Staebler-Wronski effect [4.18]. However, this mechanism plays almost no role in the sensor arrays because the total illumination of sensors under normal conditions is much less than the magnitude needed to create defects. A typical sensor array saturates with an illumination of $< 10^{-7} \text{ W/cm}^2$, whereas sunlight illumination at 10^{-1} W/cm^2 is 6 orders of magnitude more intense and even then takes hours or days to cause observable defect creation.

The actual sources of leakage current instability are all related to the mechanism of conduction. Figure 4.4 shows that the thermal generation current decreases slowly after the application of a bias, and consequently several seconds are needed for stable operation. The peripheral leakage current is often found to increase slowly with time, possibly due to a build-up of space charge in the passivation layer [4.13]. Minimization of this mechanism involves careful passivation and is helped by maintaining a low applied bias. The strong temperature dependence of the leakage current (Fig. 4.4) is another mechanism for current variation if the array temperature is allowed to vary.

The bias dependence of the photodiode current is an indirect cause of leakage current changes in sensor arrays, because the device is usually operated in charge integration mode. As light falls on the sensor, charge is collected at the electrodes and the effective bias voltage across the sensor decreases. Hence the leakage current correction measured in the dark may not apply precisely to an illuminated sensor.

For all the above reasons, it is important that the sensor has a very low leakage current so that the instability effects are negligible. P-i-n diodes satisfy this requirement better than Schottky diodes, and very stable dark currents are obtained near room temperature and at fairly low bias.

Thick Photodiode Sensors. Early in the research on sensor arrays, very thick amorphous silicon p-i-n photodiodes were investigated for detection of high energy radiation [4.19–22]. A thick layer increases the energy loss of an incident energetic charged particle – an electron or alpha particle – within the sensor, and results in a correspondingly larger signal. For reasons given in Sect. 4.3.4, recent research favors the use of other semiconductor materials for

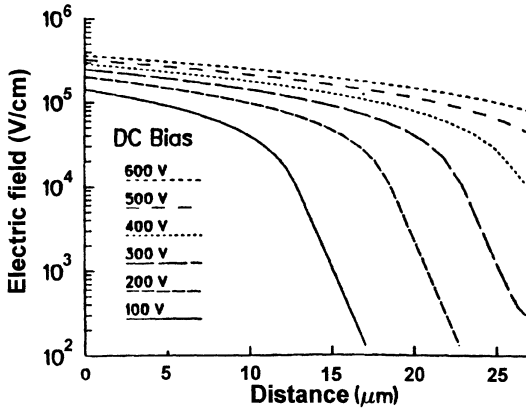


Fig. 4.7. Calculated electric field profiles in a 27 μm p-i-n photodiode showing full depletion at a bias larger than 400V [4.22]

the fabrication of thick sensors to detect ionizing radiation. However, effective amorphous silicon particle sensor diodes have been made with thickness of 20–50 μm . It is essential that the thick device is fully depleted, because the diffusion length of carriers in a-Si:H is very small, and essentially no photocurrent flows in a field-free region.

The depletion length, W , is determined by the space charge within the a-Si:H layer,

$$W = \sqrt{2\epsilon\epsilon_0 V_B / eN_{\text{DI}}}, \quad (4.9)$$

where V_B is the applied bias voltage and N_{DI} is the density of ionized defect states. The thick p-i-n device is in a condition of deep depletion, in which the ionization state of defects is governed by the relative excitation rates of electrons and holes in the defect states near the middle of the band gap. Measurements show that the density of ionized states is about 1/3 of the total density of defects, and for good quality a-Si:H, N_{DI} is about $7 \times 10^{14} \text{ cm}^{-3}$ (4.6) [4.22]. Figure 4.7 shows calculated field profiles for a 27 μm thick p-i-n sensor based on the measured ionized defect density [4.23]. The depletion layer increases with bias and measurements confirms the prediction that full depletion occurs at 300–400 V.

The depletion length increases with applied bias, and is ultimately limited by breakdown or an excessive leakage current, due to the high field at the electrical contact. The field at the contact can be reduced by growing the films with buried doped layers, giving a p-i-p-i-n-i-n structure [4.23]. The internal lightly-doped layers are ionized and cause a reduction of the field at the contact. Such devices are indeed found to have higher breakdown fields, and higher sensitivity to alpha particles.

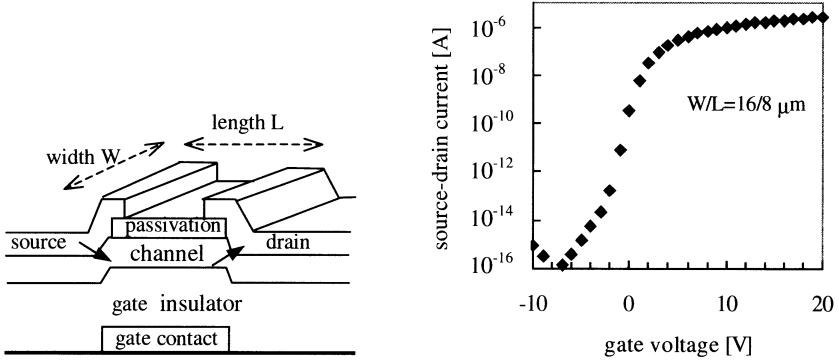


Fig. 4.8. Bottom gate TFT structure with source and drain contacts overlapping the channel (*left*). The transfer characteristics (*right*) show low leakage and a high on/off ratio

4.2.2 Thin Film Transistors

Thin film transistors, made of both amorphous and polycrystalline silicon are discussed in more detail in Chaps. 2 and 3, and only those properties of most interest for the image sensor arrays are discussed here. The most common a-Si:H TFT structure, shown in Fig. 4.8, has a bottom gate with a silicon nitride gate dielectric, an undoped a-Si:H channel, and n-type source and drain contacts. This structure has proved to be less prone to charge trapping effects than top gate designs, in part because the silicon nitride layer can be deposited at about 350°C. The TFT operates in the n-channel accumulation mode because of the particular material properties of a-Si:H. Electrons have higher mobility than holes (hence n-channel operation), and the high defect density of doped a-Si:H precludes a depletion mode of operation.

The silicon nitride gate dielectric, the a-Si:H channel, and a top nitride passivation layer are all deposited by plasma enhance chemical vapor deposition. In this fabrication process, the source-drain contacts are deposited over the protecting passivation layer which is self-aligned to the gate. The overlap of the source and drain contacts over the TFT channel ensures reliable contacts, but provides some coupling capacitance to the gate which has a significant effect on the performance of the sensor array.

The principal attributes needed for image sensors are an on-resistance of a few MΩ, a very low off-resistance of $> 10^{14} \Omega$, small size, and low parasitic capacitance. The reasons for these features are developed further in Sect. 4.3.2 describing the array operation. The TFT electrical characteristics obey the usual semiconductor relations for MOS transistors. The image sensor mostly operates in the linear regime for which the on-resistance, R_{ON} , the ratio of the source-drain voltage and current, is [4.8],

$$R_{ON} = V_{SD}/I_{SD} = [C_{G\mu FE}(V_G - V_T)W/L]^{-1}, \quad (4.10)$$

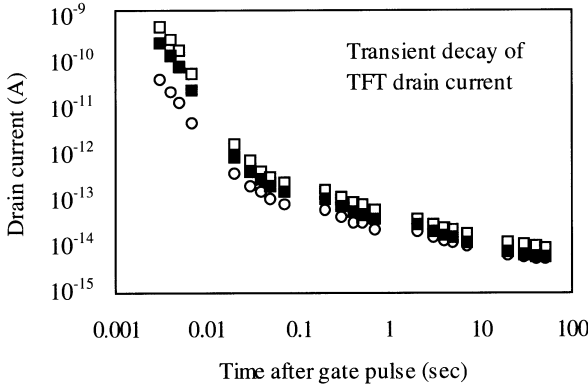


Fig. 4.9. Transient response of the TFT leakage current showing the slow decay to the steady state value. The TFT has $W/L = 75/8.5\mu\text{m}$ and the Source-drain voltage is 5 V (circles), 7.5 V (closed squares) and 12.5 V (open squares) [4.26]

where V_G is the gate voltage, V_T is the threshold voltage, W is the TFT width and L is the length. A nitride thickness of $3000\text{ \AA}$ has a gate capacitance, C_G of $5 \times 10^{-8}\text{ F/cm}^2$, and a field effect mobility, μ_{FE} , of $0.8\text{ cm}^2/\text{Vs}$, yields,

$$R_{ON} = 25[(V_G - V_T)W/L]^{-1}\text{ M}\Omega. \quad (4.11)$$

An on-resistance of a few $\text{M}\Omega$ is achieved with a width-to-length ratio, $W/L \sim 1\text{--}5$ and $V_G - V_T \sim 10\text{ V}$, and the threshold voltage is usually $0\text{--}2\text{ V}$.

The TFT transfer characteristics are shown in Fig. 4.8 [4.24]. In the sub-threshold region with V_G below V_T , the current increases exponentially. The minimum leakage current is attained with V_G between -5 V and -10 V , and the corresponding off-resistance is extremely large, $> 10^{15}\Omega$. Contributing to the low current are the barrier formed by the n-type source and drain contacts, the low density of states at the a-Si:H/nitride interface and the low mobility of a-Si:H. The leakage current is much lower than in polysilicon devices and make the a-Si:H device preferred for image sensors. The leakage current is probably a bulk generation current in the channel [4.25], similar to the mechanism of photodiode leakage described in Sect. 4.2.1.

There is a significant slow transient decay to the TFT leakage current when the device is turned off, as indicated in Fig. 4.9 [4.26]. The slow decay is similar to that of the photodiode in Fig. 4.4 and reaches a steady state only after several seconds. The effect is most likely due to the release of trapped charge and affects the image sensor by providing a source of fixed charge that can be subtracted from the signal provided that the signal and offset images are acquired with the same timing conditions.

The capacitance of the TFT is a combination of the channel capacitance, C_GWL , and the parasitic capacitance of the source and drain overlaps, which are also proportional to W . Smaller feature sizes greatly reduce the capacitance, and since this is a major contribution to the electronic noise of the

imager, there are immediate benefits in reducing the photolithography feature sizes for the large area arrays.

Undoped a-Si:H is a highly photoconductive material, so that the TFT leakage current is sensitive to illumination even when the channel is very thin. It is therefore usually necessary to provide a light shield for the TFT to obtain the very low leakage currents that are required. Shielding is readily accomplished with a metal line placed over the TFT, and the gate metal already provides a light shield from below.

Other TFT Materials. Arrays are also fabricated with different active semiconductor materials for the TFTs. The two most widely explored are polycrystalline silicon and CdSe. The use of polycrystalline silicon in active matrix LCDs has been investigated extensively, and aspects of the technology are described in Chap. 2. The interest in poly-silicon is to provide higher performance devices to allow the drive circuitry to be integrated into the array, and LCDs with completely integrated drivers have recently been introduced onto the market. The main issue with poly-silicon is to fabricate TFTs on glass substrates. High temperature processing that closely follows the silicon IC technology uses thermal oxidation to fabricate the TFT gate dielectric and annealing to activate dopants. This process results in excellent TFTs, but cannot be performed on glass substrates. Efforts to use intermediate temperatures near the glass softening point have given way to laser crystallization that allows the silicon films to be melted without heating the glass substrate. The laser crystallized material has a mobility of typically $20\text{--}100\text{ cm}^2/\text{Vs}$, which is high enough to fabricate integrated drivers [4.27]. However, the off-current is significantly higher than for a-Si:H, and as is discussed in Sect. 4.3.2, a low off-current is essential for the pixel switch of image sensor arrays. This requirement has led to the development of a hybrid technology that allows selective crystallization of some TFTs so that both devices can be made on the same array, and this is the subject of Chap. 3.

Polycrystalline CdSe has also been studied as a TFT material [4.28]. The devices are usually fabricated with a bottom gate and an SiO_2 gate dielectric. Low temperature deposition is consistent with the use of glass substrates. The carrier mobility is usually in the range $50\text{--}150\text{ cm}^2/\text{Vs}$, and sometimes even higher. The leakage current can be made to be almost as low as a-Si:H, with the low values helped by the use of a double gate structure. Despite the good properties, CdSe TFTs are not widely used, evidently because the processing is difficult. Amorphous and poly-crystalline silicon benefit greatly from the fact that the processing chemistry is very similar to that used for the single crystal silicon IC industry and so can benefit from the extensive developments that have taken place.

4.3 Sensor Array Designs

The image sensors are two-dimensional arrays of pixels. Each pixel senses the radiation that impinges on it and stores the corresponding charge until it is transferred to the external electronics. The general architecture of the pixel, shown in Fig. 4.10, illustrates the various elements. The pixel contains a sensor to respond to incident radiation, a charge storage capacitor to hold the charge until it is read out, and a pixel switch to control the readout. Future imagers may also contain some signal processing capability in the pixel. The pixels are connected together with common address lines that cross the array – a bias contact for the sensor, address lines to trigger the pixel switch and data output lines to transfer the charge to the external electronics.

The array design attempts to optimize the most important performance attributes of the imager which are the size, spatial resolution, sensitivity and dynamic range. The fact that the performance of these parameters tends to conflict with each other represents a challenge for design optimization. For arrays that are typically 20–40 cm in size, the number of pixels ranges from 100 000 to 10 000 000, depending on the pixel pitch. The spatial resolution is ultimately limited by the pixel size, and the interesting range is from 50 μm up to 300–500 μm , depending on the application. Sensitivity, in terms of the signal from a pixel, depends on the quantum efficiency of the sensor, and is also proportional to the sensor area in the pixel. Thus, high resolution arrays are intrinsically less sensitive than low resolution arrays, in the sense that for a fixed illumination flux, the charge developed per pixel is smaller.

The dynamic range is the ratio of the maximum signal to the noise, and highlights the need for low noise performance. However, the overall performance of the image sensor depends on a great many factors relating to the specific imaging environment.

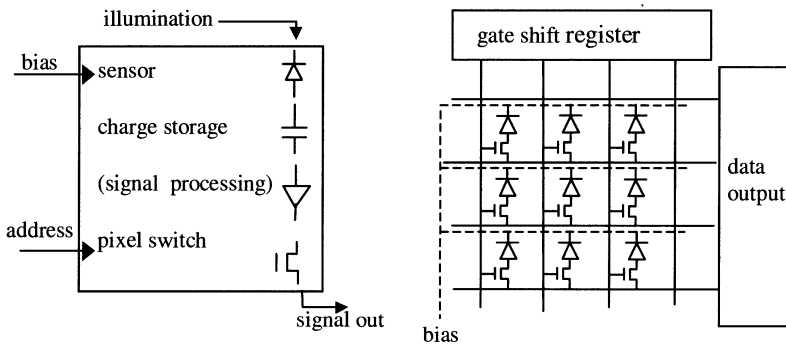


Fig. 4.10. The general design of the pixel (*left*), and the matrix addressing (*right*) of an image sensor array

4.3.1 Matrix Addressed Readout

The read-out of the image information is performed by matrix addressing, similar to that used for liquid crystal displays (Chap. 2). Matrix addressing reduces the number of individual contacts that must be made to the array, and consists of intersecting address lines and data sensing lines (Fig. 4.10). The address lines activate the pixel switches along one column of the array and those pixels transfer their signal to the data sensing lines, which are connected to the external electronics. After the measurement of the signal is complete, the next address line is activated. Thus the array is read out one line at a time until the image transfer is complete. Normally the gate lines are addressed in sequential order across the array, but in principle the columns of pixels could be sampled in any arbitrary order. Several different embodiments of this general design have been proposed and tested. In most cases the pixel switch is a thin film transistor (TFT), but diode-addressed imagers have been successfully fabricated, as they have for liquid crystal displays. Although amorphous silicon TFTs have been widely used, both poly-silicon and CdSe devices are alternatives. The a-Si:H p-i-n photodiodes form excellent light sensors (and X-ray imagers when coupled to a scintillator), while selenium and other photoconductors are also in use for X-ray sensitive imagers. Some more complex a-Si:H light sensor designs that could be used in image sensor arrays are described in Chap. 7.

4.3.2 TFT Addressed, p-i-n Photodiode Arrays

Much of the a-Si:H image sensor data is obtained from array designs which have an a-Si:H p-i-n photodiode together with a TFT pixel switch, and the following description of this device is used to develop many general aspects of image sensors which apply to other designs. A photograph of one such pixel design with a size of $127\text{ }\mu\text{m}$ is shown in Fig. 4.11, along with the pixel circuit [4.28]. The pixel is bounded on each side by the address lines. In the lower left corner of the pixel is the TFT whose gate is connected to the vertical address line to the left. The TFT source and drain contacts are connected to the photodiode and to the data line respectively. The bias contact runs horizontally across the pixel and in this particular design is placed directly over the TFT to provide a light shield. The sensor occupies the available space in the pixel between these other elements.

A schematic cross-sectional view of the pixel is shown in Fig. 4.12 and illustrates one particular structure of the array. The TFT is a bottom gate device as described in Sect. 4.2.2. The sensor is deposited directly on top of the source contact metal. For the design under consideration, the n-type layer is deposited first and the top junction is p-type, which is covered with a transparent conducting film, usually indium tin oxide. The sensor is patterned to provide isolation from the adjacent pixels, and a passivation layer is applied to protect the side walls of the sensor and to provide an inter-layer insulator

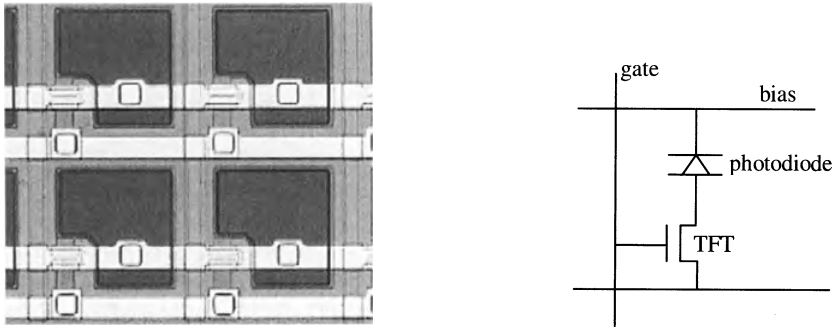


Fig. 4.11. Photograph of sensor array pixels showing the vertical gate line, the horizontal data and bias lines and the TFT in the *bottom left corner* [4.24]. The pixel size is $127\ \mu\text{m}$ and the sensor fill factor is 57%. (*Right*) The pixel circuit

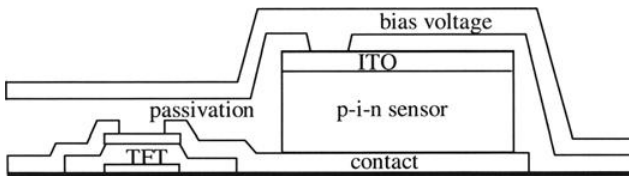


Fig. 4.12. Cross-sectional view of a pixel showing the a-Si:H TFT and p-i-n photodiode sensor

for the next metal layer. The top metal layer is used for the data address line and the bias voltage contact to the sensor, as well as the light.

Overview of Array Operation. The array performs three operations – signal acquisition, signal readout, and reset. Generally, the array is repetitively cycled through these operations, and the time for each cycle is referred to as the *frame time*. The signal acquisition begins immediately after the pixel is reset. The TFT is turned off and the sensor is charged to the full bias voltage. Incident light absorbed in the photodiode, creates electron–hole pairs which drift to the contacts and discharge the sensor. The thin sensor has a significant capacitance which stores the charge – the pixel circuit in Fig. 4.11 shows the sensor as both a diode and a capacitor.

When n photons are incident on the photodiode, it discharges by an amount $Q_S = \eta_{QE} n e$, and the voltage across the sensor is reduced to V_{SIG} , where,

$$V_{SIG} = V_B - Q_S / C_S, \quad (4.12)$$

provided that the charge is insufficient to discharge the sensor capacitance completely. Although the sensor is discharged by the light, it is convenient to think of Q_S simply as the signal charge, and it is frequently referred to in

this way. Thus, the signal charge is initially zero, and increases in proportion to the illumination flux until either pixel saturation is reached or readout occurs.

Readout is initiated when the TFT is switched on, which causes the lower contact of the sensor to be restored to the data line voltage. The charge Q_S passes from the data line to the photodiode and this amount of charge required to reset the sensor is recorded by the external electronics as the signal. Thus, the measurement of the signal charge and the reset of the photodiode are performed simultaneously.

The basic operational requirements of the pixel are therefore to convert the light flux to charge as efficiently as possible, to store the charge without loss during signal acquisition and to transfer it completely and quickly during readout. The next sections discuss the details of these operations and the design issues that allow the array to acquire images at high speed and with minimum distortion or loss of signal.

Sensitivity and Fill Factor. The design of Fig. 4.12 is one in which the sensor occupies the space remaining between the address lines and TFT. The fraction of the pixel area which is occupied by the exposed sensor surface is known as the *fill factor*, F_F , and it affects the overall sensitivity of the array. The photodiode charge that results from an incident light flux of G_L photons/cm² on a square pixel of edge size, d , is,

$$Q_S = eF_F\eta_{QE}G_Ld^2 . \quad (4.13)$$

High sensitivity is obtained with low electronic noise together with high fill factor, collection efficiency and pixel size. The minimum detectable charge is defined to be equal to the electronic noise, q_N , so that the sensitivity can be given in terms of a noise equivalent power, expressed as the light flux, G_{NE} , given by,

$$G_{NE} = q_N/(eF_F\eta_{QE}d^2) . \quad (4.14)$$

For the pixel design under consideration, the fill factor is determined by the size of the pixel and the processing design rules. A simple, illustrative model for the fill factor is,

$$F_F = (d - a)(d - b) - c , \quad (4.15)$$

where d is the pixel size, a and b are respectively the space occupied by the address lines in the gate and data directions, and c is the additional area taken up by the TFT. Figure 4.13 shows the fill factor according to (4.15) as a function of pixel size for design rules that approximately correspond to present arrays, as well as with each of the values, a , b and c , reduced by a factor 2. The fill factor approaches unity at large pixel sizes, and drops rapidly to zero with sufficiently small pixels. Present photolithographic manufacturing processes allows a fill factor of about 50% with 100 μm pixels and such designs

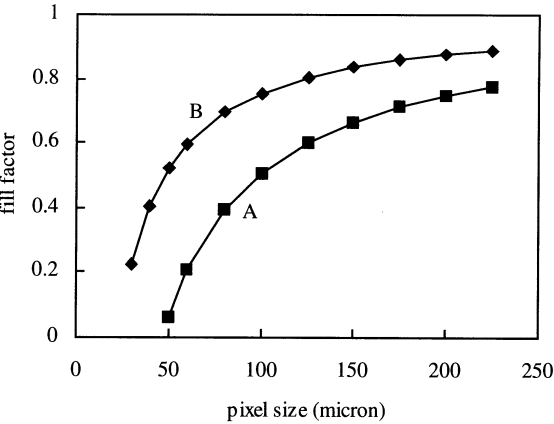


Fig. 4.13. Calculated fill factor vs pixel size for the model of (4.15). Curve A uses values, $a = 20\text{ }\mu\text{m}$, $b = 30\text{ }\mu\text{m}$, $c = 400\text{ }\mu\text{m}^2$, roughly corresponding to present design rules, and curve B has roughly half these values

are therefore quite adequate for the larger pixel arrays [4.30]. However, this design has insufficient fill factor for higher resolution devices, and the solution for such arrays is either improved design rules – which will undoubtedly come with time – or the high fill factor designs that are discussed in Sect. 4.3.3.

Table 4.1 shows the sensitivity, G_{NE} , for various pixel sizes, calculated from the fill factor model. The results assume a minimum detectable charge of 1000 electrons (0.16 fC), which is in line with current imaging systems, and a typical sensor quantum efficiency, η_{QE} , of 0.8. The rapid decrease in G_{NE} with pixel size is due to a combination of the increased fill factor and pixel size. The value of $2.5 \times 10^{-12}\text{ W/cm}^2$ at a pixel size of $150\text{ }\mu\text{m}$ illustrates the extraordinary ability of these devices to detect a very weak light flux.

Figure 4.14 shows how the maximum sensor charge, $Q_{S\text{MAX}} (= C_S V_B)$, increases with pixel size, again based on the same fill factor model and a bias voltage of 5V. For the 1000 electron minimum detectable charge, the dynamic range is in the range 10 000–100 000 for pixel sizes above $100\text{ }\mu\text{m}$. These devices therefore have excellent dynamic range, and in most cases it

Table 4.1. Calculated values of the noise equivalent power for different pixel sizes

Pixel size (μm)	Noise equivalent power, G_{NE} (W/cm^2)
50	3×10^{-10}
100	8×10^{-12}
150	2.5×10^{-12}
200	1.3×10^{-12}

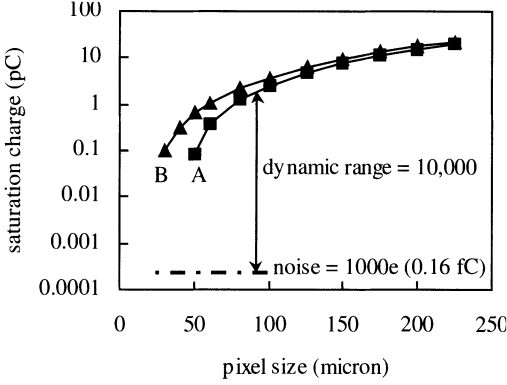


Fig. 4.14. The maximum sensor charge vs pixel size based on the fill factor model of (4.15). A and B refer to the same parameter values as in Fig. 4.13. The dynamic range of the sensor is indicated

is the readout electronics rather than the array itself that limits the overall dynamic range of the complete imaging system.

Readout Timing. The TFT and the photodiode in the pixel determine the time required to read out the image to the external electronics. During the time that the TFT is switched on, the signal charge stored on the sensor capacitance, C_S , is transferred through the TFT to the data lines. The fraction of charge transferred in time t , is $\exp[-t/R_{ON}C_S]$ when the TFT has an on-resistance of R_{ON} . Several time constants are required to transfer the charge completely (i.e., 99.3% of the charge is transferred after 5 time-constants and 99.995% after 10). The minimum time, τ_{RO} , required to read out the complete image of N gate lines, is therefore,

$$\tau_{RO} = 10 N R_{ON} C_S, \quad (4.16)$$

where 10 time constants are assumed for definiteness. For example, an array with 1000 lines, 1 pF pixel capacitance and 3 M Ω TFT on-resistance, can be read out in 30 ms. The value of τ_{RO} sets a lower limit on the imager frame time.

It is of interest to understand how the minimum readout time varies with the size and resolution of the array, for which a simple scaling analysis can be given [4.29]. The sensor capacitance is proportional to the pixel area and the fill factor ($C_S \approx C_{SO} F_F d^2$), while the TFT is limited in size by the pixel dimension ($R_{ON} \approx R_{TO} d$), where C_{SO} is the sensor capacitance per unit area, R_{TO} is the TFT resistance for unit width. Equation (4.16) therefore becomes,

$$\tau_{RO} = 10 N R_{TO} C_{SO} F_F d = 10 R_{TO} C_{SO} F_F L_D = 10^{-3} F_F L_D, \quad (4.17)$$

where $L_D (= Nd)$ is the size of the array in centimeters. For this simple analysis, the minimum readout time is independent of the pixel size, and increases with the linear dimension of the array. The reason is that the shorter time constant of small pixels is offset the larger number of gate lines in such an array. High resolution arrays can, in principal, be read out faster than lower resolution arrays for the same area because the sensor fill factor is smaller. The value of 10^{-3} given on the right-hand side of (4.17) uses typical values for amorphous silicon sensors and TFTs (a sensor thickness of $1\text{ }\mu\text{m}$, TFT channel length of $10\text{ }\mu\text{m}$, mobility $0.8\text{ cm}^2/\text{Vs}$, gate voltage 10 V etc). Video rate output can be sustained for array sizes up to $20\text{--}30\text{ cm}$, and even larger by optimizing the design, and this speed is required for X-ray fluoroscopy applications described in Sect. 4.5.1. In practice, and particularly for a large high resolution array, the speed is more constrained by the performance of the external electronics than by the array itself.

High readout speeds also require that the time constants for the gate and data lines are adequate. The address line capacitance for a typical large area array (> 1000 lines) is approximately 100 pF , so that a line resistance less than about $3 \times 10^4\text{ }\Omega$ is needed for a time constant $< 3\text{ }\mu\text{s}$. Although this seems a large value for a metal, the line is so long and thin that it corresponds to a resistance of about $0.5\text{ }\Omega/\square$, which is readily obtained by thin films of aluminum, but not by some other metals such as chromium. The choice of metals for the address lines is an important factor determining the performance of high speed arrays.

For the detection of very weak illumination, it is often desirable to integrate the signal for a long time. The limitation on the maximum integration time is the leakage current of the sensor (I_{LS}) and the TFT (I_{LT}). The sensor leakage causes a build-up of sensor charge on the pixel, which eventually exceeds the maximum sensor charge, while the TFT leakage causes the loss of sensor charge and therefore a non-linear image response. The leakage currents depend on the bias on the devices, which in turn depends on the sensor charge [4.30]. The sensor charge accumulating in the dark is given by,

$$\frac{dQ_S}{dt} = I_{LS}(Q_S) - I_{LT}(Q_S) , \quad (4.18)$$

with,

$$Q_S = C_S(V_B - V_0) , \quad (4.19)$$

where V_0 is the small bias on the TFT source after reset, due to the feed-through capacitance discussed below. Experimental observations indicate that that the sensor leakage current is nearly independent of bias while the TFT is ohmic with resistance R_{OFF} . These approximations give,

$$\frac{dQ_S}{dt} = I_{LS}(Q_S) - V_0/R_{OFF} - Q_S/R_{OFF}C_S , \quad (4.20)$$

which has the solution,

$$Q_S = R_{OFF}C_S(I_{LS} - V_0/R_{OFF})[1 - \exp(-t/R_{OFF}C_S)] . \quad (4.21)$$

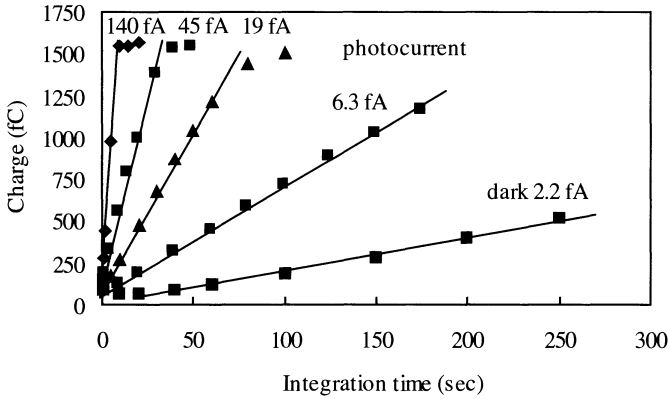


Fig. 4.15. Sensor charge in the dark and with weak illumination, at long integration times [4.30]

When $t \ll R_{\text{OFF}}C_S$,

$$Q_S = (I_S - V_0/R_{\text{OFF}})t. \quad (4.22)$$

The sensor charge initially increases at a rate corresponding to the sensor leakage currents (because V_0 is usually small) and eventually approaches a steady state value with a time constant of $R_T C_S$ provided that the sensor does not saturate first. Figure 4.15 shows long integration time data obtained with weak illumination and in the dark using a room temperature imager with $127 \mu\text{m}$ pixel size, 35% fill factor and sensor capacitance 0.5 pF . The dark signal increases linearly with integration time, apart from a small deviation at short times, and corresponds to a dark current of 2.4 fA , while weak illumination causes a more rapid increase in signal charge as is expected. The dark current is consistent with the sensor leakage measurements in Fig. 4.5 scaled to the area of the sensor. There is no indication of the signal reaching a steady state value even after 250 s , which implies that $R_{\text{OFF}}C_S > 750 \text{ s}$. This value places a lower bound on the TFT resistance of $1.5 \times 10^{15} \Omega$ for a device with $W/L = 1.5$. Again, the results are consistent with the TFT measurements in Fig. 4.8. Since both the sensor and TFT leakage currents depend strongly on temperature, cooling by a few degrees should allow integration times well in excess of 1000 s .

The deviation from a linear increase in dark signal seen at short times in Fig. 4.15 is explained by the transient TFT response [4.30]. The data in Fig. 4.9 show that the TFT current decays quite slowly to its very low steady state value, and the excess leakage current in this transient causes a loss of signal charge. Thus, at short times there is a small decrease in dark signal charge with increasing time before the linear growth of the signal sets in. This transient charge may have an effect on the imager performance when two images are compared with different integration times.

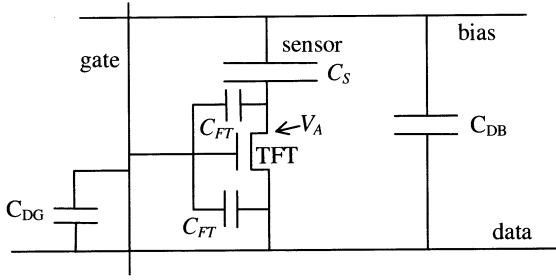


Fig. 4.16. Diagram showing the various sources of capacitance within the array

Capacitance Effects. A full understanding of the charge storage and transient readout properties of the array requires a more detailed analysis of capacitance within the array [4.31]. As described in more detail in Sect. 4.4.2, the electronic noise and much of the array performance is determined by various capacitance effects. Figure 4.16 shows an equivalent circuit that indicates the important parasitic and coupling capacitance. It has just been noted that the high address line capacitance sets limitations on the metal resistance, and in addition, a high data line capacitance is the dominant source of electronics noise in most systems. The gate and data line capacitance arises from several sources within the pixel;

- the cross-over of the gate and data lines which form parallel plate capacitors;
- the TFT channel capacitance and the parasitic gate to source and drain capacitance;
- the capacitance between the TFT source or drain and the light shield (if used);
- the fringing capacitance between the data line and the sensor.

For the type of array under discussion, these effects usually amount to about 20–50 fF per pixel, but the values can be selected by the specific design of the array.

These sources of capacitance have several effects on the readout. When the TFT gate is switched, there is a capacitive feed-through of charge, Q_{FT} , to the source and drain contacts, which may be a significant fraction of the maximum signal

$$Q_{FT} = C_{FT}\Delta V_G \approx 10 \text{ fF } 20\text{V} = 0.2 \text{ pC} , \quad (4.23)$$

where typical values are assumed for illustration. The charge on the source alters the bias on the sensor by ΔV_B , which must be taken into account in calculating the saturation charge of the pixel and other parameters, where,

$$\Delta V_B = Q_{FT}/C_S = C_{FT}\Delta V_G/C_S \approx 0.2 \text{ pC}/1 \text{ pF} = 0.2 \text{ V} . \quad (4.24)$$

The charge on the TFT drain is transferred to the readout electronics and provides a background charge that must be removed to obtain the correct image.

These effects are described in Fig. 4.17 which illustrates the voltages and charge during the readout of one pixel. The response is shown with and without exposure to illumination. The data line is attached to a charge sensitive amplifier, which holds the voltage constant. Consider first the voltage, V_A , on the TFT source (see Fig. 4.16). Near the end of the gate pulse all the charge has been transferred and the voltage V_A is equal to the data line voltage. As the gate is turned off, the parasitic capacitance causes V_A to decrease by ΔV_B . This voltage drop can be significant, and must be taken into account to obtain the actual sensor bias voltage. In the absence of illumination, V_A changes during the frame time by an amount dependent on the time-integrated sensor leakage current. When the gate is next turned on the feed-through charge raises V_A , and the current flow through the TFT resets V_A to the data line voltage. Exposure to illumination during the integration time causes V_A to decrease as extra charge is generated by the sensor. The read out again resets V_A and transfers sensor charge to the data line. If the exposure is sufficiently large, V_A reaches the sensor bias voltage and prevents further charge from being collected. The sensor is saturated and the readout charge is independent of further increase in illumination.

The charge transferred to the data line is shown in the lower curve in Fig. 4.17. The capacitive coupling between gate and data line causes an abrupt transfer of the feed-through charge when the TFT is switched. The real sensor charge is transferred to the data line more slowly, with the RC time constant $R_{ON}C_S$. When the gate is turned off there is another compensating transfer of feed-through charge. How the charge is detected by the external electronics is discussed in Sect. 4.4.1. Generally the data line charge is sampled twice – once before the TFT is switched on to give a background value, and once afterwards. After the sampling has taken place the data line is reset by the external electronics in readiness for the next measurement.

Image Lag and Charge Trapping in the Photodiode. So far it is assumed that all the sensor charge can be read out quickly and completely. Incomplete transfer that leaves signal charge at the pixel is doubly undesirable because it both reduces the detected signal, and releases the charge at a later time when it can create ghosts in subsequent images. This effect called *image lag* is fairly common in detectors, and is most noticeable under high frame rate conditions.

The simplest origin of image lag occurs when the TFT is not turned on for long enough to transfer the signal, but this situation is readily correctable by changing the timing. Image lag may also occur if the photodiode leakage current tends to drift (see Sect. 4.2.1 for a discussion of diode stability). However, in good quality photodiodes, the main source of image lag arises from

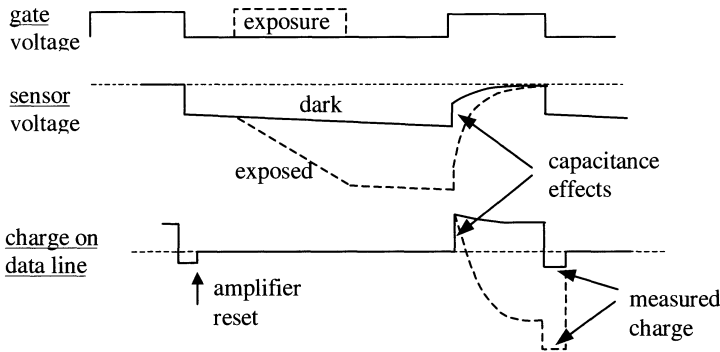


Fig. 4.17. Voltage on the sensor and charge on the data line during readout, with and without illumination, showing the effects of the parasitic capacitance, as described in the text. The illustration is for the case that the feed-through charge has the opposite sign from the signal charge

electronic traps in the undoped layer. Amorphous silicon contains deep defect states which may trap charge for much longer than the readout time. Charge trapping is governed by the mobility-lifetime product, $\mu\tau$, as described in Sect. 4.2.1. Equation (4.3) shows that the fraction of charge trapped is approximately,

$$P_T = 1 - P = t_F^2 / 2\mu\tau V \quad (4.25)$$

assuming a constant voltage and uniform field. Thus, trapping is minimized in thin samples with a high bias. In a good quality a-Si:H photodiode of $1\ \mu\text{m}$ thickness with 5 V bias, 1–3% of the electrons are trapped and 5–10% holes, because of their smaller $\mu\tau$ [4.10]. It is therefore best to design the sensor such that the electrons travel the larger distance, and this is accomplished by placing the p-type contact towards the illumination. Provided that the illumination is significantly above the band gap, then the absorption is close to the illuminated p-type contact. Under these conditions, holes do not have a significant distance to travel.

The situation in a sensor array is slightly more complicated because the bias decreases as the light flux on the sensor increases. The charge trapping therefore increases as the sensor approaches saturation. The collected signal charge when there is an illumination intensity, G_L , can be expressed as,

$$Q_S(V, t) = \int_0^t P_T(V) G_L dt. \quad (4.26)$$

Figure 4.18 shows a simulated plot of signal charge versus exposure for different degrees of initial trapping (i.e. the values of P_T at the start of illumination). The trapping causes a departure from linearity at increasingly low exposure, and the fraction of carriers which are trapped increases rapidly as saturation is approached due to the decrease in bias. Figure 4.18 also shows

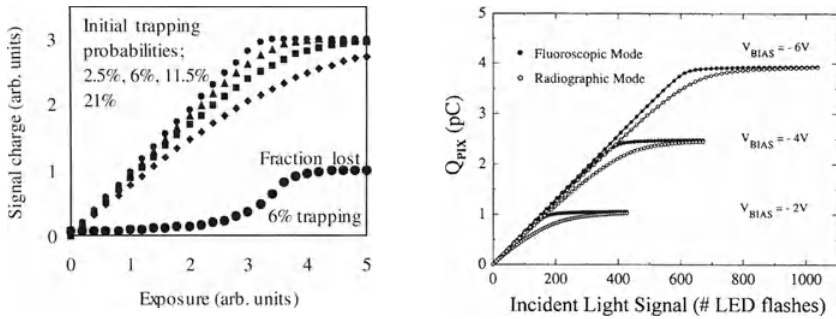


Fig. 4.18. Charge trapping effects in the photodiode simulated (*left*) and measured on an image sensor array [4.31]

that the actual data for an array agrees with the simulations. The charge trapping only reduces the charge collection in radiographic mode operation (see Sect. 4.4.1), so that the different results for the two modes clearly distinguishes the trapping effect. The results indicate that P_T is about 95% for the particular array measured [4.31].

The assumption of a uniform field is an approximation. The internal field of an unilluminated sensor has a depletion layer with a field profile that decreases away from the p-type contact and is determined by the defect density. The field profile becomes further distorted by the charge trapping. This situation has not been fully analyzed but it is clear that any region of the sensor in which the field is low greatly enhances the trapping effects.

4.3.3 High Fill Factor Array Designs

The imager sensitivity is proportional to the sensor fill factor which, as Fig. 4.13 shows, decreases rapidly as the resolution increases for the array design of Figs. 4.11, 12. The fill factor may be increased by using a 3-dimensional array architecture, in which the sensor is placed on top of the addressing matrix. Some designs of this type have been tried and are effective [4.32, 33]. Figure 4.19 illustrates the general approach by showing the cross-section view of one such design. The sensor is a continuous film covering the whole pixel. It is connected to the TFT through a contact pad and isolated from the address lines and the TFT by a passivation layer.

A continuous sensor layer can give unity fill factor, but the absence of an etched region separating pixels raises the possibility that charge created at one pixel can migrate to neighboring pixels. A continuous p-i-n sensor, in particular, allows such cross-talk due to the conductivity of the doped layer. Adjacent pixels with different signal charge have a potential difference between their contact pads and so current can flow taking charge from one pixel to the next. The extent of cross-talk depends on the conductivity of the doped layer and the frame time. In one study, the cross-talk was found

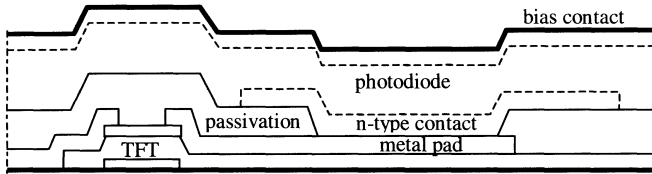


Fig. 4.19. Example of the design of a high fill factor sensor array using a continuous a-Si:H photodiode layer with a patterned n-type doped contact

to be minimal at frame times less than 0.1 s, but extensive if an integration time of 1 s or longer was used. A solution to this source of cross-talk is to eliminate the continuous doped layer by an extra lithography step, and this is the design shown in Fig. 4.19. The fill factor is slightly reduced, but the spatial resolution is restored [4.32].

Placing the sensor over the address lines also causes increased capacitance between these lines and the sensor. High capacitance is generally undesirable because it tends to increase the electronic noise (see Sect. 4.4.2), and the minimization of the capacitance is a matter of design optimization, which can include the use of a thick passivation layer. The capacitive coupling also can introduce unwanted parasitic charge into the system when gate voltage switching takes place.

An alternative high fill factor design to address these concerns is shown in Fig. 4.20 [4.33]. The two innovations are to invert the sensor so that the bias voltage plane lies between the address lines and the sensor to shield it from parasitic capacitive coupling, and to pattern the sensor with small gaps to eliminate crosstalk. This design is less susceptible to image degradation, while maintaining a high but not unity fill factor. The particular array that was fabricated had 192×192 pixels of size $200 \mu\text{m}$, with a $5 \mu\text{m}$ gap between the sensors. Together with the contact via to pass the signal from the top contact to the TFT below, the resulting fill factor is 93%. In order to minimize the data line capacitance, the sensors are separated by a $5 \mu\text{m}$ thick polymer layer with a low dielectric constant, and the resulting capacitance increased by only about 20% compared with the design of Fig. 4.12. However, some degradation of the photodiode was observed due to the polymer film. The capacitance between the sensor and the data line is virtually eliminated on this design and so removes any cross-talk between pixels that arises from this source.

4.3.4 TFT Addressed, X-Ray Photoconductor Arrays

Amorphous silicon p-i-n sensors are efficient detectors of visible light, but thin sensors have little sensitivity to X-rays because their absorption is weak. X-ray sensitivity is achieved by placing a phosphor in close contact with the a-Si:H sensor array [4.6, 34, 35]. The phosphor absorbs X-rays and emits light

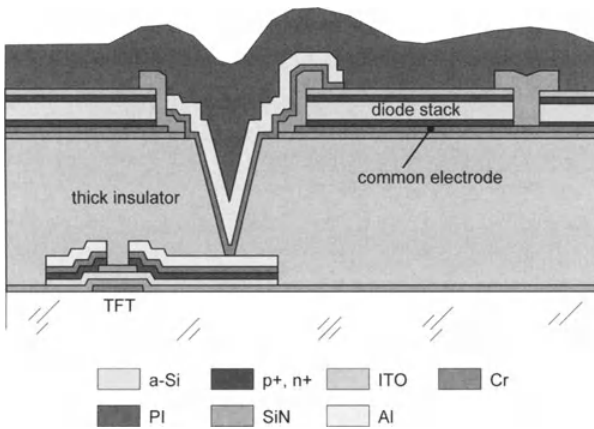


Fig. 4.20. High fill factor array with capacitance transient isolation and sensor isolation [4.33]

that is sensed by the array – the technique is described in Sect. 4.4.3. The use of a phosphor to convert X-rays to visible light is very effective and has been used for the past 100 years with X-ray film. However, an alternative approach to X-ray detection replaces the thin amorphous silicon sensor with a much thicker X-ray sensitive photo-conductor [4.36].

The requirements of the X-ray photoconductor place significant constraints on the choice of materials and the design of the array. The sensor material must absorb a high fraction of incident X-rays in order to make an effective imager. Since X-rays are weakly absorbed, the X-ray photoconductor materials must be thick – from 100 μm to 500 μm – in comparison to the 1 μm a-Si:H sensors. The thick films have several consequences for the array design. It is extremely difficult to pattern such devices into isolated sensors at each pixel because of the high aspect ratio needed for the etching and because of the difficulty of preventing etching of the underlying layers. The array designs use the same approach described above for high fill factor arrays and are fabricated as a continuous film with a contact pad at each pixel. Such thick films have very low pixel capacitance, since the capacitance is inversely proportional to the thickness, and therefore cannot hold much sensor charge. An additional capacitor is provided at each pixel to enhance the charge storage.

Figure 4.21 illustrates the structure of an X-ray photoconductor array. The pixel circuit contains the addressing TFT, the small sensor capacitance and the extra storage capacitor [4.37]. The latter requires a common electrode which must be provided along with the usual gate and data address lines. In the design shown, the storage capacitor is made from the same silicon nitride dielectric layer as for the TFT. The capacitance is comparable to that of the usual amorphous silicon sensor – of order 1 pF for a 100 μm pixel

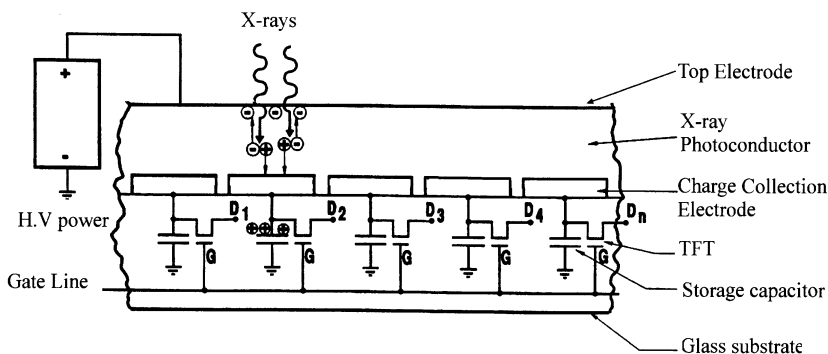


Fig. 4.21. A cross-section view of the structure of a photoconductor array with additional capacitance and matrix addressing [4.37]

– since the nitride layer is usually thinner, but also has a lower dielectric constant than a-Si:H. It can be noted in passing that the additional capacitance could be added to arrays with a-Si:H sensors to increase their charge storage capacitance.

Sensitivity. The increased thickness of the photoconductor requires a high quality material, but has the potential of high sensitivity X-ray detection. Sensitivity depends on the combined efficiency of charge generation and charge collection. Charge generation occurs when an incident X-ray interacts in the material to create a high energy electron which loses energy by ionization of electron-hole pairs. The ionization charge is collected by the applied field, and the collection efficiency is given by (4.3). As an example, a film of $300\text{ }\mu\text{m}$ thickness requires $\mu\tau V > 10^{-3}\text{ cm}^2$, which is achieved with a combination of a material with a very low defect density, and by applying a high bias voltage. Furthermore, the X-ray interactions occur throughout the material due to the low X-ray attenuation coefficient, so that efficient collection of both electrons and holes is essential.

Suitable photoconductors must have high atomic mass, large $\mu\tau$ values, and low leakage currents. To form large area arrays, the material must maintain its good properties in thin film form, which usually implies an amorphous or polycrystalline layer. There are a number of candidate materials – examples are selenium, lead iodide and oxide, thallium bromide, mercury iodide, and cadmium telluride. Amorphous selenium is used as an X-ray sensitive layer in other types of detector, and most of the other materials are known to perform well as X-ray detectors in their single crystal form. At the time of writing, Se, PbI_2 and PbO have been used in active matrix X-ray imagers and of these, Se is the most extensively studied [4.38–41].

The design of the array can mitigate some of the difficulties associated with high bias voltages and the continuous thick films. Selenium sensors may

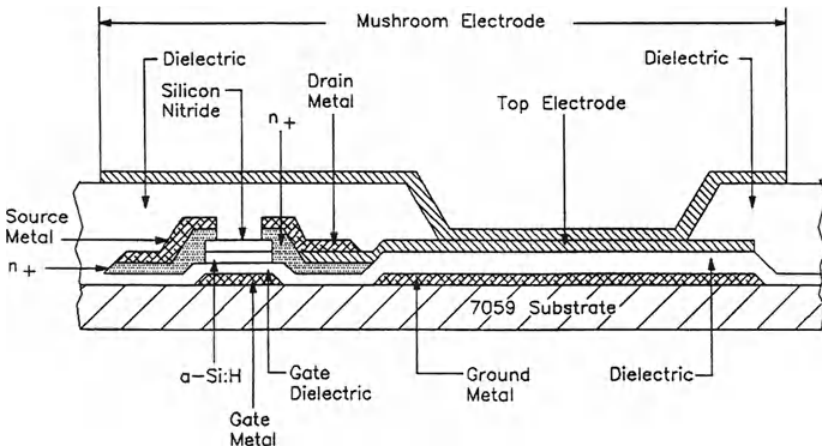


Fig. 4.22. The structure of a pixel for photoconductor detection, showing the “mushroom” electrode designed to maximize the charge collection [4.37]

require in excess of 3000 V, a voltage that would easily destroy the TFT or the charge storage capacitor if it is allowed to drop across the contacts. In principle, excessive exposure can charge up the capacitor and the source contact of the TFT to the bias voltage. One design prevents this by providing a leakage mechanism when the charge stored gets too large [4.39]. The TFT has a dual gate structure in which the second gate is connected to the source of the TFT. When the voltage rises sufficiently, the TFT is turned on and the charge leaks away before breakdown occurs.

A different problem is the build up of space charge in the sensor layer. Selenium has a low dark current and charge can be trapped between the pixels where there is no contact pad. Such charge may be released slowly and provide a source of image lag, or might be trapped near the TFT and cause an increase in its leakage current. A solution is to make the lower contact cover as large an area as possible, and in particular to cover the TFT to isolate it from the charge. The design illustrated in Fig. 4.22 is of this type. An isolation layer covers the TFT and address lines leaving the contact pads to the TFT exposed. Another metal film extends over the isolation layer and forms the bottom contact to the photoconductor. Even with the increased electrode area, there is sufficient trapped charge to cause visible ghosting effects due to image lag. This effect is removed by illuminating the imager between each image capture to reset the array to a uniform state.

4.3.5 Diode Addressed Arrays

Diode addressing of matrix addressed arrays has been applied to both liquid crystal displays and image sensors [4.42–44]. The approach is effective in

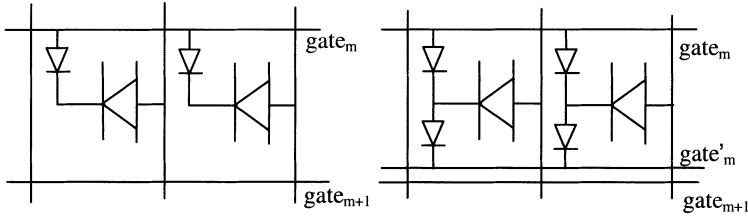


Fig. 4.23. Two alternative designs (single diode – *left*, and double diode – *right*) of diode-addressed image sensor arrays

both cases, but is not as widely used as TFT addressing. Diode addressing is an attractive choice for image sensors using a-Si:H p-i-n sensors, because the same sensor layer can in principle be used for both the sensor and the addressing device, thus simplifying the fabrication.

Figure 4.23 illustrates the pixel circuit used for addressing with a single or double diode arrangement. The single diode is placed back-to-back with the much larger photodiode, and the pair are connected between the address line and the data output line. Similar to the operation of the TFT addressed array, a voltage pulse on the address line serves both to read out and reset the pixel. The voltage pulse applies a forward bias to the addressing diode and transfers the bias voltage to the photosensor. The diode reverts to reverse bias when the pulse is removed, which holds the bias voltage across both diodes. Illumination of the photodiode causes charge collection and reduces the bias. When the voltage is reset by again applying the address pulse, charge of amount $C_S \Delta V$ is transferred from the data readout line to the sensor, where ΔV is the voltage drop on the sensor due to the illumination. This reset charge is exactly the signal developed by the sensor, and is recorded by the external electronics. The development of the signal charge and its read out is therefore generally similar for both TFT and diode addressing, and much of the discussion in Sect. 4.3.2 applies.

In both approaches, the capacitive feedthrough charge must be taken into account. The diode capacitance causes a change in the sensor bias when the address line is switched. The magnitude of the effect depends on the diode capacitance, but is similar to the gate capacitance of the TFT so the effects are of similar magnitude.

The most significant difference between diode and TFT addressing is in the readout time. The resistance of the diode varies exponentially with bias voltage, unlike the resistance of a TFT which is independent of source–drain voltage, at least for low voltages. In the diode exponential region (4.8),

$$R = (V/I_0) \exp(-eV/nkT) . \quad (4.27)$$

The diode resistance increases as the sensor voltage approaches V_B , and the reset time constant decreases correspondingly. Consequently, the sensor cannot be reset properly without waiting for a long time. This inability to reset

the sensor fully affects the dynamic range only slightly, but can cause significant image lag, because the degree to which the pixel is reset depends on the amount of charge detected in the previous image acquisition cycle.

Another property of the diode also tends to enhance image lag effects. When a diode is switched into forward bias, there is considerable charge trapping in defect states in the band gap. The charge is released slowly upon switching to reverse bias, and modifies the subsequent measurement of the signal. Similar trapping and release occurs in the TFT, but usually involves a smaller charge, because the TFT channel is 20–50 Å thick while the diode is more typically 1 μm thick, with correspondingly more trapping states.

Chabal et al. [4.43], and also Hoheisel et al. [4.44], discuss in detail the design and performance of a large area diode addressed array with 1024×1024 pixels. The arrays have a fill factor of 70% with 196 μm and 43% with 143 μm pixel sizes, using an addressing diode of $20 \times 20 \mu\text{m}^2$, but larger fill factors are expected with improved design rules. The two diodes are deposited separately so that they can be individually optimized – the photodiode for high quantum efficiency and low leakage, and the switching diode for high forward current. They overcome the limitations of the diode addressing by using a light flash to fully discharge the sensor charge and the reset of the sensor bias is separated from the readout addressing, using different bias voltages for each. The illumination ensures that all the photodiodes are reset identically by saturating their deep traps. This procedure eliminates the image lag effects but does complicate the read out. The result is an imager that operates up to 12.5 frames/s, and with excellent imaging performance.

Double Diode Addressing. The double diode approach solves some of the problems associated with single diode addressing [4.45]. The reset and readout is performed by two diodes connected to different address lines, as illustrated in Fig. 4.23. The operation is such that both diodes are switched from reverse bias to forward bias during the reset. This immediately solves the problem of a slow reset time, because the diodes maintain a high forward current and therefore have a low resistance with a correspondingly small RC time constant. The effects of the capacitance feedthrough charge are also eliminated in this arrangement because the charge transfer from one diode is offset by an equal and opposite charge from the other. The penalty for these performance improvements is that an extra address line must be included in the array to operate both diodes.

Graeve et al. have developed a double diode imaging system [4.46]. The array has 100 μm pixels in a 512×512 format with a photodiode fill factor of 45%. The readout electronics allows operation at up to 6.5 frames/s, and the imager shows good linearity and sensitivity properties with CsI and $\text{GdO}_2\text{S}_2\text{:Tb}$ phosphors. The image lag of 5–8% arises from the photodiode and is apparently not a result of the double diode addressing.

4.3.6 CMOS Sensors

It is worth giving a brief mention of the emerging field of CMOS sensor arrays, because of their use of a-Si:H photodiodes and their general similarity to the large area devices. CMOS sensor arrays are an alternative to charge coupled devices (CCD), whose widespread use ranges from video cameras to astronomical telescopes [4.47]. The attraction of the CMOS sensor is that it is fabricated with the standard technology of silicon integrated circuits, for which there is an enormous technology development effort. Unlike the CCD, the CMOS sensor usually has a matrix-addressed design based on the general architecture of Fig. 4.10. The pixel size is about $10\text{ }\mu\text{m}$, to keep the device small and of low cost. Low fill factor limits the sensitivity just as for the large area arrays because, unlike the CCD, significant space in the pixel of a CMOS sensor is needed for address lines and switching transistors. The continuing improvement in the CMOS feature sizes, now down to $0.25\text{--}0.35\text{ }\mu\text{m}$, makes the device possible by allowing more space in the pixel for the sensor.

However, the fill factor can be further increased by the technique described in Sect. 4.3.3 – coating the surface with a thin film sensor. Amorphous silicon p-i-n photodiodes are an obvious choice and have been applied successfully to CMOS sensors [4.48]. The diode provides sensitivity across the visible spectrum, high quantum efficiency, very low leakage current and ease of process integration. The design is essentially that shown in Fig. 4.19 for the high fill factor array – the continuous sensor film is connected to each pixel by a metal contact pad, with a common transparent electrode on top.

One of the attractions of the CMOS sensor array is its ability to integrate electronics on the array. Pixel circuits of considerable complexity can be fabricated for amplification, signal calibration, image processing, etc. In addition, further electronics at the periphery of the sensor array can provide control signals, analog-to-digital conversion and further signal processing. Clearly similar functions could also be integrated into the large area imagers provided that the device feature size is small enough and the TFTs are of sufficient quality. In the future both large and small area imagers may have similar levels of integration.

4.4 Imaging Systems and Their Performance

The complete imaging system comprises the sensor array together with the associated electronics to amplify, digitize, and display the image. The performance of the imager is in large part determined by the electronics, in particular the electronic noise and dynamic range of the amplifiers, which read the signals directly off the data lines. The electronics also determine the bit depth of digitization, and often limits the minimum frame time.

The performance of an image sensor array is a combination of resolution, sensitivity and noise. The analysis and measurement of the detector performance is fairly complicated, particularly for the case of X-ray imaging [4.49],

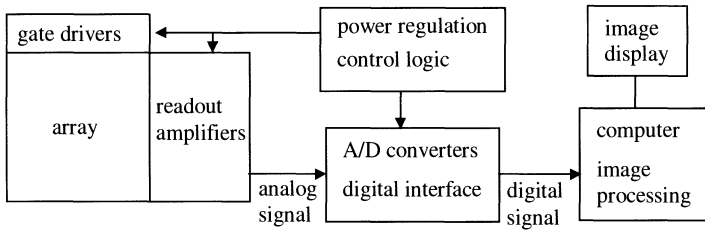


Fig. 4.24. Elements of the imaging system. The gate drivers and readout amplifiers are attached to the array. The other elements can be connected in many different ways

because of the additional effect of the X-ray conversion stage in which each X-ray generates many electronic charges that are detected.

The connection of the array to the external electronics is an important aspect of the technology. A high resolution image sensor requires several thousand such connections, and is a challenging task. The liquid crystal display technology has led the way with tape automated bonding (TAB), which allows a simple adhesive connection between the array and a driver or amplifier chip.

4.4.1 Electronics

The main elements of the imaging system are shown in Fig. 4.24 [4.50]. The gate lines of the array are connected to shift registers that provide sequential addressing pulses – the same devices that are used to address liquid crystal displays. These integrated circuits usually have 100–200 channels, so that several are required for a large area, high resolution imager. The readout amplifiers sense the charge on the data lines and the amplified analog signal is provided to analog-to-digital (A/D) converters [4.51]. The amplifiers are CMOS integrated circuits each with typically 128 channels, and several are used for each array. The signal is then digitized and passed to the host computer for processing and display. There is additionally the control logic that provides timing for all the operations and power regulation which provides filtered dc power to the system.

The task of the electronics is to take the image on the array that is acquired simultaneously at every pixel, and to organize the sequential transfer of digital data to the host computer. The task is accomplished by sequential stages of multiplexing. The first stage is to read out each line in sequence and is provided by the matrix addressing and the gate shift register. The next stage of multiplexing is performed by the readout amplifier which transforms parallel inputs into a single analog output, and further mutiplexing generally takes place either before or after the A/D converter. With each stage of multiplexing, the data rate progressively increases. The design of the elec-

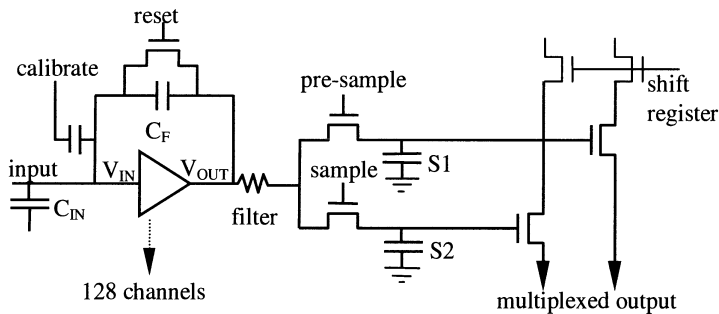


Fig. 4.25. Schematic diagram showing the elements of the charge sensitive amplifiers used to read out data from the array

tronic system matches the multiplexing stages to the speed performance of the various devices in the circuit, to obtain the desired overall readout speed.

Readout Amplifiers. The readout amplifiers are, after the array, the component that most determines the system performance [4.52, 53]. The array generates charge, and therefore a charge sensitive amplifier is the natural readout device, although voltage amplifiers have also been used [4.32]. The usual organization of the amplifier is illustrated in Fig. 4.25 and consists of several stages in sequence. After the high gain input amplifier with its feedback capacitor, there may be additional bandwidth filtering to minimize noise. The sample-and-hold stage, which stores the amplified charge, is followed by an output multiplexer. It is possible to include A/D conversion in the chip, but usually this is performed separately.

The feedback capacitor across the input amplifier determines the maximum input signal. The signal charge, Q_S , is stored on the feedback capacitance, C_F and the input capacitance, C_{IN} , which mostly arises from the data line capacitance of the array,

$$Q_S = C_F(V_{OUT} - V_{IN}) + C_{IN}V_{IN} . \quad (4.28)$$

The output voltage swing, V_{OUT} , is related to the input voltage swing, V_{IN} , by,

$$V_{OUT} = g_A V_{IN} , \quad (4.29)$$

where g_A is the amplifier gain. Hence,

$$Q_S = [C_F(g_A - 1) + C_{IN}] V_{IN} . \quad (4.30)$$

The gain must be large enough that the charge is practically all stored on the feedback capacitance rather than the input capacitance, for which the condition is,

$$C_F(g_A - 1) \gg C_{IN} . \quad (4.31)$$

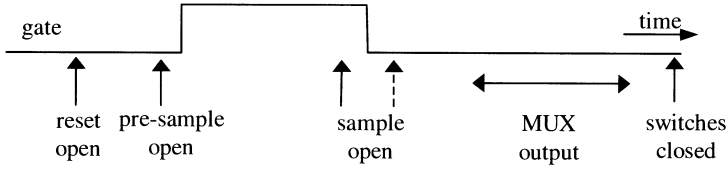


Fig. 4.26. Switching sequence to read out the array signal, using double correlated sampling

A high gain amplifier with $g_A > 1000$ is required, since C_{IN} is typically of order 100 pF, while C_F is about 1 pF.

The amplifier is designed with a single input, which is the gate of a very large FET to achieve low noise, as described in Sect. 4.4.2. The amplifier in Fig. 4.25 has various switches (reset, pre-sample, sample) to allow the measurement of the charge to be synchronized with the gate addressing pulses. In the technique of double correlated sampling, the data line charge is measured twice, a pre-sample reference occurring before the gate line is switched and the signal charge is measured afterwards. Noise is minimized because the measurements occur in the short time interval when signal charge is released from the pixel. The output charge is the difference signal,

$$Q_{OUT} = \text{sample} - \text{presample} = Q_2 + [q_2(t_2) - q_1(t_1)] , \quad (4.32)$$

where Q and q represent the signal charge and the noise, and t_1 and t_2 are the sample times. Low frequency noise which does not change between the two samples is therefore cancelled out. This double measurement of noise within a short time interval acts as a low frequency filter with a cut-off frequency of $1/(t_2 - t_1)$, which is 30–100 kHz for typical sample intervals of 10–30 μ s. In addition to removing low frequency noise, double correlated sampling corrects for any stray leakage charge that gets on to the data line.

Figure 4.26 shows how the switching sequence of the amplifier is synchronized to the gate pulses. When the feedback capacitor reset switch is closed, the amplifier input is clamped and is held at a voltage determined by the design of the amplifier. Opening the reset switch releases the amplifier and shortly afterwards the presample switch is opened to store a signal in S1 which is the data line charge before the gate pulse. The gate pulse is then applied and the signal charge transfers from the pixel to the data line. The sample S2 occurs when the charge transfer is complete, and may be before or after the gate pulse is switched off. The reset switch is closed after the samples are taken, and the complete sequence is repeated for each gate line.

After the sampling is completed by the opening of switch S2, the data are read out to the ADC though the output multiplexer. The amplifier design of Fig. 4.25 contains a shift register that sequentially transfers the two signals, and their difference is the input to the A/D converter. Apart from the low noise requirement, other important attributes of the amplifier are high dynamic range, good linearity and a high speed output shift register. Amplifier

chips can be designed to operate at 5–10 MHz on the output multiplexer, and with better than 1% linearity over a dynamic range of 10 000. Further performance improvements can be expected with the ever-continuing development of CMOS integrated circuits.

Timing, Digitization and Display. Most imagers are designed to acquire either single images well separated in time, or sequences of images recorded at video rates. The timing sequence of the data acquisition and the readout is similar in each case and is shown in Fig. 4.27 which illustrates the sequential transfer of data from each line of the array. The time taken for the complete readout is the product of the number of gate lines and the line time. The line time is that required to transfer multiplexed data from the readout amplifier chip, through the ADC and then to the host computer or to a data buffer. A chip with 128 channels takes 26 μs to transfer data at 5 MHz, which represents the minimum line time provided that the readout chip buffers the input from the output stage and the digital system can maintain the speed. Such line times are typical for video rate imaging, while single frame imaging can afford to slow down the transfer rate and have more multiplexing of the readout amplifiers.

Both single frame and video rate imaging requires that the imager is continuously cycled. If the array is not cycled, then the charge accumulates and eventually saturates the pixel sensor. We have seen that the a-Si:H TFTs and photodiodes exhibit some slow transients when the bias is changed, and therefore the first frame after the array is fully saturated may have different dark signal charge compared to subsequent frames. In normal operation,

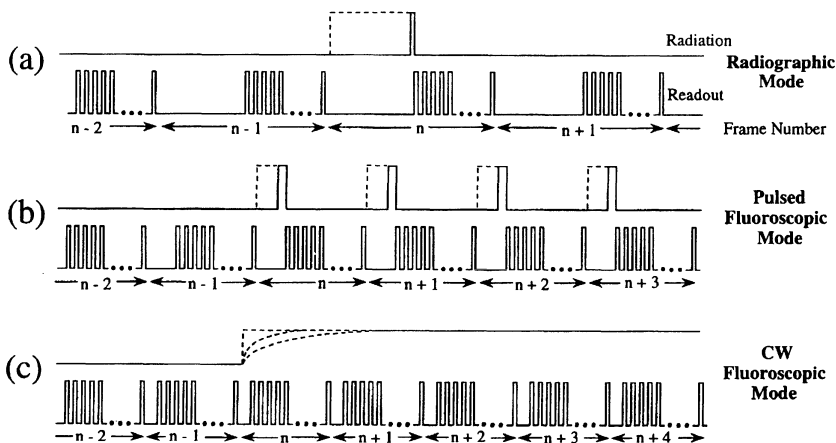


Fig. 4.27a–c. The timing sequences for radiography (a), and pulsed (b) or continuous (c) fluoroscopy imaging, showing how the X-ray radiation is synchronized to the integration time and readout over multiple image frames [4.54]

therefore, the array is cycled through the acquisition and readout cycles, and for single frame image acquisition, the exposure and the readout must be appropriately synchronized.

For the most part the images acquired in single frame or in continuous capture mode are equivalent, but they do have a different response to image lag effects, which can affect the linearity of the response. In single shot mode, some charge is retained by the pixel and does not contribute to the image. However, when readout is continuous, the charge that is retained by the pixel is ultimately readout in a later frame. Thus, although there may be some ghosting, the total signal charge making up the image sequence has no loss due to image lag. A comparison between the signal in the two modes of operation is therefore a convenient measure of the image lag and such data are shown in Fig. 4.18.

In many applications, the image is corrected for gain and offset, which removes variations in the fixed background pattern and the detector sensitivity as well as compensating for illumination non-uniformity. Such a correction is needed when better than 2–5% accuracy in the measurement of intensity is needed, because the offset variations across the imager are often about this value. The correction calculation is made on individual pixels according to the formula,

$$\text{image} = \frac{(\text{measured} - \text{dark})}{(\text{light} - \text{dark})} . \quad (4.33)$$

The correction requires that the dark and light images are separately measured before the image is acquired. There is a reduction in the digitization bit depth of the corrected image, as this reduces to the difference in the gray levels of dark and light images. Thus the image should be digitized beyond what is actually required for the final image. The correction may also increase the noise because three individual images are involved, but the extra noise can be prevented by using averaged values for correction images.

A further correction is usually made for bad pixels by using a median or average of the neighboring pixel values. The correction is very effective at removing the distracting effects of viewing the bad pixels, and usually a small number in the imager does not detract from its accurate rendering of the signal. The same correction can be made for bad lines, but generally such defects should not be present in an imager in which image fidelity is very important.

Even such simple image processing places a burden on the host computer when large video rate images are processed, and generally such system require specialized digital signal processors. However, current generations of PCs are adequate for single frame imagers for which the acquisition time is 1 s or more.

Interconnect Technology. A high resolution array with 2000×2000 pixels, requires 4000 contacts to the external electronics – 2000 to the gate drivers

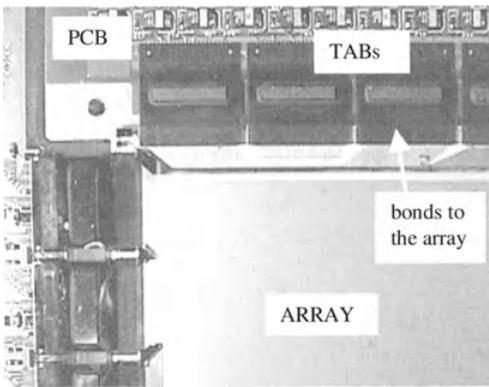


Fig. 4.28. Photograph of TAB-bonded image sensor array

and 2000 to the read-out amplifiers. The challenge of packaging the system increases as technology progress allows the development of higher resolution and larger size arrays. Present interconnect technology uses wirebonding or tape automated bonding (TAB), of which the latter is better suited to volume manufacturing [4.55]. The TAB package contains a silicon integrated circuit bump-bonded to metal traces on a flexible plastic carrier. The contact to the array is made by heat and pressure, using an anisotropic adhesive which contains small metal particles in an insulating matrix. The particles provide a conduction path between the pads bonded together but no lateral conduction between adjacent channels.

The liquid display industry has been the main driver of developments in the TAB technique and an example applied to an imager is shown in Fig. 4.28. The capabilities of the technology are determined by the outer lead bonds connected to the array and the inner lead bonds which are bump-bonded to the IC. The attachment of the TAB part to the circuit board is at lower resolution because there are fewer connections and is done either by soldering or by adhesive bond. The lower limit to the pitch of the outer lead bonds is $60\text{--}70\text{ }\mu\text{m}$, in part determined by the tendency of the plastic carrier to stretch when it is bonded to the array. For example, when using a TAB part with 128 contacts, stretching by as much as 0.5% will cause failure due to mis-alignment of the carrier to the array.

Wirebonding is a well established technique that is presently capable of finer pitch than TAB, but is slower, and more prone to damage. Figure 4.28 shows a photograph of a readout amplifier wirebonded to an image sensor array. The amplifier is on a circuit board placed next to the array, and the pitch of the contacts is $44\text{ }\mu\text{m}$, which is within the capabilities of wirebonding, although still challenging for an array with several thousand contacts.

It is obviously desirable to reduce the number of contacts from the array to the external electronics, and there are several approaches that can be

taken, again mostly pioneered by the liquid crystal display industry. Chip-on-glass technology allows the drive and readout chips to be attached directly on to the array. One approach is to use flip-chip bonding, in which the chip is inverted and attached to metal traces on the array using bump bonds. Alternatively, the readout and drive chips can be eliminated by designing their functions directly into the periphery of the array. It is generally expected that amorphous silicon TFTs do not have the required performance to make fast shift registers and amplifiers, but polysilicon has performance that can approach that of single crystal silicon as is described further in Chap. 3. Liquid crystal displays with integrated drive electronics have been demonstrated [4.56], and although there are no examples of similar image sensors, there is little reason to doubt that the gate drivers could be integrated. Polysilicon readout amplifiers are much more challenging, and most likely would not have the same low noise performance, but this approach may be effective, particularly if pixel-level amplification reduces the noise requirements of the amplifier [4.57].

4.4.2 Electronic Noise

Minimizing noise in the electronic system is essential because the signal-to-noise and dynamic range requirements for many imaging applications are very demanding. However, electronic noise is only one component of the image noise, as discussed further in Sect. 4.4.4. Several sources of electronic noise arise from the array and from the associated electronics. Some of the noise sources are fundamental limits that cannot be reduced, and some are extrinsic sources that are merely difficult to eliminate. The most important are thermal noise in the pixel TFT and data line, the amplifier input noise, and voltage fluctuations in bias supplies. The RMS values, q_i , of random noise sources add in quadrature,

$$q^2 = \sum_i q_i^2. \quad (4.34)$$

The noise is often dominated by a single component, although this may be a different source in different imaging systems. The following discussion is based on TFT-addressed, a-Si:H sensor arrays, for which there has been the most analysis and measurement. However, the discussion applies to other array types with little modification.

Resistances generate thermal noise, current sources generate shot noise, and generally any device has additional $1/f$ noise [4.58]. The $1/f$ noise is sensitive to the device fabrication, and Fig. 4.29 illustrates the noise spectrum for one a-Si:H TFT [4.59]. There is a low frequency $1/f$ noise that increases with the drain current and a white noise component evident at high frequency. The transition from $1/f$ to white noise occurs at 10^5 – 10^6 Hz depending on the current. The TFT off-resistance is so high that its noise only occurs at very low frequency and is eliminated by the double correlated sampling. Thick,

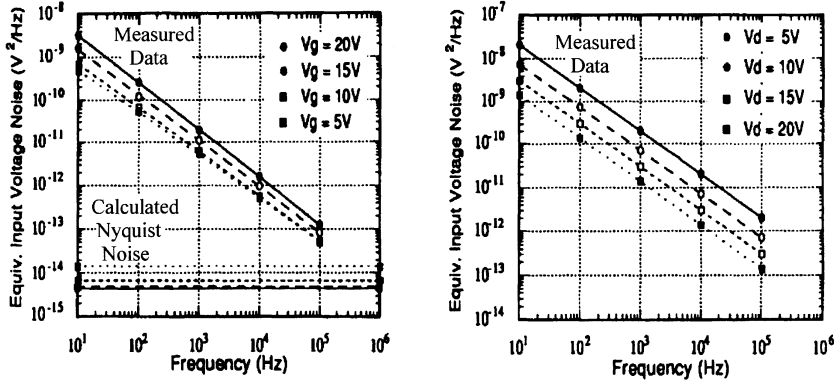


Fig. 4.29. Noise spectrum of an a-Si:H TFT, showing the $1/f$ component and its dependence on gate voltage (*left*) and source-drain voltage (*right*) [4.59]

reverse bias p-i-n photodiodes exhibits $1/f$ noise to about 10^4 Hz at high bias, but the current noise is negligible in thin, low bias sensors, because of the very low leakage currents [4.60, 61]. Photocurrent noise is discussed later and in X-ray imagers reflects the shot noise of the X-ray flux. The sensor may have extrinsic noise due to current instabilities, but these are not considered in the present discussion.

Thermal Noise from the Array. Double correlated sampling acts as a low frequency filter and greatly reduces $1/f$ noise from all the components. To a good approximation, the dominant pixel noise arises from the thermal noise of the single TFT that is switched on [4.62]. The noise voltage fluctuations, with spectral density $\nu(f)$, cause charge fluctuations on the sensor capacitance, C_S . The charge noise is given by,

$$q_{\text{pix}}^2 = \int_0^\infty [C_S \nu(f) g(f)]^2 df, \quad (4.35)$$

where $g(f)$ is the filter function of the circuit at frequency f . Equation (4.35) represents the sum of noise components over the frequency response of the circuit.

Figure 4.30 shows an approximation to the array circuit, in which the sensor capacitance C_S is in series with the TFT resistance R_{ON} and its noise source, and the components of the much larger data line capacitance are denoted C_D and in parallel with the pixel. The data line capacitance reference voltage is both the gate and bias voltages, but can be considered a single parallel capacitance. The data line resistance, R_D , is shown as a single resistor with its corresponding thermal noise source, although in reality, both C_D and R_D are distributed.

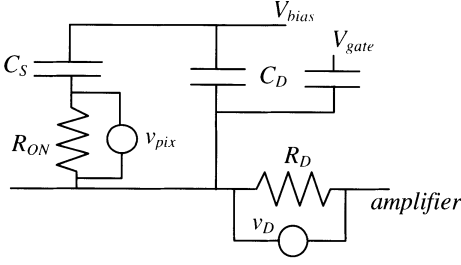


Fig. 4.30. Pixel circuit used for noise analysis, as discussed in the text

The pixel R-C circuit, with the approximation that $C_D \gg C_S$, provides a high frequency cut-off to the noise spectrum with $g(f)$ having the form, $1/[1 + (2\pi fRC_S)^2]$. Resistance noise has a white spectrum with magnitude,

$$\nu^2(f) = 4kTR. \quad (4.36)$$

Neglecting the low frequency filtering provided by the sampled readout, (4.35) yields the well known result,

$$q_{\text{pix}}^2 = kTC_S. \quad (4.37)$$

Although the noise arises solely from the resistance, its value is proportional to the capacitance and independent of the resistance, because the increase in noise from a larger resistance is cancelled out by the reduction in bandwidth. At room temperature the kTC noise from a resistance and a 1pF capacitor is 400 electrons.

There is a low frequency cut-off in $g(f)$ because the TFT is turned on only for a limited integration time of typically 10–50 μs . Usually the integration time is several times larger than the pixel RC time constant, so that the low frequency cutoff removes $1/f$ noise but only reduces the white noise component by a small factor. However, the noise is reduced significantly when a short integration time is used.

From the point of view of the array operation, one must take into account the switching of the gate lines and sampling of the pixel signal to obtain the expected noise. There has been some debate over the correct analysis, but the consensus supports the following argument. When the gate is turned on the resistance noise generates charge fluctuations as described above. While the gate is off, the charge is held on the pixel without further fluctuation until the next time the pixel is addressed (assuming an ideal TFT). Thus each time the pixel is addressed, it starts with a noise charge q_{n1} , from the previous measurement, and finishes with a charge q_{n2} , so that the measured noise charge is,

$$q_{\text{pix}}^2 = q_{n2}^2 + q_{n1}^2 = 2q_n^2 = 2kTC_S. \quad (4.38)$$

This result holds when the two noise measurements are uncorrelated which corresponds to the usual case when the integration time is much longer than $1/R_{\text{ON}}C_{\text{S}}$.

In effect, the noise is sampled twice each time the pixel charge is read out, and is therefore increased by a factor of $\sqrt{2}$. Measurements on a single pixel with a 0.7 pF sensor find a value of 620 electrons, compared with the theoretical value of 520 electrons [4.63]. The excess might be due to a small $1/f$ component. The pixel kTC noise values sets the lower limit on the possible performance of the array with a particular sensor capacitance, at least for the usual method of sensing.

The resistance of the data line is another significant source of thermal noise originating on the array. The voltage noise causes charge fluctuations on the data line capacitance. The noise is given by (4.35), but the filter function is usually determined by the high frequency cut-off of the amplifier f_{A} , rather than the R - C filtering of the data line which typically has a higher frequency cut-off. The noise is therefore approximately,

$$q_{\text{D}}^2 = 4\pi kTR_{\text{D}}C_{\text{D}}^2f_{\text{A}}. \quad (4.39)$$

For typical array parameters the data line resistance should be no more than a few hundred ohms for this noise to be less than the pixel kTC value. A low amplifier cut-off frequency helps minimize the effect and the double correlated sampling provides a low frequency filter which further reduces noise and eliminates any $1/f$ component.

Thermal noise from the gate line resistance is capacitatively coupled to the data line through the parasitic capacitance of the TFT and the other pixel elements. However, this contribution to the overall noise is sufficiently small to be neglected.

Amplifier Noise. The amplifier input for the integrated CMOS amplifier chips is the gate of a large MOS field effect transistor [4.64]. The primary sources of noise are the thermal and $1/f$ noise of the FET channel. To account properly for the effects of gain, it is conventional to calculate the equivalent noise on the input gate for which the thermal noise power in saturation is [4.64],

$$\nu_{\text{amp}}^2 = i_{\text{DN}}^2/g_{\text{m}}^2 = 4\beta kTg/g_{\text{m}}^2 = 4\beta kT/g_{\text{m}}, \quad (4.40)$$

where I_{DN} is the FET drain current thermal noise, g_{m} is the transconductance, g is the channel conductance, and β is a constant whose value depends on the details of the FET but is about 2/3. The factor $1/g_{\text{m}}^2$ refers the current noise in the channel to the gate, and the expression on the right arises because $g = g_{\text{m}}$ for an FET in saturation. $1/f$ noise is mostly eliminated by double sampling, but NMOS FETs have particularly high $1/f$ noise so that PMOS devices are invariably used, in which case the $1/f$ noise can be ignored for the normal array readout speeds.

The input charge noise is $C_{\text{in}}\nu_{\text{amp}}$, and a general expression that is a good approximation for most amplifiers is

$$q_{\text{amp}} = q_0 + \gamma C_{\text{D}} , \quad \gamma = (4\beta kT \Delta f / g_{\text{m}})^{1/2} ; \quad (4.41)$$

γ is the noise slope and q_0 is the residual noise from the FET gate capacitance and typically has a value of a few hundred electrons.

A low noise amplifier needs a small value of γ , and is therefore designed with as high a transconductance as possible, which occurs in saturation where,

$$g_{\text{m}} = \sqrt{\mu_{\text{FE}} C_{\text{G}} I_{\text{SD}} W / L} . \quad (4.42)$$

The input FET is therefore designed with large W/L – values of several thousand are common – operating at high drain current, and therefore consuming high power.

For low noise operation, the amplifier band width, Δf , should also be as low as possible. There is much theoretical work on the design of optimal filters for single charge detectors, but for the multiple channel integrated circuits the filtering tends to be a simple R – C circuit. The band width is chosen carefully to be the smallest consistent with the desired readout speed of the array [4.65]. Such an amplifier can have an input referred noise of $< 2nV/\sqrt{\text{Hz}}$, and for a bandwidth of 300 kHz, the resulting noise slope is about $\gamma = 10 e/\text{pF}$ [4.53]. The overall amplifier noise is then in the range 500–1500 for large area arrays.

Extrinsic Noise. The most problematic extrinsic source of electronic noise is the voltage fluctuations in the bias supplies. The TFT addressed, photo-diode arrays are provided with the sensor bias voltage, the TFT off-voltage and the TFT on-voltage. Each of these bias supplies is capacitatively coupled to all of the data lines of the array. Hence, a voltage noise, ν_{EXT} , on any of the bias voltages induces a charge noise at the input of the readout amplifier of approximately [4.35, 62],

$$q_{\text{EXT}} = C_{\text{D}} \nu_{\text{EXT}} . \quad (4.43)$$

The various capacitances that make up the data line capacitance are discussed in Sect. 4.3.2. Since all but one gate line is turned off, the capacitance to the TFT on-voltage is negligible compared to the capacitance to the bias and TFT off-voltage power supplies and these two capacitances are roughly comparable in magnitude. A capacitance of 50 pF with a voltage fluctuation of 3 μV , yields a noise of 950 electrons. Given that the pixel and amplifier noise can be held to this value or less, it is clear that very low noise power supplies are needed. The problem, however, is greatly helped by double correlated sampling which filters out low frequency noise. The system is sensitive to noise only in a band of roughly 30–1000 kHz.

The noise fluctuations on the TFT and bias lines are identical across the array, so that the same noise is detected on each data line, since they are all sampled at the same instant. (Here it is assumed that filtering by the array is negligible – usually a fair approximation.) The noise is therefore the same on each pixel of one line, but different from line to line. Such line-correlated noise is visibly different from the random noise and can be readily distinguished in images. Indeed human vision is particularly well adapted for detecting lines, and therefore when an image contains equal amounts of line-correlated and random noise, the line noise is much more obvious. It is therefore important to minimize this visually distracting noise source.

Extrinsic noise increases with the data line capacitance and so increases with the number of pixels. The trend to increasingly large arrays makes control of the extrinsic noise more challenging. However, systems with line noise of ≈ 1000 electrons have been reported from an array with 3000 pixels along the data line, and lower values in smaller arrays [4.35, 66–68]. Figure 4.31 shows an image of the noise from a portion of such an array for which the overall noise is about 1800 electrons. The line noise becomes more noticeable as the image is viewed from further away. The fact that the noise is correlated across a line also provides a mechanism for correcting the noise even when it is present. The technique is to sample the noise in extra pixels at the edge of the array and to subtract this value from the image. This can be implemented either directly by the readout amplifier or some other part of the electronic system, or more simply by image processing software in the host computer. As we have seen before in other contexts, the subtraction of a noise signal comes with the penalty of increasing the noise by a factor $\sqrt{2}$ because of the extra sample of random noise. In this case however, it is possible to design an array with perhaps 10–20 dummy pixels to sample the line noise, in which case the subtraction can be done without significant increase in the random noise. It should be noted that the noise cancellation is only successful if the noise is the same across the array. Any additional R - C filtering of the noise voltages by the array will cause the correction to fail.

The above discussion by no means exhausts the sources of extrinsic noise. Since the array has no ground connection, the voltages of the bias and gate lines are referenced to the amplifier input and therefore ultimately to the amplifier power supplies, which must have similar low noise properties. The whole system mixes digital controls with the low noise analog inputs and it is obviously important that digital noise does not get coupled into the input of the amplifier. Finally, one should note that the whole array, measuring perhaps 40 cm across and with up to 2 km of metal lines, may act as a large antenna and pick up radiated electromagnetic signals. Shielding to eliminate these noise sources is necessary. The total noise from the above discussion is,

$$q_N^2 = q_{\text{pix}}^2 + q_D^2 + q_{\text{amp}}^2 + q_{\text{EXT}}^2 \quad (4.44)$$

As with other high performance electronic systems, it takes a good deal of experimentation and experience to achieve the intrinsic noise performance limit.



Fig. 4.31. Example of a noise image [4.71]

In practice the reported noise performance has been improving steadily even as the array sizes and pixel number increase. Several systems have been reported with noise in the range 1000–2000 electrons [4.66–68], and there seems every reason to expect that systems will soon converge on the theoretical values of less than 1000 electrons.

In an imaging system for which the pixel noise is a small fraction of the total noise, it is obviously beneficial to have a pixel amplifier [4.57]. A gain of about 10 is sufficient to increase both the signal and noise until they are no longer limited by amplifier and bias supply noise. Pixel amplifiers have been implemented in CMOS sensors (see Sect. 4.3.6) and may be anticipated in large area array in the future.

4.4.3 X-Ray Detection

Thin amorphous silicon p-i-n photodiodes have virtually no X-ray sensitivity because there is minimal absorption of the incident beam. X-ray imaging with systems based on these devices is accomplished by placing a phosphor on the surface of the array. On the other hand, arrays designed with a thick photoconductor (see Sect. 4.3.4) are X-ray sensitive by intentional design. Either approach is effective and X-ray medical imaging systems based on both designs are being manufactured [4.68].

These two methods of X-ray imaging are compared in Fig. 4.32. The physical process for X-ray detection begins the same way in either case when a single interaction transfers some or all of the X-ray photon energy to excite a high energy electron [4.69, 70]. The mechanism is photoionization at lower energy (i.e., < 50 keV) and Compton scattering at higher energy. The energetic electron loses energy by creating many electron-hole pairs by successive

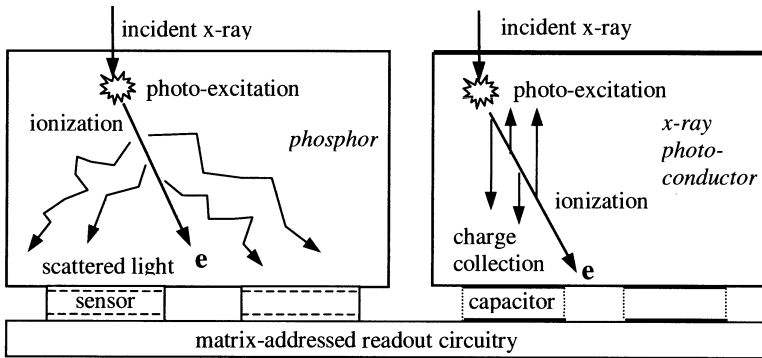


Fig. 4.32. Illustration of the phosphor/photodiode (*left*) and photoconductor (*right*) methods of X-ray detection

ionization until all its energy is dissipated. The number of pairs created, N_P , by each absorbed X-ray photon is given by,

$$N_P = E_X / W . \quad (4.45)$$

W is the average energy needed to create an electron-hole pair and is usually 2-3 times the band gap energy, and E_X is the incident X-ray energy. The ionization charge forms the latent image that is sensed by the imager.

X-ray attenuation coefficients are shown in Fig. 4.33 for some phosphor and photoconductor materials in the region of most interest for medical applications from about 10 to 100 keV. X-ray attenuation decreases with X-ray energy except for the abrupt steps at the K or L absorption edges, and also increases with atomic number. In the middle of the energy range, attenuation coefficients are roughly 10 to 100 cm^{-1} so that the thickness of the X-ray absorber is in the range 30 – $1000 \text{ }\mu\text{m}$.

When a phosphor is used for detection (Fig. 4.32, left), the electron-hole pairs recombine to emit visible light which is sensed by the photodiodes on the array. The phosphor is placed in close contact with the array to allow the maximum transfer of the light. Indeed, contact imaging is vital for high sensitivity, and is one of the principal reasons why large area a-Si:H arrays are excellent X-ray imagers. In the alternative situation in which the phosphor emission is imaged onto a small detector using a lens, then the optical transfer efficiency is given by,

$$\text{lens efficiency} = \frac{1}{1 + 8f^2(1 + 1/m)^{-1}} , \quad (4.46)$$

where m is the demagnification, f is the f -number of the lens and the constant depends on the nature of the emitting surface. For a large phosphor screen, the typical transfer efficiency is 10^{-4} – 10^{-3} , compared to $> 50\%$ for contact imaging.

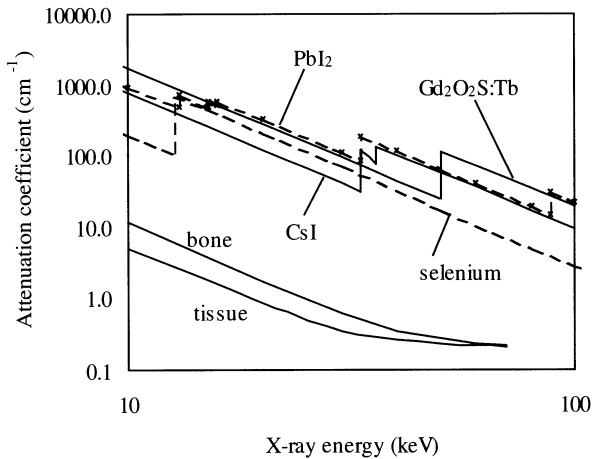


Fig. 4.33. X-ray attenuation coefficients for the detector materials described in the text, compared with the attenuation of bone and tissue

The ideal phosphor has strong X-ray attenuation, high light emission efficiency, and an emission wavelength matched to the collection efficiency of the amorphous silicon sensor. Of the numerous candidate phosphor materials, the best choices are $\text{Gd}_2\text{O}_2\text{S}_2\text{:Tb}$ and CsI:Tl . The emission from both of these phosphors is efficient, and is in the wavelength range 500–600 nm, which coincides with the peak of the a-Si:H quantum efficiency spectrum (see Fig. 4.2).

Since the recombination light is emitted isotropically in the phosphors, it is important that the photodiode detects the emission near where it is created, to maintain good spatial resolution in the image. The $\text{Gd}_2\text{O}_2\text{S}_2\text{:Tb}$ phosphor screen is fabricated as a powder in a binder and scatters light, such that the spreading of the image is approximately equal to the thickness of the film. The detection of high energy X-rays therefore involves a compromise between the need for a thick film to absorb X-rays efficiently, and the decrease of spatial resolution in the thick film.

CsI:Tl is deposited by thermal evaporation on the surface of the array [4.35]. It was discovered long ago that under suitable deposition conditions, the deposited film has a columnar structure that causes a light piping effect and reduces the loss of spatial resolution in thick films. Thus CsI:Tl provides both higher sensitivity and better spatial resolution than $\text{Gd}_2\text{O}_2\text{S}_2\text{:Tb}$, at the expense of some additional difficulty in manufacturing.

When a photoconductor is used to detect X-rays (see Fig. 4.32, right), the ionization charge is collected by the applied field. There is little lateral diffusion of the charge so that the spatial resolution of the image is maintained, regardless of the layer thickness [4.36, 37]. In principle, the photoconductor gives a higher sensitivity than the phosphors, partly because it can be made

thick enough to absorb all the X-rays and partly because the light emission and subsequent detection steps are absent. However, it represents a significant materials challenge, since high charge collection in a thick film requires a high value of the $\mu\tau$ product – 1 or 2 orders of magnitude larger than for thin a-Si:H sensors. Furthermore, high charge collection efficiency is required for both electrons and holes because X-rays are absorbed throughout the photoconductor. The charge trapping length, L , is given by

$$L = \mu\tau V_B / t_F, \quad (4.47)$$

where t_F is the thickness, V_B is the bias and a uniform electric field is assumed. Ideally L should be at least twice the thickness of the film, so that the minimum bias voltage is

$$V_{\text{MIN}} > 2t_F^2 / \mu\tau. \quad (4.48)$$

The required bias is even larger if the field is non-uniform due to a depletion layer. The photoconductor thickness must be roughly $1/\alpha$ to absorb X-rays, where α is the attenuation coefficient which varies with X-ray energy approximately as $E_X^{-2.5}$ (see Fig. 4.33). Hence,

$$V_{\text{MIN}} \approx E_X^5 / \mu\tau, \quad (4.49)$$

so that the minimum bias voltage increases rapidly with energy [4.71].

Amorphous selenium photoconductors have been extensively investigated, and polycrystalline PbI_2 appears to be a promising new material. The selenium is doped with As and Cl to give good charge collection for both electrons and holes, and is readily evaporated onto large arrays at low temperature. However, as shown in Fig. 4.34, the ionization rate, W , for selenium is unusually small and field dependent, of the form [4.37, 39]

$$\begin{aligned} W &= \text{const } F^\alpha; \quad \alpha = -(0.65 - 0.9); \\ W &\approx 50 \text{ eV/pair at } 10 \text{ V}/\mu\text{m}. \end{aligned} \quad (4.50)$$

Possibly this effect is due to geminate recombination, and is related to the similarly low quantum efficiency for visible light. The films require a field of about $10 \text{ V}/\mu\text{m}$, or about 3000 V across a $300 \mu\text{m}$ layer.

PbI_2 has a high sensitivity to X-rays, but at the time of writing, the leakage current is moderately large [4.71–73]. Further development is needed to determine whether the photoconductors can approach the ideal sensitivity. When both the charge ionization rate and the charge collection are nearly ideal, then a single 50 keV X-ray should generate 5–10 000 electrons of charge, an order of magnitude more than is typically obtained with phosphors. PbO has also been shown to be an effective material [4.74].

4.4.4 The Performance of X-Ray Detectors

Detector Performance Analysis. The goal for the design of any imaging system is to optimize the performance of the detector in terms of its ability to

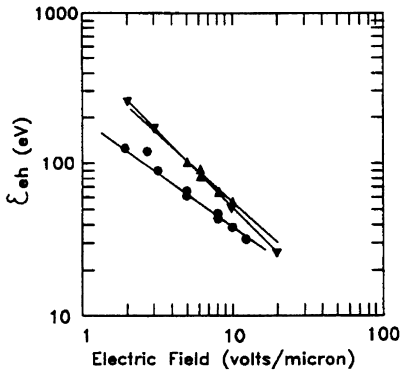


Fig. 4.34. Electric field dependence of the Se ionization rate [4.39]

faithfully reproduce the information content of the incident image. It is therefore necessary to have the appropriate analytical metrics for performance and the techniques to measure them. All aspects of the X-ray imaging system contribute in one way or another to the performance, affecting the signal, noise and spatial resolution. These can be categorized as follows [4.75–77];

- 1) **Signal gain.** At various stages in the detection there is a change in the number of photons or electrons that comprise the signal. For example, not all incident X-ray photons are absorbed by the detector, corresponding to an absorption gain of less than unity. On the other hand, each absorbed X-ray photon generates a large number of electron–hole pairs by ionization (i.e., a gain of 100–10 000). The detection of these charges at the pixel has some inefficiency which results in a further gain of less than unity.
- 2) **Image spreading.** The detection of signal generated by the phosphor or X-ray photoconductor may result in some signal spreading to neighboring pixels, and results in loss of spatial resolution of the image.
- 3) **Pixel sampling.** Even in the absence of image spreading, the size of the sensor and of the pixel places an upper limit on the ability of the detector to resolve fine features in the image.
- 4) **Additive noise.** Along with any reduction in signal-to-noise performance generated by the gain, blurring and sampling stages, there is additional noise that arises from the electronic readout, as discussed in Sect. 4.4.2.

The performance of the detector must be defined in terms of the incident signal which has its own signal-to-noise limitations. The fundamental limitation is the shot noise that arises from the counting statistics of the incident photons. N incident photons are governed by Poisson statistics and have an RMS fluctuation of $\sqrt{N}$ (and variance N). The performance of a detector is the measure of how well the incident signal-to-noise (S/N) ratio is preserved by detector. This leads to the concept of the detective quantum efficiency,

DQE, defined in its simplest form as the square of the ratio of the measured and input S/N,

$$\text{DQE} = \frac{(\text{S/N})_{\text{OUT}}^2}{(\text{S/N})_{\text{IN}}^2} . \quad (4.51)$$

The S/N ratio of a detector also depends on the spatial frequency of the measurement, because the signal from an incident X-ray is typically spread over many pixels, for example due to light scattering in the phosphor. The noise and spatial properties of the array are combined together in a DQE measure that is a function of spatial frequency and is the most complete expression of the imager performance. The full discussion of the DQE is beyond the scope of this book, but it is useful to summarize the main points to understand how the image performance depends on the system design and how the performance is measured.

Although the image comprises a signal with intensity $s(x)$ that varies with position, x , the analysis of the signal and noise is more conveniently accomplished in the spatial frequency domain, because of the properties of Fourier transforms, as will be illustrated for the case of image spreading by the phosphor. An incident delta function signal at position x_0 results in an output signal, $t(x - x_0)$, spread over a range of values of x , as illustrated in Fig. 4.35. (For simplicity a 1-dimensional analysis is used; the extensions to 2-dimensions are given in [4.75–77].) In a linear system, the output image, $o(x)$, corresponding to the input $s(x)$ is the convolution of $s(x)$ with $t(x)$ [4.75]

$$o(x) = \int s(x')t(x' - x)dx' . \quad (4.52)$$

The Fourier transform of a convolution is a product of the Fourier transforms of the separate functions, such that in frequency space

$$O(u) = S(u)T(u) , \quad (4.53)$$

where the functions of spatial frequency, $u = 1/x$, are Fourier transforms of the corresponding real space functions. The simplification of dealing with the product of functions rather than the convolution integrals is helpful both conceptually and for analysis. $T(u)$, the Fourier transform of the point-spread, or in one dimension, the line-spread function, $t(x)$, is known as the *modulation transfer function*, the MTF. It has the value unity at spatial frequency $u = 0$, and decreases to zero at higher frequencies.

All pixel arrays sample the image at discrete sensors of finite size. The signal detected by a sensor is the convolution of the image resulting from the X-ray detection stage, $o(x)$, and a rectangle function, $r(x)$, corresponding to the size, a , of the sensor, for which the Fourier transform is a sinc function. The signal at a pixel is then given by,

$$P(u) = \text{const.} S(u)T(u)R(u) = \text{const.} S(u)T(u)|\text{sinc}(\pi au)| , \quad (4.54)$$

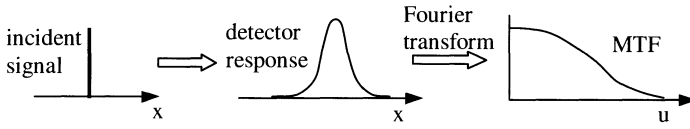
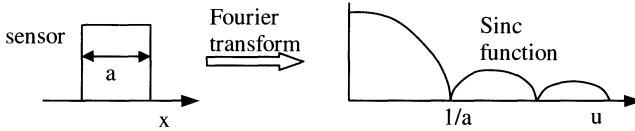
Image spreading**Pixel sampling**

Fig. 4.35. Illustration of the analysis of image spreading and pixel sampling that determine the detector response to the incident image

where the constant includes the signal gain. The product $T(u)\text{sinc}(\pi au)$ is known as the pre-sampled MTF and its measurement is discussed in the next section. The presampled MTF represents the spatial frequency response of a single sensor.

The next stage of the image chain is the sampling of the sensor signal $P(u)$ by the series of pixels that make up the array. The signal at each pixel is represented by a single quantity (the measured charge) assumed to be at the center of the pixel. The sampling is therefore represented by an periodic array of delta functions separated in real space by the pixel pitch, d , and its Fourier transform is the same function separated in spatial frequency by $1/d$.

The Nyquist frequency, $u_N = 1/2d$, represents the upper limit of the spatial frequencies that can be detected, since essentially two samples per cycle are needed to detect a modulation. If the presampled MTF extends beyond the Nyquist frequency, then an imaging artifact known as aliasing (or the Moiré effect) may result. A component of the incident image with high spatial frequency, u , beats with u_N and the difference frequency, $u - u_N$, is observed in the measured image. It is virtually impossible to distinguish aliasing from a real signal at the lower frequency.

An ideal imager has a high MTF below the Nyquist frequency to maintain the spatial resolution of the image, but a low MTF above u_N , to eliminate aliasing artifacts. A sharp cut-off in the MTF at u_N is generally not possible, so some trade-off is needed, usually with the MTF extending some way beyond u_N . If the incident image contains no spatial frequencies above u_N , then obviously no aliasing of the image can occur, although aliasing of the noise can affect the detection. The ideal imager therefore matches the pixel pitch to the MTF and to the spatial frequency content of the source.

The image noise is similarly influenced by the various gain, spreading, and sampling stages of the detector as well as the additive readout noise from the electronics. For example, the probability, g_{abs} , of absorbing an incident X-ray,

is accompanied by a statistical fluctuation in the absorption with variance $g_{\text{abs}}(1 - g_{\text{abs}})$ corresponding to a binary process. The spatial auto-correlation function of the signal describes the random variations of signal from site to site and the degree to which the noise is spatially correlated. Its Fourier transform is the noise power spectrum (NPS),

$$\text{NPS}(u) = \text{FT} \left[\int s(x')s(x - x')dx \right] = S^2(u) . \quad (4.55)$$

The zero frequency value of $\text{NPS}(u)$ is the variance of the image under conditions of uniform illumination.

When an incident image signal is modified by a detector spreading function, the resulting NPS is given in terms of the MTF

$$\text{NPS}_{\text{OUT}}(u) = \text{NPS}_{\text{IN}}(u)|T(u)|^2 . \quad (4.56)$$

In practice there is additional noise because image spreading is a stochastic process involving individual quanta rather than a continuous function, so that further statistical fluctuations are introduced.

The frequency dependence of the detector signal-to-noise performance is described by a detective quantum efficiency (DQE), related to the NPS and MTF by,

$$\text{DQE}(u) = \frac{G^2|T(u)|^2\text{NPS}_{\text{IN}}(u)}{\text{NPS}_{\text{OUT}}(u)} , \quad (4.57)$$

where G is the overall gain of the system and $\text{NPS}_{\text{OUT}}(u)$ is the NPS of the detector output signal. This expression connects together the gain, spreading and noise properties of the system into a single function that describes the imager performance. It can be seen that a high value of the measured NPS compared to the input noise corresponds to a low DQE.

The analysis of the DQE for large area detectors is fairly complete as a result of the work of Cunningham, Siewardsen and others [4.68, 75–77]. While rather involved, some general points can be made regarding the difference between phosphor and photoconductor detection, as well as the effects of electronic noise. Perhaps the most important point is that the DQE is proportional to the fraction, α_X , of X-rays that are absorbed, and this factor is the upper limit on the DQE. It is therefore important to have a high absorption.

The phosphor and photoconductor systems are distinguished by their different MTF. There is always significant image spreading when a phosphor is used, while the photoconductor devices have essentially no spreading. The absence of spreading is not always beneficial, and can reduce the DQE in two ways. First, when the fill factor, F_F , is less than unity, the absence of spreading ensures that only the fraction F_F of the absorbed flux is detectable, and consequently the upper limit on the DQE is reduced to $\alpha_X F_F$. There is no such proportional loss of DQE when there is some image spreading, because some part of the signal from all the absorbed X-rays are detected.

The second effect on the DQE is the more subtle property of noise aliasing, which places an upper limit on the DQE at the Nyquist frequency of $\approx 0.4 \alpha_X$ [4.76]. When an X-ray hits a detector with no spreading, there is no knowledge where it hit within the pixel and some spatial resolution information is lost. However, when there is image spreading, the relative intensity of signals in adjacent pixels provides the additional spatial information. The apparently paradoxical result, that a detector with image spreading has a better performance at high spatial resolution than one with no image spreading, only applies if the gain is high enough, and comes at the price of increased sensitivity to additive noise when the MTF is low.

The DQE for a detector with some image spreading can be approximated as

$$\text{DQE}(u) = \frac{\alpha_X}{1 + \beta + \frac{1}{gT^2(u)} \left(1 + \frac{q_N^2}{\alpha_X g S} \right)}, \quad (4.58)$$

where g is the total gain (excluding the X-ray absorption), q_N is the additive noise, and S is the X-ray flux [4.68, 75–78]. The term β represents additional noise from the phosphor arising from the variance in the gain, and has a typical value of 0–0.2. The term $1/gT^2$ describes the effect of the MTF in the absence of additive noise and shows that the detector can overcome a low MTF provided that the gain is large enough that $gT^2(u) > 1$. These systems have gains of 100–1000, so that in principle the DQE can be maintained to high spatial frequency even when the MTF is rather small.

The additive electronic noise further reduces the DQE, particularly where the MTF is small. At low spatial frequency (i.e., $T(u) = 1$) the DQE falls when,

$$q_N > g\sqrt{\alpha_X S}. \quad (4.59)$$

This result confirms the intuitive expectation that the additive noise has its greatest adverse effect at low X-ray exposure, and that a high gain helps to overcome the effects of noise. At high spatial frequencies, the condition for the noise to dominate the DQE becomes,

$$q_N > gT(u)\sqrt{\alpha_X S}, \quad (4.60)$$

from which it is clear that the low MTF region is more readily affected by noise. In summary, the ideal DQE occurs with high X-ray absorption, high gain, an MTF with small but non-zero spreading and low additive noise. The effects of absorption and additive noise on the DQE are illustrated in Fig. 4.36.

The analysis and measurement of the DQE begs the question of what values are required. The answer is difficult to state with any precision, and certainly depends on the specific application. We have seen that the DQE decreases at low incident X-ray flux due to additive noise, and at high spatial

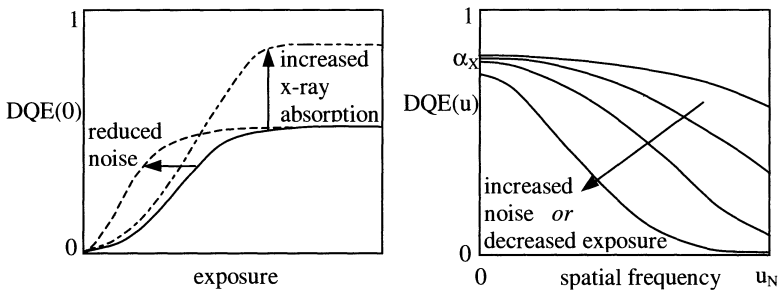


Fig. 4.36. Illustration of the form of the zero frequency DQE (*left*) and frequency dependent $DQE(u)$ (*right*) as the X-ray absorption, exposure and additive noise are varied

frequency due to image spreading. It is essential to understand the properties of the image to decide whether the DQE is adequate for any specific situation. An image suitable for medical diagnosis must contain a sufficient incident flux to allow observation the features to be discerned. Usually this represents a combination of spatial frequency and signal-to-noise requirements. If high S/N is essential then additive noise may be relatively unimportant because the incident quantum noise is large. In situations where a very weak flux is detected, it is preferable to increase the signal by having large pixels, at the expense of spatial resolution where there may be no useful information because of the low DQE. In general the imager design must be optimized for each specific application.

Detector Performance Measurements. The measurement of the pre-sampled MTF is commonly performed by imaging through a narrow slit with a width much smaller than the pixel size [4.78]. The slit is positioned at a small angle to the axis of the pixel array. The image along one row of pixels measures the signal that corresponds to illumination in a narrow line across one pixel. The next row of pixels is another sample of the signal, but with the illuminated line moved slightly across the pixel. Many such rows create a composite image equivalent to that of a line source being scanned across a single pixel. The result is the convolution of the phosphor line-spread function with the sensor shape, and its Fourier transform is the presampled MTF according to (4.54). An example of the MTF is shown in Fig. 4.37 for an amorphous silicon photodiode imager using a Lanex regular ($GdO_2S_2:Tb$) phosphor screen [4.79]. The predicted result is based on the known MTF of the phosphor, and takes into account that the pixel is not square, and has metal lines covering the surface, so that the presampled MTF is slightly different in the two orthogonal directions. The measured MTF is slightly less than the calculated value particularly at low spatial frequency where the MTF drops more rapidly than expected. Further investigation showed that the reduced MTF is due

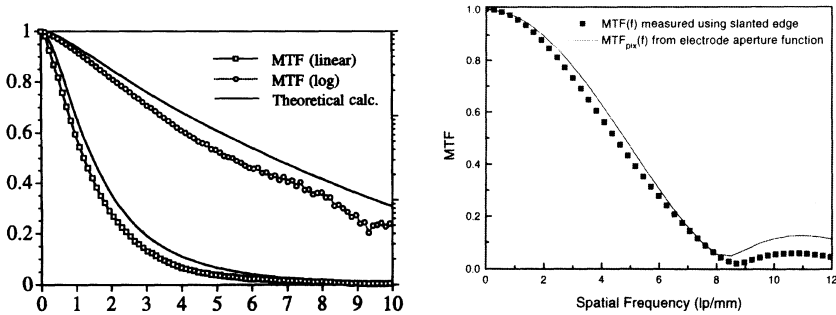


Fig. 4.37. Examples of the MTF of an a-Si:H photodiode array with a Lanex regular screen with 127 μm pixels (*left*) [4.80], and a selenium photoconductor array with 160 μm pixels (*right*) [4.39]

to X-ray fluorescence in the glass substrate arising from X-rays that are not absorbed in the phosphor [4.80]. The glass substrate contains barium, which fluoresces weakly and the spreading of the X-rays causes the small reduction in MTF. This is an illustration of the subtle effects that may influence the detector performance.

The MTF of a selenium photoconductor array is also shown in Fig. 4.37 for comparison. Because there is virtually no spreading of the image in the selenium layer, the MTF approximates to the sinc function in (4.54), for which the MTF is about 70% at the Nyquist frequency, (assuming 100% fill factor). At a spatial resolution of 3 lp/mm, the Lanex regular imager has an MTF of about 10% while the selenium imager has $\approx 70\%$. As the preceding discussion of DQE shows, the high MTF alone does not ensure that the selenium imager has the higher DQE, but does make the imager less sensitive to degradation of the high frequency DQE by additive electronic noise.

A one-dimensional NPS is measured by taking the Fourier transform of the signal along a row of pixels illuminated by a uniform source, with corrections to remove any fixed pattern signals, or by analyzing the response of individual pixels in a sequence of similar images. Some NPS data are shown in Fig. 4.38 for a range of X-ray exposures that are typical for fluoroscopy applications in an imager with 200 μm pixels and a CsI structured phosphor [4.35]. It is a small area imager which therefore has low data line capacitance and particularly low values of the additive electronic noise. The NPS at zero frequency increases in proportion to the X-ray exposure as expected for the Poisson statistics of the source (for which the variance equals the mean), and the decrease at higher spatial frequencies generally reflects the MTF according to (4.55). The NPS of the dark signal is independent of spatial frequency, which shows that the readout noise has no spatial correlation, as is expected for the pixel and amplifier noise described in Sect. 4.4.2. The observation that the NPS does not fall off as fast as the square of the MTF in Fig. 4.29, in part due to the presence of additive noise, illustrates that the detector has

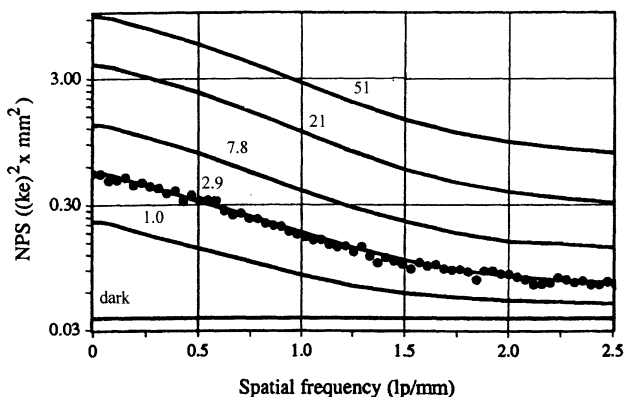


Fig. 4.38. Measured noise power spectrum in the dark and for different X-ray exposures from $1\mu\text{R}$ to $51\mu\text{R}$ at 75 kVp . The 192×192 pixel array has $200\mu\text{m}$ pixels and a CsI phosphor [4.35]

introduced excess noise at the higher spatial frequencies. The frequency dependent DQE is usually obtained from the measured NPS and MTF, using (4.57).

Siewardsen et al. have reported a detailed DQE model for the TFT/photo-diode imager with both Lanex and CsI:Tl phosphors [4.77]. The model gives an excellent fit to data from an array with $127\mu\text{m}$ pixel size and can therefore be used to predict performance for many imaging situations. Figure 4.39 shows calculations of the zero frequency DQE for conditions that correspond to applications in radiography, fluoroscopy and mammography. The figure shows the effects of radiation dose, which generally follow the trends outlined in Fig. 4.36. The DQE reaches a constant value at large exposures that is primarily determined by the X-ray absorption, and which is larger for CsI than Lanex, and lower at higher X-ray energies. An amplifier noise of 1000 electrons is assumed and it is seen that fluoroscopy falls within the dose range where the DQE is low. Figure 4.39 shows more explicitly the effects of additive noise. The noise decreases the DQE and the magnitude of the effect depends on the X-ray energy and exposure. As expected the additive noise has the largest effect with low exposure characteristic of fluoroscopy.

Figure 4.40 shows the measured values of the spatial frequency dependence of the DQE for a diode addressed array with pixel size $196\mu\text{m}$ [4.43]. The array uses CsI:Tl phosphor and has a sensitivity of 1150 detected electrons per incident X-ray at an X-ray energy of 70 kVp . The low frequency DQE values of 0.4 – 0.75 are generally consistent with the calculations in Fig. 4.4. The data show the decrease in DQE with increasing spatial frequency and the decrease with reduced exposure.

The choice of pixel size represents a compromise between sensitivity and spatial resolution, and the measurement of DQE helps achieve the optimum

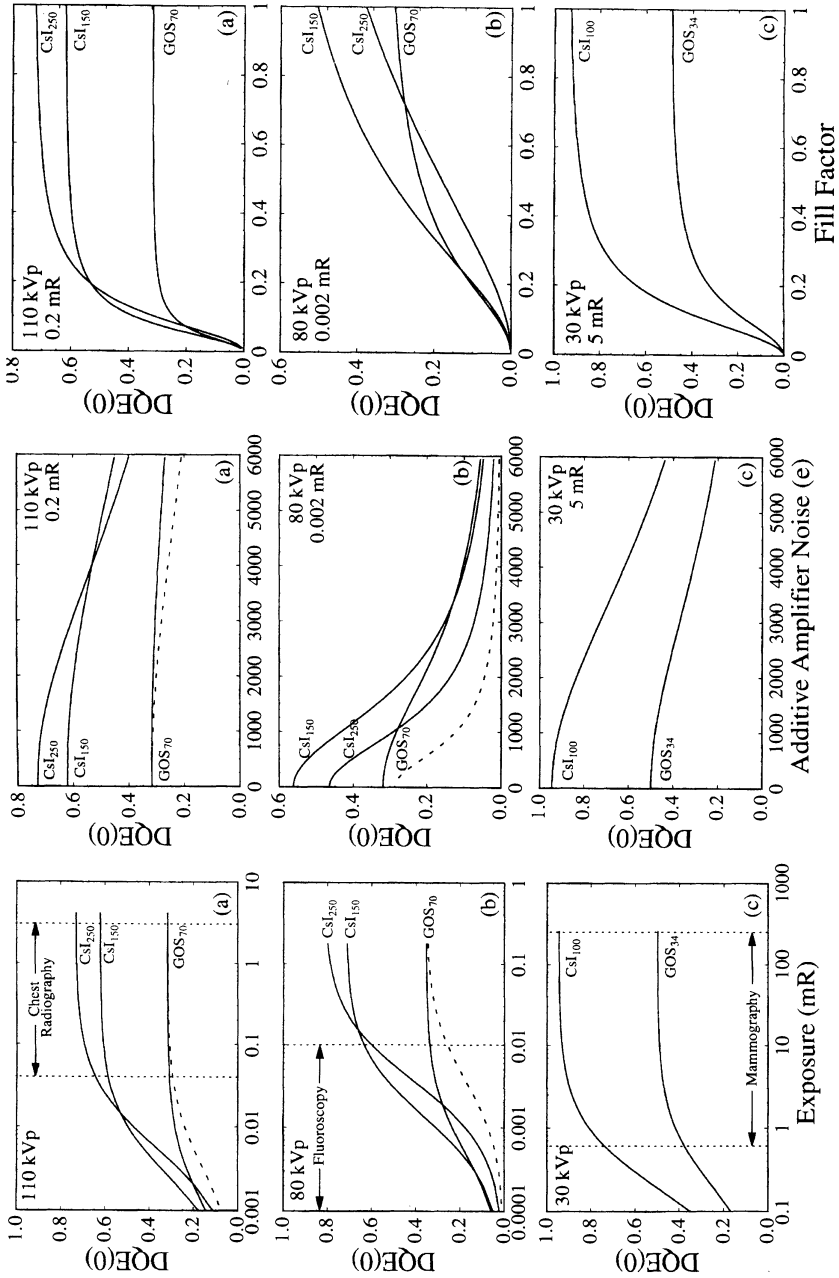


Fig. 4.39. Calculated DQE for different exposure and measurement conditions [4.77]

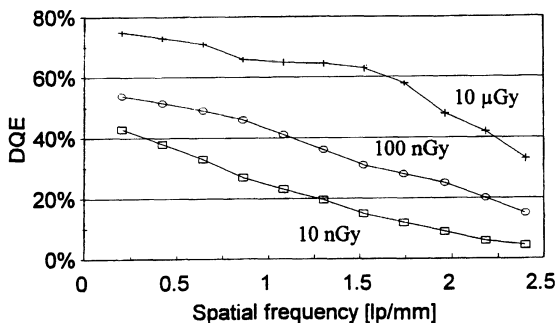


Fig. 4.40. Frequency dependent DQE of a diode addressed array

choice. At low exposure in Fig. 4.40 the DQE drops to about 10% at 2 lp/mm. A higher resolution array would have an even lower DQE because of the lower signal at each pixel. Thus little is gained by increasing the resolution because the DQE at high frequency is essentially zero. However, at high exposures a higher spatial resolution can yield additional image information.

4.5 Applications of Large Area Image Sensors

4.5.1 Medical X-Ray Imaging

Medical X-ray diagnostic imaging is expected to be the main application of a-Si:H image sensor arrays. The need to obtain images from major anatomical parts of the body – for example the chest – and the lack of a practical means to focus X-rays, necessitates the use of a large area sensing device. X-ray imaging of inanimate objects for security inspection or to confirm the internal structural integrity – known as non-destructive evaluation (NDE) – and scientific imaging applications such as X-ray crystallography, are other important applications of the technology that are discussed in Sect. 15.2. The same imagers can be configured for neutron imaging – a specialized but significant procedure for NDE.

The various techniques can be further distinguished by the need for single images or continuous video sequences. Single images are usually obtained at high resolution for careful inspection and diagnosis. The benefits of digital acquisition is that the image can be enhanced in contrast, magnified and processed in other ways to allow the optimal observation of fine detail. Video images are used to observe internal motion and are necessarily acquired in electronic form. Generally the spatial resolution requirements are more relaxed but high sensitivity is demanded. The following examples of the applications illustrate different requirements and usage of the image sensor arrays.

Radiographic Imaging. Most people have experienced an X-ray radiography procedure to diagnose a broken bone or other medical condition. Indeed, of order 1 billion X-ray medical images are taken each year. The traditional technique captures images with X-ray film, which consists of a large sheet of photographic emulsion between two phosphor screens. The film records the image of X-rays transmitted through the patient as a result of a brief X-ray exposure. After chemical development of the film, the diagnosis is performed by a radiologist who views the negative film placed on a light box. The technique has been in use for 100 years – the first diagnostic X-ray image was recorded in 1896, less than one year after X-rays were discovered by Roentgen. The procedures for the medical use of X-ray film are highly advanced as a result of the long development time.

The goal of radiographic imaging is to obtain high spatial resolution and contrast in the observation of the anatomical features under investigation, at the lowest possible dose to the patient. The principal concern with the X-ray imaging procedure is that there is no completely safe X-ray dose, and so the benefit to the patient must be matched against the risks of the exposure. An absolute requirement of any new imaging technology, such as the amorphous silicon arrays, is that the same quality of diagnosis can be achieved with an equivalent or lower dose to the patient. Fortunately, the arrays seem set to achieve this goal, and the first clinical studies appear to justify the expectations [4.81].

The attainment of high image contrast depends on the imaging conditions, the detector and the image display. The X-ray energy and dose for the procedure are chosen with care to maximize the contrast between bone and tissue. The contrast originates from the difference in their attenuation coefficients which is about a factor 3 up to 40 keV and decreases at higher energy (see Fig. 4.33). The X-ray generator emits a broad band X-ray spectrum, which varies with the accelerating voltage and can be additionally modified by filtering to remove the low energies. The X-ray energies of interest are those for which there is partial attenuation by the body with the maximum difference of transmission between bone and tissue etc. Low energy X-rays are completely attenuated by the body and are undesirable because they expose the patient without contributing to the image. High energy X-rays pass through virtually unattenuated and therefore also give no contrast. The optimum image contrast involves a choice of the X-ray energy, filtering and exposure, and differs for different parts of the body.

In a typical chest X-ray, the X-ray generator is operated at 80–120 kVp, with most of the intensity centered at about half the maximum energy. (The unit kVp refers to the generator accelerating voltage and is the upper limit on the X-ray energy spectrum.) The dose is 3–5 mR, which corresponds to an X-ray flux of $1\text{--}1.5 \cdot 10^7$ X-ray photons/cm². Approximately 10–20% of the X-rays pass through the body to the detector, and the contrast in the transmitted beam is 20–50%, or 2–10% of the incident beam. The dynamic range



Fig. 4.41. Radiographic image

of an electronic detector should be at least 4000 (i.e., ≥ 12 bit digitization), so that the low contrast regions can be viewed without being significantly affected by digitization noise.

In 1998, several medical imaging companies are introducing amorphous silicon radiographic imagers with active areas up to $17 \times 17''$, which is the preferred size for chest X-rays [4.68]. The pixel size ranges from $127\text{--}160\ \mu\text{m}$ (a spatial resolution of 3–4 line pairs/mm), so that the total pixel number in the imager is 7–10 million. Compared to fluoroscopic applications (see below), the radiographic dose is quite large, in order that the contrast detail is not obscured by the quantum noise of the X-ray beam. The DQE is therefore less sensitive to additive noise (see Fig. 4.37), and is largely determined by the absorption of X-rays (4.58). The pixel size is a compromise between sensitivity and spatial resolution. To give an example, an exposure of 1.3×10^7 photons/cm² with a pixel size of $150\ \mu\text{m}$ yields 3×10^3 photons/pixel. With an average conversion gain of 500 electrons/photon, the maximum pixel charge is 0.3 pC, which is consistent with the pixel capacitance of the array. An example of a radiographic image is shown in Fig. 4.41.

Both scintillator and photoconductor systems are suitable for medical radiography and both types are being developed. Since $\text{GdO}_2\text{S}_2\text{:Tb}$ phosphors are conventionally used for X-ray film, their use in a-Si:H imagers gives essentially the same spatial frequency performance up to the Nyquist frequency. At 4 lp/mm, a typical $\text{GdO}_2\text{S}_2\text{:Tb}$ phosphor has a MTF of 10–20%, and so the absence of detector response at higher spatial frequencies is probably not significant, although a detailed optimization of the pixel size has yet

to be reported. CsI scintillators offer improved spatial resolution, while the photoconductor arrays give a further improvement in resolution.

The means by which a radiographic image is viewed is also important to the detection of contrast detail. X-ray film is viewed in a light-box at high brightness, since this improves the perceived image by the fovea (the high resolution area of the retina). Soft displays for electronic image sensors need further development in order to match the capabilities of the detector. There are CRT displays with 2000×2500 pixels, but these only display about half a large radiographic image, and display is not very bright. Possibly, amorphous silicon active matrix LCDs will become the display of choice when their gray scale response is further improved, as they have high resolution and high brightness.

The DQE is an incomplete measure of the detector performance because it does not take into account the process of viewing the image, which depends on the complex non-linear response of the human vision system. For this reason, testing of detector performance ultimately depends on comparative observations by radiologists. New models of the human vision system are being developed which, if successful, may allow the entire system of detector, display and human observer be simulated accurately [4.82].

Mammography imaging requires a significantly higher spatial resolution than most other radiographic procedures. The purpose of mammography is to screen patients for the various precursors of breast cancer including micro-calcifications, which are very small features with low contrast. A high dose and a pixel size of $50\text{--}100\text{ }\mu\text{m}$ are needed to resolve the features. This application may be well suited to photoconductor detectors which can provide the high resolution, and the low X-ray energies used in the procedure allow for thinner photoconductor layers.

The desirable features of a digital replacement for X-ray film based on a-Si:H image sensor arrays include the following:

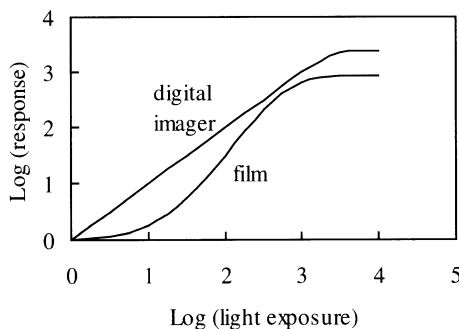


Fig. 4.42. Schematic illustration comparing the response of film with the more linear response of a digital imager

1. The acquisition and display of the electronic image is immediate, taking at most a few seconds. This provides rapid confirmation that the correct exposure conditions were used.
2. Film has a non-linear response to exposure, which is compared to the linear response of digital imagers in Fig. 4.42. As any photographer knows, the limited dynamic range of film makes it essential to have the correct exposure, and when regions of very different optical density are of interest, it is impossible to optimize the exposure for the complete image. The digital imager, on the other hand, has a linear response over a wide dynamic range, and image processing can selectively enhance the contrast of different regions, as well as reproducing the response of film to give an image that is familiar to radiologists. Film loses sensitivity at low exposures compared to the image sensor arrays, and so the new imagers offer the ability to produce good images at lower doses, which reduces the dose to the patient.
3. The archival storage of film consumes much space and labor, and incorrect filing frequently results in the loss of an image. Electronically filed images can be carefully tracked in a data base and offer tremendous space savings.
4. Telemedicine is enabled by the ability to capture and transmit digital images.

Fluoroscopy. Fluoroscopy is the real time acquisition and display of X-ray image sequences, and is used when it is important to observe internal motion of the body. A typical application of fluoroscopy is in non-invasive surgery, such as cardiac angiography to correct heart disease. In this procedure, the cardiac artery is opened by inflating a balloon that is passed into the body along a guide. The procedure relies entirely on fluoroscopic X-ray imaging to ensure that the guide is positioned correctly. These imagers are generally mounted on large C-arms, so that they can be positioned anywhere on the patient and rotated about an axis along the patient. Often, a pair of such imagers are mounted at right angles to give alternative views, and the surgeon views the progress of the procedure on a bank of video monitors as shown in the photograph in Fig. 4.43.

The existing fluoroscopy technology uses an image intensifier tube (IIT) which is a large vacuum tube. A columnar CsI phosphor layer inside the tube absorbs the X-rays and an electron emissive photocathode causes electrons to be released from the surface, where they are accelerated and focussed by the electron optics of the IIT. The result is a small bright image on a second phosphor screen which is viewed with a conventional video camera. The IIT has excellent sensitivity due to its very high gain, but is a bulky and heavy device and suffers from some image distortions and veiling glare, as well as sensitivity to external magnetic fields.

Amorphous silicon imager technology offers a flat panel replacement to the IIT which is less intrusive to the surgeon and has less image distortion.

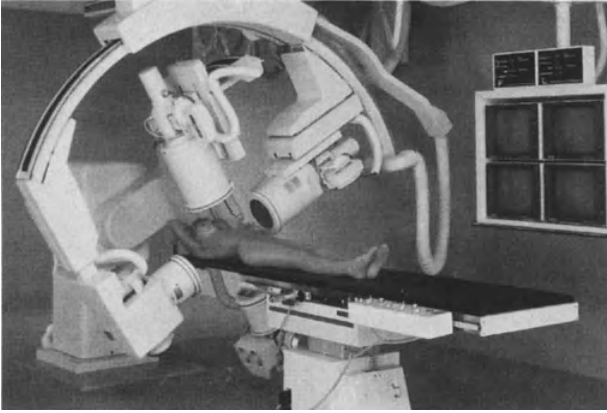


Fig. 4.43. Photograph of a hospital fluoroscopy system

Video rate image acquisition is well within the capability of the a-Si:H arrays, at least for arrays with 1000–2000 lines. The challenge for the image sensors is the exceptional sensitivity requirements. Fluoroscopic imaging does not require high contrast, but instead the emphasis is on very low dose, because the patient is exposed for an extended time. The typical exposure is 1–10 μR per frame, which is about three orders of magnitude less than the radiographic dose. Sensitivity is gained by increasing the pixel size to 200 μm or larger. Even then, an exposure of 1 μR corresponds to only about 10 X-ray photons/pixel, and the quantum limited signal-to-noise is just barely high enough to discern an image. In this regime, the DQE tends to be dominated by the electronic noise, and a good fluoroscopic imager should have high sensitivity and very low noise. A CsI phosphor of about 400–500 μm thickness, as used in IITs, has demonstrated similar performance to IITs, providing the electronic noise is no more than 1000 electrons and the remainder of the system is well optimized. Fluoroscopy is an excellent application for high fill factor array designs, and high gain X-ray photoconductors both of which have high detector sensitivity and high DQE at low exposures. Fluoroscopic imaging using a photoconductor detector has not been thoroughly studied, and may be made difficult by the build-up of trapped charge.

Image lag is an obvious concern for video imaging. A small amount of lag can actually be beneficial because the temporal averaging of the image reduces the noise, so long it is not sufficient to cause motion blurring artifacts. A more important issue is that during a fluoroscopy procedure, the dose is occasionally increased to radiographic levels to obtain a high contrast image, and then returned immediately to the low level to continue monitoring. An image lag of only 1% from the high intensity frame can overwhelm the subsequent images.

Although challenging, there is every reason to expect that a-Si:H imagers will replace the IIT for fluoroscopy because of its compact size, and fully digital operation which allows more flexibility in image processing and display. The light weight of the detector allows a considerable saving in the bulk and cost of the support structure.

Radiation Therapy. Radiation therapy is the use of large doses of radiation to destroy cancerous tumors. High energy (megavoltage) gamma rays in the range 1–50 MeV are generated by an accelerator or a radioactive source. The aim is to deliver a lethal dose to the tumor with minimal damage to the surrounding healthy tissue, and generally this is accomplished by exposing the patient from different angles with a beam that is carefully shaped to match the outline of the tumor in each direction of exposure. The procedure is one of the standard treatments for many forms of cancer, with patients receiving several doses over a period of time. An imaging device is needed to verify that the gamma beam is correctly positioned within the patient and to monitor the exposure.

The therapy imager requirements are significantly different from those used for diagnostic purposes. The therapy dose is extremely large, amounting to 10–100 R per treatment, so that radiation damage is a major concern. Most silicon integrated circuits are destroyed by total exposures of 100 kR, although special radiation hard devices can survive above 1 MR. Amorphous silicon is insensitive to high energy radiation, and both sensors and TFTs have been exposed to 10 MR of gamma rays with only small degradation of their properties [4.83]. Part of the explanation is that the devices are so thin that the probability of an interaction in the material is very low. In addition, amorphous materials may be less susceptible to radiation damage since they are already disordered.

Figure 4.44 shows that the leakage current of p-i-n photodiode only increases by a factor 5 after a rapid exposure of 2MR, and much of the excess current decays after a few days [4.83]. The TFT characteristics show similar insensitivity, with a threshold voltage shift of 1–2 V and some increase in leakage current. Neither device shows a significant increase in noise after such high exposures.

Although the radiation therapy dose is very large, image acquisition is not simple because of the high gamma-ray energy. The difference in attenuation coefficient between bone and tissue decreases such that the contrast in the image is no more than 1%. A very high dynamic range imager is therefore required to allow clear observation of the tumor. Fortunately the required spatial resolution is quite low, and pixel sizes of 500–1000 μm are sufficient to image the procedure. Figure 4.14 indicate that a dynamic range of $> 100\,000$ is achievable from arrays with such large pixels, which is more than adequate.

The sensitivity of the detector to high energy gamma-rays is low, because of the low attenuation in the phosphor screen. The sensitivity is enhanced

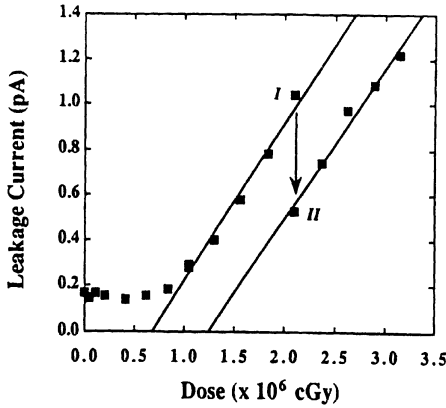


Fig. 4.44. Effect of high gamma-ray dose on the a-Si:H p-i-n photodiode leakage current. The decrease between points I and II are due to resting the sample at room temperature [4.84]

by placing a metal sheet such as copper of thickness about 1 mm on top of a phosphor such as $\text{GdO}_2\text{S}_2\text{:Tb}$, as illustrated in Fig. 4.45. Photons interact with the copper to create high energy electrons, which are scattered forward into the phosphor, where they cause ionization as at lower energy. The copper film increases the interaction probability and raises the overall emission intensity from the phosphor, but even with this addition the efficiency is much lower than for radiographic imaging.

Radiation therapy was the first medical imaging application proposed for a-Si:H image sensor arrays [4.84–86]. Research has confirmed that the approach is viable and gives imaging performance superior to any other digital technology. A $20'' \times 20''$ prototype imaging system operating up to 20 frames/s has been reported by Colbeth et al., who show quantum limited noise with doses from 0.6 to 25 cGy using both a 6 and 18 MV source [4.87]. Antonuk et al. discuss the merits of a dual energy imager that simultaneously acquires megavoltage and radiographic images [4.86]. This approach is enabled by stacking two flat panel imagers on top of each other in such a way that the top imager is relatively transparent to the high energy beam. The much better contrast of the radiographic image allows a more precise positioning of the megavoltage beam to the patient. This is just one example of novel imaging modalities that result from the flat panel imager structure.

4.5.2 Other Radiation Imaging Applications

Non-Destructive Evaluation. Non-destructive evaluation (NDE) involves both X-ray radiographic and fluoroscopic imaging of inanimate objects. Some examples of its use are the inspection for flaws in critical components such as airplanes, oil pipelines and nuclear power stations, monitoring for the

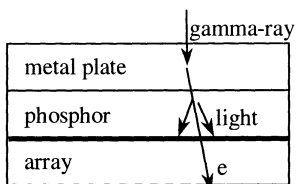


Fig. 4.45. Illustration of high energy gamma ray detection using a metal sheet and phosphor on the a-Si:H array

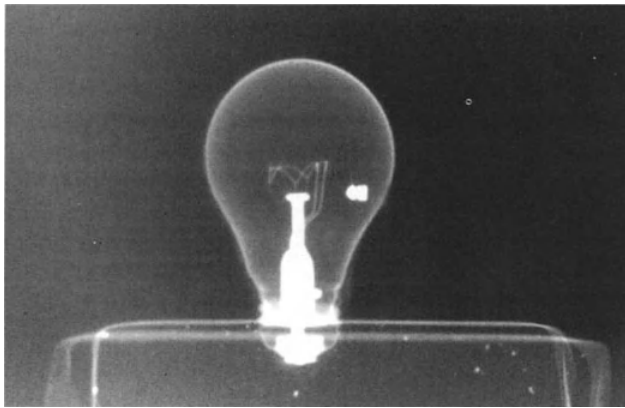


Fig. 4.46. X-ray image of a bullet piercing a light bulb

quality of a variety of manufactured goods and food, and security inspection systems in airports etc. The total market is about \$100 M which, although significant, is considerably smaller than the medical imaging market. The traditional use of X-ray film for NDE is slowly changing to real-time digital imaging. Amorphous silicon imagers offer many of the same advantages as in medical imaging – compact size, high radiation tolerance, both radiographic and fluoroscopic modes, immediate viewing of the image and digital image enhancement, storage and transmission.

The main difference between NDE and medical imaging is that a low dose is less critical and the range of exposure conditions is much broader. Very high energies are needed to penetrate thick steel structures, and various applications require high contrast, high resolution or high speed. Figure 4.46 is an example of the latter and shows an X-ray image of a bullet piercing a light bulb and was acquired with an a-Si:H imager using a very short X-ray burst to freeze the motion.

X-Ray Crystallography. Crystallography is one example of the possible scientific applications of a-Si:H image sensors. Much research is presently directed to identifying the structure of proteins, using X-ray diffraction as the

main tool. Proteins are very large molecules containing up to 100 000 atoms which form rather delicate crystals with large unit cell size. The diffraction pattern is correspondingly complex and contains a similarly large number of unique spots. Fairly low energy X-rays (5–20 keV) are employed and the usual procedure is to acquire a set of several hundred diffraction patterns by rotating the crystal in roughly 1 degree increments about an axis perpendicular to the beam. The inversion of the data set into a crystal structure is a formidable computational problem. Digital acquisition of the images eliminates the equally formidable task of obtaining all the diffraction spot coordinates by digitizing film.

A large digital imager is desirable because measurement far from the crystal reduces the effects of scattered X-rays and the blurring effect of the finite size beam. Relatively rapid image acquisition is desirable when measurements are done at a synchrotron sources where the flux is high enough to acquire an image in a few seconds. On the other hand laboratory X-ray sources produce very weak diffracted intensity and in this case, long integration times are needed. High sensitivity is important because the protein crystals are easily damaged by X-rays, and therefore the exposure must be minimized. Finally, the imager needs to have a high dynamic range, because important structural information is contained in the wide range of intensities of the Bragg peaks.

Amorphous silicon image sensors satisfy most of the requirements, with sensitivity being the most challenging [4.88–90]. As with fluoroscopy, the low flux places a particular premium on high sensitivity and low electronic noise. It is of interest to compare the amorphous silicon sensors with the charge coupled devices (CCD) that represent the present state-of-the-art in detectors. A cooled CCD has an electronic noise of < 10 electrons, which is 100 times lower than the amorphous silicon arrays. However, CCDs have too small an active area for the application. We noted in Sect. 4.3.1 that imaging from a large phosphor with a lens has very low optical transfer efficiency, which more than offsets the lower noise. The solution applied to crystallography and similar applications is to use multiple CCD devices and to couple the light from the phosphor using a tapered fiber-optic plate. Naday et al. describe an imager using 9 CCDs and a taper which de-magnifies the image by a factor 3.5, yielding a sensitive area of 15×15 cm [4.90]. Even so, they estimate that an a-Si:H imager with a phosphor converter would have a comparable performance [4.88]. Although the fiber-optic taper is more efficient than a lens, contact imaging with the phosphor has a larger optical efficiency by about a factor 20, and the larger area of the a-Si:H device yields a further performance gain which together compensate for the lower noise of the CCD.

Low energy applications such as protein crystallography are well suited to image sensors using X-ray photoconductor detectors, because thinner layer and lower fields are required. Either selenium or PbI_2 could provide a crystallography detector with better performance than the CCD devices. Other

scientific applications that have been considered for the large area imagers include gamma ray space astronomy and recording DNA fragments in gel electrophoresis.

Neutron Imaging. Neutron imaging is a highly specialized branch of non-destructive testing, but illustrates the range of possible radiation imaging applications of a-Si:H sensor arrays. Hydrogen has almost no absorption of X-rays, but scatters neutrons effectively. Thus, neutron imaging can reveal features not seen in an X-ray image, and is particularly useful for detecting corrosion which usually has water associated with it [4.91]. The lack of a convenient source of neutron clearly restricts the applications, but the technique is used on military aircraft in locations that have a nuclear reactor. Detection of neutrons is actually quite easy because of the existence of some specific neutron reactions. Neutrons react with ^6Li and one of the fragments is a high energy alpha particle. Phosphors are readily made containing ^6Li , so that the alpha particles cause ionization and light emission. The gain is actually higher than for radiographic X-rays, since one absorbed neutron can yield about 175 000 visible photons. This gain is sufficiently larger than the readout noise that the imager is able to detect and count individual neutrons, which is a desirable imaging mode since the neutron flux is very low. The second detection method uses a similar nuclear reaction with gadolinium, and therefore the standard $\text{GdO}_2\text{S}_2\text{:Tb}$ phosphor is sensitive to neutrons.

4.5.3 Document Scanning

Document scanning plays an increasing role in office management systems. Most scanners use linear sensor arrays and either the paper or the detector is moved to image the page. Two-dimensional devices capture the complete page without the need for mechanical motion. Since imaging is done in visible light, the image can be focussed onto a small detector and so the reason for a large area device is less compelling than with X-ray imaging. However, the large area arrays do offer some advantages and some novel system designs relating to high speed scanners, compact scanners and book scanning.

An a-Si:H image sensor allows a contact imaging approach to be used when the array is as large as the paper to be imaged [4.92–95]. The paper is placed in direct contact with the imager and illuminated from behind, as illustrated in Fig. 4.47. The illumination source is immediately below the array and the light passes through the gaps in the pixel between the sensor and the address lines, where it is reflected off the paper and imaged by the sensor. The sensor is protected from direct illumination by the opaque bottom metal contact. The gap between the paper and the sensor must be less than about half the pixel size enough to prevent light scattering to adjacent pixels, but large enough to allow the light to reach the front surface of the sensor. In practice, the light scattering within the paper is usually sufficient to ensure

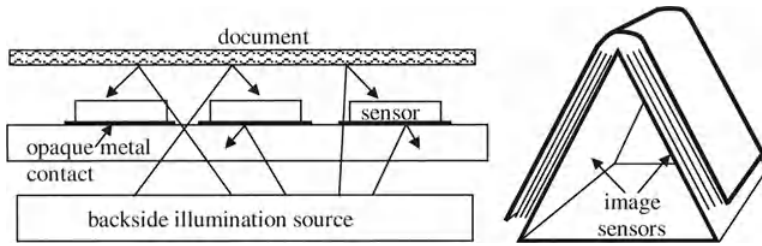


Fig. 4.47. Contact imaging of a document using back illumination (*left*). The same device configured as a compact book scanner with no moving parts

that the sensor is illuminated. This approach to document imaging has been successfully demonstrated and provides a compact imaging system with no moving parts.

Contact imaging enables other scanner designs that cannot be made with a conventional lens coupled system. Figure 4.47 illustrates a design for a book scanner that comprises two large area arrays forming a wedge-shaped structure. The book is placed over the wedge and is imaged from both surfaces. The illumination source is behind the two arrays.

Document scanning generally requires a higher resolution than X-ray imaging to avoid blurring the edges of letters and to prevent lines from showing jagged edges. FAX machines have a low resolution of 200 spot/inch (spi), while high quality full page document scanners typically have resolution of 300–600 spi. Wu et al. have implemented a design to double the spatial resolution of a a-Si:H sensor array with pixel size $127\text{ }\mu\text{m}$ (200 spi) [4.94]. The image is translated across the array by the distance of half a pixel in both directions, so that four sub-sampled images are captured and can be reassembled into a higher resolution image. This approach takes advantage of a low fill factor, which should be about 25% to image one quarter of the pixel at each sample. A slightly larger fill factor provides some oversampling which helps minimize aliasing effects. There are several ways in which the small shifts of the image can be accomplished. Wu et al. describe a one-to-one magnification lens-coupled system with a rotating glass wedge at the projection lens [4.94]. The wedge is rotated by 90° to move the image to the correct position for each sub-sample and the angle of the wedge determines the shift of the image. Measurements confirmed the increase the spatial resolution and that aliasing effects are eliminated.

The a-Si:H sensor arrays are well suited to color imaging because the spectral response of a-Si:H spans the visible spectrum (see Fig.4.2). The quantum efficiency is greater than 50% at 400 nm in a well designed sensor, increases to 80–90% at the maximum near 550 nm, and decreases strongly above about 700 nm, due to the energy of the band gap. In principle, color imaging may be performed by placing a color filter at each pixel, in a similar manner to the approach used for liquid crystal displays. Usually it is easier to

capture three consecutive images with red, green and blue illumination and superimpose the three color separations [4.93]. Provided that the color filters are chosen correctly, excellent color images are obtained. Chapter 7 describes how to fabricate color-selective a-Si:H photodiodes that could be integrated into matrix-addressed arrays.

4.6 Future Developments

At the beginning of 1999, X-ray medical imaging systems are just being introduced onto the medical imaging market. Most of these devices are $\approx 17''$ radiological imagers with pixel sizes of 127–160 μm , but smaller fluoroscopy systems are also close to product introduction. While these systems meet the requirements of the technology in terms of size and imaging performance, the technology is capable of significant improvements in sensitivity and resolution, and numerous other innovations can be expected to reduce the cost and improve the device yield. Most of the new systems use a-Si:H TFTs and photodiodes, with Lanex or CsI scintillators for X-ray detection, or a selenium photoconductor with a-Si:H TFTs. Continued experience with the technology will determine the relative roles for the scintillator and photoconductor approaches to detection. Some of the expected developments in the technology are as follows:

Array Size. LCD manufactures are introducing fourth generation process lines which use substrates of 80×80 cm or larger. The technology is therefore available to make $17'' \times 17''$ imagers from a single plate, rather than from 2 or 4 tiled arrays as in most large imagers made at this time. There seems little reason for any further increase in array size for medical imaging, and so a very large substrate is only useful when more than one array can be made on a substrate. Tiling of small arrays to make a large imager may be a preferred approach, since smaller arrays usually have significantly higher yield. The added expense of attaching readout electronics to both sides of the array might be worth the lower noise that results from dividing the data line in half.

Sensitivity. Many of the approaches discussed earlier to improve the array sensitivity can be expected to reach manufacturing over the next few years. The high fill factor designs are particularly applicable to high resolution arrays and PbI_2 or other new materials may improve the sensitivity of photoconductor arrays.

Noise Reduction. The performance of readout amplifiers can be expected to improve further with the anticipated developments of CMOS fabrication technology, and the experience of the chip design. Further improvement in

noise will result from array designs that lower the data line capacitance for which many approaches are possible. The TFT parasitic capacitance may be reduced by using a fully self-aligned device, and new developments in low dielectric constant materials as well as reduced process feature sizes can also be expected to trim the capacitance. An alternative approach is to introduce pixel amplifiers, since a gain of no more than 10 would completely remove the need for improved readout amplifiers or lower capacitance. Once the noise level is reduced to that of the kTC noise of the pixel, further improvements will involve reducing the capacitance of the sensors or developing a novel sampling scheme.

Electronics and System Integration. LCD technology is leading the way towards integrated drivers that can be applied to the image sensors. The vision is of a complete imager with gate drivers, readout amplifiers and control logic on the glass substrate. Drivers and control logic can certainly be made from polysilicon TFTs, and at least for radiography applications, they might even be made from a-Si:H. It is unclear whether a very low noise readout amplifier could be fabricated from polysilicon, but if the arrays have pixel amplifiers then extremes of amplifier performance are not needed. Other approaches to integration include chip-on-glass techniques to bond silicon ICs for drive and readout directly on the glass surface.

Processing. The feature sizes for the array are expected to decrease as the technology for large area processing improves. Such improvements will increase imager performance even without any fundamental change in design, by lowering the capacitance and increasing the sensor fill factor.

Applications. The main applications of a-Si:H image sensors have already been identified and it is clear that the medical imaging devices will dominate the field for the next few years. Document scanning applications are presently limited by the high cost of the image sensors, but these applications may expand rapidly as the manufacturing business grows. The market for large area arrays for general scientific applications is probably small compared to medical imaging, but could offer some interesting opportunities in astronomy, DNA sequencing etc.

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5 Novel Processing Technology for Macroelectronics

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Abstract. Large-area electronic circuits on thin foil substrates can be made with techniques adapted from conventional printing. Conventional printing can provide a resolution and an overlay registration of $10\text{ }\mu\text{m}$ and $\pm 5\text{ }\mu\text{m}$, respectively, which will allow making thin-film transistors (TFTs) at densities above 10 000 per square centimeter. An early example is the use of laser-printed toner etch masks for the fabrication of amorphous silicon TFTs. Patterned devices can be made by direct printing, as demonstrated by the jet printing of the active polymer for organic light-emitting diodes (OLEDs). Paper-thin foils of glass, steel, and polyimide can serve as substrates for making TFTs with characteristics comparable to those made on glass plates. Materials options for thin foil substrates are described. A study of the mechanics of films on stiff and compliant foil substrates shows that particularly rugged and flexible device structures can be made when the foils are very thin. Integrating OLEDs with thin-film transistors on steel foil substrates provides an early example of 3-D integrated components for macroelectronics.

5.1 Introduction

Following many years of experimentation, development and manufacturing, the active-matrix liquid crystal display (AM-LCD) has become a very successful product in laptop computers, workstations and personal computers (see Chap. 2). Its success seems assured in view of the favorable reaction of early users, who experience less eye fatigue when working with AM-LCD than with cathode ray tube (CRT) screens. For the wide-spread application of large-area electronics such as digital wallpaper, smart materials, and intelligent barcodes, its cost must be reduced to well below the present value of approximately \$5 per square inch (\$8 000/m²). This need for cost reduction has been recognized for some time. In the Giant Electronics program a group of Japanese laboratories sought to introduce printing techniques to the fabrication of AM-LCDs [5.1]. A group at the Philips Research Laboratories has been developing a technology for producing organic electronics by using a combination of photochemical and wet chemical reactions in spun-on layers on plastic substrates [5.2]. In this chapter we explore the application of printing techniques and thin foil substrates to large-area electronic, or macroelectronic, technology.

We begin with a brief discussion of the per-area cost of macroelectronics and make a case for the advantages of direct printing. The practicality of printing depends on the resolution and the overlay registration achievable by conventional printing techniques. These two parameters are discussed next. Then we describe the fabrication of amorphous silicon thin-film transistors with a process that uses laser printed toner masks instead of photoresist. This process illustrates the reduction in the number of steps achievable by printing. Our goal, the direct printing of patterned device materials, is illustrated by the jetting of polymer solutions to produce organic light-emitting diodes. Printing equipment often relies on the use of flexible substrates, which can be of particular advantage to macroelectronics because they are lightweight and can be very rugged. In this spirit we continue with a discussion of substrate materials, and of the mechanics of thin films on stiff and on compliant substrates. The practicality of a compliant substrate is illustrated with transistors on polyimide foil. Finally, we show that TFTs and OLEDs can be integrated to create a thin-film display on a foil substrate.

Macroelectronic products, for example display banners, digital wallpaper, or smart greeting cards in many cases must be large but need not necessarily have a high device density. Hence it is useful to gauge the cost of electronics per unit area rather than by cost of function.

We do this in Table 5.1. Inspection of the cost of integrated circuits (ICs) and displays shows that AM-LCDs cost an order of magnitude less than silicon ICs, but an order of magnitude more than present-day large-area photovoltaic (PV) modules. Thin-film PV modules are complex multilayer devices (Chap. 6). For example, the triple-junction module made by United Solar Systems Corporation contains 12 layers, some of which are only 10 nm thick [5.3]. These modules are integrated monolithically over large areas. In the Solarex module, a 0.80 m² large ten-layer device structure is interconnected using laser scribing [5.4]. Experience with PV modules shows that complex, multilayer, active electronics can be made at a cost well below \$ 1 000 per square meter. However, integrated PV modules need few patterning steps, and the individual diodes still measure many square centimeters. What will it take to fabricate inexpensive, large-area transistor electronics with a useful device density?

Table 5.1. The cost of integrated circuits and information displays

Technology	Cost (\$ · m ⁻²)
Silicon integrated circuit (microprocessor – memory)	500 000–50 000
Active-matrix liquid crystal display	10 000–6 000
Cathode ray tube	3 000–1 000
Amorphous silicon solar module (present → target)	400 → 100
Mail-order catalog (four-color print)	0.1

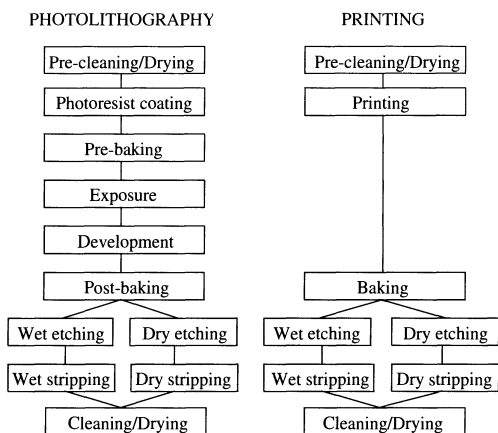


Fig. 5.1. *Left:* Steps in typical photolithography. *Right:* Steps in a process by which devices are patterned using printed etch masks. This figure illustrates the reduction in the number of process steps made possible by printing (from [5.5])

If we take the development of thin-film PV as a guide, we see that the introduction of large-area electronics relies on two coupled developments. One is the reduction of materials input, and the other is the reduction of the number of process steps. Using thin films, thin substrates and thin encapsulation reduces materials input. Reducing the number of process steps lowers the cost of equipment, and the consumption of the ancillary chemicals that are used in circuit processing. The number of process steps could be reduced greatly by the direct printing of the active materials as illustrated in Fig. 5.1 [5.5]. In drawing an analogy between the printing of books and the fabrication of integrated circuits this reduction becomes evident. If books were made like ICs, the paper would be first blackened with ink, and then the ink would be removed selectively to leave letters standing on a white background. Thus the use of laser printed masking layers, instead of photoresist, for etch or lift-off provides a good example for the transition from IC fabrication to book-printing techniques.

In IC fabrication the application or modification of the active material is separate from its patterning, because the material properties and the material pattern are optimized best when done in separate steps. If one wishes to print active circuits directly, one must devise materials that can be applied and patterned in a single step. The materials needed for the printing of active circuits include metallic conductors, insulators, semiconductors for transistors and light emitters, piezoelectric materials, etc. This approach to the printing of active circuits explores the territory that lies between ICs and printed-wire boards. In effect, large-area printed electronics will be active circuits monolithically integrated with their packaging.

Completed thin-film circuits are at most a few micrometers thick. Therefore the substrate and encapsulation constitute the bulk of the finished product. Reduction of their weight and thickness becomes important. When the substrate is reduced to a thickness where it becomes flexible, it also becomes usable in continuous, roll-to-roll paper-like production. The finished circuit then is a flexible foil, and using equally thin encapsulation will preserve this flexibility. We shall see that rugged thin-film circuits are a natural consequence of the mechanics of thin foil substrates.

Large-area transistor circuits may be integrated with light valves or emitters, light sensors, piezoelectric actuators, and many other opto-electronic or microelectromechanical devices. At the end of this chapter we illustrate the beginning of this integration with a TFT/organic light-emitting diode (OLED) pixel.

When large-area circuits are made by programmable printing, for example xerography or ink jetting, they can serve as vehicles for rapid prototyping [5.6]. It is conceivable that in an electronic printing shop single copies or short runs of circuits will be programmed and printed on short order. The laser printing of toner etch masks, which are designed on the computer that drives the laser printer, and the jet printing of polymers for organic light-emitting diodes illustrate this emerging capability.

5.2 Resolution and Registration: The Density of Functions Achievable by Printing

Programmable advertising banners may have square-centimeter size pixels and cover an area of many square meters. Intelligent barcodes, on the other hand, may cover only a few square centimeters but need high resolution. The development of microelectronics has shown that the search for high pattern density is one of the main drivers of IC technology. Therefore, it is instructive to estimate the density of active devices that could be produced by using conventional printing techniques.

Let us look at the density of amorphous-silicon thin-film transistors achievable by printing. The smallest size of a TFT will be set by two parameters. One is the smallest size of a pattern that can be defined by additive printing, which in IC technology is specified as the design rule. We give it the symbol λ . The second parameter is the accuracy of overlay, or registration, of subsequent patterns, which is quantified as the overlay alignment error $\pm\delta$. We illustrate the effect of these two parameters on the achievable density of thin-film transistors with the layout illustrated in Fig. 5.2, of a conventional inverted-staggered a-Si TFT without back channel passivation. Here we assume that any subsequent layer can be registered to any preceding layer with an accuracy of $\pm\delta$. Figure 5.2 shows that the overall length of the TFT is $(\lambda + 8\delta)$, its overall width $(W + 6\delta)$. We assume an inactive fringe of width δ . Thus the area occupied by the device is $(\lambda + 8\delta)(W + 6\delta)$.

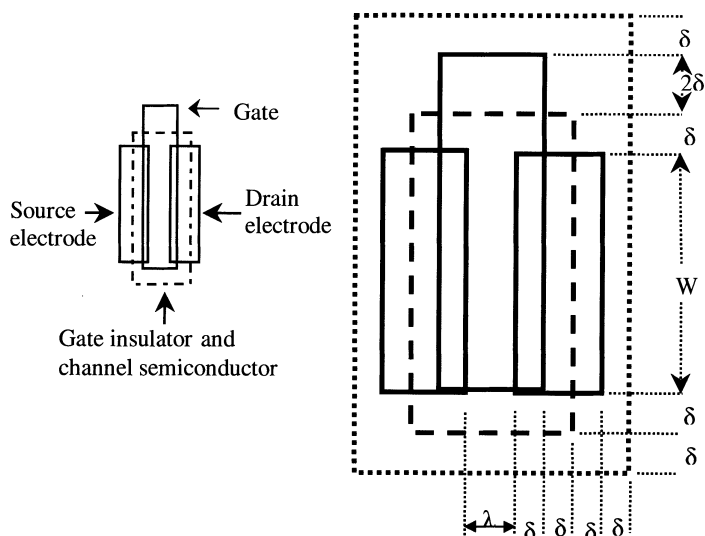


Fig. 5.2. *Left:* Layout of a thin-film transistor in the inverted staggered configuration. *Right:* The effects of resolution λ and overlay registration δ on the size of the TFT. λ sets the channel length L . The effect of the channel width W is discussed in the text

The printing industry defines resolution differently from the semiconductor industry, because it gauges by visual impact rather than device geometry and electrical function. However, the term resolution in spots per inch (spi) employed in digital imaging by the printing industry [5.7] is coming close to its use in microelectronics. For our first-order estimate we will assume that to both industries “resolution” means the number of resolvable, unbroken, line pairs per unit length. Resolution of present-day high-quality, large volume color printing is exemplified by the offset printing for the National Geographic Magazine, which is ≈ 2500 spi. Experts agree that current printing technology can achieve a resolvable line separation of $\lambda = 10\mu\text{m}$. This value will be our TFT gate length L . The accuracy of overlay registration δ achievable with present-day printing technology is $\pm 5\mu\text{m}$. This value will be our alignment tolerance [5.8].

The value of the W/L ratio will depend on the TFT application. It will be small in switches, and large in power transistors for driving OLEDs. Let us assume that we are building a logic circuit made of switches that need an ON current of $I_{\text{ON}} = 5\mu\text{A}$. The drain current in saturation is given by,

$$I_{\text{D}}(\text{sat}) = (W/L)\mu_{\text{e}} (\varepsilon_{\text{ins}}\varepsilon_0/d_{\text{ins}}) (V_{\text{g}} - V_{\text{th}})^2/2. \quad (5.1)$$

For the typical values of the electron mobility μ_{e} of $1\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, insulator dielectric constant ε_{ins} of 7.5, insulator thickness d_{ins} of 320 nm, and $(V_{\text{g}} - V_{\text{th}}) = V_{\text{S/D}} = 10\text{ V}$, $I_{\text{D}}(\text{sat})$ becomes $(W/L)\mu\text{A}$. The equivalent source–

drain resistance is $R_{SD} = 10 (L/W) \text{ M}\Omega$. A TFT that delivers $I_{ON} = 5 \mu\text{A}$ will need $W/\lambda = 5$. The area of each TFT will be $4000 \mu\text{m}^2$ (Fig. 5.2), and the packing density will be $25\,000$ transistors per cm^2 .

Note that this packing density of a-Si TFTs is less than $1/1\,000$ that of IC MOSFETs, and that the speed of a printed a-Si:H TFT will be $1/10\,000$ the MOSFET speed. Obviously, printed TFTs will not make sense as competitors of IC MOSFETs. But at a packing density of $25\,000 \text{ cm}^{-2}$, printed TFTs will be acceptable for many applications that need large area, or integrated packaging. Building-sized displays may require only a few TFTs per square centimeter, and a printed-TFT smart card with a surface of $\approx 50 \text{ cm}^2$ will hold as many as 10^6 printed TFTs on one level.

The physical limits of the resolution λ and the overlay registration $\pm\delta$ depend on the tools and materials that are used for printing. First, the ink must have sufficiently fine grain. This condition is easy to meet in principle by using molecule-based inks (solutions) or inks containing fine particles like polystyrene latex, which is available commercially in sizes down to $\approx 10 \text{ nm}$. Second, the tools for printing and alignment must have sufficient resolution. When light is used for both printing (as in electrophotography) and alignment, the physical limits for both λ and $\pm\delta$ are $\leq 1 \mu\text{m}$. Thus, in principle, both ink and tools can easily meet our requirements of 10 and $\pm 5 \mu\text{m}$, respectively.

Commercial printing is carried out in two steps. In the pre-press step, text or image is transferred to a printing plate. In a second step this plate is used to do the printing [5.7]. The resolution of plate-making and printing techniques can be as high as $2\,000\text{--}4\,000 \text{ spi}$ ($12.7\text{--}6.4 \mu\text{m}$). By using either three-point mechanical or optical alignment the overlay registration can be brought to $\pm 5 \mu\text{m}$ [5.9]. Thus the know-how and the components for the printing of active electronics at useful resolution and registration do exist.

The ratio of resolution to registration accuracy appears to be the same at all scales ranging from microelectronics to large-scale printing [5.10]. The IC resolution is $\approx 0.25 \mu\text{m}$ and the overlay tolerance $\leq 0.1 \mu\text{m}$. High-speed gravure presses print a linewidth of $\approx 150 \mu\text{m}$ with a registration of $\approx 50 \mu\text{m}$. The printing speeds are very different, though. While a modern IC plant produces approximately $10\,000 \text{ m}^2$ of ICs per year, a modern gravure press prints on this surface in about 5 min . Indeed the speed of today's printing presses is so high that large-area electronics may first be printed on plate-making equipment rather than printing presses. Note that a ratio of $\lambda/\delta = 3$ is easily compatible with the assumptions we used in calculating the packing density of printed TFTs.

The physical limits of several printing techniques are considerably finer than the resolution and registration of conventional printing equipment. Laser writing can produce a resolution of the order of $1 \mu\text{m}$. Nanoimprinting has demonstrated a resolution in the tens of nanometer range [5.11]. Therefore, the density of directly printed devices can be raised orders of magnitude above

$\approx 10\,000$ per square centimeter. We can anticipate continuous improvements of resolution and registration once a direct-printing industry for electronics has come into existence.

5.3 Printed Toner Masks for Etching and Liftoff

The fabrication of integrated circuits alternates between deposition or modification of a layer of material and the patterning of this layer. The established patterning process is photolithography, which typically consists of the nine steps shown in Fig. 5.1. The patterned photoresist serves as the etch mask for the active material that it covers. This step is shown as wet etching or dry etching in Fig. 5.1. Patterned photoresist also can serve for patterning overlying active material in a process called Liftoff. Both processes can be shortened by three steps if the etch or liftoff masks are printed directly. A typical patterning sequence using a printed mask is shown on the right-hand side of Fig. 5.1. We now describe two practical processes that use laser-printed toner as masks for etch and liftoff. The first process relies on a combination of mask printing and of toner transfer via an auxiliary paper substrate. The second exclusively uses masks that are printed directly on the substrate. The mask material is xerographic toner, which is applied with a 600 dpi laser printer. The two processes represent chronological developments and are not necessarily tied to either glass or steel substrates.

5.3.1 Toner Masks via Paper Transfer: TFTs on Glass Foil

TFTs from a-Si:H have been fabricated on 50 μm thick alkali-free glass foil (Schott AF45), with the glass foil providing the flexibility required by an office-type laser printer. The bottom-gate, back-channel-etch TFTs need four mask levels, or patterning steps. These steps include direct laser printing of the first mask [5.6] and toner transfer for the higher levels. The channel length L and width W of the TFTs are 100 μm and 500 μm , respectively. The gate electrode is 300 μm long. The complete TFT process is shown in Fig. 5.3 [5.5]. The first step is to run the glass foil through the laser printer to print a negative toner gate mask. Then an $\approx 100\text{ nm}$ thick Cr layer is thermally evaporated and the Cr-on-toner is lifted off in toluene. The silicon stack is deposited in a three-chamber plasma-enhanced chemical vapor deposition system: $\approx 410\text{ nm}$ of SiN_x , $\approx 160\text{ nm}$ of undoped a-Si:H and $\approx 50\text{ nm}$ of (n^+) a-Si:H. An $\approx 100\text{ nm}$ thick Cr layer for source/drain contacts is thermally evaporated. Then a positive source/drain pattern is printed using transfer paper [5.12, 14]. The Cr layer is wet etched, the (n^+) a-Si:H layer dry etched in CF_4 , and the toner is removed. Next, a positive toner mask is printed to define the TFT island, again using transfer paper. The undoped a-Si:H layer is dry etched in CF_4 . Without stripping the island mask, the final toner mask for opening the gate electrode pad is printed, again using transfer paper. The

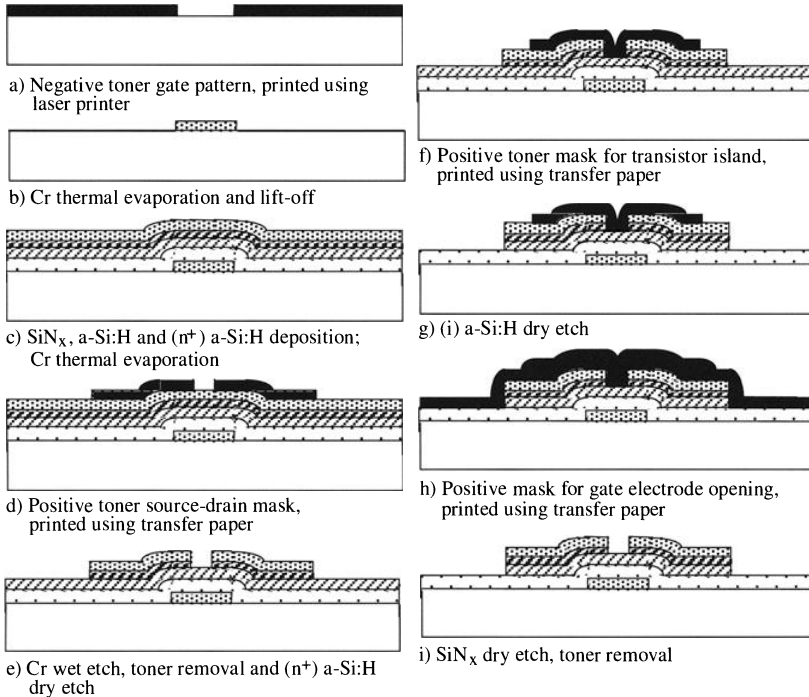
Cross-section through the transistor island

Fig. 5.3a–i. Process for making TFTs using toner masks. Steps (a) and (b) show lift-off. The other toner steps are etch masks applied by using transfer paper. Function and composition of the layers is evident from the captions (from [5.5])

SiN_x is dry etched in CF_4 and the toner is removed. Finally the TFTs are annealed in forming gas at 200°C to anneal out the radiation damage caused by the plasma during dry etching.

The photograph of a TFT made by this process, and the transfer characteristics of this transistor are shown in Fig. 5.4 [5.5]. These characteristics are identical to those of TFTs made on glass plate substrates by conventional photolithography. The channel of this transistor lies at the bottom center of the photograph, which is dominated by the contact pads, which were made large to ease the probing of curved substrates.

The size distribution of toner particles for commercial laser printers is centered at $7\text{--}10\text{ }\mu\text{m}$ [5.15]. This large particle size produces irregular edges, as can be seen in Fig. 5.5a [5.16]. The toner particles also spread into open areas, and they do not coat the printed areas perfectly. This irregularity is a consequence of the mutual repulsion of toner particles, of variations in the surface charge density of the toner particles, and of the attenuation by the glass substrate of the electric field gradient that directs the toner particles.

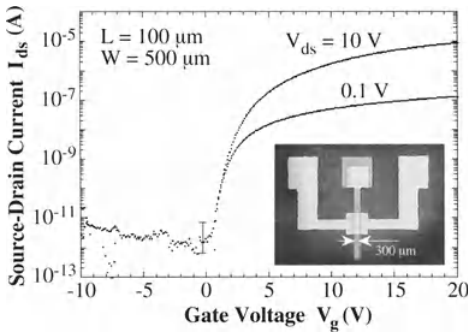


Fig. 5.4. Transfer characteristics of an a-Si:H TFT made by the process of Fig. 5.3 on glass foil. The inset is a photograph of the TFT structure. Source, gate, and drain contact pads lie near the upper edge of the photograph. The 100 μm long channel lies in the center of the TFT island, which is close to the lower edge. The gate electrode is 300 μm wide (from [5.5])

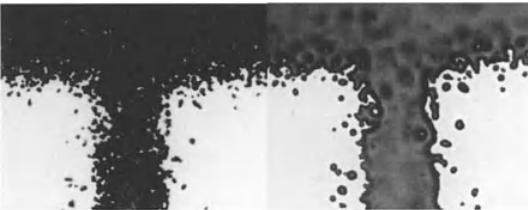


Fig. 5.5. An as-printed toner pattern before (*left*) and after (*right*) post-printer fusing. The vertical line is $\approx 100 \mu\text{m}$ wide ([5.16])

The laser printer has a fusing stage in which the toner particles are sintered to the substrate and to each other. The bulk of a typical toner particle is a polystyrene-based copolymer with a glass temperature near 100°C. During the fusing step in the printer the temperature may reach 170°C for a fraction of a second, but this treatment does not suffice to melt the toner particles completely. Printed areas therefore remain porous to etchants. A post-printer anneal for 1 h at 120°C melts the toner to the extent that it forms a contiguous, impermeable layer, and that small holes in the printed layer close. The pattern of Fig. 5.5b was fused at 160°C for 30 min. Figure 5.6 [5.17] shows surface profiler traces of a toner layer out of the laser printer, and after the post-printer anneal, respectively.

5.3.2 All Masks Printed Directly: TFTs on Steel Foil

If provisions are made for reproducible alignment of the substrate in the laser printer, all toner masks can be printed directly onto the substrate [5.18]. To do so, the substrate is aligned mechanically for each patterning step by

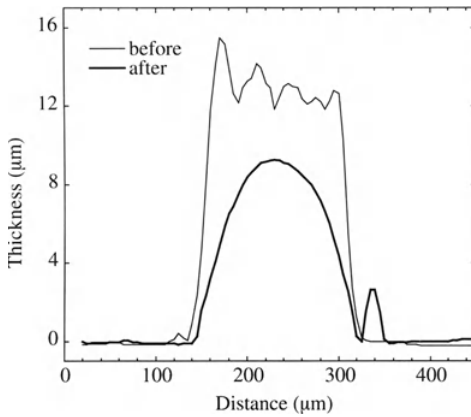


Fig. 5.6. Surface profiler traces across a toner line as produced by the printer, and after the post-print anneal. Note the reduction in cross section caused by compaction of the toner (from [5.17])

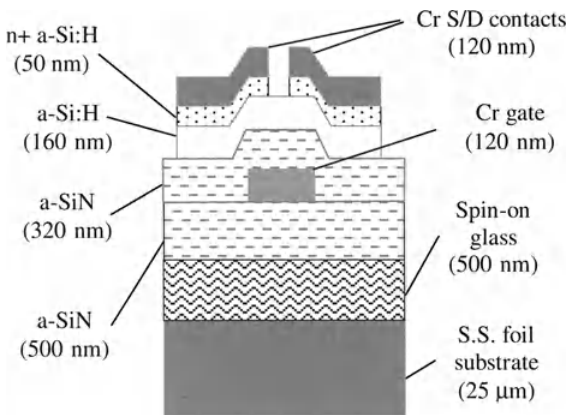


Fig. 5.7. Cross-section of a TFT on steel foil, showing materials and typical layer thicknesses (from [5.18])

matching registration marks between the substrate and a rigid carrier. The carrier is fed into the laser printer and is aligned in the printer just like a sheet of paper. The schematic cross section of a TFT on steel foil is shown in Fig. 5.7 [5.18]. The performance of TFTs made by printing all toner masks directly is comparable to that of TFTs made on similar steel foil but using photolithography, as is evident from Fig. 5.8 [5.18].

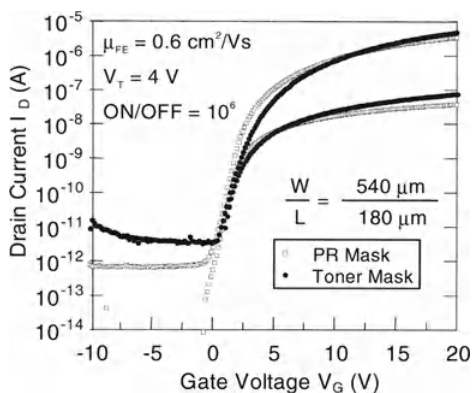


Fig. 5.8. Transfer characteristics of two TFTs made on 25 μm thick steel foil. One TFT was made using conventional photolithography, the other by printing all mask layers directly in a laser printer (from [5.18])

5.4 Printing Active Materials: Jetting Doped Polymers for Organic Light Emitting Devices

Direct printing of active materials is expected to produce large-area electronics at very low cost. An early example of direct printing is the printing of the active polymers for organic light-emitting diodes [5.19]. One group of organic materials for OLEDs consists of polymer hosts that permit charge transport and are doped with color centers. The color centers are organic dyes that emit light upon electron-hole recombination. The choice of dopant dye determines the color of emitted light. In the case of organic device materials the direct printing provides a particular advantage: It is the first simple process for the patterning of monolithically integrated three-color OLEDs.

An ink-jet printer was used with a resolution of 640 dots per inch. The piezoelectric printhead squirts ink droplets from a nozzle with a 65 μm opening. Four ink cartridges and four nozzles enable the printer to print four different colors simultaneously. As the printer head scans the page and the piezoelectric materials are pulsed, ink is squirted from the nozzles onto the page. The only modification to the ink-jet printer for printing OLEDs was to replace the original inks in the cartridges with polymer solutions.

The hole-transport polymer poly(N-vinylcarbazole) (PVK), and one of the fluorescent dyes coumarin 6 (C6) for green, coumarin 47 (C47) for blue, and Nile red were dissolved into chloroform solution, which was then deposited by jetting, or by spin coating for comparison. No electron transport material was used in this initial work. After deposition the chloroform evaporates leaving a doped polymer material. Typical concentrations of PVK dissolved in chloroform were 10 g/l, and dye dissolved in chloroform were 0.1 g/l, yielding on the order of 1% dye in the PVK. Chloroform solutions containing varying

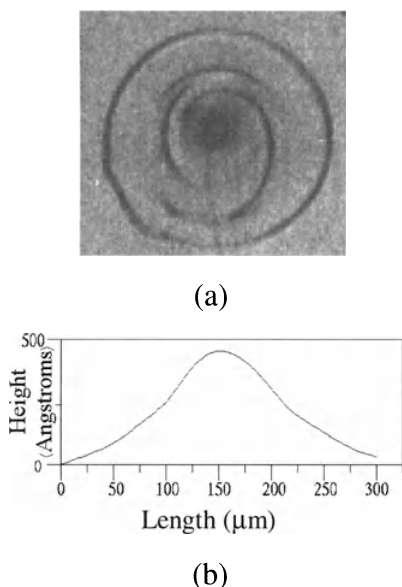


Fig. 5.9. (a) Photograph of a jet-printed dot; (b) surface profile of a jet-printed dot 300 μm wide (from [5.19])

amounts of PVK and luminescent materials were prepared by stirring and were passed through 0.45 μm filters. Thin films were jetted onto 175 μm thick flexible polyester coated with indium tin oxide (ITO). Before deposition, the ITO was treated with an oxygen plasma to modify its surface properties for making ohmic contact to the OLEDs.

The optical micrograph of a jet-printed dot and a surface profile of the shape of a typical dot are shown in Fig. 5.9 [5.19]. The thickness of the dots ranged from 40 to 70 nm and the dot widths ranged from 150 to 300 μm . The larger-diameter dots tended to be thicker, indicating that the thickness variation is due to the total amount of deposited solution. One can see some structure within the dot, which may be evidence of mass transport due to segregation as the solvent evaporated. To demonstrate the ability of the jet-printing technique to deposit patterns, PVK doped with C6 or Nile red was deposited in a jet-printed test pattern. This sample was then illuminated using ultraviolet light, which excited green (or red) emission from the patterned polymer.

Figure 5.10 shows the photoluminescence spectra of three individual jet-printed thin films and of spin-coated films made from the same solution, each with a different dye [5.19]. The photoluminescence was measured with an excitation wavelength of 380 nm for the C47 doped film and 440 and 520 nm for C6 and Nile red doped films, respectively. No significant difference in shape or magnitude is seen between the films prepared by jet-printing vs.

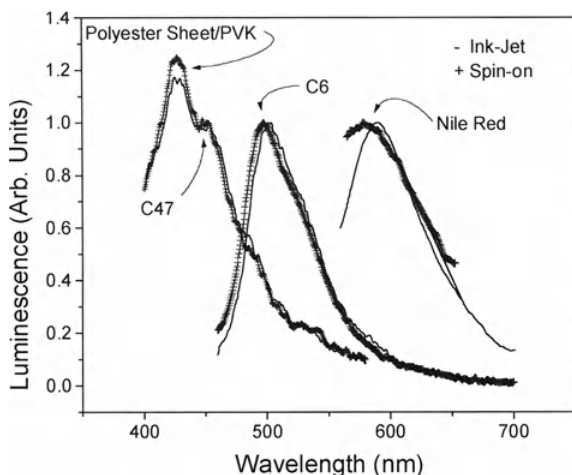


Fig. 5.10. Photoluminescence spectra of PVK doped with coumarin 47, coumarin 6, or Nile red. The spectra of jet-printed and spin-coated films are shown for each band. The luminescence spectra are identical for the two techniques of application (from [5.19])

spin coating. It should be noted that the peak of 420 nm in the C47 spectra is due to a combination of the polyester substrate and the PVK host, not the deposited film. The dye luminescence appears as a peak at 450 nm on the shoulder of the 420 nm peak.

It is difficult to fabricate devices directly on top of the polymer dots made by jet-printing because of the difficulty in aligning a shadow mask for metal cathode formation directly over a polymer dot. Therefore, to fabricate test devices the ink-jet printer was operated in a mode to create a continuous film of polymer rather than discrete dots. After jet-printing, the samples were loaded into a vacuum chamber with a base pressure of $< 10^{-7}$ torr for the metallization step of device fabrication. Typically, at least ≈ 90 min were allowed between loading of samples and metal evaporation, and no further heating of samples was done. Top metal cathodes were deposited through a shadow mask to form an array of $250\text{ }\mu\text{m}$ diameter devices on the polymer film. Metal alloys such as Mg:Ag (10:1) were deposited by co-evaporation from two separate sources, followed by the deposition of Ag as a protective layer. The ITO on the polyester sheet served as the anode. The devices were then measured in air without any protective coating.

Figure 5.11 shows the I - V curves of typical devices made by this procedure and a control device fabricated on a film spin-coated from the same polymer solution [5.19]. The organic film thickness of the control device was about 50 nm. Current densities of $\approx 2\text{ mA cm}^{-2}$ are achieved at a voltage of $\approx 7\text{ V}$ for the control device, and ≈ 7 – 11 V for the jet printed devices. The

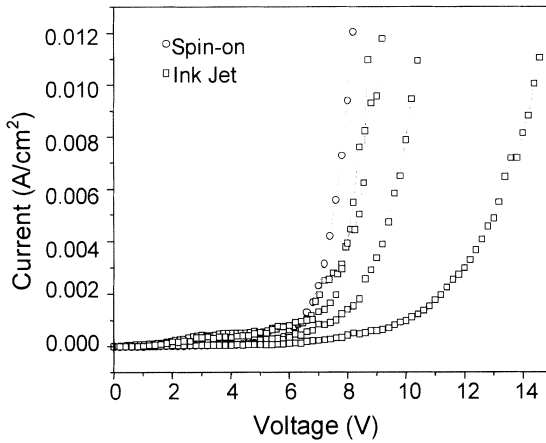


Fig. 5.11. Current-voltage characteristics for one spin-coated and four jetted OLEDs. The turn-on voltage of diodes made by jetting can come close to that of the spin-coated diode (from [5.19])

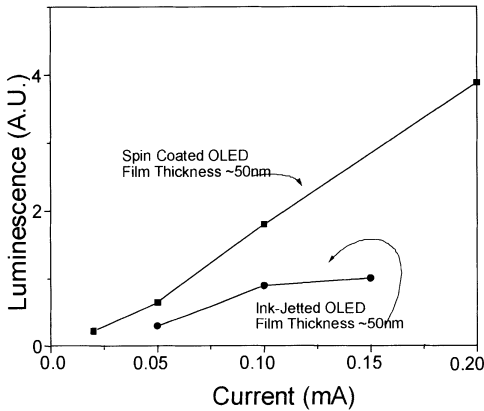


Fig. 5.12. Luminescence versus current characteristics of a spin-coated and a jetted OLED. The efficiency of the jetted OLED is lower than that of the more-developed spin-coated OLED (from [5.19])

luminescence versus current characteristics of the two OLEDs show that the efficiency of this early jet-printed device is about a factor of two lower than that of the spin coated device (Fig. 5.12 [5.19]).

A very promising modification of the approach described above is the local modification of a large-area spin-coated layer of host material by the jetting of solutions of the fluorescent-dye light-emitting dopants [5.20]. The jetted dye diffuses into the host (PVK) and forms the OLED material. This approach allows easy tuning of the UV fluorescence spectra of the film and

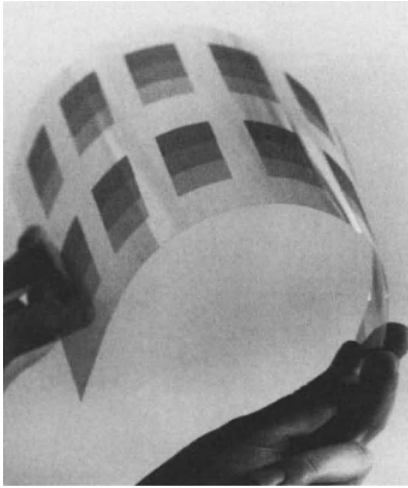


Fig. 5.13. Photograph of a page-size glass foil of $80\text{ }\mu\text{m}$ thickness printed with a transistor pattern of toner (from [5.6])

the spectra of the OLEDs made from the film, while retaining the planarity and film thickness advantages of spin-coating.

5.5 Substrates and Encapsulation for Macroelectronic Circuits

Substrates and encapsulation function as the mechanical support and protection of the thin film circuits. For use in AM-LCDs both must be transparent, while in an OLED display only the encapsulation may need to be transparent. The choice of substrate materials broadens considerably when the process temperature is reduced to below 200°C , and then ranges from the conventional silicate glasses over metals to organic polymers. A concurrent trend to thinner substrates and encapsulation seeks to reduce weight, and for very thin substrates, to increase flexibility and ruggedness. Tables 5.2 and 5.3 list properties of twelve materials that may be used as substrates or encapsulants. Note that the melting, strain or glass temperature, the thermal conductivity, and the coefficient of thermal expansion do vary widely between the materials of the table.

Glass substrates for active TFT circuits are best known and characterized [5.21]. One of the main advantages of borosilicate glasses is that their coefficients of thermal expansion are similar to those of the silicon TFT materials. Glass foil substrates that can be fed through printers with curved paper paths are available with thickness down to $50\text{ }\mu\text{m}$ from DESAG, a Schott subsidiary. The DESAG glass foil is made of borosilicate. This glass needs no

Table 5.2. Optical and electrical properties of materials for substrates and encapsulation^a

Material	Brand name	Density (g cm ⁻³)	Appearance and range of optical transparency (μm)	Refract. index at 0.55–0.6 μm	Dielectric constant at 0.1–1 MHz
Cryst. silicon		2.33	Opaque	3.4	11.8
Soda lime glass	Corning 0211	2.53	Clear 0.4–2.2	1.52	6.7
Borosilicate glass	Corning 7059 Schott AF 45	2.76	Clear 0.35–> 2.5	1.53	5.9
Borosilicate glass	Corning 1737	2.54			
Invar		8.0	Opaque		
Stainless steel	AISI 304	7.93	Opaque		
Aluminum		2.70	Opaque		
Perfluorocyclobutane aromatic ether polymer	DowXU-35033.00		Milky white <0.4–>0.6	1.50	2.45
Polyimide	DuPont Kapton E	1.46	Amber		3.4 50% RH
Polyethersulfone		1.37	Pale amber	1.65	3.7
Polyarylate	Kaneka F-1100	1.20	Clear	1.60	2.7
Polycarbonate	Lexan	1.2	Clear	1.58	2.9

^a For references and comments see footnotes to Table 5.3

further passivation prior to a standard a-Si:H TFT process. Foils of soda lime glass with thickness down to 50 μm are available from Corning, or down to 30 μm from DESAG. Soda lime glass must be passivated with a deposited SiO₂ or SiN_x barrier to prevent Na diffusion. Fusing or HF-etching the edges reduces breakage, because cracks propagate easily from the saw-damaged edges. When supported uniformly, glass foil is surprisingly resistant against impact by blunt objects, but it does shatter upon impact of sharp objects. The Corning glass foils tend to have a wavy surface that gives it anisotropic flexibility but does not affect the a-Si:H fabrication and laser printing. The flexibility of an 80 μm thick page-size glass foil is demonstrated in Fig. 5.13, which shows a laser-printed toner pattern [5.6]. A transistor made on 50 μm

Table 5.3. Mechanical and thermal properties of materials for substrates and encapsulation

Material (same brands as in Table 5.2)	Young's modulus Y (GPa)	T_{melt} , T_{strain} , or T_{glass} ($^{\circ}\text{C}$)	Coefficient of thermal expansion at 20°C (10^{-6}K^{-1})	Thermal conductivity ($\text{Wm}^{-1}\text{K}^{-1}$)	(Primary lit. references) Comments Chemical composition
Cryst. Silicon	190	$1415 T_{\text{m}}$	2.4	165	^(a,b) For comparison.
Soda lime glass	74	$508 T_{\text{s}}$	7.4 at 300°C	0.12	^(c) KNaZn borosilicate T_{strain} at 10^{14} Poise
Borosilicate glass	68	$593 T_{\text{s}}$	4.7	≈ 1	^(d,e) BaAl borosilicate T_{strain} at $10^{14.6}$ P Shrinks 10^{-4} at 450°C 8 h
Borosilicate glass		$670 T_{\text{s}}$	3.7	≈ 1	^(f) Shrinks 3×10^{-4} at 450°C 8 h
Invar	140	$1430 T_{\text{m}}$	1.2	13	^(g) 64 Fe, 36 Ni (wt.%)
Stainless steel	190	$\approx 1400 T_{\text{m}}$	18	16	^(g) 18 Cr, 10 Ni (wt.%)
Aluminum	70	$660 T_{\text{m}}$	24	237	^(g) Y for hard Al
Perfluorocyclo- butane aromatic ether polymer	2.3	$400 T_{\text{g}}$	90		^(h) Experimental grade. Contains 0.021wt.% water. Wt. loss 0.4%/h air 350°C
Polyimide	5.2	$\geq 250 T_{\text{g}}$ (est.)	12 50- 200°C	≥ 0.1	^(i,g) CHE $9.10^{-6}/\%\text{RH}$. Shrinks 0.3×10^{-3} at 200°C
Polyether-sulfone	2.4	$200 T_{\text{g}}$	55	0.15	^(g)
Polyarylate	≥ 2 (est.)	$215 T_{\text{g}}$	51		^(j) Shrinks 2×10^{-3} at 180°C 3 h
Polycarbonate	2.3	$160 T_{\text{g}}$	70	0.2	^(g,k) Degasses > 160°C

^a Bell Labs Quick Reference Manual (May 1975).^b AIP Handbook, McGraw Hill, New York (1972).^c Corning Product Information PI-0211-87.^d N.P. Bansal, R.H. Doremus, Handbook of Glass Properties. Academic (1986).^e Schott/DESAG spec. sheet AF 45 and D 263.^f D.M. Moffatt, Mat. Res. Soc. Symp. Proc. **377** (1995).^g Goodfellow Catalog (1996/97).^h D. Perettie, L. Bratton, J. Bremmer, D. Babb, Liq. Cryst. Mater., Devices and Applications II, SPIE **1911** 15 (1993).ⁱ J.A. Kreuz, S.N. Milligan, R.F. Sutton: DuPont Films Technical Paper 3/94, Reorder No. H-54504 Properties, Academic (1986).^j Kaneka spec. sheet.^k S.M. Gates: Mat. Res. Symp. Proc. **467**, 843 (1997)

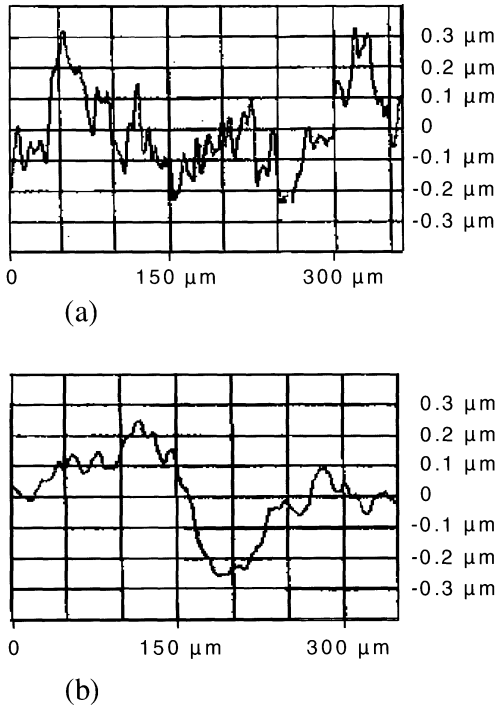


Fig. 5.14a,b. Surface profiles of a steel foil (a) as received and (b) after planarization with spin-on-glass. SOG removes the short-wavelength roughness that reduces transistor yield. The full vertical scales measures $0.8\text{ }\mu\text{m}$, and the traces are $400\text{ }\mu\text{m}$ wide (from [5.24])

thick Schott AF45 glass foil and its transfer characteristics are shown in Fig. 5.4 [5.5].

Stainless steel foil with thickness between nominally 125 and $200\text{ }\mu\text{m}$ (5 and 8 mils) has been used for many years as the substrate for amorphous silicon solar cells made in a roll-to-roll process [5.3]. It is also possible to make TFTs on steel foil [5.22], even with less than $10\text{ }\mu\text{m}$ thickness [5.23]. At low thickness the handling of the foil – if processed in free-standing form – dominates TFT fabrication. Steel foil must be coated with an insulator prior to TFT fabrication. A convenient insulator is the silicon nitride that is used as the a-Si:H TFT gate dielectric. Steel foils are made with a wide variation of surface finish, which depends on the state of the rolling equipment. Some surface finish will give high transistor yield with just the SiN_x barrier layer alone. Other surfaces have short-wavelength roughness that needs planarization, which can be done by using the sol-technique of spin-on glass (SOG) [5.24]. The most viscous spin-on-glass precursor results in $\approx 500\text{ nm}$ thick oxide layers. A surface profile of an as-received $75\text{ }\mu\text{m}$ thick AISI 304 stain-

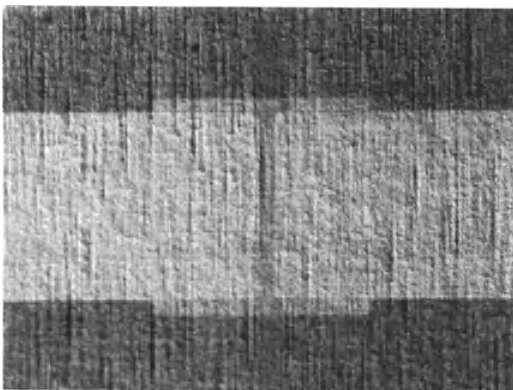


Fig. 5.15. Photograph of a working TFT made on non-planarized $15\text{ }\mu\text{m}$ thick steel foil. The surface finish of the as-received foil was adequate for high TFT yield. Source and drain contacts lie to the left and right of the channel at the center of the TFT island. The channel is $48\text{ }\mu\text{m}$ long (from [5.23])

less steel foil is shown in Fig. 5.14a [5.24]. The TFT yield on this substrate was $\approx 50\%$. Figure 5.14b illustrates the effect of SOG planarization, which suppresses the short-wavelength asperities [5.24]. The TFT yield on this substrate approaches 100%. Figure 5.15, which is a photograph of a functioning TFT on a $15\text{ }\mu\text{m}$ stainless steel foil, illustrates the ruggedness of a-Si:H TFT technology [5.23]. The gap L between the source/drain electrodes on this photograph is $48\text{ }\mu\text{m}$. Despite its rough appearance, the surface of this foil was sufficiently smooth on a microscale that it needed no SOG planarizing layer.

Foil substrates lend themselves to roll-to-roll fabrication and curved process paths. They also provide flexibility and ruggedness during use. Figure 5.16 illustrates the flexibility of TFTs fabricated on a $25\text{ }\mu\text{m}$ thick stainless steel foil [5.25]. The transistors were tested after successive bending to decreasing radii of curvature. They failed by delamination of the spin-on glass from the steel under concave (facing in) bending to 2.5 mm radius, and under convex (facing out) bending to 1.5 mm radius.

This result can be understood using a first-order analysis of the strain of a continuous thin film of TFT material deposited on a steel foil. Film and substrate have nearly identical Young's moduli of $\approx 200\text{ GPa}$ (Table 5.3). The bending is dominated by the substrate, which is much thicker than the $\approx 1\text{ }\mu\text{m}$ thick transistor film. Bending the film/foil couple, if free of strain when flat, to a cylinder as shown in Fig. 5.17 induces a strain ε in the surface [5.18].

For a film thickness d_{film} much smaller than the substrate thickness $d_{\text{substrate}}$, the strain-free neutral plane lies in the center of the foil,

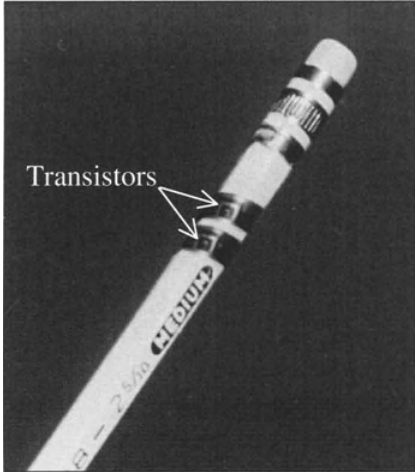


Fig. 5.16. The TFT characteristics are not affected by wrapping the TFT-on-foil around a pencil. The steel foil substrate is 25 μm thick. Note the TFT islands (from [5.25])

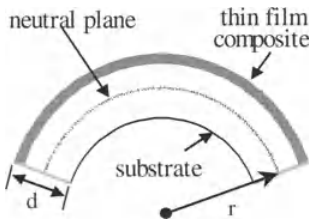


Fig. 5.17. The principal parameters of a film/substrate couple bent into cylindrical shape. The neutral plane is free of strain (from [5.18])

$\approx d_{\text{substrate}}/2$ away from the film [5.18]. The strain ε in the film induced at the bending radius r is given by:

$$\varepsilon \cong d_{\text{substrate}}/2r . \quad (5.2)$$

Assuming that the transistors fail when a certain level of strain ε_{max} is reached, it can be seen that the minimum allowable radius of bending r_{min} scales linearly with foil thickness $d_{\text{substrate}}$

$$r_{\text{min}} = d_{\text{substrate}}/2\varepsilon_{\text{max}} . \quad (5.3)$$

When the sample is held flat during film growth, it usually is under strain after fabrication, before intentional bending. Transistors grown on steel (Figs. 5.7, 5.15, 5.16) are under compressive strain as a result of differential thermal contraction between the steel ($\alpha_{\text{substrate}} = 18 \times 10^{-6} \text{ K}^{-1}$) and the silicon lay-

ers grown at $\approx 300^\circ\text{C}$ (α_{film} of a-Si:H $\cong 4 \times 10^{-6} \text{ K}^{-1}$ [5.26]). This contraction produces a mismatch strain ε_{M} , which is given by,

$$\varepsilon_{\text{M}} = (\alpha_{\text{film}} - \alpha_{\text{substrate}}) \Delta T, \quad (5.4)$$

where ΔT is the difference between the temperature of growth and room temperature. The stress in the film σ_{film} produced by the mismatch strain ε_{M} is given by,

$$\sigma_{\text{film}} = \varepsilon_{\text{M}} Y_{\text{film}}^*. \quad (5.5)$$

Here $Y_{\text{film}}^* = Y_{\text{film}}/(1 - \nu_{\text{film}})$ is the biaxial elastic modulus of the film, with Y_{film} being Young's modulus of the film and ν_{film} its Poisson ratio. This stress causes the substrate to bend to a radius of curvature R , which is given by the Stoney formula [5.27]

$$R = Y_{\text{substrate}}^* d_{\text{substrate}}^2 / 6 \sigma_{\text{film}} d_{\text{film}}. \quad (5.6)$$

When the in-plane stiffness of film and substrate becomes comparable, $Y_{\text{film}} d_{\text{film}} \approx Y_{\text{substrate}} d_{\text{substrate}}$, the substrate may deform considerably, which in turn reduces the stress in the film. Thus a substrate becomes compliant in two circumstances. In one, a high-modulus substrate material is made very thin (e.g., steel foils a few μm thick). In the other a low-modulus substrate material is chosen (typical plastic substrates have Young's moduli of $\approx 2 \text{ GPa}$, which is 1% of those of the TFT materials). When the film/substrate couple is held flat in a frame, the stress in the film is given by,

$$\sigma_{\text{film}} = \varepsilon_{\text{M}} Y_{\text{film}}^* / (1 + Y_{\text{film}}^* d_{\text{film}} / Y_{\text{substrate}}^* d_{\text{substrate}}). \quad (5.7)$$

It can be seen that for $Y_{\text{film}} d_{\text{film}} = Y_{\text{substrate}} d_{\text{substrate}}$ the stress produced in a device film deposited on a compliant substrate is reduced by a factor of 2 below that on a stiff substrate.

When a film is deposited on a compliant substrate that is held flat in a frame, and the structure then is released from the frame, the structure bends. A mismatch strain ε_{M} , which may include thermal and intrinsic components, produces a radius of curvature R that is given by [5.31],

$$R = \frac{(\overline{Y_{\text{substrate}} d_{\text{substrate}}^2} - \overline{Y_{\text{film}} d_{\text{film}}^2})^2}{6 \varepsilon_{\text{M}} (1 + \nu) \overline{Y_{\text{film}} Y_{\text{substrate}} d_{\text{film}} d_{\text{substrate}} (d_{\text{film}} + d_{\text{substrate}})} + 4(d_{\text{film}} + d_{\text{substrate}}) / 6 \varepsilon_{\text{M}} (1 + \nu)}. \quad (5.8)$$

Here we assume that $\nu = \nu_{\text{film}} = \nu_{\text{substrate}}$. The normalized radius of curvature as a function of the film/substrate thickness ratio $d_{\text{film}}/d_{\text{substrate}}$ is plotted in Fig. 5.18 for two different ratios of Young's moduli, $Y_{\text{film}}/Y_{\text{substrate}}$ [5.31]. A ratio of $Y_{\text{film}}/Y_{\text{substrate}} = 1$ corresponds to steel or glass substrates, and a ratio of 100 to plastic substrates. Note that for very small and very large $d_{\text{film}}/d_{\text{substrate}}$ ratios the substrate or the film dominate, and the radius of curvature R assumed by the structure after processing is large, reflecting

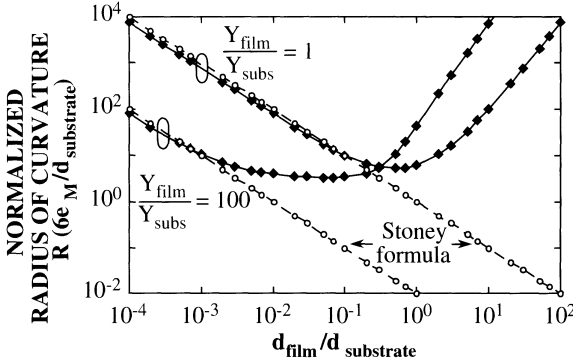


Fig. 5.18. When a film/substrate couple is released after deposition, it will assume a radius of curvature R that depends on the mismatch strain ε_M and on the elastic moduli of film and substrate. The Stoney equation is seen to be valid for $d_{\text{substrate}} \gg d_{\text{film}}$. Results of the complete theory are shown by diamonds (from [5.31])

a flat sample. The radius of curvature becomes smallest for thickness ratios near unity. Figure 5.18 also shows the results of the Stoney equation, which is seen to be a good approximation only if $d_{\text{substrate}} \gg d_{\text{film}}$.

We have seen that the stress induced in a film deposited on a compliant substrate can be reduced by a factor of 2 below that on a stiff substrate. Returning to our initial discussion of the bending of TFTs on steel foil, we now proceed to analyze the forced bending of a compliant substrate after a device film has been deposited on it. We shall see that this bending may induce much less strain in the film than on a stiff substrate. This consequence becomes qualitatively obvious from a re-inspection of Fig. 5.17. When the sheet is bent, the outside surface is in tension, and the inside surface is in compression. If the film/substrate foil has uniform elastic constants, the neutral plane coincides with the mid-plane of the sheet, as in Fig. 5.17. But if the structure consists of a stiff layer on top on a compliant substrate, the neutral plane is shifted from mid-plane toward the stiff layer. Consequently, for a given curvature R , the strain in the outside (film) surface is reduced, and is given by,

$$\varepsilon_{\text{top}} = \left(\frac{d_f + d_s}{2R} \right) \frac{(1 + 2\eta + \gamma\eta^2)}{(1 + \eta)(1 + \gamma\eta)}. \quad (5.9)$$

Here R is the radius of curvature, $\eta = d_f/d_s$ and $\gamma = Y_f/Y_s$. This situation is illustrated by Fig. 5.19, where the normalized strain in the film is plotted vs. film/substrate thickness ratio for the two ratios of Young's moduli of 1 (stiff substrate) and 100 (compliant substrate). Note that a compliant substrate can reduce the normalized strain by as much as a factor of five. In this way thin-film circuits on compliant substrates become particularly insensitive to bending. When favorable combinations of Y and d are used, the structure

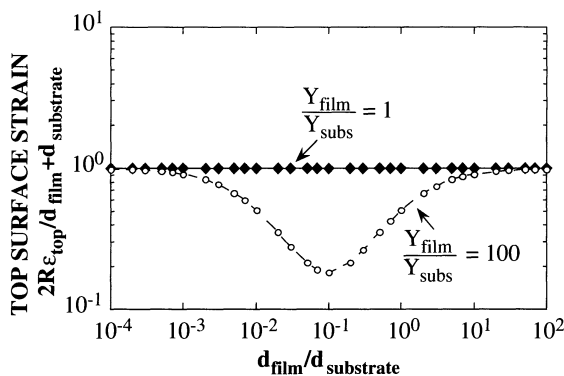


Fig. 5.19. In-plane strain ε_{top} induced in the top surface by bending an initially flat and strain-free film/substrate couple. The strain ε_{top} is reciprocal to the radius of curvature R . For a given value of R , choosing a compliant substrate and the appropriate film/substrate thickness ratio can reduce the strain by a factor of up to five

may allow extremely small radii of curvature. It even might be folded like a map.

It is noted above that TFTs made on steel foil peel off at a radius of curvature that is smaller for convex than for concave bending. This behavior is a consequence of the way the thermal strain ε_M and the strain induced by bending ε_{top} add [5.18]. For our sample this strain ε_M is $\approx 4.5 \times 10^{-3}$. (We assume that the sample is free of any intrinsic strain that often is established during growth.) Bending to a 1.5 mm radius adds a strain of $\pm 8.5 \times 10^{-3}$. The sum of bending and thermal strain in the convex (facing out) surface is $+4.5 \times 10^{-3}$, and on the concave (facing in) surface -13×10^{-3} . (We define tensile strain as positive, and compressive strain as negative). It is easy to see why the film peels off the concave surface at a larger radius than from the convex surface. Note that the peeling occurs at the large strain of close to 0.5%.

5.6 Plastic Substrate Foil: TFT on Polyimide

Thin film transistors made on thin foils of plastic serve as a good illustration of the compliant-substrate situation discussed in the preceding section. The glass transition temperatures of most organic polymers lie below 200°C, much lower than those of inorganic glass substrates (Tables 5.2 and 5.3). Therefore, the standard a-Si:H TFT processes cannot be used on plastics because they require temperatures of up to 350°C. We have fabricated a-Si:H TFTs on 51 μm (2 mil) thick polyimide foil after re-optimizing the TFT process for a maximum temperature of 150°C [5.28]. The commercially available polyimide grade Kapton[®] E was selected because it has a low coefficient of thermal

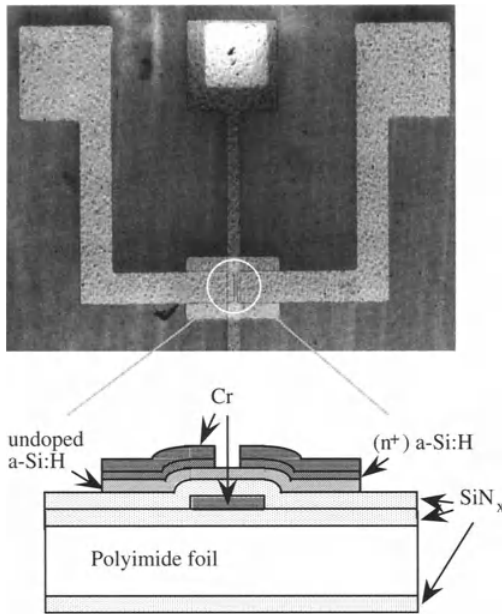


Fig. 5.20. *Top:* Top view of a TFT on a polyimide substrate. The channel is $15\ \mu\text{m}$ long. *Bottom:* Cross sectional view (from [5.28])

expansion of $12 \times 10^{-6}/^\circ\text{C}$, and its coefficient of humidity expansion is $9 \times 10^{-6}/\%$ Relative Humidity.

The transfer of such low-temperature technology from glass to plastic substrates brings new processing and mechanical issues to a-Si:H TFT fabrication. A widely usable low-temperature TFT needs to be compatible with a number of other polymers whose T_g is lower than that of Kapton. When a silicon thin film is grown on plastic foil, the contribution of the semiconductor to the mechanical behavior of the film/substrate couple becomes comparable to that of the plastic foil. This is very noticeable during processing, when the structure is observed to bend inward or outward with varying radii of curvature after each process step. We are entering a regime in which the film controls the mechanical properties of the structure as much as the substrate.

Before proceeding with a-Si:H TFT fabrication, the deposition of all layers was re-optimized for 150°C to obtain TFT electrical properties comparable to those obtained at higher temperature. The gate SiN_x was deposited from a mixture of Si:H_4 , NH_3 and H_2 , the undoped a-Si:H from a mixture of Si:H_4 and H_2 , and the $(n^+) \text{a-Si:H}$ from a mixture of Si:H_4 , PH_3 and H_2 . The TFTs have a bottom gate, back-channel etch structure. We began by passivating the polyimide substrate on both sides with a $0.5\ \mu\text{m}$ thick layer of SiN_x . These layers serve as a barrier against the solvents, bases and acids used during

photolithography. An ≈ 100 nm thick Cr layer was thermally evaporated and wet etched to create the gate electrode. Then we deposited a sequence of: ≈ 400 nm of SiN_x , ≈ 200 nm of undoped a-Si:H, and ≈ 50 nm of (n^+) a-Si:H. An ≈ 100 nm thick Cr layer was thermally evaporated. The Cr source-drain pattern was wet etched and the (n^+) a-Si:H was dry etched in CF_4 gas. Then the undoped a-Si:H was dry etched to define the transistor island. In the last photolithographic step, dry etched windows into the SiN_x were opened to access the gate contact pad. Arrays of six TFTs were fabricated on 1.5×1.5 in.² substrates. Four substrates were processed simultaneously. Figure 5.20 shows the cross section of one TFT [5.28].

The dependence of the source-drain current I_{ds} on the gate voltage V_{gs} for $V_{ds} = 0.1$ V and 10 V is shown in Fig. 5.21 [5.28]. The off-current is $\approx 1 \times 10^{-12}$ A ($< 1 \times 10^{-14}$ A/ μm gate width at $V_{DS} = 10$ V) and the on-off current ratio is 10^7 . At $V_{ds} = 0.1$ V we obtain $V_T \approx 3.5$ V. The dielectric constant of our 150°C nitride measured at 1 MHz is 7.46. The electron mobility in the linear regime is $\approx 0.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. These characteristics are comparable to those of a-Si:H TFTs fabricated on glass substrates at temperatures between 250 and 350°C. They suggest that a low-temperature a-Si:H technology can be developed that is fit for a large variety of plastic substrates.

5.7 3-D Integration on a Foil Substrate: OLED/TFT Pixel Elements on Steel

An active-matrix thin-film emissive display requires the integration of a light-emitting device with a switch. Organic light-emitting diodes can be integrated with amorphous silicon thin film transistors on steel foil, in a circuit that demonstrates the monolithic 3-D integration of very different thin-film devices on a foil substrate [5.24, 25, 29, 30]. While the devices were fabricated by conventional, non-printing techniques, the nature of the thin-film structure and the foil substrate suggests that large-area circuits based on such devices can be made by printing. A schematic cross-section of the integrated TFT/OLED structure on the steel foil is shown in Fig. 5.22a, and its equivalent circuit is shown in Fig. 5.22b [5.29]. The as-rolled stainless steel foil is planarized with 0.5 μm thick spin-on glass to remove the short-wavelength roughness of 0.3 μm rms. This planarization functions as primary insulation. Further insulation is provided by a 0.5 μm thick plasma-enhanced CVD SiN_x layer. The TFTs are made in the inverted-staggered, back-channel etch configuration with 120 nm thick Cr gates, 400 nm PECVD gate SiN_x dielectric, 150 nm a-Si:H channel layer, and 50 nm (n^+) a-Si contacts, followed by 120 nm Cr source/drain contacts. The channel length and width are 42 μm and 776 μm , respectively. The TFTs and contact pads are made large, to ease probing and diagnosis on bent or rolled substrates.

Following the fabrication of TFTs, OLEDs were made on the surface of the $2 \times 2 \text{ mm}^2$ Cr source/drain contact pads. Conventional OLEDs are built

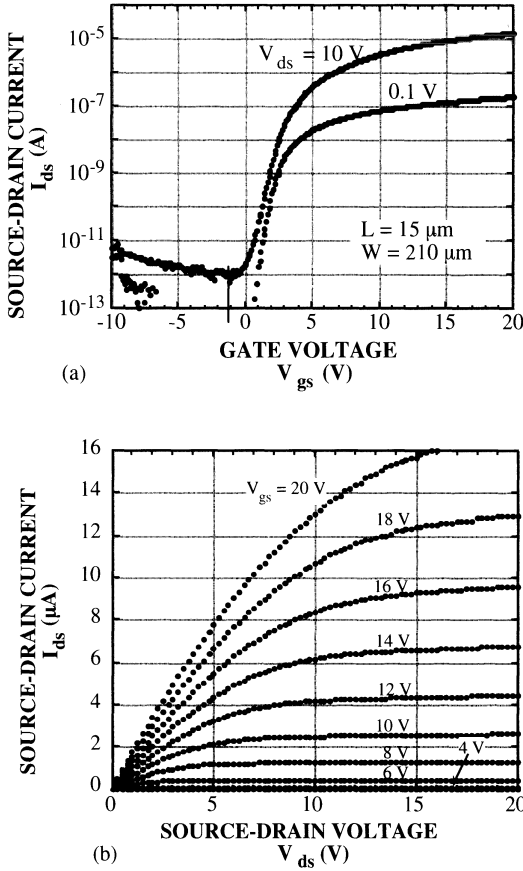


Fig. 5.21. (a) Transfer characteristics and (b) current-voltage characteristics of a TFT made at 150°C on a polyimide substrate (from [5.28])

on transparent substrates coated with a transparent hole-injecting anode contact such as indium tin oxide (ITO), so that light can be emitted through the substrate, because the top contact is an opaque electron-injecting metal cathode. Because of the opacity of the steel substrate, we developed the top-emitting structure in which the high work function metal Pt functions as the reflective bottom anode and a semi-transparent cathode is applied on top. OLEDs were fabricated by sequential electron-beam deposition and patterning of 40 nm Pt anode contacts, spin-coating of a continuous layer of 170 nm active luminescent molecularly doped polymer (MDP), followed by the electron beam evaporation of a 14 nm semi-transparent Ag top cathode. The overlap of the anode and cathode contact areas determines the active OLED device area, a $250 \mu\text{m}$ diameter dot, without the need to separately

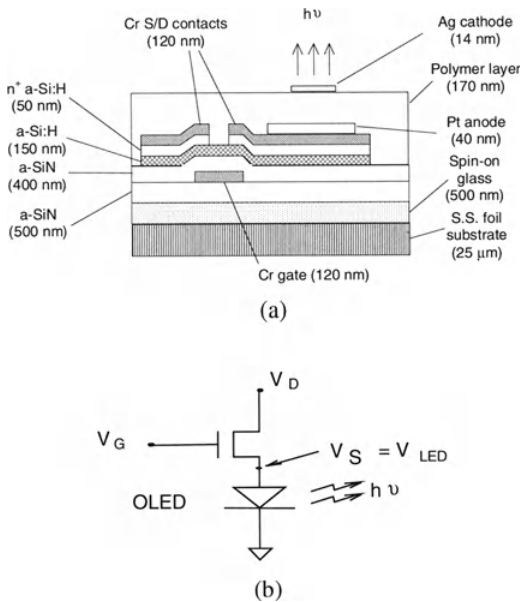


Fig. 5.22. (a) Cross section of the integrated OLED/TFT structure made on steel foil. (b) Equivalent circuit of the OLED/TFT (from [5.29])

isolate the organic layers. All OLED fabrication steps were performed at room temperature and are compatible with finished TFTs.

The active organic material used is a single-layer thin film. The hole-transport matrix polymer poly(N-vinylcarbazole) (PVK) contains dispersed electron-transport molecules of 2-(4-biphenyl)-5-(4-tert-butyl-phenyl)-1,3,4-oxadiazole and a small amount of the green fluorescent dye, coumarin 6 (C6), which provides efficient emission centers. The OLED luminescence depends linearly on device current as already shown for the spin-coated OLED of Fig. 5.12 [5.19]. The factor limiting the luminance in this device is not the polymer material itself, but rather the poor transparency of the top contact and its work function mismatch with the organic material. Here, we obtain 50 cd/m^2 at 40 mA/cm^2 ($20 \text{ }\mu\text{A/device}$) with $V_G = V_D = 40 \text{ V}$. Figure 5.23a shows the I - V characteristics of the integrated TFT/OLED device on a linear current scale [5.25]. Figures 5.23b,c illustrate how the voltage is applied to obtain the OLED and TFT/OLED curves, respectively. The shift in turn-on voltage results from the additional 3.5 V required to turn on the TFT. This functional OLED/TFT pixel circuit illustrates the ease of integrating very different materials into a 3-D thin-film configuration that could be fabricated by printing.

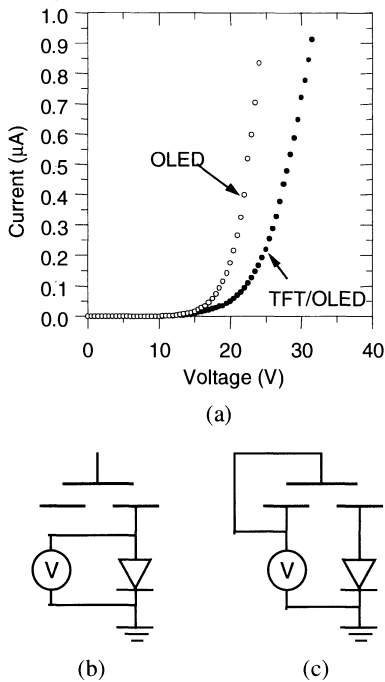


Fig. 5.23. (a) Current-voltage characteristics of the OLED and of the OLED/TFT; (b) and (c) show the circuits used for these measurements (from [5.25])

5.8 Outlook

We saw in this chapter that laser and jet printing techniques can be used to pattern thin-film transistors and organic light-emitting diodes. The resolution and registration achievable by conventional printing techniques will provide a packing density of more than 10 000 transistors per square centimeter. These transistors can be made on glass, steel, and plastic foils. The OLED/TFT structure suggests that they can be integrated into three-dimensional thin-film circuits. Direct printing will enable the manufacture of such circuits with very large-area. We also saw that these circuits are very rugged by virtue of the mechanics of thin structures.

The direct printing of macroelectronic circuits is receiving growing and worldwide attention. This newly found focus will facilitate the marriage of electronics and printing that is needed to develop the manufacturing technology for macroelectronics. An important ingredient is the development of printable materials for active circuits, which will draw on chemistry, materials science, and surface physics.

Early applications can be expected to make use of existing printing technology to make large-area circuits for displays, sensor arrays, and large-area

micro-electromechanical circuits. The pattern of increased resolution and enhanced performance that is well known from the development of silicon integrated circuits will be repeated in large-area electronics as more and more macroelectronic products are introduced.

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- 5.9 We thank the researchers of Dai-Nippon and Toppan for discussions of alignment techniques.
- 5.10 A point made by Mr. Russell Fling of R.R. Donnelley.
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