

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.
Petitioner,

v.

PICTIVA DISPLAYS INTERNATIONAL LTD.,
Patent Owner.

Case No. IPR2024-01187
Patent No. 9,257,492

DECLARATION OF P. MORGAN PATTISON, Ph.D.

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1. I, P. Morgan Pattison, Ph.D., declare as follows:

I. INTRODUCTION

2. I have been retained as an independent expert on behalf of Pictiva Displays International Ltd. (Patent Owner or Pictiva) to provide technical background and opinions related to U.S. Patent No. 9,257,492 (EX1001) (the '492 Patent) at issue in IPR2024-01187, including to Petitioner Samsung Display Co., Ltd.'s (Petitioner or Samsung) positions regarding Grounds I, II, and III involving Claims 1-3, 5, 6, 8-11, and 16, as well as other matters addressed herein.

3. For this service, I am compensated for my time at my normal consulting rate. My compensation does not depend on the outcome of any matter or on any of the opinions provided below. I have no financial interest in this matter.

4. My testimony herein is based on my educational background, technical background, my years of experience in the field of designing and fabricating semiconductor optoelectronic devices, my years of experience managing R&D of optoelectronic devices, and my review of the materials cited herein.

II. QUALIFICATION AND EXPERIENCE

5. My curriculum vitae (CV) is attached hereto as Exhibit A and provides an accurate identification of my background and experience.

6. I have over 25 years of experience in the areas of light emitting diodes (LEDs), organic light emitting diodes (OLEDs), lighting, solid state lighting (SSL), displays, lasers, and optoelectronic materials and devices.

7. I attended the University of California, Santa Barbara, receiving my M.S. in Electrical Engineering, Electronics and Photonics in 2003 and my Ph.D. Materials Science, Electronic and Photonic Materials in 2006. I received my B.S. in Electrical Engineering, Electronic Devices and Materials from the University of California, San Diego, in 1996.

8. This coursework included significant classwork in both chemistry and electronic materials and devices as well as classwork and research on the fabrication and evaluation of passive devices and optoelectronic devices, such as light emitting diodes, which require understanding of both materials chemical properties as well as electronic and optical properties.

9. Presently, I am the President of Solid State Lighting Services, Inc. In that capacity, I am responsible for, among other things, providing technical, strategic, and market expertise in the areas of LEDs, OLEDs, lighting, SSL, displays, and optoelectronic materials and devices. I work on connecting optical device technical performance with application requirements for displays, general illumination, color discrimination applications (medical, retail), and various novel lighting applications enabled by SSL technology. Solid State Lighting Services

also provides services related to LED and lighting product failure and reliability evaluation. I founded Solid State Lighting Services in 2007, and I have worked at Solid State Lighting Services, Inc. for about 17 years.

10. From January 2006 through November 2007, I worked as a Project Manager at the U.S. Department of Energy (DOE). In that capacity, I was responsible for managing DOE funded research and development projects in SSL, including efficient LED and OLED-based lighting technologies. My duties included managing the solicitation and selection of R&D projects with the objective of saving energy. As part of the solicitation and selection process, I evaluated and identified priority areas of research necessary for advancement of SSL in terms of efficiency, lighting performance, and cost. In this capacity I identified priority R&D areas to achieve the maximum energy savings, I managed R&D funding solicitations, and I managed DOE funded R&D projects covering all aspects of LED and OLED lighting technology including, light emitting materials and devices (LEDs and OLEDs), power supplies, optics, integrated fixtures, lighting controls, and lighting applications.

11. From September 2000 through January 2006, I was a Graduate Student Researcher at University of California Santa Barbara (UCSB). I performed my Doctoral thesis research under Professor Shuji Nakamura (Nobel Prize in Physics 2014) on gallium-nitride (GaN) based micro-cavity light emitting diodes.

The research included: epitaxial structure design and growth by MOCVD, semiconductor process development and fabrication, materials characterization, and electro-optical device characterization. While at UCSB, I participated in additional areas of research, including research and development of UV LEDs, vertical cavity surface emitting lasers (VCSEL), and edge emitting laser diodes.

12. From November 1996 through May 2000, I worked as a Laser Test Engineer at Cymer Laser. I was responsible for testing and developing test methodology for production and prototype KrF and ArF excimer lasers used in deep UV photolithography for manufacturing of advanced semiconductor products. Testing included optical characterization and full system troubleshooting. I also developed new electrical and optical test methodologies to improve test cycle times, automated test procedures, and developed test documentation.

13. I am listed as an inventor on at least 11 issued patents, including multiple patents in the field of LED materials and device design, LED lighting product design, and home automation and controls for lighting.

14. I have authored numerous peer reviewed journal articles and publications on the topics of SSL technology and applications.

15. Since 2008, I have also authored annually updated R&D and technology and manufacturing roadmaps used by the DOE to guide federal lighting R&D efforts. I frequently give presentations and talks on the topic of LED and

OLED technology, SSL status and R&D opportunities, and application advancements enabled by LED technology.

III. LEGAL STANDARDS

16. I am not an attorney. I have relied on instructions from counsel as to the applicable legal standards to use in arriving at my opinions in this Declaration. I am relying only on instructions from Patent Owner's attorneys for these legal standards.

17. I understand that Samsung, as the Petitioner, has the burden of proving that the challenged claims of the '492 Patent are unpatentable by a preponderance of the evidence.

A. Claim Construction

18. I understand that claim terms in an IPR are given their ordinary and customary meaning as understood by one of ordinary skill in the art (POSITA) in view of the entire patent and the prosecution history pertaining to the patent. I understand claim terms are to be given the meaning they would have to a person having ordinary skill in the art at the time of the invention, taking into consideration the patent, its file history, and, secondarily, any applicable extrinsic evidence (*e.g.*, dictionary definitions). I understand that applicants sometimes provide special definitions for claim terms that differ from the meaning the term

might otherwise possess, also known as lexicography. I have applied these standards in this declaration.

B. Obviousness

19. I understand that a patent claim is invalid if it would have been obvious in view of the prior art. I further understand that obviousness is determined from the perspective of a POSITA at the time the invention was made.

20. Whether or not explicitly stated below, my analysis of the prior art is made as of the time the invention was made (priority date). For purposes of this *inter partes* review, I have assumed that the priority date for the '492 Patent is September 27, 2012. My analysis would not change if that date was August 20, 2013, or March 25, 2015.

21. I understand that a claim may be unpatentable as obvious if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time of the invention. I understand that obviousness can be based on a single prior art reference or a combination of prior art references.

22. I understand that a prior art reference must be viewed as a whole. I further understand that the following factors must be evaluated to determine whether the claimed subject matter is obvious: (1) the scope and content of the prior art; (2) the difference or differences, if any, between each claim of the patent

and the prior art; (3) the level of ordinary skill in the art at the time the patent was filed; (4) objective indicia of non-obviousness.

23. I understand certain objective indicia can be important evidence regarding whether a patent is obvious or nonobvious. Such indicia include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention as compared to the closest prior art; praise of the invention by the infringer or others in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeding contrary to the accepted wisdom of the prior art.

24. I have been informed and understand that the teachings of two or more references may be combined if such a combination would have been obvious to one having ordinary skill in the art. It is also my understanding that where there is a reason to modify or combine the prior art to achieve the claimed invention, there must also be a reasonable expectation of success in so doing to render the claimed invention obvious. I also understand that the references themselves need not provide a specific hint or suggestion of the alteration needed to arrive at the claimed invention; the analysis may include recourse to logic, judgment, and common sense available to a POSITA.

25. I understand that when the prior art “teaches away” from combining prior art references or certain known elements, discovery of a successful means of combining them is less likely to be obvious. A prior art reference may be said to “teach away” from a patent when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the patent or would be led in a direction divergent from the path that was taken by the patent.

26. I have been informed and understand that one of ordinary skill in the art has ordinary creativity and is not an automaton. I have been informed and understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

27. Finally, I understand that Patent Examiners at the U.S. Patent and Trademark Office (“USPTO”) rely upon certain exemplary rationales in review patent applications to understand whether the subject matter of the claims is obvious. I understand that the following is a list of exemplary rationales relied upon by Patent Examiners at the USPTO:

- A. Combining prior art elements according to known methods to yield predictable results;
- B. Simple substitution of one known element for another to obtain predictable results;

- C. Use of a known technique to improve similar devices (methods, or products) in the same way;
- D. Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- E. “Obvious to try”- Choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- F. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art; and
- G. Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

C. Level of Ordinary Skill in the Art

28. I understand that interpreting patent claims and validity must be undertaken from the perspective of a hypothetical POSITA. I understand that in determining the characteristics of a hypothetical person having ordinary skill in the art of the patent at the time of the claimed invention, I must consider several things, including the type of problems encountered in the art, the solutions to those

problems, the rapidity with which innovations are made, the sophistication of the technology, and the education level and experience of people working in the field.

29. I understand that Samsung and Dr. Kattamis define a POSITA at the time of the invention as someone with “a bachelor’s degree in Electrical Engineering, Physics, or a comparable field of study, and at least three years of research or industrial experience with semiconductor (organic or inorganic) optoelectronic devices and/or lighting or displays.” Pet. 9 (citing EX1003, ¶ 46). For the purposes of this Declaration, I have been instructed to apply Samsung’s proposed level of skill in the art.

30. I express no opinion on whether this level of ordinary skill is correct. Yet this level of ordinary skill in the art is somewhat low. Integration and fabrication of optoelectronic devices was (and is) a unique, cross-disciplinary field, requiring expertise in chemistry, materials science, electronic devices, and optics.

31. Samsung’s and Dr. Kattamis’s low level of ordinary skill would mean that a POSITA would not be motivated to or reasonable able to easily deviate from the express teachings in the prior art to extrapolate broader uses with a reasonable expectation of success.

32. Given my education and experience at the time, I was at least a person of ordinary skill in the art, if not one with above average skills, at the time of the invention.

D. Materials Relied on in Forming My Opinions

33. In forming my opinions expressed in this declaration, I have relied on my own knowledge, experience, and expertise, as well as the knowledge of a POSITA in the relevant timeframe. In addition, I have reviewed and relied upon the materials cited in this declaration.

IV. TECHNOLOGICAL BACKGROUND

34. The '492 Patent relates to forming electronic components on a substrate in layers applied using different techniques. EX1001, Abstract. The '492 patent describes “a method for producing a passive electronic component [e.g., a capacitor] and/or a method for producing an optoelectronic assembly [that may include, e.g., an OLED].” *See id.* at 1:41-46. The claimed invention include forming layers of electrically conductive and dielectric (insulating) materials on a substrate. Certain layers, including first and second electrically conductive layers, can be (but need not be) applied “in a planar fashion, that is to say without structure.” *Id.* at 11:2-4, 11:24-26. When applied in a planar fashion, layers can be subject to “subsequent structuring,” using techniques such as photolithography, etching, or laser ablation. *Id.* at 2:5-7, 4:5-9.

35. In addition to at least these first two layers applied to the substrate, “the dielectric and/or the electrode layer and/or subsequently further layers or materials are ‘applied in a structured fashion,’” which means “that the desired

structure is already formed during the application of the corresponding layer,” and the “area to be coated is thus coated only in partial regions dependent on the desired structure.” *Id.* at 1:66-2:4. These layers can form a passive electronic component, such as a capacitor. *See id.* at 8:22-24. They can also form an optoelectronic assembly, which may include, for example, a passive electronic component and one or more optoelectronic components. *See id.* at 8:29-31. Each claim of the ’492 Patent further requires applying an electrically conductive electrode layer in a structured fashion, including an electrode applied to the dielectric “above the first contact region” and also in contact with the second contact region, which may form an electronic component (e.g., a capacitor). *See id.* at 20:41-43 (claim 1), 21:28-31 (claim 10), 22:39-42 (claim 16).

36. As described in EX1022, manufacturing quality control of semiconductor processes is critical. EX1022, at pp.15-18. In particular with semiconductor processes, consistent alignment of the various device layers is particularly critical. The areal resolution and accuracy of various deposition, etching, doping processes must be closely considered within the context of the materials, device type, and size of the product that is being fabricated.

37. Semiconductor processes consist of both additive and subtractive manufacturing techniques. Layers of the semiconductor device can be deposited as continuous layers or as patterns defined by a mask or by some form of printing.

These would be additive manufacturing techniques. Layers of the semiconductor device can also be removed as entire layers or in a pattern, which would be a subtractive technique.

38. Patterning of additive layers can be achieved by mask or photolithographic deposition techniques. Patterning of layers can also be achieved by printing materials in their desired location which can be lower cost for larger areas but with reduced resolution and accuracy (EX1023). The choice of deposition process depends on cost, throughput, required resolution, and accuracy of the process necessary for the ultimate device.

39. Laser ablation can be used as a subtractive technique to remove material with high resolution in specific locations.

40. Optoelectronic semiconductor devices require integration of multiple layers including electrodes and the optically active layer(s). These layers need to be aligned to each other and to the substrate. As described in the '492 Patent, the optoelectronic devices can be integrated with additional components that are integrated with the substrate.

41. Organic LEDs (OLEDs) are a unique optoelectronic element often used for displays. OLEDs are unique in that they are formed from organic semiconductor materials which can be readily printed. For displays, OLEDs can require the formation of a pixel that has red, green, and blue sub-pixel individual

OLED devices. The sub-pixels will require different materials in order to emit the different colors. The alignment and resolution of these sub-pixels with respect to each other and over the larger display area is critical. Each OLED sub-pixel device requires multiple layers to achieve optimal electrical and optical performance.

42. I understand that Samsung has mapped certain claim limitations to the formation of capacitors allegedly disclosed in the prior art. *See, e.g.,* Pet. 27, 50.

43. I agree with Dr. Kattamis that a “capacitor is a passive electronic component that is comprised of two conductors separated by an insulator or dielectric material,” and that a capacitor may be “formed by depositing an insulator or dielectric material onto a conductive surface and then forming another conductive surface above the deposited insulator or dielectric.” EX1003, ¶¶ 76-77; *see also* EX1017 (Nilsson), at 221-22; EX1018 (Grebene), at 164-66.

44. However, EX1018 (referenced by Dr. Kattamis) describes different and idealized capacitor device structures than what is described in the '492 Patent and what is described by Dr. Kattamis's modified Fig. 1I. There are also differences between those descriptions and EX1017 (also referenced by Dr. Kattamis).

45. The '492 Patent describes the creation of conductor-dielectric-conductor (or metal-oxide-metal), which is not discussed in EX1018, which focuses on semiconductor based capacitors. The critical parameters for any

capacitor are the dielectric material, the area of the electrodes on either side of the dielectric material, and the distance between the electrodes. Capacitors are typically formed with a uniform distance between the electrodes across the dielectric to create a uniform electric field across the dielectric material. Uneven distances across the dielectric material will induce regions of high electric field which will result in more rapid breakdown of the dielectric and failure and short-circuiting of the capacitor. As discussed above in paragraph 36 and in EX1022, quality control and consistency are critical in the fabrication of semiconductor devices. As it relates to the creation of capacitors, differences in the distances between the electrodes will result in differences in the capacitance altering the circuit performance, can result in reduced breakdown voltages and reliability and lifetime of the capacitor, and can even result in short-circuits between the electrodes if the printing tolerances are inadequate for the required printing accuracy. These issues will be compounded for OLED display integration where millions of individual OLED devices will be fabricated over a large area and integrated with complicated underlying circuits with active and passive electronic elements.

V. OVERVIEW OF THE ALLEGED PRIOR ART

A. Ingle (EX1004 & EX1005)

46. Ingle discloses a method for producing an “electronic component,” which purportedly can be a capacitor, OLED, among other things. Ingle, 6:3-8. While Ingle shares similar disclosures to certain aspects of the ’492 Patent, a POSITA would understand several important distinctions between the disclosures of Ingle and the invention described and claimed in the ’492 Patent. For example, even assuming that Ingle references disclose the first and second electrically conductive layers, the trench, and the dielectric, Ingle does not disclose the actual production of those electronic components, such as the cathode required to form a capacitor or the cathode required (among other components) to form an OLED, much less the structured application of those layers. Petitioner admits that “Ingle leaves open how to finish forming a capacitor on its base structure, i.e., how to apply the cathode.” Pet. 24. Ingle states that an OLED can be formed on the substrate “using a conventional process.” Pet. 18 (quoting Ingle, 21:34-36). Accordingly, Ingle’s most complete Figure 1I depicts no such topmost electrode components:

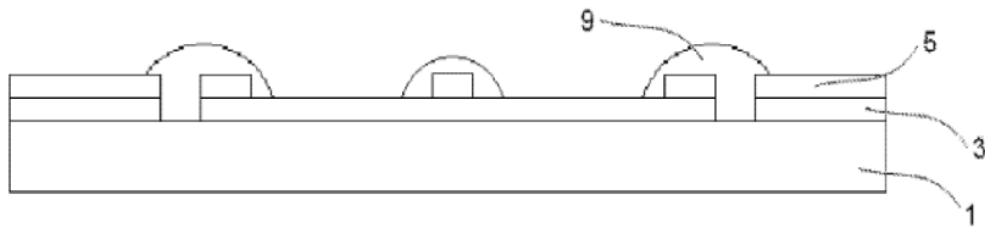
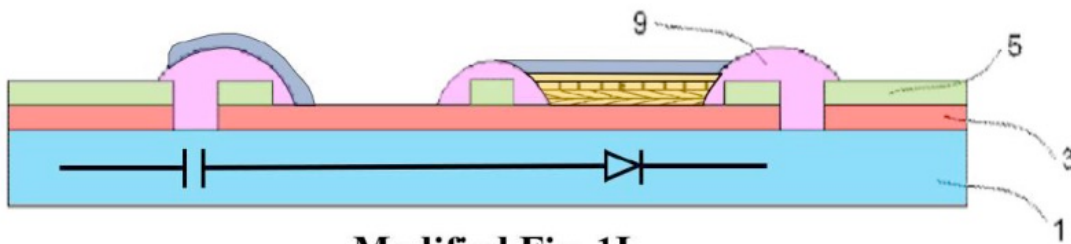


Fig. 1I

EX1005 (Ingle), Fig. 1I.

47. Thus, a POSITA would understand that Ingle’s disclosures do not describe or suggest the electrodes (shaded grey) depicted in various versions of Ingle Figure 1I “modified” by Petitioner.



Modified Fig. 1I

Pet. 27 (EX1005 (Ingle), Fig. 1I (annotated and modified by Petitioner); *see also* Pet. 20, 24, 37, 39, 45.

48. A POSITA would understand from Ingle’s disclosures that Ingle does not contemplate structured application of all layers of an electronic component or assembly. Samsung appears to disagree, citing Ingle’s statements “that its method ‘is *usually free* of photolithographic steps’ (Ingle, 18:7-10 (emphasis added)), and that ‘each layer of the component can be applied individually and, if necessary, structured according to desire or purpose.’ *Id.*, 7:20-24.” Pet. 24. “Usually free”

means that there can be occasions when one or more layers are applied using photolithographic steps. And “if necessary, structured according to desire or purpose” could be done at the time of the application or afterwards. Thus, a POSITA would not understand these quotes to suggest that any layer disclosed in Ingle could or should be applied in what Ingle describes as a structured fashion.

49. For example, the “method according to the invention” described by Ingle relates only to “printing *the insulator and the protective material* [not at issue in the independent claims] compared to the methods normally used in the prior art, such as lithographic methods.” Ingle, 16:12-16 (emphasis added); *see also id.* at 16:19-25 (“In contrast to the conventionally used lithography methods, in which each coating step is ... structured photolithographically, ... it is intended to apply only as much material of the *insulator and the protective material*, both of which can generally be expensive materials, as is required for production of the electronic component.” (emphasis added)). And the quote on page 7 merely discloses that “each layer of the component can be applied individually and, if necessary, structured according to desire or purpose.” Ingle, 7:20-27. It does not address whether the structuring occurs as part of the application or as part of subsequent steps, as noted above.

50. That Ingle does not contemplate structured application of all layers is reinforced by its disclosure that “the second electrically conductive layer” is

applied “over the entire surface of the first electrically conductive layer in accordance with the invention.” *Id.* at 7:29-31. And, as previously discussed, Ingle states that an OLED can be formed on the substrate “using a conventional process.” *Id.* at 21:34-36.

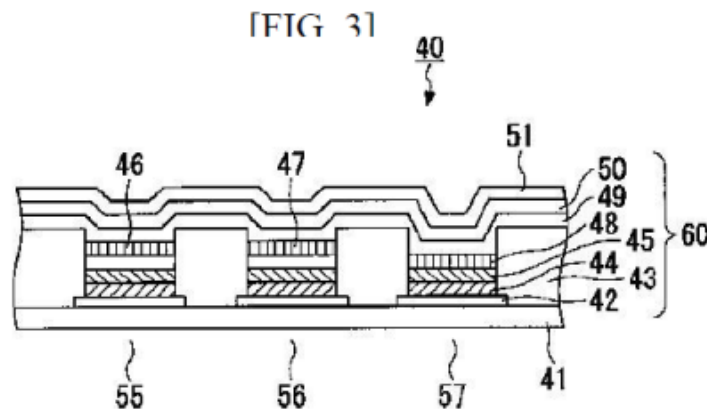
51. Neither Ingle nor Hasei describes the full scope of such a “conventional process” to fabricate an OLED. A POSITA at the time of the invention of the ’492 Patent, however, would not understand such a “conventional process” to include what Ingle describes as applying layers in a structured fashion. *See, e.g.*, Ingle, 16:19-21 (referring to “conventionally used lithography methods, in which each coating step is applied individually and structured photolithographically”); Hasei, ¶ 3 (describing the “conventional method” of photolithography); *see also* EX1001, 1:66-2:7 (describing a conventional lithography process as involving a “planar application of the corresponding layer and subsequent structuring of the layers,” and is “in contrast to” applying a layer “in a structured fashion”).

B. Hasei (EX1006 & EX1007)

52. Hasei describes using “a droplet discharging device” to discharge material “only onto the portions of the substrate where transparent electrodes or the like are to be formed.” EX1007, ¶¶ 15-16. A POSITA at the time of the invention of the ’492 Patent would not understand this to be a conventional process for

forming an OLED. Indeed, Hasei itself describes its purportedly novel approach as an improvement over what it characterizes as the “conventional method” of photolithography. Hasei, ¶ 3.

53. Hasei discloses an electro-optical device in Figure 3, but that figure does not depict the type of structured electrode claimed in the '492 Patent. For example, I understand that Petitioner relies (*e.g.*, Pet. 14) on “negative electrode 50” depicted in Hasei Figure 3, which Hasei describes as a “metal electrode.” Hasei, ¶ 3. In the variation depicted in Figure 3 relied upon by Petitioner, the negative electrode 50 appears continuous from left to right, rather than being deposited “in a structured fashion” (or only coated in partial regions dependent on the desired structure) as required by the claims.



EX1007 (Hasei), Fig. 3.

54. Based on these disclosures, a POSITA at the time of the invention of the '492 Patent would understand that this unbroken negative electrode 50 has not been structured in any manner, whether through application in a “structured

fashion” or through planar application and subsequent structuring by, for example, etching or photolithography.

55. Furthermore, a POSITA would understand that the negative electrode 50 described in Hasei and depicted in Figure 3 is continuous across the subpixels depicted in Figure 3. That is because negative electrode 50 is a common electrode. Hasei specifically teaches the use of a “negative electrode” (50) that is common among the different color emitting OLED sub-pixels, in contrast to “positive electrodes” that are individual to each sub-pixel device. In the described application of OLED displays individualizing both electrodes on each sub-pixel elements would greatly increase the complexity of the drive circuitry with no added benefits.

56. Kattamis’s references EX1010 and EX1014 which show examples of active matrix drive circuits for OLED displays describe the use of a common voltage (ground or V_{ca}) across one electrode of the OLED sub-pixel device which strongly suggests the use of a common electrode. EX1010 in figure 28 shows the use of a common electrode (2805) across multiple, individually controlled OLED sub-pixels.

57. Additionally, a POSITA at the time of invention of the ’492 Patent would understand that Hasei’s disclosures relate specifically to the printing of transparent electrodes in various optoelectronic devices. *See* EX1007, ¶¶ 15-16

(describing using “a droplet discharging device” to discharge material “only onto the portions of the substrate where transparent electrodes or the like are to be formed”). A POSITA, particularly as defined by Samsung, would not be motivated to apply the “droplet discharging” teachings of Hasei to, e.g., the common electrode of an OLED component or a capacitor like the one Petitioner proposes adding to Ingle with any reasonable expectation of success. While Hasei states that “negative electrode 50 may be formed by the droplet discharging method ... or may be formed by photolithography or etching” (Hasei, ¶ 3), the suggestion to use the “droplet discharging method” would not make sense to a POSITA in view of Figure 3 and the other teachings of Hasei. For example, Hasei discloses that “negative electrode 50 is a metal electrode” (*id.*)—i.e., not transparent. Furthermore, as discussed above in paragraphs 53-54, it would be clear to a POSITA from Figure 3 of Hasei that negative electrode 50 is a common electrode that is not structured, whereas positive electrode 42 is applied only on certain portions of the substrate 41 and “is capable of transmitting light.” Hasei, Fig. 3, ¶ 34. As such, a POSITA would not have been motivated to use Hasei’s “droplet discharging method” to form the negative electrode 50 in Figure 3 that Samsung and Dr. Kattamis rely upon. Moreover, there is no need to have a transparent electrode for a capacitor; and indeed ITO is an unsuitable material for constructing

a capacitor since it is not in the optical path of the optoelectronic device and therefore does not need to be transparent.

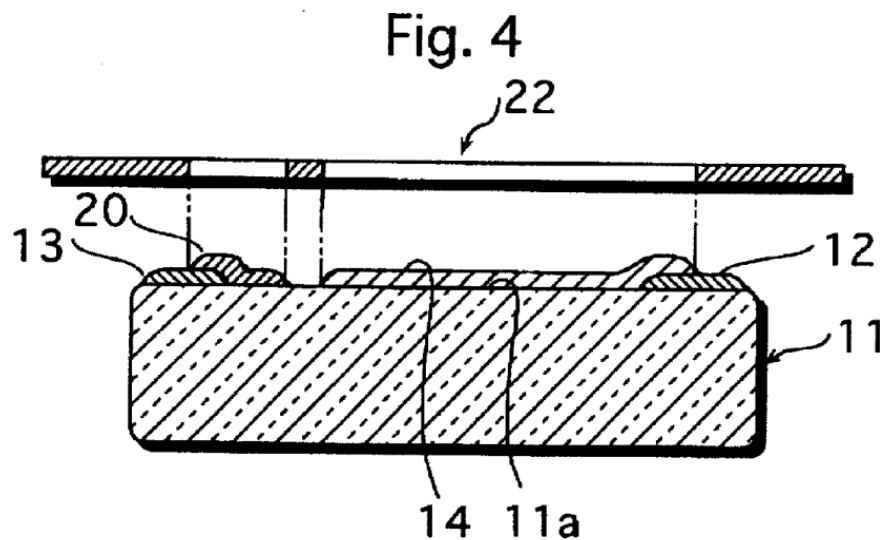
58. Furthermore, Hasei only describes a method for forming a wiring pattern of indium tin oxide, a well-known transparent conductive material, relevant for display applications where it is desirable to deploy a material on the light emitting side of the device that is both transparent and conductive. Hasei then provides exemplary embodiments for a range of display technologies, including plasma display panels, liquid crystal display, and OLED. As shown in figures 2-4 of Hasei, the different technologies have radically different device structures, which require very different drive circuits, but they all might benefit from the use of printed ITO layers on the light output side of the device.

59. Hasei does not mention or have application to the fabrication of capacitor or resistors. Hasei does not describe the fabrication process for an OLED device. It merely shows an example of a finished OLED pixel, which includes red, green, and blue sub-pixels, and provides a list of the different OLED materials that might be used without describing the deposition techniques or patterning of these layers.

C. Hanamura (EX1008)

60. Hanamura describes a technique for forming a capacitor that differs significantly from the claimed invention of the '492 Patent. For example, a

POSITA at the time of invention of the '492 Patent would not understand Hanamura to disclose or suggest the application of two electrically conductive layers into which a trench is formed. Instead, a POSITA would understand Hanamura as teaching adjacent electrodes (i.e., adjacent electrodes 13 and 20 and adjacent electrodes 12 and 14) applied selectively to a substrate to leave a “predetermined spacing” between electrodes 20 and 14 as shown below:



EX1008 (Hanamura), Fig. 4; *see also id.* at 5:55-59 (“predetermined spacing”).

61. A POSITA would not understand this “predetermined spacing”—to the extent it may be viewed as a trench—as being “in” electrodes 12, 13, 14, and 20, but only between electrode 20 and a laterally placed electrode 14. As such, a POSITA would not understand Hanamura to teach a trench “in” both first and second electrically conductive layers (mapped to electrodes 12, 13, 14, and 20), much less forming such a trench. Hanamura describes additive deposition of

adjacent electrode layers to form a space for the dielectric and the creation of a capacitor. This is in contrast to the subtractive method of creating the trench between pre-deposited electrode layers using a removal step such as laser-ablation as described in the '492 Patent.

D. Egitto (EX1013)

62. Egitto “relates to providing resistors for circuitized substrates,” and “to products including such resistors ... wherein the resistors are film resistors formed using trimming processes.” EX1013, ¶1. Egitto also discloses “representative patterns which may be etched within the resistor material.” *Id.*, ¶82.

VI. THE COMBINATION OF INGLE AND HASEI DOES NOT DISCLOSE OR SUGGEST APPLYING AN “ELECTRICALLY CONDUCTIVE ELECTRODE LAYER” AS CLAIMED

63. I have been asked to comment on Samsung’s position that a POSITA at the time of invention of the '492 Patent would read Ingle and Hasei as disclosing “applying an electrically conductive electrode layer [e.g., the cathode for a capacitor or OLED] in a structured fashion” or “above the first contact region” as required in some form by each independent claim of the '492 Patent. *See, e.g.*, Pet. 36-38. I disagree.

A. A POSITA Would Not Apply an “Electrically Conductive Electrode Layer” in a “Structured Fashion” as Specifically Claimed

64. Neither Samsung nor Dr. Kattamis provide any evidence of why a POSITA would have understood Ingle to disclose or suggest applying an

electrically conductive electrode layer in a structured fashion. To the contrary, Petitioner concedes that “Ingle leaves open how to finish forming a capacitor on its base structure, i.e., how to apply the cathode.” Pet. 24.

65. As discussed above (in Sections V.A & V.B), a POSITA at the time of invention of the ’492 Patent would not understand the combination of Ingle and Hasei to disclose this limitation.

66. For example, Ingle states that an OLED can be formed on the substrate “using a conventional process.” Ingle, 21:34-36. Neither Ingle nor Hasei describes the full scope of such a “conventional process” to fabricate an OLED. A POSITA at the time of the invention of the ’492 Patent, however, would not understand such a “conventional process” to include what Ingle describes as applying layers in a structured fashion. At least part of the “conventional” method for producing OLED tiles in Ingle, for example, refers to “the conventionally used lithography methods, in which each coating step is applied individually and structured photolithographically.” *Id.* at 16:19-21. That is consistent with the ’492 Patent, which explains that a conventional lithography process involves a “planar application of the corresponding layer and subsequent structuring of the layers,” and is “in contrast to” applying a layer “in a structured fashion.” EX1001, 1:66-2:7. That is also consistent with Hasei, which describes the “conventional method” of photolithography. Hasei, ¶ 3.

67. A POSITA would understand, however, that a top electrode layer would be a necessary component of the OLED described in Hasei that Samsung and Dr. Kattamis suggest could be formed on the structure described in Ingle. It would also be required by the challenged claims of the '492 Patent, which recites, for example, “applying the electrode layer in a structured fashion such that a part of the electrode layer covers the optically functional layer.” EX1001, 21:38-40.

68. A POSITA would understand from Ingle’s disclosures that Ingle does not contemplate structured application of the claimed electrically conductive electrode layer of an electronic component or assembly. Samsung cites Ingle’s statements “that its method ‘is usually free of photolithographic steps’ (Ingle, 18:7-10), and that ‘each layer of the component can be applied individually and, if necessary, structured according to desire or purpose.’ *Id.*, 7:20-24.” Pet. 24. But a POSITA would not understand these quotes to suggest that an electrically conductive electrode layer in Ingle could or should be applied in what Ingle describes as a structured fashion.

69. For example, the “method according to the invention” described by Ingle relates only to “printing *the insulator and the protective material* [not at issue in the independent claims] compared to the methods normally used in the prior art, such as lithographic methods.” Ingle, 16:12-16 (emphasis added); *see also id.* at 16:19-25 (“In contrast to the conventionally used lithography methods,

in which each coating step is ... structured photolithographically, ... it is intended to apply only as much material of the *insulator and the protective material*, both of which can generally be expensive materials, as is required for production of the electronic component.” (emphasis added)). And the quote on page 7 merely discloses that “each layer of the component can be applied individually and, if necessary, structured according to desire or purpose.” Ingle, 7:20-27. It does not address whether the structuring occurs as part of the application or as part of subsequent, conventional techniques.

70. That Ingle does not contemplate structured application of all layers is reinforced by its disclosure that “the second electrically conductive layer” is applied “over the entire surface of the first electrically conductive layer in accordance with the invention.” *Id.* at 7:29-31. And, as previously discussed, Ingle states that an OLED can be formed on the substrate “using a conventional process.” *Id.* at 21:34-36. Given Ingle’s description of what it viewed as a “conventional” process, a POSITA would understand that the OLED would be formed using a conventional photolithographic method that does not involve application in a “structured fashion.”

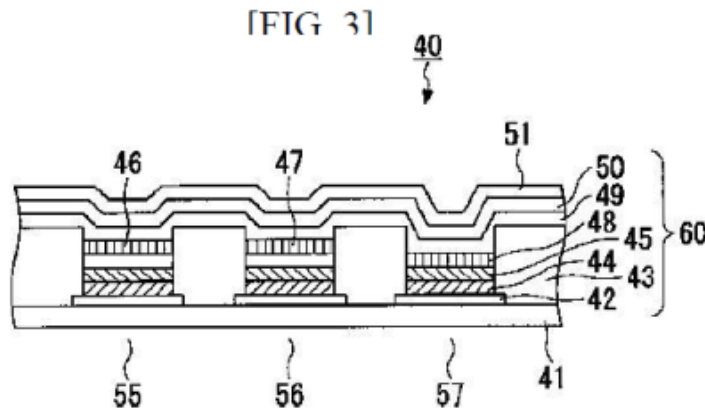
71. I understand that Samsung alleges that Hasei describes the “conventional process” for forming an OLED referenced in Ingle. Pet. 12. I disagree.

72. For example, although Hasei discloses using “a droplet discharging device” to discharge material “only onto the portions of the substrate where transparent electrodes or the like are to be formed” (EX1007, ¶¶ 15-16), this is not what Hasei calls the “conventional process.” Rather, that approach represents the purportedly novel approach described by Hasei as an improvement over the “conventional method” of photolithography. Hasei, ¶ 3 (describing “the conventional method of providing a conductive pattern [that] requires a photomask to be used in the photolithography process”). Moreover, this portion of the process precedes and is distinct from the actual fabrication of the OLED device structures. This is clear because the printing of the transparent electrodes can be used for very different display technologies which require vastly different manufacturing methods. A POSITA would not understand Hasei to disclose or suggest applying this improved process to the electrode layer 50, which is specific to the OLED device, and which is the electrode above a dielectric layer and the optical functional layer that needs to be applied in a structured fashion. *See, e.g.*, Hasei, Fig. 3 (negative electrode layer 50 is applied continuously from left to right, instead of only in discrete places as layers 42 and 46-48), ¶ 32.

73. Moreover, Hasei contains no discussion of forming capacitors. Indeed, Hasei does not include a single reference to capacitors of any type; and Petitioner and Dr. Kattamis provide no reason why a POSITA would have

extended Hasei's method for producing its OLED to a capacitor or to any other type of electronic component. Indeed, they would not have viewed the use of a transparent electrode such as ITO as appropriate for forming a capacitor. And, as discussed above (in Section V.B), a POSITA at the time of invention of the '492 Patent would understand that Hasei's disclosures relate specifically to transparent electrodes in OLED devices. As discussed above in paragraph 57, a POSITA, particularly as defined by Samsung, would not be motivated to apply the teachings of Hasei to the common electrode of an OLED component, optoelectronic components, or other types of electronic components with any reasonable expectation of success.

74. I understand that Petitioner relies (*e.g.*, Pet. 14) on “negative electrode 50” depicted in Hasei Figure 3 as the claimed electrically conductive electrode layer that must be applied in structured fashion. In the variation depicted in Figure 3 relied upon by Petitioner, the negative electrode 50 appears continuous from left to right, rather than being deposited “in a structured fashion” (or only coated in partial regions dependent on the desired structure) as required by the claims.



EX1007 (Hasei), Fig. 3.

75. Based on these disclosures, a POSITA at the time of the invention of the '492 Patent would understand that this unbroken negative electrode 50 has not been structured in any manner, whether through application in a “structured fashion” or through planar application and subsequent structuring by, for example, etching or photolithography. Additionally, neither Samsung nor Dr. Kattamis explain why a POSITA would have been motivated to form cathodes in discrete regions of Ingle’s disclosed device in this “structured fashion” based on Hasei Figure 3. And as discussed above in paragraph 57, a POSITA would not have been motivated to apply Hasei’s “droplet discharging method” to the negative electrode 50 in Figure 3 on which Samsung and Dr. Kattamis rely to support the imaginary cathode depicted in their modified version of Ingle Figure 1I. *See, e.g.*, Pet. 37.

76. Furthermore, a POSITA would understand that the negative electrode 50 described in Hasei and depicted in Figure 3 must be continuous across the subpixels depicted in Figure 3. That is because negative electrode 50 is a common

electrode to all of the sub-pixels (and most likely multiple pixels), which greatly simplifies the circuit design and the common electrode with a common voltage is described in EX1010 and EX1014 provided by Dr. Kattamis.

B. A POSITA Would Not Apply an “Electrically Conductive Electrode Layer ... Above the First Contact Region” as Specifically Claimed

77. In my opinion, a POSITA at the time of invention of the '492 Patent would not have understood the combination of Ingle and Hasei to teach applying the claimed electrically conductive electrode layer (e.g., a cathode) “above the first contact region,” which is required by each independent claim of the '492 Patent.

78. I understand that each of Samsung’s Grounds relies on mapping this claim term to a capacitor. *See, e.g.*, Pet. 27, 50. In the context of a capacitor, the layering of this electrode to the dielectric and above the first contact region, as well as to the second contact region, is critical to form the capacitor, the structure that Petitioner relies on for its unpatentability theory.

79. As discussed above (in Section IV), these features are fundamental to the structure of a capacitor. A POSITA at the time of invention of the '492 Patent would not understand Ingle or Hasei to teach the claimed structure.

80. As Samsung admits, “Ingle leaves open how to finish forming a capacitor on its base structure, i.e., how to apply the cathode.” Pet. 24. Thus, it is

not surprising that the most complete Figure 1I depicts no such topmost electrode components:

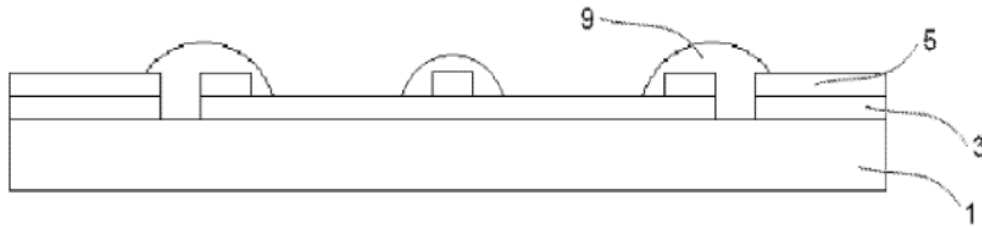
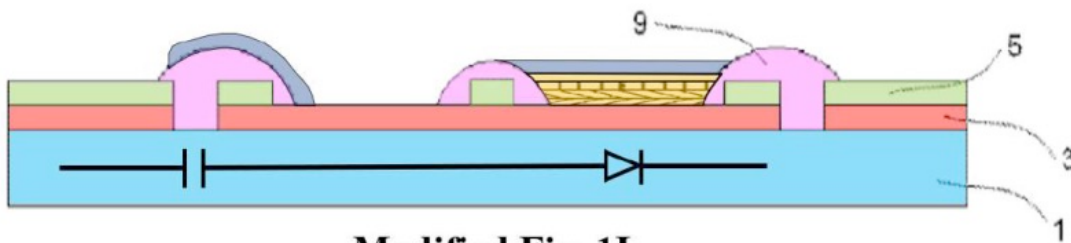


Fig. 1I

EX1005 (Ingle), Fig. 1I.

81. As such, a POSITA would understand from these disclosures that the alleged electrically conductive electrode layers (shaded grey) depicted in various versions of Ingle Figure 1I “modified” by Petitioner have no basis in Ingle’s disclosures.

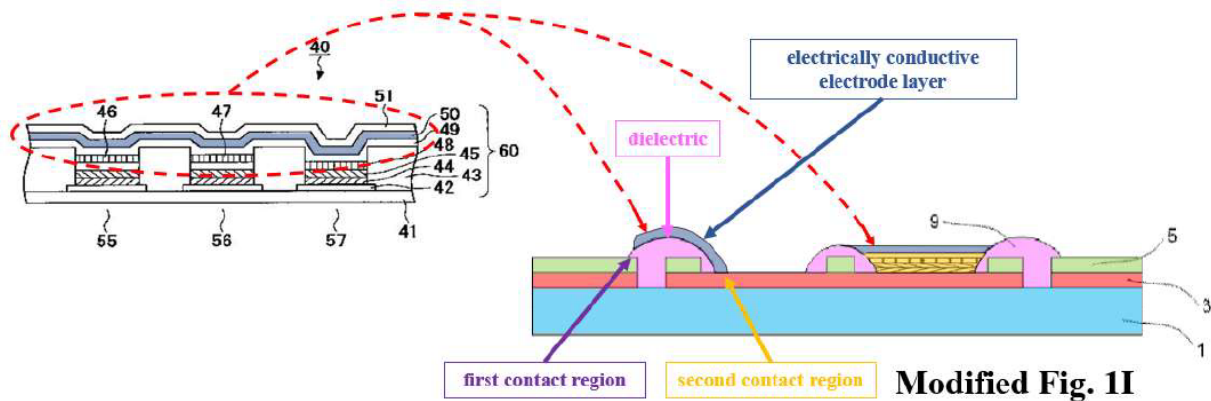


Modified Fig. 1I

Pet. 27 (EX1005 (Ingle), Fig. 1I (annotated and modified by Petitioner); *see also* Pet. 20, 24, 37, 39, 45.

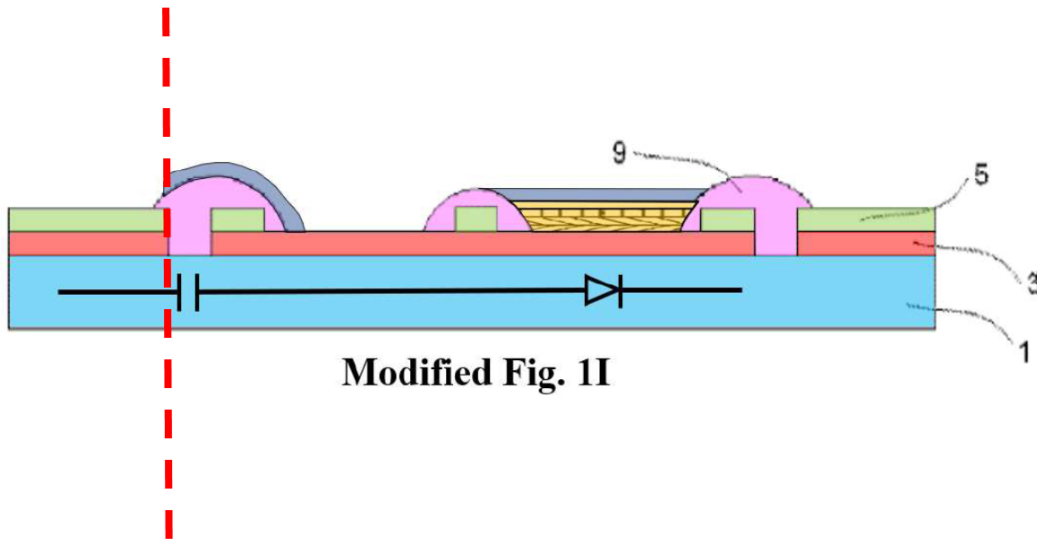
82. Even assuming that such layers were disclosed, however, Petitioner’s own modified version of Ingle Fig. 1I (reproduced below) does not depict an “electrically conductive [electrode] layer (grey) ... applied to the dielectric (pink)

above the first contact region.” Yet Petitioner relies on this “modified” figure as teaching or suggesting this limitation. *See* Pet. 37 (“As shown in the figures below....”).



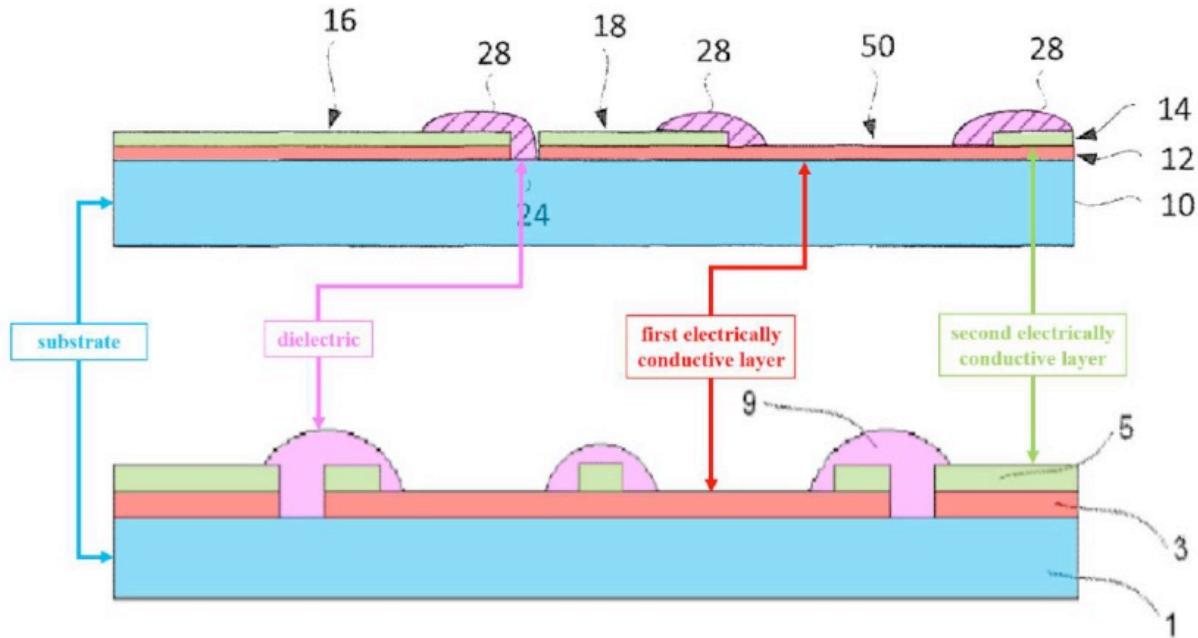
Id. (depicting Hasei, Fig. 3 (left, annotated by Petitioner), and Ingle, Fig. 1I (right, annotated and modified by Petitioner)).

83. This deficiency in Petitioner’s theory is demonstrated more clearly in the annotated version of Ingle Figure 1I on page 27 of the Petition, which—as highlighted by the further annotation of a broken red line below—demonstrates the lack of overlap:



Pet. 27 (further modified (with broken red line) version of Ingle, Fig. 1I (otherwise annotated and modified by Petitioner)). As shown above, the electrode (gray) ends at the right edge of the first contact region and it is therefore not “above” the first contact region.

84. A POSITA would thus understand Ingle’s structure as differing significantly from that of the ’492 Patent in material ways. For example, the application of the dielectric results in significant overlap of the first contact region in the ’492 Patent but not in Ingle. This is evident in Petitioner’s own annotated comparison of Figure 15 of the ’492 Patent and Figure 1I of the Ingle reference:



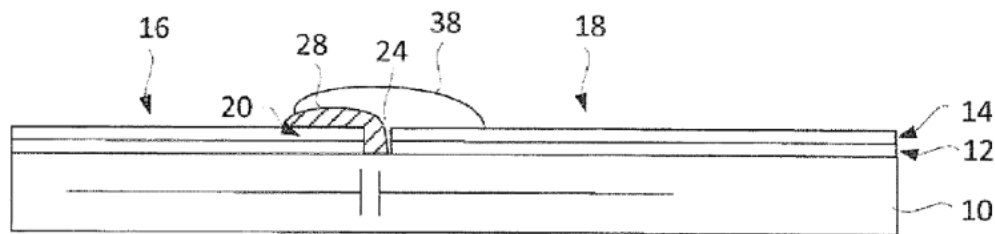
Pet. 12 (comparing '492 Patent, Fig. 15 (annotated, top) with Ingle, Fig. 1I (annotated, bottom)). As these annotated figures demonstrate, the leftmost dielectric 28 applied in the '492 Patent significantly covers region 16, whereas in Ingle, the leftmost dielectric barely covers the corner of the equivalent portion of the second electrically conductive layer (i.e., the alleged first contact region). In fact, it is difficult to envision any such overlap, given the applied dielectric's minimal overlap of the first contact region.

85. A POSITA would understand that this distinction matters. According to Petitioner, applying this electrode layer to the dielectric above the first contact region is necessary to create a capacitor. *See* Pet. 36 (referencing completing a capacitor “on Ingle’s base structure by applying an electrode above the dielectric in the first contact region” as well as forming “an electrode above the left-side

dielectric in Ingle's base structure ... to form a capacitor connected to the OLED").

That is consistent with the '492 Patent specification as it relates to the formation of a capacitor, which explains that "a first electrode of a capacitor is formed by the first contact region between the dielectric and the substrate and a second electrode of the capacitor is formed by the electrode layer on a side of the dielectric facing away from the first contact region." EX1001, 3:38-42. That claimed structure is shown in Figure 7:

Fig. 7



Id. at Fig. 7. The '492 Patent describes this electronic component:

FIG. 7 shows the substrate 10 and the first and second electrically conductive layers 12, 14 with the dielectric 28, wherein an electrode layer 38 is applied in a structured fashion on the dielectric 28 and a part of the second contact region 18. The first contact region 16 between the substrate 10 and the electrode layer 38 serves as a first electrode, for example as an anode, of the passive electronic component. The electrode layer 38 on a side of the dielectric 28 facing away from the substrate 10 serves as a second electrode, for example as a cathode, of the passive electronic component.

Id. at 12:27-36.

86. I understand that Samsung and Dr. Kattamis contend that "[a]

POSITA would readily understand that Ingle's capacitor *could be* completed on

Ingle's base structure by applying an electrode above the dielectric in the first contact region." Pet. 36 (citing EX1003, ¶ 162). But Dr. Kattamis provides no explanation for how to overcome the overlap issues described above in the cited portion of his declaration. *See* EX1003, ¶162. And while I understand the Petition also asserts that "[a] POSITA would understand that the degree to which both the dielectric (pink) and the electrically conductive [electrode] layer (grey) extend over the first contact region may be adjusted to fine-tune the capacitance of the capacitor," the cited declaration testimony merely parrots this statement without any meaningful support or explanation. *See* Pet. 38; EX1003, ¶167. Moreover, this statement assumes some degree of overlap between the electrically conductive electrode layer and the first contact region, which a POSITA would not understand to exist as explained above.

87. Furthermore, extending the imaginary electrically conductive electrode layer further to the left (and thus "over" the first contact region) would risk a short-circuit or capacitor breakdown due to irregular distance and area between the applied cathode and the first contact region, which would render the capacitor inoperable. A POSITA would not have been motivated to pursue such a capacitor. And without this overlap, applying a cathode as depicted and described by Petitioner and Dr. Kattamis would not form a reliably working capacitor, as any capacitance would be poorly controlled due to inconsistencies in the application of

the dielectric and the lack of parallel-facing electrodes. The fundamental performance is a function of the distance between the electrodes, the area of the electrodes, and the dielectric materials properties. The capacitor proposed by Dr. Kattamis would have a small overlap area of the electrodes at a small and poorly controlled distance (due to the structured deposition). This would result in inconsistent capacitance, the likelihood of capacitor breakdown, and the likelihood of short-circuiting the capacitor.

88. To the extent that Samsung or Dr. Kattamis later allege (they do not currently) that the capacitor is formed by the trench, with electrodes on either side formed by the first and second electrically conductive layers, that would render the alleged electrically conductive electrode layer superfluous because the electrode could be much more readily deposited (with greater tolerance) directly on the planar surface of the second contact region without risk of short-circuit.

89. And because, as discussed previously, Hasei does not even purport to disclose methods for forming capacitors, a POSITA would not understand it to cure any of these deficiencies in Ingle's disclosures.

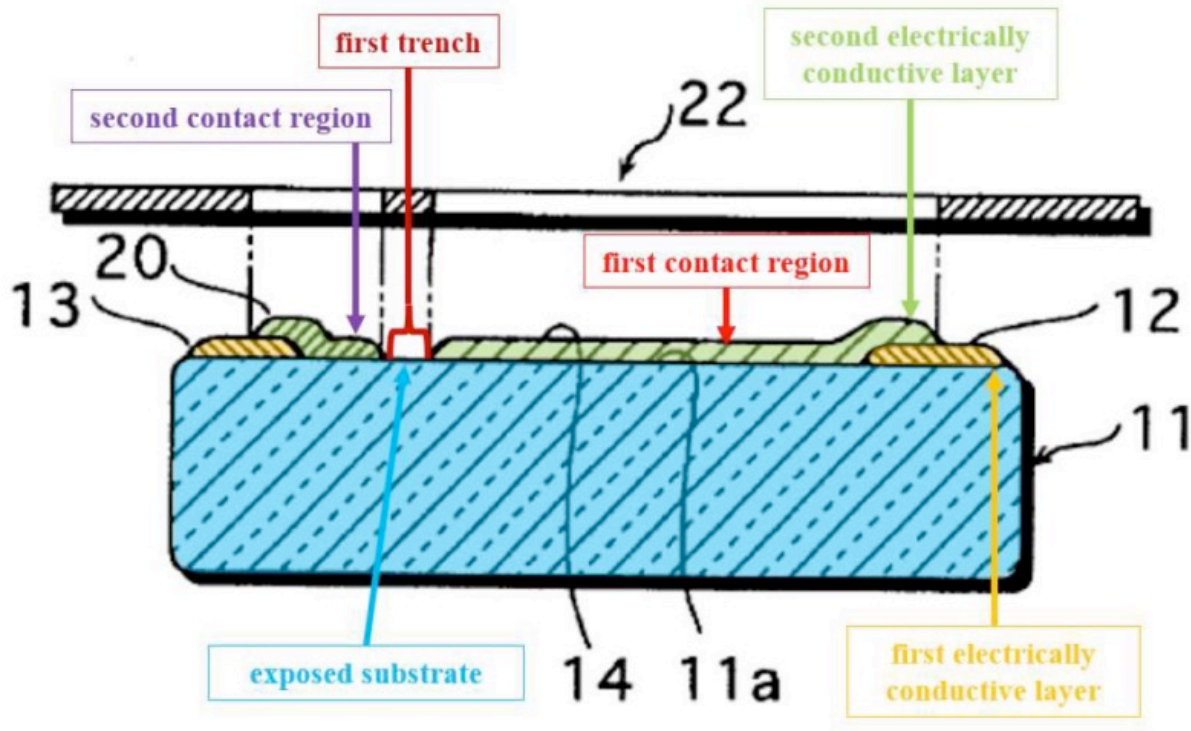
VII. HANAMURA DOES NOT DISCLOSE A TRENCH IN THE FIRST AND SECOND ELECTRICALLY CONDUCTIVE LAYERS

90. I understand that, for purposes of Grounds 2 and 3 challenging Claims 1, 2, 3, 5, 6, 8, and 16, Petitioner relies on the teachings of Hanamura for the first

and second electrically conductive layers, and well as the first trench in those layers required by independent Claims 1 and 16. *See* Pet. 51-4, 58-59.

91. In my opinion, a POSITA at the time of invention of the '492 Patent would not understand Hanamura to disclose or suggest these claimed features.

92. For example, as shown in Petitioner's own annotated versions of Hanamura's figures, the alleged "first electrically conductive layer" (electrodes 12 and 13, colored yellow below) and the alleged "second electrically conductive layer" (electrodes 14 and 20, colored green below) are in fact four adjacent and slightly overlapping electrodes. All four electrodes collectively occupy a single horizontal plane, and a POSITA would not have viewed electrode 20 as "on" the electrode 13 or electrode 14 as "on" the electrode 12.



Pet. 54 (EX1008 (Hanamura), Fig. 4 (annotated by Petitioner).

93. A POSITA would not view this disclosure as consistent with the '492 Patent's description of the claimed first and second electrically conductive layers, which are depicted as distinct planar layers. *E.g.*, EX1001, Fig. 3; *see also id.* at 11:2-4 (explaining that "[t]he first electrically conductive layer 12 can be applied to the substrate 10 for example in a planar fashion, that is to say without structure"), 11:24-26 (same as to the "second electrically conductive layer 14"). Hanamura itself does not describe these electrodes as "layers," but rather as "a first lead electrode 12 and a second lead electrode 13," and "a first capacitor electrode 14 and an auxiliary electrode 20." EX1008, 5:25-32. By contrast, Hanamura

describes a dielectric layer 15 [that] is formed on the first capacitor electrode 14.”

Id. at 5:33-36; *see also id.* at 5:45-47 (describing “a protective overcoat layer 19”).

94. Dr. Kattamis does not explain why a POSITA would view these disclosures differently. He quotes a portion of Hanamura describing the electrodes and then concludes without explanation that “a POSITA would recognized Hanamura’s electrodes 12 and 13, which are stated to be deposited simultaneously, as the ’492 patent’s claimed “first electrically conductive layer.” EX1003, ¶ 225. Similarly, Dr. Kattamis states without explanation that “Hanamura’s Fig. 4 ... also depicts a second electrically conductive layer.” *Id.*, ¶ 230.

95. Even if electrodes 13 and 20 could constitute a first electrically conductive layer and electrodes 14 and 20 could constitute a second electrically conductive layer, a POSITA would understand that Hanamura fails to disclose “a first trench in the first and second electrically conductive layers” as required by independent claims 1 and 16, and thus required by each claim challenged in Grounds 2 and 3. At most, a POSITA would understand Hanamura to disclose that a “predetermined spacing” is “reliably provided between” electrodes 14 and 20. EX1008 (Hanamura), at 5:55-59. A POSITA would not, however, view the predetermined spacing as being in electrodes 13 and 12 (the purported first electrically conductive layer), for example.

96. Merely leaving a gap or “predetermined spacing” between selectively applied electrodes (EX1008 (Hanamura), 5:55-59) is not consistent with the invention described and claimed in the ’492 Patent. Moreover, Petitioner indicates at most that a “trench” is allegedly in the second electrically conductive layer (mapped to electrodes 20 and 14). Neither Samsung nor Dr. Kattamis provides any explanation for how the trench is also in the first electrically conductive layer (mapped to electrodes 12 and 13). *See* Pet. 53; EX1003, ¶¶ 232-35.

97. Furthermore, because the space between electrodes 14 and 20 characterized as a “trench” by Petitioner already exists (*see* EX1008, Fig. 5), there is no need—and indeed no possibility—of “forming” the alleged trench as required by Claim 1. A POSITA would not be motivated to use methods such as “etching” or “laser ablation” to “form” a trench, thereby exposing the substrate and separating first and second contact regions from each other when a spacing exists that already leaves the substrate exposed and already separates the alleged contact regions. *See* EX1001, at 1:55-58, 4:5-9.

98. A POSITA would not be motivated to use Hanamura’s capacitor technique because forming a trench by the subtractive process of laser ablation would have much higher resolution and accuracy where the laser can be highly targeted and focused compared to creating a gap between adjacent additively printed layers. The trenching described in the ’492 Patent would result in more

consistent capacitor performance and reduced area so that more devices can be created within the substrate area.

VIII. A POSITA WOULD NOT HAVE BEEN MOTIVATED TO COMBINE THE TEACHINGS OF HANAMURA AND EGITTO

99. I understand that the Petition relies on the combination of Hanamura and Egitto for Claims 3 and 5. As Samsung and Dr. Kattamis admit, claim 3 (and thus dependent claim 5) “requires that the resistance region have a particular design, i.e., that a second trench and at least one third trench are formed, which delimit the resistance region, and which cause the resistance region to have taper in a direction parallel to the electrically conductive layers.” Pet. 64; *see also* EX1003, ¶ 276 (“Claim 3 of the ’492 patent requires that the resistance region have a particular geometric design.”).

100. I disagree with Samsung and Dr. Kattamis that *any* potential resistance region design is merely a “design choice” and would thereby be obvious to a POSITA at the time of invention of the ’492 Patent. *See* Pet. 64; EX1003, ¶¶ 267-78.

101. Neither the Petition nor Dr. Kattamis’s declaration provides any specific motivation to combine the teachings of Hanamura—including its disclosure of “a resistor having a reliably adjusted resistance” (Pet. 60 (quoting EX1003 (Hanamura), 2:39-40) or its disclosure that a “resistor can ‘control the rate of electric charging and discharging of the capacitor” (*id.* at 61 (quoting

Hanamura, 6:55-58))—with the *specific* “representative pattern[]” described in Egitto paragraph 82 and Figure 8.

102. Accordingly, a POSITA would not have been motivated to combine the teachings of Hanamura and Egitto in the manner suggested in the Petition.

103. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

104. Executed on November 20, 2024, in Ringgold, GA.

A handwritten signature in black ink, appearing to read "P. Morgan Pattison", is written over a horizontal line.

P. Morgan Pattison, Ph.D.

EXHIBIT A

P. Morgan Pattison
morgan@sslsinc.com
(805)217-3878

Experience

Solid State Lighting Services, Inc.

November 2007 - Present

Founder/President- Provide technical, strategic, and market expertise in the areas of LEDs, OLEDs, Lighting, Solid State Lighting (SSL), displays, and optoelectronic materials and devices. LED device, lighting, and materials product development. Horticultural lighting research and strategy. Light pollution measurement, evaluation, and mitigation. LED and lighting product failure and reliability evaluation. Manage research on human and animal physiological responses to light. Scout and evaluate new technologies for investment.

U.S. Department of Energy

January 2006 – November 2007

National Energy Technology Laboratory, Morgantown WV

Project Manager- Managed DOE funded R&D projects in SSL including LED and OLED lighting technologies. Managed solicitation and selection of new funded R&D projects. Identified priority areas of research necessary for advancement of SSL efficiency, performance, and price.

University of California, Santa Barbara

September 2000 – January 2006

Graduate Student Researcher- Doctoral thesis research under Professor Shuji Nakamura (Nobel Prize in Physics 2014) on GaN based micro-cavity light emitting diodes. Research included: epitaxial structure design and growth by MOCVD, semiconductor process development, materials characterization, and electro-optical device characterization. Additional areas of research included UV LEDs, vertical cavity surface emitting laser (VCSEL), and edge emitting laser diodes.

Cymer Laser, San Diego

November 1996 – May 2000

Laser Test Engineer- Tested and developed test methodology for production and prototype KrF and ArF excimer lasers used in deep UV photolithography for manufacturing of advanced semiconductor products. Testing included optical characterization and full system troubleshooting. Test development of new electrical and optical test methodologies to improve test cycle, Labview automation of test procedures, and development of test documentation.

Education

Ph.D. Materials Science, Electronic and Photonic Materials

University of California, Santa Barbara, 2006

Thesis: *Fabrication and Characterization of Gallium Nitride Based Micro-Cavity LEDs*

M.S. Electrical Engineering, Electronics and Photonics

University of California, Santa Barbara, 2003

B.S. Electrical Engineering, Electronic Devices and Materials

University of California, San Diego, 1996

Expertise

Optoelectronic materials and devices, lighting, LED, OLED, UV-LEDs, Germicidal UV application, R&D and technology evaluation, μ LED-LED-OLED-Quantum Dot display technology, medical lighting, SSL product evaluation and selection, LED lighting product development, R&D Management, technology roadmapping, technical meeting moderation, technical writing, IP evaluation, trial expert witness, lighting color evaluation and selection, advanced lighting performance evaluation, Energy Star LED lighting testing, photometric characterization and testing, R&D Management, Federal R&D funding processes, R&D Proposal review and evaluation, ESCO contracts and performance measurement & verification (M&V), horticultural lighting, wildlife responses to light, human physiological responses to light

Accreditations, Affiliations, and Professional Societies

Fellow - Illuminating Engineering Society (IES)

Chair – Outdoor Nighttime Environments (ONE) Committee

Voting Member – IES Horticultural Lighting Committee

Oregon State University, Civil and Construction Engineering, Courtesy Faculty

Lighting Certified (LC) by National Council on Qualifications for Lighting Professionals

Member: International Society of Horticultural Scientists (ISHS), International Dark-Sky Association (IDA), International Society for Optics and Photonics (SPIE), American Society of Agricultural and Biological Engineers (ASABE), American Physical Society (APS)

Project Management Professional (PMP) *Lapsed*, Project Management Institute (2006)

U.S. Government Contracting Officer's Representative (COR) (2006)

Leadership

Senior Technical and Strategic Advisor to DOE SSL R&D Program

Lead writer of DOE SSL R&D Opportunities, R&D Plan, and Multi-Year Program Plan

Technical content supervisor of annual DOE SSL R&D Workshops

Manage organization of DOE SSL topical R&D meetings on: LED devices and materials, OLEDs, luminaire integration, roadway lighting, germicidal ultraviolet (UV) LEDs, human physiological responses to light, domesticated and wild animal responses to light, roadway and area lighting, and horticultural lighting

New business creation/development –*Action Spectrum*, *Ultra-Yield Solutions*, *Guidance LED*, *Zuli*, *Canvas*, *Intellilight/Next*, *SSLs, Inc.*, *Diel Lighting Science*, *Blue Laser Fusion*

Scientific Advisory Board member to *GLASE (Greenhouse Lighting and System Engineering)*, NYSERDA funded controlled environment agriculture R&D program

Technical Advisory Committee of Resource Innovation Institute

Advisory Board Member of *Phosphor Global Summit* annual meeting

Advisor to *Cyclotron Road* – Clean Technology Incubator at Lawrence Berkeley National Lab

Project sponsor for Senior Design Course at UCSB (2011-2012)

1. Design and development of spectro-goniophotometer
2. Design and development of smartphone light controller (co-founder and original board member of resulting company renamed *Zuli*)

Designed, fabricated, and characterized world's first gallium nitride microcavity LED

Fabricated and characterized world's first gallium nitride semipolar LED

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Presentations

2024 Joint CEA Workshop, U.S. Fish & Wildlife Service Light Pollution & Bird Collisions expert panel, Workshop on Disorder in Semiconductor Physics and Devices 2024, University of Cincinnati IRIS 2023 Working Group, IES Raleigh Section “Horticultural Lighting – A Growing Opportunity”, IES Street and Area Lighting Conference 2022, National Park Service Science and Technology – Skyglow Measurements at Channel Islands National Park 2022, UCSB Nitride Seminar 2022, International SSL Alliance 2021 General Assembly, The Limits of Food Production – Vertical Farming 2021, Horticonn 2020, U.C. Davis Energy and Efficiency Institute,

California Energy Administration, 2020 DOE Lighting R&D Workshop, Charleston Catholic High School STEM Seminar, East Tennessee State University Physics and Astronomy Seminar, IES Rocky Mountain Section – CU Boulder, 2019 DOE SSL R&D Workshop, Harvard ES-173 Guest Lecture, U.S. DOE Building Technologies Office Brown Bag Seminar, U.C. Santa Barbara Nitrides Seminar 2018, Phosphor Global Summit 2018, West Virginia State University – Biology Seminar, East Tennessee State University Entrepreneur Club 2018, IES Aviation Lighting Committee Meeting 2017 (Best Technical Paper), ICCEA Panama 2017, NCERA 101 Controlled Environment Agriculture meeting, DOE SSL R&D Workshop 2017, The College of New Jersey Physics Colloquium, DOE SSL R&D Workshop 2017, NREL 2016, Harvard University Engineering Seminar, LightSym 2016, DOE SSL R&D Workshop 2016, DOE SSL Technology development Workshop 2015, DOE SSL R&D Workshop 2015, IDTechX Internet of Things Applications, Phosphor Global Summit 2014, International Conference on Nitride Semiconductors 2013, IES Illuminate Philadelphia 2012, Strategies in Light 2012, Energy Efficiency Expo 2011, Tennessee Association of Physical Plant Administrators 2011, East Tennessee State University Faculty Development Sustainability Seminar 2011, LED Discovery 2010, Think Tomorrow Today 2008, International Conference on Nitride Semiconductors 2005, International Symposium on Blue Lasers and Light Emitting Diodes 2004, Fall Materials Research Society 2001.

Patents

Technique for growth and fabrication of semipolar (Ga, Al, In, B) N thin films, heterostructures, and devices. #9793435, #9231376, #8686466, #7846757, #10529892

Lighting unit having lighting strips with lighting elements and a remote luminescent material. #8491165

Lighting unit with heat dissipating chimney #8360607

Lighting unit with indirect light source #8684566 B2

System for monitor and control of equipment. #9432210

Semiconductor light emitting device #8227820, #8643036

Etching technique for the fabrication of thin (Al, In, Ga) N layers. #7795146

Semiconductor micro-cavity light emitting diode. Application # 11/510,240 (abandoned), WO2007025122