

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.,
Petitioner,

v.

PICTIVA DISPLAYS INTERNATIONAL LTD.,
Patent Owner.

Case IPR2024-01187
U.S. Patent No. 9,257,492

**REPLY DECLARATION OF ALEX Z. KATTAMIS, PH.D., P.E.,
FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,257,492**

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I. Introduction

1. My name is Alex Kattamis. I make this declaration based upon my own personal knowledge and, if called upon to testify, would testify competently to the matters contained herein.

2. I have been retained by counsel for Petitioner Samsung Display Co., Ltd. (“Petitioner”) to provide technical assistance in an *inter partes* review of U.S. Patent No. 9,257,492 (the “’492 patent”).

3. I am a salaried employee of Exponent, Inc. (“Exponent”). Exponent charges \$575 per hour for my time plus expenses for work performed in connection with this project. I have received no additional compensation for work in this case, and my compensation does not depend upon the contents of this declaration, any testimony I may provide, or the ultimate outcome of this case.

4. I have been asked to provide this reply declaration in response to certain arguments made by Pictiva Displays International Ltd. (“Pictiva”), the Patent Owner (“PO”), in the Patent Owner’s Response (Paper 20, “POR”) to the Petition (Paper 1) and made in the supporting declarations of Dr. Pattison (Ex. 2001 “Pattison Decl.”, Ex. 2005 “Pattison Suppl. Decl.”). I incorporate by reference my opening declaration (Ex. 1003, “Opening Decl.”) in its entirety. In forming my opinions, I reviewed the documents in the following table, as well as the documents cited in the POR and the declarations of Dr. Pattison (Ex. 2001, Ex. 2005).

Ex.	Description of Exhibit
1001	U.S. Patent No. 9,257,492
1002	Certified File History for U.S. Patent No. 9,257,492
1004	World Intellectual Property Organization Published Application No. 2011/036089 A1 (Ingle)
1005	Certified English Translation of World Intellectual Property Organization Published Application No. 2011/036089 A1 (Ingle)
1006	Japanese Patent Application Publication No. JP 2003-317610 (Hasei)
1007	Certified English Translation of Japanese Patent Application No. JP 2003-317610 (Hasei)
1008	U.S. Patent No. 5,691,877 (Hanamura)
1010	U.S. Patent No. 7,817,117
1013	U.S. Patent Publication No. 2009/0178271 (Egitto)
1014	TFT AMOLED Pixel Circuits and Driving Methods, James L. Sanford, et. al., SID 03 DIGEST
1015	Reiji Hattori et al., Current-Writing Active-Matrix Circuit for Organic Light-Emitting Diode Display Using aSi:H Thin-Film-Transistors, IEICE Trans. Electron., Vol.e83-C, No. 5 (May 2000)
1016	U.S. Patent No. 3,997,411 (Muenz)
1017	James W. Nilsson and Susan A. Riedel, Electric Circuits, Addison-Wesley Publishing Co. (5th ed. 1996)
1018	Alan B. Grebene, Bipolar And MOS Analog Integrated Circuit Design, John Wiley & Sons (1983)
1019	IEEE 100, The Authoritative Dictionary of IEEE Standards Terms (7th ed. Dec. 2000)
1020	Jiun-Haw Lee et al., Introduction To Flat Panel Displays, John Wiley & Sons (2008)
1021	Robert A. Street, Technology and Applications of Amorphous Silicon in Materials Science, Vol. 37 (2000)
1022	Gary S. May and Costas J. Spanos, Fundamentals of Semiconductor Manufacturing and Process Control (2006)

Ex.	Description of Exhibit
1023	Bruce E. Kahn, Printing Methods for Printed Electronics, Soc’y For Imagin Sci. & Tech.: NIP24 and Digital Fabrication 15-20 (2008), https://doi.org/10.2352/ISSN.2169-4451.2008.24.1.art00005_1
1024	Ana C. Arias et al., Materials and Applications for Large Area Electronics: Solution-Based Approaches, 110 Chemical Reviews 3-24 (2010)
1031	Merriam-Webster’s Collegiate Dictionary, 11th ed. 2007 (Excerpts)
1032	Merriam-Webster’s Collegiate Dictionary, 11th ed. 2012 (Excerpts)
1033	Transcript of August 20, 2025 Deposition of Dr. P. Morgan Pattison

A. Background and Qualifications

5. My background and qualifications are detailed in my Opening Declaration.

B. Relevant Legal Standards

6. I am not an attorney. I have been instructed by counsel regarding certain aspects of patent law, which were discussed in my Opening Declaration. Ex. 1003, Opening Decl. at ¶¶ 16-30. My understanding of the law remains the same, and I have continued to apply this understanding for purposes of this reply declaration.

C. Level of Ordinary Skill in the Art

7. I have applied the same definition of a person of ordinary skill in the art (“POSITA”) as explained in my Opening Declaration (Ex. 1003, ¶46) for purposes of this reply declaration.

II. Claim Construction

8. I understand that Pictiva has proposed claims constructions for four claim terms, which Dr. Pattison asserts he agrees with, in support of its arguments that Hanamura does not render claims 1, 2, 8, and 16 obvious. Ex. 2001, Pattison Decl. at ¶¶ 90-98; POR at 15-28, 53-62; Ex. 2005, Pattison Suppl. Decl. at ¶¶ 21-31. As discussed below, I disagree with Pictiva's constructions.

9. As explained in my Opening Declaration, I have been informed by counsel that claim words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else, e.g., by acting as their own lexicographer to provide their own special meaning to the terms or by intentionally disclaiming, disavowing, or surrendering any claim scope. Ex. 1003, Opening Decl. at ¶¶ 18-23.

A. *First Electrically Conductive Layer on a Substrate and Second Electrically Conductive Layer on the First Electrically Conductive Layer (Claims 1, 10, and 16)*

10. I understand that Pictiva proposes that the term *first electrically conductive layer on a substrate* should be construed as “electrically conductive material formed on a substrate” and the term *second electrically conductive layer on the first electrically conductive layer* should be construed as “electrically conductive material formed on the first conductive layer.” POR at 16; Ex. 2005, Pattison Suppl. Decl. at ¶¶ 21-22. I also understand that Pictiva argues that:

The Board should interpret these terms to include only the electrically conductive material, and not any areas lacking such material. Nor should it interpret “first electrically conductive layer” to include materials not formed on the substrate or “second electrically conductive layer” to include materials not formed on the first electrically conductive layer.

POR at 16.

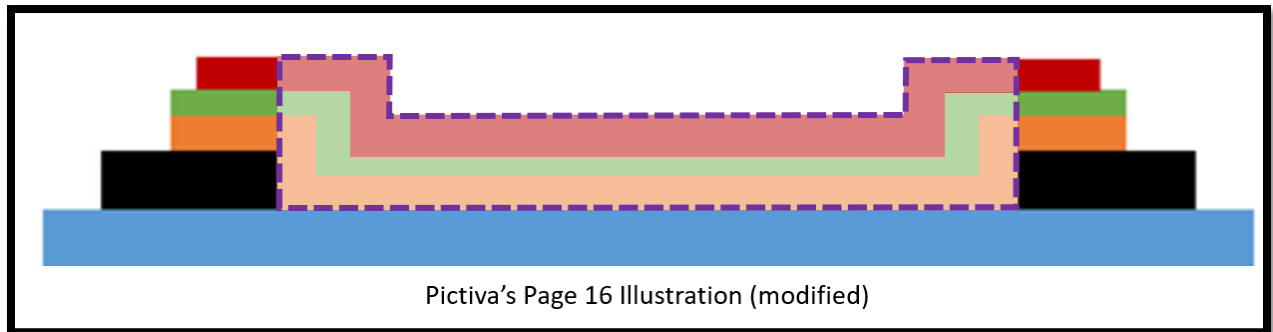
11. I disagree with Pictiva’s proposed constructions for these terms. Essentially, Pictiva is arguing: (1) that the *first electrically conductive layer* must exclude “materials not formed on the substrate” and the *second electrically conductive layer* must exclude “materials not formed on the first electrically conductive layer,” and (2) that the terms “include only the electrically conductive material, and not any areas lacking such material.” *Id.* The ’492 patent’s applicant did not act as his own lexicographer in defining these terms, nor did he disclaim the scope of the claims, let alone this way, and this is not these terms’ plain and ordinary meaning nor how a POSITA would interpret them.

12. The flaws in Pictiva’s construction are demonstrated by its own hypothetical, which divides layers based on what lies beneath each portion, as opposed to how a POSITA would understand a layer’s plain and ordinary meaning:

[I]f the black layer is mapped to the first electrically conductive layer, at least the central portion of the orange,

green, or red layer [shown by the annotated purple dashed-line] is not a second electrically conductive layer because it is not on the black first electrically conductive layer.

POR at 16.



The plain and ordinary meaning of *second electrically conductive layer on the first electrically conductive layer* should not be interpreted so narrowly, and nothing in the '492 patent supports such a construction. Instead, a POSITA would understand that the orange, green, and red layers, in their entirety, each constitute an electrically conductive layer. This is consistent with how a POSITA would expect such a structure to be manufactured. As Dr. Pattison explained, and with which I agree, a POSITA would expect each of the orange, green, and red layers to be deposited in a planar deposition process, one layer at a time. Ex. 1033, Pattison Deposition Tr. at 102:5-105:14. Portions of those layers do not cease to be part of those layers simply because of what lies beneath them.

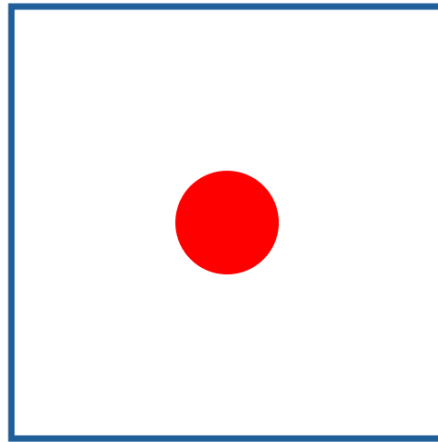
13. Additionally, I disagree with Pictiva and Dr. Pattison's assertion "that some electrically conductive material," should "remain[]" to serve as a bottom electrode

for the OLED,” POR at 20, Ex. 2005, Pattison Suppl. Decl. at ¶29, as justification for why the *second electrically conductive layer* should be limited to only the portions of that layer atop the first. First, independent claims 1 and 16 do not even require an OLED; accordingly, how the layers may hypothetically be structured in conjunction with an OLED should not bear on how the claims are read generally. Second, even if a hypothetical OLED/capacitor structure required that the second electrically conductive layer be formed on the first electrically conductive layer in one region, that does not mean that the second electrically conductive layer needs to be formed on the first electrically conductive layer at all locations, i.e., that it be entirely atop the first electrically conductive layer, as Pictiva and Dr. Pattison suggest.

B. *A First Trench in the First and Second Electrically Conductive Layers (Claims 1 and 16)*

14. I understand that Pictiva proposes that the term *a first trench in the first and second electrically conductive layers* should be construed as “a trench defined by (and thus adjacent to) edges of the electrically conductive material of both the first and second electrically conductive layers.” POR at 21; Ex. 2005, Pattison Suppl. Decl. at ¶¶ 24-25. I disagree with Pictiva’s proposed construction. The ’492 patent’s applicant did not act as his own lexicographer in defining this term, nor did he disclaim the scope of the claims, let alone in this way, and this is not the term’s plain and ordinary meaning nor how a POSITA would interpret it. Read in light of the specification, a POSITA would understand that the plain and ordinary meaning of the term *in* should not be

limited so narrowly to require the trench to be “defined by (and thus adjacent to) edges of the electrically conductive material of both the first and second electrically conductive layers.” Indeed, *in* is a nontechnical word with a commonly understood meaning, i.e., “used as a function word to indicate inclusion, location, or position within limits.” Ex. 1031, Merriam-Webster Collegiate Dictionary, 11th ed. 2007 at 627; Ex. 1032, Merriam-Webster Collegiate Dictionary, 11th ed. 2012 at 627 (same). For example, just as the red circle below is *in* (i.e., positioned within the limits of) the blue square without being “defined by (and thus adjacent to)” the square’s walls, *a first trench* can be *in the first and second electrically conductive layers* without being “defined by (and thus adjacent to)” those layers’ edges.



C. *Forming a First Trench* (Claim 1)

15. I understand that Pictiva proposes that the term *forming a first trench* should be construed as “requir[ing] the creation of something that did not previously exist,” and “requir[ing] the creation of a trench by removing certain portions of the

previously formed first and second electrically conductive layers.” POR at 24. I disagree with Pictiva’s proposed construction. The ’492 patent’s applicant did not act as his own lexicographer in defining this term, nor did he disclaim the scope of the claims, let alone in this way, and this is not the term’s plain and ordinary meaning nor how a POSITA would interpret it. Read in light of the specification, a POSITA would understand that *forming’s* plain and ordinary meaning in the context of semiconductor manufacturing includes not only subtractive processes like removal, but also additive processes. Accordingly, a POSITA would understand that *forming a first trench* includes *forming* the *first trench* via both subtractive processes (e.g., etching down into preexisting material to form the trench) as well as via additive processes (e.g., depositing material with predetermined spacing therebetween, such that a trench is formed between the two deposits).

III. Ground I: Claims 1, 2, 8-11 and 16 of the ’492 Patent Are Rendered Obvious By Ingle in View of Hasei

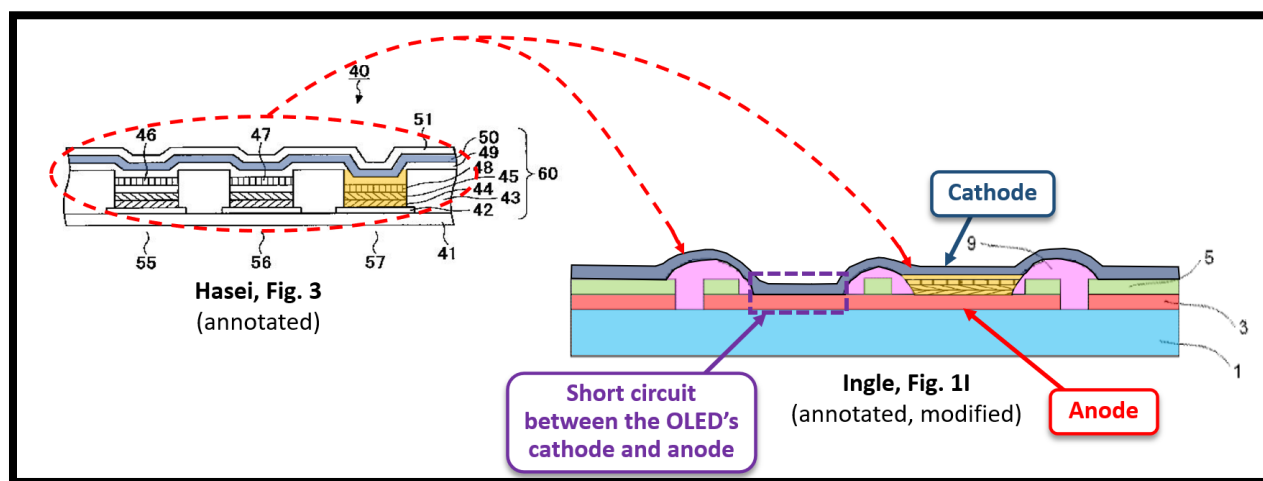
16. I understand that Pictiva and Dr. Pattison dispute that Ingle in view of Hasei renders obvious claims 1, 2, 8-11, and 16. Ex. 2001, Pattison Decl. at ¶¶ 63-89; POR at 28-51; Ex. 2005, Pattison Suppl. Decl. at ¶¶ 10-16. I disagree. Ingle and Hasei render these claims obvious for the reasons I explained in my Opening Declaration. Ex. 1003 at ¶¶ 108-217. I have been asked to respond to certain arguments Pictiva and Dr. Pattison provide regarding this combination. I address these arguments below.

17. First, I understand that Pictiva and Dr. Pattison assert that a POSITA would not be motivated to use Hasei's droplet discharge method to form *an electrically conductive electrode layer in a structured fashion* (limitations 1[e], 10[f]-[1], 16[e]) because Ingle's "conventional process" is limited to "lithography." POR at 31; Ex. 2001, Pattison Decl. at ¶ 66. I disagree. Hasei was published in 2003, and its droplet discharge method would have been conventional by the time Ingle was published five years later, and even more so by the '492 patent's claimed 2012 priority date. Ex. 1007, Hasei at Cover; Ex. 1005, Ingle at Cover; '492 patent, Cover. Semiconductor manufacturing was a rapidly advancing field in the early 2000s, such that techniques that were novel in 2003 would have become conventional five, or especially nine, years later. Indeed, Ingle contemplates applying layers, including its electrode regions, via "printing, by deposition with the aid of SAMs (self-assembling monolayers) and the like," Ex. 1005, Ingle at 6:9-23, evidencing that Ingle itself contemplated the use of Hasei's droplet discharge method (which is a form of printing).

18. Second, I understand that Pictiva and Dr. Pattison assert that Hasei does not disclose depositing its negative electrode 50 in a structured fashion based on Hasei's Figure 3. Ex. 2001, Pattison Decl. at ¶ 53; POR at 34-35. I disagree. As I previously explained, the text of Hasei teaches that "negative electrode 50 may be formed by the droplet discharging method." Ex. 1007, Hasei at [0037]. Notably, Figure

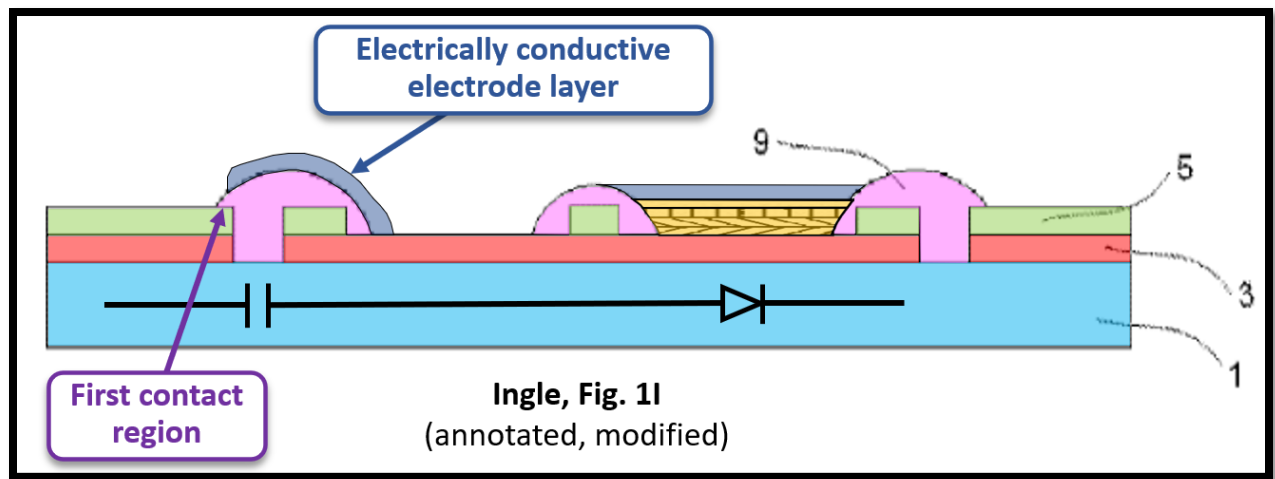
3 is a two-dimensional cross-section lacking a planar view. As such, one cannot determine, based on Figure 3 alone, whether negative electrode 50 is structured.

19. Moreover, a POSITA would understand that applying negative electrode 50 in a planar fashion to the device in Ingle would create a short circuit between the OLED's anode and cathode, as illustrated below.



Such a planar application would therefore require subsequent etching in order to remove the overlap that creates the short circuit. However, a POSITA would understand that etching, e.g., photolithography, should not be used after the organic layers of an OLED have been deposited—e.g., when forming a cathode atop the OLED—as photolithography can damage the organic layers. *See, e.g.*, Ex. 1023, Kahn at 16 (“The harsh conditions required for dissolving resists, etching the underlying layers, and removing the photoresist will destroy the activity of most organic electronic materials.”).

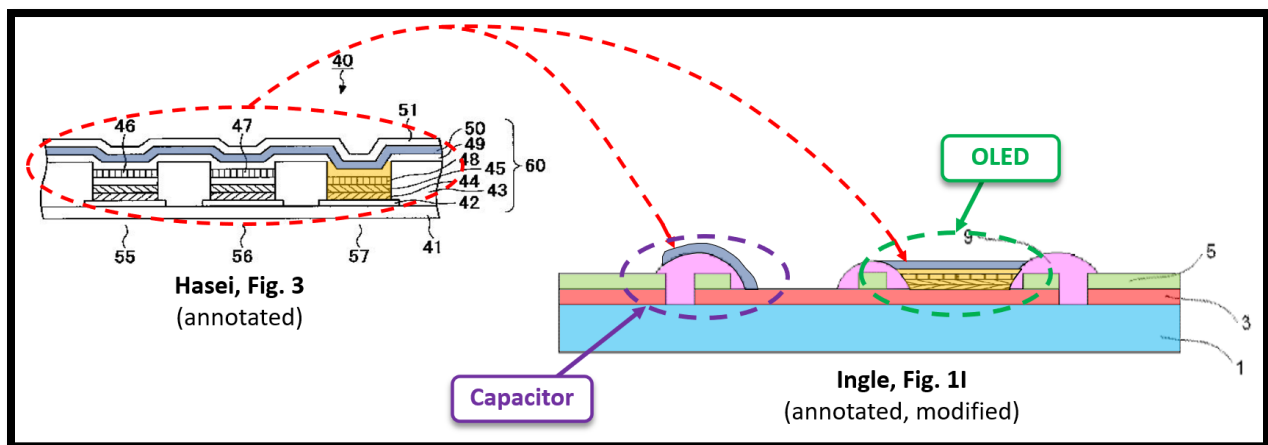
20. Third, I understand that Pictiva and Dr. Pattison assert that Ingle in view of Hasei does not render obvious *applying an electrically conductive electrode layer ... above the first contact region*, because they assert that the electrode does not overlap Ingle's first contact region. Ex. 2001, Pattison Decl. at ¶ 83; POR at 42-43. I disagree. First, as explained in my Opening Declaration, Ingle, as modified by Hasei, results in a device wherein the *electrically conductive electrode layer* does overlap *the first contact region*, as illustrated below.



Ex. 1003, Opening Decl. at ¶¶ 161-171. Second, as I also explained in my Opening Declaration, a POSITA “would understand that the degree to which both the dielectric (pink) and the electrically conductive layer (grey) extend over the first contact region may be adjusted to fine-tune the capacitance of the capacitor.” Ex. 1003, Opening Decl. at ¶ 167. A POSITA would understand that the capacitance of a capacitor in an AMOLED display may need to be fine-tuned for a number of reasons, e.g., to meet capacitance requirements for individual pixel circuits.

21. Fourth, I understand that Pictiva asserts that Ingle discloses that its dielectric is “steeply curved.” POR at 50. I disagree. A POSITA would not expect Ingle’s dielectric to be “steeply curved” in a real-world implementation of Ingle’s teachings. Instead, a POSITA would understand that Ingle’s figures are simplified representations and would not be representative, or limiting, of what real-world components would look like. Indeed, Ingle explains as such, stating that the “present invention is illustrated below without limiting the generality with reference to the figures.” Ex. 1005, Ingle at 18:21-22. Moreover, a POSITA would likewise understand that the processes for forming the dielectric could be readily adjusted to change how rounded, if at all, the dielectric is.

22. Fifth, I understand that Pictiva asserts that I did not explain why a POSITA would apply Hasei’s negative electrode 50 above the dielectric in Ingle’s first contact region as depicted below. POR at 46 (citing Ex. 1003, Opening Decl. at ¶ 162). I disagree.



As explained in my opening declaration, it would have been obvious to form a capacitor alongside the OLED. Ex. 1003, Opening Decl. at ¶¶ 120–125. As also explained, capacitors are elements comprising two conductors separated by an insulator or dielectric material. Ex. 1003, Opening Decl. at ¶ 76; Ex. 1017, Nilsson at 221. As further explained, Ingle’s “conductive material deposited on the substrate functions as one plate, while the electrically conductive layer deposited on the dielectric [(Hasei’s negative electrode 50)] functions as the second plate.” Ex. 1003, Opening Decl. at ¶ 167. That is, Ingle’s base structure already includes a location alongside where it proposes building its OLED that contains two of the three components necessary to form a capacitor (the first plate and the dielectric) such that applying Hasei’s negative electrode 50 to this location (i.e., above the dielectric in Ingle’s first contact region) to form the capacitor—which would then be in series with the OLED—would have been obvious. *Id.*, ¶162. Because two of the three capacitor components were already present, forming the capacitor here would have the added benefit of being done in the same manufacturing step as the cathode of the OLED, thus saving time and costs, which would have only made it more desirable to do so. *Id.*, ¶170.

IV. Ground II: Claims 1, 2, 8, and 16 Are Rendered Obvious Based on Hanamura

23. I understand that Pictiva and Dr. Pattison dispute that Hanamura renders obvious claims 1, 2, 8, and 16. Ex. 2001, Pattison Decl. at ¶¶ 90-98; POR at 51-62; Ex.

2005, Pattison Suppl. Decl. at ¶¶ 17-31. I disagree. Hanamura renders these claims obvious for the reasons I explained in my Opening Declaration. Ex. 1003, Opening Decl. at ¶¶ 218-256. I have been asked to respond to certain arguments Pictiva and Dr. Pattison provide regarding this ground. I address these arguments below.

24. First, I understand that Pictiva and Dr. Pattison argue that “Hanamura’s thick film capacitor formed on an insulating chip for the express purpose of soldering onto circuit boards differs dramatically from the integral capacitors and other electronic components contemplated by the ’492 patent.” POR at 52; Ex. 2005, Pattison Suppl. Decl. at ¶¶ 18-20. I disagree. The claims do not specify a specific size nor require “integral capacitors,” and Dr. Pattison does not cite any evidence supporting his assertion that “[t]his dramatic difference in size and scale is relevant.” Ex. 2005, Pattison Suppl. Decl. at ¶ 20.

25. Second, I understand that Pictiva and Dr. Pattison argue that Hanamura’s *first trench* (predetermined spacing) is only in the *second electrically conductive layer* (electrodes 14, 20) and not the *first electrically conductive layer* (electrodes 12, 13). POR at 60; Ex. 2001, Pattison Decl. at ¶¶ 95; Ex. 2005, Pattison Suppl. Decl. at ¶¶ 27. I disagree. If Hanamura’s *first trench* was not in the *first electrically conductive layer*, electrodes 12 and 13 would touch and therefore short-circuit, causing Hanamura’s capacitor to become inoperable.

V. Ground III: Claims 3, 5, and 6 Are Rendered Obvious Based on Hanamura in View of Egitto

26. I understand that Pictiva and Dr. Pattison assert that I did not “provide any specific motivation to combine the teachings of Hanamura with the specific ‘representative pattern[] described in Egitto.” POR at 64; Ex. 2001, Pattison Decl. at ¶ 101. I disagree. As explained in my Opening Declaration:

A POSITA would have been motivated to combine Hanamura and Egitto because (1) Hanamura contemplates incorporation of a resistor having a “reliably adjusted resistance” ... while teaching that resistance may be adjusted by altering the resistor’s dimensions; and (2) Egitto illustrates adjusting resistance by trimming or making other alterations to the shape and size of the resistance material. Thus, using the design from Egitto in the electrically conductive layers of Hanamura would involve nothing more than applying a known technique to a known device ready for improvement to yield predictable results.

Ex. 1003, Opening Decl. at ¶ 257. As further discussed in my Opening Declaration, Hanamura illustrated a resistor with a reliably adjusted resistance in its second embodiment, and taught that the resistance could be adjusted by trimming a groove 30A to change the resistor’s dimensions. Ex. 1003, Opening Decl. at ¶ 259; Ex. 1008, Hanamura at 5:63-7:39. Egitto also taught a specific method and design (using

formulas which would have been well-known to a POSITA) that would have enabled a POSITA to alter resistance by removing material to form a precise path for current flow. Ex. 1003, Opening Decl. at ¶ 267; Ex. 1013, Egitto at [0069]-[0073]. For example, as I explained:

Egitto teaches that this groove 30A may be formed into specific, preferable patterns using a layer. Carving this groove would result in a predictable change to resistance, as resistance is directly computable from the resistivity and dimensions of the material via a well-known formula.... Indeed, Egitto teaches this very line of reasoning, stating that its method “enables the circuit designer to alter the resulting resistance by selectively removing ... material and leaving a desired, precise width thereof remaining as the current path.” Ex. 1013, Egitto at [0082].

Ex. 1003, Opening Decl. at ¶ 269. Indeed, Egitto only discloses two adjustable resistor patterns to use in this configuration—Figures 7 and 8. A POSITA would recognize that they could choose between these patterns. Moreover, Egitto’s Figure 8 pattern avoids 90-degree angles that could negatively affect the resistance by causing current crowding.

* * *

27. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and

further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

September 3, 2025
Date



Alex Kattamis, Ph.D., P.E.