

**UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD**

SAMSUNG DISPLAY CO., LTD.
Petitioner,
v.
PICTIVA DISPLAYS INTERNATIONAL LTD.
Patent Owner.

IPR2024-01187

November 19, 2025



pictivadisplays

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Pictiva EX2008
Samsung v Pictiva
IPR2024-01187

Pictiva Slide 1

U.S. Patent No. 9,257,492 (the '492 Patent)

US009257492B2

(12) **United States Patent**
Ingle

(10) **Patent No.:** **US 9,257,492 B2**
(45) **Date of Patent:** **Feb. 9, 2016**

(54) **METHOD FOR PRODUCING A PASSIVE ELECTRONIC COMPONENT, METHOD FOR PRODUCING AN OPTOELECTRONIC ASSEMBLY AND PASSIVE ELECTRONIC COMPONENT**

(71) Applicant: **OSRAM OLED GmbH, Regensburg (DE)**

(72) Inventor: **Andrew Ingle, Allershausen (DE)**

(73) Assignee: **OSRAM OLED GmbH, Regensburg (DE)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/430,942**

(22) PCT Filed: **Aug. 20, 2013**

(86) PCT No.: **PCT/EP2013/067348**
§ 371 (c)(1),
(2) Date: **Mar. 25, 2015**

(87) PCT Pub. No.: **WO2014/048639**
PCT Pub. Date: **Apr. 3, 2014**

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(30) **Foreign Application Priority Data**
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H01L 21/8222 (2006.01)
H01L 29/00 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC **H01L 27/3225** (2013.01); **H01G 4/005** (2013.01); **H01G 4/33** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 23/5227; H01L 27/0658
USPC 438/329, 957; 257/528, 532
See application file for complete search history.

(56) **References Cited**
U.S. PATENT DOCUMENTS
6,335,211 B1 * 1/2002 Lee 438/22
6,800,999 B1 * 10/2004 Duggal et al. 315/169.1
(Continued)

FOREIGN PATENT DOCUMENTS
DE 102009060066 A1 3/2011
DE 112008003787 T5 3/2012

German Search
0(5 pages) date:
Primary Exam
(74) *Attorney*
Partner

(57) Various embodiments of a passive electronic component, comprising a substrate, a first electrically conductive layer, a second electrically conductive layer, a first trench, a dielectric, and an electrically conductive electrode layer.

Fig. 4

1. A method for producing a passive electronic component, comprising:
forming a first electrically conductive layer on a substrate,
forming a second electrically conductive layer on the first electrically conductive layer,
forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region,
applying a dielectric in a structured fashion to the second electrically conductive layer in the first contact region and at least partly to the substrate in the first trench such that the dielectric electrically insulates the first contact region from the second contact region, and
applying an electrically conductive electrode layer in a structured fashion to the dielectric above the first contact region and to the second contact region.

U.S. Patent No. 9,257,492 (the '492 Patent)

(12) United States Patent		(10) Patent No.: US 9,257,492 B2
Ingle		(45) Date of Patent: Feb. 9, 2016
(54) METHOD FOR PRODUCING A PASSIVE ELECTRONIC COMPONENT, METHOD FOR PRODUCING AN OPTOELECTRONIC ASSEMBLY AND PASSIVE ELECTRONIC COMPONENT	(58) Field of Classification Search CPC H01L 23/5227; H01L 27/0658 USPC 438/329, 957; 257/528, 532 See application file for complete search history.	
(71) Applicant: OSRAM OLED GmbH, Regensburg (DE)	(56) References Cited U.S. PATENT DOCUMENTS 6,335,211 B1 * 1/2002 Lee 438/22 6,800,999 B1 * 10/2004 Duggal et al. 315/169.1 (Continued)	
(72) Inventor: Andrew Ingle, Allershausen (DE)	FOREIGN PATENT DOCUMENTS DE 102009060066 A1 3/2011 DE 112008003787 T5 3/2012 OTHER PUBLICATIONS German Search Report based on Application No. 10 2012 109 142. 0(5 pages) dated Jun. 25, 2013. Primary Examiner — Theresa T Doan (74) Attorney, Agent, or Firm — Viering, Jentschurn & Partner	
(73) Assignee: OSRAM OLED GmbH, Regensburg (DE)	(57) ABSTRACT Various embodiments may relate to a method for producing a passive electronic component, including forming a first electrically conductive layer on a substrate, forming a second electrically conductive layer on the first electrically conductive layer, forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region, applying a dielectric in a structured fashion to the second electrically conductive layer in the first contact region and at least partly to the substrate in the first trench such that the dielectric electrically insulates the first contact region from the second contact region, and applying an electrically conductive electrode layer in a structured fashion to the dielectric above the first contact region and to the second contact region.	
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(87) PCT Pub. No.: WO2014/048639 PCT Pub. Date: Apr. 3, 2014		
(65) Prior Publication Data US 2015/0255521 A1 Sep. 10, 2015		
(30) Foreign Application Priority Data Sep. 27, 2012 (DE) 10 2012 109 142		
(51) Int. Cl. H01L 21/8222 (2006.01) H01L 29/00 (2006.01) (Continued)		
(52) U.S. Cl. CPC H01L 27/3225 (2013.01); H01G 4/005 (2013.01); H01G 4/33 (2013.01); (Continued)		
18 Claims, 6 Drawing Sheets		

16 28 38 18 28 38 50 54 28 14 12 10

10. A method for producing an optoelectronic assembly, comprising:

forming a passive electronic component,

the passive electronic component, comprising:

a first electrically conductive layer on a substrate,

a second electrically conductive layer on the first electrically conductive layer,

a first trench formed in the first and second electrically conductive layers,

wherein the first trench separates a first contact region from a second contact region,

a dielectric, which is applied in a structured fashion to the second electrically conductive layer in the first contact region and at least partly on the substrate in the first trench such that the dielectric electrically insulates the first contact region from the second contact region, and an electrically conductive electrode layer, which is applied in a structured fashion to the dielectric above the first contact region and to the second contact region,

applying the dielectric in a structured fashion to the second layer such that the dielectric demarcates a component region for forming an optoelectronic component relative to the second contact region,

forming an optically functional layer in the component region, and

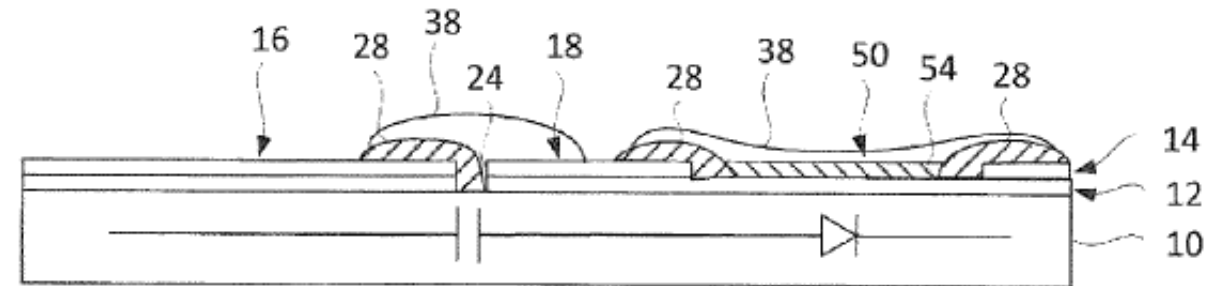
applying the electrode layer in a structured fashion such that a part of the electrode layer covers the optically functional layer.

U.S. Patent No. 9,257,492 (the '492 Patent)

The fact that the dielectric and/or the electrode layer and/or subsequently further layers or materials are “applied in a structured fashion” means, in various embodiments, that the desired structure is already formed during the application of the corresponding layer. The area to be coated is thus coated only in partial regions dependent on the desired structure.

This is in contrast to planar application of the corresponding layers and subsequent structuring of the layers, as is the case for example in a photolithographic method. The structured application of the layers makes it possible to be able to dispense with the firstly planar application of the corresponding layers and the subsequent complex structuring of the layers, for example the photolithographic method, and/or an expensive photoresist for the photolithographic method. This contributes to simple and/or cost-effective production of the passive electronic component.

Fig. 16



CLAIM CONSTRUCTION

- “electrically conductive layer” terms
- “a first trench in the first and second electrically conductive layers”
- “forming a first trench”

Petitioner Does Not Dispute Plain and Ordinary Meaning Constructions Proposed by Patent Owner

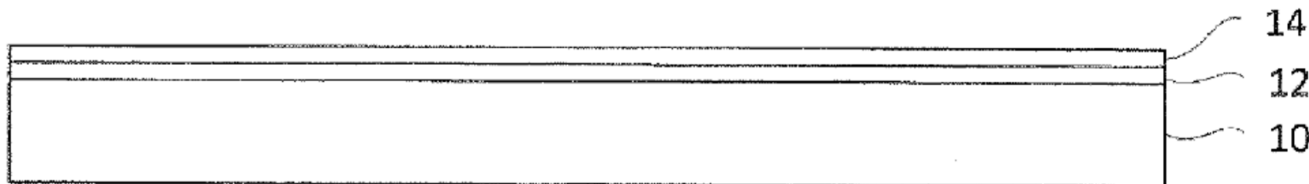
Pictiva initially purports to apply the “plain and ordinary meaning” by replacing *layer* with “material formed”:

[forming] a first electrically conductive ~~layer~~ material formed on a substrate,

[forming] a second electrically conductive ~~layer~~ material formed on the first electrically conductive layer,

**Samsung Offers No
Proposed Constructions**

Fig. 3



Petitioner Disputes the Logical Implications of Those Constructions

Samsung disagrees with the logical results that:

(1) *first electrically conductive layer* must exclude “materials not formed on the substrate” and *second electrically conductive layer* must exclude “materials not formed on the first electrically conductive layer,” and
(2) the terms “include only the electrically conductive material, and not any areas lacking such material.”

Samsung’s arguments fail because:

- 1. They would read “electrically conductive” and “on” out of the claim terms; and**
- 2. Samsung does not dispute that *every* disclosed embodiment is consistent with Pictiva’s construction.**

Petitioner Does Not Dispute That Pictiva's Construction Is Consistent with Every Disclosed Embodiment



“An explicit definition is not required to inform a claim term’s meaning. ... We have held that a patent’s repeated and consistent description of a claim term may inform its construction.”

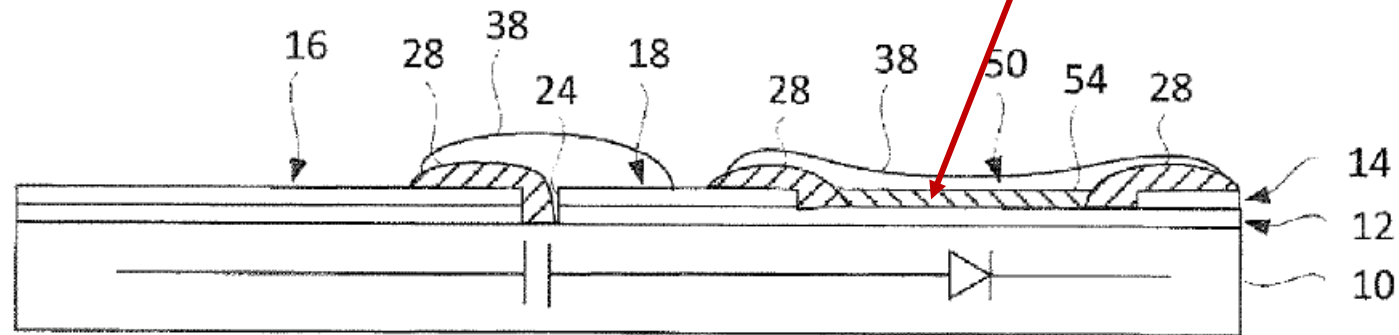
Groove Digital, Inc. v. United Bank, 825 F. App’x 852, 856 (Fed. Cir. 2020) (collecting cases)

The Claim 11 Embodiment Further Supports Pictiva's Construction

11. The method as claimed in claim 10, wherein before the optically functional layer is applied, the second electrically conductive layer is removed in the component region and the optically functional layer is applied to the first electrically conductive layer in the component region.

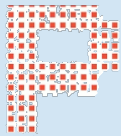
Samsung fails to sufficiently address the importance of the overlapping layers or explain how a layer can be “removed” in a region consistent with its arguments.

Fig. 16



Unrebutted Expert Testimony Establishes the Importance of the Second Layer Being “On” the First Layer

Dr. Pattison
Expert Witness



pictivadisplays

The '492 Patent explains that the material for the first electrically conductive layer “can withstand an etching process ... for removing a second electrically conductive material.” *Id.* at 10:10-14. Having a first electrically conductive layer with that property below the second electrically conductive layer ensures that sufficient electrically conductive material (i.e., the first layer) remains to serve as the bottom electrode for the OLED or other optically functional layer applied in the component region. Otherwise, the etching process (*see, e.g., id.* at 14:19-24) would remove all electrically conductive material necessary for the bottom electrode and thus the operation of the OLED or other optically functional layer.

EX2005, ¶ 29; EX1001, 14:15-64, Figs. 14-16, Claim 11; POR 20-21

CLAIM CONSTRUCTION

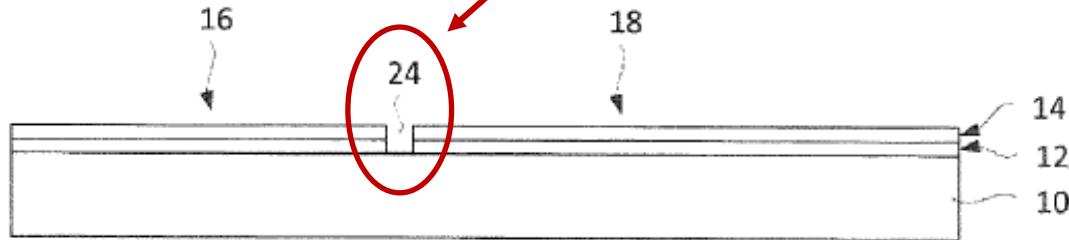
- “electrically conductive layer” terms
- “a first trench in the first and second electrically conductive layers”
- “forming a first trench”

Pictiva's Construction Is Consistent with Fig. 4 and Every Other Embodiment

Samsung Offers No Proposed Construction

Pictiva's Proposed Construction: "a trench defined by (and thus adjacent to) edges of the electrically conductive material of both the first and second electrically conductive layers"

Fig. 4



laser ablation, for example. The material of the substrate 10 is exposed in the first trench 24. In other words, a depth of the first trench corresponds to a common thickness of the two electrically conductive layers 12, 14. By way of example, a laser operated continuously or in a pulsed fashion, for

Again, Petitioner Does Not Dispute That Pictiva's Construction Is Consistent with Every Disclosed Embodiment

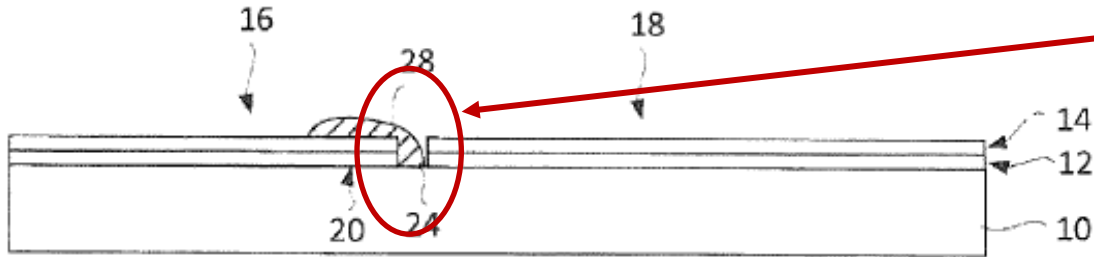


“An explicit definition is not required to inform a claim term’s meaning. ... We have held that a patent’s repeated and consistent description of a claim term may inform its construction.”

Groove Digital, Inc. v. United Bank, 825 F. App’x 852, 856 (Fed. Cir. 2020) (collecting cases)

Pictiva's Construction Required by Claim 9, Fig. 6, and Numerous Embodiments

Fig. 6

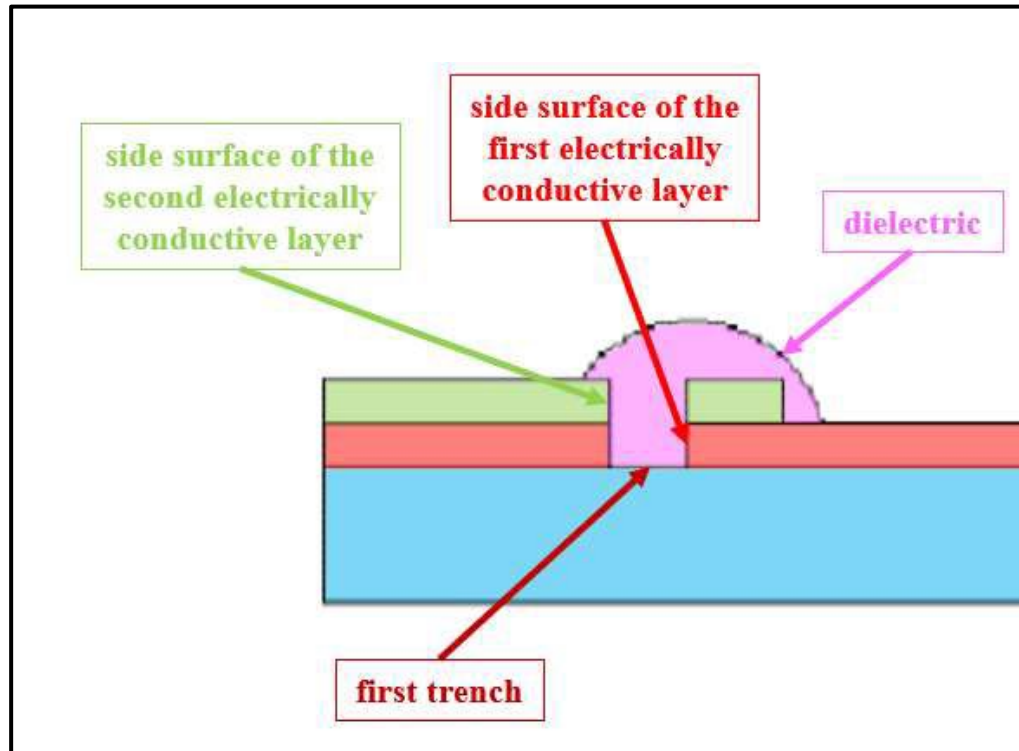


The Encapsulation Step Requires Edges and/or Side Surfaces of the First and Second Electrically Conductive Layers

9. The method as claimed in claim 1, wherein the dielectric firstly is applied in a structured fashion to the second electrically conductive layer in such a way that it adjoins the first trench, and wherein then the dielectric is heated in such a way that it deforms and encapsulates edges and/or side surfaces of the first and second electrically conductive layers in the first trench.

In various embodiments, the dielectric firstly is applied in a structured fashion to the second electrically conductive layer in such a way that the dielectric adjoins the first trench, and is then heated in such a way that it deforms and encapsulates edges and/or side surfaces of the first and second electrically conductive layers in the first trench. The dielectric adjoining the trench flows on account of the heating over these exposed edges and/or side surfaces of the first and second electrically conductive layers and encapsulates them.

The Petition Itself Reflects Pictiva's Understanding of Claim 9



Ingle discloses heating the dielectric so that it deforms and encapsulates edges

/ side surfaces of the first and second electrically conductive layers in the first trench.

For example, Ingle discloses that “[t]he substrate 1 or the insulator 9 is then heated directly such that the insulator 9 softens (reflow) and flows over the open edges of the second electrically conductive layer 5 and the first electrically conductive layer 3,” as shown in Figure 1I. Ingle, 21:27-30; *see, id.*, 20:20-22 (“The insulator 9 should be selected so that it can be softened by subsequent treatment and brought into a flowable state.”); Ex.1003, ¶210. As shown in Figure 1I below, the dielectric (pink)

encapsulates edges and/or side surfaces of the first and second electrically conductive layers (red and green, respectively) in the first trench.

Claim Differentiation Does Not Compel Samsung's Interpretation



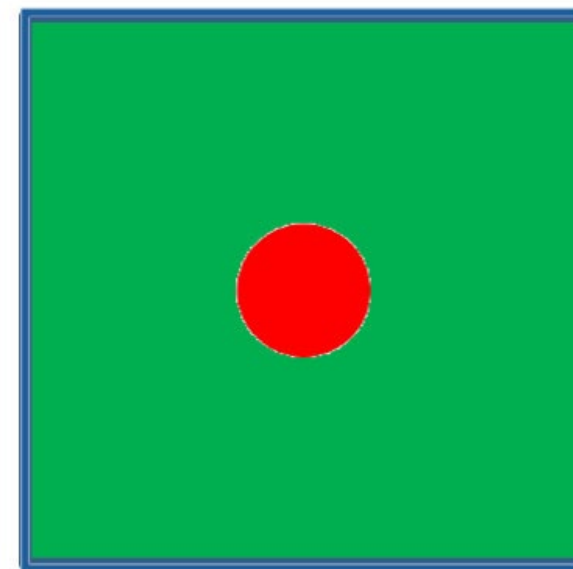
“That presumption is especially strong when the limitation in dispute is the ***only meaningful difference*** between an independent and dependent claim, and one party is urging that the limitation in the dependent claim should be read into the independent claim.”

SunRace Roots Enter. Co. v. SRAM Corp., 336 F.3d 1298, 1303 (Fed. Cir. 2003) (emphasis added)

Samsung's Circular "Square" Analogy Is Inapt

Samsung argues that the red circle is "in" the blue square without being defined by (and thus adjacent to) the square's walls. But here:

- 1. The layers are made of electrically conductive material; they are not an outline with "walls";**
- 2. Being "in" such a layer requires being adjacent to such material consistent with Pictiva's proposed construction (i.e., the green area is part of the square); and**
- 3. Samsung does not explain how a "trench" can be formed "in" a layer without being defined by (and thus adjacent to) the material of that layer.**



Petitioner Improperly Focuses on the Word “in” in the Abstract



“The customary meaning of a claim term is not determined in a vacuum and should be harmonized, to the extent possible, with the intrinsic record, as understood within the technological field of the invention.”

Lexion Med., LLC v. Northgate Techs., Inc., 641 F.3d 1352, 1356 (Fed. Cir. 2011)

CLAIM CONSTRUCTION

- “electrically conductive layer” terms
- “a first trench in the first and second electrically conductive layers”
- “forming a first trench”

The Plain Claim Language Compels Pictiva's Construction

The plain and ordinary meaning of the claim language requires the creation of a trench by removing certain portions of the previously formed first and second electrically conductive layers.

1. A method for producing a passive electronic component, comprising:

forming a first electrically conductive layer on a substrate,

forming a second electrically conductive layer on the first electrically conductive layer,

forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region,

applying a dielectric in a structured fashion to the second electrically conductive layer in the first contact region and at least partly to the substrate in the first trench such that the dielectric electrically insulates the first contact region from the second contact region, and

applying an electrically conductive electrode layer in a structured fashion to the dielectric above the first contact region and to the second contact region.

Fig. 2

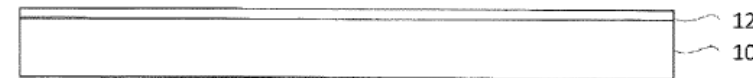


Fig. 3

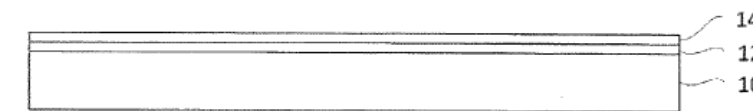
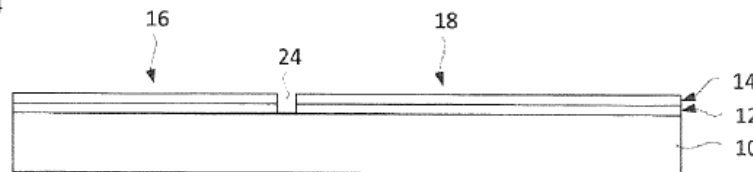


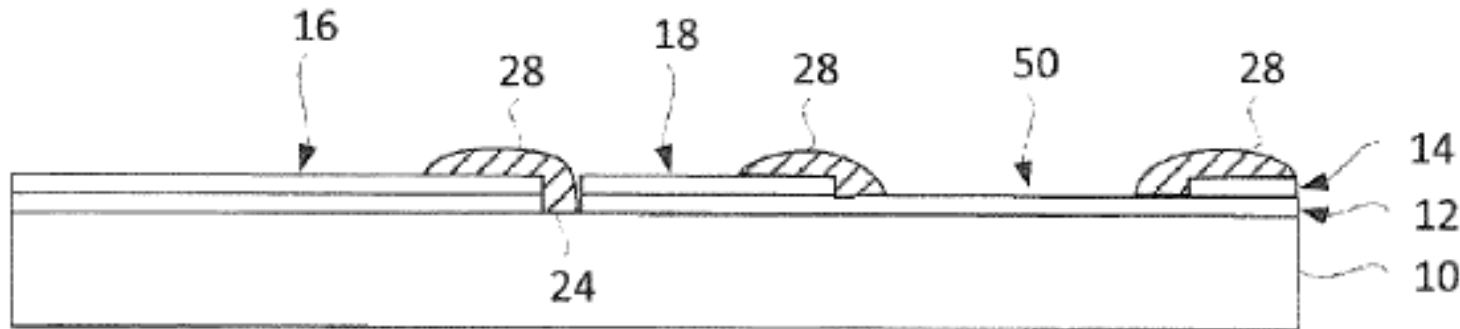
Fig. 4



In Contrast to Other Claim Terms Describing Simultaneous Performance

applying the dielectric in a structured fashion to the second layer such that the dielectric demarcates a component region for forming an optoelectronic component relative to the second contact region,

Fig. 15



Federal Circuit Precedent Requires Ordered Performance of Claim Steps Here



“Although not an ironclad rule, when the current step of a method claim refers to a previous step using the definite article ‘the,’ the claim language indicates that the previous step occurs sequentially before the current step.”

Medtronic, Inc. v. Teleflex Life Scis. Ltd., No. 2022-1605, 2024 WL 1208642, at *3 (Fed. Cir. Mar. 21, 2024)
(citing *Wi-Lan, Inc. v. Apple, Inc.*, 811 F.3d 455, 462 (Fed. Cir. 2016))

“As a matter of logic, a mailbox must be established before the contents of said mailbox can be transmitted.”

Mformation Techs., Inc. v. Rsch. in Motion Ltd., 764 F.3d 1392, 1400 (Fed. Cir. 2014)

“[P]rocessing” an “electronic advertisement” necessarily indicates that “the creation of the ad must happen before the processing begins.”

Function Media, L.L.C. v. Google, Inc., 708 F.3d 1310, 1320 (Fed. Cir. 2013)

And Again, Petitioner Does Not Dispute That Pictiva's Construction Is Consistent with Every Disclosed Embodiment



Like *Wi-Lan*: “The *ordering requirement* described above is *consistent with the specification*. Every embodiment discussed in the specification randomizes the data symbols before combining them. ... No disclosure in the specification depicts or discusses the possibility of combining before randomizing. The intrinsic record is therefore clear that the asserted claims cover only structure that randomizes data symbols in parallel before combining them for transmission.”

Wi-Lan, Inc. v. Apple, Inc., 811 F.3d 455, 462 (Fed. Cir. 2016) (emphasis added)

Unlike *Moba*: “[T]he *specification explicitly describes simultaneous performance* of guiding steps two and three.”

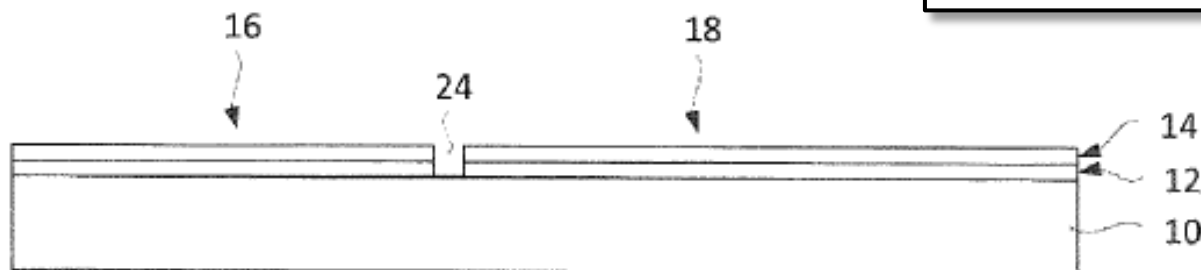
Moba, B.V. v. Diamond Automation, Inc., 325 F.3d 1306, 1314 (Fed. Cir. 2003) (emphasis added)

Pictiva's Construction Is Consistent with Every Disclosed Embodiment

The trench can be formed by laser ablation, for example. Furthermore, the trench can extend partly or completely around the first contact region and/or the second contact region. Furthermore, even further trenches can be formed and/or the trenches can be part of a trench structure extending two-dimensionally in a plane.

FIG. 4 shows the substrate 10 and the first and second electrically conductive layers 12, 14, wherein one embodiment of a first trench 24 is formed in the two electrically conductive layers 12, 14. The first trench can be formed by laser ablation, for example. The material of the substrate 10 is exposed in the first trench 24. In other words, a depth of the first trench corresponds to a common thickness of the two electrically conductive layers 12, 14. By way of example, a laser operated continuously or in a pulsed fashion, for example a femto-, nano- or pico-laser, can be used for the laser ablation. The laser can emit for example electromagnetic radiation in the IR range or in the UV range, for example at 200 to 300 nm, and/or with a power of 0.5 W to 1 W.

Fig. 4



Claim 1 Encompasses Etching, Which Likewise Requires Removal of Material

In various embodiments, at least one of the trenches is formed by laser ablation. This can contribute to the simple and cost-effective production of the passive electronic component. By way of example, an etching process for etching the trench can be dispensed with.

or ITO-Ag-ITO multilayers. The first electrically conductive material of the first electrically conductive layer 12 can be chosen for example such that it can withstand an etching process (explained below) for removing a second electrically conductive material (explained below).

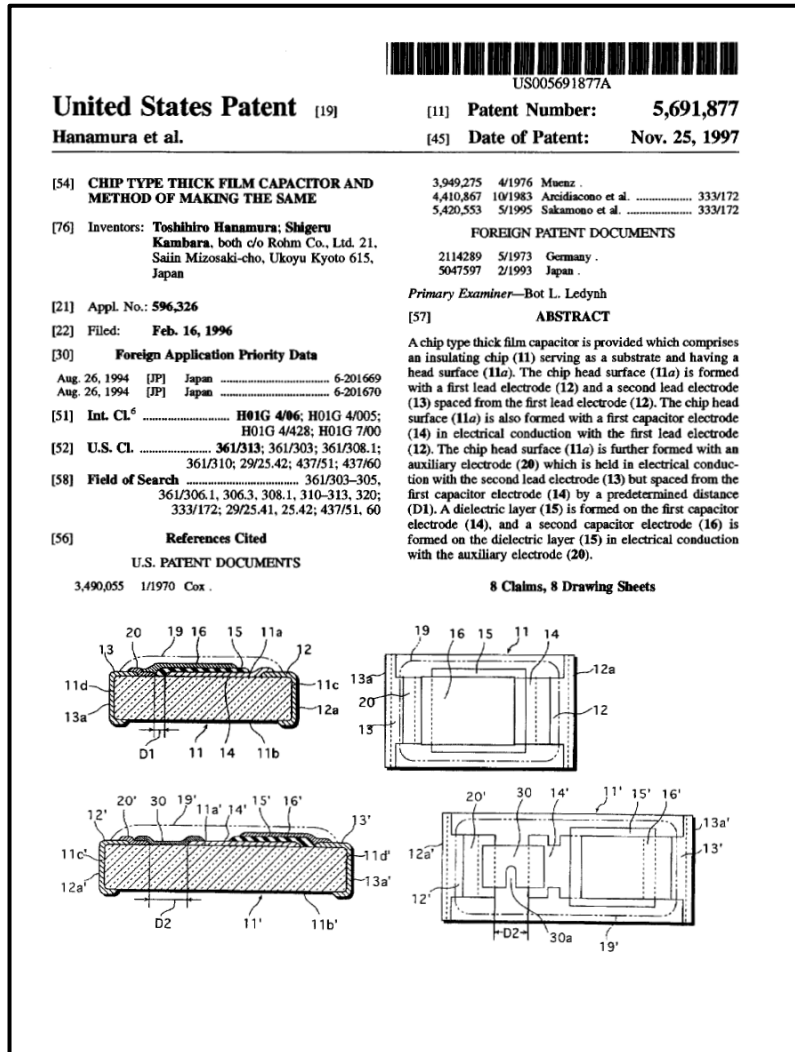
In a further development of the method according to the invention, the method according to the two preceding alternatives comprises removing the first electrically conductive material (step E)) or removing the first electrically conductive material and the second electrically conductive material (step F)) by laser ablation.

GROUND 2: Hanamura

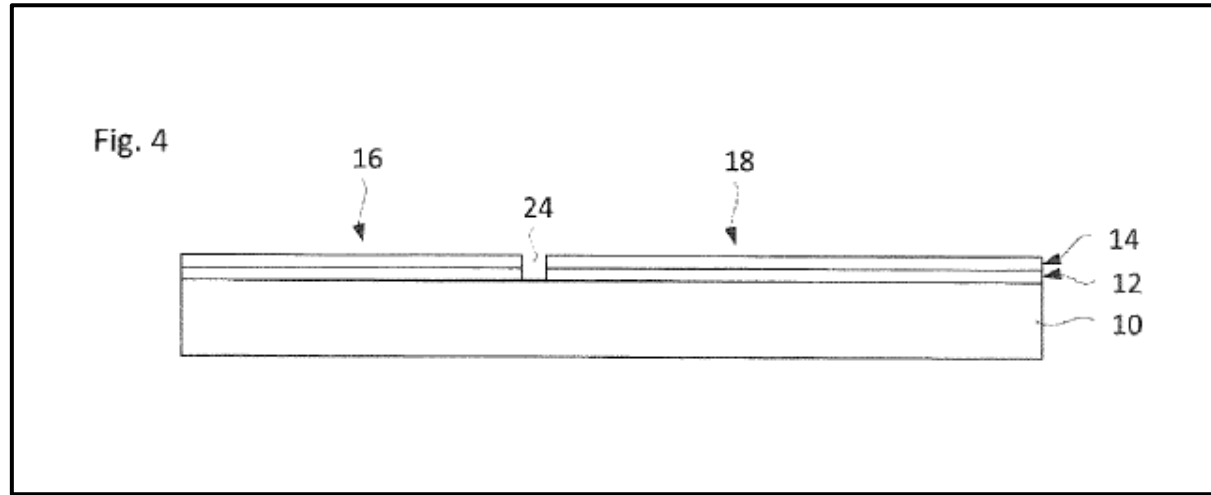
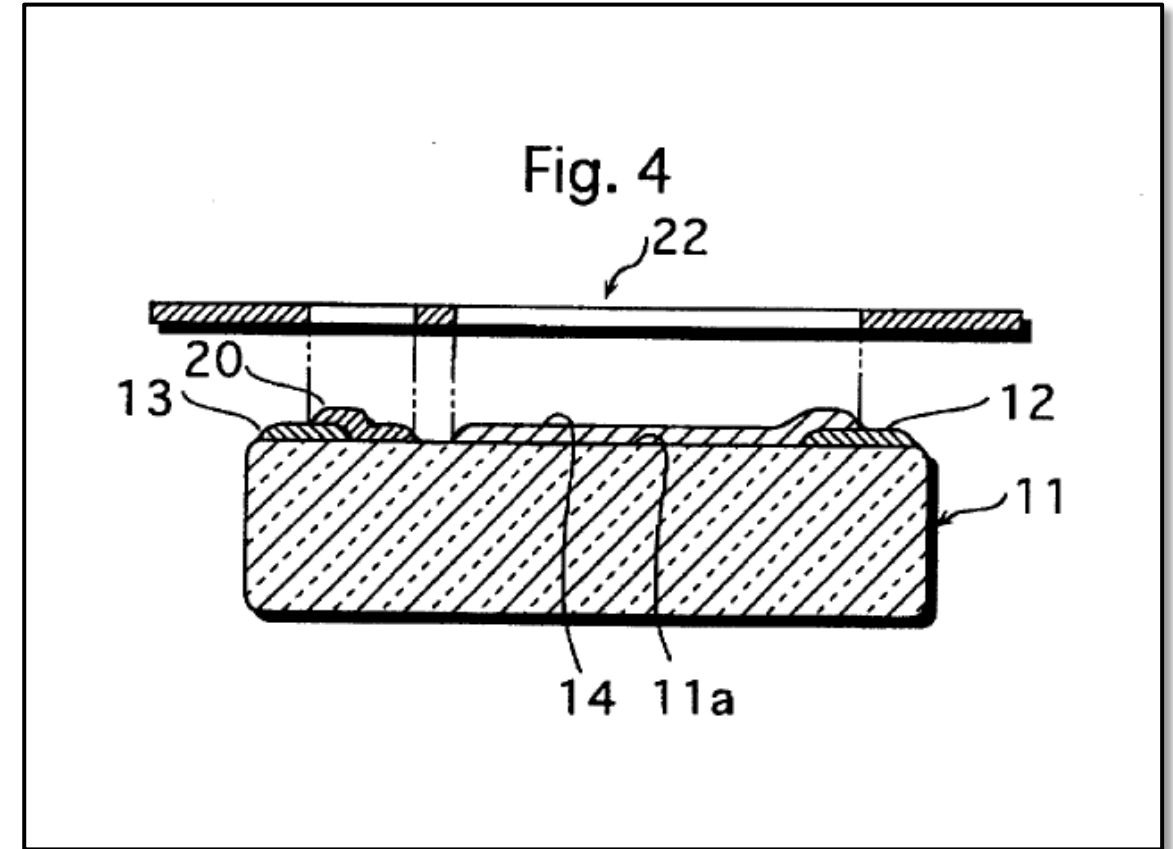
Hanamura (EX1008)

**With one exception in a footnote,
Petitioner does not argue
obviousness under Pictiva's
proposed claim constructions.**

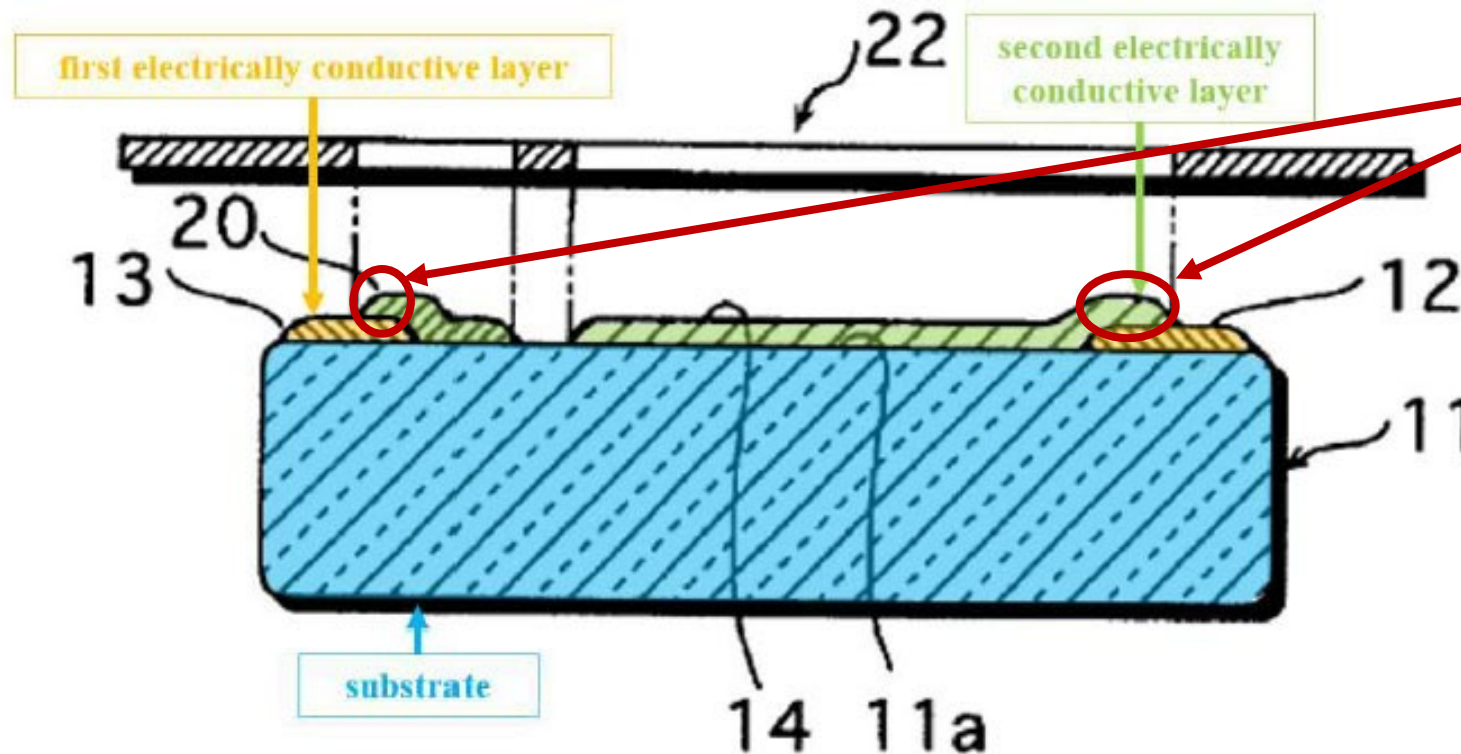
⁹ This limitation is met even under Pictiva's construction because portions of electrodes 14 and 20 lie directly above the *first electrically conductive layer* (electrodes 12 and 13). See POR, 16 (discounting only the portions of the second layer not directly above the first).



'492 Patent Fig. 4 Compared to Hanamura Fig. 4

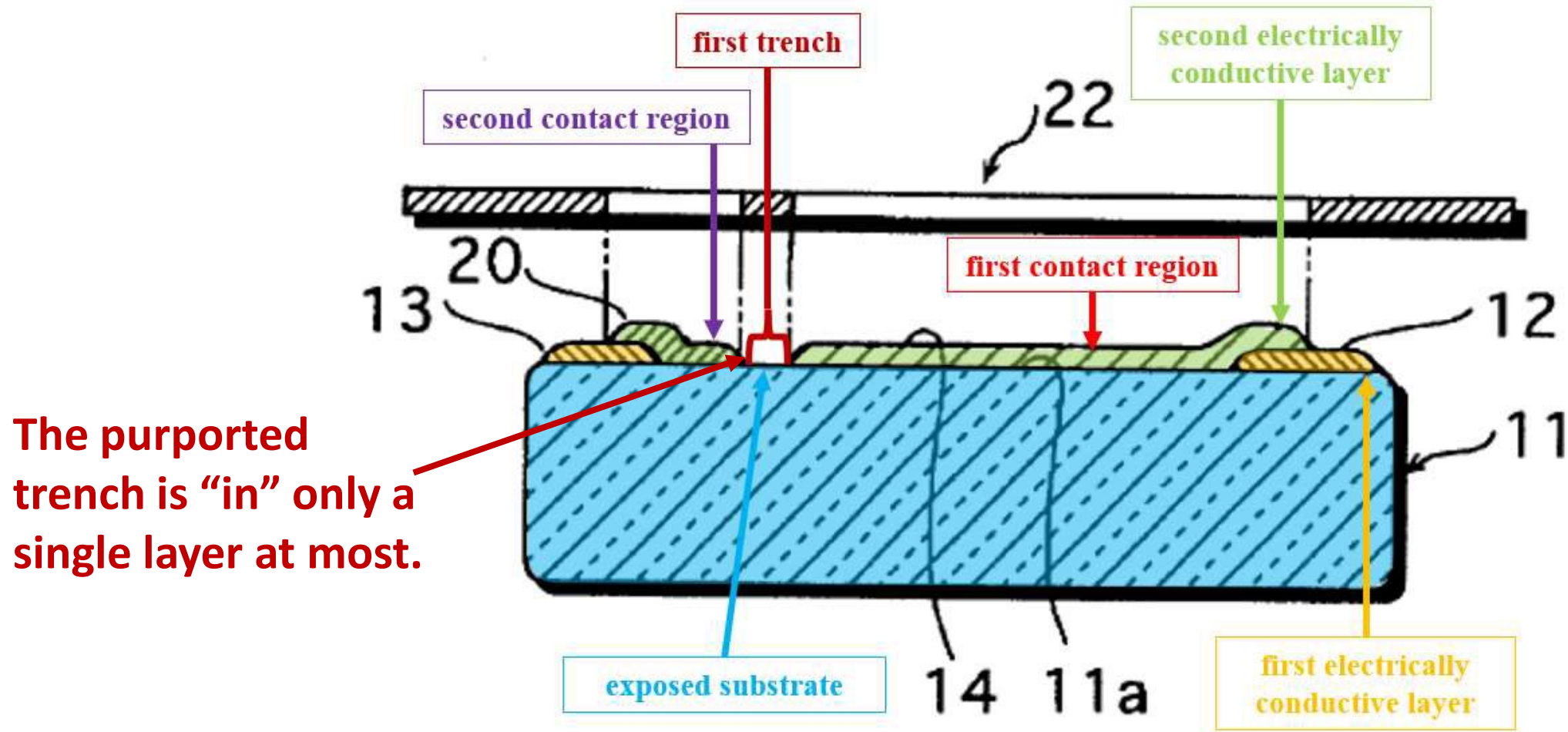


Even Petitioner's Annotations of Hanamura Fail to Establish First and Second Electrically Conductive Layers



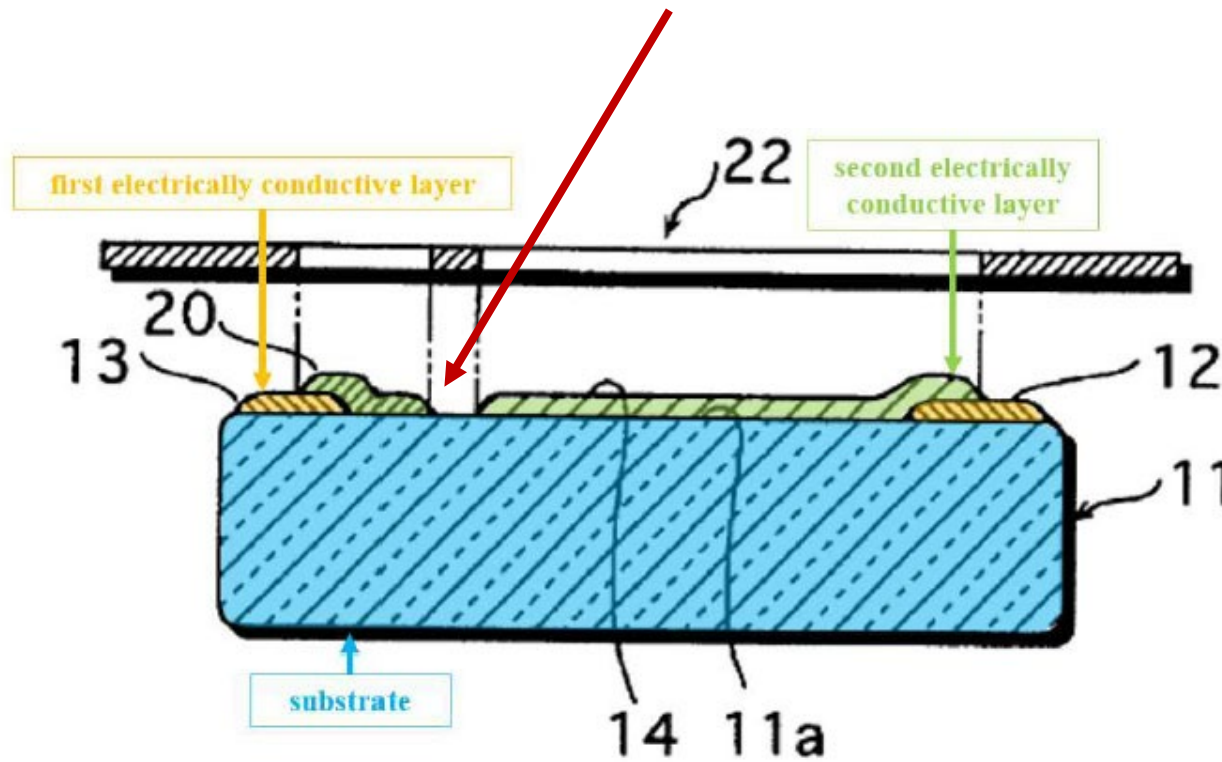
At most only these portions of electrodes 14 and 20 could constitute a second electrically conductive layer formed on the first electrically conductive layer.

Even Petitioner's Annotations of Hanamura Fail to Establish a First Trench in the First and Second Electrically Conductive Layers



Even Petitioner's Annotations of Hanamura Fail to Establish Forming the Purported First Trench

Purported trench is neither “formed” nor “in” the alleged first and second electrically conductive layers. At most it is a “predetermined spacing” between *simultaneously formed* electrodes 14 and 20.



According to the first embodiment described above, the first capacitor electrode 14 and the auxiliary electrode 20 are formed simultaneously on the head surface 11a of the chip 11 by using the second screen 22, as shown in FIG. 4. Thus, the predetermined spacing D1 is reliably provided between the first capacitor electrode 14 and the auxiliary electrode 20 even if the second screen 22 positionally deviates slightly relative to the previously formed lead electrodes 12, 13. In other words, it is possible to prevent the first capacitor electrode 14 from being electrically shorted to the second

GROUND 3: Hanamura and Egitto

Ground 3 Relevant Only for Dependent Claims 3, 5, and 6

US009257492B2

(12) **United States Patent**
Ingle

(10) **Patent No.:** US 9,257,492 B2
(45) **Date of Patent:** Feb. 9, 2016

(54) **METHOD FOR PRODUCING A PASSIVE ELECTRONIC COMPONENT, METHOD FOR PRODUCING AN OPTOELECTRONIC ASSEMBLY AND PASSIVE ELECTRONIC COMPONENT**

(71) Applicant: **OSRAM OLED GmbH**, Regensburg (DE)
(72) Inventor: **Andrew Ingle**, Allershausen (DE)
(73) Assignee: **OSRAM OLED GmbH**, Regensburg (DE)

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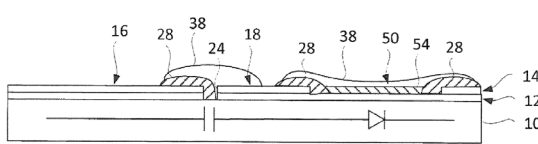
(21) Appl. No.: 14/430,942
(22) PCT Filed: Aug. 20, 2013
(86) PCT No.: PCT/EP2013/067348
§ 371 (c)(1),
(2) Date: Mar. 25, 2015
(87) PCT Pub. No.: WO2014/048639
PCT Pub. Date: Apr. 3, 2014
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(30) **Foreign Application Priority Data**
Sep. 27, 2012 (DE) 10 2012 109 142
(51) **Int. Cl.**
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H01L 29/00 (2006.01)
(Continued)
(52) **U.S. Cl.**
CPC H01L 27/3225 (2013.01); H01G 4/005 (2013.01); H01G 4/33 (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 23/5227; H01L 27/0658
USPC 438/329, 957; 257/528, 532
See application file for complete search history.

(56) **References Cited**
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(Continued)
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DE 10200906066 A1 3/2011
DE 112008003787 T5 3/2012
OTHER PUBLICATIONS
German Search Report based on Application No. 10 2012 109 142, 0(5 pages) dated Jun. 25, 2013.
Primary Examiner — Theresa T Doan
(74) **Attorney, Agent, or Firm** — Viering, Jentschura & Partner

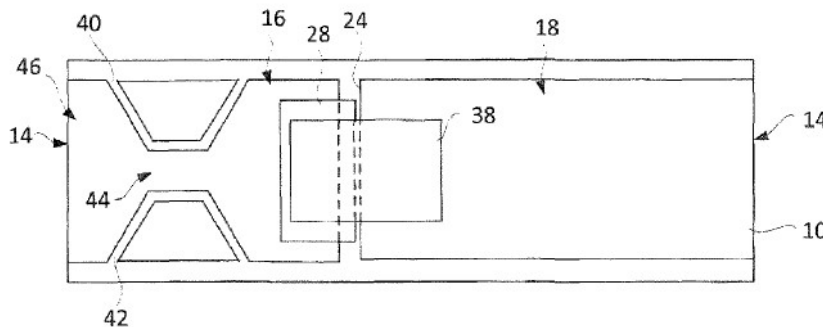
(57) **ABSTRACT**
Various embodiments may relate to a method for producing a passive electronic component, including forming a first electrically conductive layer on a substrate, forming a second electrically conductive layer on the first electrically conductive layer, forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region, applying a dielectric in a structured fashion to the second electrically conductive layer in the first trench such that the dielectric electrically insulates the first contact region from the second contact region, and applying an electrically conductive electrode layer in a structured fashion to the dielectric above the first contact region and to the second contact region.

18 Claims, 6 Drawing Sheets



3. The method as claimed in claim 1, wherein, before the dielectric is applied, a second trench and at least one third trench are formed, which delimit a resistance region, which comprises a part of the first and second electrically conductive layers and which has a taper in a direction parallel to the electrically conductive layers and which leads into the first contact region on a first side of the taper.

Fig. 9



Egitto (EX1013)

(19) United States
(12) Patent Application Publication (10) Pub. No.: US 2009/0178271 A1
Egitto et al. (43) Pub. Date: Jul. 16, 2009

(54) METHOD OF MAKING CIRCUITIZED SUBSTRATES HAVING FILM RESISTORS AS PART THEREOF

(75) Inventors: Frank D. Egitto, Binghamton, NY (US); John S. Kresge, Binghamton, NY (US); John M. Lauffer, Waverly, NY (US)

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(73) Assignee: Endicott Interconnect Technologies, Inc., Endicott, NY (US)

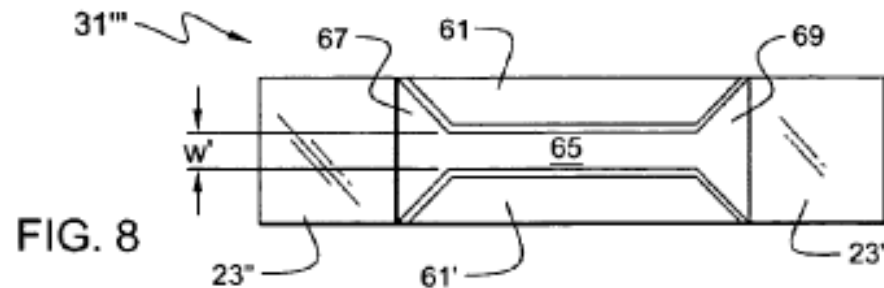
(21) Appl. No.: 12/007,820

(22) Filed: Jan. 16, 2008

Publication Classification
(51) Int. Cl. H01C 17/06 (2006.01)
(52) U.S. Cl. 29/620
(57) ABSTRACT
A method of making a circuitized substrate which involves forming a plurality of individual film resistors having approximate resistance values as part of at least one circuit of the substrate, measuring the resistance of a representative (sample) resistor to define its resistance, utilizing these measurements to determine the corresponding precise width of other, remaining film resistors located in a defined proximity relative to the representative resistor such that these remaining film resistors will include a defined resistance value, and then selectively isolating defined portions of the resistive material of these remaining film resistors while simultaneously defining the precise width of the resistive material in order that these film resistors will possess the defined resistance.



- The Petition argued that while the “claim requires that the resistance region have a particular design,” this “is *nothing more than a design choice.*”
- In Reply, Samsung argues that Patent Owner “overlooks that *Egitto only discloses two adjustable resistor patterns.*”



But Petitioner's Expert Agrees That Claims 3 and 5 Require a Particular Design Out of Many, Many Possibilities (Not Just Those in Egitto)

Dr. Kattamis
Expert Witness

SAMSUNG

Q. Would you agree there are many, many ways that one could design the geometry of a resistor?

ATTORNEY WEIDENFELLER: Objection.

THE WITNESS: There are, and then there are issues with control and ensuring proper tolerance on those resistors. So there are, as with many processing steps, domineering conditions to consider pros and cons with different techniques.

EX2006, 106:7-16; POR 65; Sur-Reply 26

Obviousness Precedent Requires More



“[T]he expert’s testimony on obviousness was essentially a **conclusory statement** that a person of ordinary skill in the art would have known, **based on the ‘modular’ nature of the claimed components**, how to combine any of a number of references to achieve the claimed inventions. This is not sufficient and is **fraught with hindsight bias**.”

ActiveVideo Networks, Inc. v. Verizon Commc’ns, Inc., 694 F.3d 1312, 1327 (Fed. Cir. 2012)
(emphases added)

“The obviousness inquiry does not merely ask whether a skilled artisan **could** combine the references, but instead asks whether they **would** have been motivated to do so.”

Adidas AG v. Nike, Inc., 963 F.3d 1355, 1358-59 (Fed. Cir. 2020)

GROUND 1: Ingle and Hasei

Ingle (EX1005)

No disclosure of applying an “electrically conductive electrode layer” (e.g., a cathode) “in a structured fashion,” nor any particular location or shape for such a cathode.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International publication date
March 31, 2011 (03/31/2011)

(10) International publication number
WO 2011/036089 A1

(51) International patent classification:
H01L 51/10 (2006.01)

(21) International file number: PCT/EP2010/063623 (74) Attorneys: EPPING HERMANN FISCHER PATENT-ANWALTSGESellschaft MBH; Rüdigerstraße 55, 80339 Munich (DE)

(22) International filing date:
September 16, 2010 (09/16/2010)

(25) Filing language: German

(26) Language of publication: German

(30) Priority information:
10 2009 043 066.0 September 25, 2009 (09/25/2009) DE
10 2009 060 066.3 December 22, 2009 (12/22/2009) DE

(71) Applicant (for all designated states except US): OSRAM OPTO SEMICONDUCTORS GMBH [DE/DE]; Leibnizstraße 4, 93055 Regensburg (DE)

(72) Inventors; and
(75) Inventors/applicants (only for US): INGLE, Andrew [US/DE]; Anton-Bruckner-Straße 5, 85391 Allershausen (DE); SCHLENKER, Tilman [DE/DE]; Jacklberg 17, 93152

(81) Designated countries (unless otherwise indicated, for each available national type of IP right): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated countries (unless otherwise indicated, for each available regional type of IP right): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO,

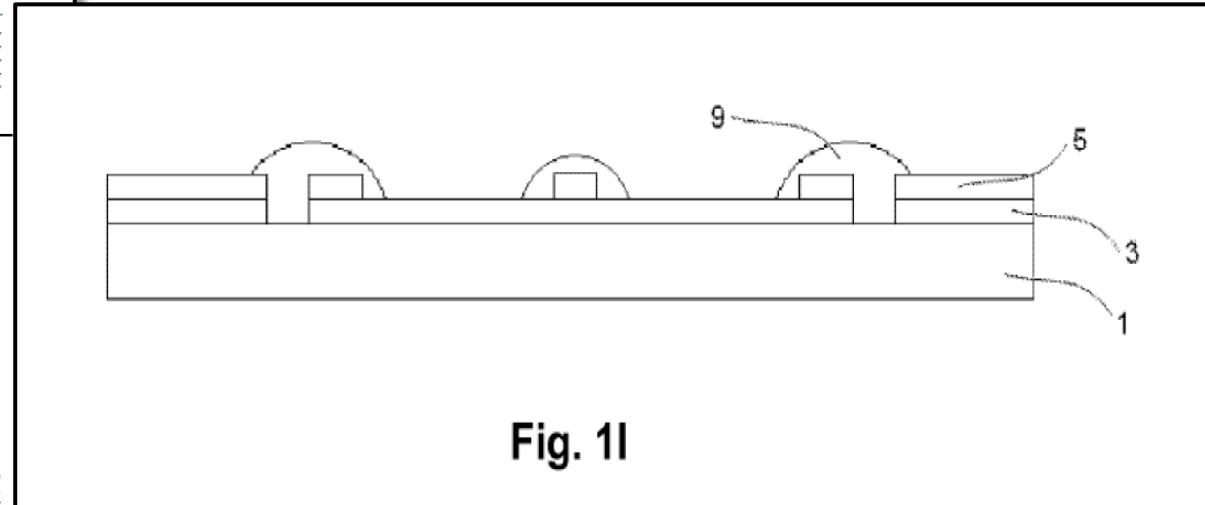
[Continued on the next page]

(54) Title: METHOD FOR PRODUCING AN ELECTRONIC COMPONENT AND ELECTRONIC COMPONENT

Fig. 3

(57) Abstract: The present invention relates to a method for producing an electronic component having at least one first electrode region (21) and a second electrode region (23), said regions being separated from each other by an insulator (9) and each comprising at least one partial layer of a first electrically conductive material. The present invention further relates to an electronic component that can be produced by means of the method according to the invention.

[Continued on the next page]



Ingle Discloses a Base and Explains That Electronic Components Can Be Produced Using a “Conventional Process”

The **electronic component**, for example an OLED, can now be produced on the substrate layer prepared in this way using a **conventional process**.

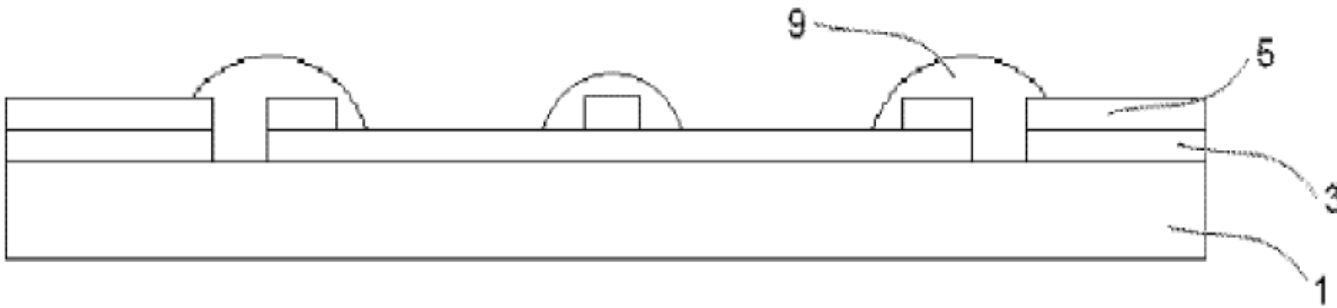


Fig. 1I

Petitioner's Expert Agrees That Ingle Lacks Details Regarding the Cathode

Dr. Kattamis
Expert Witness

SAMSUNG

Q. But the specific location of where one might apply such a cathode layer is not disclosed in Ingle, is it?

A. That's correct. Yes.

Q. And Ingle also does not disclose any particular shape for a cathode layer that one might apply to the structure disclosed in Ingle, correct?

A. I'm just pulling it up. One moment.

That's correct.

EX2006, 92:8-16; POR 30

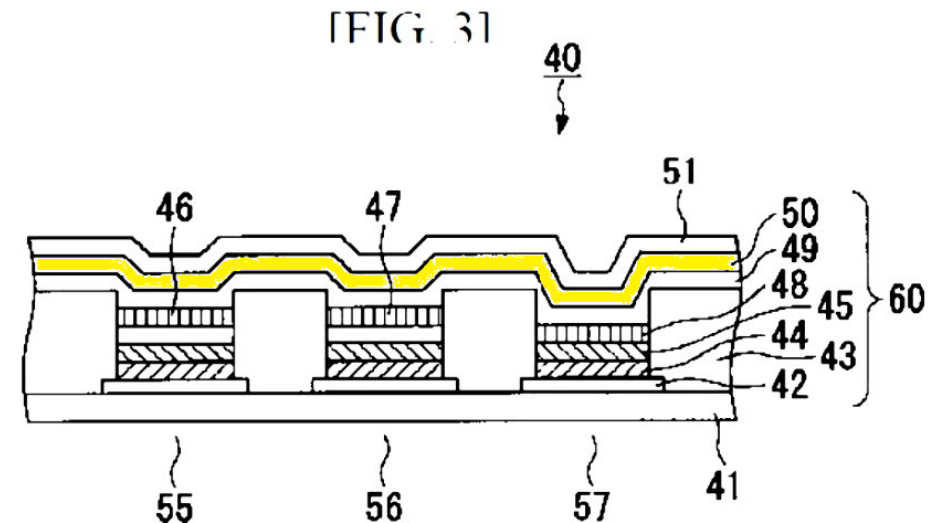
Hasei (EX1007)

- No disclosure of capacitors
- No structured cathode (regardless of application method)
- Describes photolithography as conventional method

(19) Japanese Patent Office (JP)	(12) Patent Application Gazette (A)	(11) Published Application No. JP2003-317610 (P2003-317610A)
(43) Appl. Published: Nov. 7, 2003		
(51) Int. Cl. ⁷	ID Number	FI
H 01 J	9/02	H 01 J
	11/02	
H 01 I	21/288	H 01 I
H 05 B	33/10	H 05 B
	33/14	
Request for Examination: No		Number of Claims: 9 OL Total pages: 9
		Continued on last page
(21) Filed Appl. No.: 2002-116693 (P2002-116693)	(71) Applicant:	000002369 SEIKO EPSON CORPORATION 4-1, Nishi-Shinjuku 2-chome, Shinjuku-ku, Tokyo
(22) Filed: Apr. 18, 2002	(72) Inventor:	Hironobu HASEGAWA c/o Seiko Epson Corporation 3-5, 3-chome, Owa, Suwa-shi, Nagano-ken
	(74) Agent or Attorney:	100095728 Masataka KAMIYANAGI, Patent Attorney
	(2 others)	
Continued on last page		
(54) [Title of the Invention] PATTERN FORMING METHOD, DEVICE, ELECTRONIC APPARATUS, AND DEVICE MANUFACTURING METHOD		
(57) ABSTRACT		
[PROBLEM] To provide a pattern forming method, a device, an electronic apparatus, and a method for manufacturing a device, which are capable of reducing waste in the manufacturing process.		
[RESOLUTION MEANS] A liquid or fluid containing indium tin oxide (ITO) is discharged from an inkjet head of a droplet discharging device onto a desired position on a substrate, thereby patterning the indium tin oxide on the substrate (step S1).		

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graph TD
    S1[ITO patterning using liquid discharging method] --> S2[Dry and form film]
    S2 --> S3[Ink repellent surface treatment]
    S3 --> S4[Patterning conductive material]
    S4 --> S5[Baking]
    S5 --> END([END])
        
```



Petitioner's Expert Agrees That Hasei Does Not Disclose Capacitor Fabrication

Dr. Kattamis
Expert Witness

SAMSUNG

Q. But to be clear, Hasei does not describe the fabrication of a capacitor, does it?

ATTORNEY WEIDENFELLER: Objection.

THE WITNESS: I think that's correct.

It doesn't describe the steps.

EX2006, 90:1-5; POR 3, 36

Hasei Describes Photolithography as the “Conventional Method”

(19) Japanese Patent Office (JP)

(12) Patent Application Gazette (A)

(11) Published Application No. JP2003-317610 (P2003-317610A)

(43) Appl. Published: Nov. 7, 2003

(51) Int. Cl.⁷

ID Number

FI

H 01 J

9/02

H 01 J

9/02

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3K007

H 01 J

11/02

B

4M104

H 01 I

21/288

H 01 I

21/288

Z

5C027

H 05 B

33/10

H 05 B

33/10

A

5C040

H 05 B

33/14

A

Request for Examination: No

Number of Claims: 9 OL Total pages: 9 Continued on last page

(21) Filed Appl. No.: 2002-116693 (P2002-116693)

(22) Filed: Apr. 18, 2002

(71) Applicant: 000002369 SEIKO EPSON CORPORATION 4-1, Nishi-Shinjuku 2-chome, Shinjuku-ku, Tokyo

(72) Inventor: Hironobu HASEGAWA c/o Seiko Epson Corporation 3-5, 3-chome, Owa, Suwa-shi, Nagano-ken

(74) Agent or Attorney: 100095728 Masataka KAMIYANAGI, Patent Attorney

(2 others)

Continued on last page

(54) [Title of the Invention] PATTERN FORMING METHOD, DEVICE, ELECTRONIC APPARATUS, AND DEVICE MANUFACTURING METHOD

(57) ABSTRACT [PROBLEM] To provide a pattern forming method, a device, an electronic apparatus, and a method for manufacturing a device, which are capable of reducing waste in the manufacturing process. [RESOLUTION MEANS] A liquid or fluid containing indium tin oxide (ITO) is discharged from an inkjet head of a droplet discharging device onto a desired position on a substrate, thereby patterning the indium tin oxide on the substrate (step S1).

ITO patterning using liquid discharging method S1

Dry and form film S2

Ink repellent surface treatment S3

Patterning conductive material S4

Baking S5

END

[0003]
PROBLEMS TO BE SOLVED BY THE INVENTION
However, with the conventional method of providing a conductive pattern, most of the conductive material formed over the entire surface of the substrate (other than the conductive pattern portion) must be removed by etching, and the removed conductive material is wasted in the manufacturing process. Furthermore, the conventional method of providing a conductive pattern requires a photomask to be used in the photolithography process, which lengthens the manufacturing process and requires that a photomask be made each time the model of the conductive pattern is changed, resulting in increased manufacturing costs and a longer manufacturing period. Furthermore, conventional conductive patterns have the problem that even a single break in the wiring of the conductive pattern provided on the substrate means that the prescribed function cannot be achieved.

GROUND 1: Ingle and Hasei

- No application of an “electrically conductive electrode layer” (e.g., a cathode) in a “structured fashion”
- No application of an “electrically conductive electrode layer” (e.g., a cathode) “above the first contact region”
- No working electronic component

No Motivation to Combine Ingle and Hasei to Apply Cathodes in a Structured Fashion

The electronic component, for example an OLED, can now be produced on the substrate layer prepared in this way using a conventional process.

In contrast to the conventionally used lithography methods, in which each coating step is applied individually and structured photolithographically, in the methods according to the invention it is intended to apply only as much material of the insulator and the protective material, both of which can generally be expensive materials, as is required for the production of the electronic component. In this way, for example, OLED light tiles, which were complex and expensive to produce using conventional methods, can be advantageously produced in a time- and material-saving manner.

EX1005, 21:34-36, 16:19-29

[0003]

PROBLEMS TO BE SOLVED BY THE INVENTION

However, with the conventional method of providing a conductive pattern, most of the conductive material formed over the entire surface of the substrate (other than the conductive pattern portion) must be removed by etching, and the removed conductive material is wasted in the manufacturing process. Furthermore, the conventional method of providing a conductive pattern requires a photomask to be used in the photolithography process, which lengthens the manufacturing process and requires that a photomask be made each time the model of the conductive pattern is changed, resulting in increased manufacturing costs and a longer manufacturing period. Furthermore, conventional conductive patterns have the problem that even a single break in the wiring of the conductive pattern provided on the substrate means that the prescribed function cannot be achieved.

EX1007, ¶ 3

Obviousness Precedent Requires More

“The obviousness inquiry does not merely ask whether a skilled artisan ***could*** combine the references, but instead asks whether they ***would*** have been motivated to do so.”

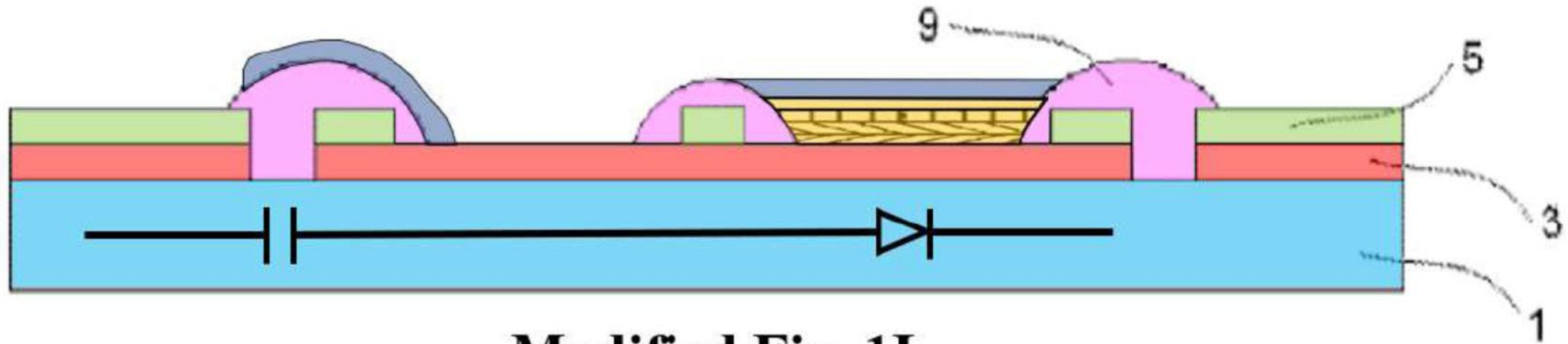
Adidas AG v. Nike, Inc., 963 F.3d 1355, 1358-59 (Fed. Cir. 2020)

Obviousness requires Samsung “to explain why a person of ordinary skill in the art would have combined elements from specific references ***in the way the claimed invention does.***”

ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc., 694 F.3d 1312, 1328 (Fed. Cir. 2012)
(citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418-19 (2007))



Cathodes Added by Annotation by Samsung and Its Expert Are Pure Conjecture



Modified Fig. 1I

Undisputed That Ingle Includes No Such Disclosure

Dr. Kattamis
Expert Witness

SAMSUNG

Q. But there's no disclosure in Ingle of applying the cathode layer in a structured fashion, correct?

A. No. Ingle leaves that open for how to complete the optoelectronic device.

Q. In fact, there's no embodiment described in Ingle wherein every layer is fabricated using an additive technique; is that right?

A. Sure. In the process, it describes not every layer is additive. I think that that's true.

Petitioner Relies Solely on Hasei for the Structured Application of the Cathode

Dr. Kattamis
Expert Witness

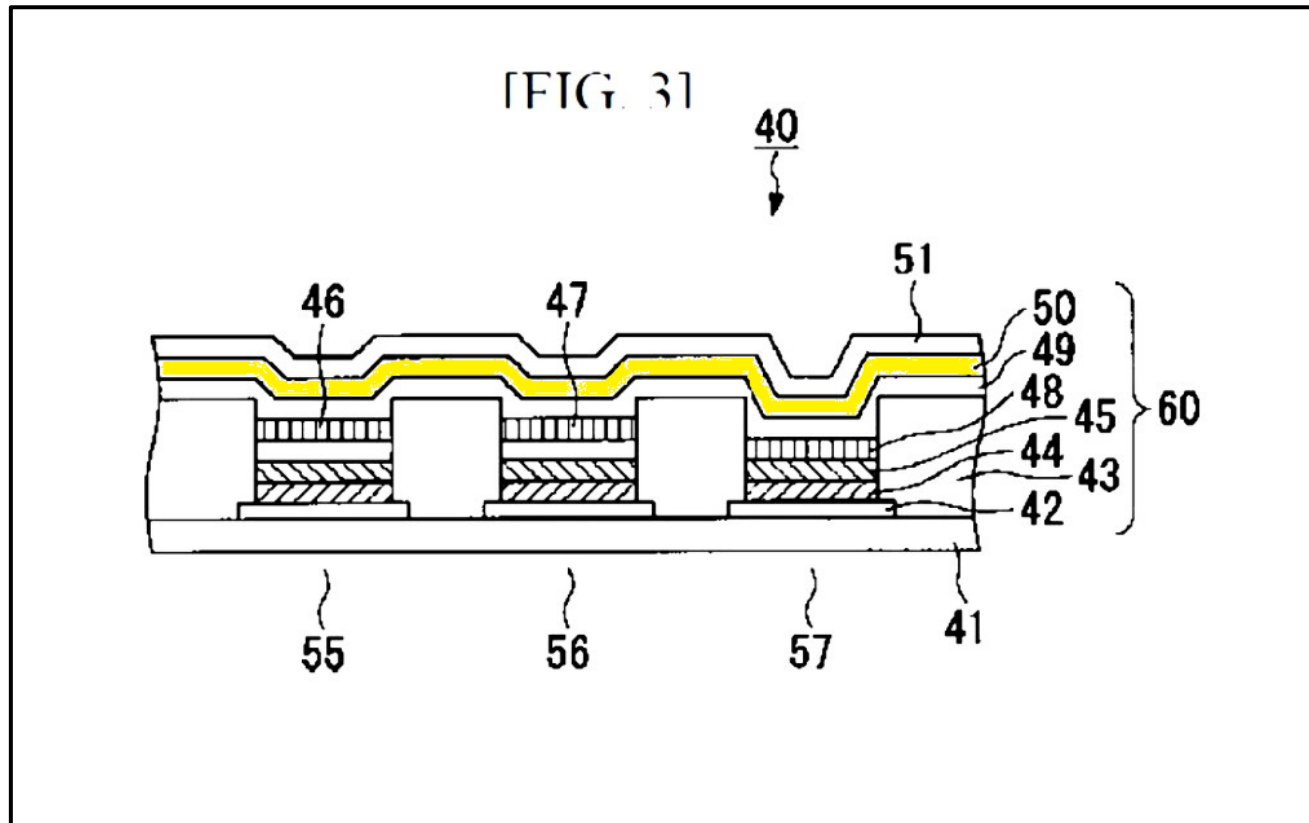
SAMSUNG

THE WITNESS: Other than Hasei, I know that we did this kind of stuff when we were applying cathodes to OLED displays for different substrates, but I don't have a publication that would show that.

Q. So for purposes of your expert opinion in this particular matter, the only evidence you point to as disclosing in your view the structured application of the cathode layer of an OLED display device prior to 2012 is Hasei, correct?

A. Yes. That's correct. That's why I signed to it. Yes.

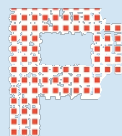
Hasei Does Not Disclose an Electrode Structured in Any Manner



[0037] The light emitting layers 46, 47, and 48 can be formed from small molecule organic light emitting dyes or polymer light emitting bodies, or in other words, light emitting materials such as various fluorescent and phosphorescent materials, and organic electroluminescent materials such as Alq₃ (aluminum chelate complex). Among the conjugate polymers that serve as light emitting substances, those containing an arylenevinylene or polyfluorene structure are particularly preferable. Examples of small molecule light emitting bodies that can be used include naphthalene derivatives, anthracene derivatives, perylene derivatives, dyes such as polymethine, xanthene, coumarin, and cyanine dyes, metal complexes of 8-hydroquinoline and its derivatives, aromatic amines, tetraphenylcyclopentadiene derivatives, and known substances described in Japanese Unexamined Patent Application S57-51781 and Japanese Unexamined Patent Application S59-194393. The negative electrode 50 is a metal electrode made of aluminum (Al), magnesium (Mg), gold (Au), silver (Ag), and the like. The negative electrode 50 may be formed by the droplet discharging method depicted in the description of step S1 in FIG. 1, or may be formed by photolithography or etching.

Unrebutted That Hasei Does Not Disclose a Structured Cathode

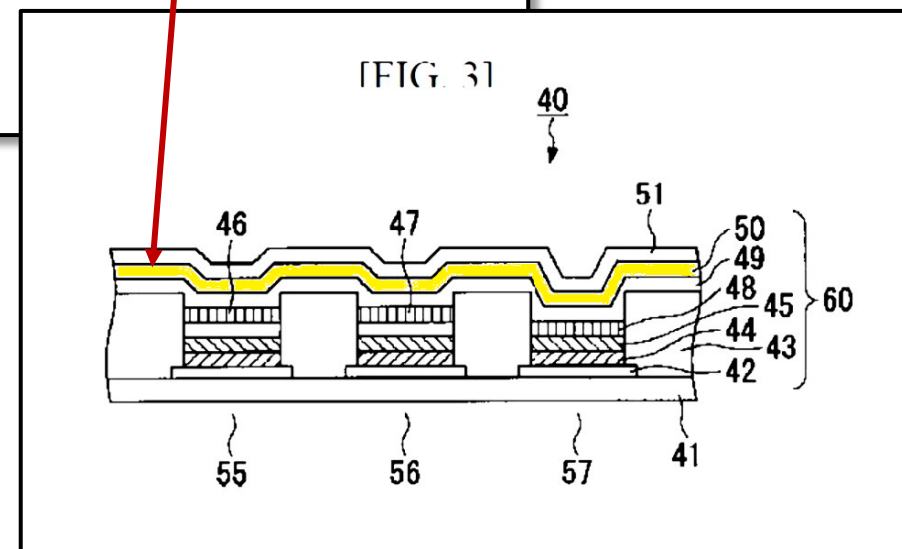
Dr. Pattison
Expert Witness



pictivadisplays

54. Based on these disclosures, a POSITA at the time of the invention of the '492 Patent would understand that this unbroken negative electrode 50 has not been structured in any manner, whether through application in a “structured fashion” or through planar application and subsequent structuring by, for example, etching or photolithography.

EX2001, ¶ 54; EX1007, Fig. 3 (annotated);
POR 36; Sur-Reply 15-16



Undisputed That Hasei's Droplet Discharge Method Can Be Used to Fabricate an Unstructured Layer

Dr. Kattamis
Expert Witness

SAMSUNG

Q. And if you did so, if you used the droplet discharge method to apply a layer, a continuous layer across the entire device, that would not be a structured layer, would it?

ATTORNEY WEIDENFELLER: Objection.

THE WITNESS: Sure. If I coat an entire workpiece using that method, it would be continuous.

Q. And it would not be structured, would it?

A. One could do that, yes. It would not be structured, but I think generally it would be considered a structured method, and there's other disclosure, like in Step 1 of Hasei, which is also pointing to a patterning. So I think it's pretty clear that it can be used for structured deposition.

EX2006, 77:16-78:7; POR 37; Sur-Reply 16

Undisputed That Hasei's Cathode Is Not Structured as Expressly Disclosed

Dr. Kattamis
Expert Witness

SAMSUNG

Q. In contrast, in Figure 3 of Hasei, the negative electrode or cathode layer 50 does not include any structuring; it is continuous across the device, correct?

ATTORNEY WEIDENFELLER: Objection.

THE WITNESS: In this cross-sectional view, so not taking into account any change of, you know, in a planar view, and for these three OLEDs, yes, it's continuous along this figure.

EX2006, 79:11-20; POR 37; Sur-Reply 16

Petitioner Offers Only Speculation Regarding Conventionality of Hasei's Droplet Discharge Method and the Structure of Hasei Electrode 50

cover. What Ingle describes as “conventional” is not limited to what Hasei believed to be “conventional” years earlier.⁵ The opposite is true—one would expect Hasei’s teachings to become conventional by Ingle’s time, let alone by the ’492 patent’s 2012 claimed priority date. *Institut Pasteur v. Focarino*, 738 F.3d 1337, 1349 (Fed. Cir. 2013) (“obviousness is determined at the time the invention was made”).

Figure 3 is a two-dimensional cross-section lacking a planar view. Ex.2006, 74:17-75:1. Accordingly, it cannot be determined based on Figure 3 alone whether negative electrode 50 is structured. Ex.2006, 74:20-75:1, 79:4-20. Ex.1033, 69:15-73:5 (agreeing that cross-sections are not definitive as to structure).

But Simply Being Disclosed in a Reference Does Not Mean a Technique Was “Conventional”



“The mere fact that something is disclosed in a piece of prior art ... does not mean it was well-understood, routine, and conventional.”

Berkheimer v. HP Inc., 881 F.3d 1360, 1369 (Fed. Cir. 2018)

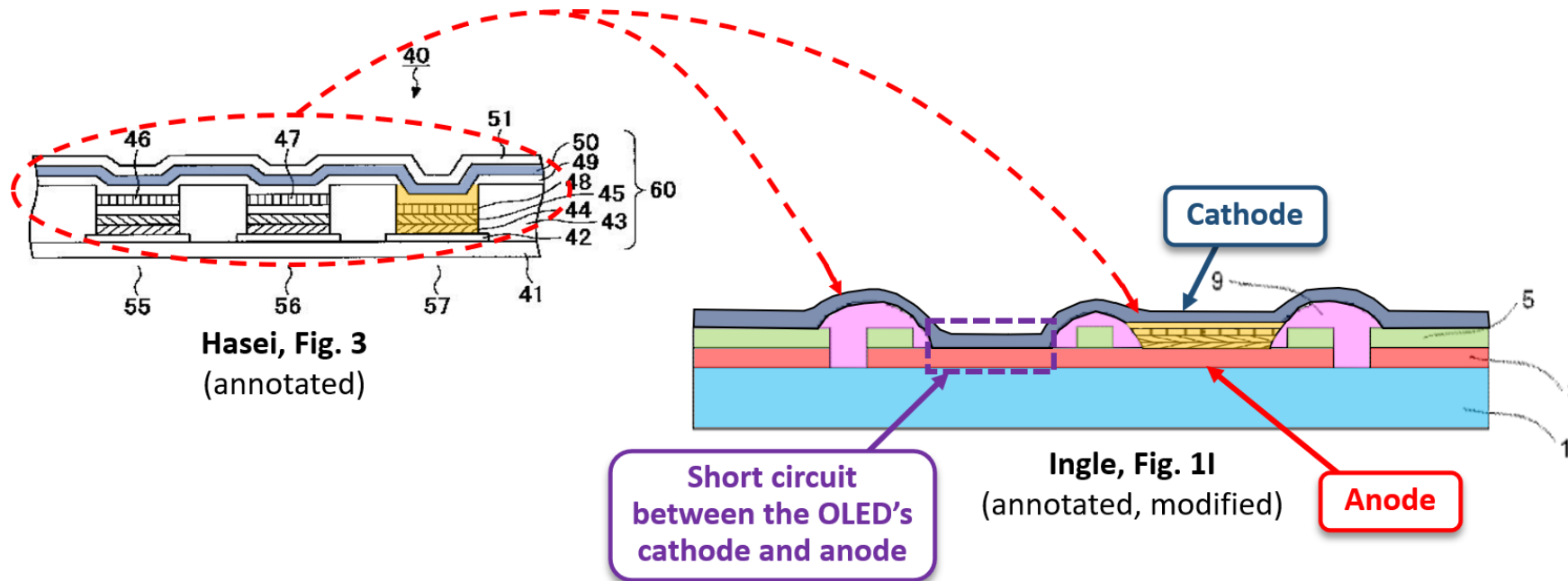
And Samsung Improperly Attempts to Shift the Burden to Patent Owner



“In an inter partes review, the burden of persuasion is on the petitioner to prove ‘unpatentability by a preponderance of the evidence,’ 35 U.S.C. § 316(e), and that burden never shifts to the patentee.”

Dynamic Drinkware, LLC v. Nat’l Graphics, Inc., 800 F.3d 1375, 1378 (Fed. Cir. 2015)

Petitioner's Belated Annotations Only Further Illustrate Distinctions Between Ingle and Hasei



Petitioner's Arguments Regarding POSITA at the Time of the Invention Are Also Difficult to Reconcile with Its Own Expert's Testimony

Dr. Kattamis
Expert Witness

SAMSUNG

Q. But to be clear, you're personally not aware of anyone having fabricated such a device in the claimed manner prior to the '492 Patent, correct?

A. Correct.

GROUND 1: Ingle and Hasei

- No application of an “electrically conductive electrode layer” (e.g., a cathode) in a “structured fashion”
- No application of an “electrically conductive electrode layer” (e.g., a cathode) “above the first contact region”
- No working electronic component

Petitioner's Expert Agrees That Ingle Lacks Details Regarding the Location and Shape of Any Hypothetical Cathode

Dr. Kattamis
Expert Witness

SAMSUNG

Q. But the specific location of where one might apply such a cathode layer is not disclosed in Ingle, is it?

A. That's correct. Yes.

Q. And Ingle also does not disclose any particular shape for a cathode layer that one might apply to the structure disclosed in Ingle, correct?

A. I'm just pulling it up. One moment.

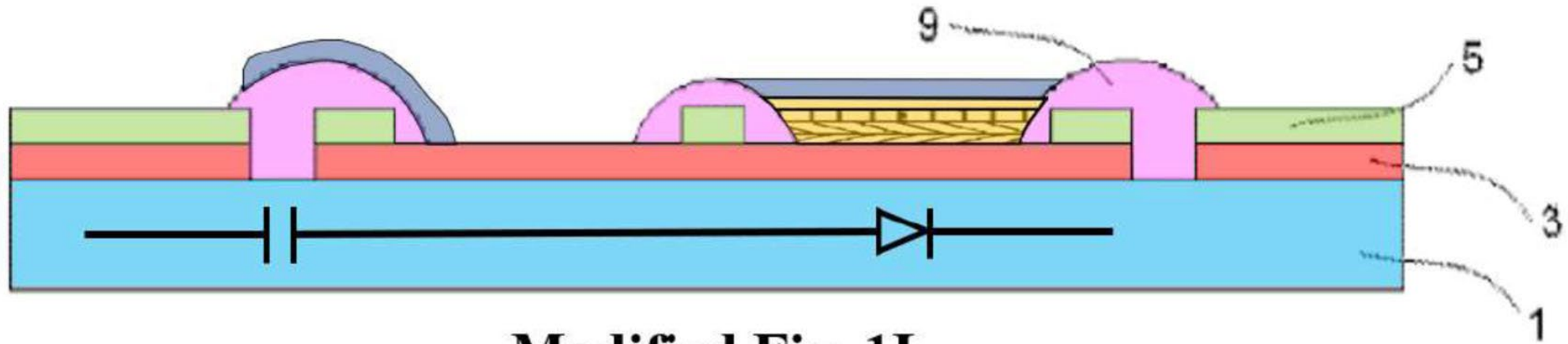
That's correct.

Q. My question is whether Ingle discloses applying a cathode over the first contact region.

ATTORNEY WEIDENFELLER: Objection.

THE WITNESS: I think no, other than the fact that it teaches you to build these other structures on that backplane, and those would require electrodes.

Petitioner's Own Imaginary Cathode Has Minimal Overlap, If Any



Modified Fig. 1I

Petitioner's Expert Agrees Any Overlap Is "Just a Little"

Dr. Kattamis
Expert Witness

SAMSUNG

Q. Now, it appears to me that your hypothetical cathode layer, in gray, does not extend over the first contact region, the leftmost green region. Am I correct?

ATTORNEY WEIDENFELLER: Objection.

THE WITNESS: No. Apologies. It does, just a little, and then that's why I had the conversation in 167 which describes that you could change that distance by tailoring both the dielectric and -- the overall size of the dielectric and the electrode layer.

EX2006, 95:3-13; POR 3; Sur-Reply 29

GROUND 1: Ingle and Hasei

- No application of an “electrically conductive electrode layer” (e.g., a cathode) in a “structured fashion”
- No application of an “electrically conductive electrode layer” (e.g., a cathode) “above the first contact region”
- No working electronic component

A POSITA Would Not Be Motivated to Create a Non-Working Capacitor

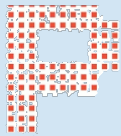


“If references taken in combination would produce a ‘*seemingly inoperative device*,’ we have held that such references teach away from the combination and thus cannot serve as predicates for a prima facie case of obviousness.”

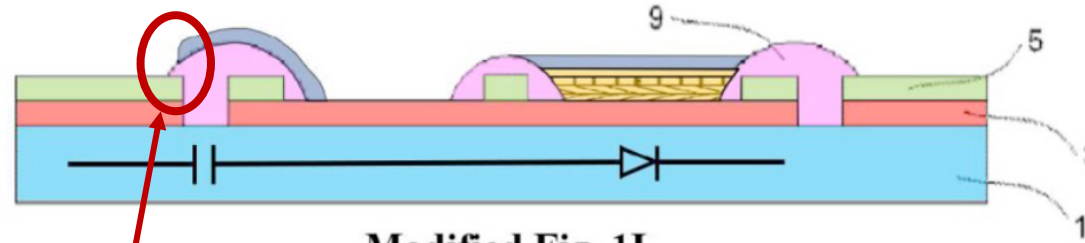
McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 1354 (Fed. Cir. 2001) (emphasis added)

Minimal Overlap Insufficient for a Working Capacitor

Dr. Pattison
Expert Witness



pictiva displays



Modified Fig. 1I

Petition 27 (Ingle Fig. 1I as modified by Petitioner).

11. Assuming Dr. Kattamis is correct, a POSITA would understand that the minimal overlap between the imaginary grey cathode and the purported first contact region in green would be insufficient to produce a reliably working capacitor. That is because the opposing surface areas of the two purported electrodes would be too small to generate anything beyond a theoretical capacitance. A POSITA would not have been motivated to pursue such a capacitor.

EX2005, ¶ 11; POR 48; Sur-Reply 22

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Pictiva Slide 65

Petitioner's Expert Agreed in an Similar Context

Dr. Kattamis
Expert Witness

SAMSUNG

Q. So looking at Figure 1I, the electrically conductive layers on either side of the dielectric, Number 9, why does that combination not form a capacitor such that you have electrodes on either side of the dielectric?

A. I think, again, it's a scaling issue. If we look at layer 1 as being a substrate, then this isn't really to scale, because what it's showing me is the metal layers, or the conductive layers 3 and 5, are of similar thickness.

So you would have a very, very tiny surface area for any capacitor. So I wouldn't consider it a capacitor, nor would it be something you could easily tailor to adjust capacitance.

So it's a capacitor in the same way as if I hold two pieces of metal across from each other with an air gap, there's theoretically a capacitance there, but it's not something you can tailor unless you make extremely thick films.

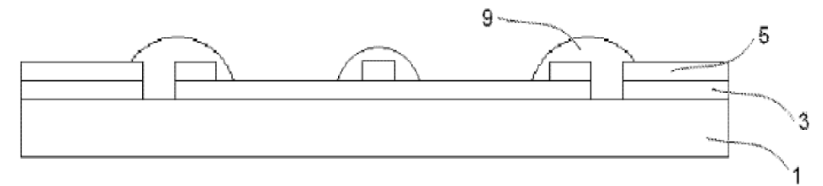
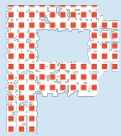


Fig. 1I

Extending the Hypothetical Cathode Insufficient

Dr. Pattison
Expert Witness



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87. Furthermore, extending the imaginary electrically conductive electrode layer further to the left (and thus “over” the first contact region) would risk a short-circuit or capacitor breakdown due to irregular distance and area between the applied cathode and the first contact region, which would render the capacitor inoperable. A POSITA would not have been motivated to pursue such a capacitor. And without this overlap, applying a cathode as depicted and described by Petitioner and Dr. Kattamis would not form a reliably working capacitor, as any capacitance would be poorly controlled due to inconsistencies in the application of the dielectric and the lack of parallel-facing electrodes. The fundamental performance is a function of the distance between the electrodes, the area of the electrodes, and the dielectric materials properties. The capacitor proposed by Dr. Kattamis would have a small overlap area of the electrodes at a small and poorly controlled distance (due to the structured deposition). This would result in inconsistent capacitance, the likelihood of capacitor breakdown, and the likelihood of short-circuiting the capacitor.

Extending the Hypothetical Cathode Insufficient

Dr. Kattamis
Expert Witness

SAMSUNG

Q. And it's important that the electrodes not be permitted to touch, correct?

A. Yes. That would be a design consideration. Of course.

Q. Because that would create a short circuit, right?

A. Yeah. You wouldn't have a capacitor then.

EX2006, 47:16-23; POR 49-50; Sur-Reply 23

Extending the Hypothetical Cathode Insufficient

Dr. Kattamis
Expert Witness

SAMSUNG

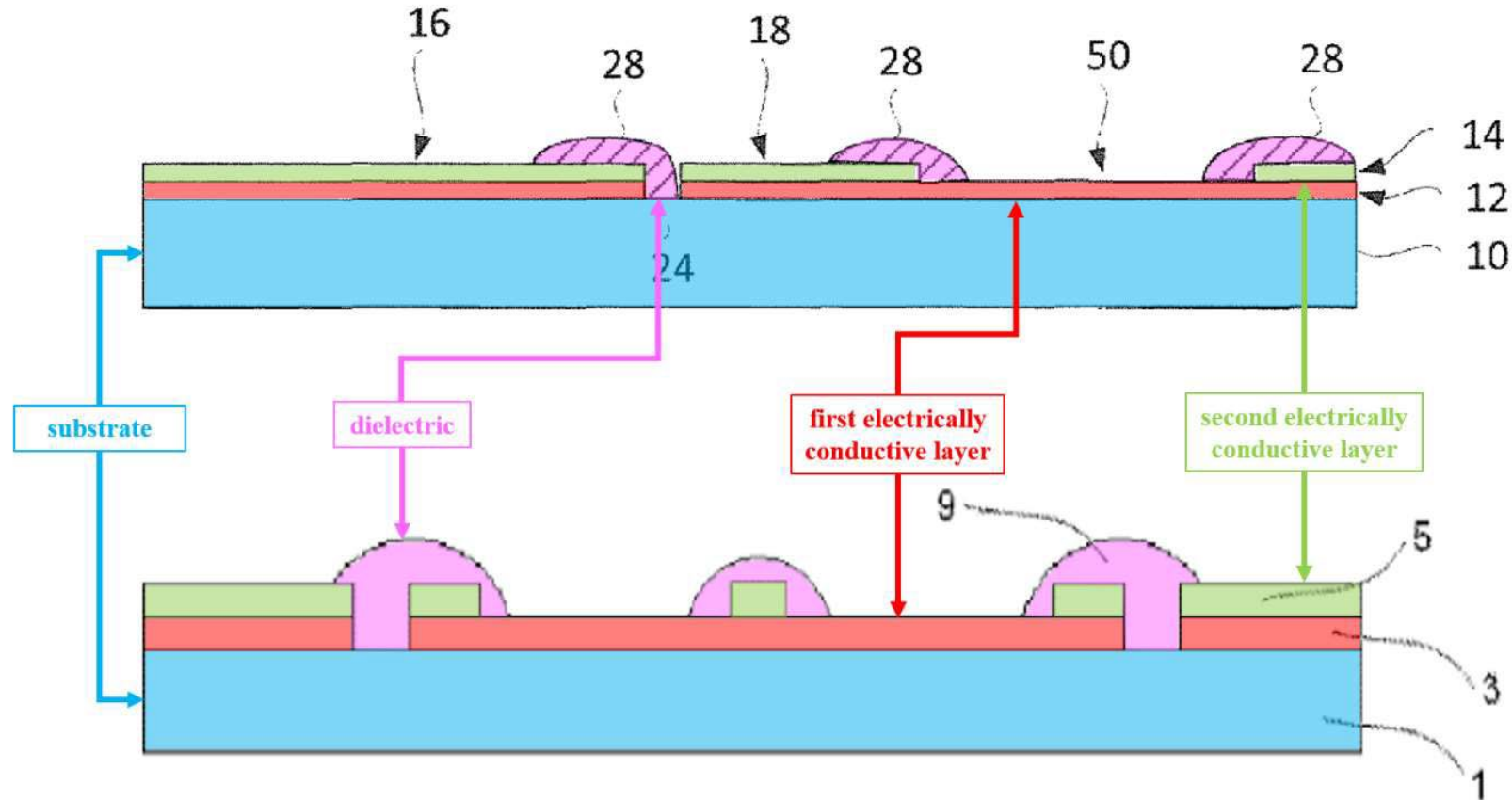
Q. And I'm correct, am I not, that you cannot extend this gray cathode layer to the point that it extends beyond the pink dielectric layer, correct?

ATTORNEY WEIDENFELLER: Objection.

THE WITNESS: Sure. It can't contact or run risk of contacting layer 5, the first contact region. And so the dielectric would have to be extended, as I explained.

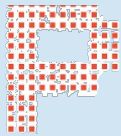
EX2006, 100:9-17; POR 49-50; Sur-Reply 23

Increasing the Dielectric Size Also Insufficient Due to Its Rounded and Steeply Sloped Shape



Increasing Size of Dielectric Insufficient

Dr. Pattison
Expert Witness



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13. Ingle discloses a particular shape for the dielectric, as Dr. Kattamis has agreed. EX2006, at 101:1-12. That shape is round, and the dielectric overlapping the purported first contact region is steeply curved away from the purported first contact region. See Ingle Fig. 1I. As such, any purported cathode following the curvature of the dielectric would necessarily lead to irregular spacing between the purported anode and cathode layers and thus a lack of uniform dielectric thickness.

14. A POSITA would understand that this lack of uniformity could lead to regions with higher electric field, which can result in breakdown of the dielectric, which can potentially trigger a short circuit or capacitor breakdown. A POSITA would also understand that dielectric leakage is also a function of dielectric thickness and can also cause capacitor failure. These problems could render a capacitor inoperable.

EX2005, ¶¶ 13-14; EX2001, ¶ 87; POR 50-51; Sur-Reply 20-21

Petitioner's Expert Agrees the Distance Between the Anode and Cathode of His Hypothetical Capacitor Would Not Be Uniform

Dr. Kattamis
Expert Witness

SAMSUNG

Q. To the extent that the dielectric is curved and to the extent this hypothetical cathode follows that curvature, I am correct that the spacing between the cathode and the first contact region would not be uniform, due to that curvature, correct?

ATTORNEY WEIDENFELLER: Objection.

THE WITNESS: Yeah. It would not be uniform, in that there would be some gradient in the separation distance, right, between the two plates. Still a capacitor, you know, with the same things we discussed earlier to be avoided. Right.

EX2006, 102:20-103:7; POR 50-51; Sur-Reply 21

Petitioner Relies on Improper New (and Conclusory) Theory That a POSITA Would Also Change the Shape of Ingle's Dielectric



“It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’ 35 U.S.C. § 312(a)(3).”

Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd., 821 F.3d 1359, 1369 (Fed. Cir. 2016)

Petitioner's New Theory Also at Odds with Its Own Expert's Prior Testimony That Ingle Discloses a Particular Shape for the Dielectric

Dr. Kattamis
Expert Witness

SAMSUNG

Q. Well, at least in Figure 1I of Ingle, Ingle does disclose a particular shape for the dielectric. Yes?

ATTORNEY WEIDENFELLER: Objection.

THE WITNESS: It discloses a shape, but it does not appear to be to scale. As I mentioned earlier, specifically looking at layers 3 and 5 in the context of layer 1, so I think it's there to give a sense of some geometry, but it's not giving you specific measurements, by any means.

21. Fourth, I understand that Pictiva asserts that Ingle discloses that its dielectric is “steeply curved.” POR at 50. I disagree. A POSITA would not expect Ingle’s dielectric to be “steeply curved” in a real-world implementation of Ingle’s teachings. Instead, a POSITA would understand that Ingle’s figures are simplified representations and would not be representative, or limiting, of what real-world components would look like. Indeed, Ingle explains as such, stating that the “present invention is illustrated below without limiting the generality with reference to the figures.” Ex. 1005, Ingle at 18:21-22. Moreover, a POSITA would likewise understand that the processes for forming the dielectric could be readily adjusted to change how rounded, if at all, the dielectric is.

Petitioner Improperly Relies on Its Own Expert's Self-Contradictory Testimony



“When the party with the burden of proof ... rests its case on an *expert’s self-contradictory testimony*, we may conclude the evidence is insufficient to satisfy that standard.”

Finesse Wireless LLC v. AT&T Mobility LLC, No. 2024-1039, 2025 WL 2713518, at *4 (Fed. Cir. Sept. 24, 2025) (emphasis added); see also *Interactive Commc’ns Int., Inc. v. Blackhawk Network Inc.*, IPR2024-00456, Paper 40 (Revised Director Review Order), at 3 (PTAB Oct. 9, 2025) (reversing final written decision premised on expert who “gave conflicting testimony about how he proposed that the ordinarily skilled artisan would have modified [the prior art]”)