

Samsung Display Co., Ltd.
v.
Pictiva Displays International Ltd.

Case No. IPR2024-01187
U.S. Patent No. 9,257,492

Petitioner's Demonstratives

November 19, 2025 Oral Hearing

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SDC Ex. 1034

The Challenged '492 Patent

(12) United States Patent		(10) Patent No.: US 9,257,492 B2
Ingle		(45) Date of Patent: Feb. 9, 2016
<p>(54) METHOD FOR PRODUCING A PASSIVE ELECTRONIC COMPONENT, METHOD FOR PRODUCING AN OPTOELECTRONIC ASSEMBLY AND PASSIVE ELECTRONIC COMPONENT</p>		
<p>(71) Applicant: OSRAM OLED GmbH, Regensburg (DE)</p>		
<p>(72) Inventor: Andrew Ingle, Allershausen (DE)</p>		
<p>(73) Assignee: OSRAM OLED GmbH, Regensburg (DE)</p>		
<p>(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.</p>		
<p>(21) Appl. No.: 14/430,942</p>		
<p>(22) PCT Filed: Aug. 20, 2013</p>		
<p>(86) PCT No.: PCT/EP2013/067348</p>		
<p>§ 371 (c)(1), (2) Date: Mar. 25, 2015</p>		
<p>(87) PCT Pub. No.: WO2014/048639</p>		
<p>PCT Pub. Date: Apr. 3, 2014</p>		
<p>(65) Prior Publication Data</p>		
<p>US 2015/0255521 A1 Sep. 10, 2015</p>		
<p>(30) Foreign Application Priority Data</p>		
<p>Sep. 27, 2012 (DE) 10 2012 109 142</p>		
<p>(51) Int. Cl.</p>		
<p>H01L 21/8222 (2006.01)</p>		
<p>H01L 29/00 (2006.01)</p>		
<p>(Continued)</p>		
<p>(52) U.S. CL.</p>		
<p>CPC H01L 27/3225 (2013.01); H01G 4/005 (2013.01); H01G 4/33 (2013.01);</p>		
<p>(Continued)</p>		
<p>(58) Field of Classification Search</p>		
<p>CPC H01L 23/5227; H01L 27/0658</p>		
<p>USPC 438/329, 957; 257/528, 532</p>		
<p>See application file for complete search history.</p>		
<p>(56) References Cited</p>		
<p>U.S. PATENT DOCUMENTS</p>		
<p>6,335,211 B1 * 1/2002 Lee 438/22</p>		
<p>6,800,999 B1 * 10/2004 Duggal et al. 315/169.1</p>		
<p>(Continued)</p>		
<p>FOREIGN PATENT DOCUMENTS</p>		
<p>DE 102009060066 A1 3/2011</p>		
<p>DE 112008003787 T5 3/2012</p>		
<p>OTHER PUBLICATIONS</p>		
<p>German Search Report based on Application No. 10 2012 109 142, 0(5 pages) dated Jun. 25, 2013.</p>		
<p>Primary Examiner — Theresa T Doan</p>		
<p>(74) Attorney, Agent, or Firm — Viering, Jentschura & Partner</p>		
<p>(57) ABSTRACT</p>		
<p>Various embodiments may relate to a method for producing a passive electronic component, including forming a first electrically conductive layer on a substrate, forming a second electrically conductive layer on the first electrically conductive layer, forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region, applying a dielectric in a structured fashion to the second electrically conductive layer in the first contact region and at least partly to the substrate in the first trench such that the dielectric electrically insulates the first contact region from the second contact region, and applying an electrically conductive electrode layer in a structured fashion to the dielectric above the first contact region and to the second contact region.</p>		
<p>18 Claims, 6 Drawing Sheets</p>		

'492 Patent

In various embodiments, a method for producing a passive electronic component and/or a method for producing an optoelectronic assembly are provided which enable the production of a passive electronic component and/or an optoelectronic assembly simply and/or in a cost-effective manner and/or without the use of a photolithographic process.

The fact that the dielectric and/or the electrode layer and/or subsequently further layers or materials are “applied in a structured fashion” means, in various embodiments, that the desired structure is already formed during the application of the corresponding layer. The area to be coated is thus coated only in partial regions dependent on the desired structure.

The corresponding materials or layers can be applied in a structured fashion to the substrate for example by printing, for example inkjet printing or screen printing, by blade coating and/or by deposition with the aid of SAMs (self assembling monolayers) and the like.

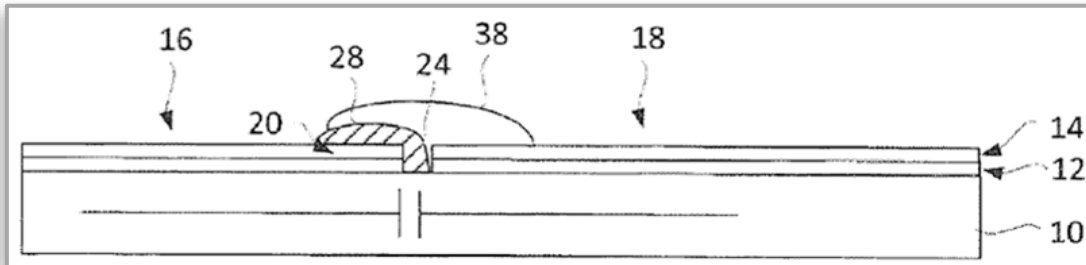
'492 Patent, 1:41-2:19

Claims Directed to “Passive Electronic Component” (1, 16) or “Optoelectronic Assembly” (10)

1. A method for producing a passive electronic component, comprising:

16. A passive electronic component, comprising:

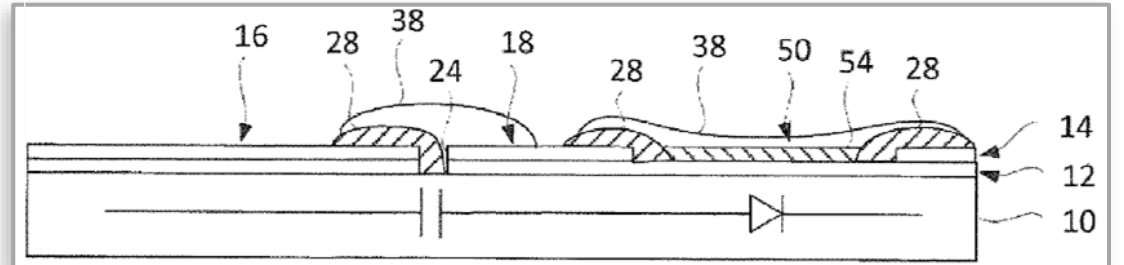
'492 Patent, cls. 1, 16



'492 Patent, Fig. 7

10. A method for producing an optoelectronic assembly, comprising:

'492 Patent, cl. 10



'492 Patent, Fig. 16

Instituted Grounds of Unpatentability

Ground I. Ingle, in view of Hasei, Renders Obvious
Claims 1, 2, 8, 9, 10, 11, and 16

Ground II. Hanamura Renders Obvious
Claims 1, 2, 8, and 16

Ground III. Hanamura, in view of Egitto, Renders Obvious
Claims 3, 5, and 6

* Independent claims underlined.

Primary Disputes

■ Ground I

- “Applying an electrically conductive electrode layer in a structured fashion” (1[e], 10[f], 10[i], 16[e])
- “Applying an electrically conductive electrode layer . . . above the first contact region” (1[e], 10[f], 16[e])
- Whether the combination results in a working capacitor

■ Ground II

- Whether the Board should adopt Pictiva’s narrowing constructions:
 - “First electrically conductive layer on a substrate” / “second electrically conductive layer on the first electrically conductive layer” (1[a]-[b], 16[a]-[b])
 - “A first trench in the first and second electrically conductive layers” (1[c], 16[c])
 - “Forming a first trench” (1[c])

■ Ground III

- Whether a POSITA would have been motivated to implement Egitto’s resistor shape in Hanamura

Ground I – Ingle in View of Hasei

Claims 1, 2, 8–11, and 16

Ingle Shares the Same Named Inventor as the '492 Patent

(12) United States Patent Ingle	(10) Patent No.: US 9,257,492 B2 (45) Date of Patent: Feb. 9, 2016
(54) METHOD FOR PRODUCING A PASSIVE ELECTRONIC COMPONENT, METHOD FOR PRODUCING AN OPTOELECTRONIC ASSEMBLY AND PASSIVE ELECTRONIC COMPONENT	(58) Field of Classification Search CPC H01L 23/5227; H01L 27/0658 USPC 438/329, 957; 257/528, 532 See application file for complete search history.
(71) Applicant: OSRAM OLED GmbH , Regensburg (DE)	(56) References Cited U.S. PATENT DOCUMENTS 6,335,211 B1 * 1/2002 Lee 438/22 6,800,999 B1 * 10/2004 Duggal et al. 315/169.1 (Continued) FOREIGN PATENT DOCUMENTS DE 102009060066 A1 3/2011 DE 112008003787 T5 3/2012 OTHER PUBLICATIONS German Search Report based on Application No. 10 2012 109 142.0(5 pages) dated Jun. 25, 2013. <i>Primary Examiner</i> — Theresa T Doan (74) <i>Attorney, Agent, or Firm</i> — Viering, Jentschura & Partner
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.	
(21) Appl. No.: 14/430,942	
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(87) PCT Pub. No.: WO2014/048639	

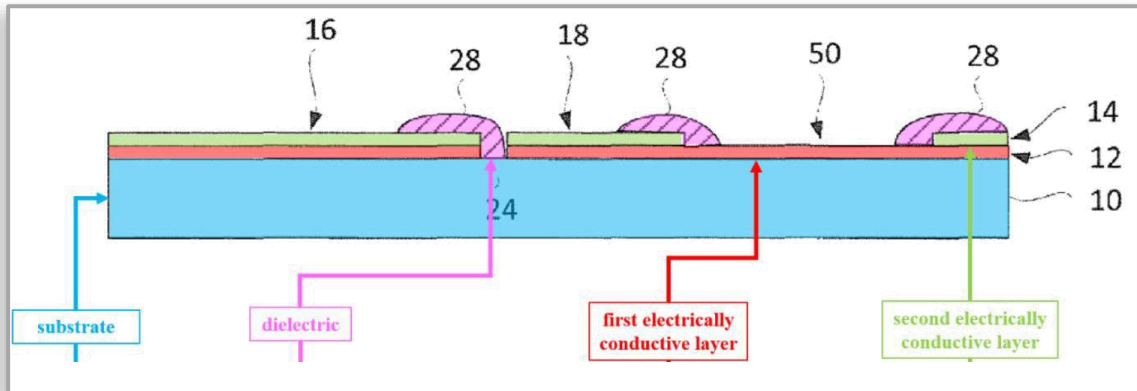
'492 Patent

(19) World Intellectual Property Organization International Bureau		
(43) International publication date March 31, 2011 (03/31/2011)	PCT	(10) International publication number WO 2011/036089 AI
(51) International patent classification: <i>H01L 51/10</i> (2006.01)		Nittendorf (DE). HEUSER, Karsten [DE/DE]; Georg-Frank-Straße 17, 91056 Erlangen (DE).
(21) International file number: PCT/EP2010/063623	(74) Attorneys: EPPING HERMANN FISCHER PATENT-ANWALTSGESELLSCHAFT MBH ; Ridlerstraße 55, 80339 Munich (DE).	
(22) International filing date: September 16, 2010(09/16/2010)		
(25) Filing language: German	(81) Designated countries (unless otherwise indicated, for each available national type of IP right): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.	
(26) Language of publication: German		
(30) Priority information: 10 2009 043 066.0 September 25, 2009 (09/25/2009) DE 10 2009 060 066.3 December 22, 2009 (12/22/2009) DE		
(71) Applicant (for all designated states except US): OSRAM OPTO SEMICONDUCTORS GMBH [DE/DE]; Leibnizstraße 4, 93055 Regensburg (DE).		
(72) Inventors; and (75) Inventors/applicants (only for US): INGLE, Andrew [US/DE]; Anton-Bruckner-Straße 5, 85391 Allershausen (DE). SCHLENKER, Tilman [DE/DE]; Jacklberg 17, 93152		

Ingle

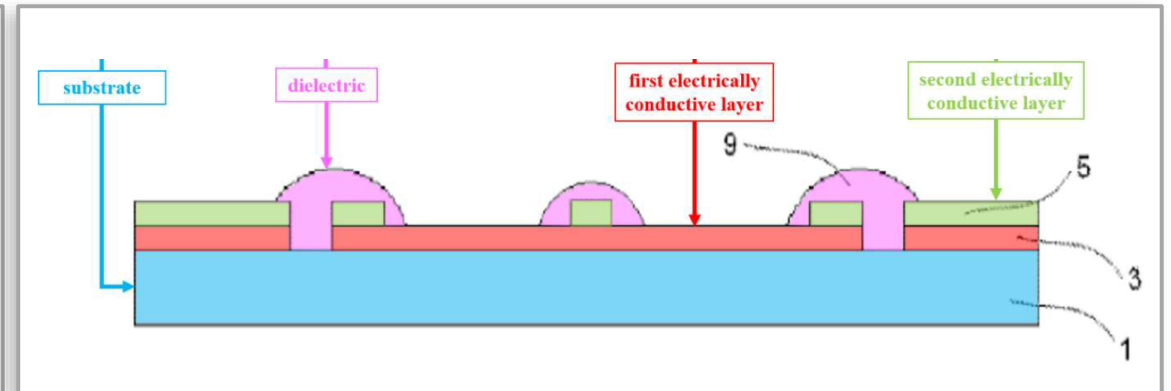
The '492 Patent Uses Substantially the Same Base Structure as Ingle

The '492 Patent's Base Structure



'492 Patent, Fig. 15 (annotated)

Ingle's Base Structure



Ingle, Fig. 1I (annotated)

Ingle Teaches Use of a Structured Process to Avoid the Downsides of Photolithography

With the method according to the invention, it is possible to separate two electrode regions from one another, wherein the electrode regions are structured at a preselected position already during the application of the layers of the electrode regions or later and the insulator applied to the second electrically conductive layer is arranged in the region formed by the structuring. The structuring is usually applied later.

Ingle, 6:9-16

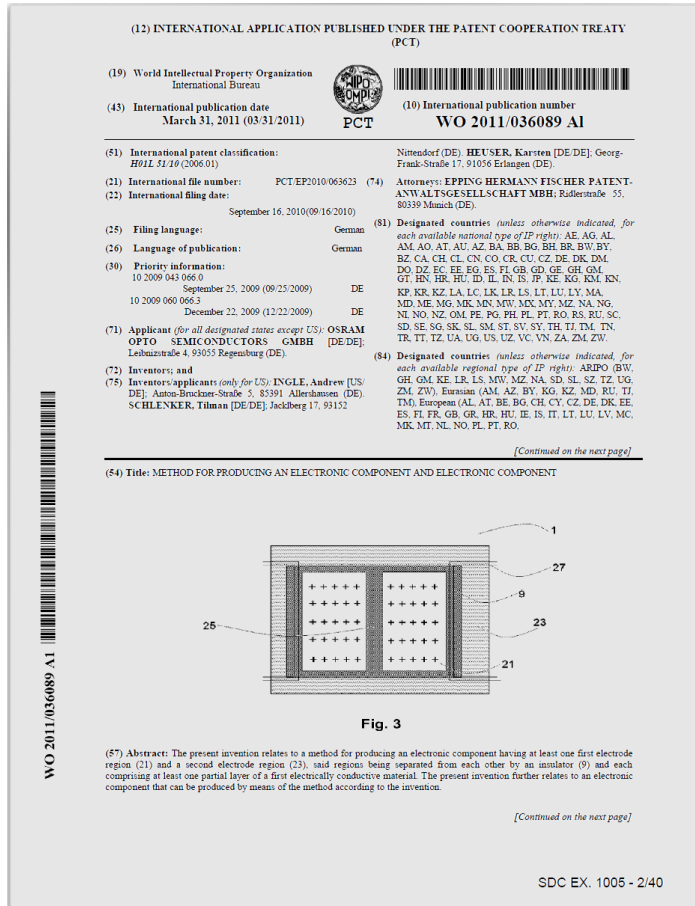
The method according to the invention for producing an electronic component can be used to produce electronic components with cost and time savings. Since each layer of the component can be applied individually and, if necessary, structured according to desire or purpose (as can be seen from the following further developments of the method), time-consuming coating or application steps can thus be avoided and (often expensive) material can also be saved.

Ingle, 7:20-27

The method according to the invention is usually free of photolithographic steps and can therefore be used as a cost-effective method for producing an electronic component, such as an organic light-emitting diode. By means of the method according to the invention, it is possible to produce an electronic component with a robust design. The method according to the invention can therefore also be used for the mass production of electronic components.

Ingle, 18:7-14

Ingle Teaches That a Capacitor and/or an OLED Can Be Built on Its Base Structure



An "electronic component" which can be produced by the method according to the invention can be, but is not limited to, a transistor, a capacitor, a thermistor, an organic electronic component, such as an organic light-emitting diode, a solar cell, and the like.

Ingle, 6:3-7

The electronic component, for example an OLED, can now be produced on the substrate layer prepared in this way using a conventional process.

Ingle, 21:34-36

Ingle

See Pet., 9-12

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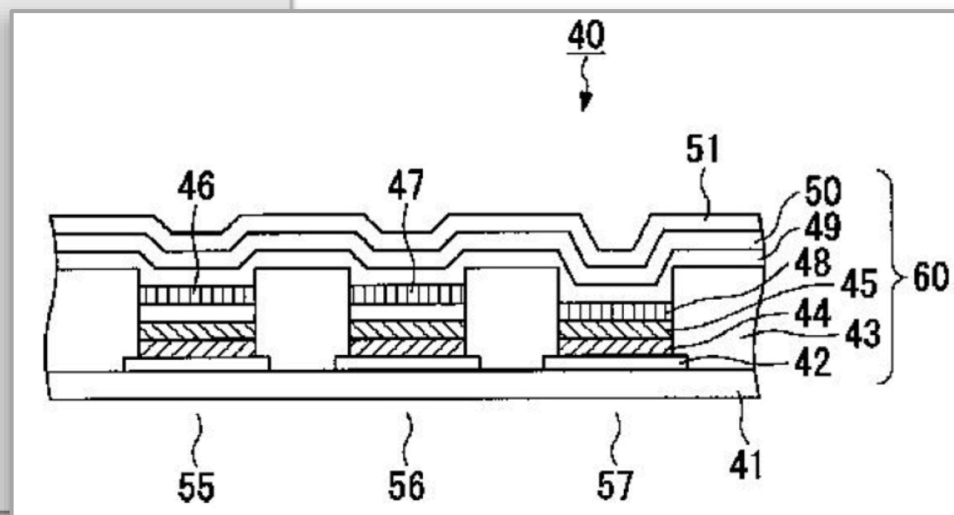
Demonstrative Exhibit – Not Evidence 10

Hasei Discloses Building an OLED

(19) Japanese Patent Office (JP)		(12) Patent Application Gazette (A)		(11) Published Application No. JP2003-317610 (P2003-317610A)	
				(43) Appl. Published: Nov. 7, 2003	
(51) Int. Cl. ⁷	ID Number	FI		Theme code (ref.)	
H 01 J	9/02	H 01 J	9/02	F	3K007
	11/02		11/02	B	4M104
H 01 I	21/288	H 01 I	21/288	Z	5C027
H 05 B	33/10	H 05 B	33/10	A	5C040
	33/14		33/14		
Request for Examination: No		Number of Claims: 9 OL Total pages: 9			
		Continued on last page			
(21) Filed Appl. No.: 2002-116693 (P2002-116693)		(71) Applicant: 000002369 SEIKO EPSON CORPORATION			
(22) Filed: Apr. 18, 2002		4-1, Nishi-Shinjuku 2-chome, Shinjuku-ku, Tokyo			
		(72) Inventor: Hironobu HASEGAWA			
		c/o Seiko Epson Corporation 3-5, 3-chome, Owa, Suwa-shi, Nagano-ken			
		(74) Agent or Attorney: 100095728 Masataka KAMIYANAGI, Patent Attorney			
		(2 others)			
		Continued on last page			
(54) [Title of the Invention] PATTERN FORMING METHOD, DEVICE, ELECTRONIC APPARATUS, AND DEVICE MANUFACTURING METHOD					
(57) ABSTRACT					
[PROBLEM]					
To provide a pattern forming method, a device, an electronic apparatus, and a method for manufacturing a device, which are capable of reducing waste in the manufacturing process.					
[RESOLUTION MEANS]					
A liquid or fluid containing indium tin oxide (ITO) is discharged from an inkjet head of a droplet discharging device onto a desired position on a substrate, thereby patterning the indium tin oxide on the substrate (step S1).					

[0039] Although not depicted, the organic EL device 40 of the present embodiment is an active matrix type, and actually, a plurality of data lines and a plurality of scanning lines are arranged in a lattice pattern on the substrate 41. An organic

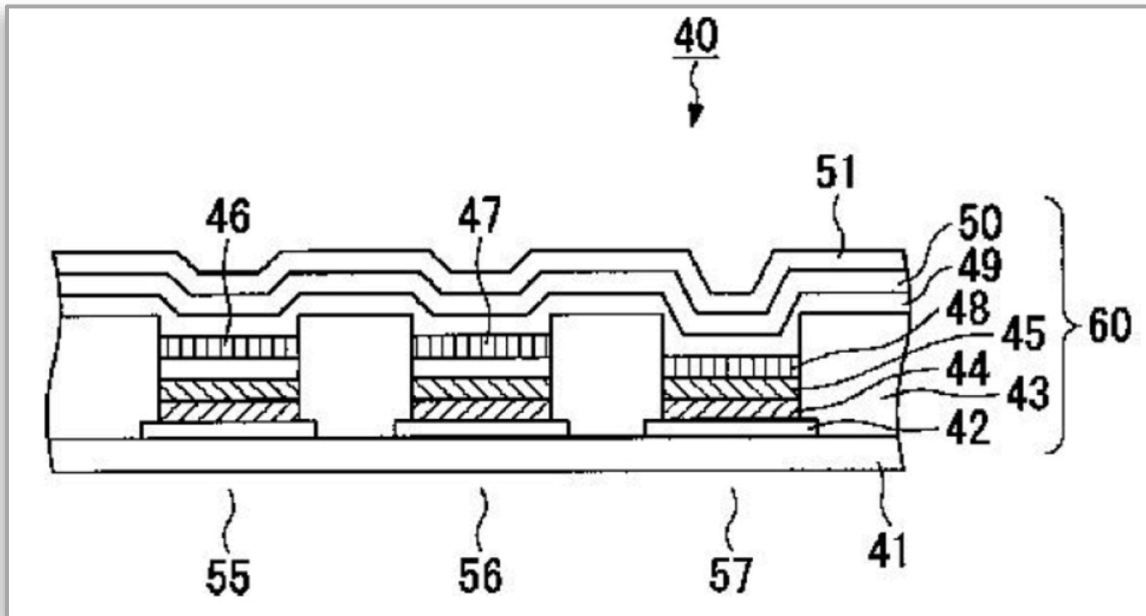
Hasei, [0039]



Hasei

Hasei, Fig. 3

Hasei Discloses Building an OLED Using a Structured Process



Hasei, Fig. 3

gold (Au), silver (Ag), and the like. The negative electrode 50 may be formed by the droplet discharging method depicted in the description of step S1 in FIG. 1, or may be formed by photolithography or etching.

Hasei, [0037]

a droplet discharging device. With this method, the transparent electrode material is discharged only onto the portion of the substrate where the conductive pattern is to be formed. On the other hand, when a conductive pattern is

Hasei, [0005]

Hasei Teaches Use of a Structured Process to Avoid the Downsides of Photolithography

PROBLEMS TO BE SOLVED BY THE INVENTION

However, with the conventional method of providing a conductive pattern, most of the conductive material formed over the entire surface of the substrate (other than the conductive pattern portion) must be removed by etching, and the removed conductive material is wasted in the manufacturing process. Furthermore, the conventional method of providing a conductive pattern requires a photomask to be used in the photolithography process, which lengthens the manufacturing process and requires that a photomask be made each time the model of the conductive pattern is changed, resulting in increased manufacturing costs and a longer manufacturing period. Furthermore, conventional conductive patterns have the problem that even a single break in the wiring of the conductive pattern provided on the substrate means that the prescribed function cannot be achieved.

[0004] An object of the present invention is to provide a pattern forming method, a device, electronic apparatus, and a method for manufacturing a device, which can reduce waste and eliminate disconnections in the manufacturing process related to a substrate.

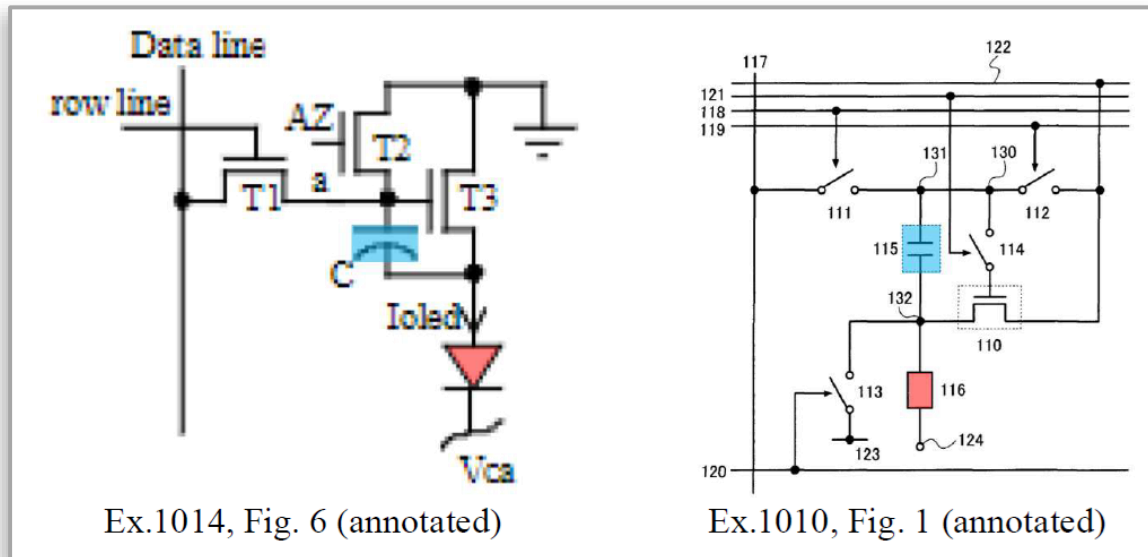
Hasei, [0003]-[0004]

MEANS FOR SOLVING THE PROBLEM

In order to achieve the aforementioned object, the pattern forming method of the present invention is a pattern forming method for forming a wiring pattern at a prescribed location on a substrate, wherein the wiring pattern is formed by discharging a liquid containing a conductive material using a droplet discharging device. With this method, the transparent electrode material is discharged only onto the portion of the substrate where the conductive pattern is to be formed. On the other hand, when a conductive pattern is formed by photolithography, etching, or the like, a transparent electrode material must first be provided over the entire surface of the substrate. Therefore, with the method of the present invention, the amount of transparent electrode material wasted in the manufacturing process can be significantly reduced compared to a conventional method. Furthermore, with this method, there is no need to create a photomask, so the manufacturing time required for forming a conductive pattern of a transparent electrode or the like can be shortened, and manufacturing costs can be reduced.

Hasei, [0005]

POSITAs Understood That Building an AMOLED Entails Building a Capacitor Next to the OLED



5 Q And what is an active matrix display?

6 A It's got transistors and capacitors and

7 resistors, you know, a circuit associated with the

8 individual subpixels to control and hold the

9 on/off state of each of those subpixels.

10 Q And you mentioned it having capacitors.

11 What is the purpose of a capacitor in an active

12 matrix display?

13 A To hold the charge.

...

10 Q Do any of the claims of the '492 patent

11 call out an integrated circuit?

12 A It's in the context, like we talked

13 about. Yeah. I mean, that's the whole reason why

14 you put a capacitor next to an optoelectronic

15 device, to integrate them together. That's

16 exactly what it's talking about.

Pet., 22

20 Q. Does Hasei disclose fabricating a

21 capacitor?

22 A. I think the term "capacitor" doesn't

23 appear in Hasei, but it does disclose active matrix

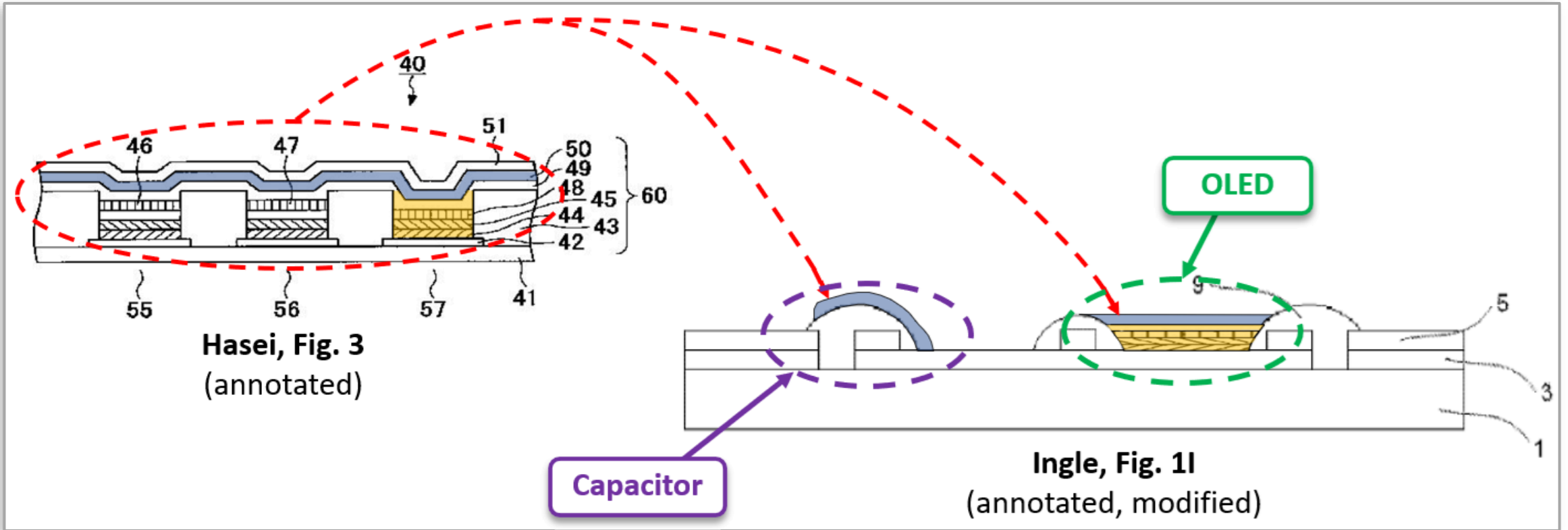
24 displays, which would require a capacitor and a

25 pixel.

Ex.2006 (Kattamis Tr.), 89:20-25

Ex.1033 (Pattison Tr.), 29:5-13, 86:10-16

Using Hasei's Process for Building an AMOLED on Ingle's Base Structure

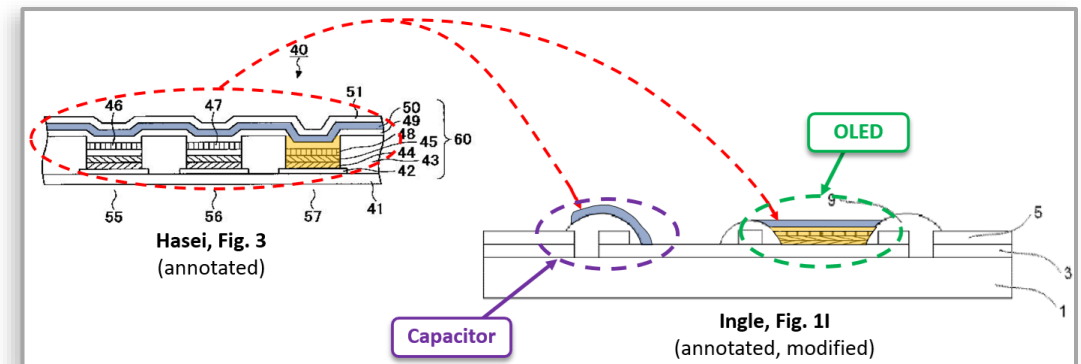


Reply, 16
(certain highlighting omitted)

A POSITA Would Have Been Motivated to Form the Capacitor on Ingle's Base Structure

162. As explained, it would have been obvious for a POSITA to form an electrode above the left-side dielectric in Ingle's base structure using Hasei's droplet discharge method, or Ingle's vapor-deposition method, in order to form a capacitor in series with the OLED. *See* Section XI.A.1. A POSITA would readily understand that Ingle's capacitor could be completed on Ingle's base structure by applying an electrode above the dielectric. This is because a capacitor is a passive electronic element that is comprised of two conductors separated by an insulator (*see* Section X.A), and Ingle's base structure in the first contact region already provides a conductive layer and an insulative layer, above which a second electrode may readily be applied. Ingle further informs the POSITA to complete the capacitor by applying a cathode in a structured fashion. *See, e.g.*, Ex. 1005, Ingle, 7:20-24 ("each layer of the component can be applied individually"); 18:7-10 (claimed invention "is usually free of photolithographic steps").

Ex.1003 (Kattamis Decl.), ¶ 162; *see also id.*, ¶¶ 120-25



Reply, 16
(certain highlighting omitted)

Using Hasei's Method to Form Both the OLED's and Capacitor's Cathode Would Have Been Obvious

168. While Ingle leaves open how a POSITA may complete the capacitor (*i.e.*, apply the cathode), Ingle's teachings about the benefits of structured application would have made it obvious to the POSITA to adopt such technique. *See, e.g.*, Ex. 1005, Ingle at 18:7-10 (claimed method "is usually free of photolithographic steps"). Hasei also advocates for a structured application process (*e.g.*, inkjet printer). *See, e.g.*, Ex. 1007, Hasei at [0005], [0007], [0014]-[0015], [0037].

169. Additionally, as elaborated below in relation to Element 10[i], a POSITA would understand Ingle and Hasei as teaching structured application of the OLED's cathode. *See, e.g.*, Ex. 1005, Ingle, at 21:34-22:5 (forming an OLED comprises "vapor-deposit[ing] onto the substrate layer in subsequent processing steps" "the semiconducting, light-emitting organic layers and the second electrode layer, for example a cathode layer."); *see also* Ex. 1007, Hasei at [0037] ("The negative electrode 50 may be formed by the droplet discharging method.").

170. Ingle and Hasei thus disclose forming the cathode of *each of* the OLED and the capacitor using additive techniques. The POSITA would recognize that both cathodes may advantageously be formed during the same manufacturing step; it is well understood that reducing fabrication steps lowers costs and risk of manufacturing defects. A POSITA would have a reasonable expectation of success considering the teachings in Ingle and Hasei. *See, e.g.*, Ex. 1007, Hasei at [0005], (structured application allows material to be "discharged only onto the portion of the substrate where the conductive pattern is to be formed."), [0007] (structured application allows material to be "discharged only onto the portion of the substrate where a conductive pattern that will become a structural element of the device is to be formed."); *see also* Ex. 1005, Ingle at 15:19-24 (invention allows applying "material at specific points by means of a printing process.").

Ex.1003 (Kattamis Decl.), ¶ 170

Ex.1003 (Kattamis Decl.), ¶¶ 168-69

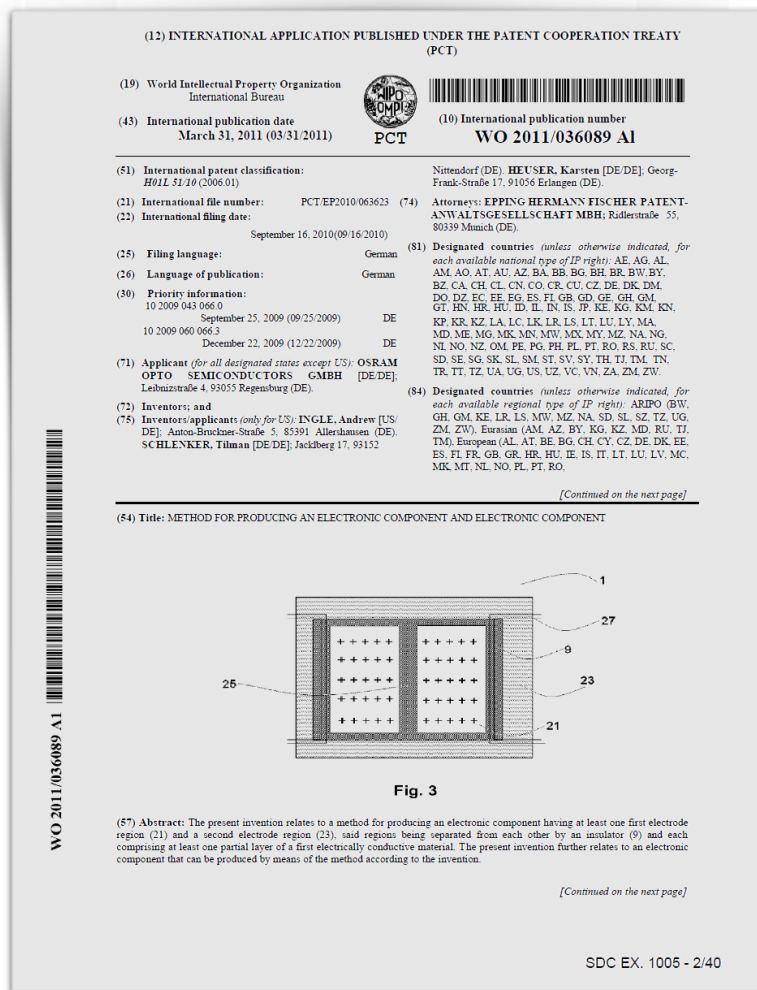
Ground 1 – Issues in Dispute

- Pictiva acknowledges that Ingle discloses limitations 1[a]-[d], 10[b]-[e], [g], and 16[a]-[d]. *See* POR, 9.
- It is undisputed that Ingle in view of Hasei renders obvious limitation 10[h] and the additional limitations of dependent claims 2 and 8-11.
- Pictiva only disputes that Ingle and Hasei fail to render obvious:
 - “applying an electrically conductive electrode layer in a structured fashion”;
 - “applying an electrically conductive layer . . . above the first contact region; and”
 - a working capacitor.

Ground I – “Applying an Electrically Conductive Electrode Layer in a Structured Fashion”

Claims 1[e], 10[f], 10[i], and 16[e]

Ingle Teaches Structuring Its Electrode Regions via Printing



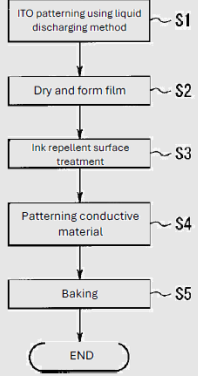
With the method according to the invention, it is possible to separate two electrode regions from one another, wherein the electrode regions are structured at a preselected position already during the application of the layers of the electrode regions or later and the insulator applied to the second electrically conductive layer is arranged in the region formed by the structuring. The structuring is usually applied later.

If the structuring is already present (i.e. is applied "earlier"), this can be done by applying the first and second electrically conductive layers or parts thereof to the substrate, for example by printing, by deposition with the aid of SAMs (self-assembling monolayers) and the like.

Ingle, 6:9-23

Ingle

Hasei Teaches That Its Cathode (Negative Electrode 50) May Be Structured

(19) Japanese Patent Office (JP)	(12) Patent Application Gazette (A)	(11) Published Application No. JP2003-317610 (P2003-317610A)	(43) Appl. Published: Nov. 7, 2003
(51) Int. Cl. ⁷	ID Number	FI	Theme code (ref.)
H 01 J	9/02	H 01 J	F 3K007
	11/02		B 4M104
H 01 I	21/288	H 01 I	Z 5C027
H 05 B	33/10	H 05 B	5C040
	33/14		A
Request for Examination: No		Number of Claims: 9 OL Total pages: 9 Continued on last page	
(21) Filed Appl. No.: 2002-116693 (P2002-116693) (22) Filed: Apr. 18, 2002	(71) Applicant: 000002369 SEIKO EPSON CORPORATION 4-1, Nishi-Shinjuku 2-chome, Shinjuku-ku, Tokyo		
	(72) Inventor: Hironobu HASEGAWA c/o Seiko Epson Corporation 3-5, 3-chome, Owa, Suwa-shi, Nagano-ken		
	(74) Agent or Attorney: 100095728 Masataka KAMIYANAGI, Patent Attorney		
	(2 others)		
Continued on last page			
(54) [Title of the Invention] PATTERN FORMING METHOD, DEVICE, ELECTRONIC APPARATUS, AND DEVICE MANUFACTURING METHOD			
(57) ABSTRACT [PROBLEM] To provide a pattern forming method, a device, an electronic apparatus, and a method for manufacturing a device, which are capable of reducing waste in the manufacturing process. [RESOLUTION MEANS] A liquid or fluid containing indium tin oxide (ITO) is discharged from an inkjet head of a droplet discharging device onto a desired position on a substrate, thereby patterning the indium tin oxide on the substrate (step S1).			
			
- 1 -			
SDC EX. 1007 - 2/10			

gold (Au), silver (Ag), and the like. The negative electrode 50 may be formed by the droplet discharging method depicted in the description of step S1 in FIG. 1, or may be formed by photolithography or etching.

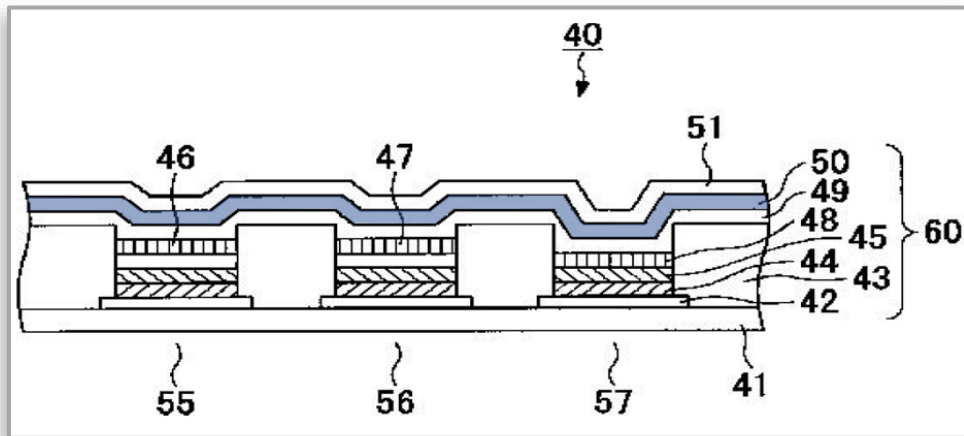
Hasei, [0037]

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Hasei, [0005]

Hasei

Hasei's Figure 3 Embodiment Can Be Structured



Hasei, Fig. 3

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Hasei, [0037]

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Hasei, [0005]

Hasei's Figure 3 Embodiment Can Be Structured



[D]rawings in a patent need not illustrate the full scope of the invention.

Arlington Indus., Inc. v. Bridgeport Fittings, Inc., 632 F.3d 1246, 1254 (Fed. Cir. 2011)

Hasei's Figure 3 Embodiment Can Be Structured

17 Q. Looking at Figure 3 of Hasei, do you see
18 any structure in layer 50?
19 ATTORNEY WEIDENFELLER: Objection.
20 THE WITNESS: In looking in this one
21 embodiment, which is a cross-section, I have
22 no plan view. Right here in this embodiment,
23 it shows a layer that's continuous, for 50,
24 but there is a disclosure clearly in the
25 patent that says that negative electrode may
1 be formed by droplet discharge method.

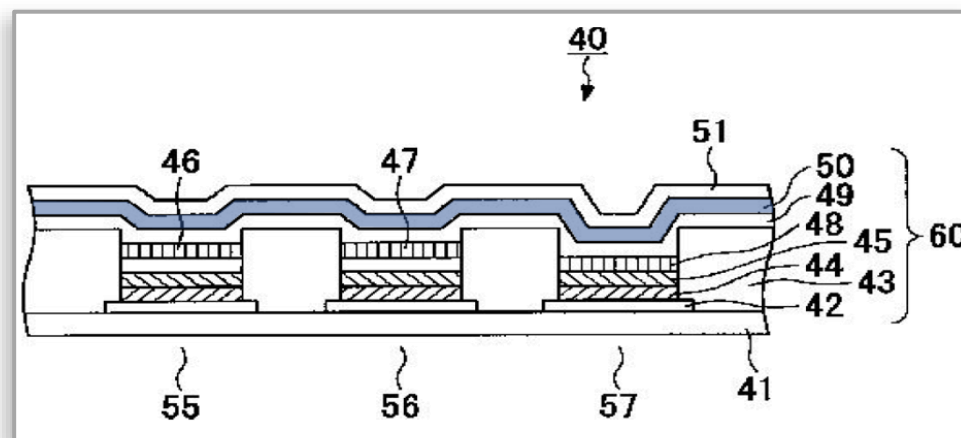
Ex.2006 (Kattamis Tr.), 74:17-75:1

15 Q Let's look at Figure 9 for a moment.
16 Figure 9 is also a plan view, right?
17 A That's right.
18 Q And one of the things that's shown in
19 the plan view, among other things, is the shapes
20 of the second and third trenches 40 and 42, right?
21 A That's right.
22 Q Now, if I took a horizontal
1 cross-section of Figure 9, right in the middle,
2 you wouldn't actually see either of those
3 trenches, 40 or 42, correct?
4 MR. WARRICK: Objection. Form.
5 A Yeah, that's correct.

Ex.1033 (Pattison Tr.), 72:15-73:5

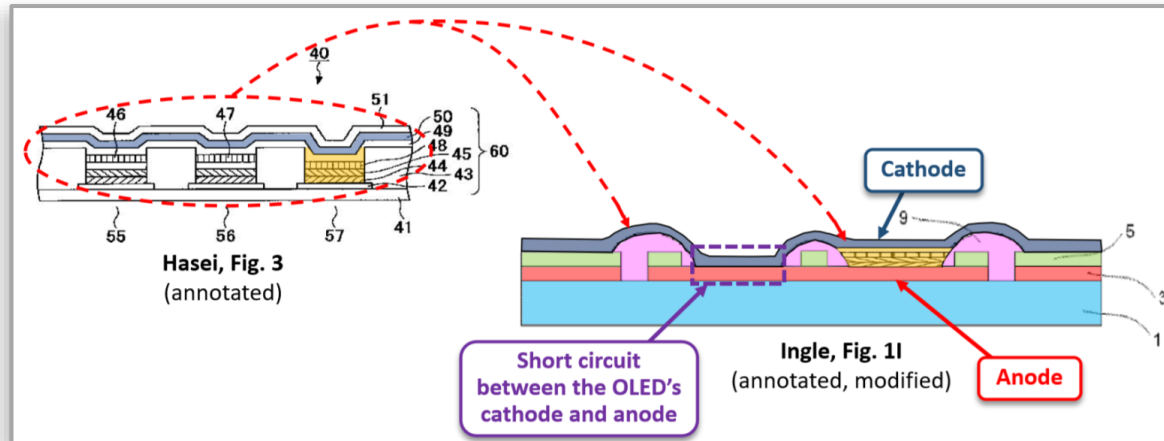
76. Furthermore, a POSITA would understand that the negative electrode 50 described in Hasei and depicted in Figure 3 must be continuous across the subpixels depicted in Figure 3. That is because negative electrode 50 is a common electrode to all of the sub-pixels (and most likely multiple pixels), which greatly simplifies the circuit design and the common electrode with a common voltage is described in EX1010 and EX1014 provided by Dr. Kattamis.

Ex.2001 (Pattison Decl.), ¶ 76



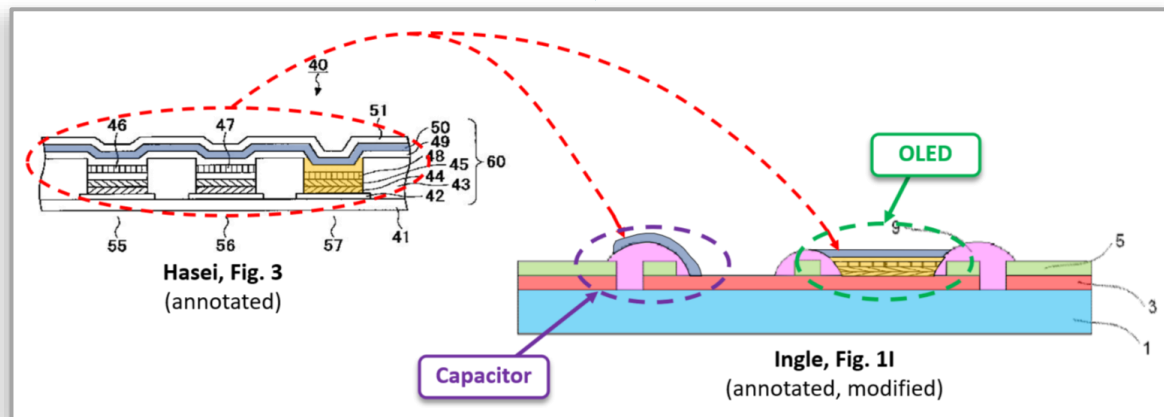
Hasei, Fig. 3

In Fact, Applying Electrode 50 in a Non-Structured Fashion Would Require Subsequent Etching



Reply, 16

Required Etching



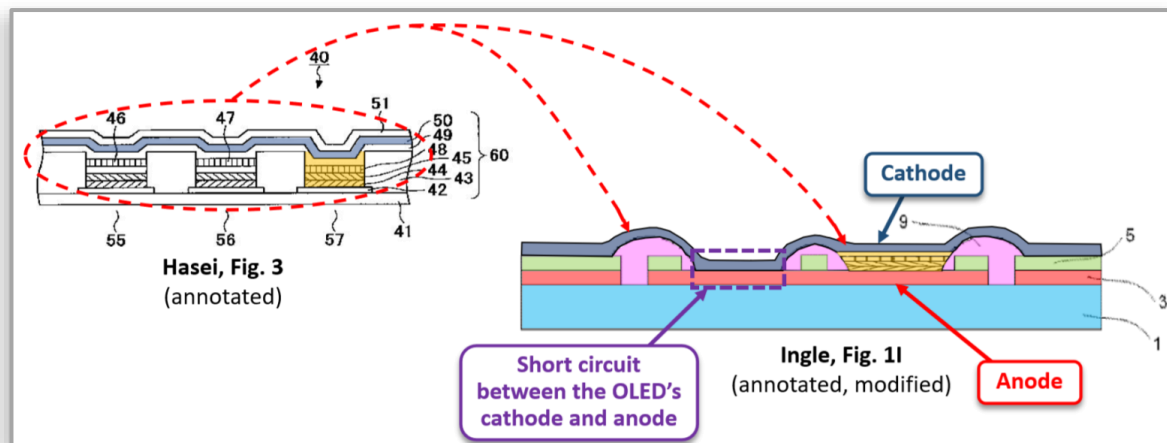
Reply, 16

See Reply, 16

19. Moreover, a POSITA would understand that applying negative electrode 50 in a planar fashion to the device in Ingle would create a short circuit between the OLED's anode and cathode, as illustrated below.

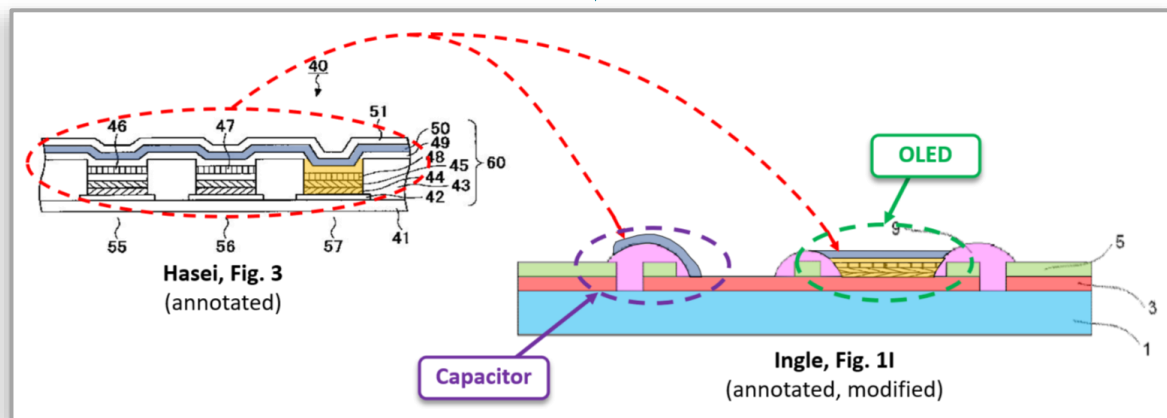
Ex.1030 (Kattamis Reply Decl.), ¶ 19

Moreover, A POSITA Would Avoid Subsequent Etching, as It Would Damage the OLED's Organic Material



Reply, 16

Required Etching



Reply, 16

See Reply, 16

remove the overlap that creates the short circuit. However, a POSITA would understand that etching, e.g., photolithography, should not be used after the organic layers of an OLED have been deposited—e.g., when forming a cathode atop the OLED—as photolithography can damage the organic layers. *See, e.g.*, Ex. 1023, Kahn at 16 (“The harsh conditions required for dissolving resists, etching the underlying layers, and removing the photoresist will destroy the activity of most organic electronic materials.”).

Ex. 1030 (Kattamis Reply Decl.), ¶ 19

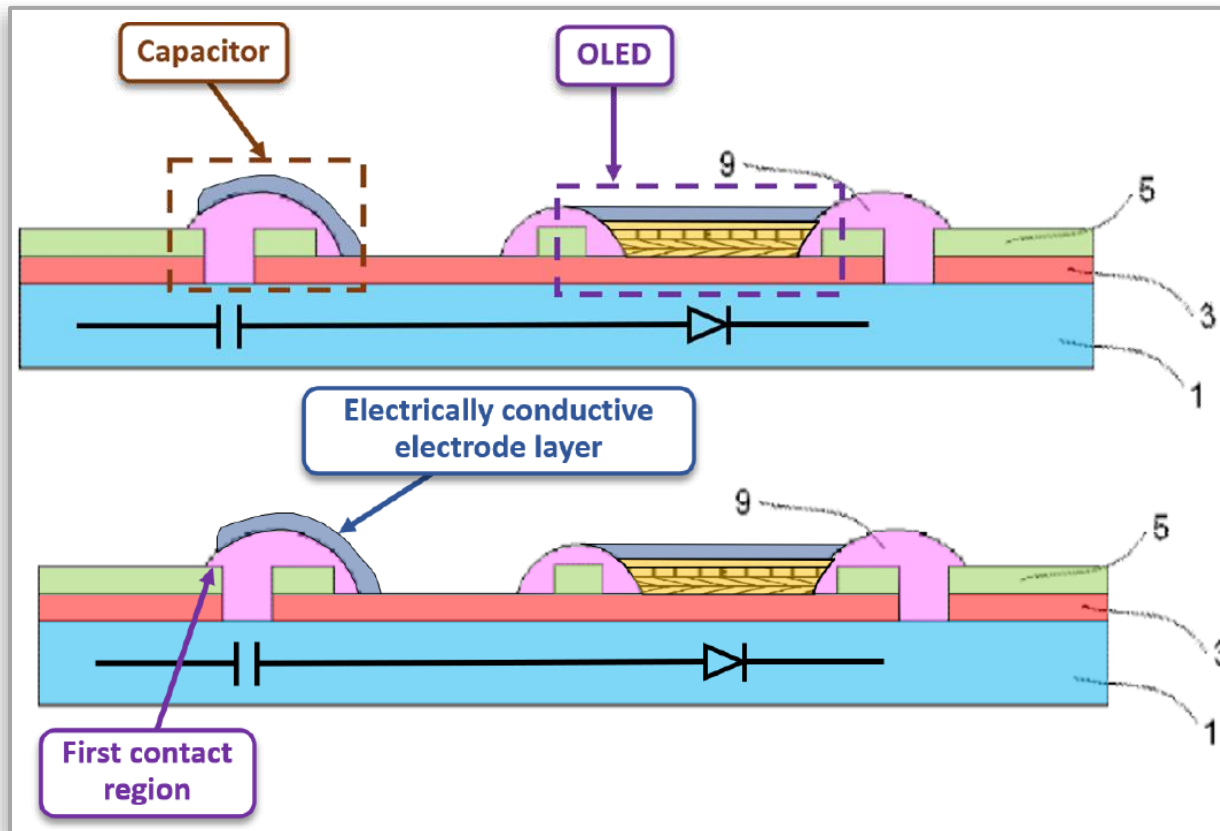
The method according to the invention is usually free of photolithographic steps and can therefore be used as a cost-effective method for producing an electronic component, such as an organic light-emitting diode. By means of the method

Ingle, 18:7-10

Ground I – “Applying an Electrically Conductive Electrode Layer . . . Above the First Contact Region”

Claims 1[e], 10[f], 16[e]

Forming a Capacitor on Ingle's Structure Results in “an Electrically Conductive Layer . . . Above the First Contact Region”



Ex.1003, ¶166. A POSITA would understand that the degree to which both the dielectric (pink) and the electrically conductive layer (grey) extend over the first contact region may be adjusted to fine tune the capacitance of the capacitor. See Ex.1003, ¶167-70.

Pet., 38

Reply, 17

Adjusting the Dielectric and Electrically Conductive Layer to Fine Tune Capacitance Was Well Within a POSITA's Skill

167. A POSITA would understand that the degree to which both the dielectric (pink) and the electrically conductive layer (grey) extend over the first contact region may be adjusted to fine-tune the capacitance of the capacitor. It is well understood that larger plates provide greater capacity to store electric charge, and thus, larger plates (with greater area) allow higher capacitance. Here, conductive material deposited on the substrate functions as one plate, while the electrically conductive layer deposited on the dielectric acts as the second plate. The area of the electrically conductive layer (second plate) can readily be controlled due to structured application, as both Ingle and Hasei teach (see Section XI.A.1.c), and adjusting the area would adjust the capacitance.

Ex.1003 (Kattamis Decl.), ¶ 167

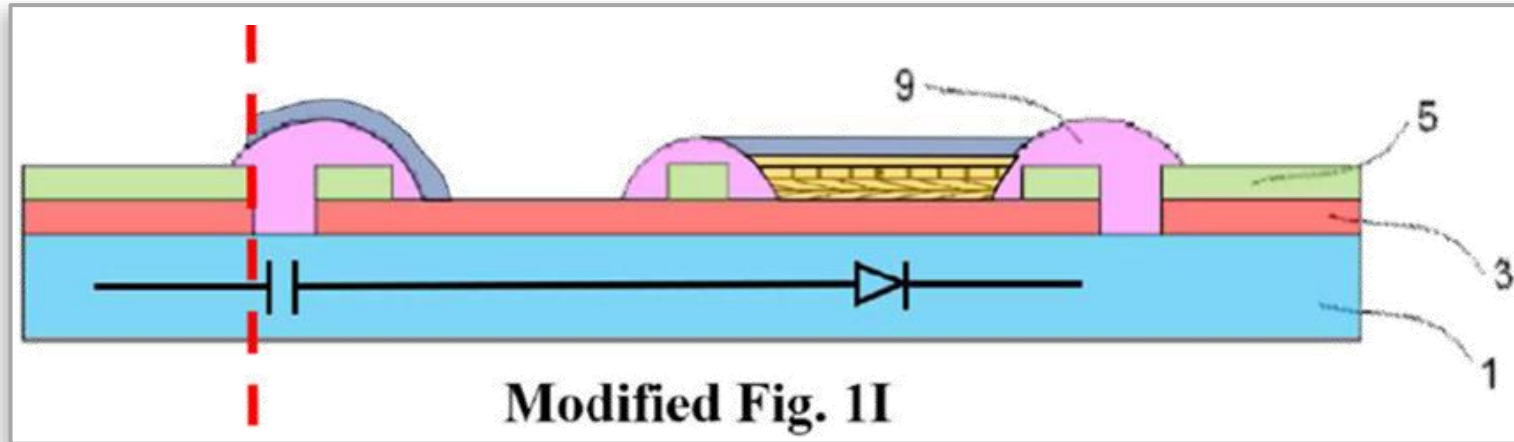
3 Q And you said that capacitors have been
4 known for a long time. Are those fundamental
5 components of the two electrodes, the dielectric
6 between them, have those been known for a long
7 time as well?
8 A Yes.
9 Q And would a person of ordinary skill in
10 the art understand that if you had an electrode
11 and a dielectric on top of it, that to finish the
12 capacitor, you'd have to form an opposite
13 electrode on the other side of the dielectric?
14 MR. WARRICK: Objection. Form.
15 A Yeah. I mean, it depends on what
16 you're trying to do. But they would understand
17 that. They would understand that you need to
18 have, you know, control over the capacitor
19 performance and over the -- you know, these
20 parameters that define the performance. And in a
21 circuit, in any circuit or circuit board, there
22 can be undesirable capacitance that occur that are

Ex.1033 (Pattison Tr.), 61:3-22

1 kind of out of control, that you want to avoid, so
2 that the -- you know, when you are trying to make
3 a capacitor, you're trying to make it with defined
4 performance, controllable performance.
5 Q And the parameters that you've just
6 been discussing, are those what you have in
7 paragraph 45, when you talk about the critical
8 parameters?
9 MR. WARRICK: Objection. Form.
10 A Yeah, those are the critical
11 parameters, as well as, you know, consistency and
12 avoiding shorts and stuff like that, if you're
13 doing it in a semiconductor system context.
14 Q And were those critical parameters
15 known to persons of ordinary skill in the art
16 prior to the '492 patent?
17 A Yes.

Ex.1033 (Pattison Tr.), 62:1-17

Pictiva's Expert Concedes That Its "Broken Red Line" Demonstrates Overlap



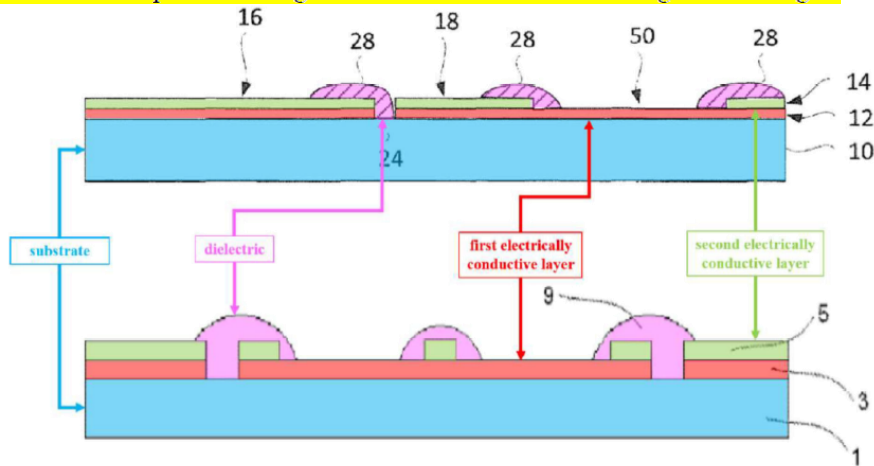
POR, 42-43

19 Q And so, actually, this does indicate
20 that there is some overlap between the gray layer
21 and the green layer, right?
22 A There's overlap, but it's, like, a very
1 small area. Like, it goes back to what you would
2 do if you're making an actual capacitor, is you
3 would want to have control over that area, and you
4 want to have a consistent thickness. That's the

Ex.1033 (Pattison Tr.), 80:19-22

Pictiva Improperly Assumes the '492 Patent's and Ingle's Figures Are To Scale

structures and methods disclosed in Ingle differ in significant and material ways. For example, the application of the dielectric results in significant overlap of the first contact region in the '492 Patent but not in Ingle. This is evident in Petitioner's own annotated comparison of Figure 15 of the '492 Patent and Figure II of Ingle:



Pet. 12 (comparing '492 Patent, Fig. 15 (annotated, top) with Ingle, Fig. II (annotated, bottom)). As these annotated figures demonstrate, the leftmost dielectric 28 applied in the '492 Patent significantly covers region 16, whereas in Ingle, the leftmost dielectric barely covers the corner of the equivalent portion of the second electrically conductive layer alleged to constitute the first contact region. EX2001,



The district court erred in not applying the principles set forth in our prior precedents that arguments based on drawings not explicitly made to scale in issued patents are unavailing.

Nystrom v. TREX Co., Inc., 424 F.3d 1136, 1149 (Fed. Cir. 2005)

The Figures in the '492 Patent and Ingle Are Explicitly Not Drawn to Scale

The present invention is illustrated below without limiting the generality with reference to the figures. In the drawing, the same reference signs denote the same or identical elements, in which:

Ingle, 18:21-22

In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the disclosed embodiments. In the following description, various embodiments described with reference to the following drawings, in which:

'492 Patent, 7:11-14

4 Q And electrode 38 is shown as following
5 the curvature of the dielectric?

6 MR. WARRICK: Objection. Form.

7 A Yeah, and this is, like I said, not an
8 engineering drawing, but it's showing it as kind
9 of -- yeah, it has a rounded structure on top.

10 Q And you noted that this is not an
11 engineering drawing. Why did you note that?

12 A Well, because it looks like it's hand
13 drawn, not a picture or -- you know, with
14 tolerances or dimensions involved.

...

1 Q From a figure like this, though, would
2 you read into whether or not the dielectric is
3 rounded?

4 MR. WARRICK: Objection. Form.

5 A It's -- I don't know, the rounding's a
6 little bit subtle in the dielectric. I mean, it's
7 noticeable. I wouldn't -- and I'd say, within the
8 context of the patent, where they do talk about a
9 kind of a melting process, it might be somewhat
10 rounded. So, yeah, I would say there could be
11 some rounding, but that's not necessarily rounded.

Ex. 1033 (Pattison Tr.), 74:4-75:11 (discussing the '492 Patent)

Demonstrative Exhibit – Not Evidence 32

Pictiva Disregards Explanation That Forming an Electrode Above Ingle's Left-Side Dielectric *Would* Have Been Obvious

The Petition attempts to address this problem by citing its expert's declaration to support the proposition that "[a] POSITA would readily understand that Ingle's capacitor *could be* completed on Ingle's base structure by applying an electrode above the dielectric in the first contact region." Pet. 36 (citing EX1003, ¶ 162). Obviousness, however, concerns not only what "could be" done, but also what would have been done. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015).

POR, 46

This element would have been obvious to a POSITA based on Ingle in view of Hasei. Ex.1003, ¶¶161-71. As explained above, it would have been obvious for a POSITA to form an electrode above the left-side dielectric in Ingle's base structure using Hasei's droplet discharge method to form a capacitor connected to the OLED. *See supra* VIII.A.1; Ex.1003, ¶162. A POSITA would readily understand that Ingle's capacitor could be completed on Ingle's base structure by applying an electrode above the dielectric in the first contact region, Ex.1003, ¶162, and Ingle informs the POSITA to apply the electrode in a structured fashion. *See, e.g.*, Ingle, 7:20-24, 18:7-10; *see also* Ex.1003, ¶162.

Pet., 36

The Petition Explained in Detail Why a POSITA *Would* Have Been Motivated to Use Hasei's Teachings to Form an OLED

1. Motivation to Combine Ingle and Hasei

A POSITA would have been motivated to combine Ingle and Hasei. Ex.1003, ¶¶108-25.

- a) Ingle contemplates forming an optoelectronic assembly using a conventional process, like that of Hasei.

. . .

- b) Both Ingle and Hasei teach forming an OLED device using structured application of layers, and Ingle teaches a substrate suitable for this purpose.

A POSITA would recognize the electronic components contemplated in Ingle—e.g., “a capacitor” and “an organic electronic component, such as an organic light-emitting diode” (Ingle, 6:3-7)—as conventional components of an optoelectronic assembly. Ex.1003, ¶¶120-121. A POSITA would understand that such OLED devices typically require passive circuit components, and that placing capacitors in close proximity (or directly connected) to optically functional layers are a conventional way to form such devices. Ex.1003, ¶¶101-07; 120-22. For instance, pixel circuits were already widely used in OLED mobile phone screens as of the '492 patent, Ex.1003, ¶123, and it was well understood that such circuits (as shown below) rely on OLEDs in conjunction with common passive components like transistors and capacitors. *Id.*, ¶101-07.

Ingle leaves open how to finish forming a capacitor on its base structure, *i.e.*, how to apply the cathode. Nonetheless, given Ingle's emphasis on applying layers in a structured manner, it would have been obvious to a POSITA to apply the capacitor's cathode in such manner. For example, Ingle touts that its method “is usually free of photolithographic steps” (Ingle, 18:7-10), and that “each layer of the component can be applied individually and, if necessary, structured according to desire or purpose.” *Id.*, 7:20-24. Hasei similarly advocates for a structured application process, *e.g.*, using a droplet discharge device like an inkjet printer, rather than photolithography. *See, e.g.*, Hasei, ¶¶14-15, 37. Hasei explains that using such a method, the electrode material “is discharged only onto the portion of the substrate where the conductive pattern is to be formed,” and thus wastage of electrode material is “significantly reduced.” *Id.*, ¶¶5, 7. Hasei further teaches that, because there is no need to create a photomask, “the manufacturing time required for forming a conductive pattern . . . can be shortened.” *Id.*

Pet., 18-26

The Petition Explained in Detail How a POSITA Would Have Formed the Capacitor on Ingle's Base Structure

This element would have been obvious to a POSITA based on Ingle in view of Hasei. Ex.1003, ¶¶161-71. As explained above, it would have been obvious for a POSITA to form an electrode above the left-side dielectric in Ingle's base structure using Hasei's droplet discharge method to form a capacitor connected to the OLED. *See supra* VIII.A.1; Ex.1003, ¶162. A POSITA would readily understand that Ingle's capacitor could be completed on Ingle's base structure by applying an electrode above the dielectric in the first contact region, Ex.1003, ¶162, and Ingle informs the POSITA to apply the electrode in a structured fashion. *See, e.g.*, Ingle, 7:20-24, 18:7-10; *see also* Ex.1003, ¶162.

Pet., 36

The Petition Explained Why Using Hasei's Method to Form Both the OLED's and Capacitor's Cathode Would Have Been Obvious

above the dielectric in the first contact region, Ex.1003, ¶162, and Ingle informs the POSITA to apply the electrode in a structured fashion. *See, e.g.*, Ingle, 7:20-24, 18:7-10; *see also* Ex.1003, ¶162.

Hasei similarly teaches applying the cathode in a structured fashion. In particular, Hasei deposits material using “an inkjet head of a droplet discharging device,” *i.e.*, “inkjet device” (Hasei, ¶15), and so “the electrode material is discharged only onto the portion of the substrate where the conductive pattern is to be formed.” *Id.*, ¶5. Similarly, the '492 patent contemplates applying materials “in a structured fashion . . . for example by printing, for example inkjet printing.” '492 patent, 1:66-2:19 (“‘applying in a structured fashion’ means . . . that the desired structure is already formed during the application of the corresponding layer” and “[t]he area to be coated is thus coated only in partial regions dependent on the desired structure.”); Ex.1003, ¶163-65.

Pet., 36-37

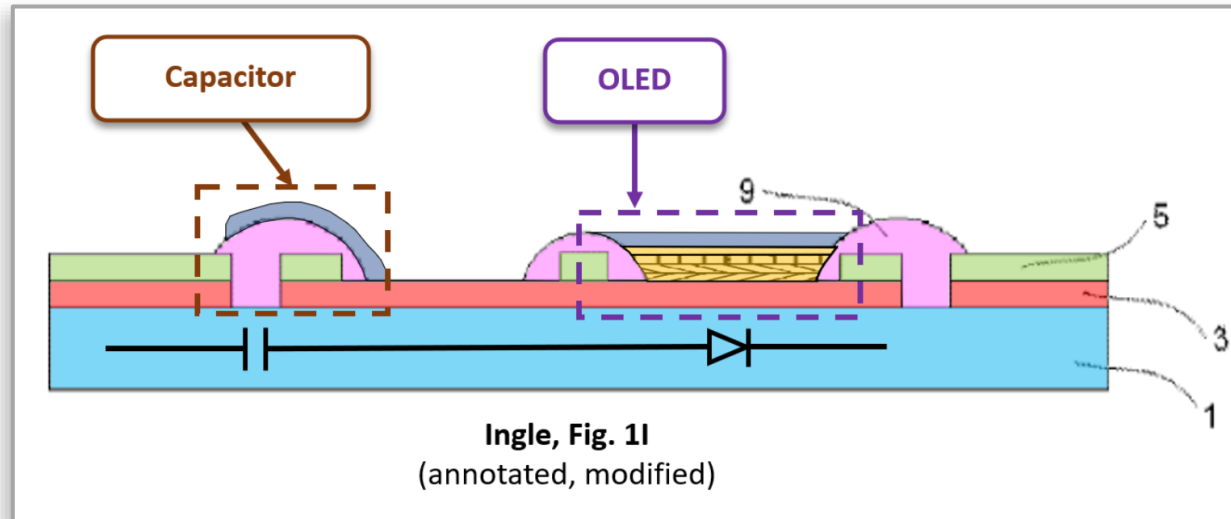
Furthermore, a POSITA would recognize that this approach could allow both cathodes to be formed during the same manufacturing step. *See* Ex.1003, ¶170. A POSITA would have a reasonable expectation of success considering Hasei's disclosures that structured application allows material to be “discharged only onto the portion of the substrate where the conductive pattern is to be formed.” Hasei, ¶¶5, 7; *see also* Ingle, 15:19-24 (applying “material at specific points by means of a printing process [makes it] possible to reduce or eliminate the risk of errors caused by incorrect alignment of the photolithographic system.”). Thus, using Hasei's inkjet printing method would have been nothing more than applying a known method of structured application, *e.g.*, droplet discharge, to improve a similar device, *e.g.*, the OLED and capacitor of Ingle, to obtain predictable results, *e.g.*, a manufacturing process free from photolithography. Ex.1003, ¶¶168-170.

Pet., 25-26

Ground I – Ingle, as Modified by Hasei, Results in a Working Capacitor

Claims 1-2, 8-11, and 16

Pictiva Disregards That There Is Overlap, and That the Degree of Overlap May Be Adjusted to Fine Tune the Capacitor's Capacitance



Reply, 21

Ex.1003, ¶166. A POSITA would understand that the degree to which both the dielectric (pink) and the electrically conductive layer (grey) extend over the first contact region may be adjusted to fine tune the capacitance of the capacitor. See Ex.1003, ¶167-70.

Pet., 38

Dr. Kattamis Explained That Adjusting Capacitance Would Have Been Obvious

167. A POSITA would understand that the degree to which both the dielectric (pink) and the electrically conductive layer (grey) extend over the first contact region may be adjusted to fine-tune the capacitance of the capacitor. It is well understood that larger plates provide greater capacity to store electric charge, and thus, larger plates (with greater area) allow higher capacitance. Here, conductive material deposited on the substrate functions as one plate, while the electrically conductive layer deposited on the dielectric acts as the second plate. The area of the electrically conductive layer (second plate) can readily be controlled due to structured application, as both Ingle and Hasei teach (*see* Section XI.A.1.c), and adjusting the area would adjust the capacitance.

Ex.1003 (Kattamis Decl.), ¶ 167

Changing the Dielectric's Size and Shape to Avoid Short-Circuits Would Have Been Obvious

167. A POSITA would understand that the degree to which both the dielectric (pink) and the electrically conductive layer (grey) extend over the first contact region may be adjusted to fine-tune the capacitance of the capacitor. It is

Ex.1003 (Kattamis Decl.), ¶ 167

9	Q. And I'm correct, am I not, that you
10	cannot extend this gray cathode layer to the point
11	that it extends beyond the pink dielectric layer,
12	correct?
13	ATTORNEY WEIDENFELLER: Objection.
14	THE WITNESS: Sure. It can't contact or
15	run risk of contacting layer 5, the first
16	contact region. And so the dielectric would
17	have to be extended, as I explained.

Ex.2006 (Kattamis Tr.), 100:9-17

A POSITA Would Not Expect Ingle's Dielectric to Be “steeply curved” in a Real-World Implementation

21. Fourth, I understand that Pictiva asserts that Ingle discloses that its dielectric is “steeply curved.” POR at 50. I disagree. A POSITA would not expect Ingle's dielectric to be “steeply curved” in a real-world implementation of Ingle's teachings. Instead, a POSITA would understand that Ingle's figures are simplified representations and would not be representative, or limiting, of what real-world components would look like. Indeed, Ingle explains as such, stating that the “present invention is illustrated below without limiting the generality with reference to the figures.” Ex. 1005, Ingle at 18:21-22. Moreover, a POSITA would likewise understand that the processes for forming the dielectric could be readily adjusted to change how rounded, if at all, the dielectric is.

Ex.1030 (Kattamis Reply Decl.), ¶ 21

The Process for Forming the Dielectric Could be Readily Adjusted to Change How Rounded, if at All

21. Fourth, I understand that Pictiva asserts that Ingle discloses that its dielectric is “steeply curved.” POR at 50. I disagree. A POSITA would not expect Ingle’s dielectric to be “steeply curved” in a real-world implementation of Ingle’s teachings. Instead, a POSITA would understand that Ingle’s figures are simplified representations and would not be representative, or limiting, of what real-world components would look like. Indeed, Ingle explains as such, stating that the “present invention is illustrated below without limiting the generality with reference to the figures.” Ex. 1005, Ingle at 18:21-22. Moreover, a POSITA would likewise understand that the processes for forming the dielectric could be readily adjusted to change how rounded, if at all, the dielectric is.

Ex.1030 (Kattamis Reply Decl.), ¶ 21

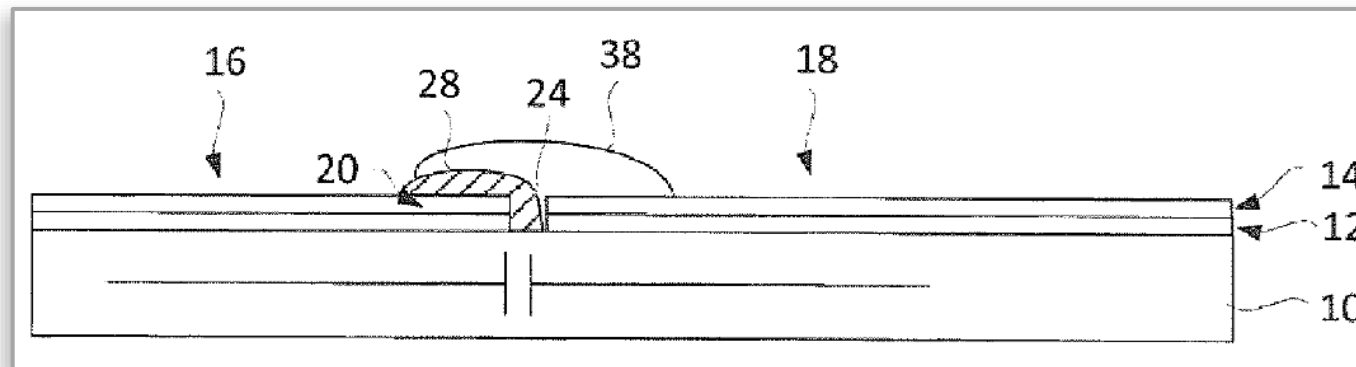
The '492 Patent Has Similar Rounding

4 Q And electrode 38 is shown as following
5 the curvature of the dielectric?
6 MR. WARRICK: Objection. Form.
7 A Yeah, and this is, like I said, not an
8 engineering drawing, but it's showing it as kind
9 of -- yeah, it has a rounded structure on top.
10 Q And you noted that this is not an
11 engineering drawing. Why did you note that?
12 A Well, because it looks like it's hand
13 drawn, not a picture or -- you know, with
14 tolerances or dimensions involved.

Ex.1033 (Pattison Tr.), 74:14

12 Q And so, there would be an irregular
13 distance here between the anode and cathode of the
14 capacitor in Figure 7, right?
15 MR. WARRICK: Objection. Form.
16 A There could be. I mean, I think these
17 figures are meant to convey the concept, and I
18 think you could adjust the processes to make it
19 more or less rounded.
...
2 Q And the '492 patent never identifies an
3 irregular distance between its anode and cathode
4 of the capacitor as being a problem, right?
5 A I don't believe it does, no.

Ex.1033 (Pattison Tr.), 75:12-76:5



'492 Patent, Fig. 7

Pictiva's Attempts to Distort Dr. Kattamis' Testimony

POR. For example, Petitioner maintains that Hasei's "droplet discharging method" was an example of a "conventional process" to form an OLED on the structure disclosed in Ingle despite Petitioner's own expert's admission that he was "personally *not aware of anyone having fabricated such a device in the claimed manner* prior to the '492 Patent." EX2006, 43:25-44:4.¹ And confronted with the

Sur-Reply, 1; *see also id.*, 14, 17

25	Q.	But to be clear, you're personally not
1		aware of anyone having fabricated such a device in
2		the claimed manner prior to the '492 Patent,
3		correct?
4	A.	Correct.

Ex.2006 (Kattamis Tr.), 43:25-44:4

Pictiva's Attempts to Distort Dr. Kattamis' Testimony

POR. For example, Petitioner maintains that Hasei's "droplet discharging method" was an example of a "conventional process" to form an OLED on the structure disclosed in Ingle despite Petitioner's own expert's admission that he was "personally *not aware of anyone having fabricated such a device in the claimed manner* prior to the '492 Patent." EX2006, 43:25-44:4.¹ And confronted with the

Sur-Reply, 1; *see also id.*, 14, 17

18 Q. I believe you testified earlier that as
19 of the 2012 priority date of the '492 Patent, you're
20 not personally aware of anyone fabricating an OLED
21 in that particular manner; is that right?

...

5 A. No. I must have misspoken or not
6 understood. I do not expect the top layer of an
7 OLED to have any subsequent photolithography
8 performed at that time. We would do it through
9 shadow masks.

10 Q. So you are aware of, personally aware
11 of, someone fabricating an OLED device prior to 2012
12 in which the cathode layer is applied in a
13 structured manner as the '492 Patent describes it?

14 A. Yes. Yeah. I mean, this is something
15 I've worked on.

16 Q. Did you identify any such examples in
17 your declaration, Exhibit 1003?

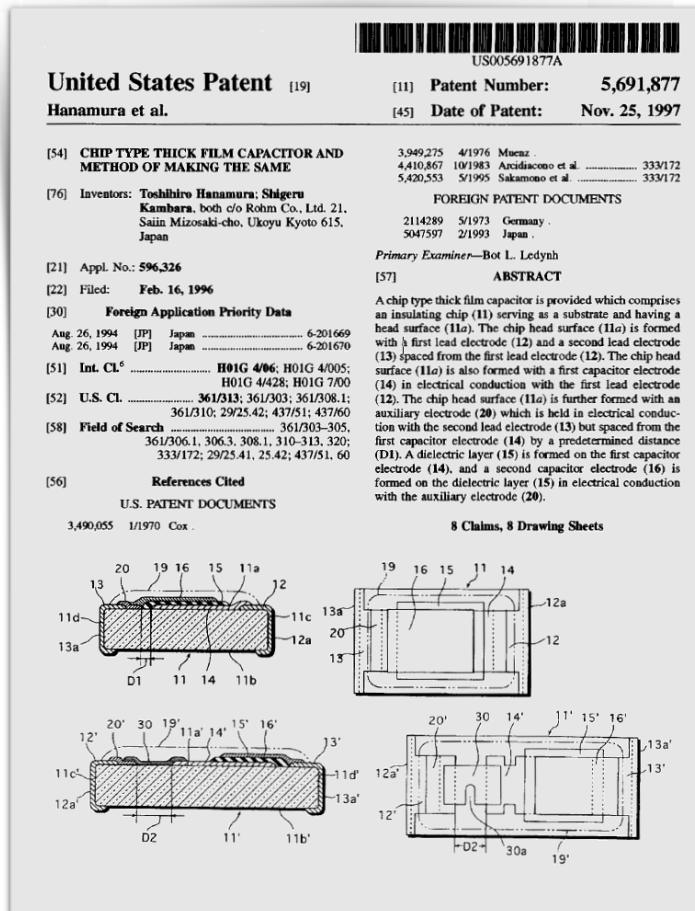
18 A. Where the OLED was -- where the top
19 cathode of the OLED was put in a structured fashion?
20 Yes. Hasei, I think, describes that.

Ex.2006 (Kattamis Tr.), 68:18-69:20

Ground II - Hanamura

Claims 1, 2, 8, and 16

Hanamura



Hanamura

- Undisputedly renders obvious 1[pre]-[a], 1[d]-[e], 16[pre]-[a], 16[d]-[e], and the additional limitations of dependent claims 2 and 8.
- Pictiva argues only that Hanamura does not render obvious 1[b]-[c] and 16[b]-[c], depending primarily on the adoption of its constructions.

Pictiva's Argument That Hanamura "differs dramatically [in size] from the integral capacitors . . . contemplated by the '492 patent" Fails

1. A method for producing a passive electronic component, comprising:
forming a first electrically conductive layer on a substrate,
forming a second electrically conductive layer on the first electrically conductive layer,
forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region,
applying a dielectric in a structured fashion to the second electrically conductive layer in the first contact region and at least partly to the substrate in the first trench such that the dielectric electrically insulates the first contact region from the second contact region, and
applying an electrically conductive electrode layer in a structured fashion to the dielectric above the first contact region and to the second contact region.

2. The method as claimed in claim 1, wherein a first electrode of a capacitor is formed by the first contact region between the dielectric and the substrate and a second electrode of a capacitor is formed by the electrode layer on a side of the dielectric facing away from the first contact region.

8. The method as claimed in claim 1, wherein the dielectric is applied by a printing method.

16. A passive electronic component, comprising:
a first electrically conductive layer on a substrate,
a second electrically conductive layer on the first electrically conductive layer,
a first trench in the first and second electrically conductive layers, wherein the first trench separates a first contact region from a second contact region,
a dielectric, which is applied in a structured fashion on the second electrically conductive layer in the first contact region and at least partly on the substrate in the first trench such that said dielectric electrically insulates the first contact region from the second contact region, and
an electrically conductive electrode layer, which is applied in a structured fashion on the dielectric above the first contact region and at least partly on the second contact region.

'492 Patent, cls. 1, 2, 8, 16

Like the '492 Patent, Hanamura Is Directed to Building a Passive Electronic Component

In various embodiments, a method for producing a passive electronic component and/or a method for producing an optoelectronic assembly are provided which enable the production of a passive electronic component and/or an optoelectronic assembly simply and/or in a cost-effective manner and/or without the use of a photolithographic process.

...

A passive electronic component can be for example a capacitor and/or a resistor or a combination, for example a series circuit and/or a series connection of one, two or more capacitors and/or one, two or more resistors.

'492 Patent, 1:41-46, 2:20-24

This invention relates to a chip type thick film capacitor wherein a capacitor element is formed on an insulating chip substrate. The present invention also relates to a chip type thick film capacitor which incorporates a resistor to work as a composite device. Moreover, the present invention further relates to a method of advantageously making a chip type thick film capacitor.

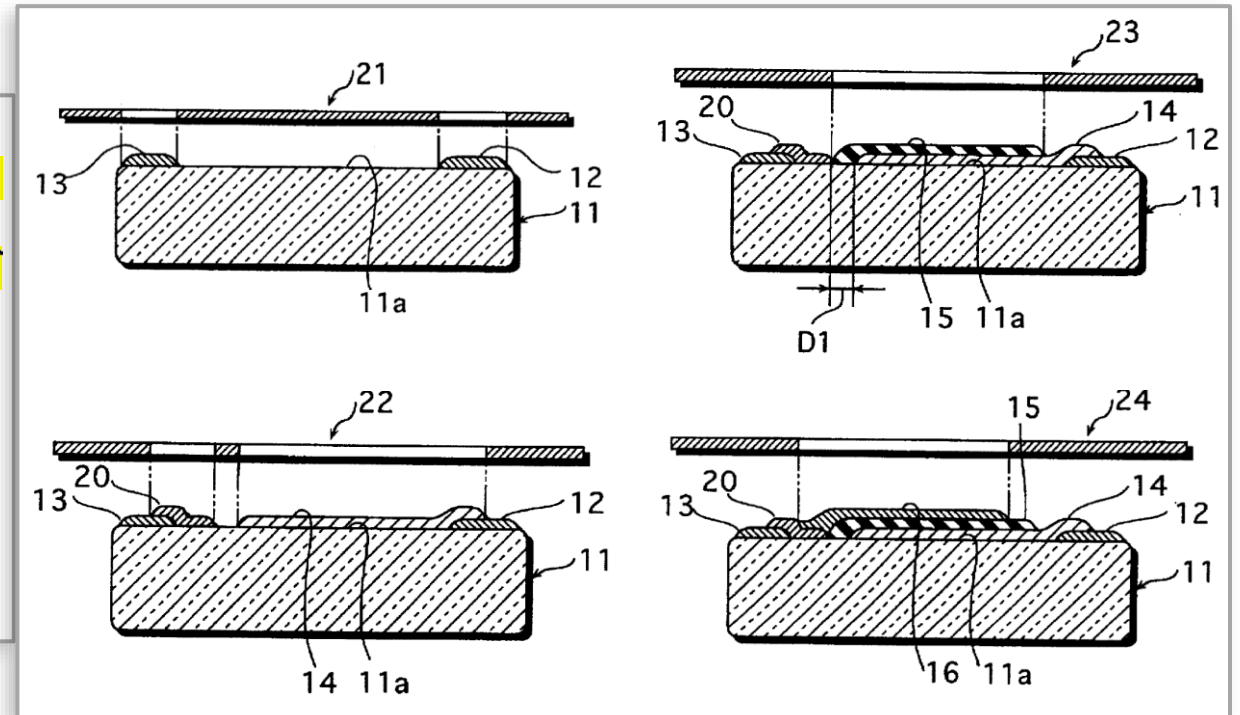
Hanamura, 1:6-112

Like the '492 Patent, Hanamura Deposits Layers in a Structured Fashion

The fact that the dielectric and/or the electrode layer and/or subsequently further layers or materials are “applied in a structured fashion” means, in various embodiments, that the desired structure is already formed during the application of the corresponding layer. The area to be coated is thus coated only in partial regions dependent on the desired structure.

The corresponding materials or layers can be applied in a structured fashion to the substrate for example by printing, for example inkjet printing or screen printing, by blade coating and/or by deposition with the aid of SAMs (self assembling monolayers) and the like.

'492 Patent, 1:66-2:19

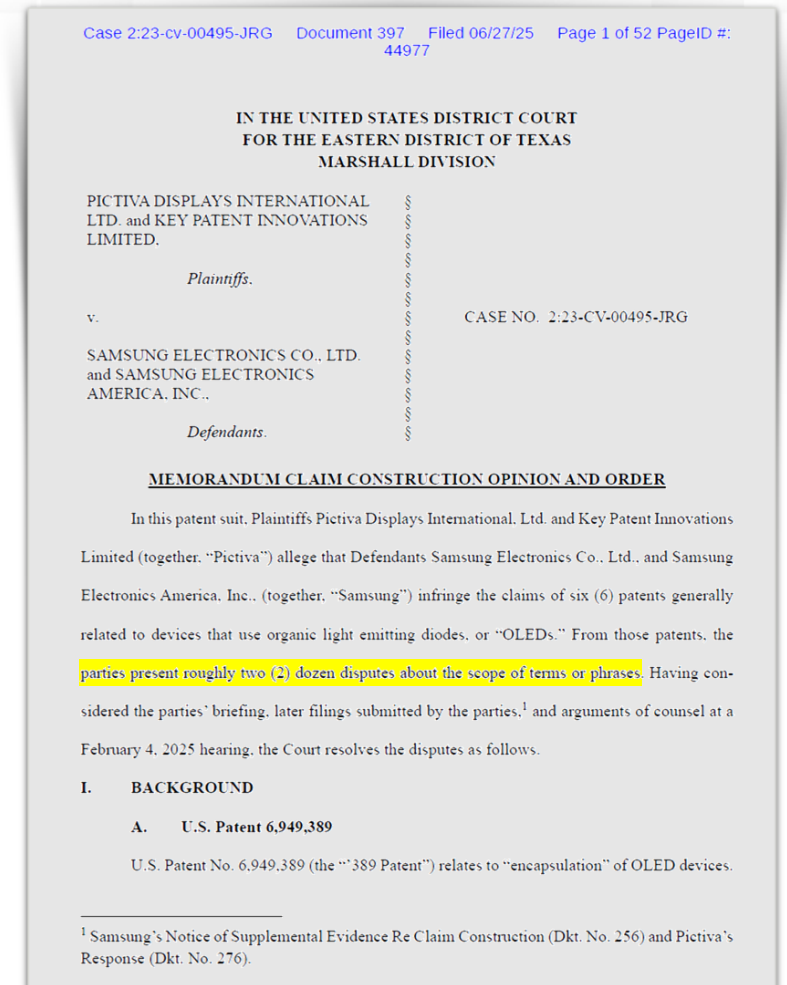


Hanamura, Figs. 2-6

Ground II – Pictiva's Proposed Claim Constructions

Disputed Constructions

- “First Electrically Conductive Layer on a Substrate” / “Second Electrically Conductive Layer on the First Electrically Conductive Layer”
- “First Trench in the First and Second Electrically Conductive Layers”
- “Forming a First Trench”



Ex.2007 (District Court *Markman* Order)

Pictiva Does Not Assert That the '492 Patent Engages in Lexicography

- “First Electrically Conductive Layer **on** a Substrate” / “Second Electrically Conductive Layer **on** the First Electrically Conductive Layer”
- “First Trench **in** the First and Second Electrically Conductive Layers”
- “**Forming** a First Trench”

5	Q	So you don't provide any opinions, in
6		this proceeding, that the applicants for the '492
7		patent have engaged in lexicography, correct?
8	A	Not in this declaration.
9	Q	And not in your other declaration
10		either, right?
11	A	Yeah --

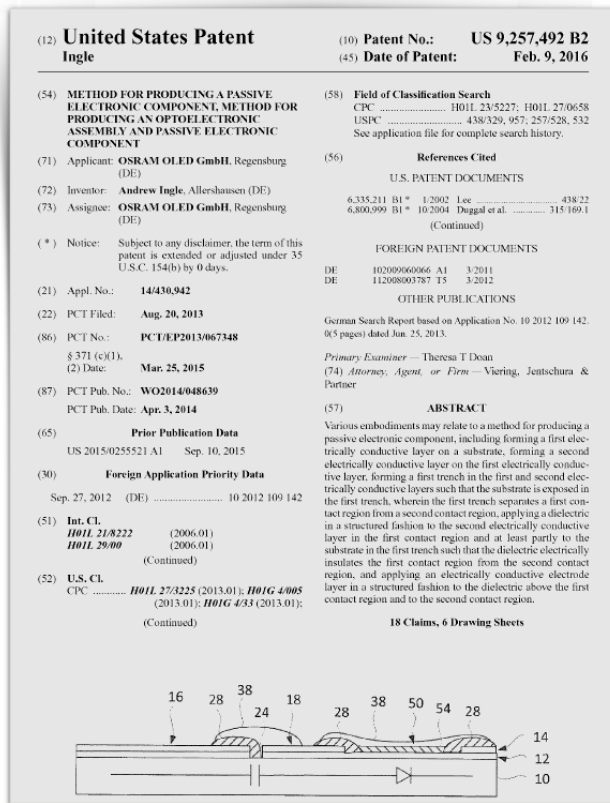
Ex.1033 (Pattison Tr.), 57:5-58:2

Ground II – “First” and “Second Electrically Conductive Layers”

Claims 1, 10, and 16

The Claimed “First” and “Second Electrically Conductive Layers”

- No specialized construction is necessary.



'492 Patent

1. A method for producing a passive electronic component, comprising:
forming a first electrically conductive layer on a substrate,
forming a second electrically conductive layer on the first electrically conductive layer,

10. A method for producing an optoelectronic assembly, comprising:
forming a passive electronic component,
the passive electronic component, comprising:
a first electrically conductive layer on a substrate,
a second electrically conductive layer on the first electrically conductive layer,

16. A passive electronic component, comprising:
a first electrically conductive layer on a substrate,
a second electrically conductive layer on the first electrically conductive layer,

'492 Patent, cls. 1, 10, 16

The Claimed “First” and “Second Electrically Conductive Layers”

- Pictiva seeks to significantly narrow its own construction to exclude (1) **materials not formed on the substrate/first electrically conductive layer**, and (2) **portions of a layer that are non-conductive**.

The Board should construe “first electrically conductive layer” according to its plain and ordinary meaning as “electrically conductive material formed on a substrate” and “second electrically conductive layer” according to its plain and ordinary meaning as “electrically conductive material formed on the first conductive layer.” The Board should interpret these terms to include only the electrically conductive material, and not any areas lacking such material. Nor should it interpret “first electrically conductive layer” to include materials not formed on the substrate or “second electrically conductive layer” to include materials not formed on the first electrically conductive layer.

POR, 16

A “Layer” Is Not Defined by What It Is “On”

1. A method for producing a passive electronic component, comprising:
forming a first electrically conductive layer on a substrate,
forming a second electrically conductive layer on the first electrically conductive layer,

10. A method for producing an optoelectronic assembly, comprising:
forming a passive electronic component,
the passive electronic component, comprising:
a first electrically conductive layer on a substrate,
a second electrically conductive layer on the first electrically conductive layer,

16. A passive electronic component, comprising:
a first electrically conductive layer on a substrate,
a second electrically conductive layer on the first electrically conductive layer,

'492 Patent, cls. 1, 10, 16

2 Q And claim 16 further requires, in the
3 next limitation, a second electrically conductive
4 layer on the first electrically conductive layer,
5 right?

6 A Yes.

7 Q Would you agree with me that in order
8 to determine if something meets this limitation,
9 you, first, have to identify a first electrically
10 conductive layer, then you have to identify a
11 second electrically conductive layer, and,
12 finally, you have to determine if what you've
13 identified as the second electrically conductive
14 layer is on what you've identified as the first
15 electrically conductive layer?

16 MR. WARRICK: Objection. Form.

17 A Yeah. That would be how you would look
18 at it.

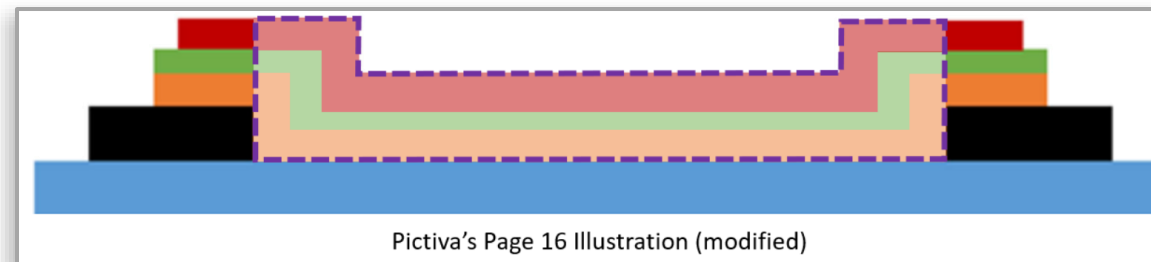
Ex.1033 (Pattison Tr.), 96:8-97:18

Pictiva Arbitrarily Divides Single Layers Based on Underlying Materials

Put another way, in the hypothetical configuration below, assume that the black, orange, green, and red regions each contain electrically conductive materials, and the blue support is a substrate. In that context, the first and second electrically conductive layers may be, for example, respectively (i) the orange and green layers, (ii) the orange and red layers, or (iii) the green and red layers. But if the black layer is mapped to the first electrically conductive layer, at least the central portion of the orange, green, or red layer is not a second electrically conductive layer because it is not on the black first electrically conductive layer.



POR, 16



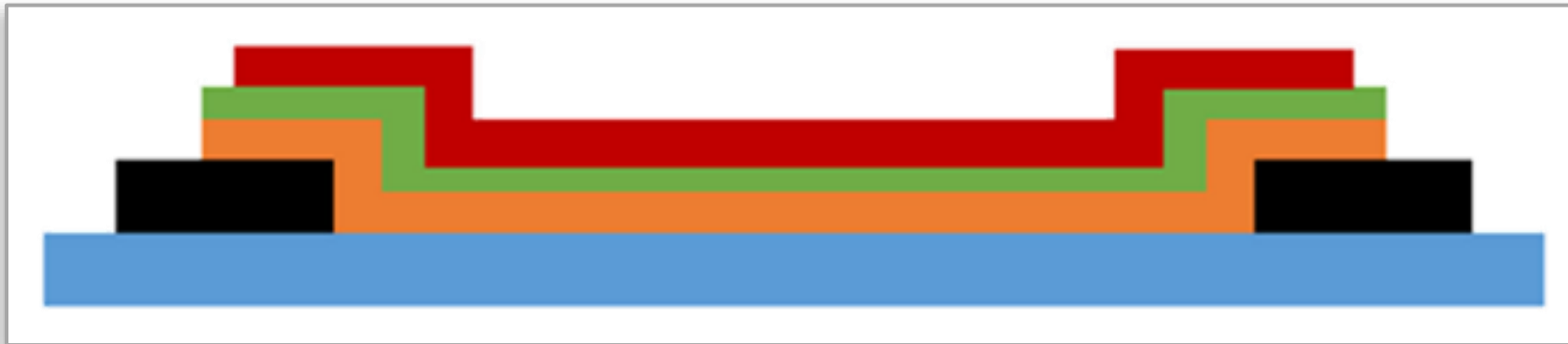
Pictiva's Page 16 Illustration (modified)

Reply, 3

Pictiva Arbitrarily Divides Single Layers Based on Underlying Materials

10 Q So am I understanding correctly, is it
11 the different materials that, essentially,
12 determines if you kind of move from one layer to
13 another?
14 MR. WARRICK: Objection. Form.
15 A That's the context in the patent.

Ex.1033 (Pattison Tr.), 100:10-15



POR, 16

Precedent Holds That Claims Should Not Be Limited to Disclosed Embodiments



Even when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using “words or expressions of manifest exclusion or restriction.”

Liebel-Flarsheim Co., v. Medrad, Inc., 358 F.3d 898, 906 (Fed. Cir. 2004)



Figure 5 A ... shows an embodiment where there does not appear to be any air gap between layers. Nowhere does the written description, however, limit the meaning of ‘on’ to that embodiment.

Hisense USA Corp. v. Brightplus Ventures LLC, IPR2023-01410, Paper 7 at 11-12 (Apr. 2, 2024)

“It Goes Without Saying That Other Embodiments Can Be Used”

way whatsoever. It goes without saying that other embodiments can be used and structural or logical changes can be made, without departing from the scope of protection of the present invention. It goes without saying that the features of

...

FIG. 3 shows the substrate 10, the first electrically conductive layer 12 and one embodiment of a second electrically conductive layer 14, which is formed on the first electrically conductive layer 12. The second electrically conductive layer

...

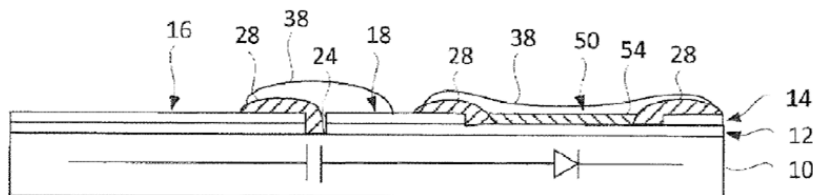
While the disclosed embodiments have been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the disclosed embodiments as defined by the appended claims. The scope of the disclosed embodiments is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

'492 Patent, 8:8-11, 11:5-8, 20:16-25

Pictiva's Hypothetical OLED/Capacitor Argument Is Irrelevant

This is for good reason. For example, where an OLED is formed together with a capacitor as in claim 11, portions of only the second electrically conductive layer are etched away in the component region as shown in Figure 16 below.

Fig. 16



The '492 Patent teaches that the material for the first electrically conductive layer “can withstand an etching process ... for removing a second electrically conductive material.” *Id.* at 10:10-14; *see also id.* at 14:19-24 (describing etching process).

As Dr. Pattison explains (EX2005, ¶ 29), a POSTIA would understand that this is to ensure that some electrically conductive material (i.e., the first electrically conductive layer) remains to serve as a bottom electrode for the OLED. *See e.g.*,

POR, 19-20

1. A method for producing a passive electronic component, comprising:

16. A passive electronic component, comprising:

'492 Patent, cls. 1, 16

that layer atop the first. First, independent claims 1 and 16 do not even require an OLED; accordingly, how the layers may hypothetically be structured in conjunction with an OLED should not bear on how the claims are read generally. Second, even if a hypothetical OLED/capacitor structure required that the second electrically conductive layer be formed on the first electrically conductive layer in one region, that does not mean that the second electrically conductive layer needs to be formed on the first electrically conductive layer at all locations, i.e., that it be entirely atop the first electrically conductive layer, as Pictiva and Dr. Pattison suggest.

Ex.1030 (Kattamis Reply Decl.), ¶ 13

Pictiva's Overly Narrow Construction Is Contrary to Established Federal Circuit Law

The first electrically conductive layer **includes** a first electrically conductive material and the second electrically conductive layer **includes** a second electrically conductive material. The first and/or the second electrically conductive

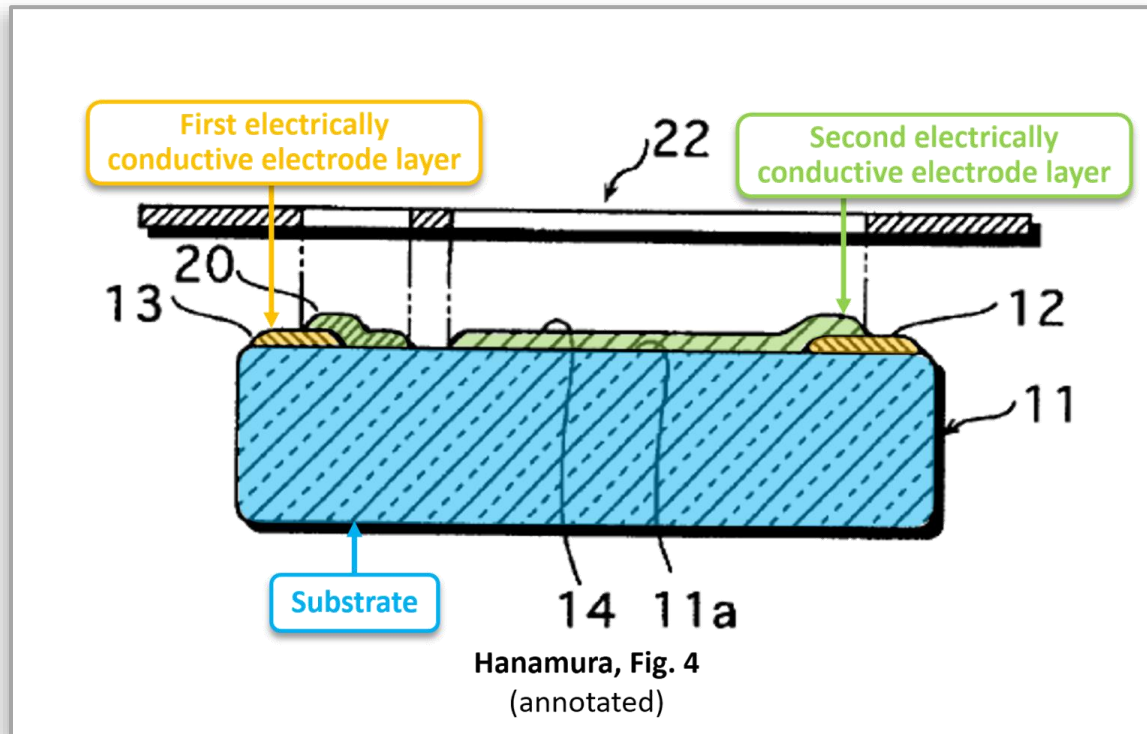
'492 Patent, 2:36-41



As a patent law term of art, “includes” means “comprising.” Neither includes, nor comprising, forecloses additional elements that need not satisfy the stated claim limitations.

Sandisk Corp. v. Memorex Prods., Inc., 415 F.3d 1278, 1284 (Fed. Cir. 2005) (citation omitted)

Hanamura Renders Obvious a “Second Electrically Conductive Layer” (Limitations 1[b], 16[b])



Reply, 25

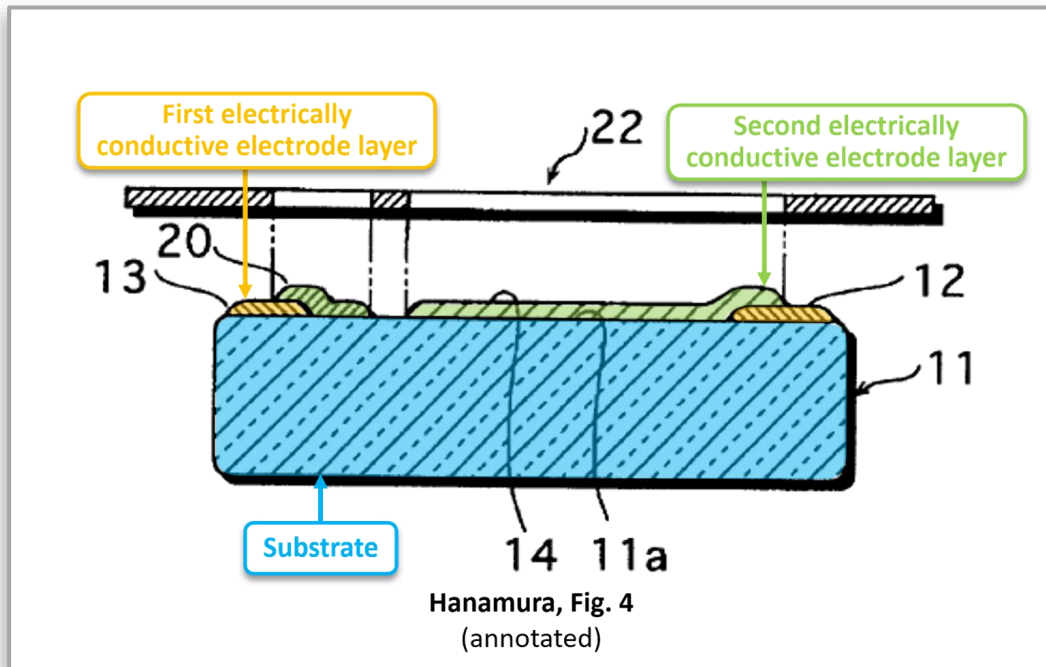
On the present record, we determine that there is a reasonable likelihood that lead electrodes 12 and 13 teach a first conductive layer and that first capacitor electrode 14 in conjunction with auxiliary electrode 20 teaches the claimed second conductive layer.

Institution Decision, 19

at 20:29-31 (claim 1), 22:28-30 (claim 16). Electrodes 20 and 14 as described and depicted in Hanamura do not comprise such a layer. As shown in Petitioner’s own annotated versions of Hanamura’s figures, the alleged “first electrically conductive layer” (electrodes 12 and 13, colored yellow below) and the alleged “second electrically conductive layer” (electrodes 14 and 20, colored green below) are in fact four adjacent and slightly overlapping electrodes applied selectively on the same substrate. See EX2001, ¶ 92 (“a POSITA would not have viewed electrode 20 as ‘on’ the electrode 13 or electrode 14 as ‘on’ the electrode 12”).

POR, 53-54

That Hanamura Calls Layers 11-13 and 20 “electrodes” Does Not Mean They Are Not the Claimed *Layers*



Reply, 25



[I]nventor’s lexicography governs.

Phillips v. AWH Corp., 415 F.3d 1303, 1316 (Fed. Cir. 2005)

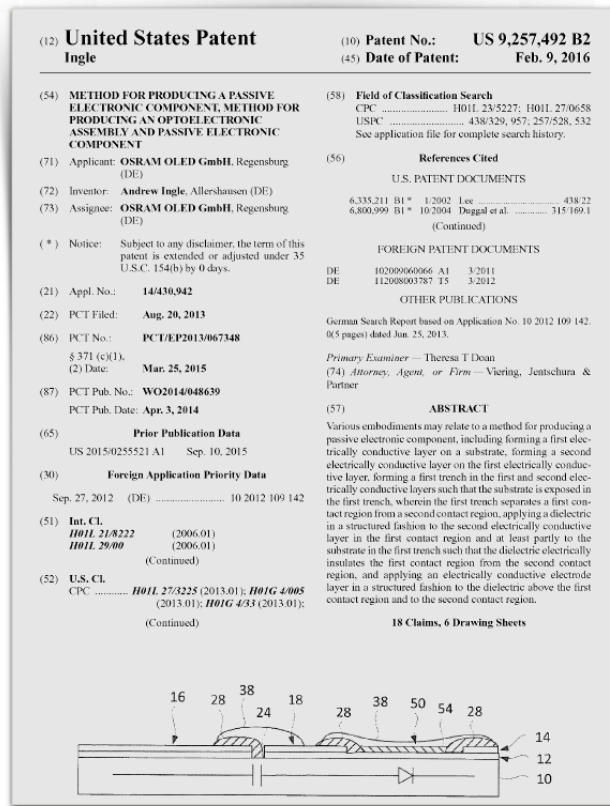
manufacturing techniques. Layers of the semiconductor device can be deposited as continuous layers or as patterns defined by a mask or by some form of printing.

Ex.1033 (Pattison Decl.), ¶ 37

Ground II – “First Trench in the First and Second Electrically Conductive Layers”

Claims 1 and 16

- No specialized construction is necessary.



'492 Patent

1. A method for producing a passive electronic component, comprising:

- forming a first electrically conductive layer on a substrate,
- forming a second electrically conductive layer on the first electrically conductive layer,
- forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region,

16. A passive electronic component, comprising:
a first electrically conductive layer on a substrate,
a second electrically conductive layer on the first electrically conductive layer,
a first trench in the first and second electrically conductive layers, wherein the first trench separates a first contact region from a second contact region,

'492 Patent, cls. 1, 16

“First Trench in the First and Second Electrically Conductive Layers”

- Pictiva’s construction relies on an overly narrow construction of “in” requiring the trench to be **adjacent to the edges of the electrically conductive layers**.

The Board should construe this term according to its plain and ordinary meaning as “a trench defined by (and thus adjacent to) edges of the electrically conductive material of both the first and second electrically conductive layers.” This interpretation follows naturally from the plain language of the claims, which require the first trench to be ***in*** the first and second electrically conductive layers. *See* EX2005, ¶¶ 24-25 (confirming a POSITA’s understanding of this term). This construction is also consistent with the first trench depicted in Figure 4 and every other embodiment of the ’492 Patent.

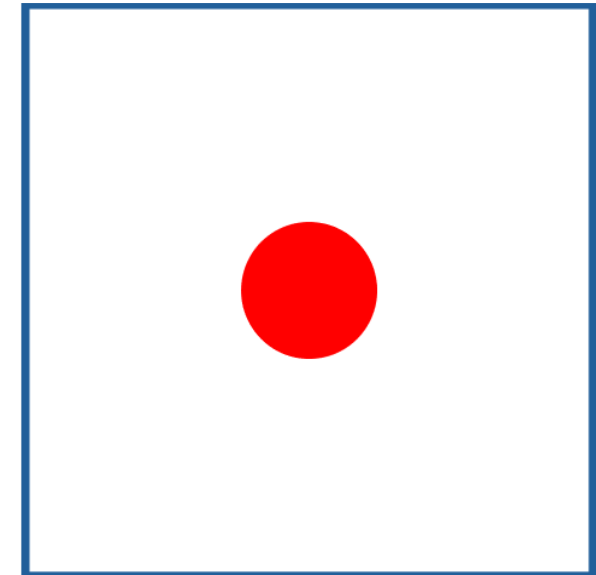
POR, 21

“In” Is a Nontechnical Term With a Commonly Understood Meaning (the Red Circle Is “in” the Blue Square)

in \ˈin, ən, ˈn\ *prep* [ME, fr. OE; akin to OHG *in* in, L. *in*, Gk *en*] (bef. 12c) **1 a** — used as a function word to indicate inclusion, location, or position within limits <~ the lake> <wounded ~ the leg> <~ the summer> **b** : INTO 1 <went ~ the house> **2** — used as a function word to indicate means, medium, or instrumentality <written ~ pencil> <bound ~ leather> **3 a** — used as a function word to indicate limitation, qualification, or circumstance <alike ~ some respects> <left ~ a hurry> **b** : INTO 2a <broke ~ pieces> **4** — used as a function word to indicate purpose <said ~ reply> **5** — used as a function word to indicate the larger member of a ratio <one ~ six is eligible>

Ex.1031 (Webster’s 11th ed. 2007), 627; *see also*

Ex.1032 (Webster’s 11th ed. 2012), 627 (same)



“In” Was Not Redefined or Disavowed



The words of a claim are generally given their ordinary and customary meaning.... There are only two exceptions to this general rule: 1) when a patentee sets out a definition ... or 2) when the patentee disavows the full scope of a claim term....

Thorner v. Sony Comput. Entm't Am. LLC, 669 F.3d 1362, 1365 (Fed. Cir. 2012)(citation omitted)

5	Q	So you don't provide any opinions, in
6		this proceeding, that the applicants for the '492
7		patent have engaged in lexicography, correct?
8	A	Not in this declaration.
9	Q	And not in your other declaration
10		either, right?
11	A	Yeah --

Ex.1033 (Pattison Tr.), 57:5-58:2

Pictiva Improperly Limits the Claims to Preferred Embodiments and Reads in Dependent Claim Limitations

The Board should construe this term according to its plain and ordinary meaning as “a trench defined by (and thus adjacent to) edges of the electrically conductive material of both the first and second electrically conductive layers.” This . . . construction is also consistent with the first trench depicted in Figure 4 and every other embodiment of the '492 Patent.

. . . See Section IV.A, *supra*. For example, in the context of describing the subsequent step of applying a dielectric in the first trench, as required by each independent claim, see '492 Patent at 20:36-40 (claim 1) (“applying a dielectric . . . at least partly 12:13-18, Fig. 6. That encapsulation step—which is expressly recited in dependent claim 9 (*id.* at 21:8-11)—is only possible if those edges or side surfaces are adjacent to (and in fact define the sides of) the first trench. Further, the encapsulation step

POR, 21-22



This court has repeatedly “cautioned against limiting the claimed invention to preferred embodiments or specific examples in the specification.”

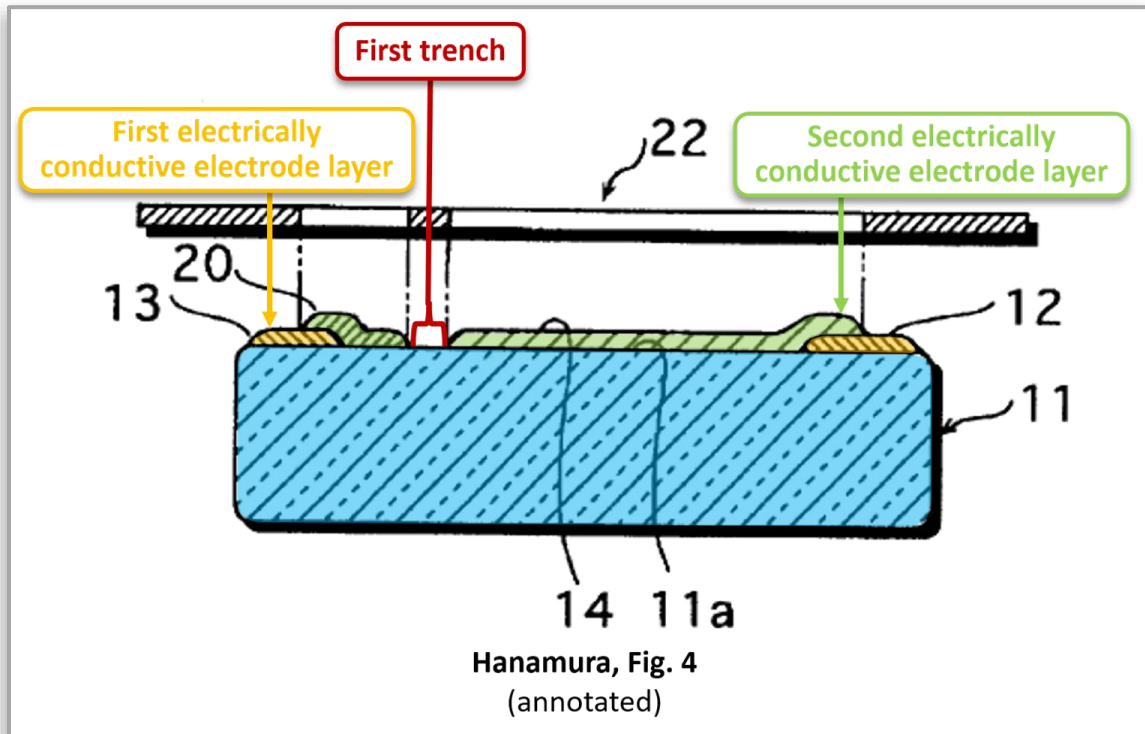
Williamson v. Citrix Online LLC, 792 F.3d 1339, 1346-47 (Fed. Cir. 2015)



An independent claim usually covers a scope broader than the preferred embodiment, especially if the dependent claims recite the precise scope of the preferred embodiment.

RF Del., Inc. v. Pac. Keystone Techs., Inc., 326 F.3d 1255, 1264 (Fed. Cir. 2003) (footnote omitted)

Hanamura Renders Obvious “a First Trench in the First and Second Electrically Conductive Layers” (Limitations 1[c], 16[c])



On the present record, we determine that there is a reasonable likelihood that Hanamura teaches a trench in the first and second electrically conductive layers.

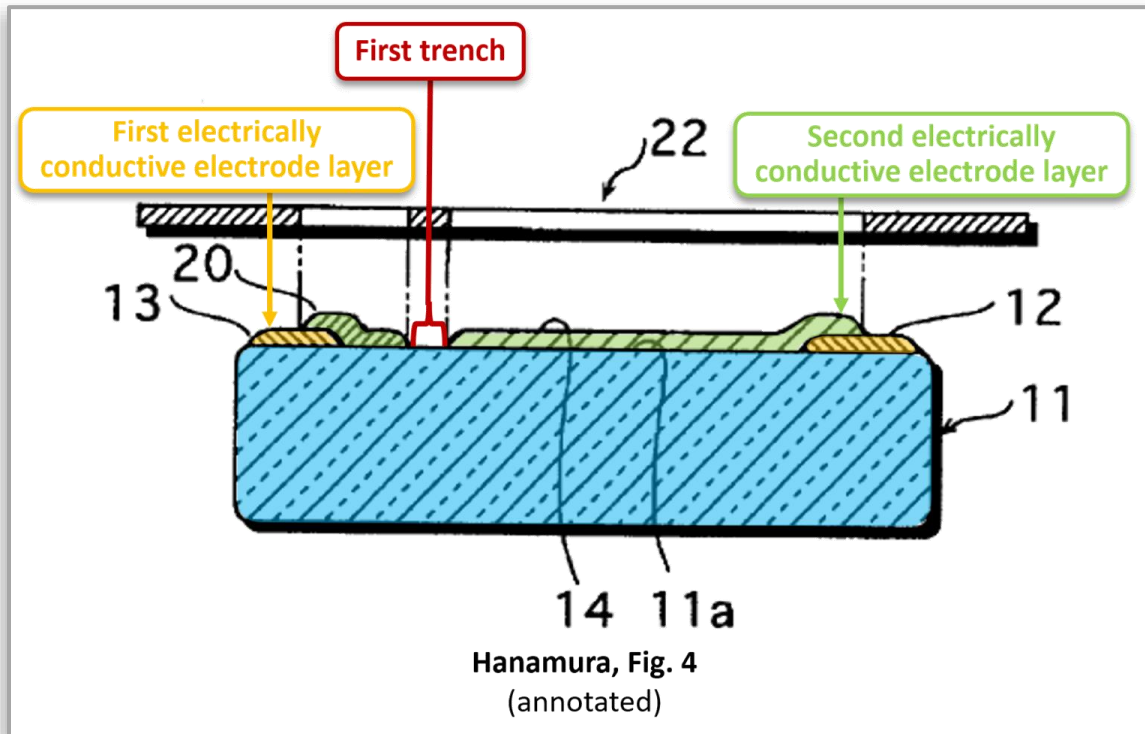
Institution Decision, 20

I disagree. If Hanamura's *first trench* was not in the *first electrically conductive layer*, electrodes 12 and 13 would touch and therefore short-circuit, causing Hanamura's capacitor to become inoperable.

Ex.1030 (Kattamis Reply Decl.), ¶ 25

Reply, 27

Hanamura Renders Obvious “a First Trench in the First and Second Electrically Conductive Layers” (Limitations 1[c], 16[c])

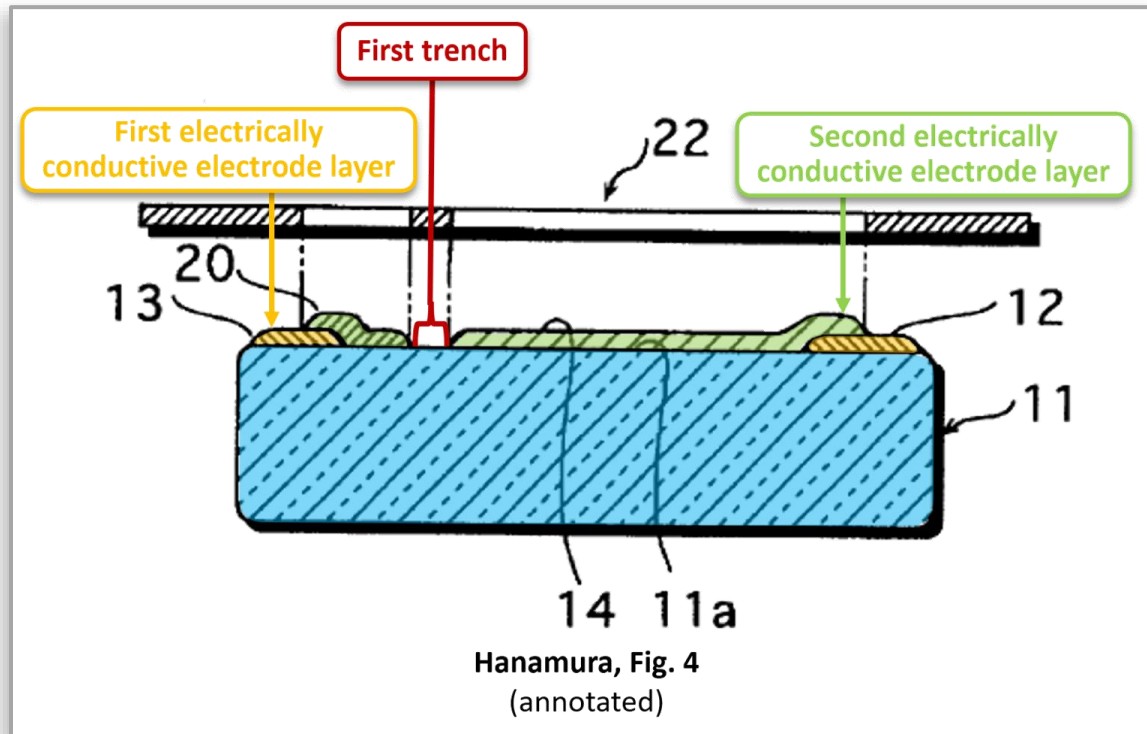


Reply, 27

10 Q And using that screen-printing process,
11 Hanamura makes sure that there is a defined
12 distance between those electrodes, right?
13 MR. WARRICK: Objection. Form.
14 A A defined distance between -- yes,
15 between -- yeah, between the layers -- the layer
16 that they're putting down.
...
16 A D1 is the spacing between the, I guess,
17 call it the auxillary electrode and the other
18 electrode, 14.
19 Q And what is the purpose of D1?
20 A To make sure the electrodes don't
21 short.
...
2 Q So that's why, in Figure 3, to keep the
3 second lead electrode 13 and the first lead
4 electrode 12 from short-circuiting, they're
5 selectively deposited with a space between them,
6 right?
7 A In Figure 3? Yeah.

Ex.1033 (Pattison Tr.), 85:10-16, 94:16-21, 95:2-7

Hanamura Renders Obvious “a First Trench in the First and Second Electrically Conductive Layers” (Limitations 1[c], 16[c])



31. In my opinion, a POSITA would understand the importance of the claimed “first trench” being “in” both of these electrically conductive layers because the functionality of certain components disclosed in the ’492 Patent (e.g., a capacitor) requires the trench to expose the substrate and separate the first and second contact regions, which lie on either side of the first trench. *See, e.g.,* ’492 Ex.2005 (Pattison Suppl. Decl.), ¶ 31

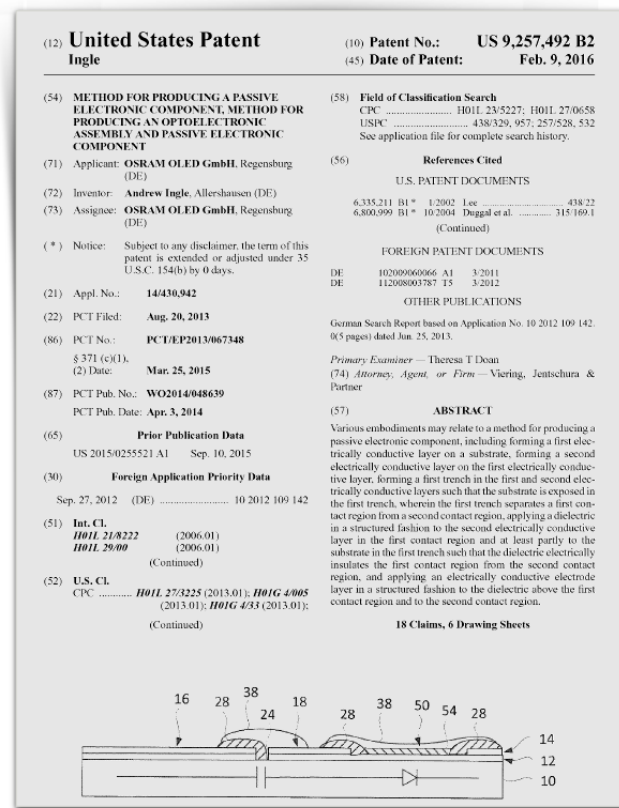
Reply, 27

Ground II – Forming a First Trench

Claim 1

“Forming a First Trench”

- No specialized construction is necessary.



’492 Patent

1. A method for producing a passive electronic component, comprising:
forming a first electrically conductive layer on a substrate,
forming a second electrically conductive layer on the first electrically conductive layer,
forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region,

’492 Patent, cl. 1

“Forming a First Trench”

- Pictiva seeks to significantly narrow its own construction by requiring **removal**.

As it did pre-institution, Pictiva proposes construing the term “forming a first trench,” ’492 Patent, 20:32-35 (claim 1), according to its plain and ordinary meaning, which requires the creation of something that did not previously exist.

...

The plain and ordinary meaning of the claim term **requires the creation of a trench by removing certain portions of the previously formed first and second electrically conductive layers.** See ’492 Patent at 20:27-35 (claim 1) (reciting

POR, 24

The Claim Does Not Use “Removing”; It Merely Requires “Forming” the “First Trench”

1. A method for producing a passive electronic component, comprising:
forming a first electrically conductive layer on a substrate,
forming a second electrically conductive layer on the first electrically conductive layer,
forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region,

'492 Patent, cl. 1

2^{form} *v* (13c) 1 **a** : to give a particular shape to : shape or mold into a certain state or after a particular model <~ the dough into a ball> <a state ~ed along republican lines> **b** : to arrange themselves in <the dancers ~ed a line> **c** : to model by instruction and discipline <a mind ~ed by classical education> 2 : to give form or shape to : FASHION, CONSTRUCT 3 : to serve to make up or constitute : be an essential or basic element of 4 : DEVELOP, ACQUIRE <~ a habit> 5 : to arrange in order : DRAW UP 6 **a** : to assume an inflection so as to produce (as a tense) <~s the past in -ed> **b** : to combine to make (a compound word) ~ *vi* 1 : to become formed or shaped 2 : to take form : come into existence : ARISE 3 : to take on a definite form, shape, or arrangement — **form·abil·i·ty** \,fôr-mə-'bi-lə-tē/ *n* — **formable** \'fôr-mə-bəl/ *adj* — **form on** : to take up a formation next to

Ex.1031 (Webster's 11th ed. 2007), 492; *see also*

Ex.1032 (Webster's 11th ed. 2012), 492 (same)

Claim 1 Does Not Require a Particular Order



[A]lthough a method claim necessarily recites the steps of the method in a particular order, as a general rule the claim is not limited to performance of the steps in the order recited, unless the claim explicitly or implicitly requires a specific order.

Baldwin Graphic Sys., Inc. v. Siebert, Inc., 561 F.3d 1351, 1357 (Fed. Cir. 2009)
(emphasis added)

Claim 1 Does Not Explicitly Require a Specific Order (left), Despite the Applicant Knowing How to Draft Claims Containing Explicit Language (right)

1. A method for producing a passive electronic component, comprising:
forming a first electrically conductive layer on a substrate,
forming a second electrically conductive layer on the first electrically conductive layer,
forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region,

'492 Patent, cl. 1

3. The method as claimed in claim 1, wherein, before the dielectric is applied, a second trench and at least one third

9. The method as claimed in claim 1, wherein the dielectric firstly is applied in a structured fashion to the second electrically conductive layer in such a way that it adjoins the first trench, and wherein then the dielectric is heated in such a way

11. The method as claimed in claim 10, wherein before the optically functional layer is applied, the second electrically

12. The method as claimed in claim 11, wherein after the structured application of the dielectric and before the removal of the second electrically conductive layer

'492 Patent, cls. 3, 9, 11, 12

Claim 1 Does Not Implicitly Require a Particular Order



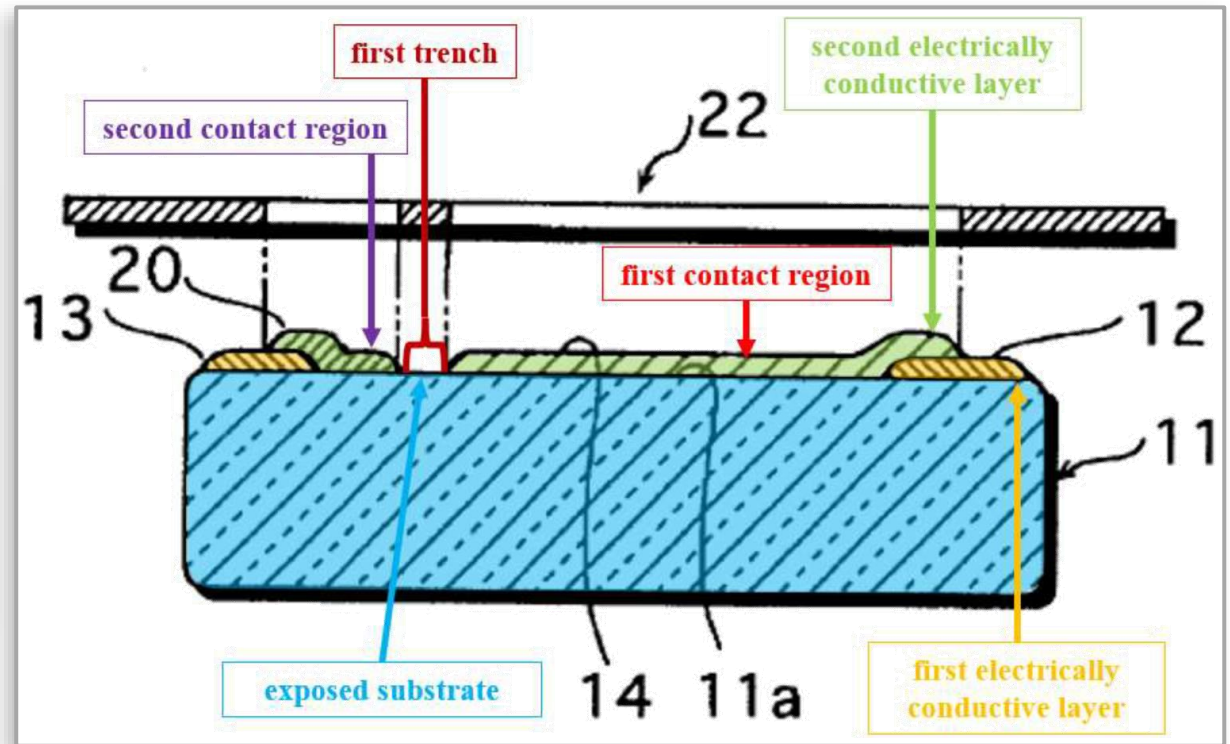
[I]f the steps of a method claim . . . do not otherwise recite an order. . . . [W]e look to the claim language to determine if, as a matter of logic or grammar, they must be performed in the order written. . . . If not, we next look to the rest of the specification to determine whether *it* “directly or implicitly requires such a narrow construction.”

Altiris, Inc. v. Symantec Corp., 318 F.3d 1363, 1369-70 (Fed. Cir. 2003)
(citations omitted)

Claim 1 Does Not Logically Require a Specific Order

1. A method for producing a passive electronic component, comprising:
forming a first electrically conductive layer on a substrate,
forming a second electrically conductive layer on the first electrically conductive layer,
forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region,

'492 Patent, cl. 1



Hanamura, Fig. 4

Claim 1 Does Not Grammatically Require a Specific Order

1. A method for producing a passive electronic component, comprising:
forming a first electrically conductive layer on a substrate,
forming a second electrically conductive layer on the first electrically conductive layer,
forming a first trench in the first and second electrically conductive layers such that the substrate is exposed in the first trench, wherein the first trench separates a first contact region from a second contact region,

'492 Patent, cl. 1

3. The method as claimed in claim 1, wherein, before the dielectric is applied, a second trench and at least one third

9. The method as claimed in claim 1, wherein the dielectric firstly is applied in a structured fashion to the second electrically conductive layer in such a way that it adjoins the first trench, and wherein then the dielectric is heated in such a way

11. The method as claimed in claim 10, wherein before the optically functional layer is applied, the second electrically

12. The method as claimed in claim 11, wherein after the structured application of the dielectric and before the removal of the second electrically conductive layer

'492 Patent, cls. 3, 9, 11, 12

The Claimed Invention Should Not Be Limited to Preferred Embodiments or Specific Examples



This court has repeatedly “cautioned against limiting the claimed invention to preferred embodiments or specific examples in the specification.”

Williamson v. Citrix Online LLC, 792 F.3d 1339, 1346-47 (Fed. Cir. 2015)

The Specification Is Clear That It Is Not Limited to Its Examples

way whatsoever. It goes without saying that other embodiments can be used and structural or logical changes can be made, without departing from the scope of protection of the present invention. It goes without saying that the features of

...

(PVD) or the like. The second electrically conductive layer 14 can be applied to the first electrically conductive layer 12 for example in a planar fashion, that is to say without structure.

...

physical vapor deposition (PVD) or the like. The first electrically conductive layer 12 can be applied to the substrate 10 for example in a planar fashion, that is to say without structure.

'492 Patent, 8:8-11, 11:2-4, 11:24-26

The Specification Is Clear That It Is Not Limited to Its Examples

In various embodiments, at least one of the trenches is formed by laser ablation. This can contribute to the simple and cost-effective production of the passive electronic component. By way of example, an etching process for etching the trench can be dispensed with.

...

conductive layers 12, 14. The first trench can be formed by laser ablation, for example. The material of the substrate 10 is

'492 Patent, 4:5-9, 11:27-46

Case Law Holds That Dependent Claim Limitations Cannot Be Read Into Independent Claims

7. The method as claimed in claim 3, wherein at least one of the trenches is formed by laser ablation.

'492 Patent, cl. 7



It is settled law that when a patent claim does not contain a certain limitation and another claim does, that limitation cannot be read into the former claim in determining either validity or infringement.

SRI Intern v. Matsushita Elec. Corp. of Am., 775 F.2d 1107, 1122 (Fed. Cir. 1985)

Pictiva's Caselaw Is Readily Distinguishable



“11. The method of deinking waste paper . . . comprising . . . then dewatering the slurry so as to separate the ink particles from the fibers.”

In re Altmann, 264 F.2d 894, 894 (C.C.P.A. 1958)



The sequence of steps in the claim defines an insulated gate . . . used as a mask when the ion implementation barriers are established.

...

During prosecution, the patent applicant limited his claim to the sequence of steps enumerated.

Loral Fairchild Corp. v. Sony Corp., 181 F.3d 1313, 1317-18, 1321 (Fed. Cir. 1999) (citations omitted)



Because the acidic conditions and the ferrous ion must be present before the hydrogen peroxide can undergo the Fenton-like reaction, step (d) must come after both steps (b) and (c).

Mantech Env't. Corp. v. Hudson Env't. Servs., Inc., 152 F.3d 1368, 1375-76 (Fed. Cir. 1998)

Pictiva's Caselaw Is Readily Distinguishable



[T]he antecedent basis for the substantially rigid portion in the inserting and advancing the ICD step (step 1.f) is the substantially rigid portion in the inserting a substantially rigid portion and advancing the flexible tip portion steps (steps 1.d and 1.e). Thus, the logic of claim 1 demonstrates that the inserting and advancing the ICD step follows the advancing the flexible tip portion step.

Medtronic, Inc. v. Teleflex Life Scis. Ltd., 2024 WL 1208642, at *3 (Fed. Cir. Mar. 21, 2024)



[T]he separate sub-step for establishing a connection would become “superfluous” if we concluded that a connection did not have to be established (completed) before transmission. That is because, under such construction of the claim, establishing a connection is necessarily encompassed in transmitting a command.

Mformation Techs., Inc. v. Rsch. in Motion Ltd., 764 F.3d 1392, 1400 (Fed. Cir. 2014)



The claim clearly states that the “processing” is done to the “electronic advertisement,” not the inputted information. It follows that the creation of the ad must happen before the processing begins.

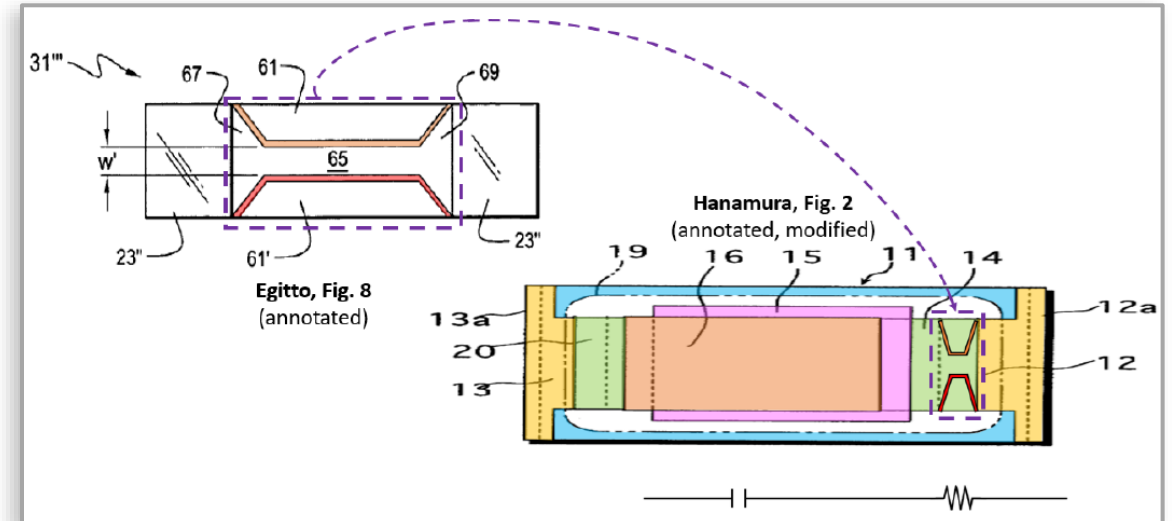
Function Media, L.L.C. v. Google, Inc., 708 F.3d 1310, 1320 (Fed. Cir. 2013)

Ground III – Hanamura in View of Egitto

Claims 3, 5, and 6

Modifying Hanamura to Include Egitto's Resistor Would Have Been Obvious

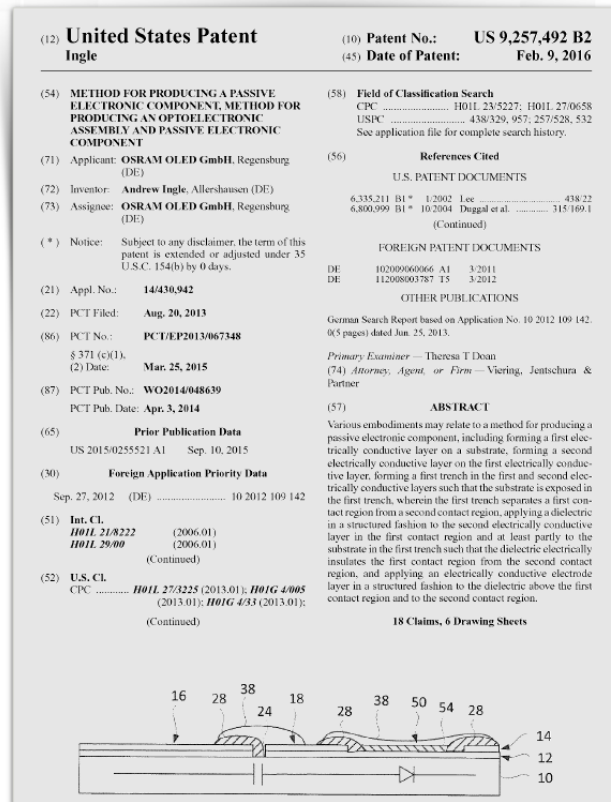
- Pictiva does not dispute that:
 - including a resistor in Hanamura would have been obvious;
 - Egitto discloses materially the same resistor design claimed in the '492 patent; or
 - Egitto's resistor in Hanamura would function.



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- Pictiva's only argument is that "neither the Petition nor Dr. Kattamis' declaration provide any specific motivation to combine the teachings of Hanamura with the specific 'representative pattern[]' described in Egitto." POR, 64.

Pictiva Does Not Dispute that Hanamura in View of Egitto Renders Obvious the Additional Limitations of Claim 6



'492 Patent

3. The method as claimed in claim 1, wherein, before the dielectric is applied, a second trench and at least one third trench are formed, which delimit a resistance region, which comprises a part of the first and second electrically conductive layers and which has a taper in a direction parallel to the electrically conductive layers and which leads into the first contact region on a first side of the taper.

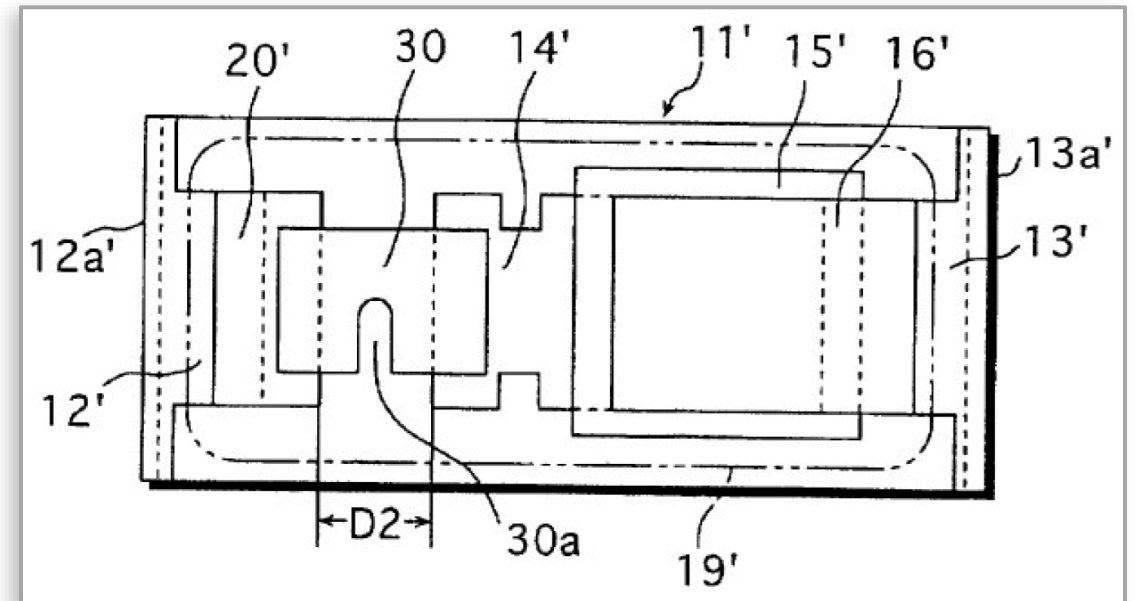
5. The method as claimed in claim 3, wherein the resistance region is formed such that it forms a third contact region on a second side of the taper and thus forms a resistor that is electrically connected in series with the capacitor.

6. The method as claimed in claim 2, wherein a plurality of capacitors and/or resistors are formed electrically in parallel with one another and/or electrically in series one after another.

'492 Patent, cls. 3, 5, 6

Modifying Hanamura to Include Egitto's Resistor Would Have Been Obvious

Hanamura in view of Egitto renders obvious the claimed second and third trench that delimit a resistance region. For example, Hanamura discloses that “[a]nother object of [its] present invention is to provide a chip type thick film capacitor which additionally incorporates a resistor having a reliably adjusted resistance.” Hanamura, 2:39-40; Ex.1003, ¶257. Hanamura provides an example of such a structure in its second embodiment, Hanamura, 5:63-7:39. Hanamura teaches that the resistance of the device can be “reliably adjusted” by adjusting the dimensions of a resistor layer 30, *id.*, 6:50-58, as well as by trimming a groove 30a to change the overall shape of the layer, *id.*, 7:34-39, as shown in Figure 8 below.



Hanamura, Fig. 8

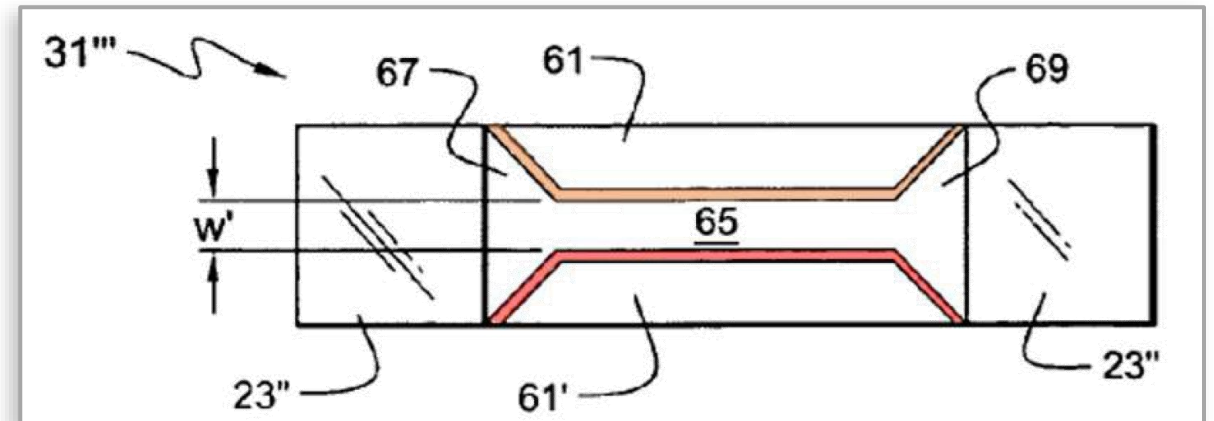
Pet., 60-61

Modifying Hanamura to Include Egitto's Resistor Would Have Been Obvious

As previously discussed, Egitto relates to providing resistors for circuitized substrates and is focused on adjusting the resistance of thin film resistors in a circuit. Egitto teaches that “[t]o increase the resistance of a film resistor, the resistor [can be] ‘trimmed’, often by forming a slot across the electrical current path in the resistor and to make the effective width of the resistor (and the current path there-through) smaller and thereby increasing resistance.” Egitto, ¶5. Egitto’s Figure 8 discloses a “representative pattern[,]” which is materially the same design claimed in the ’492 patent. Ex.1003, ¶279.

...

Egitto teaches that the resistor material can be etched away to form “isolated parts 61 and 61’,” which are “substantially trapezoidal, meaning that the center, remaining material (65) has a rectangular shape with substantially triangular ends 67 and 69.” See Egitto, ¶82. Egitto discloses that the etching process is “preferably accomplished using a laser.” *Id.*, ¶83. As shown above, the process involves creating two trenches (orange and red), creating a taper in a direction parallel to the resistor material. Ex.1003, ¶280.



Egitto, Fig. 8

Pet., 64-65

See Pet., 60-66

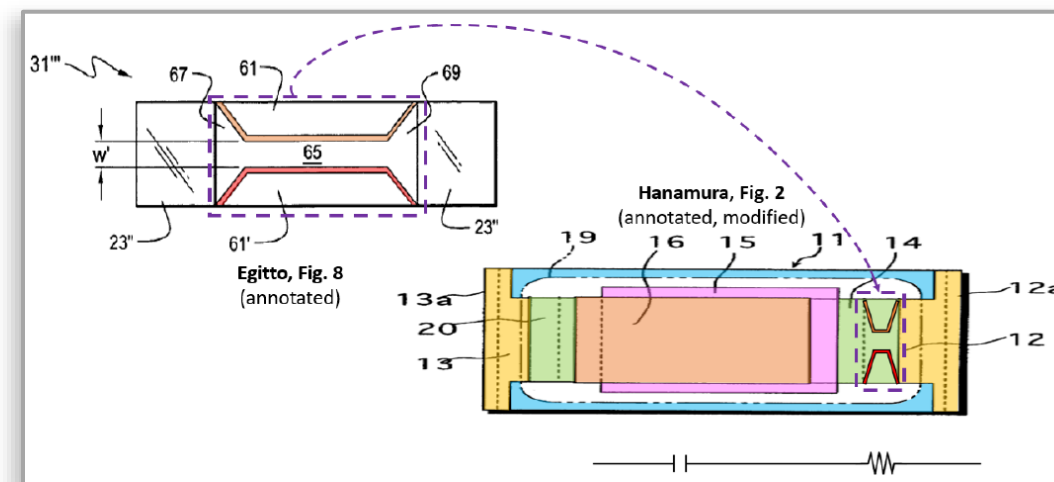
COVINGTON

Demonstrative Exhibit – Not Evidence 94

Modifying Hanamura to Include Egitto's Resistor Would Have Been Obvious

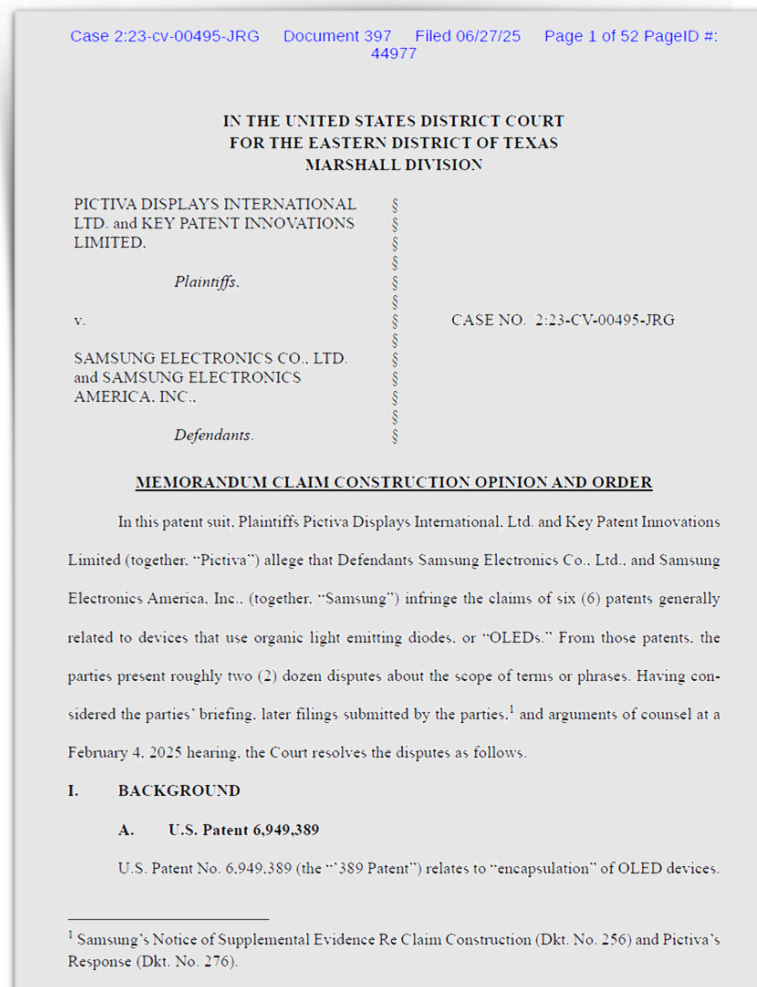
269. A POSITA would expect success from adopting Egitto's design in the electrically conductive layers of Hanamura. Hanamura discloses the concept of trimming a groove 30A in its resistor material to tune its resistance. *See* Hanamura at 6:50-58. Further, Egitto teaches that this groove 30A may be formed into specific, preferable patterns using a laser. Carving this groove would result in a predictable change to resistance, as resistance is directly computable from the resistivity and dimensions of the material via a well-known formula. Since this result is straightforward to predict, a POSITA would have expected the method to be successful. Indeed, Egitto teaches this very line of reasoning, stating that its method "enables the circuit designer to alter the resulting resistance by selectively removing ... material and leaving a desired, precise width thereof remaining as the current path." Ex. 1013, Egitto at [0082].

Ex.1003 (Kattamis Decl.), ¶269



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Pictiva's Claim of Nonobviousness Is Belied by Its Actions in the Related Litigation



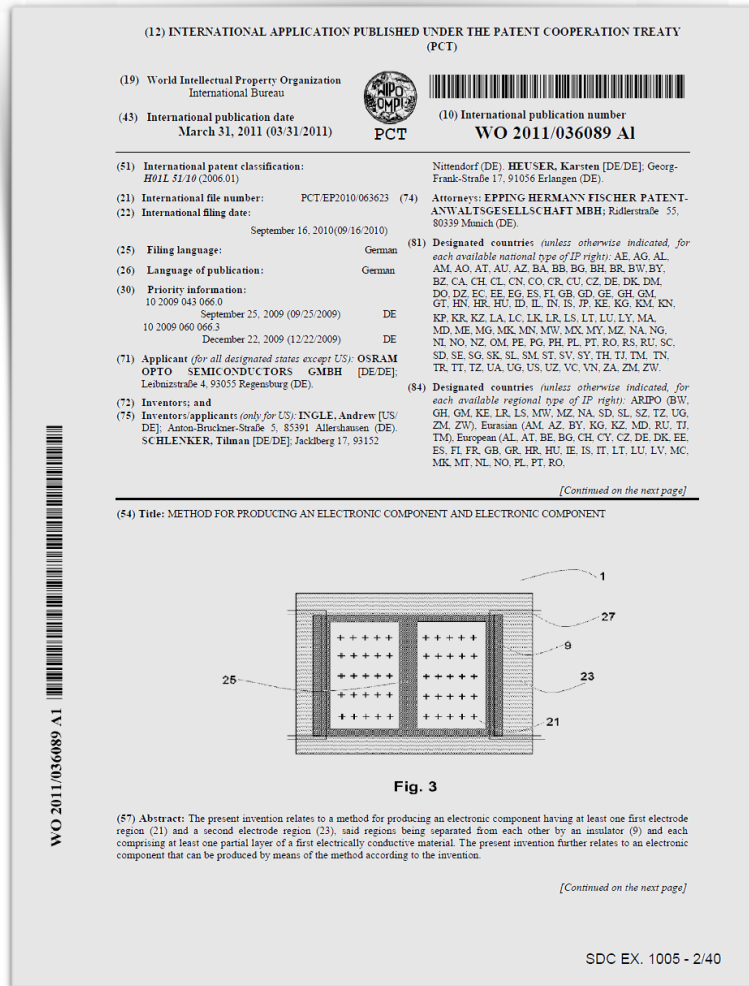
Ex. 2007 (District Court *Markman* Order)

Citing *Bicon, Inc. v. Staumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006), Samsung argues that because all possible taper directions would satisfy the disputed phrase, the limitation is superfluous and therefore invalid. (Dkt. No. 143 at 26.) Pictiva does not dispute that all possible taper directions would satisfy this language, but stresses that Samsung never argues the meaning of the term is unclear. (Dkt. No. 150 at 9.)

Ex.2007 (District Court *Markman* Order), 43

Back-up Slides

Pictiva Incorrectly Asserts Ingle's “a conventional process” Is Limited to “lithography”



The electronic component, for example an OLED, can now be produced on the substrate layer prepared in this way using a conventional process.

Ingle, 21:33-35

In contrast to the conventionally used lithography methods, in which each coating step is applied individually and structured photolithographically, in the methods according to the invention it is intended to apply only as much material of the insulator and the protective material, both of which can generally be expensive materials, as is required for the production of the electronic component. In

Ingle, 16:19-25

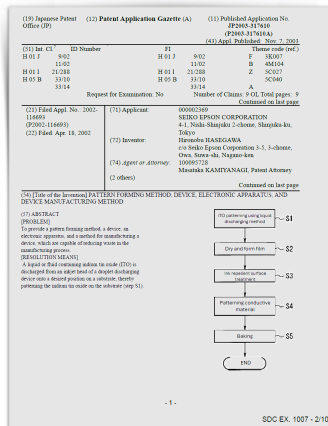
Ingle

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COVINGTON

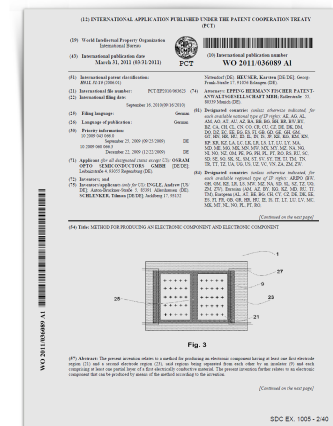
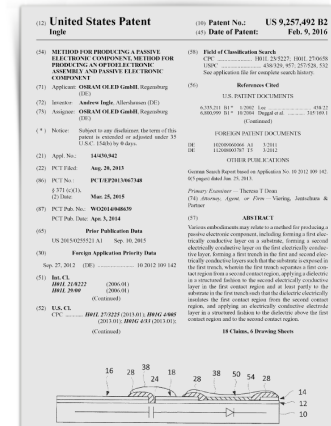
Demonstrative Exhibit – Not Evidence 98

Hasei's Teachings Were Conventional by Ingle's Time, Let Alone by the '492 Patent's Priority Date



If the structuring is already present (i.e. is applied "earlier"), this can be done by applying the first and second electrically conductive layers or parts thereof to the substrate, for example by printing, by deposition with the aid of SAMs (self-assembling monolayers) and the like.

Ingle, 6:9-23



Timeline diagram showing the progression of Hasei and Ingle from 2003 to 2012. The timeline is marked with years from 2003 to 2012. Hasei is represented by a horizontal line starting at 2003 and ending at 2010. Ingle is represented by a horizontal line starting at 2003 and ending at 2012. A vertical line at 2010 is labeled '492 Patent'.

Pictiva's Attempts to Distort Dr. Kattamis' Testimony

As for the imaginary capacitor allegedly suggested by Petitioner's combination, Samsung's expert conceded that, at least in the context of passive electronic components in integrated circuits, photolithography was the conventional method—not the application of layers in a structured manner claimed in the '492 Patent. *See* EX2006, at 85:2-86:2. And he further admitted that “generally the techniques that were used for photolithography ... [were] at that time [2012] much more advanced than printing methods.” *Id.* at 35:2-11.

POR, 40; *see also id.*, 3

2 Q. Paragraph 3 describes a conventional
3 method of providing a conductive pattern.
4 Do you see that?
5 A. Sure. I do.
6 Q. And you agree that Paragraph 3 is
7 describing a conventional method that involves a
8 subtractive fabrication technique and not the
9 application of layers in a structured manner?
11 THE WITNESS: Sure. I mean, it's using
12 the term "conventional" in 2002 to describe
13 photolithography as being conventional at
14 that time.
16 Q. And do you disagree that
17 photolithography was conventional in 2012?
19 THE WITNESS: It depends on the context.
21 Q. In the context of forming a passable
22 electronic component?
24 THE WITNESS: So for passable electronic
25 components in integrated circuits, I would
1 say yes, or in -- let me rephrase that. In
2 inorganic semiconductors, yes.

Ex. 2006 (Kattamis Tr.), 85:2-86:2 (objections omitted)

The Federal Circuit Has Held Concurrent Performance Is Allowable



Nowhere does the plain language of claim 24 require separate and consecutive performance of the various guiding steps.

Moba, B.V. v. Diamond Automation, Inc., 325 F.3d 1306, 1314 (Fed. Cir. 2003)