

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CANADIAN SOLAR INC.,
Petitioner

v.

MAXEON SOLAR PTE. LTD.,
Patent Owner

Case IPR2024-01194
U.S. Patent No. 11,251,315

**DECLARATION OF DAVID L. CARROLL, PH.D. IN SUPPORT OF
PATENT OWNER PRELIMINARY RESPONSE**

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Maxeon EX2001
CSI v. Maxeon
IPR2024-01194

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I. INTRODUCTION

1. I submit this declaration in support of the preliminary response submitted by Maxeon Solar Pte. Ltd. (“Maxeon” or “Patent Owner”) in connection with the Petition for *Inter Partes* Review of U.S. Patent No. 11,251,315 (“the ’315 patent”) filed by Canadian Solar Inc. (“CSI” or “Petitioner”).

2. I am not an employee of Maxeon or any affiliate of subsidiary thereof.

3. I am being compensated for my work in this matter at my standard rate of \$300/hour. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this matter.

4. My compensation is not contingent on the outcome of this matter or the content of my testimony.

5. I understand from Maxeon’s counsel that CSI has challenged the validity of claims 16 and 19 of the ’315 patent (the “Challenged Claims”) based on obviousness under 35 U.S.C. § 103.

6. Accordingly, I have been asked to provide certain opinions relating to the validity of the Challenged Claims. Specifically, I have been asked to provide my opinions regarding (i) the level of ordinary skill in the art to which the ’315 patent pertains; (ii) the scope and content of the prior art; (iii) the differences between the prior art and the Challenged Claims; and (iv) whether a person of

ordinary skill in the art at the time of the claimed invention would have been motivated to combine or modify the prior art to achieve the claimed invention.

7. As set forth in detail below, it is my opinion that the Challenged Claims would not have been obvious based on the proposed combinations in CSI's Petition.

8. In preparation of this declaration, I have reviewed the following documents and any other documents cited in this Declaration:

Exhibit	Description
EX1001	U.S. Patent No. 11,251,315 ("the '315 patent")
EX1002	File History of U.S. Patent No. 11,251,315
EX1003	Declaration of Sanjay Banerjee, Ph.D. Regarding U.S. Patent No. 11,251,315
EX1004	Curriculum Vitae of Sanjay Banerjee, Ph.D.
EX1005	U.S. Patent Pub. No. 2011/0214719, "Method of Fabricating a Back-Contact Solar Cell and Device Thereof" ("Li")
EX1006	King, Sinton and Swanson, "Studies of Diffused Phosphorous Emitters: Saturation Current, Surface Recombination Velocity, and Quantum Efficiency," IEEE Transactions On Electron Devices, Vol 37, No. 2 (Feb. 1990) ("King")
EX1007	Marvin and Froedge, "Interdigitated Back Contact Silicon Solar Cell Analysis and Design Recommendations for Space Use," AD-A220-414 (Sept. 30, 1989) ("Marvin-DTIC")
EX1008	Muller et al., "Ion Implantation for All-Alumina IBC Solar Cells with Floating Emitter," Energy Procedia 55 (2014), 265-271 ("Muller")

Exhibit	Description
EX1011	Neuhaus and Munzer, <i>Industrial Silicon Wafer Solar Cells</i> , Advances in OptoElectronics, 1-15, at 11 (2007) (“Neuhaus”)
EX1015	U.S. Patent No. 4,234,352, “Thermophotovoltaic Converter and Cell for Use Therein” (“Swanson-352”)
EX1017	U.S. Patent No. 4,053,335, “Method of Gettering Using Backside Polycrystalline Silicon” (“Hu”)
EX1025	Ramappa and Benley, “Diffusion of Iron in Silicon Dioxide,” Journal of the Electrochemical Society 146(1) 3773-3777 (1999) (“Ramappa”)
EX1026	U.S. Patent Pub. No. 2006/0118868, “A Semiconductor Substrate Comprising a Support Substrate Which Comprises a Gettering Site” (“Yoshimura”)
EX1029	Liu et al., “Effective impurity gettering by phosphorous- and boron-diffused polysilicon passivating contacts for silicon solar cells,” Solar Energy Materials and Solar Cells 179 (2018) 136-141 (“Liu-2”)
EX1035	Marvin and Froedge, “Analysis of Interdigitated Back Contact Silicon Solar Cells for Space Use,” IEEE (1989) (“Marvin-IEEE”)
EX2015	Granek et al., “Front surface passivation of n-type high-efficiency back junction silicon solar cells using front surface,” Solar Energy Materials and Solar Cells, 91(7) (2007)
EX2016	“Nanotechnology improves solar cell efficiency,” <i>EarthSky</i> , August 28, 2007 (accessible at https://earthsky.org/human-world/nanotechnology-improves-solar-cell-efficiency ; last accessed October 14, 2024)
EX2017	“New Plastic Solar Cell Breaks Efficiency Record,” <i>ScienceDaily</i> , April 20, 2007 (accessible at https://www.sciencedaily.com/releases/2007/04/070419140902.htm), last accessed October 14, 2024)

Exhibit	Description
EX2018	Capshaw-Mack, C., “Power Games: Project seeks to improve methods of harnessing solar energy,” <i>Winston-Salem Journal</i> , August 4, 2013 (accessible at https://journalnow.com/news/local/article_1d243ff0-fc9e-11e2-b607-001a4bcf6878.html ; last accessed October 15, 2024)

9. In forming the opinions expressed below, I have considered the documents listed above and my own knowledge and experience in the field of solar cell technology, as described below.

II. QUALIFICATIONS AND PROFESSIONAL EXPERIENCE

10. My complete qualifications and professional experience are described in my Curriculum Vitae (“CV”), a copy of which can be found at Appendix A. The following is a brief summary of my relevant qualifications and professional experience.

11. In 1985, I received my Bachelor of Science degree in Physics from North Carolina State University (“N.C. State”). In 1993, I received my Ph.D. in Physics from Wesleyan University. My dissertation was titled *Defect Formation and Electron Trapping in Oxides* and comprised a study on the dynamic energy redistribution and statistics of charged defects in oxide materials.

12. I am currently a Professor in the Department of Physics at Wake Forest University and also serve as an Adjunct Associate Professor of Biomedical Engineering at the Virginia Tech – Wake Forest University School of Biomedical

Engineering and Sciences, and as an Adjunct Associate Professor of Cancer Biology at the Wake Forest School of Medicine. From 2003 to 2010, I was an Associate Professor in the Department of Physics at Wake Forest University and was a Director of the Center for Nanotechnology and Molecular Materials, during which time I was awarded tenure.

13. From 2002 to 2003, I was as an Associate Professor of Materials Science in the Department of Physics and Astronomy at Clemson University. In the same department, I was an Associate Professor of Physics from 2001 to 2002, and an Assistant Professor of Physics from 1997 to 2001.

14. From 1995 to 1997, I served as a research associate at the Max-Planck-Institut für Metallforschung, Institut für Werkstoffwissenschaft, in Stuttgart, Germany in 1994. From 1993 to 1995, I served as a Postdoctoral Research Associate in the Department of Materials Science and Engineering at the University of Pennsylvania.

15. At Wesleyan University, I served as an observational astronomer in the Van Vleck Observatories from 1987 to 1989, and as a graduate and research assistant in the Department of Physics from 1987 to 1992.

16. Beyond my academic experience, I have significant professional experience in the fields of physics, materials science, and solar technology. In 2001, I helped found Tetramer Technologies, an advanced materials company

dedicated to the development of market-driven materials and transitioning those materials from the lab to the market, and served as a technical advisor and board member from 2001 to 2003. I also helped found and served in the same positions at NanoTechLabs, a nanomaterial and nanocomposite application development company, from 2001-2004; PureLux, a nanotechnology lighting company, from 2007 to 2011; FiberCell, a laboratory-scale hollow fiber solar cell company, from 2007 to 2010; and Camel City Solar, a spin-out solar cell company from the Wake Forest Nanotechnology Center, from 2011 to 2013. I also served as a technical advisor at CeeLite, a clean technology lighting company, from 2011 to 2013, and VF Corporation, one of the world's largest apparel, footwear, and accessories companies, from 2013 to 2019. In 2022, I helped found Quoherent, a cutting-edge startup pioneering the next frontier in quantum computing, and have since served as a technical advisor.

17. I have received a number of awards and honors for my academic and professional accomplishments, including being named as a Fellow of the American Physical Society in 2013 and the International Association of Advanced Materials (Europe) in 2024. A complete a list of my awards and honors can be found in Section 2 of my CV.

18. I have authored several books and book chapters and my work has been published in nearly 300 publications since 1990, including numerous

publications on my work with solar cell technologies. A complete list of my publications and publication metrics are listed in Sections 3.1 to 3.3 of my CV.

19. I am an inventor on 35 issued U.S. patents, including patents related to solar cell technologies. A complete list of my patents can be found in Section 3.4 of my CV.

20. I have received over \$29 million in research grants from various federal and industrial funding sources, including over \$500,000 in research grants related to my work with solar cell technologies. A complete list of my research grants can be found in Section 3.5 of my CV.

21. I have presented my work at numerous scholarly conferences, including my work with solar cell technologies. A complete list of my scholarly presentations can be found in Section 3.6 of my CV.

22. My work with solar cell technologies has also been recognized by various publications, including EarthSky, ScienceDaily, and the Winston-Salem Journal. *See* EX2016; EX2017; EX2018.

III. LEGAL STANDARDS

23. I understand that in *inter partes* review proceedings, a patent claim is construed using the same standard that would be used in a civil action, and that a claim should be construed in accordance with the ordinary and customary meaning

of the claim as it would be understood by a person of ordinary skill in the art (“Skilled Artisan”).

24. While I am neither a patent lawyer nor an expert in patent law, I have been informed of the applicable legal standards for obviousness. I have relied upon these legal principles, as explained to me by counsel, in forming my opinions set forth in this Declaration.

25. I understand that a patent may be deemed invalid based on obviousness over the prior art. My understanding of this basis for invalidity is discussed in greater detail below.

26. In addition, I understand that objective evidence of non-obviousness such as (i) commercial success, (ii) long-felt but unresolved need, (iii) failure of others, (iv) skepticism by experts, and (v) unexpected results should also be considered in determining whether a claim would have been obvious, if relevant.

27. I understand that in undertaking an invalidity analysis, the claims are to be interpreted from the perspective of a Skilled Artisan.

A. Person of Ordinary Skill in the Art

28. I am informed and understand that patent claims are interpreted from the perspective of a person of ordinary skill in the art (“Skilled Artisan”) at the time of the invention.

29. I understand that a Skilled Artisan is a hypothetical person who is presumed to have known the relevant art at the time of the invention. Such a hypothetical person would have the capability of understanding the scientific and engineering principles applicable to the pertinent art of the claimed invention. Factors that may be considered in determining the level of ordinary skill in the art include: (A) the type of problems encountered in the art; (B) prior art solutions to those problems; (C) rapidity with which innovations are made; (D) sophistication of the technology; and (E) educational level of active workers in the field.

30. The '315 patent generally relates to a TOPCon solar cell—a solar cell with a silicon substrate, a dielectric region formed over the back side of the silicon substrate, an emitter region over the dielectric region, and a metal contact formed over the emitter region. I understand that CSI asserts that the “person of ordinary skill in the art in the 315 Patent’s field of solar cell design or manufacture in the December 2014 timeframe (“Skilled Artisan”) would have been someone with an advanced degree involving the discipline of electrical engineering, applied physics, chemistry, or materials science, and at least two years of experience designing, developing, or researching in the field.” Pet., 11. CSI also asserts, alternatively, that the Skilled Artisan “would have had a bachelor’s degree in electrical engineering, applied physics, or materials science, and at least three years of experience designing, developing, or researching in the field.” Pet., 11.

31. For the purposes of this Declaration, I apply CSI's level of ordinary skill. Further, I possessed at least such experience and knowledge at the relevant time frame for the '315 patent, and my opinions apply equally under either proposed level of ordinary skill. I will therefore apply the same definition in this declaration.

B. Obviousness

32. I have been informed that a patent claim is invalid as being obvious in view of the prior art if the differences between the patented subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time of the invention to a person having ordinary skill in the art. In making a determination of obviousness, I understand that the following factors are analyzed: (i) the scope and content of the prior art; (ii) the differences, if any, between the prior art and the claims at issue; (iii) the level of ordinary skill in the pertinent art; and (iv) objective evidence of non-obviousness, if any exists.

33. I have been informed that any of the following rationales are some of the acceptable bases for the conclusion that a claim is obvious: (i) the claimed invention is simply a combination of prior art elements according to known methods to yield predictable results; (ii) the claimed invention is a simple substitution of one known element for another to obtain predictable results; (iii) the claimed invention uses known techniques to improve similar devices (methods, or

products) in the same way; (iv) the claimed invention was “obvious to try” because it was a choice from a finite number of identified, predictable solutions, with a reasonable expectation of success; (v) there is known work in one field of endeavor that may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces, if the variations would have been predictable to a Skilled Artisan; or (vi) there is some teaching, suggestion, or motivation in the prior art that would have led a Skilled Artisan to modify the prior art references or to combine prior art reference teachings to arrive at the claimed invention.

34. I have been informed that in order for a patent claim to be considered obvious, at the time the invention was made, each and every limitation of the claim must be present within the prior art, or within the prior art in combination with the general knowledge held by a Skilled Artisan, and that such a person would have a reasonable expectation of success in combining these teachings to achieve the claimed invention. I also understand that the reason to select and combine features, the predictability of the results of doing so, and a reasonable expectation of success of doing so may be found in the teachings of the prior art themselves, in the nature of any need or problem in the field that was addressed by the patent, in the knowledge of a Skilled Artisan in the field at the time, as well as in common sense

or the level of creativity exhibited by a Skilled Artisan. There need not be an express or explicit suggestion to combine references.

35. I understand that substituting one known element for another known element would have been obvious when it leads to reasonably predictable results.

36. I understand that a combination of elements would have been obvious when a Skilled Artisan has a good reason to pursue the combination, which is among a finite number of known options within his or her technical grasp, and leads to reasonably expected results.

37. I understand that, when a prior art reference does not expressly disclose a claim limitation, inherency may supply the missing claim limitation. I also understand that, if a limitation is inherent in the prior art reference, that limitation may not be clearly described in the prior art reference but is a natural result flowing from the explicit disclosure of the prior art. I understand that for a claimed element to be inherently present within a prior art document, it must be necessarily present. That is, the prior art reference must necessarily function in accordance with or include the claimed element. I understand that inherency may not be established by probabilities or possibilities—the mere fact that a certain thing may result from a given set of circumstances is not sufficient.

38. A prior art reference can be said to teach away when a Skilled Artisan would be discouraged from following the path set out in the reference or would be

led in a direction divergent from the path that was taken in the claimed invention.

The mere disclosure of more than one alternative does not constitute a teaching away from alternatives that are not disclosed when the prior art does not criticize, discredit, or otherwise discourage the solution claimed in the alleged invention.

Similarly, a prior art reference that merely expresses a general preference for an alternative invention does not teach away.

39. I have relied upon this understanding of the applicable legal standards in reaching my opinion set forth in this Declaration.

IV. OVERVIEW OF THE '315 PATENT

A. The '315 Patent

40. The '315 patent discloses “solar cell fabrication techniques to improve solar cell lifetime, passivation and/or efficiency” (EX1001, 3:17-21) in tunnel oxide passivated contact (“TOPCon”) solar cell configurations.¹ “Efficiency is an important characteristic of a solar cell as it is directly related to the solar cell’s capability to generate power.” EX1001, 1:35-37. As explained below, charge

¹ While the TOPCon moniker was not coined until 2013 by researchers at the Fraunhofer Institute for Solar Energy Systems, SunPower had been developing and optimizing solar cells employing tunnel oxide layers between the silicon substrate and doped polysilicon regions prior to 2013.

carrier lifetime and surface passivation are inter-related characteristics, in which improving one has the potential to negatively impact the other or increase the cost and complexity of the solar cell. But the solar cell covered by the Challenged Claims provides for improvements in *both* of these performance characteristics *and* a boost in solar cell efficiency.

41. The “lifetime” of charge carriers in a solar cell refers to the average time that electrons and holes can exist before recombining. The longer the charge carriers can remain separate, the greater the chance they have to reach the electrical contacts of the solar cell and contribute to the current output, thus increasing the solar cell’s efficiency. Accordingly, a “[h]igher lifetime is preferred for high efficiency solar cells.” EX1001, 9:35-36. Neuhaus and Munzer, *Industrial Silicon Wafer Solar Cells*, Advances in OptoElectronics, 1-15, at 11 (2007) (“Neuhaus”), discloses that to improve the lifetime of charge carriers, manufacturers often use high-quality, pure semiconductor materials and carefully control the manufacturing process to reduce defects within the crystal lattice. *See* EX1011, 11 (“SunPower is using wafers with lifetimes greater than 1millisecond.”). These defects can act as recombination centers where electrons and holes prematurely recombine, reducing

the lifetime of charge carriers. These higher-grade materials and more stringent manufacturing controls, however, increase costs.²

42. “Surface passivation” involves the treatment of a solar cell’s surface to reduce the number of recombination sites available. This is typically achieved by creating a thin insulating layer (such as silicon nitride or aluminum oxide) on the surface of the semiconductor material, which can prevent charge carriers from recombining at the surface. The ’315 patent states that “[l]ower surface passivation is preferred for high efficiency solar cells.” EX1001, 9:27-28. The deposition of passivation layers requires additional steps in the production process, which can increase the time and resources needed to manufacture solar cells. Moreover, if not carefully optimized, the passivation layer can introduce electronic defects or impede the collection of charge carriers, potentially reducing the overall efficiency or preventing one from achieving optimized conditions.

B. The ’315 Patent’s Novel Solar Cell Fabrication Technique

43. The ’315 patent discloses a solar cell fabricated by (1) forming a dielectric region (e.g., a tunnel oxide layer) over a silicon substrate, (2) forming an

² Additionally, the processes used to improve lifetime, such as thermal treatments, can introduce other challenges, such as increased stress within the solar cell, which can affect its mechanical stability.

emitter region over the dielectric region, (3) forming a dopant region (e.g., a dopant source layer) on a surface of the silicon substrate, and (4) heating the solar cell above 900 degrees Celsius such that the surface of the solar cell is doped to a concentration of less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ and the emitter region contains contaminants gettered from the silicon substrate through the dielectric region. These fabrication steps are illustrated in Figures 1-4 (annotated below).³

³ Throughout its Petition, CSI and Dr. Banerjee allege that the solar cell design disclosed in the '315 patent is a “back-contact solar cell” to draw comparisons with the asserted Li reference. However, the '315 patent is not limited to a “back contact solar cell.” EX1001, 7:13-14. In fact, independent claims 1 and 10 require only a single emitter region and contact (e.g., a first emitter region and a first metal contact). For claim 1, the emitter and metal contact are on the front side of the solar cell, and, for claim 10, they are on the back side. Dependent claim 20, which CSI has not challenged, is the first limitation that requires both “P-type” and “N-type doped polysilicon region[s]” formed on the back side of the solar cell, which is a “back contact solar cell” configuration.

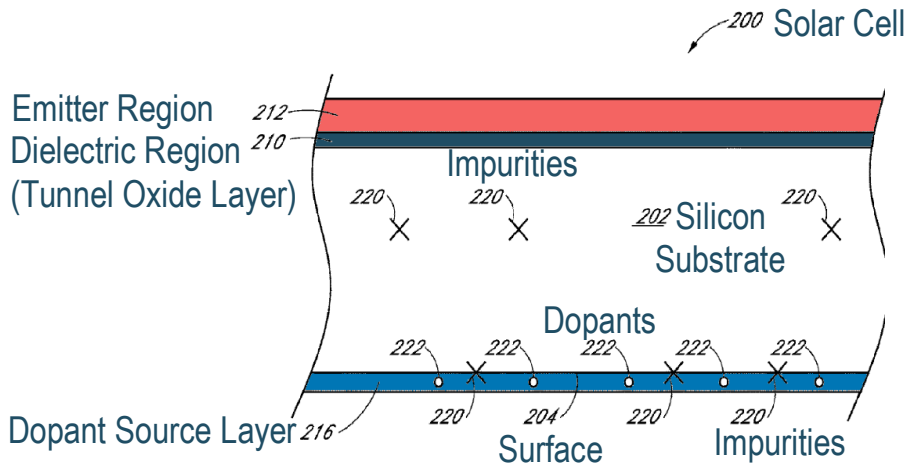


FIG. 2

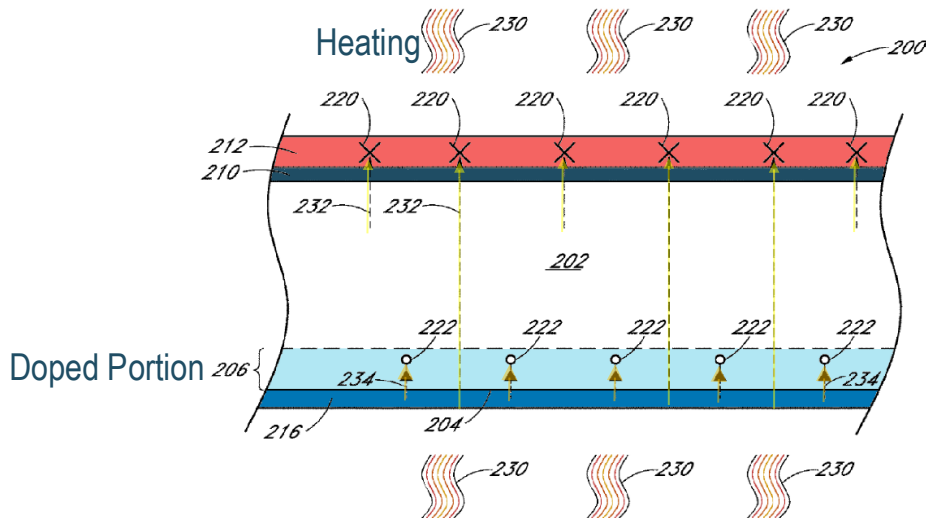


FIG. 3

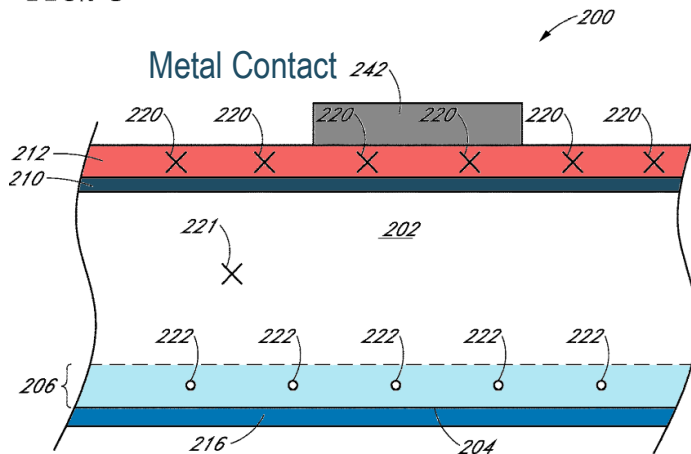


FIG. 4

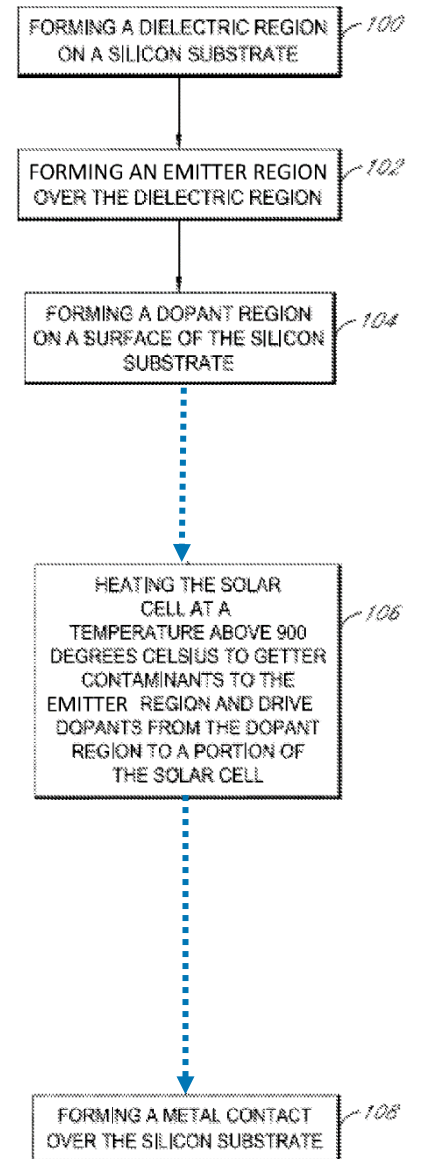


FIG. 1

EX1001, FIGs. 1-4 (annotated).

44. The '315 patent explains (and summarizes in Figure 11) that this particular combination of steps to form a solar cell provided increased efficiency that was both unique and unexpected. Figure 11 shows four processes where the heating temperature and surface dopant concentrations were varied and the gettering location, surface passivation, lifetime, and efficiency results were measured.⁴ See EX1001, FIG. 11 (below, color annotations added).

⁴ I agree that an inadvertent error was made in Figure 11 that shows all the temperature settings to be less than or equal to 900 degrees Celsius. See Pet., 13 n.3. The original application included the same information as Table 1 in the specification, which was later amended to be Figure 11. EX1002, 43. Table 1 in the original application correctly shows that the Example Processes C and D in Figure 11 should have temperature settings at *greater than* 900 degrees Celsius as described in the text. EX1002, 43.

Variables			Results			
Example Process	Temp	Surface Dopant Conc.	Gettering Location	Surface Passivation	Lifetime	Efficiency
A	≤ 900 deg-C	$2 \times 10^{18} \text{ cm}^{-3}$	non-poly	2 fA/cm^2	$\sim 3 \text{ msec}$	Baseline
B	≤ 900 deg-C	$4 \times 10^{18} \text{ cm}^{-3}$	non-poly	5 fA/cm^2	$\sim 10 \text{ msec}$	Baseline
> 900 deg-C C	≤ 900 deg-C	$2 \times 10^{18} \text{ cm}^{-3}$	poly	2 fA/cm^2	$\sim 10 \text{ msec}$	+0.5 % abs.
> 900 deg-C D	≤ 900 deg-C	$4 \times 10^{18} \text{ cm}^{-3}$	poly	5 fA/cm^2	$\sim 10 \text{ msec}$	Baseline

Table 1. Example Processes for Solar Cell Fabrication

FIG. 11

EX1001, FIG. 11 (annotated).

45. In Example Process A, low temperature (e.g., ≤ 900 degrees Celsius) heating and low surface dopant concentration (e.g., $2 \times 10^{18} \text{ cm}^{-3}$) were used. The '315 patent explains that "[o]xides and/or tunnel oxides, such as the dielectric region . . . , can be barriers to gettering of the metal impurities 220 to emitter regions" and that "heating at temperature at 900 degrees Celsius or below can be insufficient to diffuse metal impurities through a tunnel oxide and into a polysilicon region." EX1001, 5:15-20. Accordingly, the "Gettering Location" for Example Process A is the "non-poly" silicon substrate, rather than the "poly" emitter region. The combination of low temperature gettering and low surface dopant concentration allows for good surface passivation, but poor lifetime.

46. Example Process B also uses low temperature heating, but a higher surface dopant concentration (e.g., $4 \times 10^{18} \text{ cm}^{-3}$). Like Example Process A, the gettering location remains in the “non-poly” silicon substrate. The low temperature gettering and higher surface dopant concentration results in a good lifetime, but poor surface passivation. Example Processes A and B demonstrate the kind of trade-offs that are made when designing solar cells. Having a low surface dopant concentration results in good surface passivation, but poor lifetime; whereas a high surface dopant concentration results in good lifetime, but poor surface passivation. For both processes, the efficiency of the solar cell remained the same.

47. The unexpected result came from Example Process C, where high-temperature (e.g., > 900 degrees Celsius) heating and low surface dopant concentration are used. In this process, contaminants from the silicon substrate getter through the dielectric region and into the “poly” emitter region. At the same time, dopants are driven deeper into the silicon substrate from the surface of the silicon substrate resulting in a lower surface dopant concentration. At the time of the invention, it was not known whether high-temperature heating would getter contaminants through the dielectric region, while leaving this region intact and functional, or whether there would be some split between contaminants gettered between the surface of the “non-poly” silicon substrate and the “poly” emitter region, such that lifetime would not show any improvement (which was the case

for Example Process D, described below). Further, a Skilled Artisan would not have expected lifetime to improve by high-temperature heating because the silicon substrate also contains oxygen defects, which would be enlarged at higher temperatures and increase the likelihood of Ingot Ring Defects (IRD), which would reduce lifetime. Example Process C, however, provided both improved surface passivation and lifetime, resulting in a 0.5% increase in efficiency over the other example processes.

48. Example Process D also produced an unexpected result in that high-temperature (e.g., > 900 degrees Celsius) heating did not further improve the lifetime beyond what a high surface dopant concentration already produced in a TOPCon solar cell configuration (e.g., Example Process B). Thus, Example Process D demonstrates that a high-temperature heating step alone does not yield improved efficiency in the claimed solar cell configuration unless the surface dopant concentration is low. In other words, the '315 patent requires a specific combination of fabrication steps and surface dopant concentration to improve the performance of a particular solar cell structure.

C. The '315 Patent Prosecution History

49. It is my understanding that the Examiner agreed that the claimed invention was patentable:

4. The following is an examiner's statement of reasons for allowance: Claims **1 – 20** are allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

portion of the silicon substrate is formed at the back side of the solar cell and a first dielectric region formed over the silicon substrate, wherein the first dielectric region is formed over the front side of solar as recited in the independent claim **1**; and portion of the silicon substrate is formed at the front side of the solar cell; a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of solar; a first emitter region having metal impurities formed over the dielectric region as recited in the independent claim **10**.

EX1002, 207.

50. While the Examiner allowed these claims without issuing any rejections, I note that a significant number of references cited during prosecution resulted from previous searches in related patents.

51. It is my understanding that CSI's petition asserts four grounds of unpatentability against the Challenged Claims. Pet., 3-4. I understand that challenged claim 16 depends from independent claim 10 and thus incorporates the limitations of claim 10. I also understand that challenged claim 19 depends from claim 16 and thus incorporates the limitations of claims 10 and 16. In my opinion, none of CSI's grounds establish that the prior art discloses, teaches, or suggests the claimed "first emitter region having metal impurities formed over the dielectric region" of independent claim 10. Neither do any of CSI's grounds establish that the prior art discloses, teaches, or suggests the claimed "second emitter region

having metal impurities formed over the dielectric region” of dependent claim 16.

Additionally, in my opinion, CSI also does not show that it would have been obvious to a Skilled Artisan to combine the primary reference (Li) with the secondary references (King, Swanson-352, Marvin, and Muller) to teach or suggest the claimed “dopant concentration of approximately less than or equal to 2×10^{18} cm⁻³” of independent claim 10.

V. ALL GROUNDS: CSI AND DR. BANERJEE DO NOT SHOW THAT THE PRIOR ART DISCLOSES “A FIRST EMITTER REGION HAVING METAL IMPURITIES FORMED OVER THE DIELECTRIC REGION” AND “A SECOND EMITTER REGION HAVING METAL IMPURITIES FORMED OVER THE DIELECTRIC REGION.”

52. CSI and Dr. Banerjee rely on U.S. Patent Pub. No. 2011/0214719, “Method of Fabricating a Back-Contact Solar Cell and Device Thereof” (“Li,” EX1005), but acknowledges that Li does not expressly disclose the “metal impurities” in the “first emitter region” of claim 10 and in the “second emitter region” of claim 16. Pet., 47; EX1003, ¶[157]. Instead, CSI and Dr. Banerjee assert that Li inherently discloses these missing limitations. Pet., 47; EX1003, ¶¶[157]-[158]. As explained below, CSI does not show that “metal impurities” are “necessarily present” in the “first emitter region” (claim 10) and the “second emitter region” (claim 16). CSI and Dr. Banerjee also assert two additional prior art references, U.S. Patent No. 4,053,335, “Method of Gettering Using Backside Polycrystalline Silicon” (“Hu,” EX1017), and Ramappa and Benley, “Diffusion of

Iron in Silicon Dioxide,” Journal of the Electrochemical Society 146(1) 3773-3777 (1999) (“Ramappa,” EX1025), which do not disclose a solar cell (let alone a TOPCon solar cell). Pet., 48-49, 70-72; EX1003, ¶¶[162]-[163], [234]-[237].

A. Grounds 1 and 2: CSI and Dr. Banerjee do not show that Li necessarily discloses “a first emitter region having metal impurities” and “a second emitter region having metal impurities.”

53. CSI and Dr. Banerjee concede that Li does not include any mention of a “first emitter region having metal impurities” (claim 10) and a “a second emitter region having metal impurities” (claim 16) (Pet., 47; EX1003, ¶[157]), and I understand that CSI and Dr. Banerjee rely on inherency to meet these limitations. But in my opinion both CSI and Dr. Banerjee do not show that “metal impurities” are necessarily present in Li’s polysilicon doped regions of material layer 506 (e.g., the “first emitter region” and the “second emitter region”).⁵ As discussed below, the cited references used for CSI’s and Dr. Banerjee’s inherency arguments create contradictions, which are not addressed by either CSI or Dr. Banerjee.

⁵ CSI identifies the “polysilicon doped regions of the material layer 506” in Li as corresponding to the claimed “first and second emitter regions” of claims 10 and 16. *See* Pet., 43-44, 47.

1. CSI's and Dr. Banerjee's inherency argument is speculative because Li does not disclose enough information about its dielectric film to determine whether it will allow for gettering.

54. CSI and Dr. Banerjee not only assume that Li's dielectric film allows diffusion of metal impurities during a gettering process, but also misinterprets the teachings of the cited references to wrongly conclude that "Li's heating and diffusing of the dopants into the polysilicon layer at 950°C . . . would necessarily have resulted in impurities being gettered and present in both of Li's doped polysilicon emitter regions, even despite an intervening thin 1-2 nm interfacial silicon oxide layer." Pet., 53; EX1003, ¶[170].

55. CSI states that "publications before and after December 2014 show that metallic impurities are transferred from silicon substrates into polysilicon layers, including through thin silicon oxide layers . . . by gettering." Pet., 48. But a Skilled Artisan would have understood that is not what the references cited by CSI teach. To the contrary, Liu-2 states that there are large "[d]iscrepancies in the reported iron solubility in SiO₂" and "the results are contradictory," which "make it difficult to assess and quantify the blocking mechanisms of the oxide interlayer" between a substrate and a polysilicon film. EX1029, 140. Besides, both Hu and Liu-2 reported that polysilicon layers need to be deposited under optimum fabrication conditions for gettering to occur. EX1017, 4:26-28 ("The polycrystalline silicon deposition temperature has a diverse number of effects and

must be optimized for suitable use in gettering.”); EX1029, 141 (“The presence of the oxide interlayer hinders the gettering effectiveness, although at optimum polysilicon fabrication conditions...the blocking effect is small.”). That is, the gettering of metal impurities into a polysilicon layer is not a simple and straightforward process that inevitably occurs from a substrate into a polysilicon layer as claimed by CSI and Dr. Banerjee. Pet. 47, 49; EX1003, ¶¶[157], [162]. As I explain below, Liu-2 (1) discloses configurations where gettering into polysilicon layers will not occur, and (2) contradicts CSI’s claims related to the teachings of Hu and Ramappa.

56. Liu-2 compared the gettering effectiveness of polysilicon layers by “varying the interlayer oxide properties (chemical oxide, thermal oxide of different thicknesses, and no oxide), and replacing the dopant diffusions with nitrogen anneals.” EX1029, 137. Figure 3 of Liu-2 shows the results of this comparison, where effective gettering is indicated by a low bar (or no bar) on the chart. EX1029, 139 (shown below).

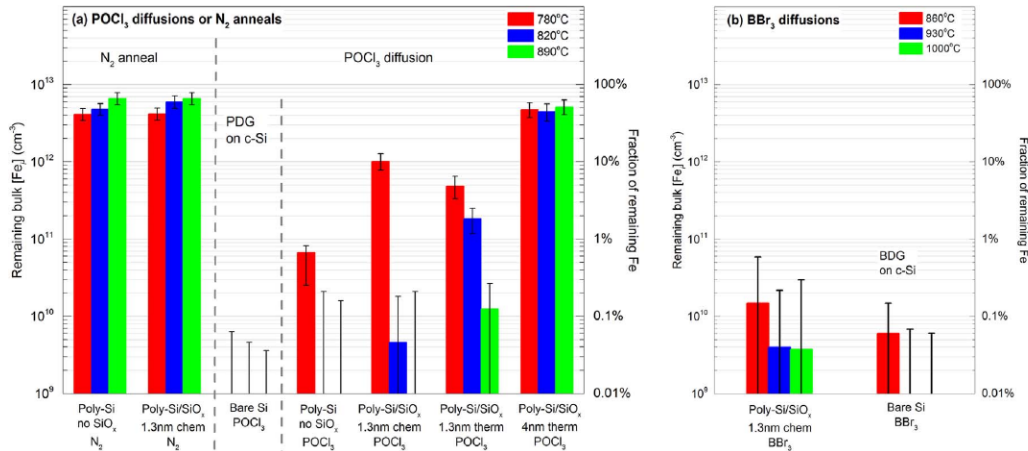


Fig. 3. (a) Comparison of the remaining bulk Fe_i concentrations in samples with intrinsic polysilicon layers annealed in N₂ (with and without chemical oxide interlayer); with POCl₃ diffusions performed on bare crystalline silicon (c-Si) wafers, i.e. conventional phosphorus diffusion gettering (PDG); and with POCl₃-diffused polysilicon layers in the presence of different oxide interlayers (no oxide, chemical oxide of ~1.3 nm, thermal oxide of ~1.3 nm, and thermal oxide of ~4 nm). The N₂ anneal and POCl₃ diffusion temperatures are 780 °C, 820 °C, and 890 °C, and the temperature-time profiles are the same for each temperature. (b) Comparison of the remaining bulk Fe_i concentrations in samples that underwent the same BBr₃ diffusions with and without the polysilicon/oxide layers (1.3 nm chemical oxide). The BBr₃ diffusion temperatures are 860 °C, 930 °C, and 1000 °C. All samples had an initial bulk Fe_i concentration of 10¹³cm⁻³.

EX1029, FIG. 3.

57. Starting from the left, Figure 3 shows that “intrinsic [(i.e., undoped)] polysilicon films . . . do not have a significant gettering action . . . with and without the oxide interlayer.” EX1029, 139, FIG. 3 (annotated below). Similarly, Li discloses doped polysilicon wafers in material layer 506, but lacks any discussion about to what extent the layers are doped and CSI offers no analysis on this point. In my opinion, low doping would weigh against effective gettering, as Liu-2 states that “more effective gettering could be achieved in more heavily doped samples.” EX1029, 140. Thus, with Li being silent about the doping concentration of its polysilicon regions in material layer 506, it would not have been obvious to a Skilled Artisan that gettering of metal impurities into Li’s polysilicon regions in material layer 506 is inevitable.

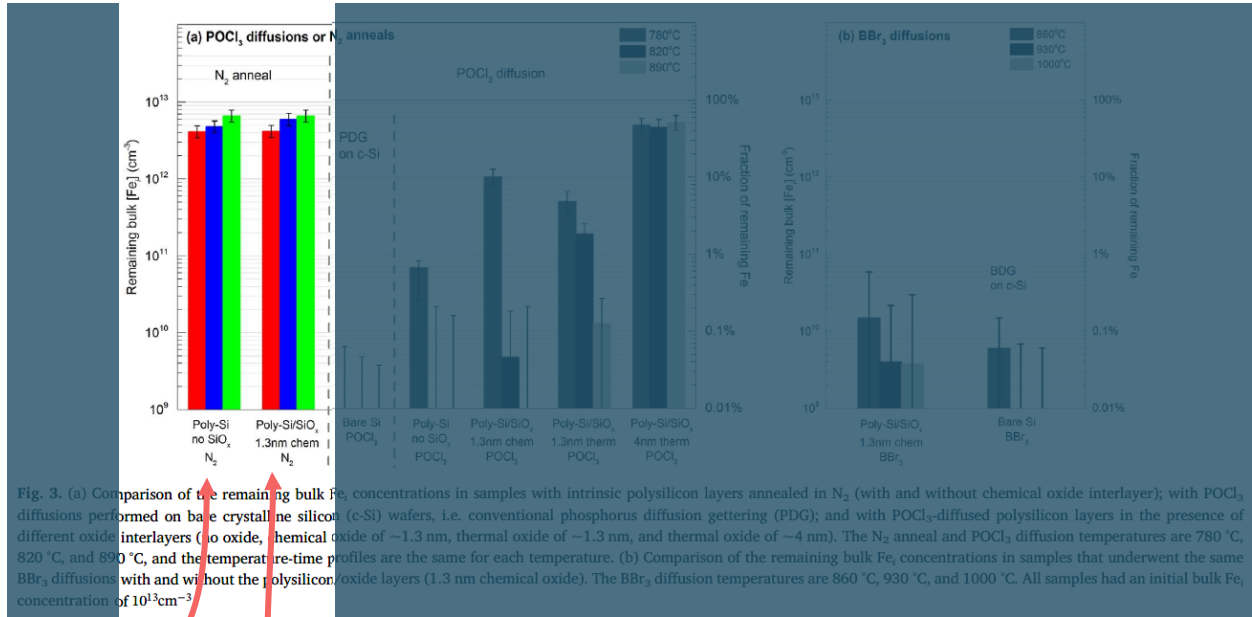


Fig. 3. (a) Comparison of the remaining bulk Fe concentrations in samples with intrinsic polysilicon layers annealed in N_2 (with and without chemical oxide interlayer); with POCl_3 diffusions performed on bare crystalline silicon (c-Si) wafers, i.e. conventional phosphorus diffusion gettering (PDG); and with POCl_3 -diffused polysilicon layers in the presence of different oxide interlayers (no oxide, chemical oxide of ~1.3 nm, and thermal oxide of ~4 nm). The N_2 anneal and POCl_3 diffusion temperatures are 780 °C, 820 °C, and 890 °C, and the temperature-time profiles are the same for each temperature. (b) Comparison of the remaining bulk Fe concentrations in samples that underwent the same BBr_3 diffusions with and without the polysilicon oxide layers (1.3 nm chemical oxide). The BBr_3 diffusion temperatures are 860 °C, 930 °C, and 1000 °C. All samples had an initial bulk Fe concentration of 10^{13}cm^{-3} .

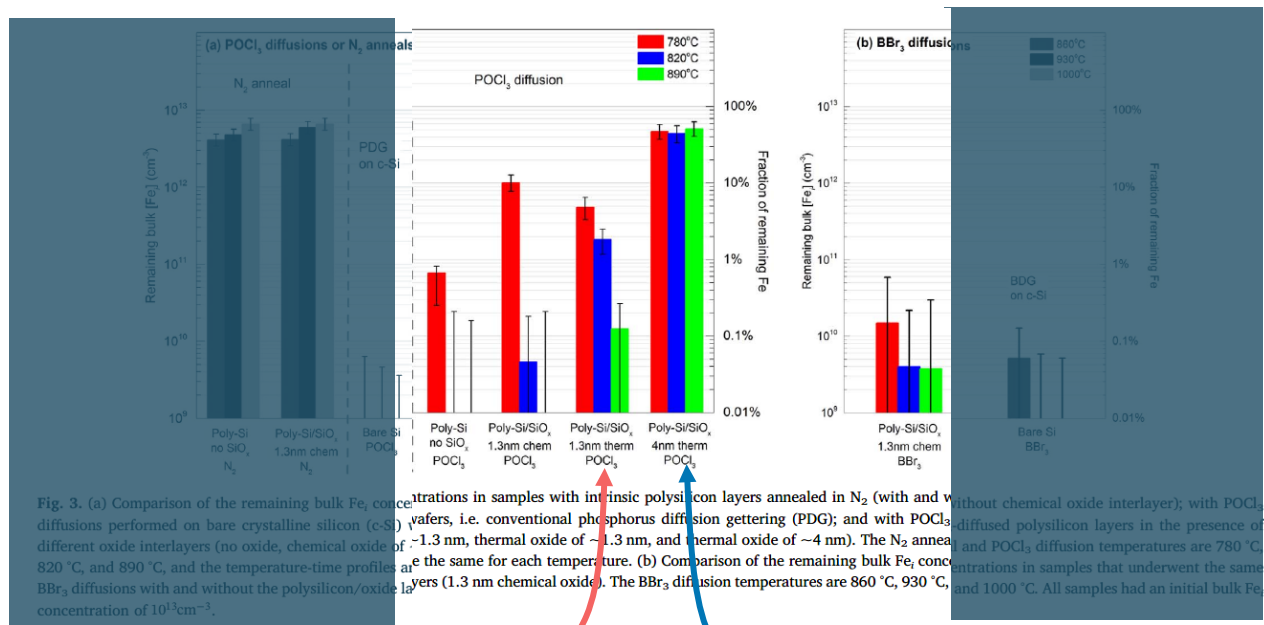
Poly-Si/ SiO_2 1.3nm chem, N_2 = Polysilicon layer with interfacial oxide of 1.3 nm thickness, formed by chemical oxide, no doping

Poly-Si no- SiO_2 N_2 = Polysilicon Emitter with no interfacial oxide, no doping

EX1029, FIG. 3 (annotated).

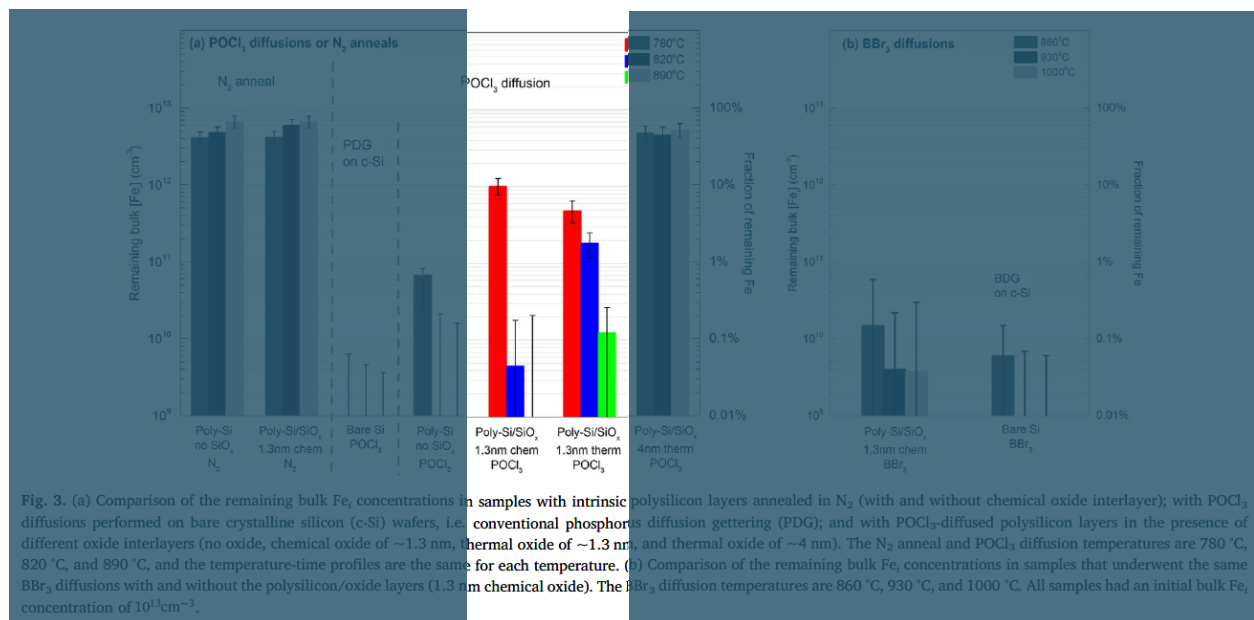
58. Figure 3 of Liu-2 also shows that “[t]he gettering effectiveness of both polysilicon contacts and diffused c-Si wafers . . . increase[s] with increasing diffusion temperature, for both POCl_3 and BBr_3 diffusions,” but “[f]or samples with a 4-nm thick thermal oxide interlayer, ineffective gettering is observed for all diffusion temperatures.” EX1029, 139-40, FIG. 3 (annotated below). This finding of Liu-2 directly contradicts CSI’s and Dr. Banerjee’s argument that “iron diffuses readily across silicon dioxide layers even much thicker (50-100nm)” and there is no explanation regarding this apparent contradiction with Liu-2. See Pet., 49

(discussing Ramappa); EX1003, ¶[163]. Based on such contradicting results, a Skilled Artisan would have understood that gettering of metal impurities into polysilicon layer through oxide layers can be a possibility under certain process conditions, but gettering *cannot necessarily happen under any condition*. And with Li being silent about the thickness of its dielectric oxide film, a Skilled Artisan would not have concluded from these contradicting results that gettering necessarily occurs in Li's solar cell structure.



EX1029, FIG. 3 (annotated).

59. Figure 3 of Liu-2 further shows that gettering effectiveness is related to how the oxide layer is grown. EX1029, FIG. 3 (annotated below). Liu-2 states that “[t]he different gettering effectiveness of the chemical and thermal oxides of the same thickness likely relate to the different oxide density achieved by the two growth methods.” EX1029, 140. In contrast, Li is silent on how its dielectric film is formed.



Gettering for n-type (POCl₃) doped Polysilicon with 1.3 nm oxide is more effective for chemically grown oxide versus thermally grown oxide

EX1029, FIG. 3 (annotated).

60. Thus, Liu-2 teaches that a variety of structural and process dependent variables influence whether an oxide layer will allow effective gettering. And CSI has not shown that all of these variables are disclosed by Li such that gettering of metal impurities through Li's dielectric film is inevitable.

61. Liu-2's teachings about gettering contradict CSI's and Dr. Banerjee's claims related to Hu and Ramappa. Hu discloses "[a]n integrated circuit structure [(i.e., not a solar cell)] . . . which provides for gettering with a backside layer of polycrystalline silicon" that is "either undoped or suitably doped with oxygen." EX1017, Abstract, 3:24-27. CSI and Dr. Banerjee claim that Hu teaches "metal impurities in the silicon substrate would have naturally and inevitably gettered to the backside polysilicon 'material layer' of Li." Pet., 49; EX1003, ¶[162]. But according to Liu-2, undoped (or intrinsic) polysilicon films have an "inability . . . to getter bulk impurities." EX1029, 139. Neither CSI nor Dr. Banerjee reconciles the teaching of Liu-2 with Hu regarding the gettering effectiveness of polysilicon layers. Fortunately, Liu-2 explains that in its solar cell, the polysilicon film was

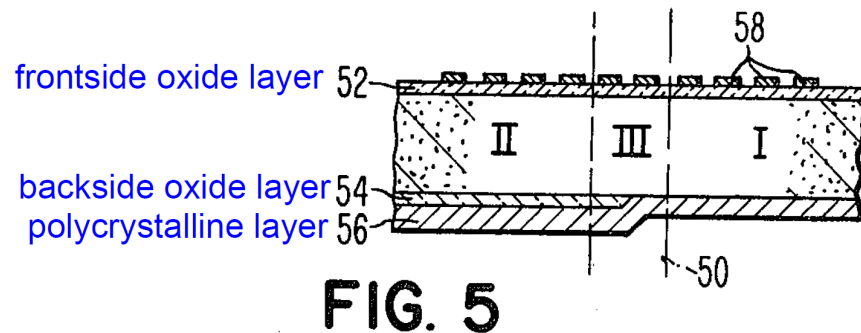
Deposited . . . at low temperature of ~250°C, while those used in microelectronics for backside gettering purposes consist of polysilicon deposited by CVD at much higher temperatures of 600-800°C. In addition, the recommended film thickness for backside polysilicon gettering is 500 nm to 3 µm, which is much thicker than our 30–40 nm deposited a-Si films, offering more grain boundary area for impurity segregation and relaxation. . . . [T]he provision of a sufficient amount of grain boundaries is important for the gettering action of intrinsic polysilicon layers, that is, the thickness ratio of the polysilicon film to the bulk crystalline silicon substrate, where impurities are gettered from, should be considered.

EX1029, 139.

62. Indeed, Hu is a microelectronics patent and discloses polycrystalline silicon films formed within those ranges of temperatures and thicknesses. *See* EX1017, 14:58-15:10 (claiming a layer of polysilicon, “wherein the temperature for depositing said layer is between about 680°C and 800°C and the thickness of said layer being between about 5000 Å and 50000 Å” (i.e., 500 nm to 5 µm)). Li is silent about the thickness of its backside polysilicon material layer 506, the temperature at which it is formed, and the thickness ratio between the backside polysilicon material layer 506 and the substrate 508, which all impact whether gettering would occur. Both CSI and Dr. Banerjee are also silent regarding the same and does not show that metal impurities would be necessarily getterred to the backside polysilicon material layer 506 through dielectric film 510 in Li.

63. Regarding Ramappa, which discloses a “quantitative analysis of diffusion of iron in silicon dioxide,” CSI claims that “iron diffuses readily across silicon dioxide layers even much thicker (50-100nm) than the 1-2 nm layer used by Li.” Pet., 49; EX1003, ¶[163]. Liu-2, however, teaches that “[f]or samples with a 4-nm thick thermal oxide interlayer, ineffective gettering is observed for all diffusion temperatures.” EX1029, 140; *see also* U.S. Patent Pub. No. 2006/0118868, “A Semiconductor Substrate Comprising a Support Substrate Which Comprises a Gettering Site” (“Yoshimura”), EX1026, ¶¶[0047], [0054] (teaching that “the group of impurity metals [can] hardly pass through the SiO₂

film” that was 50 nm thick). Moreover, Hu discloses “an oxide layer on frontside 52 and backside 54” that extends across region I, but not region II, of the structure, and “it was expected that gettering would take place in region I, but not in region II because of the presence of an intermediary oxide barrier.” EX1017, 8:29-44, FIG. 5 (annotated below).



EX1017, FIG. 5 (annotated).

64. In view of Liu-2, Yoshimura, and Hu—which all disclose oxide layers that prevent gettering—CSI and Dr. Banerjee do not reconcile how it can assert that a 100 nm oxide layer could allow for gettering.

65. Thus, the art demonstrates “it [is] difficult to assess and quantify the blocking mechanisms of the oxide interlayer” without at least the information about its numerous variables, such as formation processes, temperatures, densities, dopants, thickness, etc. EX1029, 140. As Li is silent about this information regarding its dielectric film 510, CSI’s and Dr. Banerjee’s claim that “metal impurities in the silicon substrate would have naturally and inevitably gettering to

the backside polysilicon ‘material layer’ of Li” (Pet., 49; EX1003, ¶[162]) through the dielectric film is speculation.

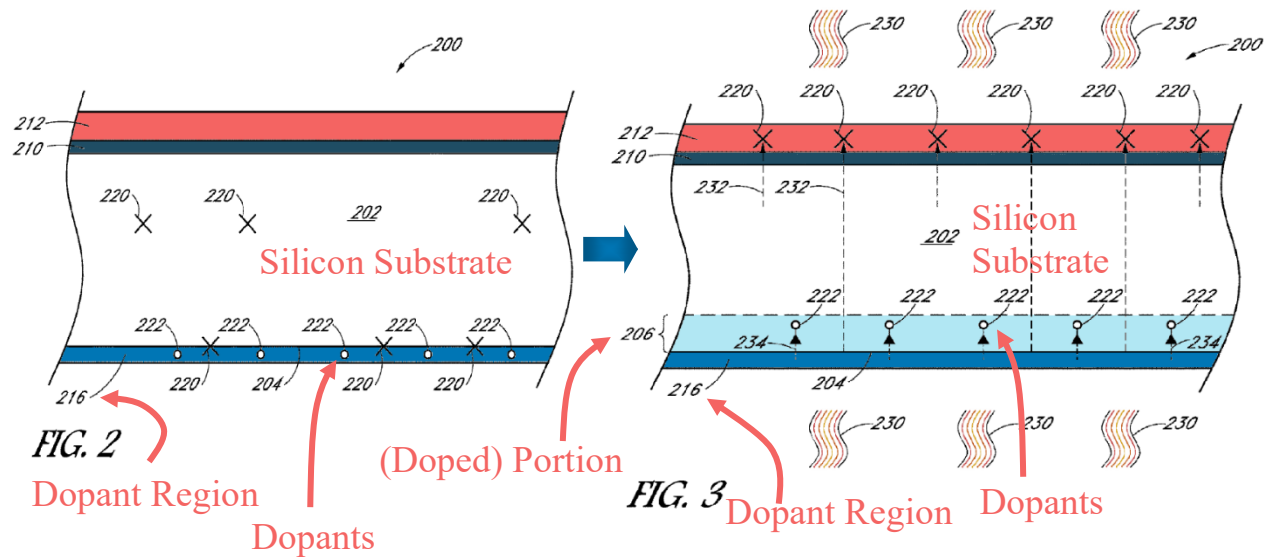
2. CSI’s and Dr. Banerjee’s inherency argument is flawed because Li and the ’315 patent disclose different dopant diffusion processes and heating steps that would affect whether metal impurities are present in the first and second emitter regions.

66. Li and the ’315 patent use different doping processes and high-temperature heating steps at different stages of their fabrication processes, and CSI and Dr. Banerjee have not shown that, despite these differences, “metal impurities” will necessarily be gettered into the “material layer” of Li. Initially, CSI asserts that Li and the ’315 patent are the same with regard to their (1) doping processes and (2) heating steps. Pet., 23, 47. Later, CSI and Dr. Banerjee concede that Li discloses a different heating approach, but claims that it would have been obvious to a Skilled Artisan to make Li like the ’315 patent. Pet., 53, n.9; EX1003, ¶[171].

67. **Different Doping Processes.** CSI incorrectly states that “*like the 315 Patent*, Li describes diffusing dopants at the front surface to form the front portion 520 (shown in red above) *with a ‘gaseous N-type dopant source.’*”⁶ Pet., 23. But the ’315 patent does not dope the front surface with a “gaseous N-type dopant

⁶ All emphasis added, unless otherwise noted.

source”; rather the ’315 patent discloses that “a dopant region 216 can be formed on a surface 204 of silicon substrate 202,” and a high-temperature heating step drives “the dopants 222 from the dopant region 216 to a portion 206 of the silicon substrate 202.” EX1001, 4:55-56, 5:64-67, FIGs. 2 and 3 (annotated below).

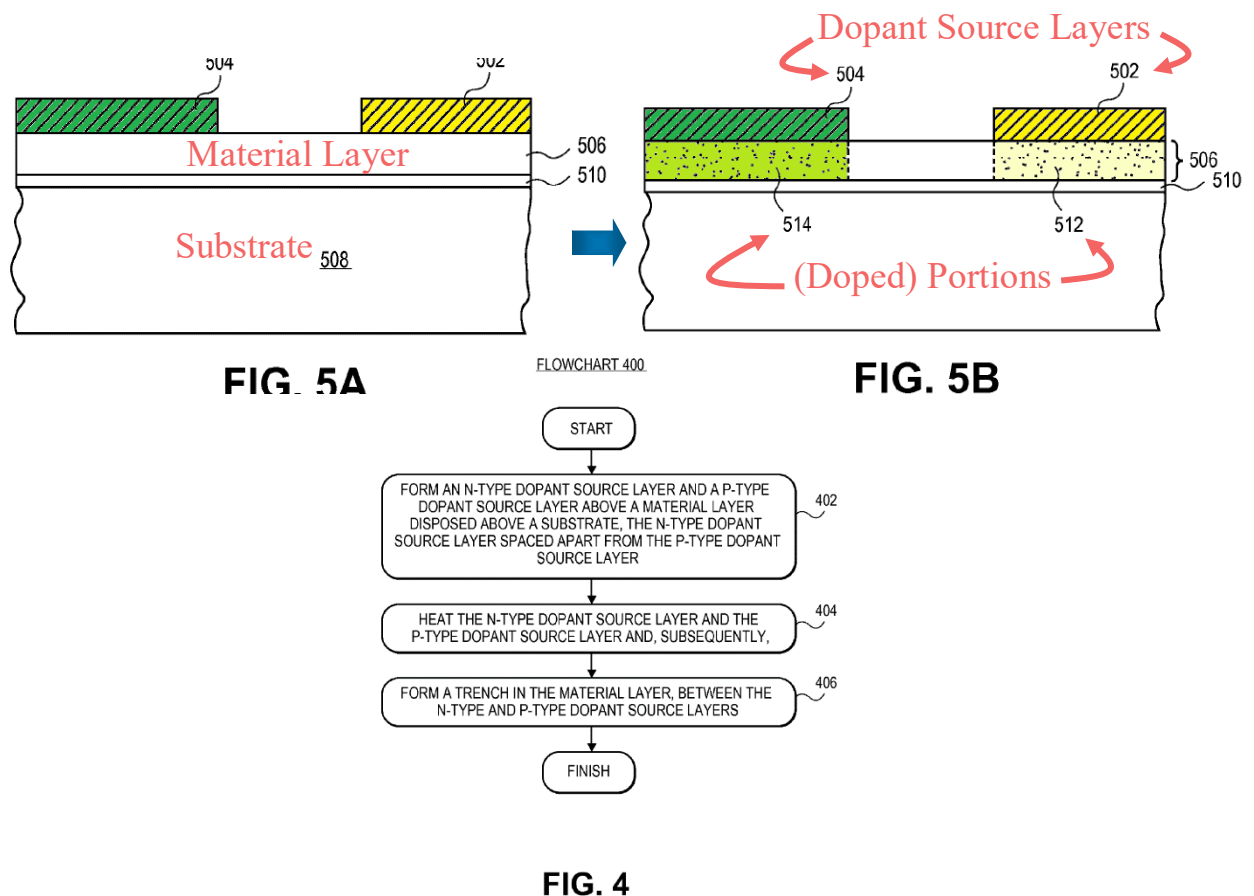


EX1001, FIGs. 2 and 3 (annotated).

68. Figure 3 shows the portion 206 that is doped by driving dopants 222 from the dopant region 216 in the silicon substrate 202. Accordingly, the ’315 patent is not “just like” Li because it does not disclose a “gaseous” (delivery of dopant) drive-in method.

69. **Different Heating Steps.** CSI and Dr. Banerjee also assert that the ’315 patent discloses that “heating the solar cell above 900°C can getter metal impurities into the emitter region and at the same time *perform dopant diffusion*,” and that “[i]n Li, dopant diffusion is conducted above 900°C, *just like in the 315 Patent*.” Pet., 46-47 (emphases added); See EX1003, ¶[172]. CSI and Dr. Banerjee

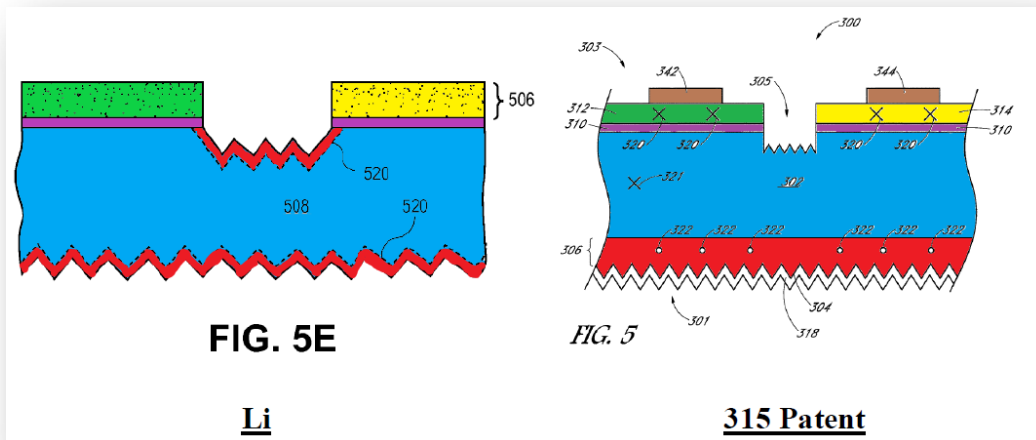
improperly conflate the high-temperature heating step that diffuses dopants into the front surface of the substrate in the '315 patent (discussed above) with Li's diffusing of dopants into the emitter regions on the back of the substrate 508. Li discloses that the high-temperature (950°C) dopant diffusion step occurs when portions 512 and 514 of Li's material layer 506 (e.g., the first and second emitter regions) are doped. *See* EX1005, ¶¶[0044]-[0045] (explaining that dopant source layers 502, 504 are heated to transfer dopants into portions 512, 514), FIG. 4 (operation 404 of flowchart 400), FIGs. 5A, 5B (annotated below).



EX1005, FIGs. 4, 5A, and 5B (annotated).

70. The high-temperature heating step in Li dopes the emitter regions, whereas the high-temperature heating step in the '315 patent dopes the silicon substrate. The “dopant regions 520” in Li, which CSI identifies as the doped portion of the silicon substrate 508, are not formed until several steps later by “heating substrate 508 . . . in the presence of a gaseous N-type dopant source.” EX1005, ¶[0049]. Thus, Li does not disclose “[performing] dopant diffusion . . . just like in the 315 Patent” because the high-temperature heating step is performed at different times and to drive dopants in at different regions. Pet., 47. These timing differences are significant because a Skilled Artisan would have understood the need to account for the thermal history of the substrate when implementing additional heating steps.

71. A comparison of Figure 5E in Li with Figure 5 of the '315 patent (annotated by CSI and Dr. Banerjee) confirms these differences between the dopant processes and heating steps of the '315 patent and Li. *See* Pet., 22 (reproduced below).



Pet., 21 (comparing EX1005, FIG. 5E (left) to EX1001, FIG. 5 (right)).

72. As can be seen, unlike the doped portion 306 of the '315 patent, dopant regions 520 in Li are on the front surface of the substrate 508 **and in the trench**, indicating that substrate doping occurred after the trench was formed, whereas the '315 patent has no doping in the trench indicating that doping occurred before the trench was formed. *See* Pet., 22 (figure comparison). Moreover, the profile of the dopant regions 520 in Li follows the textured surface profile indicating that doping was performed after texturing, unlike the '315 patent. *See* Pet., 22 (figure comparison). The doped portion 306 of the '315 patent also extends further into the silicon substrate 302 than the dopant regions 520 in Li, which is consistent with the high-temperature heating step for driving dopants into the silicon substrate disclosed by the '315 patent, and not the “gaseous” drive-in method disclosed by Li. *See* Pet., 22-23 (figure comparison).

73. Both CSI and Dr. Banerjee later concede that Li uses a “two-step heating approach for the back and front of the solar cell.” Pet., 53, n.9; EX1003, ¶[171]. But rather than admit that Li does not disclose a high-temperature heating step for doping the front side of the substrate, CSI and Dr. Banerjee incorrectly contend that “it would ... have been obvious to the Skilled Artisan to combine the two heating steps of Li into a single heating step for the doping of the front and back sides of the solar cell.” Pet., 53, n.9; EX1003, ¶[171]. Dr. Banerjee proposes “using a single loading of the solar cell into a single heating furnace after the deposition of the back side dopant sources onto the polysilicon layer and include the gaseous dopant for diffusion [sic] the front portion.” EX1003, ¶[171]. That is, Dr. Banerjee proposes introducing a gaseous dopant at the emitter doping stage shown in Figure 5B of Li. Immediately, Dr. Banerjee recognizes the problem that a gaseous phosphorus (i.e., n-type) dopant will cross-dope the p-type polysilicon region, so he further proposes depositing “a diffusion mask” on the backside of the substrate. EX1003, ¶[171]. But the purpose of Li’s invention is to avoid the “ledge” feature, “which may undesirably result from partial mask 210 lift-off 218 and/or undercut 220 of mask 206 during the etch process,” so re-introducing a mask over the same problematic region would not have been obvious. EX1005, ¶[0031].

B. Grounds 3 and 4: CSI and Dr. Banerjee do not show that the combination of Li with Hu and Ramappa teaches “a first emitter region having metal impurities” and “a second emitter region having metal impurities.”

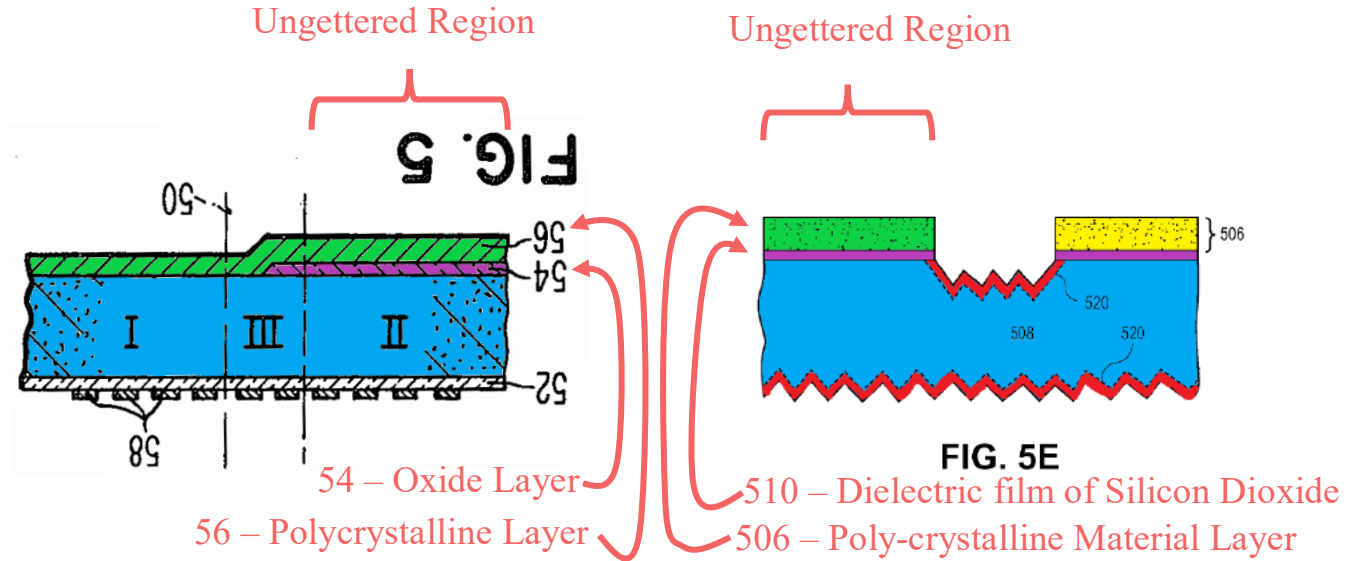
74. CSI and Dr. Banerjee contend that Li in view of Hu and Ramappa teaches claim 10’s “first emitter region having metal impurities” and claim 16’s “second emitter region having metal impurities.” Pet., 70-74; EX1003, ¶¶[231]-[241]. But CSI and Dr. Banerjee do not show the “first emitter region having metal impurities” when “formed over the dielectric region,” as required by claim 10. EX1001, 10:59-60. Neither do CSI and Dr. Banerjee show the “second emitter region having metal impurities” when “formed over the dielectric region,” as required by claim 16. EX1001, 11:6-7. The specification of the ’315 patent discloses that “heating at temperatures above 900 degrees Celsius can include gettering metal impurities 220 through the dielectric region 210, e.g., tunnel oxide, to into [sic] the emitter region 212, e.g., polysilicon regions.” EX1001, 5:21-24. A Skilled Artisan would not have combined the teachings of Hu and Ramappa with Li because, as explained below, these references do not teach “metal impurities” in the “emitter regions” formed over the “dielectric region” of Li.

1. Hu does not disclose gettering of metal impurities across an oxide layer into a polycrystalline layer.

75. CSI asserts that Hu teaches the “gettering of metal impurities from a silicon ‘semiconductor body’ into a ‘polycrystalline layer’ on the backside of the

silicon at temperatures of 1000°C or less.” Pet., 71. Similarly, Dr. Banerjee claims that Hu teaches “heating a ‘semiconductor ‘body’ and ‘polycrystalline layer’ at 1000°C or less, results in ‘getterable impurities... [diffusing] to, and becom[ing] trapped in, the polycrystalline silicon film.’” EX1003, ¶[235]. But neither CSI nor Dr. Banerjee addresses Hu’s explicit disclosure of a region where the polycrystalline layer is separated from the silicon by an oxide layer and gettering does not occur. EX1017, 8:39-44.

76. Figure 5 of Hu illustrates both “region I,” which has a polycrystalline layer 56 deposited on the backside of the silicon wafer 50, and “region II,” which has a backside oxide layer 54 formed between the silicon wafer 50 and the polycrystalline layer 56. EX1017, FIG. 5 (annotated, below left). Similarly, Li discloses dielectric film 510 in between the poly-crystalline material layer 506 and substrate 508. EX1005, FIG. 5E (annotated by CSI, below right).



EX1017, FIG. 5 (annotated).

EX1005, FIG. 5E (annotated).

77. Hu explains that “it was expected that gettering would take place in region I, but not in region II because of the presence of an intermediary oxide barrier.” See EX1017, 8:39-44. Table 1 of Hu confirmed that Region II between the backside oxide layer 54 and the semiconductor body 50 is “ungettered.”

EX1017, 9:47-54 (Table 1 annotated below).

TABLE I			
Column	Region	Mean Generation Current Nano Amp/cm ²	Remarks
1-4	II	108	ungettered
5-6	III	3.4	transition
7-10	I	1.7	region gettered

EX1017, 9:47-54 (annotated).

78. Accordingly, Hu does not disclose—rather, it teaches away from—gettering impurities into the polycrystalline layer formed over the oxide layer.

2. Ramappa does not disclose gettering metal impurities across an oxide layer into a polycrystalline layer.

79. Ramappa’s teachings directly contradict CSI’s and Dr. Banerjee’s claim that “[b]ased on Ramappa, it would be apparent to the Skilled Artisan that iron would readily diffuse across Li’s 1-2 nm silicon dioxide layer into both polysilicon emitter regions of Li.” Pet., 73-74; EX1003, ¶[239]. But Ramappa does not contemplate gettering or the diffusion of metal impurities from a silicon oxide layer into a polysilicon layer. *See generally* EX1025. Rather, as shown in Figure 1, Ramappa analyzes iron traveling from the SiO₂ layer into the silicon bulk, not out of the silicon bulk. *Compare* Ramappa, EX1025, FIG. 1 *with* Li, EX1005, FIG. 5E (annotated, below right). Applying this teaching to Li, as CSI and Dr. Banerjee propose, a Skilled Artisan would have understood that the diffusion of metal impurities in Li’s structure would be away from the poly-crystalline material layer

506.

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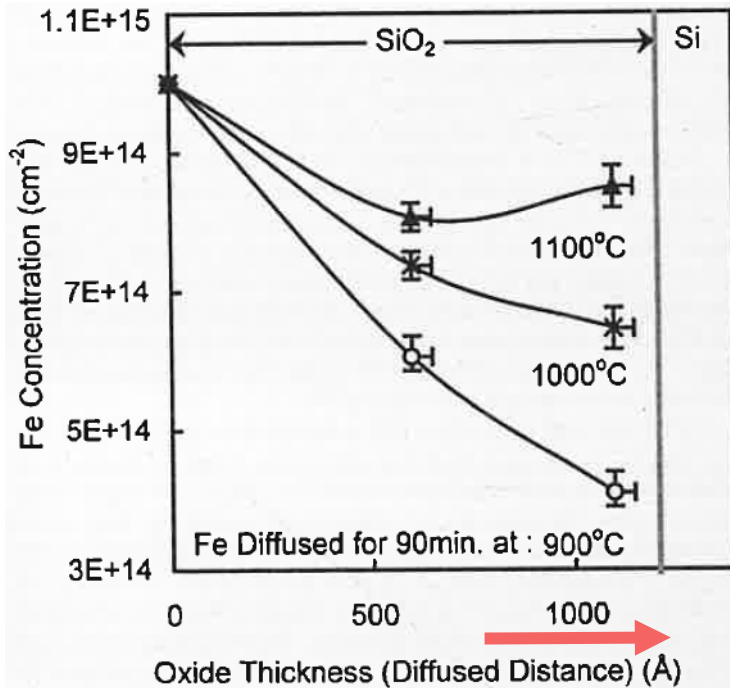


Figure 1. Iron concentration profile in SiO_2 following in-diffusion at temperatures of 900, 1000, and 1100°C for 90 min. Iron concentrations were measured by TXRF.

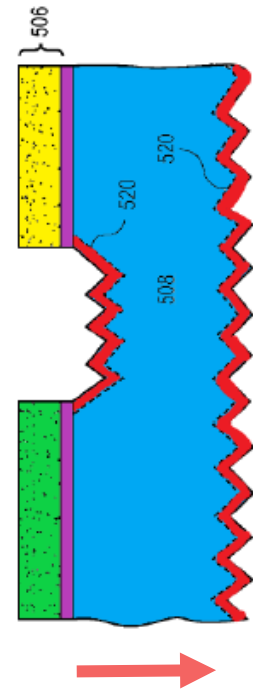


FIG. 5E

EX1025, FIG. 1 (annotated; left) and EX1005, FIG. 5E (annotated; right).

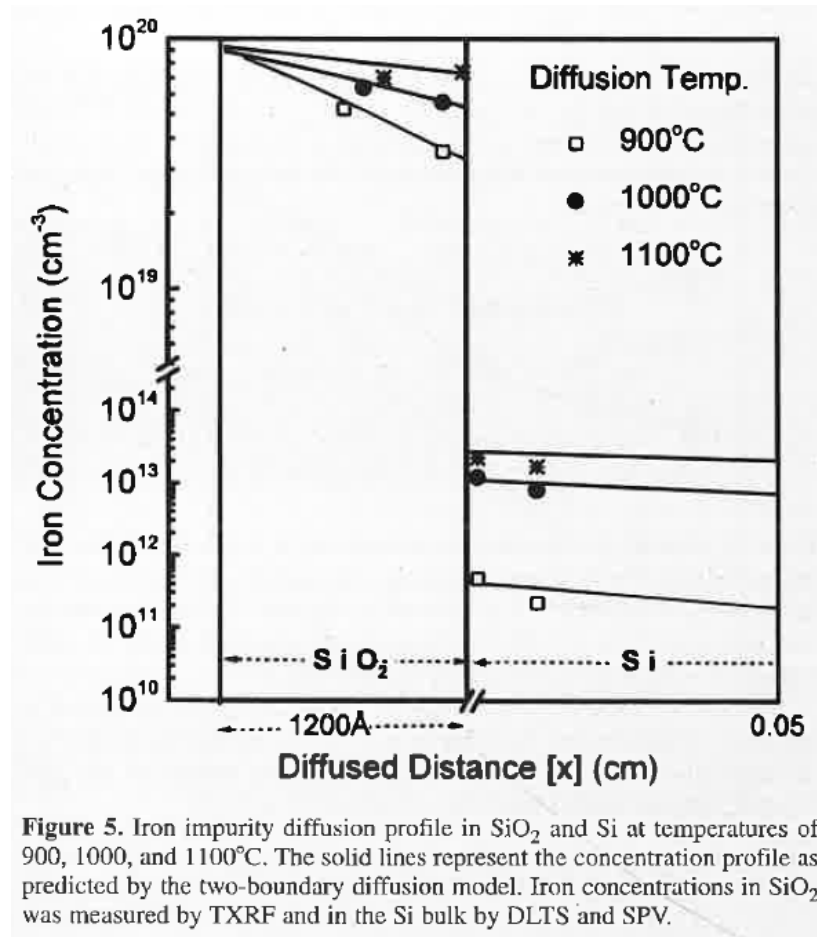
80. There is also no teaching in Ramappa about a silicon oxide layer acting as a tunnel oxide barrier layer between a substrate and a polysilicon material layer. The context and direction of diffusion studied in Ramappa are opposite from what is required for gettering metal impurities from Li's substrate 508 to the polycrystalline material layer 506. The findings in Ramappa suggest that the silicon oxide layer would act as a barrier, preventing such diffusion and thereby impeding any gettering process through this layer. Ramappa discloses that:

[I]t is observed that in agreement with previous published literature iron has a strong tendency to preferentially segregate to the SiO_2 side of the SiO_2 -Si interface. This strong segregation tendency seemingly **impedes**

the diffusion of iron from SiO_2 into the silicon bulk. In the process the segregation could lead to supersaturation of iron impurity and eventually precipitation which in turn could provide detrimental to the gate oxide integrity.

EX1025, 3776.

81. Ramappa discloses that silicon dioxide acts as an impurity sink and does not readily allow iron to pass from the silicon dioxide layer to the silicon bulk—as illustrated in Figure 5 (below).



EX1025, FIG. 5.

82. Figure 5 of Ramappa shows a starting iron concentration of 10^{20} cm^{-3} that drops to under 10^{12} cm^{-3} (8 orders of magnitude) when entering the silicon bulk at 900 degrees Celsius. Thus, a Skilled Artisan reading Ramappa would have concluded that the silicon dioxide layer 510 of Li would act as an impurity sink to metal impurities, instead of allowing metal impurities to be gettered into the polycrystalline material layer 506.

3. Hu and Ramappa taken together do not teach gettering metal impurities across an oxide layer into a polycrystalline layer.

83. Based on the teachings of Hu and Ramappa, a Skilled Artisan would not have found the presence of metal impurities in Li's polysilicon material layer 506 to be obvious. From the combination of Hu's structure and Ramappa's disclosure that "iron has a strong tendency to preferentially segregate to the SiO_2 side of the SiO_2 -Si interface . . . [, which] impedes the diffusion of iron from SiO_2 into the silicon bulk" (EX1025, 3776), a Skilled Artisan would have concluded that Region II in Hu is ungettered because of the oxide layer between the silicon and polysilicon layers. Thus, applying Hu's and Ramappa's teachings to Li's structure, a Skilled Artisan would have concluded that no metal impurities are gettered into Li's polysilicon material layer 506 due to the presence of Li's silicon dioxide film 510 between its substrate 508 and polysilicon material layer 506.

84. Moreover, CSI and Dr. Banerjee do not mention the oxide layer in Hu nor provide an explanation for Ramappa's express teaching that "[t]he SiO₂-Si interface is known to act as a sink for impurities." EX1025, 3775.

VI. ALL GROUNDS: CSI AND DR. BANERJEE DO NOT SHOW THAT IT WOULD HAVE BEEN OBVIOUS TO COMBINE LI WITH OTHER REFERENCES TO TEACH THE CLAIMED "DOPANT CONCENTRATION."

85. For Grounds 1 and 3, CSI and Dr. Banerjee rely on three references (King et al., "Studies of Diffused Phosphorous Emitters: Saturation Current, Surface Recombination Velocity, and Quantum Efficiency," IEEE Transactions On Electron Devices, Vol 37, No. 2 (Feb. 1990) ("King," EX1006); U.S. Patent No. 4,234,352, "Thermophotovoltaic Converter and Cell for Use Therein" ("Swanson-352," EX1015); and Marvin and Froedge, "Analysis of Interdigitated Back Contact Silicon Solar Cell Analysis and Design Recommendations for Space Use," IEEE (1989)AD-A220-414 (Sept. 30, 1989) AD-A220-414 (Sept. 30, 1989) ("Marvin," EX1035)), disclosing outdated and incompatible solar cell configurations that a Skilled Artisan would not have considered when determining a suitable dopant concentration for the portion of the silicon substrate at the front side of the solar cell in Li. Pet., 25-37; EX1003, ¶¶[111]-[134]. CSI and Dr. Banerjee do not account for the teachings of more recent references, such as Granek (EX2015), that show the use of higher dopant concentrations on the front surface of substrates to

eliminate the need for a thick oxide passivation layers, as in the solar cell configurations of King, Swanson-352, and Marvin.

86. For Grounds 2 and 4, based on the combination of Li and Muller et al., “Ion Implementation for All-Alumina IBC Solar Cells with Floating Emitter,” Energy Procedia 55 (2014), 265-271 (“Muller,” EX1008), CSI and Dr. Banerjee propose a new solar cell configuration that would not have been obvious absent CSI’s hindsight based on the ’315 patent. Pet., 59-67; EX1003, ¶¶[205]-[219]. In my opinion, the proposed solar cell would only have been achieved through hindsight as CSI and Dr. Banerjee propose significant modifications to Li’s solar cell—by adding ion-implanting steps, changing dopant polarities, adding new passivation layers, reversing fabrication order, and adding masking techniques—which contradicts Li’s goal of reducing the number of process operations.

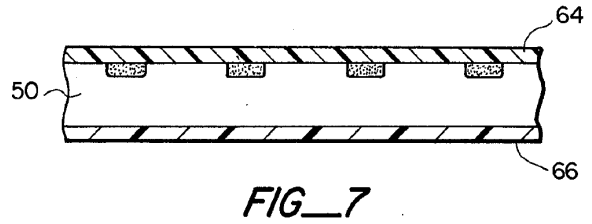
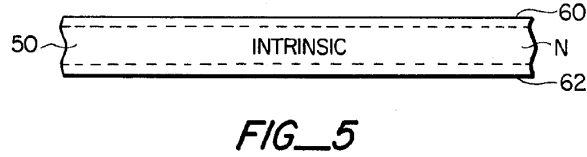
A. Grounds 1 and 3: A Skilled Artisan would not have been motivated to combine Li with King, Swanson-352, or Marvin.

87. CSI’s and Dr. Banerjee’s obviousness argument is contradicted by the prior art itself, which discloses different and conflicting dopant concentrations depending on various design parameters, such as the radiation environment, the thickness of the silicon oxide passivation layer, and the shape of the dopant profile. CSI and Dr. Banerjee also do not account for the teachings of more recent references, such as Granek, that show that higher dopant concentrations were used and preferred for back-contact solar cells with thin silicon oxide passivation layers.

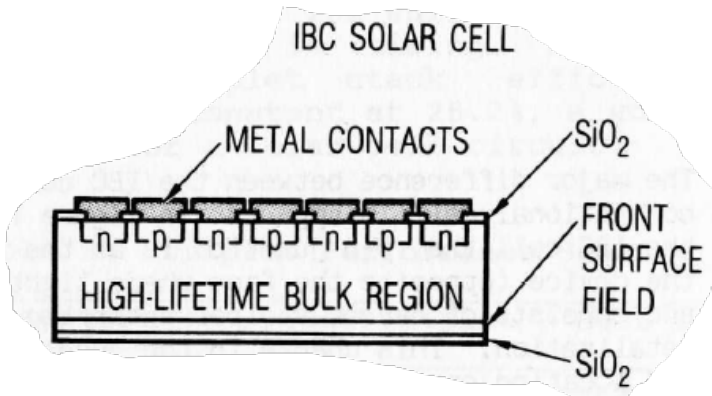
1. King, Swanson-352, and Marvin disclose a dopant concentration related to an outdated solar cell structure that would not have been obvious to combine with Li.

88. In the proposed combinations with Li, CSI and Dr. Banerjee do not explain why a Skilled Artisan would have found it obvious to look to the different solar cell configurations of King, Swanson-352, and Marvin for determining dopant concentrations in the front sides of solar cells. These solar cell structures are incompatible with Li.

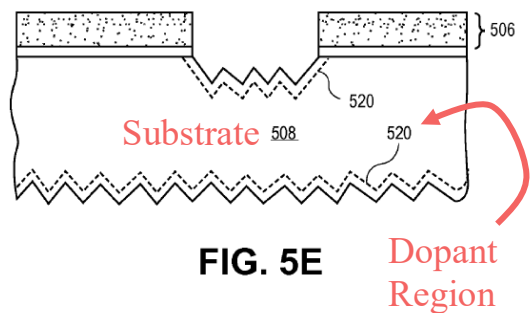
89. The disclosures in King, Swanson-352, and Marvin hearken back to an era when Interdigitated Back Contact (IBC) cells included thick silicon oxide passivation layers formed over both sides of the silicon substrate. *See* EX1006, 366 (explaining its experimental method included “lightly doped silicon substrate that has identical planer dopant diffusion with thermal oxide passivation on both sides of the wafer.”); EX1015, 4:45-61 (disclosing “[S]hallow diffused regions 60 and 62 are formed in the opposing surfaces of the wafer by the diffusion of an N type dopant . . . [and] silicon oxide layers 64 and 66 are then formed on the surfaces of substrate 50.”); EX1035, 822 (annotated figure below, left). Swanson-352 discloses that its silicon oxide layers were on the order of 175 nm thick. *See* EX1015, 4:61-66, FIGs. 5 and 7 (below). In contrast, Li does not disclose using a passivation oxide layer on the front side of its substrate 508. *See* EX1005, FIG. 5E (annotated below, right).



EX1015, FIGs. 5 and 7.



EX1035, FIG. 1.



EX1005, FIG. 5E (annotated).

90. CSI and Dr. Banerjee do not take into account the differences in the solar cell structures between Li and the cited references and do not explain how or whether the presence of the silicon oxide passivation layer in King, Swanson-352, and Marvin would affect doping concentrations, but Granek and Muller do.

91. Granek shows a correlation between the thickness of the silicon oxide passivation layer and the dopant concentration on the front side of the substrate. Granek analyzes similar solar cell performance characteristics as King did, and compares the results of “thin thermal oxides” (i.e., 2007 technology) against a “thick 105 nm antireflection oxide passivation” (i.e., 1990s technology in King, Swanson-352, and Marvin). See EX2015, 1-2. Granek plots dopant profiles for

different dopant concentrations using a thin 10 nm thermal oxide passivating layer (unfilled shapes $\square$, $\diamond$, $\triangle$, ∇) and one dopant profile for a thick 105 nm oxide passivation (filled shape $\bullet$). See EX2015, 2, FIG. 4 (annotated below).

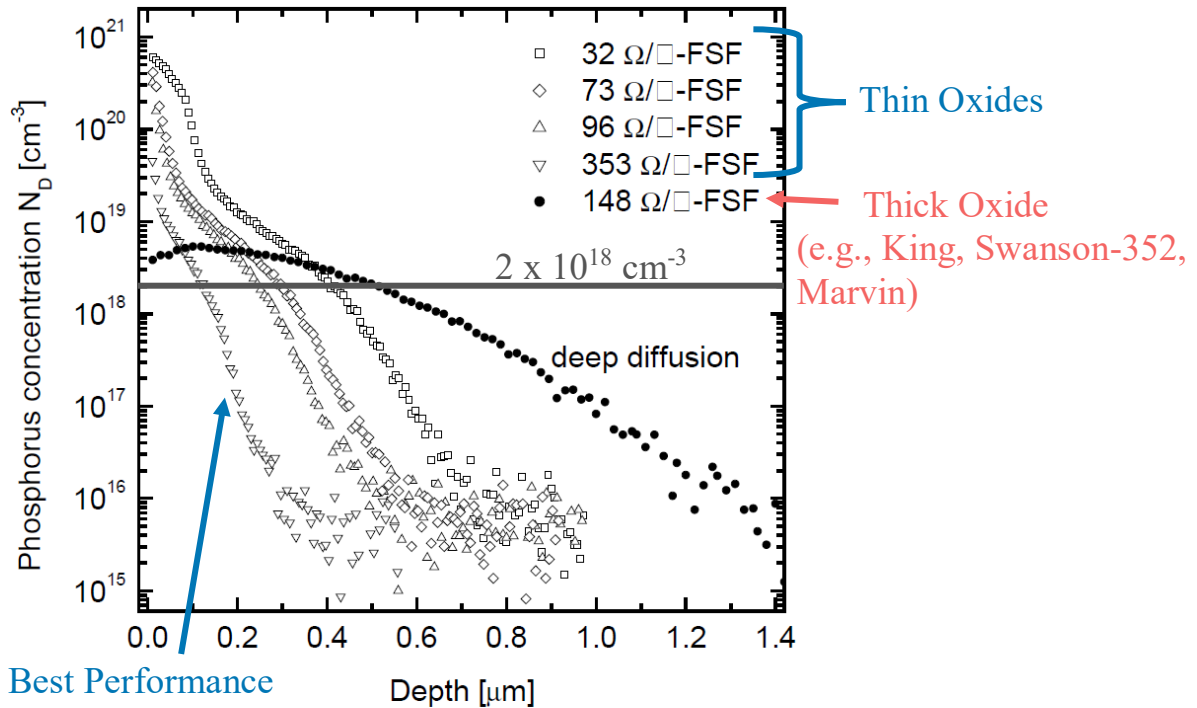


Figure 4: Secondary ion mass spectrometry (SIMS) profiles of the studied phosphorus dopant profiles measured for untextured samples after all high temperature processing steps. Sheet resistance FSF was calculated by integrating the dopant profiles using the mobility model from Masetti [9].

EX2015, FIG. 4 (annotated).

92. Granek confirmed that lower saturation current densities were possible using thin thermal oxide passivation layers and high surface dopant

concentrations rather than thick oxide passivation. *See* EX2015, 5 (Table II annotated below).

Table II. Summary of the results for the textured samples with different front surface field diffusions.

		$\rho_{base} = 1 \Omega \text{ cm}$		$\rho_{base} = 10 \Omega \text{ cm}$	
		low-level-injection		high-level-injection	
n^+ diffusion		J_{0s}	$V_{OC, Limit}$	J_{0s}	$V_{OC, Limit}$
[$\Omega/\text{sq.}$]		[fA/cm ²]	[mV]	[fA/cm ²]	[mV]
Thin Oxides	32	1170	615	1180	615
	73	290	651	296	651
	96	138	671	161	667
	353	31	710	36	706
	148 (deep)	38	705	40	703
no diffusion		27	714	31	710

Thick Oxide (e.g., King, Swanson-352, Marvin)

EX2015, Table II (annotated).

93. Accordingly, Granek's proposed dopant concentration for producing a front surface field was much higher than Swanson-352 and required a different thickness of oxide passivation layer to be used. At a minimum, Granek proves that "front surface doping concentration" is dependent on the thickness of the front side oxide passivation layer and that it was not settled in 1990. Moreover, Muller shows adopting thin silicon oxide layers with "quite strong doping on the front side" that created a front surface field capable of suppressing UV-illumination degradation and improving long term UV-stability of the passivation. EX1008, 267-70 (~10 nm thick thermal oxide used in experimentation); EX2015, 3 (same).

94. In my opinion, a Skilled Artisan would not have found it obvious to adopt design parameters for solar cell structures from the 1990s (such as those solar cell structures disclosed by King, Swanson-352, and Marvin) that are no longer in use. Moreover, in my opinion, it would not have been obvious to a Skilled Artisan to adopt King, Swanson, and Marvin's front surface doping concentrations that are tied to front side oxide passivation layers, where Li does not disclose such a layer. Neither CSI nor Dr. Banerjee addresses these significant technical differences and show why it would have been obvious to modify Li's solar cell configuration based on the incompatible solar cell teachings of King, Swanson-352, and Marvin.

2. King, Swanson-352, and/or Marvin do not disclose an “optimum” dopant concentration.

95. CSI's statement that “[b]y December 22, 2014, it had been known for decades that the front portion formed in the silicon substrate of a back-contact solar cell should be optimally doped at a concentration of approximately $2 \times 10^{18} \text{ cm}^{-3}$ or less” is incorrect. Pet., 17-18. Dr. Banerjee also makes a similar incorrect statement. EX1003; ¶[76]. Marvin contradicts both CSI's and Dr. Banerjee's positions, disclosing two different doping concentrations based on a solar radiation environment. *See* EX1035, 826-27 (recommending a doping concentration of $5 \times 10^{18} \text{ cm}^{-3}$ for terrestrial environments and $1 \times 10^{18} \text{ cm}^{-3}$ for high-radiation environments). CSI and Dr. Banerjee select a front surface doping

recommendation of $1 \times 10^{18} \text{ cm}^{-3}$ for a solar cell intended for use in space (i.e., a high-radiation environment) and asserts that “Marvin’s focus on high radiation environments, such as space, would not have deterred the Skilled Artisan from combining with Li because Li does not limit its back-contact solar cell to low radiation or terrestrial environments.” Pet., 35; EX1003, ¶[130]. But, in my opinion, an “optimum” dopant concentration will vary based on design parameters. See EX1035, 827 (“The light intensity to be used and the radiation environment affect the [Interdigitated Back Contact cell] design to a greater extent than in conventional cells.”).

96. Similarly, Swanson-352 discloses a photovoltaic cell designed for use in a high-radiation environment:

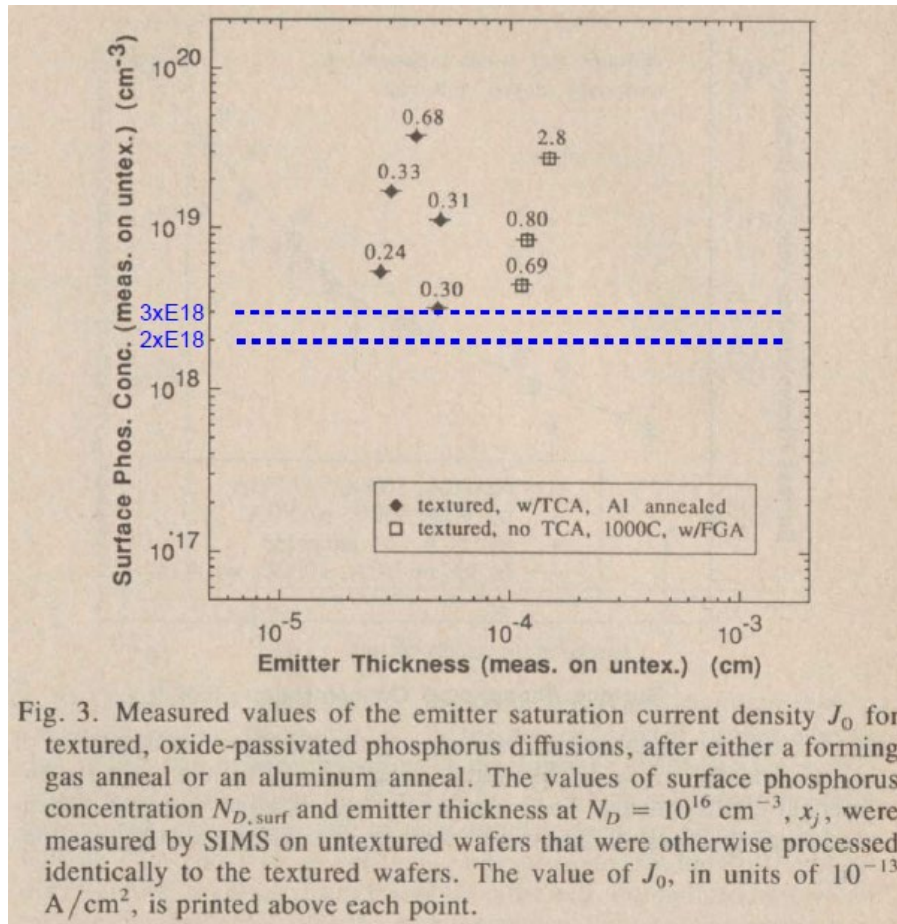
The means for receiving *concentrated radiation* includes a housing having a radiation receiving window, a secondary concentrator defined by walls of the housing within the window, and a chamber for confining the concentrated radiation. A radiator element may be positioned within the chamber for receiving the concentrated radiation, and the photovoltaic cell is positioned within the chamber in close proximity to the radiator element for receiving radiated energy from the radiator.

EX1015, 2:13-22.

97. Thus, like Marvin, Swanson-352’s disclosure of a “surface dopant concentration” of $1 \times 10^{18} \text{ cm}^{-3}$ is indicative of the structure and radiation

environment of that *particular* solar cell and not an “optimum” doping concentration for any solar cell. EX1015, 4:49-51. CSI and Dr. Banerjee do not address that Swanson-352 is designed as a concentrator solar cell and do not explain why a Skilled Artisan would have looked to a solar cell designed for a high-radiation environment to determine an “optimum” dopant concentration in Li.

98. Finally, King’s conjecture about a surface dopant concentration of $1 \times 10^{18} \text{ cm}^{-3}$ of a passivated emitter being “probably near optimum in [saturation current density] J_0 when [the solar cell] has a textured front surface” appears to be either highly approximated or aspirational. EX1006, 369. Figure 3 of King does not show any samples near that dopant concentration. *See* EX1006, FIG. 3 (annotated in blue below).



EX1006, FIG. 3 (annotated).

99. Moreover, neither CSI nor Dr. Banerjee addresses the disparity of dopant concentrations disclosed in Marvin ($5 \times 10^{18} \text{ cm}^{-3}$ for terrestrial (i.e., one sun) environment) and King, especially in light of the fact that King was also analyzing a one sun environment. *See* EX1006, 369. In my opinion, a Skilled Artisan, reading King as a whole, would not have found it obvious to set an upper limit of dopant concentration for a surface of the substrate where no dopant concentration in King was below that limit.

B. Grounds 2 and 4: A Skilled Artisan would not have been motivated to combine Li with Muller.

100. CSI's and Dr. Banerjee's proposed combination of Li and Muller creates an entirely new solar cell, which would not have been obvious to create without the benefit of hindsight in view of the '315 patent. Li only discloses doping the front surface of the substrate by heating substrate 508 "in the presence of a gaseous N-type dopant source." *See* EX1005, ¶[0049]. In contrast, Muller does not use a gaseous drive-in method, but ion-implanting to achieve "very lowly doped" front surface regions on *n*-type IBC solar cells. EX1008, 266.

101. When Muller used an N-type dopant source (e.g., phosphorus) as disclosed in Li to create a front surface field (FSF) profile, it was found that the "[c]ells with FSF degraded strongly under UV-illumination due to the instable SiO₂ passivation on the front side." EX1008, 265. The degradation was severe, in which "[t]he efficiency of FSF cells dropped dramatically by more than 50%." EX1008, 271. Muller, however, noted that "[t]he degradation of the cells investigated by Granek *et al.* was efficiently suppressed by using a quite strong doping on the front side." EX1008, 269. Thus, a Skilled Artisan, looking to determine the specific dopant concentration to use for the front-side **N-type** dopant region 520 disclosed in Li, would have concluded from Muller that using an extremely weak doping concentration (i.e., $< 2 \times 10^{18} \text{ cm}^{-3}$) would fail and that a "quite strong doping" should be considered. EX1008, 269. In my opinion, a Skilled

Artisan would have understood that Muller teaches away from using a low doping concentration for the front-side N-type dopant region 520 in Li.

102. Without a suitable dopant concentration for the front-side N-type dopant region 520 in Li, CSI proposes to significantly modify Li's solar cell to replace Li's diffused front-side N-type dopant region 520 with Muller's floating front emitter ("FFE"). As Muller discloses ion implanting the front surface region with a **P-type** dopant source (e.g., boron) to create the FFE (EX1008, 265), CSI and Dr. Banerjee propose "insert[ing] Muller's ion-implanted boron FFE process steps for the front side" of Li's solar cell (Pet., 67; EX1003, ¶[217]). This would involve the following additional processing steps:

- Adding an ion-implanting process (Pet., 63);
- Changing the polarity of the n-type doped portion 520 formed by a gaseous dopant process disclosed by Li and replacing it with a p-type doped portion formed by ion-implanting boron (Pet., 63; EX1003, ¶[210]);
- Adding "aluminum oxide and silicon nitride passivation" layers not disclosed by Li (Pet., 63; EX1003, ¶[210]);
- Reversing the order of fabrication disclosed by Li to ion-implant the front dopant regions first, instead of last (Pet., 67; EX1003, ¶[217]); and
- Masking the backside to diffuse the trench region (Pet., 67; EX1003, ¶[217]).

103. It is evident that CSI's and Dr. Banerjee's proposed combination of Li and Muller creates an entirely new solar cell, which would not have been obvious to create without the benefit of hindsight in view of the '315 patent. Moreover, in my opinion, it would not have been obvious to combine Li and Muller because the proposed modification of Li's fabrication process increases the number of processing steps, which expressly contradicts Li's objective to achieve "a reduction in the sheer number of process operations." EX1005, ¶[0024].

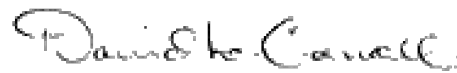
VII. CONCLUSION

104. I understand that this Declaration is to be filed as evidence in a contested IPR proceeding before the Patent Trial and Appeal Board. I acknowledge that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

105. I hereby declare under penalty of perjury that the foregoing is true and correct, that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and may jeopardize the validity of the application or any patent issuing thereon. If called to testify as to the truth of the matters stated herein, I could and would testify competently.

Respectfully submitted,

Dated: October 29, 2024



David L. Carroll, Ph.D.