

A Polysilicon Emitter Solar Cell

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Abstract—A new solar cell structure is reported in which the emitter consists of a thin layer of *in situ* phosphorus-doped polysilicon deposited by a low-pressure chemical vapor deposition (LPCVD) technique. The highest process temperature required to fabricate this structure is only 627°C. Although the use of a polysilicon emitter results in some degradation in blue response, both theoretical and experimental results are presented indicating that photocurrent densities in excess of 30 mA·cm⁻² are attainable under AM1 illumination. The low back-injection current associated with the polysilicon emitter has allowed a very high open circuit voltage of 652 mV to be obtained at 28°C in a cell illuminated to give a short circuit current density of 30 mA·cm⁻².

I. INTRODUCTION

IT HAS been known for over a decade that polysilicon emitter contacts can reduce the back-injection current and thereby improve the performance of bipolar transistors [1]. It is, therefore, somewhat surprising that consideration has only recently been given to the use of polysilicon contacts in the production of high-efficiency solar cells. The first suggestion that polysilicon might be used to advantage as a contact grid material appears to have been made by Van Overstraeten [2]. This idea was explored experimentally by Green and Blakers, who reported briefly on the enhancement in open-circuit voltage provided by the use of polysilicon contacts in an MINP structure [3]. Closely related research into the use of semi-insulating polysilicon (SIPOS) as a solar cell contact material has been carried out by Yablonovitch, Swanson, and Kwark [4]. Very recently, Lindholm, Neugroschel, Arienzo, and Iles demonstrated that both n⁺ and p⁺ polysilicon layers could function as efficient back surface field regions [5]. This letter reports on a solar cell structure in which a thin, continuous layer of *in situ* doped polysilicon actually forms the entire emitter region, rather than simply serving as a contact.

II. DEVICE FABRICATION

The solar cells were fabricated on 5-cm diam silicon wafers of (100) orientation obtained from three different vendors. A 2 × 2-cm cell and a variety of smaller test diodes were placed on each wafer. To provide some degree of surface passivation, the wafers were first coated with 250 nm of SiO₂ deposited by low-temperature techniques. After device wells were opened in this oxide, the wafers were RCA cleaned, briefly etched in 10 percent HF, and then spun dry and loaded into a low-pressure chemical vapor deposition (LPCVD) reactor as rapidly as possible to minimize growth of an interfacial native

oxide layer. The emitter deposition was carried out from a 300/1 silane/phosphine mixture at a temperature of 627°C and a pressure of 0.3 torr. Polysilicon thicknesses of 50 and 80 nm were examined. It should be stressed that no high-temperature anneal was carried out after this deposition, so the highest temperature to which the wafers were exposed in the process sequence was 627°C. The resistivity of the polysilicon film was estimated to lie in the range 0.01–0.02 Ω·cm.

Contacts to the cells were made with aluminum. The back contact was annealed at 450°C in a hydrogen ambient. The 1-μm thick front contact grid was deposited by thermal evaporation and given no annealing treatment, for the annealing of Al contacts to polysilicon/silicon junctions has been found to lead to drastic degradation in device characteristics. The grid consisted of a central busbar collecting current from nominally 18-μm wide fingers with centers spaced 317-μm apart. Some scatter in finger width from cell to cell resulting from variations in etching conditions was noted. The busbar itself was tapered linearly from a width of 500 to 100 μm. The grid finger coverage was 6 percent, and the busbar coverage 1.6 percent.

III. TEST RESULTS

The short-circuit photocurrent of the polysilicon emitter cells was first measured in natural sunlight in Ottawa with the sun at approximately 30° from the zenith. Under these test conditions a 2 × 2 cm back-surface field-space cell manufactured by Applied Solar Energy Corporation (ASEC) gave a short circuit current within 2 percent of its AM1 rating. Later, an antireflection coating consisting of 700 Å of thermally evaporated SiO was applied to three of the cells, and the photocurrent density was remeasured under ELH lamp illumination. The lamp intensity was adjusted to give the rated AM1 photocurrent in the ASEC cell. Results of these measurements are presented in Table I. Measurements of open-circuit voltage and fill factor were made at a controlled temperature of 28°C with the incident light intensity to produce a photocurrent density of 30 mA·cm⁻² in each device; results are given in Table II.

Previous work has established that it is possible to form high-quality n⁺p junctions by the deposition of heavily *in situ* doped polysilicon on monocrystalline substrates [12]. Confirmation of these findings is provided by Fig. 2, which presents the dark *J-V* characteristics for a small-area diode fabricated following the procedure outlined above. The diode law is obeyed with an "ideality factor" *n* of approximately 1.1 over nearly seven decades of current. At high-current densities, resistive effects which may be associated with the tunneling of carriers across the polysilicon-silicon junction are observed,

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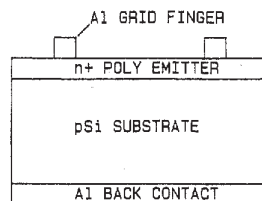


Fig. 1. Structure of the polysilicon emitter cell.

TABLE I
TOTAL-AREA SHORT-CIRCUIT CURRENT DENSITY FOR 2×2 cm
POLYSILICON EMITTER CELLS. $J_{sc,1}$ WAS MEASURED ON UNCOATED
CELLS IN NATURAL SUNLIGHT; $J_{sc,2}$ WAS MEASURED UNDER ELH LAMP
ILLUMINATION AFTER THE APPLICATION OF AN SiO ANTIREFLECTION
COATING; THE LAMP-INTENSITY WAS SET TO SIMULATE AM1
CONDITIONS

Cell #:	Substrate:	Polysilicon Thickness:	$J_{sc,1}$:	$J_{sc,2}$:
1	Semimetals 1.8 - 2.6 μcm	80nm	22.5 mAcm^{-2}	30.5 mAcm^{-2}
2	" "	50nm	22.2	—
3	Monsanto 1.5 - 2.5 μcm	80nm	22.2	—
4	" "	50nm	22.0	30.2
5	Wacker Float Zone 0.1 μcm	80nm	20.0	28.5

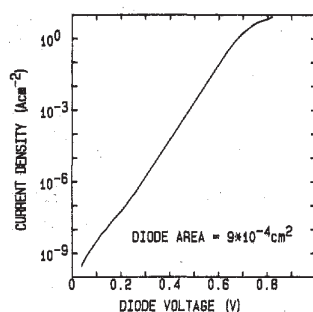


Fig. 2. Dark current-voltage characteristics for a small-area polysilicon-silicon diode.

but these should not interfere with solar cells operating in unconcentrated sunlight.

IV. DISCUSSION

At first inspection, it might be thought that the incorporation of polysilicon in the emitter region of a solar cell would lead to a sharp degradation in short-wavelength response, since minority carriers photogenerated in the polysilicon are likely to recombine before they can reach the junction and contribute to the photocurrent. In fact, theoretical calculations summarized in Fig. 3 reveal that for a polysilicon emitter thickness of 50 nm, the maximum available AM1.5 photocurrent is reduced by less than 5 percent, while for an emitter thickness of 100 nm the photocurrent loss is only 8 percent. Fig. 3 was produced using a model in which all carriers generated in the polysilicon emitter recombine before reaching the junction, while all carriers generated in the monocrystalline base are collected. A perfect antireflection coating and a quantum efficiency of unity are assumed. Data on the AM1.5 spectral

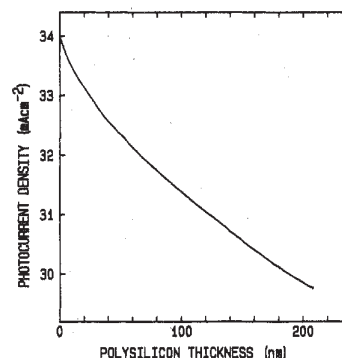


Fig. 3. Maximum available AM1.5 photocurrent as a function of polysilicon emitter thickness. Assumptions made are a perfect antireflection coating, a quantum efficiency of unity, a substrate thickness of 300 μm , complete collection of carriers photogenerated in the monocrystalline base, and complete loss of carriers generated in the emitter.

composition and the absorption coefficient of silicon were both obtained from [6]. The substrate thickness was taken as 300 μm . Fig. 3 actually provides a worst-case estimate for the photocurrent loss expected when using a polysilicon emitter, since there is some evidence that minority carrier holes can diffuse across a thin polysilicon layer [7]. The J_{sc} data presented in Table II support the contention that the photocurrent loss associated with a polysilicon emitter is not severe, in that AM1 current densities in excess of 30 $\text{mA} \cdot \text{cm}^{-2}$ have been obtained for cells equipped with primitive single-layer SiO antireflection coatings formed on substrates of indifferent quality.

The main motivation in using a polysilicon emitter in a solar cell is to exploit the reduced back-injection current this structure provides in order to achieve a high open-circuit

voltage. In polysilicon emitter transistors fabricated with the same basic process used here, a base-emitter bias of approximately 700 mV must be applied to give a base current density of $30 \text{ mA} \cdot \text{cm}^{-2}$ [8]. Assuming that I_B is dominated entirely by back injection into the polysilicon emitter, this suggests that the limiting open-circuit voltage of a polysilicon emitter solar cell is approximately 700 mV. To achieve such a high V_{oc} it would, of course, be necessary to completely eliminate recombination in the monocrystalline substrate and at the back contact. Previously reported high V_{oc} cells have made use of high-quality float-zone refined silicon with resistivities in the range $0.1\text{--}0.3 \Omega \cdot \text{cm}$. One such wafer was included in the present fabrication run, and gave a V_{oc} of 652 mV at 28°C with $J_{sc} = 30 \text{ mA} \cdot \text{cm}^{-2}$ (see Table II). This high open-circuit voltage compares favorably with the record values obtained by Blakers *et al.* using MIS tunnel junction contacts in an MINP structure [9]. The highest V_{oc} reported by Blakers *et al.* [9] under AM1 illumination at 28°C is 655 mV, although V_{oc} 's of up to 694 mV have been recorded by this group for similar cells under AM0 illumination at 25°C . As discussed at greater length elsewhere [8], it seems quite probable that the low back-injection current obtained in the polysilicon emitter structure results from a quantum reflection mechanism similar to that operating in the MIS tunnel junction contacts of the MINP cells.

The minimum resistivity obtainable in an as-deposited *in situ* phosphorus-doped LPCVD polysilicon LPCVD polysilicon is approximately $0.01 \Omega \cdot \text{cm}$. In consequence, the sheet resistance of a 50-nm thick polysilicon emitter is approximately $2 \text{ k}\Omega/\square$. Although this sheet resistance value is high, it should not preclude the attainment of reasonable fill factors in polysilicon emitter cells with properly designed contact grids. Fill factors of 0.78 have been obtained for inversion layer cells [10], even though in these devices the electron density in the "emitter" is unlikely to exceed 10^{12} cm^{-2} , corresponding to a sheet resistance in the $5\text{--}10 \text{ k}\Omega/\square$ range. Indeed, the original "violet cell" had an emitter sheet resistance of approximately $1 \text{ k}\Omega/\square$, yet provided a fill factor of 0.8 [11]. It should be possible to reduce the resistivity of a polysilicon emitter approximately an order of magnitude by annealing at a temperature of 900°C , in which case the emitter sheet resistance would have a negligible effect on the cell fill factor. However, it is not yet clear whether exposure to temperatures in this range will degrade the minority carrier reflecting properties of the polysilicon contact. In general, optimization of the efficiency of a polysilicon emitter cell requires that a compromise be made between the loss of blue response encountered with a thick polysilicon layer, and the high series resistance associated with a thin layer.

Examination of Table II reveals that the fill factors of this first group of polysilicon emitter cells are rather poor. This can be attributed entirely to an inadequate busbar metal thickness, giving a parasitic series resistance of approximately 1Ω . In comparison, the parasitic resistance associated with the grid fingers and the polysilicon emitter itself was estimated as being roughly 0.2Ω . Fill factors as high as 0.7 were obtained for cells with areas on the order of a square millimeter, adding further support to this interpretation.

TABLE II
OPEN-CIRCUIT VOLTAGE V_{oc} AND FILL FACTOR FF FOR CELLS OF TABLE I WHEN ILLUMINATED TO GIVE A PHOTOCURRENT DENSITY OF $30 \text{ mA} \cdot \text{cm}^{-2}$ AT A CONTROLLED TEMPERATURE OF 28°C

Cell #:	V_{oc} :	FF:
1	584 mV	0.622
2	582	0.614
3	583	0.611
4	583	0.614
5	652	0.605

In the introduction several references which dealt with the prospect of forming a high-efficiency solar cell by using a polysilicon grid to contact a shallow diffused or ion-implanted junction were cited. Such a structure should in principle allow the high open-circuit voltages characteristic of polysilicon contacts to be combined with the enhanced blue responses provided by shallow, oxide-passivated monocrystalline emitters. However, fabrication of such a cell would require exposure of the substrates to temperatures in the range $850\text{--}900^\circ\text{C}$. Although such temperatures are low by the standards of integrated circuit processing, they might still lead to some degradation in the minority carrier lifetime of high-quality material. In contrast, the simple polysilicon emitter structure described here can be formed without raising the substrate temperature above 630°C , and requires no critical diffusion or implant anneal steps.

V. CONCLUSION

It has been shown that thin *in situ* doped polysilicon layers hold considerable promise in forming the emitter regions of silicon solar cells. Although the use of a polysilicon emitter inevitably leads to some degradation in blue response, if the polysilicon thickness is kept below 50 nm theoretical calculations indicate that the AM1.5 photocurrent should not be reduced by more than 5 percent. Experimental results support this prediction, in that total-area photocurrent densities of over $30 \text{ mA} \cdot \text{cm}^{-2}$ have been recorded under simulated AM1 illumination in polysilicon emitter cells with simple SiO_2 antireflection coatings. As expected, the polysilicon emitter has proven effective in reducing the back injection component of the dark current, enabling an open circuit voltage of 652 mV to be obtained under simulated AM1 conditions for a cell formed on a high-quality $0.1 \Omega \cdot \text{cm}$ float-zone substrate. This last result supports recent suggestions that the use of a polysilicon contact grid should enhance the open-circuit voltages of more conventional cells with shallow, diffused, or implanted emitters.

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REFERENCES

- [1] P. Ashburn and B. Soerwirdjo, "Comparison of experimental and theoretical results on polysilicon emitter bipolar transistors," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 853-859, 1984.

- [2] R. J. Van Overstraeten, "Advances in silicon solar cell processing," in *Proc. 15th IEEE Photovoltaic Spec. Conf.* New York: IEEE, 1981, pp. 372-375.
- [3] M. A. Green and A. W. Blakers, "Advantages of metal-insulator-semiconductor structures for silicon solar cells," *Solar Cells*, vol. 8, pp. 3-16, 1983.
- [4] E. Yablonovitch, R. M. Swanson, and Y. H. Kwark, "An n-SIPOS:pSIPOS Homojunction and a SIPOS-Si-SIPOS Double Heterostructure," in *Proc. 17th IEEE Photovoltaic Spec. Conf.*, New York: IEEE, 1984, pp. 1146-1148.
- [5] F. A. Lindholm, A. Neugroschel, M. Arienzo, and P. A. Iles, "Heavily doped polysilicon contact solar cells," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 363-365, 1985.
- [6] M. A. Green, *Solar Cells: Operating Principles, Technology and System Applications*. Englewood Cliffs, NJ: Prentice Hall, 1982.
- [7] P. M. Solomon, D. D. Tang and R. D. Isaac, "A polysilicon base bipolar transistor," in *1979 IEDM Tech. Digest*, New York: IEEE, 1979, pp. 510-514.
- [8] M. B. Rowlandson and N. G. Tarr, "A true polysilicon emitter transistor," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 288-290, 1985.
- [9] A. W. Blakers, M. A. Green, S. Jiquin, E. M. Keller, S. R. Wenham, R. B. Godfrey, T. Szpitalak, and M. R. Willison, "18% efficient terrestrial silicon solar cells," *IEEE Electron Device Lett.*, vol. EDL-5, pp. 12-23, 1984.
- [10] R. B. Godfrey and M. A. Green, "655 mV open-circuit voltage, 17.6% efficient silicon MIS solar cells," *Appl. Phys. Lett.*, vol. 34, pp. 790-793, 1979.
- [11] J. Lindmayer and J. F. Allison, "The violet cell: An improved silicon solar cell," *Comsat Tech. Rev.*, vol. 3, pp. 1-6, 1973.
- [12] Z. Lieblich and A. Bar-Lev, "A polysilicon-silicon n-p junction," *IEEE Trans. Electron Devices*, vol. ED-24, pp. 1025-1031, 1977.