

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HANWHA SOLUTIONS CORPORATION,

Petitioner,

v.

MAXEON SOLAR PTE. LTD.,

Patent Owner.

Case No. IPR2024-01198

U.S. Patent No. 11,251,315

**DECLARATION OF DR. ZACHARY HOLMAN REGARDING
CLAIMS 10-20 OF U.S. PATENT NO. 11,251,315**

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I, Zachary Charles Holman, Ph.D., declare as follows:

I. INTRODUCTION

1. My name is Zachary Charles Holman.

2. I am making this declaration at the request of Hanwha Solutions Corporation (“HSC” or “Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office and to provide testimony pertinent to HSC’s Petition for *Inter Partes* Review of U.S. Patent No. 11,251,315 (“’315 patent”). I understand that Petitioner is challenging the patentability of claims 10-20 of the ’315 patent (“Challenged Claims”).

II. QUALIFICATIONS AND EXPERIENCE

3. I have been involved in the field of solar cell technology for over 19 years. My qualifications for forming the opinions set forth in this declaration are summarized below. Attached as **Appendix A** is my curriculum vitae, which describes my education, experience, and professional activities and lists, among other things, my publications and patents.

4. I received a Bachelor of Arts in Physics from Reed College in 2005. While pursuing my undergraduate degree, I researched the movement of electrons in semiconductor materials used for solar cells. My research was summarized in my undergraduate thesis, which was titled *Electron Transport in Amorphous Silicon*. My thesis explained how “[m]any mechanisms reduce the output of a solar cell

including imperfect incident light absorption, recombination of charge carriers, and poor charge transport through the cells,” and it described research that I conducted using time-of-flight measurement techniques to characterize electron transport in hydrogenated amorphous silicon. *See* Ex.1018-Holman-Thesis, 2-4. My thesis revealed trapping of electrons in defect states in amorphous silicon, which inhibited their collection at metal contacts. *See generally*, Ex.1018-Holman-Thesis.

5. I received a Doctor of Philosophy (“Ph.D.”) in Mechanical Engineering from the University of Minnesota in 2010. I started my Ph.D. program in September 2005. For the entire duration of my Ph.D., my research focused on the design, manufacture, and characterization of materials and layers used in solar cells. My Ph.D. thesis was titled *Germanium Nanocrystal Solar Cells*, and it described the use of thin films of plasma-synthesized germanium and silicon nanocrystals and their use in novel solar cells.

6. I co-authored multiple academic papers in the fields of semiconductor materials and solar cell technology while I was working on my Ph.D., including: A. LaLonde, Z Holman, et al., “Metal Coatings on SiC Nanowires by Plasma-enhanced Chemical Vapor Deposition,” *Journal of Material Research* **20**, 549 (2005) (describing method for coating silicon carbide nanowires with metal nanoparticles); R. Gresback, Z. Holman, and U. Kortshagen, “Plasma Synthesis of Highly

Monodisperse Ge Nanocrystals and Self-assembly of Dense Nanocrystal Layers,” *Materials Research Society Symposium Proceedings* 974 (2007) (describing synthesis method for germanium nanocrystals using low pressure, nonthermal plasma); Z. Holman, R. Gresback, and U. Kortshagen, “Nonthermal Plasma Synthesis of Conductive Germanium Nanocrystal Films for Photovoltaic Applications,” *ISPC-18 Proc.* (2007) (describing the nonthermal plasma synthesis of germanium nanocrystals and reporting on the current-voltage measurements of highly porous films of such nanocrystals); R. Gresback, Z. Holman, and U. Kortshagen, “Nonthermal Plasma Synthesis of Size-Controlled, Monodisperse, Freestanding Germanium Nanocrystals,” *Applied Physics Letters* **91**, 093119 (2007) (describing the synthesis of monodisperse germanium nanocrystals via a nonthermal plasma approach); U. Kortshagen, Z. Holman, et al., “Plasma Synthesis of Group IV Quantum Dots for Luminescence and Photovoltaic Applications,” *Pure and Applied Chemistry* (2008) (describing the application of silicon and germanium nanocrystals in solar cells); C.Y. Liu, Z. Holman, and U. Kortshagen, “Hybrid solar cells from P3HT and silicon nanocrystals,” *Nano Letters* **9**, 449 (2009) (describing a new solar cell comprised of silicon nanocrystals and poly-3(hexylthiophene) and reporting the properties of such cells); C.Y. Liu, Z. Holman, and U. Kortshagen, “Optimization of Si NC/P3HT hybrid solar cells,” *Advanced Functional Materials* **20**, 2157 (2010),

and X. Pi, Z. Holman, and U. Kortshagen, “Silicon and Germanium Nanocrystal Inks for Low Cost Solar Cells,” *4th International Conference on Energy Sustainability ASME Conf. Proc.* **2**, 471 (2010) (presenting method for forming silicon and germanium thin films using nanocrystals).

7. From 2010 to 2013, I was a postdoctoral researcher in the Photovoltaics and Thin-Film Electronics Laboratory at the Institute of Microengineering at Ecole Polytechnique Fédérale de Lausanne in Neuchâtel, Switzerland. I also served as a visiting professor with the Photovoltaics and Thin-Film Electronics Laboratory in 2014. While serving in these roles, I continued to research the design and manufacture of solar cells and their components.

8. While a postdoctoral researcher, I published extensively on silicon solar cells, including on passivation layers, transparent conductive oxide and metal contacts, contact resistance, parasitic absorption, and optimization of cell designs. Select peer-reviewed papers related to silicon solar cells that I co-authored while a postdoctoral researcher include: A. Descoeudres, Z. Holman, et al., “Improved amorphous/crystalline silicon interface passivation by hydrogen plasma treatment,” *Applied Physics Letters* **99**, 123506 (2011) (describing reducing recombination at silicon wafer surfaces with deposited amorphous silicon layers); Z. Holman, et al., “Current losses at the front of silicon heterojunction solar cells,” *IEEE Journal of*

Photovoltaics **2**, 7 (2012) (describing parasitic absorption in deposited emitters at the front of silicon solar cells); S. De Wolf, Z. Holman, et al., “High-efficiency silicon heterojunction solar cells: A review,” *Green* **2**, 7 (2012) (reviewing the status of silicon heterojunction solar cell science and technology); Z. Holman, et al., “Infrared light management in high-efficiency silicon heterojunction and rear-passivated solar cells,” *Journal of Applied Physics* **113**, 013107 (2013) (describing parasitic absorption in electrodes of silicon solar cells); and Z. Holman, et al., “Record infrared internal quantum efficiency in silicon heterojunction solar cells with dielectric/metal rear reflectors,” *IEEE Journal of Photovoltaics* **3**, 1243 (2013) (reporting a design for a silicon solar cell with record rear reflectance).

9. From 2013 to 2019, I was Assistant Professor in the School of Electrical, Computer, and Energy Engineering at Arizona State University in Tempe, Arizona. In 2019, I became an Associate Professor, and, in 2023, I became a Professor, both again in the School of Electrical, Computer, and Energy Engineering at Arizona State University. From 2019 to 2023, I also served as Director of Faculty Entrepreneurship in the Ira A. Fulton Schools of Engineering at Arizona State University. Since 2023, I have served as the Vice Dean for Research and Innovation of the Ira A. Fulton Schools of Engineering at Arizona State University.

10. My research interests as a professor include, among other things, contacts to solar cells, interconnection of solar cells, light management in silicon solar cells, and silicon-based tandem solar cells. While at Arizona State University, I have co-authored dozens of peer-reviewed articles in the field of solar cell technology, including: M. Boccard and Z. Holman, “Amorphous silicon carbide passivating layers for crystalline-silicon-based heterojunction solar cells,” *Journal of Applied Physics* **118**, 065704 (2015) (describing passivation layers for silicon solar cells); Y. Zhao, Z. Holman, et al., “Monocrystalline CdTe solar cells with open-circuit voltage over 1 V and efficiency of 17%,” *Nature Energy* **1**, 16067 (2016) (reporting the highest open-circuit voltage measured for a cadmium telluride solar cell, made by using an emitter from silicon solar technology); Z. Yu, M. Leilaieoun, and Z. Holman, “Selecting tandem partners for silicon solar cells using spectral efficiency,” *Nature Energy* **1**, 16137 (2016) (describing a methodology for designing tandem solar cells); K. Bush, Z. Holman, et al., “23.6%-efficient monolithic perovskite/silicon tandem solar cells with improved stability,” *Nature Energy* **2**, 17009 (2017) (describing improved perovskite/silicon tandem solar cells); B. Hallam, Z. Holman, et al., “Pre-fabrication gettering and hydrogenation treatments for silicon heterojunction solar cells: A possible path to >700 mV open-circuit voltages using low-lifetime commercial-grade p-type Czochralski silicon,” *Solar*

RRL 1700221 (2018) (describing improvement of silicon solar cells through gettering and hydrogenation); Z. Ni, Z. Holman, et al., “Resolving Spatial and Energetic Distributions of Trap States in Metal Halide Perovskite Solar Cells,” *Science* **367**, 1352 (2020) (reporting on the spatial and energetic distributions of trap states in metal halide perovskite single-crystalline and polycrystalline solar cells.); J. Xu, Z. Holman, et al., “Triple-halide Wide-band Gap Perovskites with Suppressed Phase Segregation for Efficient Tandems,” *Science* **367**, 1097 (2020) (describing efficient wide-band gap perovskite top cells using triple-halide alloys); and K. Chen et al., “Self-aligned selective area front contacts on poly-Si/SiO_x passivating contact c-Si solar cells,” *IEEE Journal of Photovoltaics* **12**, 678 (2022) (describing a method to pattern polycrystalline silicon / silicon dioxide layers in silicon solar cells). Additional journal articles, book chapters, and conference papers are described in further detail in my CV (**Appendix A**).

11. I have received numerous awards for both my teaching and research. For my teaching, I have been honored with the ASU Fulton Schools of Engineering Top 5% Teaching Award in 2023, 2017, and 2015. For my research, I have received the IEEE Stuart R. Wenham Young Professionals Award in 2019 and the NSF CAREER Award in 2019 (an award given to photovoltaic researchers), among other honors, prizes, and awards. My awards and honors are listed in my CV. I have also

received numerous research grants, as detailed in my CV, including eighteen grants from the Department of Energy's Solar Energy Technologies Office. Two exemplary grants are "Development of new metallization pastes for front-side tunnel oxide passivated contact crystalline silicon solar cells" and "ASU-NREL joint silicon solar cell research: passivated contacts, metallization, and bulk defects."

12. Among the courses I teach at Arizona State University are "Electrical Engineering 465/591: Photovoltaic Energy Conversion," "Electrical Engineering: 498/591: Solar Energy," and "Electrical Engineering 565: Solar Cells." I have also taught innovation and venture development courses that combine academic learning with an applied business development approach. Other courses I have taught are listed in my CV.

13. I have advised numerous doctoral students and other researchers in training. Students whom I have advised have won numerous honors and awards, including many best-paper awards at top solar conferences. A full list of students I have advised and their awards are provided in my CV.

14. Some of my many professional activities include being editor of the *IEEE Journal of Photovoltaics* since 2022; serving as an organizing member for the IEEE Photovoltaic Specialists Conference, World Conference on Photovoltaic Energy Conversion, and International Workshop on Silicon Heterojunction Solar

Cells; serving as a member and chair of the ASU Solar Fabrication Core Facility Board since 2020; being a reviewer for journals including *Journal of Applied Physics*, *ACS Nano*, *Solar Energy Materials and Solar Cells*, *Thin Solid Films*, *Nanotechnology*, and *IEEE Journal of Photovoltaics*; being a reviewer for grant proposals for the Department of Energy and the National Science Foundation; and serving as a session chair for numerous symposia and conferences on solar science and technology. A full list of my professional and outreach activities is provided in my CV.

15. My research, engineering and entrepreneurial endeavors have been regularly recognized by the industry. For example, Arizona PBS has reported on one of my start-up companies, SunFlex Solar, which has developed an improved method for interconnecting back-contact solar cells into solar modules. See “New Solar Panel Technology,” *Arizona PBS* (Mar. 29, 2023), available at <https://azpbs.org/horizon/2023/03/new-solar-panel-technology>. Also, I worked with two United States based solar cell manufacturers relating to an instrument that I developed to analyze recombination in solar cells; copies of the instrument are now used in their research and development facilities. As another example, my research demonstrating a manufacturing technique for high-efficiency perovskite-silicon tandem solar cell was covered in *PV Magazine*, a leading solar cell industry

publication. See Emilliano Bellini, “New Manufacturing Technique for 26%-efficient Tandem Perovskite Solar Cell,” *PV Magazine* (Apr. 20, 2020), available at <https://www.pv-magazine.com/2020/04/20/new-manufacturing-technique-for-26-efficient-tandem-perovskite-solar-cell>.

16. I am also an entrepreneur and have founded three companies to bring new solar technology to market. In 2021, I co-founded Beyond Silicon, Inc. (“Beyond Silicon”), which is developing perovskite/silicon tandem solar cells. Beyond Silicon was a finalist for the American-Made Perovskite Startup Prize. In 2020, I co-founded SunFlex Solar LLC (“SunFlex Solar”), which develops interconnected back-contact solar cells using aluminum foil for improved efficiency and durability. SunFlex Solar won the American-Made Solar Prize and has a partnership with a US solar panel manufacturer to commercialize its interconnection technology. In 2016, I co-founded Swift Coat, Inc. (“Swift Coat”), which has developed a transparent coating for solar panels that prevents dust buildup that would otherwise reduce solar panel efficiency. Swift Coat has also won a contract from NASA to deposit similar coatings—but modified to provide an anti-fogging functionality—on the inside of the helmet of NASA’s next generation xEMU space suit. In 2018, I received the Gordon and Betty Moore Foundation Inventor

Fellowship to support my efforts to accelerate the translation of my research to market.

17. I am being compensated for my work on this matter at my standard hourly consulting rate of \$500 per hour. My opinions are based on my own views and understanding of the prior art, the knowledge of a person of ordinary skill in the art, and the '315 patent. My compensation is not dependent on and in no way affects the substance of my statements, opinions, or conclusions in this declaration and it is also not dependent on any testimony I give or on the outcome of this proceeding.

18. I have no financial interest in Petitioner or Patent Owner. I similarly have no financial interest in the '315 patent, and I have had no contact with the named inventors of the '315 patent.

III. LEGAL PRINCIPLES

19. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law was provided to me by Petitioner's attorneys.

A. Scope of Opinion

20. I have been informed and understand that the petitioner in an *inter partes* review may request cancellation of claims as unpatentable only on grounds that such claims are anticipated or would have been obvious to a person of ordinary

skill in the art at the time of the purported invention, and only on the basis of prior art consisting of patents and/or printed publications. My opinions in this matter address only such grounds.

B. Anticipation

21. I have been informed that a patent claim is anticipated and therefore unpatentable if every element of the claim is present in a single prior art reference.

C. Obviousness

22. I understand that a claim is unpatentable if, at the time the alleged invention was made, it would have been obvious to a person of ordinary skill in the art. I understand that a claim can be obvious based on the teachings or suggestions of either a single prior art reference or a combination of two or more prior art references. I understand that the obviousness analysis requires an understanding of the scope and content of the prior art, any differences between the prior art and the alleged invention, and the level of ordinary skill in evaluating the pertinent art.

23. I understand that in order to be considered for obviousness, prior art must be analogous to the patent at issue. I further understand that art is analogous if it either pertains to the same field of endeavor as the patent at issue or, alternatively, if it is reasonably related to the problem faced by the inventor(s) of the patent at issue.

24. I understand that a claim would have been obvious if it unites old elements with no change to their functions or alters prior art by mere substitution of one element for another known in the field such that the combination yields predictable results. Also, I understand that obviousness does not require a physical combination or example, but rather is concerned with what the combined teachings would have taught or suggested to persons of ordinary skill in the art at the time of the alleged invention.

25. In connection with obviousness, I have been informed that there must have been some reason or motivation for a person of ordinary skill in the art to have combined or modified the relevant teachings in the prior art to obtain the claimed invention, and one of ordinary skill in the art must have had a reasonable expectation of success making the combination or modification.

26. I understand that a claim would have been obvious if a person of ordinary skill in the art would have had reason to combine multiple prior art references or add missing features to reproduce the alleged invention recited in the claims. I further understand that there is no rigid requirement of finding an express teaching, suggestion, or motivation to combine within the references, although such an express teaching or suggestion may be helpful in identifying a reason for the combination.

27. If a person of ordinary skill in the art can implement a predictable variation, that variation is likely unpatentable as obvious. For the same reason, if a technique has been used to improve one device and a person of ordinary skill in the art would have recognized that it would improve similar devices in the same way, using the technique to make such an improvement would have been obvious.

28. I understand that when considering obviousness, it is important not to use the benefit of hindsight derived from the patent being considered. I also understand that one of ordinary skill in the art has ordinary creativity (i.e., is not a mindless automaton).

29. In sum, I understand that a determination of whether a claim would have been obvious is based upon the following non-exclusive considerations:

- whether prior art references teach or disclose known concepts combined in familiar ways, such that when combined they would yield predictable results;
- whether a person having ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, where those skilled in the art would have had a reasonable expectation of success in implementing that design choice;

- whether a person having ordinary skill would have been motivated based on the prior art to combine known elements in the manner described in the claim;
- whether there is a teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the alleged invention applies a known technique that had been used to improve at least one similar device or method in a similar way.

30. I further understand that certain additional factors, commonly referred to as secondary considerations or objective indicia, may support or rebut the obviousness of a claim. I understand that secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, copying of the alleged invention by others in the field, and contemporaneous and independent invention by others. I understand that there must be a nexus (i.e., a connection) between any such secondary considerations and the alleged invention. I also understand that secondary considerations cannot be used to overcome anticipation. I further understand that

contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

31. I reserve the right to respond to any allegations that Patent Owner may put forth in this proceeding suggesting that secondary considerations tend to rebut the obviousness of any claim of the '315 patent as discussed in this declaration.

D. Claim Dependency

32. I understand patents may include two types of claims: independent claims and dependent claims. An independent claim stands alone and simply recites the limitations it covers. In contrast, a dependent claim depends from either an independent claim or another dependent claim, and incorporates all the limitations recited in the claim or claims from which it depends along with the limitations it recites itself.

E. Written Description

33. I have been informed and understand that an application is required to describe the claim limitations contained in the application. I understand this requirement is called the “written description requirement.” I have been informed and understand that to satisfy the written description requirement, the patent’s specification must describe the claimed invention with enough detail for a person of

ordinary skill in the art to reasonably conclude that the inventor had possession of the claimed invention at the time of filing.

* * *

34. The analysis that follows in this declaration is in accordance with the above-stated legal principles.

IV. MATERIALS CONSIDERED

35. In forming my opinions, in addition to my knowledge and experience, I have considered the materials cited herein and listed in **Appendix B**.

V. PRIORITY DATE

36. I have been informed that the '315 patent claims priority to App. No. 14/579,935 filed on December 22, 2014. I have formed my opinions in reference to this priority date. Should Patent Owner suggest a different priority date, I reserve the right to revise my opinions accordingly.

VI. LEVEL OF ORDINARY SKILL IN THE ART

37. I understand that when considering the claims of the '315 patent and the prior art, I must do so from the perspective of one of ordinary skill in the art as of the patent's effective priority date.

38. I have been informed and I understand the factors to be considered in determining who would be a person of ordinary skill in the art include: (1) the types of problems encountered in the art; (2) the prior art solutions to those problems; (3)

the rapidity with which innovations are made; (4) the sophistication of the technology; and (5) the educational level of active workers in the field.

39. Based on these factors as well as my experience and expertise, a person of ordinary skill in the art as of the claimed priority date of the '315 patent (also called a "POSITA") would have had (1) an advanced degree in applied physics, chemistry, electrical engineering, materials science, mechanical engineering, or a related discipline and (2) at least one year of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. Alternatively, a person of ordinary skill in the art would have had (1) a bachelor's degree in one of the aforementioned disciplines and (2) at least two years of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. Additional work experience may compensate for less formal education, and vice versa.

40. My analysis and opinions herein regarding the '315 patent have been based on the perspective of a person of ordinary skill in the art as of the priority date for the '315 patent (i.e., December 22, 2014).

41. I have the qualifications and experience necessary to assess the '315 patent based on the perspective of a person of ordinary skill in the art, including as of the priority date for the '315 patent. *See* Section II. For example, by 2014, I had

an advanced degree in mechanical engineering. I also had approximately nine years of experience designing, developing, or researching the design and/or manufacture of solar cells, including as a postdoctoral researcher in the Photovoltaics and Thin-Film Electronics Laboratory at the Institute of Microengineering at École Polytechnique Fédérale de Lausanne from October 2010 to March 2013 and as Assistant Professor at Arizona State University's School of Electrical, Computer, and Energy Engineering beginning March 2013.

VII. TECHNOLOGY BACKGROUND

A. Overview of Solar Cells

42. A solar cell is a solid-state electrical device that absorbs solar radiation (sunlight) and converts that solar radiation to electricity. An individual solar cell generates electricity when it is exposed to solar radiation by directing excited electrons around an external circuit. Ex.1072-Komp, 2-4; Ex.1018-Holman-Thesis, 1-2. To generate a usable amount of energy, a single solar cell is typically not used in isolation; instead, multiple solar cells are electrically connected to each other to form a solar module. Ex.1072-Komp, 49-51. An example solar module is below, which is the BP MSX-120 Solar Module that was available before 2014 and includes “72 multicrystalline silicon solar cells” that are electrically connected to each other.



Ex.1054-BP-MSX-120, 1. Multiple solar modules are connected together in a solar array to generate larger amounts of electricity. Ex.1072-Komp, 34-36, 49-53.

43. The design and manufacture of solar cells have been studied for several decades. A solar cell is typically made of a slab of silicon, called a “wafer,” and thin layers added to each side of the wafer. Ex.1072-Komp, 13-14, 20-21, 30-34. The thin layers can be made of many materials, including silicon. Silicon can come in different forms depending on how its atoms are organized. Ex.1072-Komp, 25-29, 37-39. For example, silicon can be “monocrystalline” if its atoms are all arranged in a perfectly periodic structure—a crystal. Ex.1072-Komp, 27-29; Ex.1023-Nelson, 179 (“Materials can be prepared as single crystals (monocrystalline) or as polycrystalline or multicrystalline wafers.”); *see also* Ex.1018-Holman-Thesis, 19-

20. Silicon can also be “polycrystalline” silicon (also called “polysilicon”), which means that it has multiple crystalline regions or “grains,” but they are not aligned with each other, resulting in “grain boundaries” at their interfaces. Ex.1072-Komp, 37-38; Ex.1023-Nelson, 179. A third type of silicon, amorphous silicon, is also utilized by some solar cells and has a non-crystalline structure—a somewhat randomized arrangement of atoms. Ex.1072-Komp, 40-47; Ex.1018-Holman-Thesis, 20-22. These three types of silicon have long been used in solar cells and were well-established in the art prior to 2014. Ex.1072-Komp, 25.

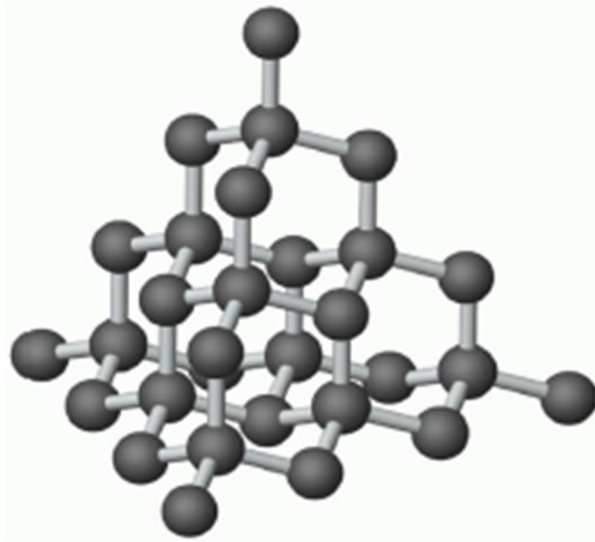
44. Prior to 2014, it was well known that solar cells had wafers or layers that were doped with phosphorus or boron to create PN junctions, solar cells included metal contacts to connect the cells to each other, and the front side of solar cells were textured and had anti-reflective coatings. The following sections briefly discuss these concepts.

1. Doping

45. In typical solar cells, chemical elements are introduced into silicon wafers or silicon layers to change the material properties of the silicon in the region where the elements are present. Ex.1018-Holman-Thesis, 23-24. The process for introducing these chemical elements, which are typically boron or phosphorus, is known as doping. *E.g.*, Ex.1023-Nelson, 181-182. As explained below, doping

introduces extra “electrons” or “holes,” which can alter the behavior of electrons that are excited in the solar cell when it is illuminated. Ex.1072-Komp, 7-9; Ex.1018-Holman-Thesis, 23-25.

46. An electron is a negatively charged particle and is part of an atom. Ex.1072-Komp, 7-9. An atom has one or more “valence” electrons, which are electrons on the outermost shell of an atom. Ex.1072-Komp, 7-9. Silicon has four valence electrons, and its outermost shell can hold up to eight. Ex.1024-Pierret, 26; Ex.1018-Holman-Thesis, 20. In a crystalline silicon solid, silicon atoms bond with four neighboring silicon atoms in a periodic arrangement or “lattice.” *See* Ex.1018-Holman-Thesis, 19-20 (showing two-dimensional crystalline lattice); Ex.1024-Pierret, 26. The silicon atoms share their valence electrons with the atoms to which they are bonded, resulting in each silicon atom perceiving that it has a filled valence shell of eight atoms. Ex.1023-Nelson, 44; Ex.1024-Pierret, 26. A simplified diagram of a silicon lattice is the following:



Ex.1018-Holman-Thesis, 20; *see also* Ex.1075-Green-1995, 5; Ex.1024-Pierret, 9-10.

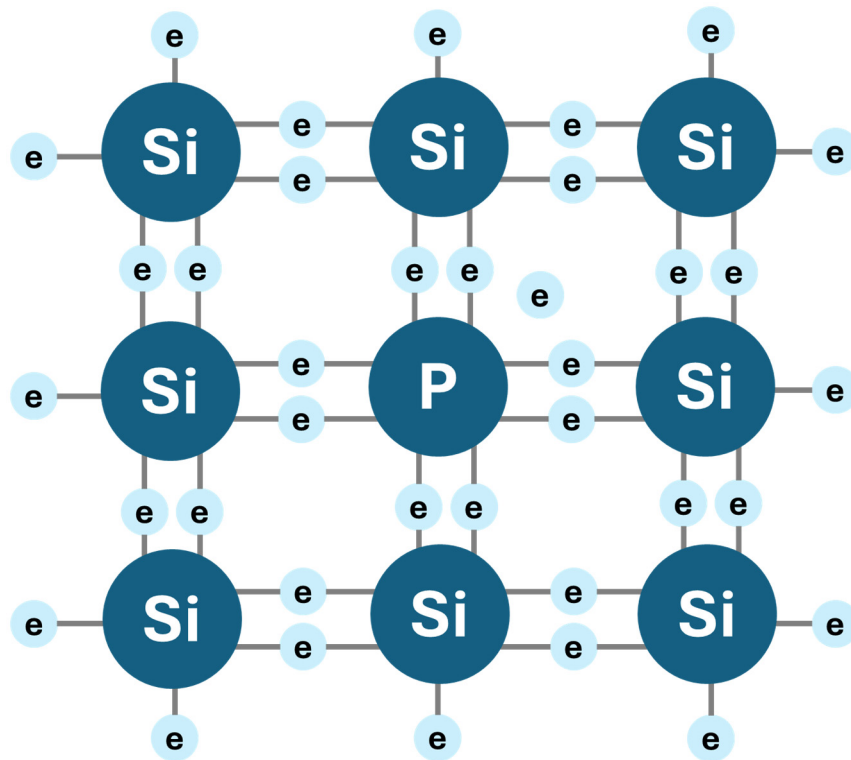
47. Once silicon atoms are bonded together in a solid, their valence electrons no longer reside in the individual shells of the isolated atoms, but instead populate a “valence band.” *See* Ex.1072-Komp, 13-18; Ex.1024-Pierret, 26-29; Ex.1018-Holman-Thesis, 6. The valence band is normally mostly full of electrons. Ex.1024-Pierret, 26-29. Silicon also has another band that is important to the function of solar cells, the “conduction band.” Ex.1024-Pierret, 29-32; Ex.1018-Holman-Thesis, 6. The conduction band is at a higher energy than the valence band and is thus normally mostly empty of electrons, but it may become (partially) populated either by the introduction of dopant atoms into the silicon crystal or by excitation of an electron from the valence band. Ex.1024-Pierret, 29-32. The

energetic distance between the top of the valence band and the bottom of the conduction band is the “bandgap energy.” Ex.1024-Pierret, 29-32; Ex.1018-Holman-Thesis, 6.

48. Introducing atoms with one more valence electron than silicon into the silicon crystal creates an extra electron that does not fit in the valence band. Ex.1024-Pierret, 35-39. Instead, at the temperatures at which solar cells normally operate, the extra electron resides in the conduction band. Ex.1024-Pierret, 35-39. The extra electron does not participate in bonding and is free to move around in the solid. Introducing such atoms is called doping, and in particular, n-type doping when extra electrons are introduced. Ex.1023-Nelson, 181-182; Ex.1024-Pierret, 35-39; Ex.1018-Holman-Thesis, 23-24. In solar cells, n-type doping is used to create extra electrons in certain regions of the silicon wafer or layers of the solar cell. Ex.1023-Nelson, 181-182; *see also* Ex.1018-Holman-Thesis, 23-25.

49. It was well known prior to 2014 that phosphorous was commonly used as a dopant to create n-type regions or layers. As shown in the simplified diagram below, because phosphorus has five valence electrons (one more than silicon), an extra electron is introduced in the conduction band that can move through the lattice structure. Ex.1024-Pierret, 35-39; Ex.1072-Komp, 12-13 (“[I]f a small amount of phosphorus is added to the silicon crystal, the atoms of phosphorus (which have 5

valence electrons) will contribute 4 electrons and 4 levels to the valence band, and the extra electron will occupy a level near the bottom of the conduction band...It takes very little energy for the extra electron to jump to the conduction band from this donor level, so-called because it can donate conduction electrons to the system.”).



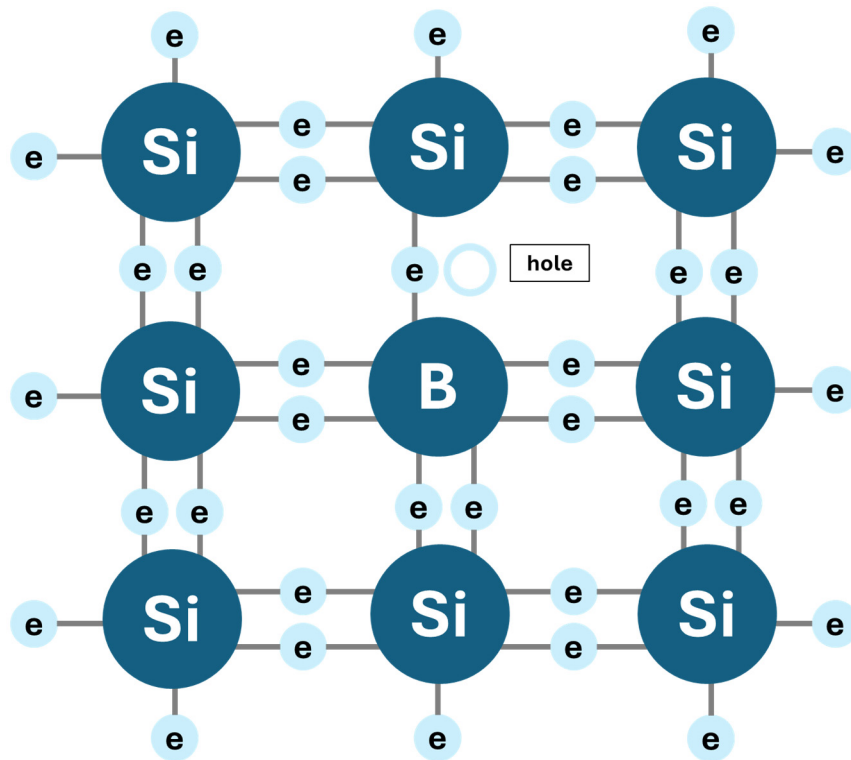
See Ex.1018-Holman-Thesis, 25; *see also* Ex.1024-Pierret, 36.

50. On the other hand, introducing atoms with one fewer valence electron than silicon into the silicon crystal creates a “hole” in the valence band. Ex.1024-Pierret, 35-39. A hole is not a physical object, like an electron, but rather a mathematical concept that represents an absence of an electron in the valence band.

Ex.1024-Pierret, 35-39; Ex.1018-Holman-Thesis, 8. A hole in the valence band is mobile, much like an electron in the conduction band. Ex.1018-Holman-Thesis, 8. A hole does not physically move like an electron does, but because electrons move by filling holes, the science considers that holes also move, figuratively. Ex.1024-Pierret, 35-39; Ex.1018-Holman-Thesis, 8. A moving electron carries a negative charge, and a moving hole carries a positive charge. Ex.1018-Holman-Thesis, 8. Thus, in the solar cell field, electrons and holes are both called “charge carriers” or simply “carriers” (of electricity). Ex.1072-Komp, 7-11.

51. Introducing atoms with one fewer valence electron than silicon is called p-type doping. Ex.1024-Pierret, 35-39; Ex.1023-Nelson, 181-182; Ex.1018-Holman-Thesis, 23-24. In solar cells, p-type doping is used to create extra holes in certain regions of the silicon wafer or layers of the solar cell. It was well known prior to 2014 that boron was commonly used as a dopant to create p-type regions or layers. Ex.1023-Nelson, 181-182. As shown in the simplified diagram below, because boron has three valence electrons (one fewer than silicon), a hole is introduced in the valence band that can move through the lattice structure. *See* Ex.1072-Komp, 11 (“[I]f an atom of boron (which has a valence of 3) is added to the crystal, it will contribute only 3 electrons to the system. It will also contribute 3 valence levels, plus 1 level which will be created in the band gap slightly above the

top of the valence band...These extra levels, called acceptor levels, are capable of accepting an electron from the valence band. Since the acceptor level is associated with a particular impurity atom, the electron that occupies it is trapped and cannot move. However, the hole created when the electron leaves the valence band can move.”).



See Ex.1018-Holman-Thesis, 25; *see also* Ex.1024-Pierret, 36.

52. Techniques for doping solar cell layers with phosphorous or boron were well-established by 2014. Ex.1072-Komp, 11 (“The process of deliberately adding a known impurity to a pure semiconductor is called doping.”). Silicon wafers were commonly purchased by solar cell manufacturers already uniformly doped (i.e., with

spatially uniform “background” dopant concentration). A wafer with uniform n-type doping was referred to as an “n-type wafer;” a wafer with uniform p-type doping was referred to as a “p-type wafer.” *See* Ex.1024-Pierret, 40; Ex.1018-Holman-Thesis, 22-23.

53. A common doping technique used in solar cell fabrication, called “diffusion,” involved driving dopant atoms from a dopant source—a gas, a liquid, or a solid containing dopant atoms—into a silicon wafer or a polysilicon layer at high temperatures in a furnace. Ex.1074-Benick, Abstract (“Emitter formation by in-line deposition of a PECVD PSG and subsequent diffusion in an in-line belt furnace”); Ex.1013-Froitzheim, [0011] (“diffusion from a p-type dopant from a liquid that is applied to the rear side”); Ex.1068-Smith-288 (depositing boron-doped silicon dioxide (“BSG”) and phosphorus-doped silicon dioxide and diffusing dopants into a wafer). Diffusion was commonly used during solar cell fabrication to dope the region(s) near a surface of a wafer n-type or p-type, which either further enhanced the background doping of the wafer (if the diffused region had the same polarity as the wafer) or converted the polarity of the surface region of the wafer (if the diffused region had the opposite polarity as the wafer).

54. One well-known technique for diffusing phosphorus into a silicon wafer or polysilicon layer was known as phosphosilicate glass (PSG) diffusion. The

PSG diffusion technique involved forming a layer of PSG on the surface of the wafer (or a polysilicon layer on the wafer). One method to do this involved vaporizing phosphorus-containing liquid such as phosphorus oxychloride (POCl_3) into a furnace containing silicon wafers, where it reacted with the silicon atoms to form the PSG. Applying heat then drove the phosphorus from the PSG into the silicon or polysilicon via diffusion. *See, e.g.*, Ex.1023-Nelson, 187 (“Phosphorus may be deposited either from the vapour phase by exposure to nitrogen gas bearing POCl_3 ; from solid phase, for example by chemical vapour deposition of phosphorus oxide; or directly by ion implantation.”); Ex.1068-Smith-288, 3:56-57 (“atmosphere containing phosphorus oxychloride”); Ex.1013-Froitzheim, [0044] (“diffusion of Phosphorous from the gas phase”); Ex.1073-Krygowski, 1 (“ POCl_3 diffusion step is used to co-diffuse the emitter and pre-alloyed BSF”); Ex.1074-Benick (explaining POCl_3 diffusion).

55. Another known technique for diffusing boron into a silicon wafer or polysilicon layer was known as borosilicate glass (BSG) diffusion. This technique involved forming a layer of BSG on the surface of the wafer (or a polysilicon layer on the wafer) to form BSG. Ex.1068-Smith-288, 2:44-4:2; Ex.1013-Froitzheim, [0040]-[0041]. One method to do this involved vaporizing boron-containing liquid such as boron tribromide (BBr_3) into a furnace containing silicon wafers, where it

reacted with the silicon atoms to form the BSG. Ex.1034-Kerr, 153-155. Applying heat then drove the boron from the BSG into the silicon or polysilicon via diffusion. Ex.1068-Smith-288, 2:44-4:2; Ex.1013-Froitzheim, [0040]-[0041].

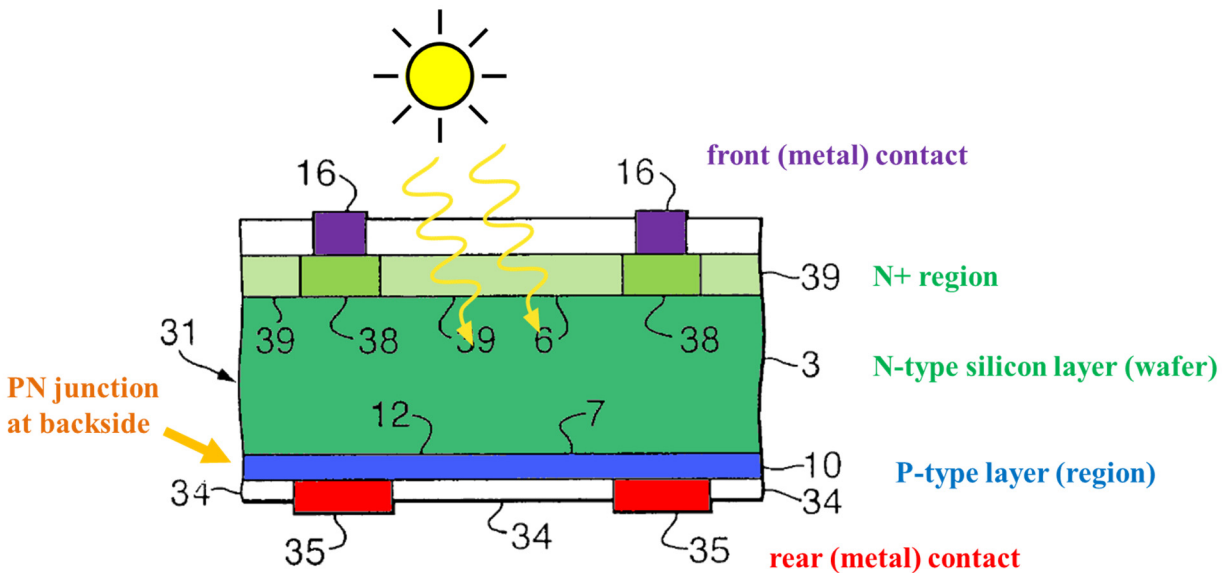
2. PN Junction

56. In a typical solar cell, an interface between n-type and p-type regions in a silicon wafer, or between an n-type wafer and a p-type layer added to that wafer (alternatively, a p-type wafer and an n-type layer added to it), is formed and is commonly known as the “PN junction.” Ex.1072-Komp, 5-18; *e.g.*, Ex.1016-Tarr, 655-57. At the center of a PN junction is established an “electric field.” An electric field exerts a force on charge carriers that pushes them in the direction of the electric field or opposite the direction of the electric field, depending on the polarity of the charge carriers. Ex.1024-Pierret, 75-79. The PN junction—because of its built-in electric field—acts as the driving force to create electrical current when the solar cell is illuminated. Ex.1024-Pierret, 101; Ex.1018-Holman-Thesis, 26 (“The internal electric field separates the charges and pulls them towards the appropriate contacts. They flow through an external circuit, and—voilà!—electricity.”).

57. When solar radiation reaches a solar cell, and when the energy of the photons is greater than the bandgap energy of the silicon wafer, electrons in the valence band may be excited to the conduction band, absorbing the photons’ energy

to make the transition. *See* Ex.1072-Komp, 5-18, 10 (“The electron might be thermally excited by...a photon of light of sufficient energy might be absorbed by the crystal and cause the electron to jump. Once the electron is in the upper conduction band, it is free to move and can act as a carrier of electricity.”); Ex.1018-Holman-Thesis, 14-15. Each “photoexcited” electron leaves behind a hole in the valence band; light absorption creates an “electron-hole pair.” *See* Ex.1072-Komp, 5-18, 182 (defining “band gap energy” as “[t]he energy needed to raise an electron from the top of the valence band to the bottom of the conduction band”); Ex.1018-Holman-Thesis, 14-15. As discussed herein, the photoexcited electrons are mobile in the conduction band, and the photoexcited holes are mobile in the valence band. Ex.1018-Holman-Thesis, 14-15. A solar cell produces electricity when the photoexcited electrons are conveyed to one metal contact and the photoexcited holes are conveyed to a separate metal contact. Ex.1018-Holman-Thesis, 16. The PN junction facilitates this separation of the charge carriers. In particular, photoexcited electrons that encounter the PN junction are swept to the n-type region or layer by the PN junction’s electric field, and photoexcited holes that encounter the PN junction are swept to the p-type region or layer. *See* Ex.1072-Komp, 2-18; *see also* Ex.1018-Holman-Thesis, 24-25.

58. As an example, the below solar cell shown includes an **n-type silicon layer (wafer)** containing n-type dopants such as phosphorous. Ex.1013-Froitzheim, [0010]-[0011], Fig.3. The wafer is often called a “substrate” because it is the base upon which other layers of the solar cell are built. It is also the thickest layer in the solar cell, commonly being 100-300 μm thick. The backside (also called a rear side in literature) of the solar cell below includes a **p-type layer (region)**, made by diffusing p-type dopants such as boron into the substrate’s backside. Ex.1013-Froitzheim, [0010]-[0011], Fig.3. Diffused regions are thin relative to the wafer’s thickness, commonly extending 0.3-3 μm into the wafer’s surface. Ex.1013-Froitzheim, [0026]. At the interface of the n-type substrate and p-type region, the “PN junction” is formed. Ex.1013-Froitzheim, [0010], [0022], [0025]. Because the diffused region is thin and the wafer is thick, the PN junction is much closer to the backside of the solar cell than its middle or front. The p-type layer, in this case, as it is oppositely doped from the substrate, is called an “emitter.” In the field of solar cell technology, “emitter” usually refers to the region or layer that is oppositely doped from the substrate.



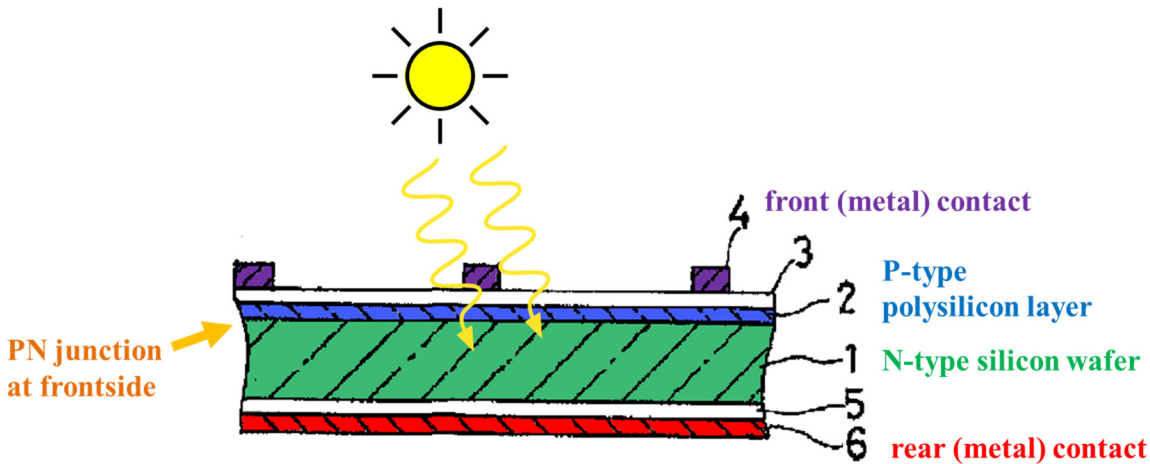
Ex.1013-Froitzheim, Fig.3.¹

59. Throughout the history of solar cells, many different arrangements of solar cell components have been developed. The placement of the PN junction, whether at the “backside” of the solar cell (formed by, e.g., a diffusion into the back of the wafer) or at the “frontside” of the solar cell (formed by, e.g., a diffusion into the front of the wafer), was one of the well-known arrangement options. *Compare* Ex.1023-Nelson, 188 (Fig.7.7, frontside configuration); Ex.1013-Froitzheim, Fig.3 (backside configuration). In a “back-junction” (also called “backside junction”)

¹ All annotations and emphasis in figures and text throughout this Declaration are added unless otherwise noted.

configuration, in which the junction is at the solar cell's backside (as shown in Froitzheim above), the uniformly doped "bulk" of the wafer is closer to the sun than the oppositely doped emitter region or layer, and the sunlight hits the former first. *E.g.*, Ex.1013-Froitzheim, Fig.3. The PN junction is thus formed at the backside of the substrate, at the interface between the wafer bulk (n-type in the above figure) and the emitter (p-type in the above figure). Ex.1013-Froitzheim, Fig.1, Fig.3; Ex.1069-Li, Fig.1; Ex.1017-Meier, Fig.2, 4:27-65.

60. Alternatively, in a "front-junction" (also called "frontside junction") configuration, the emitter region or layer is located closer to the sun than the wafer bulk, and the sunlight hits the emitter first. *E.g.*, Ex.1014-Okayasu, Fig.1. The PN junction is formed at the frontside of the substrate, at the interface between the emitter (p-type in the below figure) and the wafer bulk (n-type in the below figure):



Ex.1014-Okayasu,² Fig.1.

61. A second method to form an emitter, in addition to dopant diffusion into a region near a surface of the wafer, as in Froitzheim above, is to “deposit” a layer onto the wafer surface that has the opposite doping polarity of the wafer. Deposition refers to a process to add such a layer, which is commonly built up atom by atom. Known processes include chemical vapor deposition and physical vapor deposition. Amorphous silicon and polycrystalline silicon emitter layers were well known by 2014. *E.g.*, Ex.1069-Li, Fig.1; Ex.1014-Okayasu, Fig.1. Okayasu above shows a polycrystalline silicon emitter.

62. The manufacturing processes for front- and back-junction solar cells were functionally similar. For instance, they both involved a doped silicon wafer,

² See Ex.1015-Okayasu-Decl. (translator declaration for Okayasu translation).

diffusing dopants into the surface of the wafer or into polycrystalline silicon layers deposited on the wafer to form a PN junction, adding an anti-reflection coating, and adding metal contacts, among other standard manufacturing steps. *E.g., compare* Ex.1013-Froitzheim, [0038]-[0051] *with* Ex.1014-Okayasu, [0044].

B. Solar Cell Efficiency

63. As discussed above, solar cells generate electricity when incident light excites electron-hole pairs that are separated and reach metal contacts connected to an external circuit. Solar cell efficiency is the ratio of power output from the cell to the power input from the sun under specific conditions, and solar cell efficiency is referred to as “power conversion efficiency.” Ex.1023-Nelson, 289. In other words, power conversion efficiency is a measure of the amount of electrical power extracted from the solar cell per amount of radiation power incident on the solar cell under particular conditions. For terrestrial solar cells, the conditions for evaluating efficiency are Air Mass 1.5 Global spectrum, 1000 W/cm², and 25 °C. Ex.1023-Nelson, 289.

64. Since the first modern solar cell was created in 1954 by Bell Laboratories (Ex.1058-Chapin), skilled artisans have worked continuously to improve cell efficiency. When the modern solar cell was initially created, the efficiency was about 6%. Ex.1058-Chapin. In 1961, a groundbreaking paper

discussing the limit of solar cell efficiency was published by William Shockley and Hans Queisser. Ex.1059-Shockley. It noted that a “theoretically justifiable upper limit” of efficiency exists in solar cells based on the laws of physics. Since then, the Shockley-Queisser limit for silicon-based solar cell (bandgap energy of 1.12eV) efficiency has been known to be about 30%. Ex.1059-Shockley. Because of the physical limit on a cell’s efficiency, even small efficiency gains were desirable. Ex.1045-Sah, 1:15-20 (patent filed in 1986 noting that “[s]ince about 1956, silicon solar cell conversion efficiency has been improved from about 5% to more than 16%”); Ex.1048-Metz (claiming 18.5% efficiency); Ex.1049-De Ceuster (claiming 22% efficiency); Ex.1074-Benick (claiming 17.5% efficiency).

65. As I explained above, a solar cell generates electricity through the separation of photogenerated electrons and holes. One important goal of solar cell design is to maximize the number of electron-hole pairs that contribute to generating electricity by exiting through their respective metal contacts (i.e., electrodes). This is because the created electricity becomes usable only when it powers an external circuit. Ex.1072-Komp, 3-4, 121, 154-57.

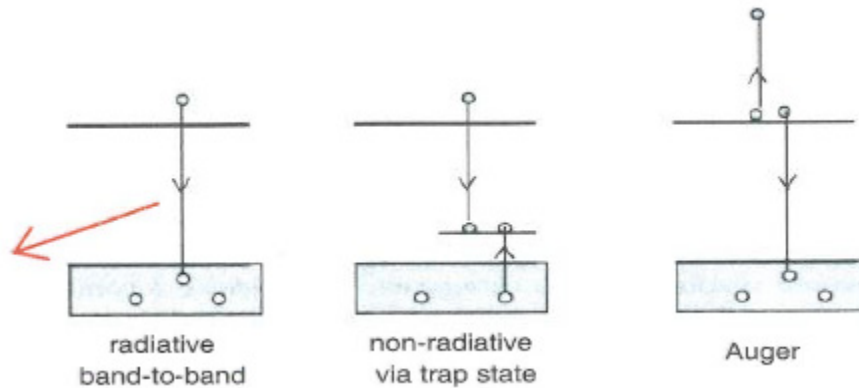
1. Recombination

66. One well-known way to increase the number of electrons and holes that reach their metal contacts is to prevent the electrons and holes from “recombining”

with each other before exiting the cell. Recombination is “the loss of mobile electrons or holes by any number of removal mechanisms.” Ex.1023-Nelson, 99. Recombination “annihilates” mobile electrons and holes (i.e., de-excites an electron from the conduction band to fill a hole in the valence band) and prevents them from contributing to the solar cell’s output current, thereby reducing the solar cell’s efficiency. Ex.1024-Pierret, 105. Long before 2014 it was well known that recombination would limit the efficiency of a solar cell device.

67. One measure of recombination is saturation current density, J_0 . Ex.1034-Kerr, 18-19. High J_0 indicates high recombination levels and low J_0 indicates low recombination levels. Ex.1034-Kerr, 18-19.

68. It was well known by the earliest possible priority date of the ’315 patent that carriers (*i.e.*, electrons or holes) recombine in many ways. Generally, there exist three types of recombination: (1) radiative band-to-band recombination; (2) non-radiative recombination; and (3) Auger recombination. Ex.1023-Nelson, 100; Ex.1025-Fonash, 37-38.



Ex.1023-Nelson, 100, Fig.4.7.

69. **Radiative band-to-band recombination** occurs when electrons and holes recombine and release energy in the form of a photon. Ex.1025-Fonash, 37-38; Ex.1024-Pierret, 105. This process is uncommon in silicon solar cells due to the nature of the silicon lattice.

70. **Non-radiative recombination**, also known as Shockley-Read-Hall (SRH) recombination, is common in silicon semiconductor devices. Ex.1023-Nelson, 106-107. This type of recombination occurs when the substrate has lattice defects or chemical impurities and involves two steps: (1) the trapping of an electron or hole at an energy level created by the defect, and (2) the movement of an opposite charged carrier (hole or electron) to the defect energy level, resulting in recombination and the release of energy in the form of heat. Ex.1023-Nelson, 106-107; Ex.1026-Hu, 48.

71. “Surface recombination” is a common type of SRH recombination whereby electrons or holes recombine at surfaces or interfaces between materials. Ex.1023-Nelson, 110; Ex.1010-Granek, 117-118. By 2014, it was well known that the surface of a semiconductor substrate was “severely disturbed” with non-saturated bonds (i.e., it was a spatially extended lattice defect). Ex.1010-Granek, 117. For example, defect states that facilitate carrier recombination are located at broken bonds, also called dangling bonds, at the surface of the silicon substrate or its interface with many other materials (e.g., metals). Ex.1010-Granek, 117-118.

72. **Auger recombination** occurs when two electrons (or two holes) collide, and one of the electrons (or one of the holes) is excited to a higher energy level (where it subsequently releases its excess energy in the form of heat). The other electron (or hole) recombines with a hole (or electron). Ex.1023-Nelson, 104; Ex.1024-Pierret, 107. This type of recombination increases as dopant levels increase because more dopants increase the likelihood of there being available carriers to which electron-hole pairs may transfer their energy. Ex.1023-Nelson, 104; Ex.1026-Hu, 48.

2. Methods of Reducing Recombination

a. Surface Passivation

73. It was well known by the earliest possible priority date of the '315 patent that surface passivation techniques reduce carrier recombination. Ex.1010-Granek, 117-119. For example, doping a front region of the silicon substrate reduces the concentration of one carrier type (and increases the concentration of the other), and without the presence of both carrier types, recombination decreases. Ex.1010-Granek, 117-119.

74. This doped front region is called a front surface field ("FSF") in a back-contact solar cell. I discuss back-contact solar cells below in Section VII.C.2.

75. For other types of solar cell structures, the same concept applies, although the name of the front doped layer might be different. For example, in both-side-contacted solar cells, which I also discuss below in Section VII.C.1, this doped front region may be the emitter.

76. As early as 1978, FSFs were well known as a way to reduce recombination near the solar cell surface. Ex.1027-von Roos, 1119-1120; Ex. 1008-Marvin, 3. Numerous researchers have incorporated FSFs in solar cell devices over the years. *E.g.*, Ex.1028-van Kershaver, 112; Ex.1030-Swanson-352, 4:42-51; Ex.1021-King, 369; Ex.1017-Meier, 4:36-48, 5:43-6:2.

77. A FSF is created by doping a region near the substrate's surface above the background dopant concentration of the substrate. Ex.1027-von Roos, 1119-1120. This region is typically denoted as being p⁺ in a p-type solar cell (i.e., a solar cell with a p-type wafer), wherein the "+" indicates a higher dopant concentration than the p-type substrate. Similar notation is used for n-type solar cells.

78. The increased doping forms an electric field between the more heavily doped region of the semiconductor substrate and the rest of the substrate. The electric field forms an energetic barrier that inhibits one type of charge carrier (i.e., electrons or holes) from moving toward the recombination-active region near the front surface of the wafer. Ex.1027-von Roos, 1119. In this way, the FSF assists with moving charge carriers to the appropriate metal contacts to generate current. Ex.1027-von Roos, 1119. The likelihood increases of electrons reaching the negative metal contact and holes reaching the positive metal contact before they recombine, thereby increasing solar cell efficiency. Ex.1027-von Roos, 1119.

79. In addition, before the earliest possible priority date, it was well known that Auger recombination, a type of recombination I discussed in Section VII.B.1 above, limited FSF dopant concentrations. Specifically, researchers understood that FSF dopant concentrations above $1 \times 10^{18} \text{ cm}^{-3}$ induced Auger recombination, which in turn reduced solar cell efficiency. For example, a 1989 report, *Interdigitated Back*

Contact Silicon Solar Cell Analysis and Design Recommendations for Space Use, by Marvin et al. (which I discuss in more detail below in Section X.D), explained that “[t]he FSF effectiveness is relatively constant over a rather broad range around $1\text{E}17$ to $1\text{E}18\text{ cm}^{-3}$ ” and the effectiveness will “decreas[e]” if FSF dopant concentration is increased above $1\text{E}18\text{ cm}^{-3}$ “due to increased Auger recombination.” Ex.1008-Marvin, 15.

80. Numerous publications disclosed the desired dopant concentration in a region near the substrate’s surface was around $1\times 10^{18}\text{ cm}^{-3}$ due to Auger recombination effects. For example, a 1990 IEEE paper by King et al. explained:

Above $N_D \approx 10^{18}\text{ cm}^{-3}$, hole lifetime in the heavy phosphorus doped emitter should be dominated by band-to-band Auger recombination.

...

In the case of a back-contacted cell in which the sunside diffusion is used mainly to reduce surface recombination, not to collect current, the optimum emitter is the one with the lowest J_0 . For untextured surfaces, this corresponds an emitter with $N_{D, \text{ surf}} \approx 1\times 10^{18}\text{ cm}^{-3}$ that is as thin as possible. ... [A]n emitter with these specifications is probably near optimum in J_0 when it has a textured front surface, as well.

Ex.1021-King, 367, 369.³

81. As another example, a 1980 patent by Swanson et al. disclosed “an improved photovoltaic cell” and a fabrication process for such a cell that involves “dop[ing] N-type silicon substrate 50...[i.e.,] the bulk substrate material [at] 10^{14} dopant atoms per cubic centimeter or less.” Ex.1030-Swanson-352, 2:1-6, 4:42-45. That step of the fabrication process is shown in Figure 5:

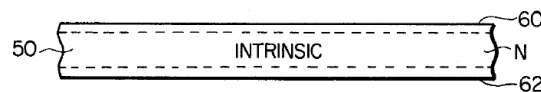
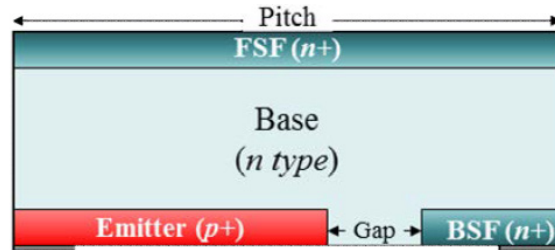


FIG_5

Ex.1030-Swanson-352, Fig.5. Diffused regions 60 and 62 are then formed on opposite sides of the wafer by diffusing N-type dopants into the wafer. Ex.1030-Swanson-352, 4:45-51. The maximum surface dopant concentration of the diffused regions 60 and 62 is 10^{18} atoms per cubic centimeter.” Ex.1030-Swanson-352, 4:45-51.

82. A 2014 IEEE publication by Procel et al. disclosed “a back-contact back-junction solar cell,” shown in Figure 1 below. Ex.1040-Procel, 1.

³ A person of ordinary skill in the art would have understood that the “emitter” described in this portion of King corresponds to the doped region near the substrate’s surface (i.e., front surface field) of a back-contact solar cell.



Ex.1040-Procel, 2, Fig.1. Procel discloses:

The doping profiles in back surface field (BSF), front surface field (FSF) and emitter are gaussian functions of the spatial coordinate featuring the peak located at the edge of the interface and junction depth of ... $0.5\mu\text{m}$ for FSF region. Peak concentration doping is ... $1\times 10^{18}\text{cm}^{-3}$ for FSF ...

Ex.1040-Procel, 1.

b. Gettering

83. It was known by the earliest possible priority date that wafer manufacturing and subsequent device fabrication on the wafer could introduce metal impurities into silicon-based semiconductor devices. For example, a 2000 publication by Istratov et al. described “iron contamination” “during [silicon wafer] device manufacturing” and the need for “removal of iron contamination from the wafers” by, *inter alia*, “gettering of iron.” Ex.1047-Istratov-2000, 491-493. It was also known that other transition metals such as copper, nickel, and titanium could be gettered. *Id.* at 489, 514. Gettering was only required in solar cells with significant metal impurity levels in the wafer.

84. Gettering was particularly relevant in the solar cell industry, which, as of the filing date of the '315 patent, oftentimes used lower grade silicon wafers.⁴ Ex.1077-Paudyal, 437 (“The Silicon photovoltaic (Si-PV) industry can suffer from poor manufacturing control of metal impurities in low cost directionally solidified or cast wafers making up > 85% of the capacity being delivered today.”); Ex.1078-Pizzini, 2928 (“The high areal costs of crystalline silicon modules comes today at least in part ($\approx 30\%$) from the cost of the Cz-grown silicon ingots and wafers, prepared using electronic grade (EG) silicon....For this reason, worldwide research efforts were spent in the last two decades, dedicated to the study ... of a kind of a low-grade silicon, called solar grade silicon, which could be adapted to solar cell fabrication, without loosing [sic] conversion efficiency.”).

85. By the early 1960s, gettering during fabrication was known to reduce the harmful effects of metal impurities in silicon-based semiconductor devices. Ex.1057-Stradins, 4 (“The higher bulk lifetime in the cell than that of a symmetric B-emitter (typically ~ 1.5 ms) suggests impurity gettering by n^+ poly-Si/SiO₂

⁴ This is not necessarily the case nowadays as the quality of silicon wafers has significantly improved since 2014 (the earliest possible priority date of the '315 patent).

layers.”); Ex.1060-Goetzberger, 1822-1824 (1960 paper about the removal or “gettering” of “[m]etal precipitates” “in Silicon p-n Junctions”); Ex.1061-Ing, 533-534 (“In the modern day manufacturing of diffused silicon devices [in the 1960s], one or more gettering steps are usually incorporated in the process to prevent introduction of undesirable metal impurities into the junction region or to remove any metal impurities that may be already there.”); Ex.1062-Mets, Abstract, 422-424 (1965 paper “describ[ing] the conditions by which fast diffusing metal impurities can precipitate within junction regions under certain high-temperature ambients”).

86. Application of gettering to solar cells devices, a type of silicon-based semiconductor device, was well known by the earliest possible priority date. It was well known that gettering would “enhance[] [solar] cell performance” in solar cells with significant metal impurity levels. Ex.1031-Bultman, 73. A 2002 publication by Perichaud described gettering in “crystalline silicon wafers” “to prepare solar cells.” Ex.1033-Perichaud, 315.

87. As another example, a 2010 paper by Bultman et al. described gettering impurities into “highly doped emitter regions,” which “may act as sinks for impurities” in solar cells. Ex.1031-Bultman, 72-73.

88. A 2012 patent publication assigned to Varian Semiconductor Equipment Associates, Inc. also disclosed gettering of “[m]etallic contaminants” such as iron into emitters of solar cells. Ex.1035-Gupta, [0037].

89. Gettering is a three-step process for moving metal impurities out of active regions of semiconductor devices such as solar cells. Ex.1033-Perichaud, 316-318. The 2002 paper by Perichaud about gettering in solar cells explains that, in the first step, metal impurities are released from their location in the semiconductor by heating the solar cell to a high temperature. Ex.1033-Perichaud, 316-318. In the second step, the newly mobile metal impurities diffuse through the semiconductor toward a front or back surface of the solar cell as the solar cell cools. Ex.1033-Perichaud, 316-318. In the third step, the mobile impurities are captured at a gettering trap site—often, but not always, a heavily-doped layer—where they cause less recombination. Ex.1033-Perichaud, 316-318.

90. It was well known by the earliest possible priority date that materials that are highly defective, such as polysilicon, make for good gettering trap sites for metal impurities, effectively acting as a sponge for impurities. Ex.1053-Nippon, 11-12, 16; Ex.1062-Mets, 422-424; Ex.1052-Lysacek, 1-2. Polysilicon is inherently a structurally defective material—that is, polysilicon has high defect density due to its

grain boundaries (interfaces between different lattice regions of the polysilicon) that heat treatment does not cure. Ex.1053-Nippon, 11-12; Ex.1025-Fonash, 10-11.

91. For solar cells with significant impurity levels, gettering was performed well before the earliest possible priority date to move metal impurities from the substrate into the emitter. For example, a 1995 patent assigned to NEC Corporation discloses that “silicon substrate 31 contains the contaminants 32,” which “are removed,” and “the lower polycrystalline silicon film 34b [is] utilized as a getter sink.” Ex.1032-Tokuyama, 9:60-10:49, Fig.10.

92. As another example, a 2010 paper by Bultman et al. teaches gettering impurities into “highly doped emitter regions,” which “may act as sinks for impurities” in solar cells. Ex.1031-Bultman, 72. Further, a 2012 patent application assigned to Varian Semiconductor teaches the gettering of “[m]etallic contaminants” such as iron into emitters of solar cells and states that “[a]nother benefit of having slightly higher dopant concentrations on the facets in close proximity with each other may be an improvement in gettering efficiency of the emitters.” Ex.1035-Gupta, [0037]; *see also* Ex.1033-Perichaud, 315-318.

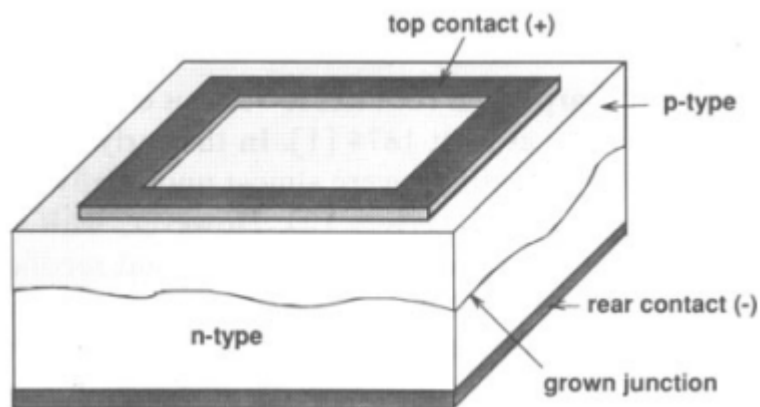
93. Higher doping of the emitter results in fewer opposite-type carriers because semiconductor physics dictates that, if one type of carrier increases in concentration, the other type of carrier decreases (in equilibrium). This effect is

captured by the equation $np = n_i^2$. Ex.1024-Pierret, 53-55. Because recombination can only occur when both an electron and hole are present, moving impurities to the emitter results in less recombination than if they were left elsewhere in the substrate.

C. Solar Cell Structures

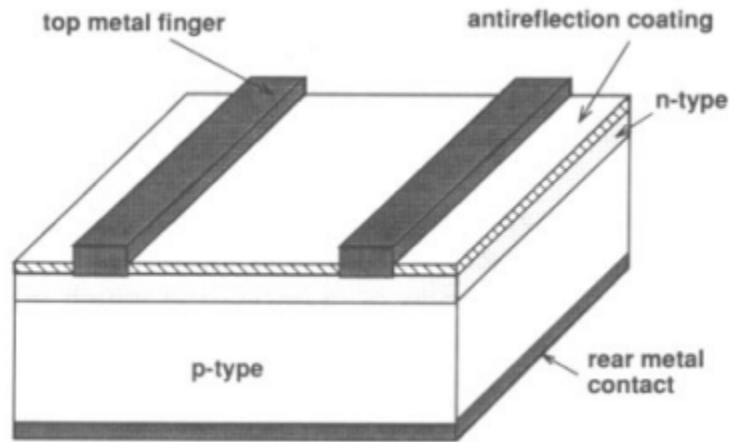
1. Both-Sides-Contacted Solar Cells

94. Solar cells having both front side and back side metal contacts (“both-sides-contacted” solar cells) were known well before the ’315 patent’s earliest possible priority date. A 1941 photovoltaic device (shown below) had both a top (i.e., front) contact and rear (i.e., back) contact with a “grown junction”—a PN junction formed from segregation of impurities during recrystallization of pure silicon after a heating process. Ex.1046-Green, 2.



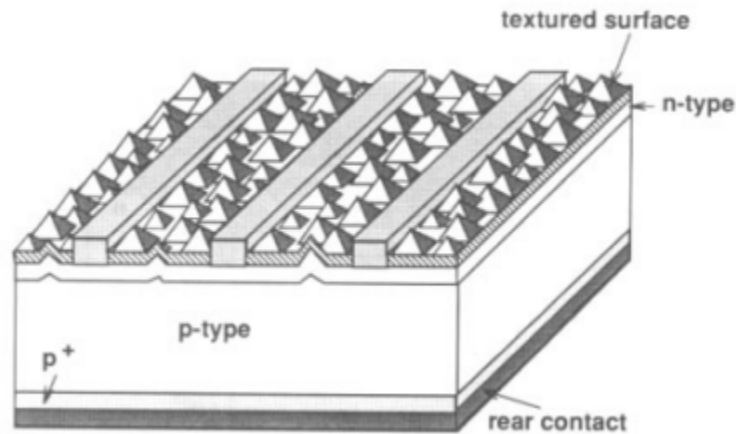
Ex.1046-Green, 2 (Fig.2). Efficiency was very low due to the lack of control over the junction formation. Ex.1046-Green, 2. Over time, technology improved, and more efficient solar cells were developed.

95. In the 1960s, solar cells for space applications had metal contacts on both the top and bottom surfaces as shown in the figure below. Example solar cell having the design below achieved efficiencies above 14%.



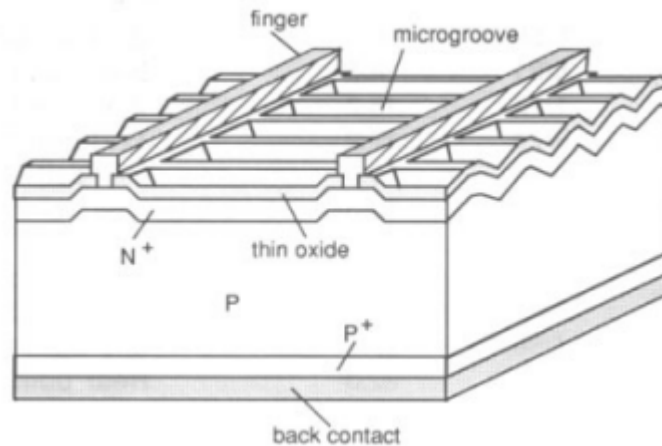
Ex.1046-Green, 2 (Fig.4).

96. In the 1970s, the next innovation in both-sides-contacted solar cells related to the observation that placing aluminum on the back side improved solar cell efficiency. Anti-reflection coatings were also added. These solar cells had approximately 17% efficiency. Ex.1046-Green, 3.



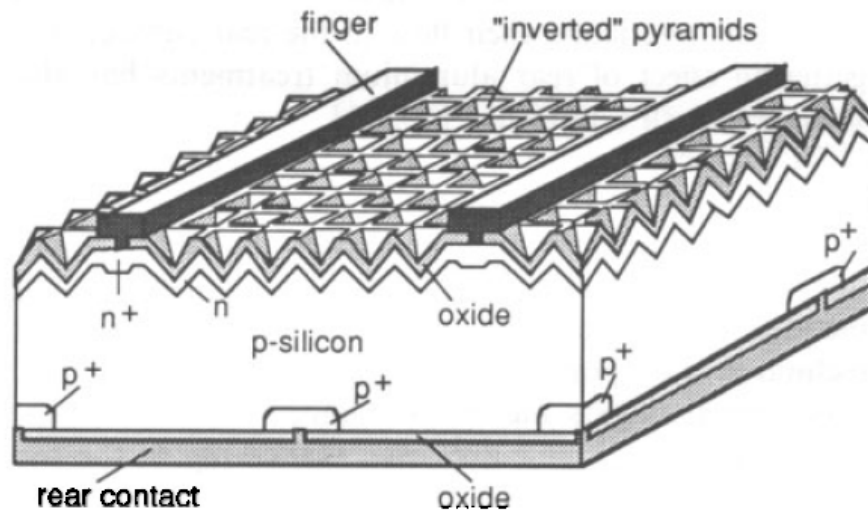
Ex.1046-Green, 3 (Fig.5).

97. In the mid-1980s, the passivated emitter solar cells (PESC), shown below, reduced the solar cell's top metal contact area and achieved 20% efficiency, which was considered the practically achievable efficiency limit of silicon solar cells at the time.



Ex.1046-Green, 3 (Fig.6).

98. The efficiency of the PESC solar cell was later surpassed in the 1990s by the passivated emitter, rear-locally diffused cell (PERL), which was able to achieve an efficiency above 23%. Ex.1046-Green, 4.



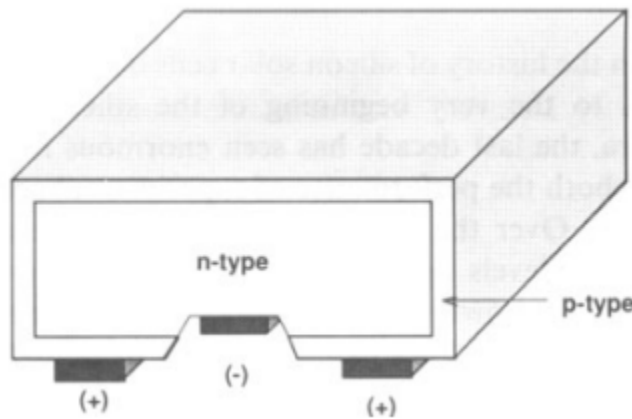
Ex.1046-Green, 4 (Fig.8). All these solar cells utilized a metal contact on the front surface and a metal contact on the back surface.

2. Back-Contact Solar Cells

99. Back-contact solar cells were known well before the earliest possible priority date of the '315 patent. Ex.1051-Lammert, 337-338; Ex.1010-Granek, 18. As I discussed in Section VII.C.1, both-sides-contacted solar cells have metal contacts on the front and back side. Back-contact solar cells have both polarities of metal contacts on the back side, as shown in the figure below, and necessarily have the PN junction on the back side. Ex.1010-Granek, 17; Ex.1008-Marvin, 3.

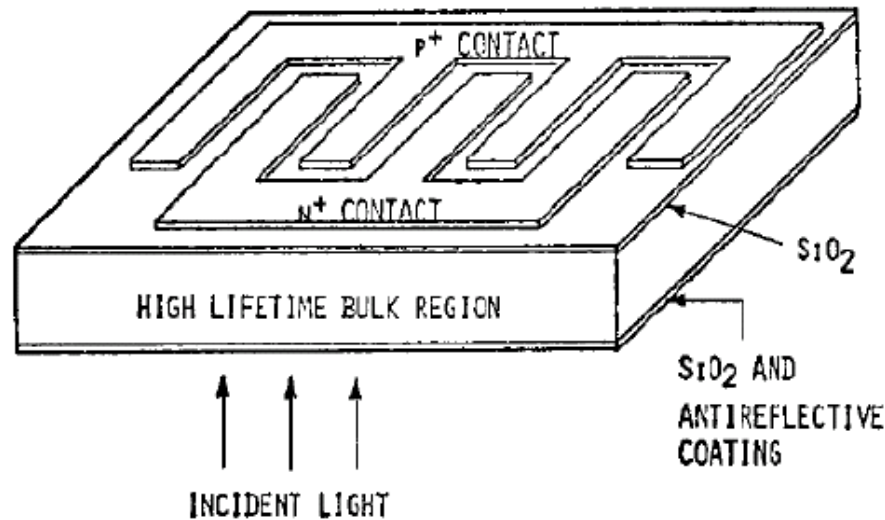
100. The main advantage of back-contact solar cells over both-sides-contacted solar cells is the elimination of light loss due to reflection away from the solar cell by the metal front contact (“shadowing”). Ex.1010-Granek, 17.

101. The “first modern solar cell” having “dual rear contact structure” with contacts of both polarities situated on the back was created in 1954, shown below:



Ex.1046-Green, 2 (Fig.3).

102. The idea for the interdigitated back-contact (“IBC”) solar cell (shown below) was known as early as 1977. Ex.1051-Lammert, 337-338. Since then, numerous researchers have sought to improve upon it. *See, e.g.*, Ex.1019-Verlinden; Ex.1020-Sinton; Ex.1021-King; Ex.1022-Mulligan.



Ex.1051-Lammert, Fig.1.

103. IBC solar cells are a type of back-contact solar cell having interdigitated negative and positive polarity metal contacts, as shown in the figure above.

Ex.1051-Lammert, Fig.1; Ex.1008-Marvin, 3-4.

VIII. OVERVIEW OF THE '315 PATENT

A. Summary of the '315 Patent

104. The '315 patent describes two concepts that were known to improve the efficiency of solar cells by reducing recombination, which I discussed in Section VII.B. First, to reduce recombination near the surface, the '315 patent describes creating a doped layer at the front side of the solar cell. Ex.1001-USP315, 4:55-64 ("a dopant region 216 can be formed on a surface 204 of silicon substrate 202...to dope the surface 204 ... to repel charge carriers and prevent and/or reduce

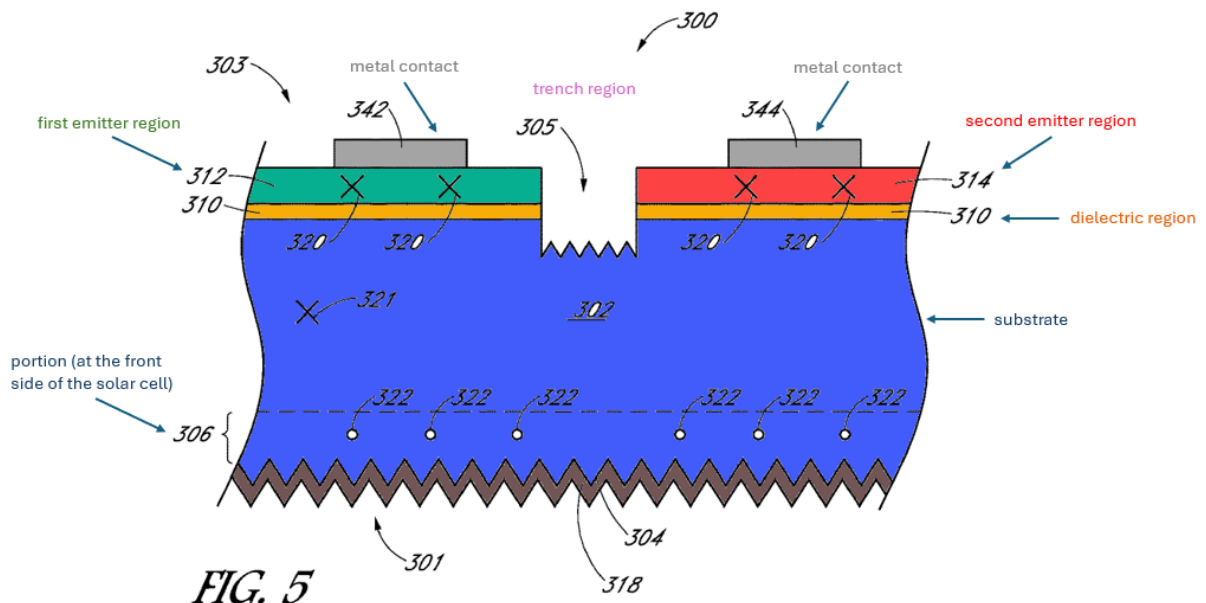
recombination at the surface 204 of the solar cell,” and the dopant region 216 formed on the “surface 204, can be on a front side ... of the solar cell”), Fig. 2. The doped layer at the front side has a higher dopant concentration than the background doping concentration of the substrate. Ex.1001-USP315, 4:15-24 (“[A] heating process can be performed to drive dopants into a portion of the silicon substrate. In an embodiment, the portion of the silicon substrate can have a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ after the heating process[.]”). I discussed such surface passivation techniques for reducing carrier recombination in Section VII.B.2.a.

105. Second, to reduce recombination caused by metal impurities in the substrate, the patent describes a heating process that getters metal impurities into the emitter region of the solar cell. Ex.1001-USP315, 5:1-5 (“Metal impurities can be detrimental to the electrical conduction of the solar cell as these impurities can be sources of recombination, resulting in poor lifetime, surface passivation and/or lower solar cell efficiency.”). That is, the heating process causes the metal impurities to migrate from the substrate of the solar cell to the emitter, where they do not cause—or cause less—recombination, thereby improving solar cell lifetime and efficiency. Ex.1001-USP315, 5:10-25 (“A gettering process can be used to trap the metal impurities 220 in the emitter regions 212, reducing recombination within the silicon

substrate 202 and improving overall solar cell lifetime.”). I discussed gettering of metal impurities in Section VII.B.2.b.

1. Solar Cell Structure of Claims 10-20

106. The configuration recited in claims 10-20 is depicted in Figure 5 of the '315 patent, annotated below.



Ex.1001-USP315, Fig.5 (annotated).

107. Figure 5 of the '315 patent shows a solar cell (300) “hav[ing] a front side 301 [that] faces the sun...and a back side 303 opposite the front side 301.” Ex.1001-USP315, 6:40-49, Fig.5. The solar cell 300 has a silicon substrate 302 (blue). Ex.1001-USP315, 6:40-49, Fig.5. The silicon substrate 302 has a portion 306 at the front side of the solar cell with “a dopant concentration 322 of

approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$.” Ex.1001-USP315, 6:40-49, Fig.5. Figure 5 also shows a dielectric region 310 (orange) formed over the silicon substrate 302, first emitter region 312 (green) and second emitter region 314 (red) formed over the dielectric region, and metal contacts 342, 344 (gray) formed over the first emitter region 312 and second emitter region 314. Ex.1001-USP315, 6:50-62. The first emitter region 312 and second emitter region 314 can be doped either p-type and n-type or vice versa. Ex.1001-USP315, 6:50-62. A person of ordinary skill in the art would have understood that the first emitter region 312 and second emitter region 314 are oppositely doped, else the solar cell would not generate electricity. A trench region 305 (purple) separates the first emitter region 312 from second emitter region 314. Ex.1001-USP315, 6:65-67.

108. Regarding the first emitter region 312 (green) and second emitter region 314 (red), the '315 patent teaches “an emitter region can be a doped region of a solar cell for collecting positive and negative charge carriers.” Ex.1001-USP315, 2:40-42. Further, “the emitter region can be a doped polysilicon region” and “can be a P-type doped polysilicon region or an N-type doped polysilicon region.” Ex.1001-USP315, 2:42-46. In the embodiment disclosed in Figure 5, the substrate and “second emitter region” are n-type, and the “first emitter region” is p-type. Ex.1001-USP315, 6:40-57.

109. Figure 5 of the '315 patent also shows that the front surface of the solar cell can be textured to improve light absorption. Ex.1001-USP315, 7:1-6. Moreover, the solar cell may have an **anti-reflective coating 318 (brown)**. Ex.1001-USP315, 7:6-12.

2. Example Processes A-D

110. The '315 patent purports to improve the efficiency of a solar cell by (1) doping “a surface, or a portion near the surface” of the solar cell at approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$, and (2) gettering metal impurities into the emitter at a temperature above 900° Celsius. Ex.1001-USP315, 8:40-45.

111. This purported gain in efficiency is described in the '315 patent through a purported series of experiments. Ex.1001-USP315, 8:35-50, Fig.11 (showing results for Example Processes A-D). In those experiments, the '315 patent varies two process parameters: dopant concentration in a region near the substrate's surface and temperature (which purportedly affects the ability to getter impurities into the emitter of the solar cell). Ex.1001-USP315, 8:35-50, Fig.11 (figure 11 is “a table” showing the temperature and dopant concentration used in each Example Process and the corresponding output results). The two processing parameters and the purported results from the experiments (“Gettering Location,” “Surface

Passivation,” “Lifetime,” and “Efficiency”) are summarized in Figure 11 of the ’315 patent (shown below). Ex.1001-USP315, 8:35-50, Fig.11.⁵

⁵ Figure 11 appears to contain typographical errors. The second column (“Temp”) of Figure 11 shows Example Processes C and D occurring at temperatures of less than or equal to 900° Celsius, while the corresponding description in the ’315 patent states Example Processes C and D are both “heated to a temperature above 900 degrees Celsius.” Ex.1001-USP315, 8:40-45, 9:1-9. Fig.11. The specification also states that the result from Example Processes C and D was successful “gettering in a polysilicon region of the silicon substrate,” which Figure 11 confirms, and that “heating at temperature at 900 degrees Celsius or below can be insufficient to diffuse metal impurities through a tunnel oxide and into a polysilicon region.” Ex.1001-USP315, 5:18-25. A person of ordinary skill in the art would have understood Example Processes C and D as “heated to a temperature above 900 degrees Celsius” given the disclosure in the ’315 patent specification. Ex.1001-USP315, 8:40-45, 9:1-9.

Example Process	Temp	Surface Dopant Conc.	Gettering Location	Surface Passivation	Lifetime	Efficiency
A	≤ 900 deg-C	$2 \times 10^{18} \text{ cm}^{-3}$	non-poly	2 fA/cm^2	$\sim 3 \text{ msec}$	Baseline
B	≤ 900 deg-C	$4 \times 10^{18} \text{ cm}^{-3}$	non-poly	5 fA/cm^2	$\sim 10 \text{ msec}$	Baseline
C	≤ 900 deg-C	$2 \times 10^{18} \text{ cm}^{-3}$	poly	2 fA/cm^2	$\sim 10 \text{ msec}$	+0.5 % abs.
D	≤ 900 deg-C	$4 \times 10^{18} \text{ cm}^{-3}$	poly	5 fA/cm^2	$\sim 10 \text{ msec}$	Baseline

Table 1. Example Processes for Solar Cell Fabrication

FIG. 11

Ex.1001-USP315, Fig.11.

112. In Example Processes A and B (highlighted below), the solar cells were heated to a temperature of *less than or equal to* 900° Celsius, which purportedly failed to getter metal impurities in the polysilicon emitter. Ex.1001-USP315, 8:51-67 (“[T]he solar cell[s] of Example Process A [and Example Process B] [were] heated to a temperature below 900 degrees Celsius resulted in gettering in a non-polysilicon region of the solar cell”). Figure 11 indicates the purported failure to getter metal impurities into the polysilicon emitter with the “non-poly” result in the “Gettering Location” column. Ex.1001-USP315, Fig.11. As indicated by the “Baseline” result in the “Efficiency” column of Figure 11, purported efficiency improvements that would be achieved by gettering were not realized in Example Processes A and B, and the specification states that there was “no

considerable...efficiency increase from the baseline.” Ex.1001-USP315, 8:51-67, Fig.11; *see above* Section VII.B.2.b.

Example Process	Temp	Surface Dopant Conc.	Gettering Location	Surface Passivation	Lifetime	Efficiency
A	≤ 900 deg-C	$2 \times 10^{18} \text{ cm}^{-3}$	non-poly	2 fA/cm^2	$\sim 3 \text{ msec}$	Baseline
B	≤ 900 deg-C	$4 \times 10^{18} \text{ cm}^{-3}$	non-poly	5 fA/cm^2	$\sim 10 \text{ msec}$	Baseline
C	≤ 900 deg-C	$2 \times 10^{18} \text{ cm}^{-3}$	poly	2 fA/cm^2	$\sim 10 \text{ msec}$	+0.5 % abs.
D	≤ 900 deg-C	$4 \times 10^{18} \text{ cm}^{-3}$	poly	5 fA/cm^2	$\sim 10 \text{ msec}$	Baseline

Table 1. Example Processes for Solar Cell Fabrication

Ex.1001-USP315, Fig.11 (annotated).

113. Conversely, in Example Processes C and D, in which the solar cells were “heated to a temperature *above* 900 degrees Celsius,” gettering into the polysilicon emitter was purportedly successful. Ex.1001-USP315, 8:40-50, 9:1-9, Fig.11. Figure 11 shows the metal impurities were gettered into the polysilicon emitter with the “poly” result in the “Gettering Location” column. Ex.1001-USP315, Fig.11. The specification states that Example Processes C and D “resulted [in] gettering in a polysilicon region of the silicon substrate.” Ex.1001-USP315, 8:40-50, 9:1-9.

114. Moreover, Example Processes B and D used a dopant concentration of “approximately $4 \times 10^{18} \text{ cm}^{-3}$,” whereas Example Processes A and C used a dopant

concentration of “approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$.” Ex.1001-USP315, 8:40-9:9, Fig.11.

Example Process	Temp	Surface Dopant Conc.	Gettering Location	Surface Passivation	Lifetime	Efficiency
A	≤ 900 deg-C	$2 \times 10^{18} \text{ cm}^{-3}$	non-poly	2 fA/cm^2	$\sim 3 \text{ msec}$	Baseline
B	≤ 900 deg-C	$4 \times 10^{18} \text{ cm}^{-3}$	non-poly	5 fA/cm^2	$\sim 10 \text{ msec}$	Baseline
C	≤ 900 deg-C	$2 \times 10^{18} \text{ cm}^{-3}$	poly	2 fA/cm^2	$\sim 10 \text{ msec}$	+0.5 % abs.
D	≤ 900 deg-C	$4 \times 10^{18} \text{ cm}^{-3}$	poly	5 fA/cm^2	$\sim 10 \text{ msec}$	Baseline

Table 1. Example Processes for Solar Cell Fabrication

FIG. 11

Ex.1001-USP315, Fig.11 (annotated).

115. The '315 patent specification states that for Example Processes B and D, “no considerable” “efficiency increase from the baseline” was realized. Ex.1001-USP315, 8:60-67, 9:1-9, Fig.11. In particular, in Example Processes A and C, which used the lower dopant concentration of $2 \times 10^{18} \text{ cm}^{-3}$, the saturation current density (J_0) was only 2 fA/cm^2 . In Example Processes B and D, when the dopant concentration was increased to “approximately $4 \times 10^{18} \text{ cm}^{-3}$,” the J_0 suffered an increase to 5 fA/cm^2 . Ex.1001-USP315, 8:40-9:9, Fig.11.

116. Example Process C (shown below), which heated the solar cell “to a temperature above 900 degrees Celsius” and doped “a surface, or a portion near the surface, of a silicon substate...at approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$,” realized an “efficiency increase” of “+0.5%” as compared to the other Example Processes. Ex.1001-USP315, 8:40-50, Fig.11.

Example Process	Temp	Surface Dopant Conc.	Gettering Location	Surface Passivation	Lifetime	Efficiency
A	≤ 900 deg-C	$2 \times 10^{18} \text{ cm}^{-3}$	non-poly	2 fA/cm^2	$\sim 3 \text{ msec}$	Baseline
B	≤ 900 deg-C	$4 \times 10^{18} \text{ cm}^{-3}$	non-poly	5 fA/cm^2	$\sim 10 \text{ msec}$	Baseline
C	≤ 900 deg-C	$2 \times 10^{18} \text{ cm}^{-3}$	poly	2 fA/cm^2	$\sim 10 \text{ msec}$	+0.5 % abs.
D	≤ 900 deg-C	$4 \times 10^{18} \text{ cm}^{-3}$	poly	5 fA/cm^2	$\sim 10 \text{ msec}$	Baseline

Table 1. Example Processes for Solar Cell Fabrication

Ex.1001-USP315, Fig.11 (annotated).

B. Prosecution History

117. I understand that U.S. Patent Application No. 16/877,255 (“’255 Application” or Ex.1002-USP315FH) issued as the ’315 patent. Ex.1001-USP315, Cover (21). I also understand that the ’255 Application was filed on May 18, 2020. Ex.1001-USP315, Cover (22).

118. Further, I understand that the ’255 Application is a continuation of U.S. Patent Application No. 16/228,165 (“’165 Application” or Ex.1039-USPA165FH),

which is a division of U.S. Patent Application No. 15/876,927 (“’927 Application” or Ex.1038-USPA927FH), which is a continuation of U.S. Patent Application No. 15/213,273 (“’273 Application” or Ex.1037-USPA273FH), which is a continuation of U.S. Patent Application No. 14/579,935 (“’935 Application” or Ex.1036-USPA935FH). Ex.1001-USP315, Cover, (60). The ’935 Application was filed on December 22, 2014. Ex.1001-USP315.

119. The same Examiner—Examiner Long K. Tran—reviewed all five of these applications. *E.g.*, Ex.1001-USP315, Cover; Ex.1036-USPA935FH, 60-61; Ex.1037-USPA273FH, 63-64; Ex.1038-USPA927FH, 159-161; Ex.1039-USPA165FH, 82-87.

120. I understand that the Examiner allowed the claims of the ’255 Application without any rejection under 35 U.S.C. § 102 and/or 103 over any reference. *See generally* Ex.1002-USP315FH. In the Notice of Allowance, the Examiner stated that:

[N]one of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach *[sic]*:

...

portion of the silicon substrate is formed at the front side of the solar cell; a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of solar; a first emitter region having metal impurities formed over the dielectric region as recited in the independent claim 10.

Ex.1002-USP315FH, 207.

121. Based on my review of the prosecution histories of the '255 Application, '165 Application, '927 Application, '273 Application, and '935 Application and my review of the prior art that I discuss in Section X, I understand that the Examiner was unaware that prior art existed disclosing each of these limitations. The Examiner did not consider Choi, Granek, Marvin, Istratov, or Smith during prosecution of the '255 Application, '165 Application, '927 Application, '273 Application, or '935 Application.

122. The Examiner's search history for the parent '935 Application included Cousins, but he made no reference to the contents of Cousins during prosecution of the '255 Application, '165 Application, '927 Application, '273 Application, or '935 Application. Ex.1036-USPA935FH, 185-187. The Examiner did not address the substance of Cousins during prosecution of any of the five applications.

IX. CLAIM CONSTRUCTION

123. I was informed and I understand that the words used in the patent's claims and the context in which the words are used in the claims are highly relevant to determine a word's meaning. I also understand that the words of a claim are to be interpreted in the context of the entire patent. This includes the patent's claims, its specification, and its figures.

124. For the “approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ ” limitation of claim 10, the description in the ’315 patent specification of “approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ ” is informative to its meaning. As I explain above in Section VIII.A.2, the ’315 patent specification describes an Example Process C that, due to the processing parameters utilized, realized the highest efficiency increase as compared to the other Example Processes. Ex.1001-USP315, 8:35-50, Fig.11. In Example Process C, “a surface, or a portion near the surface, of a silicon substrate was doped at approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$.” Ex.1001-USP315, 8:40-45. Meanwhile, Example Processes B and D used a dopant concentration of approximately $4 \times 10^{18} \text{ cm}^{-3}$, and “no considerable” “efficiency improvement” was realized. Ex.1001-USP315, 8:60-9:9, Fig.11. The specification therefore teaches that “approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ ” cannot encompass a dopant concentration as high as $4 \times 10^{18} \text{ cm}^{-3}$.

125. I have been further instructed that a patent’s prosecution history (also called the file history) may provide helpful evidence about how the U.S. Patent and Trademark Office and the applicant understood the patent and its claims. Therefore, I have been instructed that claims should also be interpreted with the patent’s prosecution history in mind.

126. I have also been instructed that “extrinsic evidence” (such as pertinent scientific or technical references or dictionaries) may also help inform how a person of ordinary skill in the art would have understood a claim term. I have been instructed that extrinsic evidence must always be considered with intrinsic evidence.

127. I have applied these instructions in this declaration. If Patent Owner proposes an express claim construction in this proceeding or in another proceeding involving the patent, I reserve the right to respond to that construction. I also reserve the right to propose an express construction if one is needed.

X. OVERVIEW OF THE ASSERTED PRIOR ART

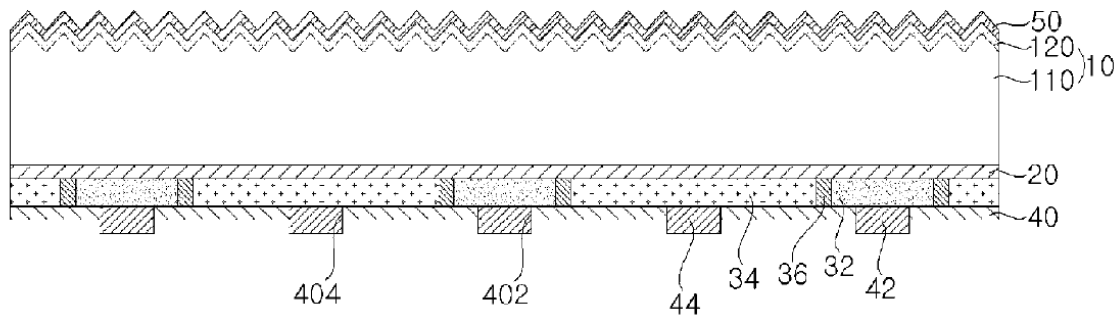
128. Before discussing the specific grounds, I provide below a brief overview of the references in the grounds.

A. Choi

129. Choi describes a solar cell “which is capable of improving reliability and maximizing efficiency.” Ex.1006-Choi, [0007]. Specifically, Choi teaches a solar cell structure that is commonly referred to as an interdigitated back-contact, or IBC, solar cell. The solar cell of Choi has a front side that faces the sun (as shown by the top, textured side in the following Figure 1 of Choi) and a back side opposite the front side. Ex.1006-Choi, Figs.1, 3k.

FIG. 1

100



Ex.1006-Choi, Fig.1.

130. A person of ordinary skill in the art would have understood that the textured surface is the front side of the solar cell that faces the sun during normal operation. For example, as explained in Choi, the front surface of a solar cell can be textured to reduce reflection of incident light, thus increasing the efficiency of the solar cell. Ex.1006-Choi, [0027].

131. Choi's solar cell includes the same layers recited in independent claim 10 of the '315 patent. Choi's solar cell 100 comprises a semiconductor substrate 10 that may be formed of a "crystalline semiconductor (for example, crystalline silicon) containing a first conductive-type dopant." Ex.1006-Choi, [0023], [0025], Figs.1, 3k. Choi explains that the "first conductive-type dopant" can be either "n-type"—in which case the substrate is doped with a Group V element (or "impurity") such as "phosphorous (P), arsenic (As), bismuth (Bi), antimony (Sb)"—or "p-type"—in

which case the substrate is doped with a Group III element such as “boron (B), aluminum (Al), gallium (Ga), indium (In).” Ex.1006-Choi, [0025].

132. Choi teaches a “front surface field layer 120.” As its name indicates, the front surface field layer 120 is formed at the front side of the solar cell 100. Ex.1006-Choi, [0029], Figs.1, 3k. The front surface field layer of Choi “is an area where the first conductive-type dopant is doped at a concentration higher than the semiconductor substrate 10.” Ex.1006-Choi, [0029], Figs.1, 3k. Choi explains that the front surface field “performs similar functions to a back surface field (BSF) layer.” Ex.1006-Choi, [0029]. Specifically, “the front surface field layer 120 prevents electrons and holes separated by incident light from being recombined and then decay on the front surface of the semiconductor substrate 10.” Ex.1006-Choi, [0029].

133. Choi also teaches “a tunneling layer 20.” The tunneling layer 20 of Choi “may include a variety of materials enabling tunneling of carriers and examples of the materials include oxides, nitrides and conductive polymers.” Ex.1006-Choi, [0033]. Choi teaches that the tunneling layer 20 “may be entirely formed on the back surface of the semiconductor substrate 10.” Ex.1006-Choi, [0033], Figs.1, 3k. Choi teaches that “[t]he tunneling layer 20 improves interface properties of the back

surface of the semiconductor substrate 10 and enables produced carriers to be efficiently transferred through tunneling effect.” Ex.1006-Choi, [0033].

134. Choi further teaches a first conductive type area 32 and a second conductive type area 34. The first conductive type area 32 and the second conductive type area 34 are “formed on the tunneling layer 20.” Ex.1006-Choi, [0023], [0035], Figs.1, 3k. Choi explains that “[t]he first conductive type area 32 may include a semiconductor (for example, silicon) having the same conductive type as the semiconductor substrate 10.” Ex.1006-Choi, [0036], Figs.1, 3k. The first conductive type area 32 “forms a back surface field structure and thereby functions to prevent carrier loss through recombination on the surface of the semiconductor substrate 10.” Ex.1006-Choi, [0036]. Moreover, Choi explains that “[t]he second conductive type area 34 may include a semiconductor (for example, silicon) having a conductive type opposite to the semiconductor substrate 10.” Ex.1006-Choi, [0037], Figs.1, 3k. As a result, the second conductive type area 34 “forms a tunnel junction with the semiconductor substrate 10 through the tunneling layer 20.” Ex.1006-Choi, [0037], Figs.1, 3k.

135. Like with the semiconductor substrate 10, Choi explains that the “first conductive type dopant” and the “second conductive type dopant” can be an “n-type dopant” or a “p-type dopant.” Ex.1006-Choi, [0036]-[0037]. If the first conductive

type dopant or the second conductive type dopant is an n-type dopant, the corresponding conductive type area is doped with a “Group V element such as phosphorus (P), arsenic (As), bismuth (Bi) or antimony (Sb).” Ex.1006-Choi, [0036]-[0037]. If the first conductive type dopant or the second conductive type dopant is a p-type dopant, the corresponding conductive type area is doped with a “Group III element such as boron (B), aluminum (Al), gallium (Ga) or indium (In).” Ex.1006-Choi, [0036]-[0037].

136. Choi teaches “first and second electrodes 42 and 44 which are connected to first and second conductive type areas 32 and 34, respectively” and “collect produced carriers and transport the same to the outside.” Ex.1006-Choi, [0023], [0044], Figs.1, 3k.

B. Cousins

137. Cousins teaches a bipolar, both-sides-contacted solar cell having a front side that faces the sun during normal operation to collect solar radiation and a back side opposite to the front side. Ex.1007-Cousins, 2:31-38, Fig.1.

2:49-55, Fig.1. Cousins teaches that the doped region 105 may be an n-type doped region that “may have a sheet resistance of 100 to 500 $\Omega/\text{sq.}$ ” Ex.1007-Cousins, 2:49-55.

140. At the back side, opposite to the front side, Cousins teaches a “thin dielectric layer 107” that “may comprise silicon dioxide thermally grown to a thickness of about 10 to 50 Angstroms on the back side surface of the substrate 101.” Ex.1007-Cousins, 3:12-20, Fig.1.

141. Cousins further teaches a “polysilicon layer 108 [] formed on [the] thin dielectric layer 107.” Ex.1007-Cousins, 3:12-13, Fig.1. The polysilicon layer 108 forms a back side junction with the substrate 101. Ex.1007-Cousins, 2:39-42 (“the solar cell 100 includes a backside junction formed by a P-type doped polysilicon layer 108 serving as a P-type diffusion region and the N-type silicon substrate 101 serving[] as an N-type diffusion region”). Cousins teaches that the polysilicon layer 108 may have an “emitter saturation current of about 10 $\text{fA}\cdot\text{cm}^{-2}$.” Ex.1007-Cousins, 2:42-44.

142. Cousins teaches a “metal contact 110” that “electrically connects to the polysilicon layer 108 through contact holes 123.” Ex.1007-Cousins, 3:20-24.

C. Granek

143. Granek studies “high-efficiency back-contact back-junction (BC-BJ) silicon solar cells for one-sun applications.” Ex.1010-Granek, Abstract. Granek uses “back-contact back-junction (BC-BJ) silicon solar cells” as another name for “Interdigitated Back-Contact (IBC) solar cells.” Ex.1010-Granek, 17 (IBC “solar cells ... have both contacts and the connection junction placed on the back side of the cell”). Granek states that recombination and other processes reduce “the cell efficiency” of IBC solar cells. Ex.1010-Granek, Abstract, 13 (listing “recombination losses” as one of the “[f]our main loss mechanisms” “on the cell efficiency”).

144. Granek studies the “[p]ositive effects of the phosphorus doped n+ front surface field (FSF) on the performance of” IBC solar cells. Ex.1010-Granek, Abstract. Granek analyzes the performance of solar cells having different FSF diffusion profiles. Ex.1010-Granek, 14, 117 (analyzing “different phosphorus-doped front surface field diffusion profiles”).

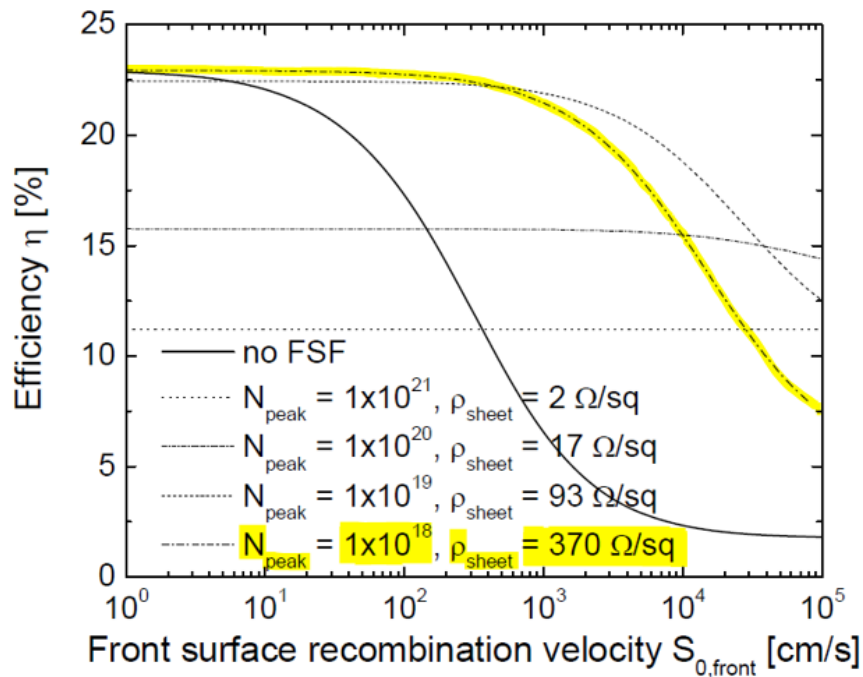
145. Granek teaches that “a low front surface recombination [] is one of the critical factors influencing the efficiency of the back-junction cell type.” Ex.1010-Granek, 117. “A lowly doped FSF results in high quantum efficiency” because “Auger recombination inside the highly doped region and the surface recombination velocity are low.” Ex.1010-Granek, 120. Granek then concludes that “[a] proper

choice of the front surface field profile is therefore one of the most critical points in the design of the back-contact, back-junction solar cell device.” Ex.1010-Granek, 120.

146. Granek simulates solar cells with FSF dopant concentrations ranging from 1×10^{18} to $1 \times 10^{21} \text{ cm}^{-3}$ and shows that the solar cell having a FSF with a dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ had the highest efficiency. Ex.1010-Granek, 120-122; *see* Ex.1010-Granek, 184 (N_{peak} is the peak dopant concentration of the FSF in cm^{-3}).⁶

147. In Figure 7-1, Granek shows the “[i]nfluence of the front surface recombination velocity [] on the efficiency of the back-junction n-type Si solar cells with different phosphorus FSF diffusion profiles.” Ex.1010-Granek, 121.

⁶ Granek uses the PC1D simulator that is commonly used in the solar cell research community and widely accepted as accurate. Ex.1010-Granek, 120.

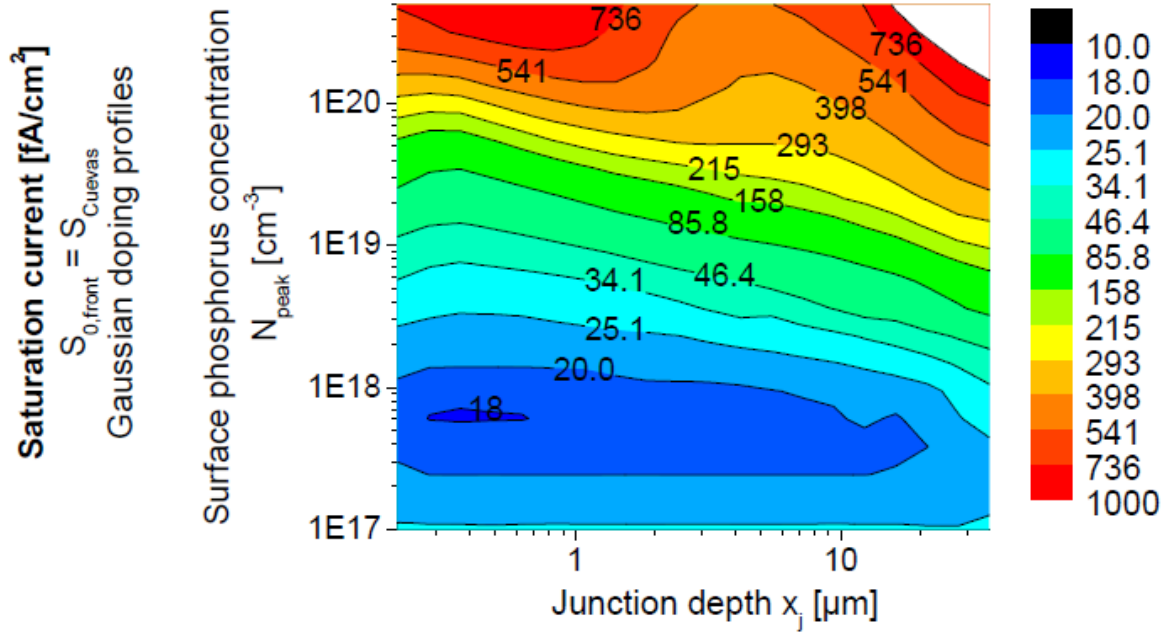


Ex.1010-Granek, 121, Fig.7-1 (annotated). As shown in Figure 7-1, the simulated solar cell's efficiency is highest when the FSF dopant concentration is $1 \times 10^{18} \text{ cm}^{-3}$. Specifically, Figure 7-1 of Granek shows that the simulated solar cell's efficiency is highest when the FSF dopant concentration is $1 \times 10^{18} \text{ cm}^{-3}$ when the front surface recombination velocity of the solar cell is moderate or low. Ex.1010-Granek, 121, Fig.7-1.

148. As a person of ordinary skill in the art would have understood, front surface recombination velocity of a solar cell is low when the surface of the solar cell is well passivated. Indeed, Granek states that “for the well passivated surfaces, an optimal diffusion profile is lowly doped and shallow.” Ex.1010-Granek, 123. This is particularly the case for solar cells like the ones described by Choi and

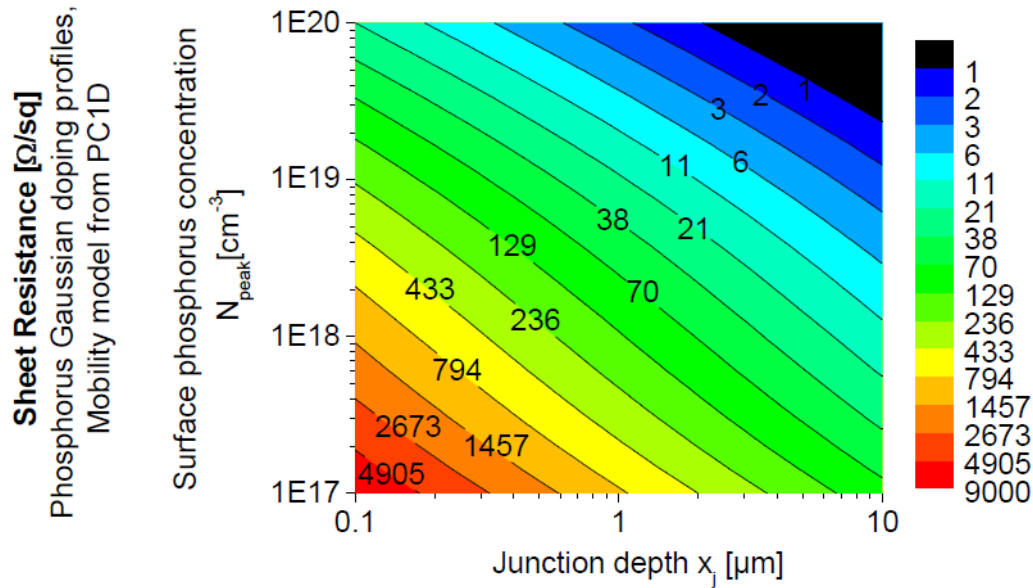
Cousins, which have a dielectric passivation layer on the front surface of the substrate.

149. Figure 7-3 shows simulated saturation current density as a function of FSF dopant concentration (vertical axis) and junction depth (horizontal axis). Saturation current density is a metric of recombination in the solar cell, with larger values indicating more recombination. As shown in the figure, as the FSF dopant concentration (N_{peak}) decreases, the saturation current density decreases from the higher red-orange values at $1E20\text{ cm}^{-3}$ (i.e., $1 \times 10^{20}\text{ cm}^{-3}$) to the lowest values in dark blue of approximately $1E18\text{ cm}^{-3}$ (i.e., $1 \times 10^{18}\text{ cm}^{-3}$).



Ex.1010-Granek, 122 (Fig.7-3). Granek demonstrates that the simulated solar cell's recombination level is lowest when the FSF dopant concentration is approximately $1 \times 10^{18} \text{ cm}^{-3}$.

150. In Figure 7-4, Granek shows the sheet resistance as a function of N_{peak} and diffusion depth (assuming a Gaussian diffusion):



Ex.1010-Granek, 123 (Fig.7-4).

151. Granek also describes experimental results in which solar cells were fabricated to study the effect various FSF dopant concentration levels have on solar cell performance. Ex.1010-Granek, 124-126, 131 (IBC “n-type silicon solar cells were processed with different FSF diffusion profiles. Thus, the influence of the FSF profile on the solar cell performance could be analyzed.”).

152. Of the fabricated solar cells, the best performing one (FSF5) had the lowest FSF doping level, as shown in Tables 7-1 and 7-5 below. Ex.1010-Granek, 126, 131-132. The solar cell with the FSF5 profile has a FSF dopant concentration of $3.8 \times 10^{18} \text{ cm}^{-3}$. Ex.1010-Granek, 126, 184 (N_s is “surface doping concentration” in “ cm^{-3} ”).

Profile	Type	ρ_{sheet} [Ω/sq]	N_s [cm^{-3}]	x_j [μm]
FSF1	erfc	32	6.0×10^{20}	0.78
FSF2	erfc	73	4.0×10^{20}	0.66
FSF3	erfc	96	3.2×10^{20}	0.56
FSF4	erfc	353	4.5×10^{19}	0.38
FSF5	Gauss	148	3.8×10^{18}	1.44

Ex.1010-Granek, 126 (Table 7-1) (annotated).

Cell no.	FSF Profile	Type	ρ_{sheet} [Ω/sq]	J_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	η [%]
BC47-2b	FSF2	erfc	73	34.1	647	81.7	18.0
BC47-6b	FSF3	erfc	96	36.1	657	81.9	19.5
BC47-11b	FSF4	erfc	353	37.8	651	81.1	20.0
BC47-16b	FSF5	Gauss	148	38.1	663	82.3	20.8
BC47-22b	no FSF	-	-	36.4	659	82.0	19.7

Ex.1010-Granek, 132 (Table 7-5) (annotated). Granek concludes that “[t]he highest efficiency of 20.8% was achieved on ... deep diffused (FSF5).” Ex.1010-Granek, 131, 141 (“The best solar cell efficiency of 20.8 % was obtained with deep diffused Gaussian profile of the FSF.”).

153. Although Granek did not experimentally analyze a solar cell having a FSF dopant concentration of $1.0 \times 10^{18} \text{ cm}^{-3}$, Granek’s experimental results validate the simulation results. Based on my own experience, it is difficult to predict the final dopant concentration of a semiconductor layer when performing an experiment

varying diffusion conditions, and Granek does not explain why lower dopant concentrations were not studied experimentally. Although Granek's experiment resulted in an FSF dopant concentration of $3.8 \times 10^{18} \text{ cm}^{-3}$, Granek's experimental results validate his simulation results that a low FSF dopant concentration is desirable. Moreover, a person of ordinary skill in the art, looking at both Granek's simulation results and experimental results in conjunction, would have expected that a FSF dopant concentration of about $1.0 \times 10^{18} \text{ cm}^{-3}$ would have achieved a higher efficiency.

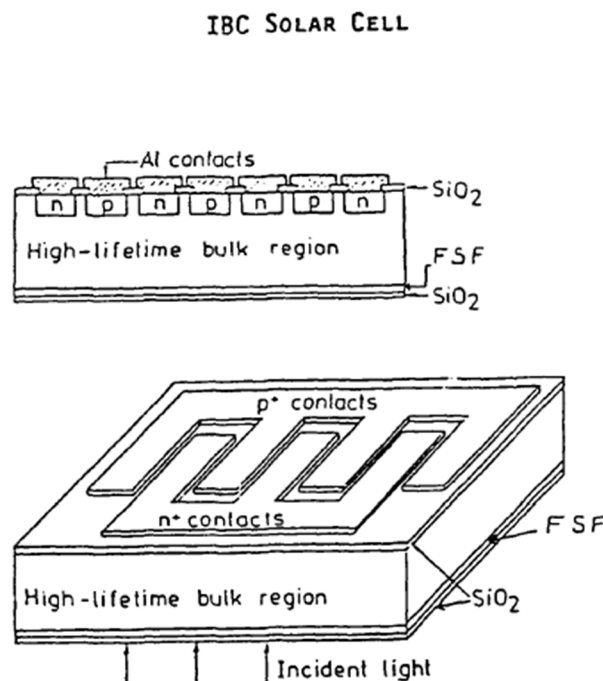
D. Marvin

154. Marvin "evaluate[s] the IBC cell design for use in space missions," including "optimization of the IBC cell design ... and assessment of the effects of certain design parameters on cell performance." Ex.1008-Marvin, 5, 9. Marvin explains that "the primary incentive for use of such [IBC] cells is increased efficiency." Ex.1008-Marvin, 5.

155. Marvin states that front surface field structures have been known since as late as "the mid 1980s." Ex.1008-Marvin, 3. Marvin further states that "[t]he front surface field (FSF) is a heavily doped region ... which covers the entire front face of the solar cell" and "is generally introduced by heavier doping in a thin layer near the interface." Ex.1008-Marvin, 15. Marvin also explains that the "purpose [of

the FSF] is to provide an electric field that repels one carrier type away from the front surface,” which “effectively reduces the surface recombination velocity by reducing the concentration of one type of carrier near the surface.” Ex.1008-Marvin, 15.

156. Marvin teaches an interdigitated back-contact silicon solar cell having a doped region on the front side (i.e., the front surface field) and p- and n-type doped regions on the back side, with metal contacts formed over the back-side doped regions, as shown in Marvin’s figures below. Ex.1008-Marvin, 4. In these figures, the front side that faces the sun is on the bottom (i.e., corresponding to the arrows for “incident light”).



Ex.1008-Marvin, 4.

157. To produce “an optimum design for various applications,” Marvin “var[ied] the critical design parameters” such as “base thickness and doping, contact region doping and dimensions, and front surface field (FSF) parameters.” Ex.1008-Marvin, 5, 16. Marvin discloses that “[b]asic IBC cell design parameters include base thickness and doping, contact region doping and dimensions, and front surface field (FSF) parameters.” Ex.1008-Marvin, 5.

158. Marvin considers two different profiles for the FSF, abrupt FSF and graded FSF. Ex.1008-Marvin, 15. Marvin explains “the FSF doping level becomes very important for a graded FSF” where “the field is present over the entire region thickness.” Ex.1008-Marvin, 15.

159. With respect to evaluating “[t]he effects of FSF ... doping level,” Marvin reports that “over a rather broad range around $1\text{E}17$ to $1\text{E}18\text{ cm}^{-3}$,” “[t]he FSF effectiveness is relatively constant.” Ex.1008-Marvin, 15. Decreasing the FSF doping level below $1\text{E}17\text{ cm}^{-3}$ reduces the FSF effectiveness “due to the weakness of the electric field.” Ex.1008-Marvin, 15. As I explained in Section VII.B.2.a, doping the FSF forms an electric field between it and the adjacent substrate that assists with moving charge carriers to the appropriate metal contact to generate current, thereby increasing solar cell efficiency. Decreasing the FSF doping level

decreases the difference between the doping concentrations of the FSF and the rest of the substrate, which weakens the electric field.

160. Marvin states that increasing the FSF doping level above $1\text{E}18\text{ cm}^{-3}$ also reduces FSF effectiveness “due to increased Auger recombination.” Ex.1008-Marvin, 15. As I explained in Section VII.B.2.a, by 2014, researchers in the field understood that FSF dopant concentrations above $1\times 10^{18}\text{ cm}^{-3}$ induced Auger recombination, which in turn reduced solar cell efficiency.

E. Istratov

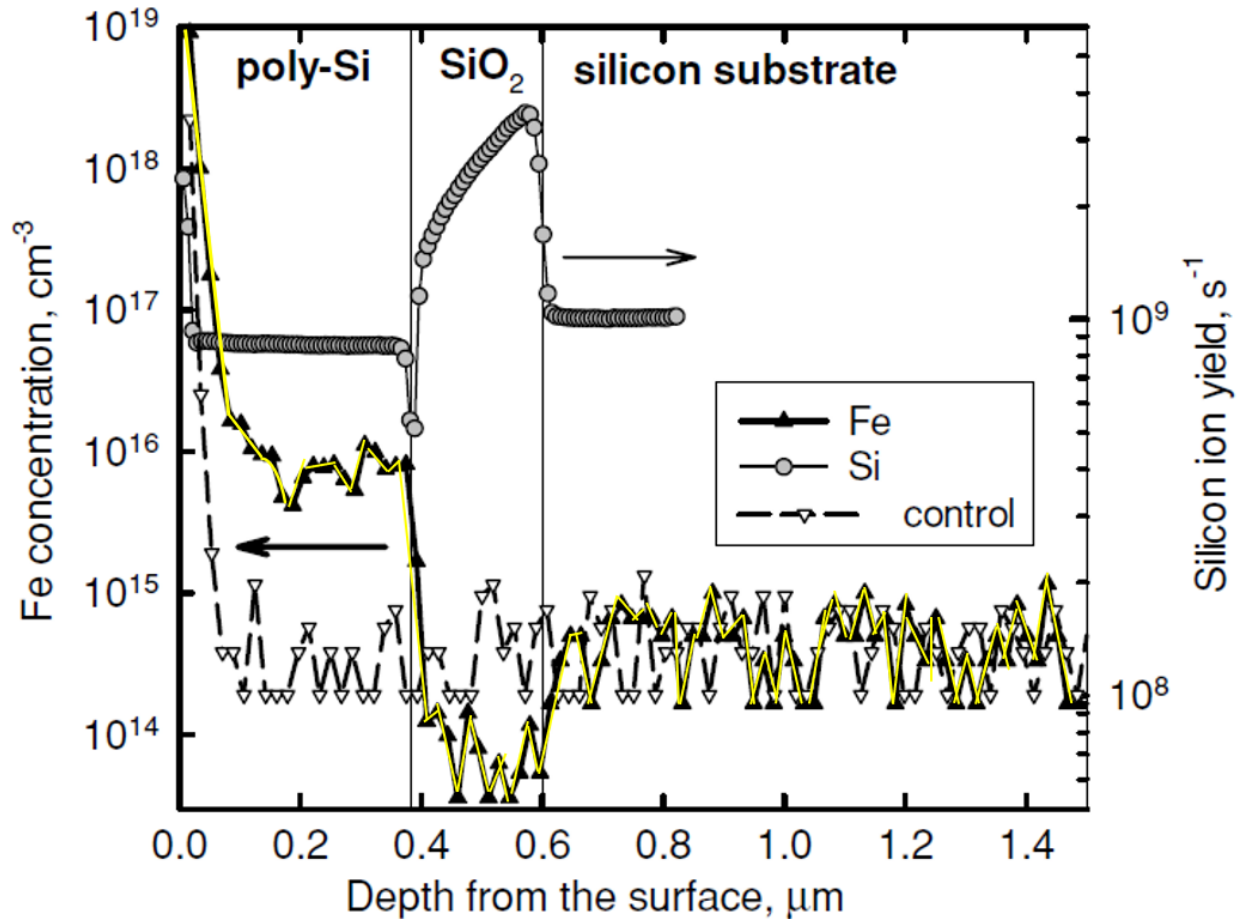
161. In order to perform “predictive modelling of gettering,” Istratov “perform[s] several experiments to determine or verify the materials parameters essential for correct quantitative description of the processes involved in gettering of metals” in silicon devices. Ex.1012-Istratov, 569-70.

162. Istratov uses a test structure consisting of a “197 nm thick thermal oxide grown on” a silicon substrate, “covered by a 370 nm [] layer of [chemical vapor deposition]-grown polysilicon.” Ex.1012-Istratov, 570. Istratov explains that the oxide layer was “intentionally chosen thicker than in typical production wafers in order to separate diffusion profiles and equilibrium metal concentration within the oxide from metals accumulated at Si/SiO₂ interfaces.” Ex.1012-Istratov, 570.

Istratov “evaluated” “gettering techniques for iron and copper.” Ex.1012-Istratov, Abstract.

163. For the experiments with iron, the “[i]ron contamination was performed by scratching the backside of the sample” (opposite from the polysilicon layer) with an iron wire, followed by “annealing for 8 h[ours] at 1020 °C.” Ex.1012-Istratov, 570.

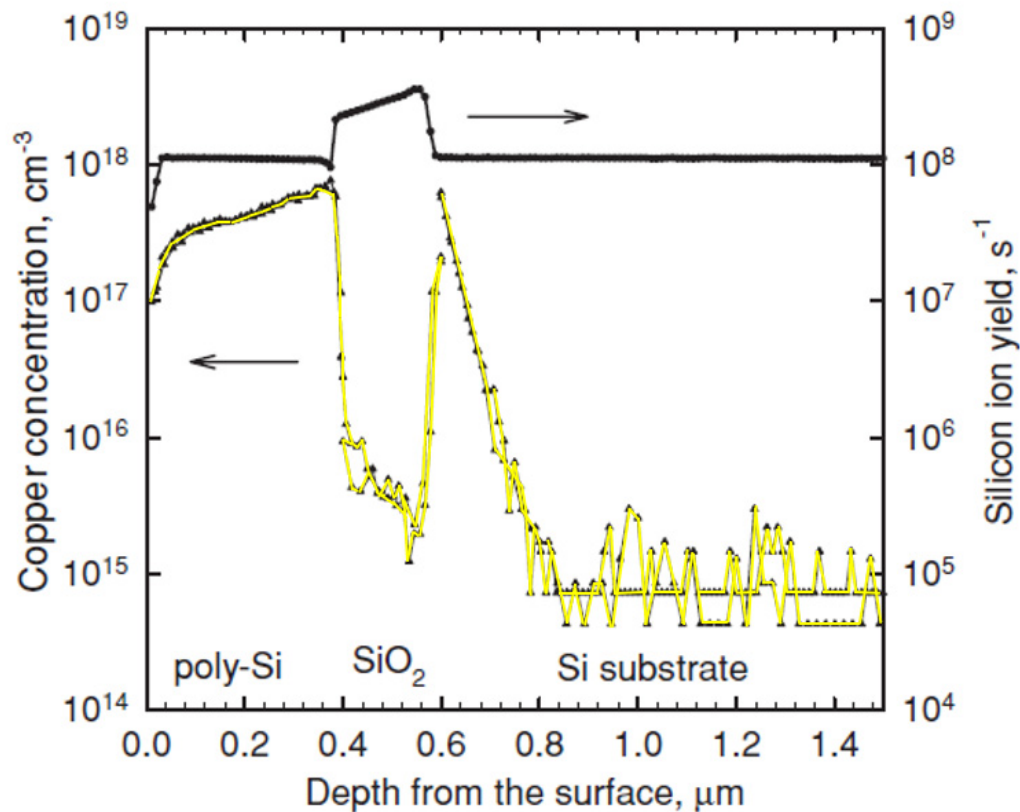
164. Istratov’s Figure 2 shows the depth profile of iron concentration after the iron contamination, heating “at 1020 °C for 8 h[ours],” and diffusion of iron within the test structure:



Ex.1012-Istratov, 570, Fig.2 (annotated).

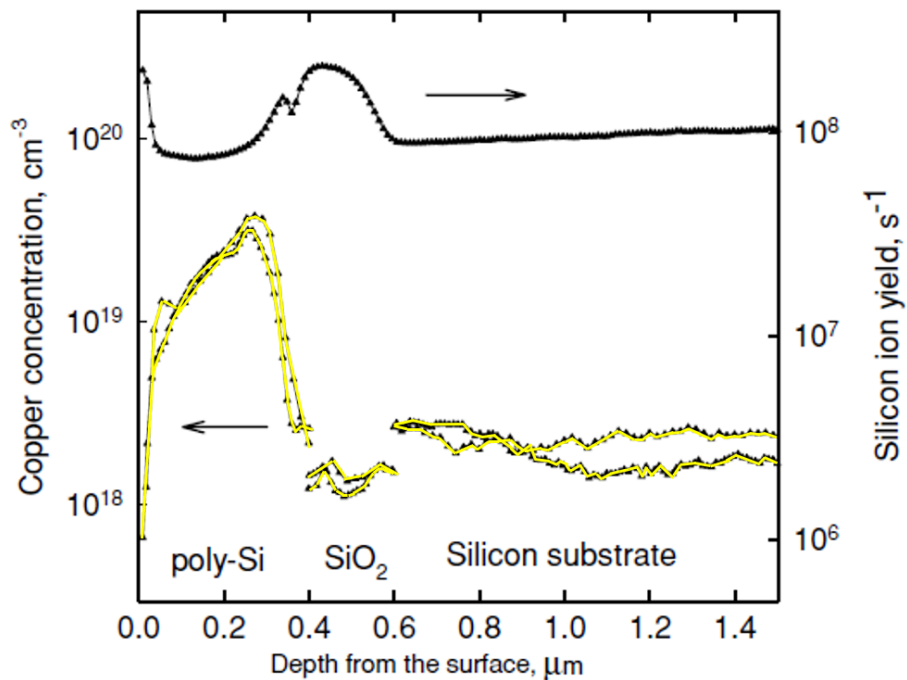
165. Istratov explains that “it follows from Figure 2 that the solubility of iron in poly-silicon ... is more than an order of magnitude higher than in the silicon substrate,” which Istratov interprets as “segregation gettering of iron by poly-silicon.” Ex.1012-Istratov, 570. Moreover, a person of ordinary skill in the art would have understood that a heating step at 1020 °C is compatible with the fabrication of solar cells.

166. For the experiments with copper, in a first experiment, the “poly-Si/SiO₂/Si structure [was] intentionally contaminated with copper” and the copper was diffused from the backside of the wafer “at 690 °C for 5 h[ours] and quenched to room temperature.” Ex.1012-Istratov, 571. Istratov’s Figure 4 shows the depth profile of copper concentration, with copper concentration consistently highest in the poly-Si layer than in the silicon substrate:



Ex.1012-Istratov, 571, Fig.4 (annotated). “The two bottom curves are depth profiles taken at two different locations within the sample.” Ex.1012-Istratov, 571.

167. Istratov performs a second experiment for copper that contaminates the poly-Si/SiO₂/Si structure and then performs “diffusion[] ... at 1150 °C for 2 h[ours], terminating by quench at room temperature. Ex.1012-Istratov, 571. Figure 5 shows the depth profile of copper concentration:



Ex.1012-Istratov, 571, Fig.5 (annotated). “The two bottom curves are depth profiles taken at two different locations within the sample.” Ex.1012-Istratov, 571.

168. In Figure 5, “[t]he enhancement factor of Cu solubility in poly-Si relatively to Si substrate was [] 7.” Ex.1012-Istratov, 571. “The higher concentration of Cu in the poly-silicon layer can be interpreted as segregation of Cu at structural defects in the poly-silicon layer.” Ex.1012-Istratov, 571. A person of

ordinary skill in the art would have understood that a heating step at 690 °C or 1150 °C is compatible with the fabrication of solar cells.

F. Smith

169. Smith, like Choi, Granek, and Marvin, teaches a structure for a back-contact solar cell. Ex.1011-Smith, [0016]-[0022].

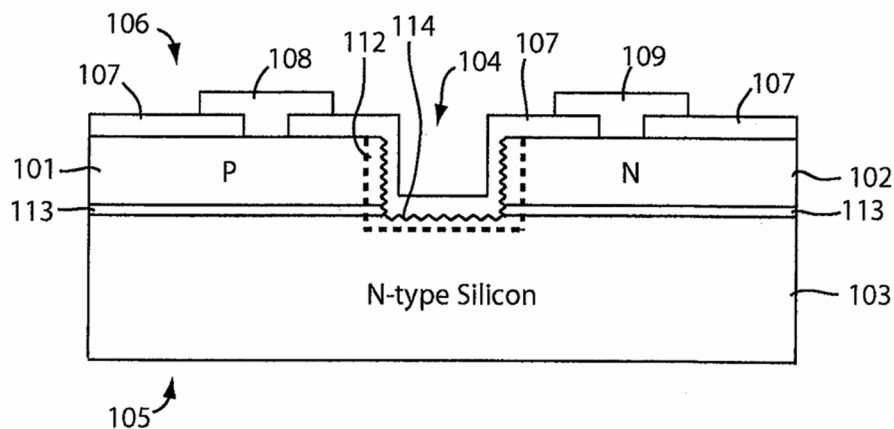


FIG. 2

Ex.1011-Smith, Fig.2.

170. Smith teaches a back-contact solar cell having a front side that faces the sun during normal operation, and a back side opposite the front side. Ex.1011-Smith, [0016] (“[T]he solar cell is a backside contact solar cell in that its doped regions 101 and 102 are on the backside 106 opposite to the front side 105. The front side 105 faces the sun during normal operation.”).

171. Smith teaches a dielectric layer formed on the back side of a substrate. Ex.1011-Smith, [0016] (“In one embodiment, the dielectric layer 113 comprises silicon dioxide thermally grown on the surface of the substrate 103”).

172. Smith further teaches p- and n-type doped regions formed over the dielectric layer. Ex.1011-Smith, [0016] (“The doped regions 101 and 102 are formed on a thin dielectric layer 113.”). In the embodiment of Figures 1 and 2, the substrate and doped region 102 are n-type doped, and doped region 101 is p-type doped. Ex.1011-Smith, [0017]; Fig.2. Smith further explains that the doped regions “may comprise polysilicon.” Ex.1011-Smith, [0018]. Smith also teaches interdigitated metal contacts connected to the doped regions. Ex.1011-Smith, [0024] (“[I]nterdigitated metal contact fingers 108 and 109 may be formed through the silicon nitride 107 to make an electrical connection to the doped regions 101 and 102, respectively.”). Smith specifies that one metal contact may be connected to a positive electrical terminal and the other to a negative electrical terminal. Ex.1011-Smith, [0024] (“In the example of Fig.2, the metal contact finger 108 may be connected to a positive electrical terminal and the metal contact finger 109 may be connected to a negative electrical terminal.”).

173. Smith teaches that “[i]n solar cells with P-type and N-type doped regions in the substrate, the P-type and N-type doped regions may be formed with

separate or abutting perimeters.” Ex.1011-Smith, [0015]. However, Smith explains that “this is not true with polysilicon doped regions because recombination in the space charge region where the polysilicon doped regions touch is very high due to the lifetime of charge carriers in the polysilicon being very low.” Ex.1011-Smith, [0015]. Accordingly, Smith teaches that touching polysilicon doped regions “adversely affect efficiency” of the solar cell. Ex.1011-Smith, [0015].

174. To address this problem, Smith teaches a trench between the doped polysilicon regions. Ex.1011-Smith, [0019] (“As shown in Fig.1, the doped regions 101 and 102 are separated by a trench 104, which serves as a gap between the doped regions 101 and 102.”). Smith explains that the trench “addresses the aforementioned issues relating to polysilicon parasitic space charge recombination” in three ways. Ex.1011-Smith, [0025]. First, Smith explains that “the trench 104 separates the doped regions 101 and 102 so they are not physically in contact,” which “prevents the space charge region from existing in either polysilicon film.” Ex.1011-Smith, [0025]. Second, “the resulting accumulation layer under the trench 104 repels minority carriers to improve surface passivation.” Ex.1011-Smith, [0025]. Third, “the textured surface 114 in the trench 104 increases solar radiation collection.” Ex.1011-Smith, [0025]. Smith explains that these features “advantageously help increase solar cell efficiency.” Ex.1011-Smith, [0025].

XI. GROUNDS FOR FINDING THE CHALLENGED CLAIMS INVALID

175. It is my opinion that the Challenged Claims are unpatentable on the following grounds.

- **Ground I:** Claims 10-17 and 19-20 are invalid as obvious over Choi, Granek or Marvin, and Istratov.
- **Ground II:** Claim 18 is invalid as obvious over Choi, Granek or Marvin, Istratov, and Smith.
- **Ground III:** Claims 10-15 are invalid as obvious over Cousins, Granek or Marvin, and Istratov.

The below discussion demonstrates in detail that claims 10-20 of the '315 patent are unpatentable as obvious. A copy of the Challenged Claims is attached as **Appendix C**.

A. GROUND I: Claims 10-17 and 19-20 Are Invalid as Obvious Over Choi, Granek or Marvin, and Istratov.

176. As detailed below, the combination of Choi, Granek or Marvin, and Istratov renders claims 10-17 and 19-20 obvious.

1. Analogous Art, Motivation to Combine, and Reasonable Expectation of Success

177. As I explained in Section III.C, I was informed and I understand that one of the requirements for obviousness is that the references must be analogous to the claims being challenged. *See* above §III.C. As I explained in Section III.C, I was informed and understand that a person of ordinary skill in the art must have been

motivated to combine the references with a reasonable expectation of success. *See* above §III.C. It is my opinion that each requirement is met here.

178. In my opinion, it would have been obvious to combine the techniques of Choi, Granek or Marvin, and Istratov together to reduce recombination to improve the efficiency of solar cells. Choi, Granek, Marvin, and Istratov each describe techniques to reduce recombination. Ex.1006-Choi, [0029]; Ex.1010-Granek, 117-136; Ex.1008-Marvin, 3-5; Ex.1012-Istratov, 569-70.

179. Specifically, Choi teaches reducing recombination with a front surface field (or FSF) on a back-contact solar cell. Ex.1006-Choi, [0029].

180. Like Choi, Granek and Marvin are in the same field of endeavor as the '315 patent and teach the use of front surface fields in back-contact solar cells for similar purposes. *See* above §§X.C-X.D. Granek discloses that a FSF dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ is desired, and Marvin discloses that FSF dopant concentrations of $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$ are suitable. Ex.1010-Granek, 121-122; Ex.1008-Marvin, 15. Both Granek and Marvin explain that the FSF dopant concentration level must be high enough to achieve a reduction in surface recombination while low enough to avoid the increased recombination rates—within the front surface field itself—associated with higher dopant

concentration levels (*i.e.*, Auger recombination). Ex.1010-Granek at 117-136; Ex.1008-Marvin, 3-5, Fig.1.

181. Istratov is directed to a gettering process to reduce metal impurities in a semiconductor structure. Ex.1012-Istratov, 569-70. As of the earliest possible priority date, gettering was well known to improve the efficiency and performance of solar cells (*see* above §VII.B.2.b)—a stated goal of Choi, Granek, and Marvin. Ex.1006-Choi, [0006]; Ex.1010-Granek, Abstract; Ex.1008-Marvin, 5.

182. Thus, for similar reasons, a person of ordinary skill in the art would have found it obvious to implement Istratov's gettering in the Choi-Granek and Choi-Marvin combinations.

a. Choi with Granek or Marvin

i. Analogous Art

183. **First**, it is my opinion that Choi, Granek, and Marvin are in the same field as the Challenged Claims—namely, solar cell devices. All the references are focused on improving device efficiency by reducing recombination. Ex.1006-Choi, [0003], [0006], [0029]; Ex.1010-Granek, Abstract; Ex.1008-Marvin, 5, 15; Ex.1001-USP315, 1:21-39, cls.10-20. Like the '315 patent, Choi, Granek, and Marvin specifically teach back-contact solar cell structures with front surface fields.

Ex.1006-Choi, [0003], [0006], [0029]; Ex.1010-Granek, Abstract; Ex.1008-Marvin, 5, 15; Ex.1001-USP315, 1:21-39, cls.10-20.

ii. Motivation to Combine

184. *Second*, it is my opinion that a person of ordinary skill in the art would have been motivated to implement a FSF dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ and $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$ as disclosed in Granek and Marvin, respectively, in Choi's front surface field region. Ex.1010-Granek, 121-122 (Figs.7-1, 7-3); Ex.1008-Marvin, 15.

185. The substrate of Choi's back-contact solar cell has a front surface field region used to reduce recombination. Ex.1006-Choi, [0026], [0029]. Choi states that the front surface field region has a higher dopant concentration than the semiconductor substrate but does not provide a value for the dopant concentration. Ex.1006-Choi, [0026], [0029]. Choi, however, teaches that "the base area 110 not including the doping area may have a specific resistance of 0.5 ohm·cm to 20 ohm·cm." Ex.1006-Choi, [0095]. A person of ordinary skill in the art would have recognized that a specific resistance of 0.5 ohm·cm to 20 ohm·cm corresponds to a substrate dopant concentration of $6.7 \times 10^{14} \text{ cm}^{-3}$ to $3.3 \times 10^{16} \text{ cm}^{-3}$ for a p-type silicon substrate, and $2.2 \times 10^{14} \text{ cm}^{-3}$ to $1.1 \times 10^{16} \text{ cm}^{-3}$ for an n-type silicon substrate. Well before the earliest priority date of the '315 patent, the relationship between specific

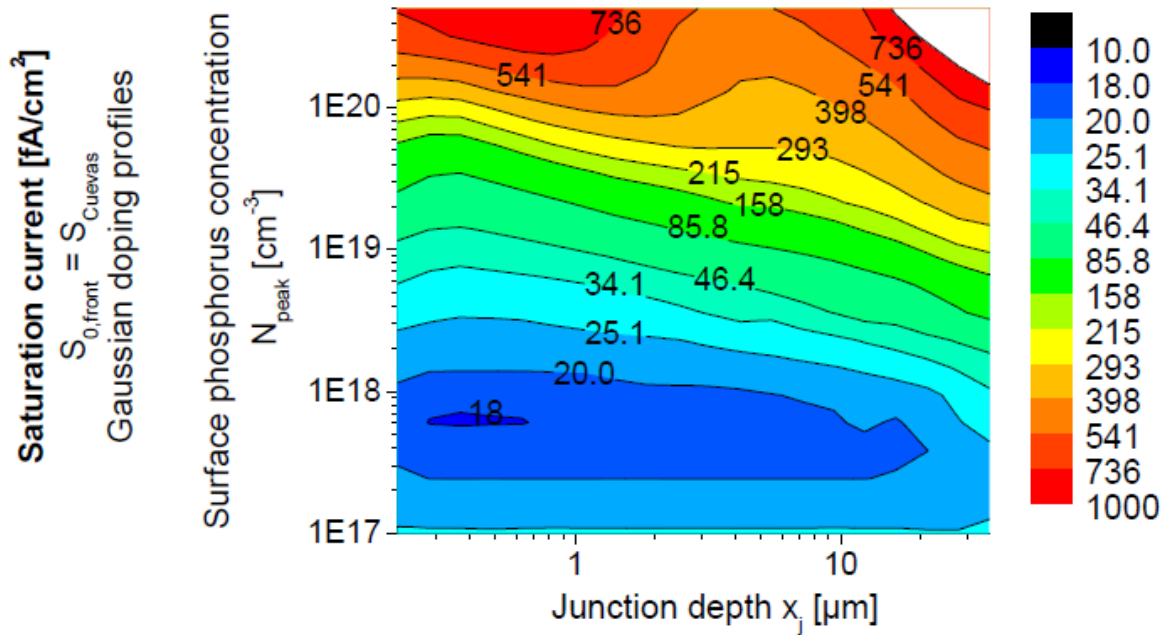
resistance and doping concentration was well known for uniformly doped silicon, and charts, graphs, and other tools were available to calculate a doping concentration from a specific resistance value. Thus, a person of ordinary skill in the art would have understood that the front surface field region of Choi has a dopant concentration higher than $3.3 \times 10^{16} \text{ cm}^{-3}$ for a p-type substrate and $1.1 \times 10^{16} \text{ cm}^{-3}$ for an n-type substrate.

186. Looking at Choi, a skilled artisan would have been motivated to turn to a reference such as Granek or Marvin to identify a dopant concentration that is high enough to minimize surface recombination while at the same time low enough to minimize Auger recombination, which occurs at higher doping levels as I previously discussed in Section VII.B.2.a.

187. Granek states:

A lowly doped FSF results in high quantum efficiency. This is because Auger recombination inside the highly doped region and the surface recombination velocity are low. A proper choice of the front surface field profile is therefore one of the most critical points in the design of the back-contact, back-junction solar cell device.

Ex.1010-Granek, 120. As I explained in Section X.C, Granek demonstrates that the simulated solar cell's saturation current density—and thus overall recombination—is lowest when the FSF dopant concentration is approximately $1 \times 10^{18} \text{ cm}^{-3}$ in Figure 7-3:



Ex.1010-Granek, 122 (Fig.7-3).

188. Marvin states:

The FSF effectiveness is relatively constant over a rather broad range around $1E17$ to $1E18$ cm⁻³, decreasing below this level due to the weakness of the electric field and decreasing above this level due to increased Auger recombination.

Ex.1008-Marvin, 15.

189. It is also my opinion that a person of ordinary skill in the art would have been motivated to combine Choi with Granek or Choi with Marvin because it would have merely involved the use of known techniques (doping a region near a surface of the solar cell at a particular dopant concentration) to a known device (back-contact solar cell) in the same way.

190. The dopant concentrations identified in Granek and Marvin would have been applied in the front surface field layer 120 of Choi. Ex.1010-Granek, 120-121; Ex.1006-Choi [0029], [0074]; Ex.1008-Marvin, 15. Choi teaches how to form the front surface field layer 120:

A front surface field layer 120 may be formed on the front surface of the semiconductor substrate 10 (that is, on the base area 110). The front surface field layer 120 is an area where the first conductive-type dopant is doped at a concentration higher than the semiconductor substrate 10 and performs similar functions to a back surface field (BSF) layer. That is, the front surface field layer 120 prevents electrons and holes separated by incident light from being recombined and then decay on the front surface of the semiconductor substrate 10.

...

[T]he front surface field layer 120 may be formed by doping the semiconductor substrate 10 with a first conductive type dopant by a variety of methods such as ion implantation or thermal diffusion

Ex.1006-Choi, [0029], [0074].

191. Granek also teaches how to form the front surface field, i.e., by phosphorus (thermal) diffusion. Ex.1010-Granek, 117 (“The passivation quality of different phosphorous-doped front surface field diffusion profiles was analyzed.”), 119 (“The phosphorus-doped front surface field, applied in the analyzed solar cells is therefore a high-low junction which passivated the silicon surface by a strong reduction of holes concentration at the surface.”), 124 (“The front surface field was created on both sample sides by a tube furnace phosphorus diffusion form [sic] liquid POCl_3 source.”).

192. Similarly, Marvin describes adding a front surface field through a doping step. Ex.1008-Marvin, 15 (“The FSF is generally introduced by heavier doping in a thin layer near the interface.”).

193. As I explained in Section VII.B.2.a, the FSF dopant concentration recited by claim 10 of the ’315 patent (“approximately less than or equal to 2×10^{18} cm⁻³”) was well known before the earliest possible priority date. *See, e.g.*, Ex.1021-King, 369 (“In the case of a back-contacted solar cell ... the optimum emitter is the one with the lowest J_0 . For untextured surfaces, this corresponds to an emitter with $N_{\text{Dsurf}} \approx 1 \times 10^{18}$ cm⁻³ that is as thin as possible.”); Ex.1030-Swanson-352, 4:43-51 (“Shallow diffused regions 60 and 62 are formed in the opposing surfaces of the wafer by the diffusion of an N type dopant such as phosphorous into the surfaces to a depth of 0.1 micron. The maximum surface dopant concentration of the diffused regions 60 and 62 is 10^{18} atoms per cubic centimeter.”); Ex.1040-Procet, 1 (“Peak concentration doping is ... 1×10^{18} cm⁻³ for FSF.”); Ex.1041-Hermle, 5-6 (“For FSF doping concentrations of above 10^{19} cm⁻³, J_{sc} decreases strongly with increasing FSF doping concentration because of the increased Auger recombination ... For thicker FSF regions, the FSF doping concentration should be lower than 10^{18} cm⁻³....”).

194. Therefore, it is my opinion that a person of ordinary skill in the art would have been motivated to use the FSF dopant concentrations disclosed by

Granek and Marvin because problems with recombination were well known and the dopant concentrations of Granek and Marvin had been found to reduce recombination while at the same time limiting Auger recombination.

iii. Reasonable Expectation of Success

195. *Third*, it is my opinion that a person of skill in the art would have had a reasonable expectation of success in implementing the dopant concentrations of Granek and Marvin in the solar cell of Choi. The silicon-based solar cells of Choi, Granek, and Marvin are fabricated using silicon semiconductor fabrication techniques, which were well-established and standardized by the earliest possible priority date of the '315 patent. Indeed, the '315 patent states that certain fabrication steps for forming the dopant region, dielectric region, and emitter region were “conventional.” Ex.1001-USP315, 3:56-66 (“the dielectric region and/or the emitter region are described as being grown by a thermal process or deposited through conventional deposition process, respectively”), 4:32-41 (“the dopant region is described as being grown by a thermal process or deposited through conventional deposition process, respectively”), Fig.1.

196. As examples of the conventional fabrication steps, most silicon semiconductor device fabrication processes involve steps such as cleaning the substrate (wafer), optionally depositing semiconductor layers onto the substrate,

doping regions of the substrate or the deposited semiconductor layers, depositing dielectric layers, and depositing metal layers.

197. Further, the solar cells of Choi, Granek, and Marvin are all back-contact solar cell structures with front surface fields. For example, Choi teaches a front surface field layer 120 may be formed by “a variety of methods such as ion implantation and diffusion.” Ex.1006-Choi, [0074]. The front surface field layer 120 “is doped at a higher concentration than the semiconductor substrate 10” and “prevents electrons and holes separated by incident light from being recombined and then decay[ing] on the front surface of the semiconductor substrate 10.” Ex.1006-Choi, [0029]. Like Choi, the solar cell of Marvin is a back-contact solar cell with a front surface field. Ex.1006-Choi, Figs.1, 3k; Ex.1008-Marvin, 5, Fig.1. Marvin teaches that “[t]he FSF effectiveness is relatively constant over a rather broad range around $1\text{E}17$ to $1\text{E}18\text{ cm}^{-3}$ ” Ex.1008-Marvin, 15. In addition, Granek teaches a desired dopant concentration of approximately $1 \times 10^{18}\text{ cm}^{-3}$. Ex.1010-Granek, 120-122, Figs.7-1, 7-3. The FSF in the back-contact solar cell of Granek is doped with phosphorus—one of the same n-type dopants disclosed by Choi. Ex.1010-Granek, 117, 121; Ex.1006-Choi, [0025] (“That is, the first conductive-type dopant may be an n-type impurity such as a Group V element including phosphorous (P), arsenic (As), bismuth (Bi), antimony (Sb) or the like.”), [0059] (“Examples of the n-type

impurity include Group V elements such as phosphorous (P), arsenic (As), bismuth (Bi) and antimony (Sb).”); Ex.1010-Granek, 117 (“The passivation quality of different phosphorous-doped front surface field diffusion profiles was analyzed.”), 119 (“The phosphorus-doped front surface field, applied in the analyzed solar cells is therefore a high-low junction which passivated the silicon surface by a strong reduction of holes concentration at the surface.”), 124 (“The front surface field was created on both sample sides by a tube furnace phosphorus diffusion from [sic] liquid POCl_3 source.”). Therefore, given the similarities among the references, a person of ordinary skill in the art would have been able to achieve an improved efficiency solar cell using the dopant concentrations disclosed by Granek and Marvin.

198. Further, it is my opinion that the absence of a disclosed dopant concentration in Choi is evidence that the inventors of the Choi patent thought a person of ordinary skill in the art would be able to ascertain a dopant concentration from experience or outside sources, such as Granek and Marvin, to make an efficient solar cell.

199. Moreover, it is my opinion that only minor adjustments to the solar cell fabrication process would be required to make the solar cell of Choi with the dopant concentrations taught by Granek and Marvin. To the extent that Choi’s solar cell is not already fabricated with the front surface field having the disclosed dopant

concentrations of Granek and Marvin, only a small adjustment would be required to dope the front surface field at these concentrations, and a person of ordinary skill in the art would have known how to adjust the dopant concentration. For example, the heating time and temperature during the dopant diffusion process would need to be changed, but no additional processing steps or adjustments would be necessary. Furthermore, no other existing processing steps would be affected.

200. As I explained in Section VII.B.2.a, numerous researchers in the field were able to obtain a FSF dopant concentration of “approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ ” before 2014. *E.g.*, Ex.1040-Procel, 2 (“Peak concentration doping is ... $1 \times 10^{18} \text{ cm}^{-3}$ for FSF[.]”); Ex.1021-King, 367, 369 (“emitter with $N_{D, \text{ surf}} \approx 1 \times 10^{18} \text{ cm}^{-3}$ ”).

201. Finally, it is my opinion that the front surface field dopant concentration in Marvin is not dependent on the environment (space or terrestrial) in which the solar cell is used. The teachings from Marvin described herein are those of solar cells under “1 sun conditions” at “beginning of life (BOL).” Ex.1008-Marvin, 11, 15. Standard 1 sun solar cell test conditions for a space environment are only slightly different—Air Mass 0 spectrum having 1353 W/cm^2 irradiance—than those for a terrestrial environment—Air Mass 1.5 Global having 1000 W/cm^2 irradiance—and thus teachings for one environment were commonly implemented in the other.

Ex.1046-Green, 2; Ex.1008-Marvin, 5. BOL refers to the state of a solar cell after it is manufactured and before it has undergone any degradation caused by its operating environment. Consequently, observations at BOL do not incorporate environment-specific factors (e.g., degradation due to ionizing radiation found only in space). In discussing BOL solar cell performance under 1 sun conditions, Marvin states that “FSF effectiveness is relatively constant over a rather broad range around $1\text{E}17$ to $1\text{E}18\text{ cm}^{-3}$.” Ex.1008-Marvin, 15.

202. Since Choi is not directed specifically to either a space or terrestrial environment, a person of ordinary skill in the art would have understood that Choi’s solar cells, like Marvin’s, could be implemented in both space and terrestrial environments.

b. Choi with Granek or Marvin and Istratov

i. Analogous Art

203. *First*, Istratov is in the field of silicon semiconductor devices, which encompasses solar cells. Ex.1012-Istratov, 570 (Istratov teaches “a poly-Si/SiO₂ structure.”). Since silicon-based solar cells and microelectronics technologies such as transistors are closely related in structure (e.g., both rely on PN junctions) and manufacturing techniques, skilled artisans in solar cells frequently learned from and adopted microelectronic processing technologies. Ex.1079-Harley, 1:17-21

(“Generally, solar cells are fabricated on a semiconductor wafer or substrate using semiconductor processing techniques to form a p-n junction near a surface of the substrate.”); Ex.1080-Cousins-2011, [0002] (“Solar cells are well known devices for converting solar radiation to electrical energy. They can be fabricated on a semiconductor wafer using semiconductor processing technology.”); Ex.1081-Sunpower-2002, 1 (“‘This is a natural partnership,’ said Dick Swanson, president and CEO of SunPower. ‘SunPower has a superior technology with high cell efficiency and low cost-per-watt in a fast-growing market that depends upon silicon-based manufacturing expertise. Cypress is a company that has demonstrated its ability to provide continuous innovation in silicon manufacturing in high volumes and at very low cost.’”); Ex.1082-Sunpower-2003, 1 (“Cypress Semiconductor Corporation is sharing its expertise in technology development and high-volume manufacturing with SunPower, providing the solar cell company with a substantial competitive advantage in a silicon-intensive, highly cost-sensitive business.”); Ex.1075-Green-1995, 218 (“To achieve design objectives in [surface passivation,] full advantage had to be taken of developments in microelectronics”), 224 (stating that recombination and the usage of thermal oxide have been “well documented for microelectronics”). Choi, Granek, Marvin, and Istratov are in the same field as the Challenged Claims of the ’315 patent—namely, silicon semiconductor devices

encompassing solar cell devices. Further, like the ‘315 patent, all the references are focused on improving device efficiency by reducing recombination. Ex.1012-Istratov, 569-571; Ex.1006-Choi, [0003], [0006], [0029]; Ex.1010-Granek, Abstract; Ex.1008-Marvin, 5, 15; Ex.1001-USP315, 1:21-39, cls.10-20; *see* above Section VIII.A.

204. In addition, Choi, Granek, Marvin, and Istratov are directed to solving the same problems as the Challenged Claims—improving device efficiency by reducing recombination. *See* above Sections VIII.A, XI.A.1.a, X.A, X.C-E. Choi, Granek, and Marvin are all directed to improving silicon-based solar cell efficiency, and Istratov describes improving a silicon device structure that is directly applicable to improving solar cells. Ex.1012-Istratov, 569-570 (Fig.2) (“[S]olubility of iron in poly-silicon at this temperature is more than an order of magnitude higher than in the silicon substrate. We interpret [this] observation as segregation gettering of iron by poly-silicon.”), 571 (“The higher concentration of Cu in the poly-silicon layer can be interpreted as segregation of Cu at structural defects in the poly-silicon layer.”).

ii. Motivation to Combine

205. ***Second***, it is my opinion that a person of ordinary skill in the art would have been motivated to combine Choi and Granek (“Choi-Granek”) or Choi and

Marvin (“Choi-Marvin”) with Istratov by adding Istratov’s gettering process to the Choi-Granek or Choi-Marvin solar cell to trap impurities in a polysilicon layer such as an emitter and thereby reduce the amount of recombination. By the earliest possible priority date of the ’315 patent, it was well known that metal impurities could be effectively gettered in a silicon-dielectric-polysilicon layered structure. *See* Ex.1064-Istratov-2004, 4473 (“The second experimental procedure which we used to separate the segregation gettering consists in using a thin diffusion barrier between the polySi and the substrate. Figure 2 is a SIMS profile taken on a structure consisting of 0.37 μm of polysilicon and 200 nm of SiO_2 on top of a silicon substrate. The sample was annealed for 8 h at 1020 $^{\circ}\text{C}$, which was sufficient for iron to diffuse through silicon dioxide and establish its equilibrium distribution at the annealing temperature.”). As I discussed in Section VII.B.2.b, by 2014, gettering metal impurities from the substrate into the emitter (where they cause less recombination) was well known in the solar cell field. *E.g.*, Ex.1033-Perichaud, 315-318; Ex.1035-Gupta, [0037]; Ex.1031-Bultman, 72.

206. Choi discloses a back-contact solar cell designed to improve efficiency. Ex.1006-Choi, [0006]-[0007]. Choi teaches that recombination would be reduced, and efficiency improved, by adding various features such as a front surface field to a silicon solar cell. Ex.1006-Choi, [0031]. Istratov provides another way of

reducing recombination in a silicon-based device (and thereby increasing efficiency)—by a gettering process. Ex.1012-Istratov, 569-571, Figs.2, 4-5. Istratov describes the gettering process in a test structure composed of a silicon substrate, silicon dioxide (SiO_2) layer, and polysilicon layer. Ex.1012-Istratov, 569-571. Upon heating to a sufficient temperature, the metal impurity, either iron or copper, moves from the substrate through the SiO_2 layer to the polysilicon layer. Ex.1012-Istratov, 569-570 (“ [I]t follows from figure 2 that the solubility of iron in polysilicon at this temperature is more than an order of magnitude higher than in the silicon substrate ... [which shows] segregation gettering of iron by poly-silicon.”), 571 (“The higher concentration of Cu in the poly-silicon layer can be interpreted as segregation of Cu at structural defects in the poly-silicon layer.”).

207. Upon identifying detrimental levels of metal impurities in a solar cell substrate, a person of ordinary skill in the art would have recognized that Choi’s solar cells include the same layers as the test structure of Istratov—namely, a silicon substrate, SiO_2 layer, and polysilicon layer—and would have been motivated to use the gettering technique of Istratov to improve the efficiency of the Choi-Granek and Choi-Marvin solar cells by trapping the impurities in a polysilicon region, such as an emitter, where they are less capable of contributing to recombination.

208. It was well known by the earliest possible priority date of the '315 patent that recombination is suppressed in regions of a solar cell with low concentrations of at least one carrier type because recombination requires two carrier types. It was also well known that doped layers, particularly those at the back side of a solar cell, where there is only weak absorption of light and excitation of electron-hole pairs, have low concentrations of one carrier type (i.e., that with the opposite polarity of the doping). And it was well known that n- and p-type polysilicon layers, like Choi's first conductive type area 32 and the second conductive type area 34 are such doped layers.

209. It is also my opinion that a person of ordinary skill in the art would have been motivated to combine Choi-Granek or Choi-Marvin with Istratov because the combinations would have merely involved the use of known techniques (gettering of metal impurities) to a known device (back-contact solar cell with a selected FSF dopant concentration) in the same way (by using solar cell fabrication processing techniques). As I explained above, Choi's solar cells have the same layers as the test structure of Istratov. A person of ordinary skill in the art would therefore have recognized that Istratov's disclosure of removing iron or copper metal impurities from the substrate through the silicon dioxide layer and relocating them to the

polysilicon layer would have been desirable in the similar solar cell structure of Choi to reduce recombination and improve solar cell efficiency.

iii. Reasonable Expectation of Success

210. *Third*, it is my opinion that a person of ordinary skill in the art would have had a reasonable expectation of success in combining Choi-Granek or Choi-Marvin with Istratov. The combination of Istratov with Choi-Granek or Choi-Marvin would have been straightforward to implement; it simply requires heating the silicon solar cell to a temperature high enough to allow gettering to occur through an oxide layer to a polysilicon layer. The doping process for Choi's first and second conductive type areas 32, 34, which can be made of polycrystalline silicon, involves a thermal treatment step—but Choi does not specify the temperature used during the thermal treatment. Ex.1006-Choi, [0036]-[0037] ("The first conductive type area 32 may include a semiconductor (for example, silicon) having the same conductive type as the semiconductor substrate 10 ... For example, the first conductive type area 32 may be easily formed by doping ... polycrystalline silicon or the like with a first conductive type dopant ... For example, the second conductive type area 34 may be easily formed by doping ... polycrystalline silicon or the like with a second conductive type dopant by a variety of methods such as deposition or printing."), [0070] ("[T]he first conductive type dopant in the first doping layer 322 is diffused

into the semiconductor layer 30 by thermal treatment to form a plurality of first conductive type areas 32, and the second conductive type dopant in the second doping layer 342 is diffused into the semiconductor layer 30 to form a plurality of second conductive type areas 34.”).

211. A person of ordinary skill in the art would have known that such a thermal treatment step would have been used to getter metals from the substrate to the first and second conductive type areas by simply heating the solar cell to a high enough temperature. Ex.1064, Istratov-2004, 4472 (“Gettering of transition metals by a layer of polycrystalline silicon (polysilicon) deposited on the back side of silicon wafers has been widely used by the silicon industry as a means to remove transition metals from the wafer and improve the minority carrier lifetime.”), 4473 (“anneal[ing] for 8 h at 1020 °C[] was sufficient for iron to diffuse through silicon dioxide and establish its equilibrium distribution at the annealing temperature”). To the extent that an existing processing temperature was not high enough or an existing heating time was not long enough, a person of ordinary skill in the art would merely have had to increase the temperature of the tube furnace that the solar cell was heated in or the heating time to cause gettering. Ex.1083-Fenning, 214504-1 (“An alternative path to reduce the impact of metal impurities is to use higher-temperature processes. By increasing bulk solubility and speeding diffusion to near-surface

gettering layers, higher-temperature diffusions are expected to improve the extraction of metals from the bulk, including deleterious iron.”), Figs.1, 5.

212. For the gettering of iron, Istratov teaches that heating for “8 h[ours]” “at 1020 °C” was “sufficient to equilibrate the iron through the SiO₂ layer.” Ex.1012-Istratov, 570; *see above* §X.E. For the gettering of copper, Istratov teaches that heating at “690 °C for 5 h[ours]” or “at 1150 °C for 2 h[ours]” was sufficient to move the copper through the SiO₂ layer into the poly-silicon layer. Ex.1012-Istratov, 571; *see above* §X.E. Those annealing temperatures were compatible with solar cell manufacturing. *See, e.g.*, Ex.1084-Neuhaus, 2, 4, 6 (teaching a range of solar cell fabrication processes with a range of temperatures).

213. Furthermore, Istratov’s SiO₂ layer is significantly thicker than Choi’s tunneling layer 20. Istratov states the SiO₂ layer is “197 nm,” and Choi states the tunneling layer 20 “may be 0.5 nm to 5 nm.” Ex.1012-Istratov, 570; Ex.1006-Choi, [0034]. A skilled artisan would have understood that a thinner SiO₂ layer would facilitate gettering at lower temperatures or shorter times than the gettering temperatures and times taught by Istratov.

214. In addition, it is my opinion that a person of ordinary skill in the art would have known that solar cells are modular structures and therefore would have known that combining the Choi-Granek or Choi-Marvin solar cell with Istratov

would have reduced recombination. By “modular,” I mean that the solar cell front side and the back side can be designed and optimized independently of each other, after taking into account processing sequence and thermal and chemical compatibility of materials. By the earliest possible priority date, it was well known that manufacturing techniques could be employed on either side of the solar cell without substantially affecting the performance or function of structures on the other side of the solar cell.

215. As an example of the modularity of solar cells, Glunz describes a silicon solar cell study in which a variety of back surface structures (e.g., boron-diffused back surface fields, screen-printed alloyed Al back surface field, etc.) were combined with a front structure. Ex.1043-Glunz, 365 (“Thus, an experimental study of different rear surface structures combined with a high-efficiency front structure which does not limit cell performance was performed. This makes it possible to determine the surface recombination velocity S_{rear} and the internal reflectance R_{int} quite accurately.”).

2. Claim 10

- a. Element 10[Pre]: A solar cell, the solar cell having a front side which faces the sun during normal**

**operation and a back side opposite the front side, the
solar cell comprising:**

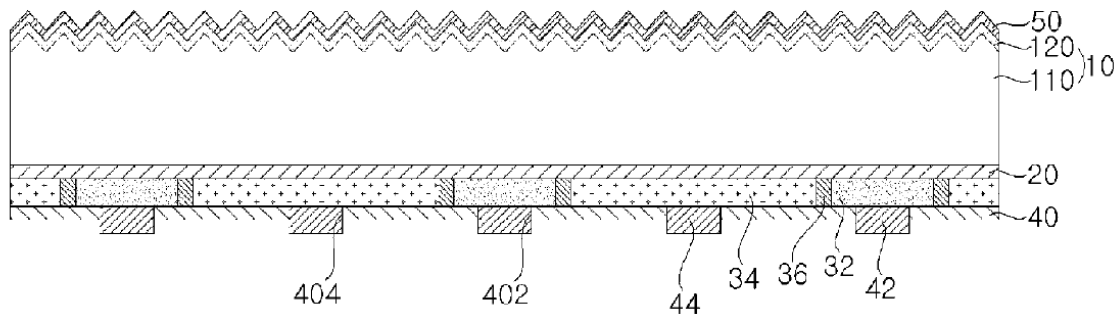
216. Choi teaches a *solar cell having a front side which faces the sun during normal operation and a back side opposite the front side.*⁷

217. Choi teaches a “solar cell 100,” Ex.1006-Choi, [0023], which is illustrated in Figure 1. Ex.1006-Choi, Fig.1; *see also* Ex.1006-Choi, Fig.2, 5. Choi teaches that the structure of solar cell 100 includes, among other layers, a “tunneling layer 20” formed on the back surface of solar cell 100. *See* Ex.1006-Choi, [0023] (“[T]he solar cell 100 according to the present embodiment includes a semiconductor substrate 10, a tunneling layer 20 formed on one surface (for example, back surface) of the semiconductor substrate 10”), [0033] (“In the present embodiment, a tunneling layer 20 is formed on the back surface of the semiconductor substrate 10.... The tunneling layer 20 may be entirely formed on the back surface of the semiconductor substrate 10.”), [0062]. Tunneling layer 20 is shown toward the bottom of solar cell 100 in Figure 1.

⁷ Italicized text is used to indicate claim language unless otherwise noted.

FIG. 1

100



Ex.1006-Choi, Fig.1.

218. Choi also teaches a “first conductive type area 32” and a “second conductive type area 34.” Ex.1006-Choi, [0023]. Choi teaches that “[t]he first conductive type area 32 forms a back surface field structure.” Ex.1006-Choi, [0023]. Choi also teaches a “barrier area 36 interposed between the first conductive type area 32 and the second conductive type area 34 disposed on one surface (for example, back surface) of the semiconductor substrate 10.” Ex.1006-Choi, [0056]. The first and second conductive type areas 32 and 34 are shown at the bottom of solar cell 100 in Figure 1.

219. Choi also teaches “front surface field layer 120” formed on the front surface of the semiconductor substrate 10. Ex.1006-Choi, [0029] (“A front surface field layer 120 may be formed on the front surface of the semiconductor substrate

10 (that is, on the base area 110).”). Front surface field layer 120 is shown toward the top of solar cell 100 in Figure 1.

220. Choi also teaches an anti-reflective layer 50 formed on the front of solar cell 100. Ex.1006-Choi, [0030] (“[A]n anti-reflective film 50 may be formed on the front surface field layer 120.”). Anti-reflective layer 50 is shown at the top of solar cell 100 in Figure 1.

221. A person of ordinary skill in the art would have recognized that the top side of solar cell 100 in Figure 1 is a “front side” of solar cell 100 because Choi describes the layers at the top of the solar cell as “front” layers that are formed on the front surface of the semiconductor substrate. Likewise, a person of ordinary skill in the art would have recognized that the bottom side of solar cell 100 in Figure 1 is a “back side” of solar cell 100 because it describes layers at the bottom of the solar cell (specifically first conductive type area 32) as “back surface field structure” and explains that areas formed at the bottom of the solar cell are formed at the “back surface” of the semiconductor substrate.

222. Further, a person of ordinary skill in the art would have recognized that the front (top) side of solar cell 100 is “opposite” the back (bottom) side.

223. A person of ordinary skill in the art would have understood that the top (front) side of Choi's solar cell 100 *faces the sun during normal operation* for several reasons.

224. **First**, Choi teaches that the first and second conductive type areas 32 and 34 are formed on the tunneling layer 20, on the back surface of the semiconductor substrate. Ex.1006-Choi, [0023], [0056]. Choi also teaches that the base area 110 of the semiconductor substrate may be n-type doped, in which case the second conductive area 34 is p-type doped. Ex.1006-Choi, [0026] ("The base area 110 may have an n-type impurity as the first conductive-type dopant. As a result, the second conductive type area 34 forming a tunnel junction through the tunneling layer 20 with the base area 110 may be a p-type."). Based on Choi's disclosure of the structure of solar cell 100 and function of the base and first and second conductive type areas, a person of ordinary skill in the art would have recognized Choi's solar cell 100 as an IBC solar cell, which has a front surface that faces the sun during normal operation.

225. **Second**, Choi teaches that the anti-reflective layer 50 formed at the front surface of solar cell "decreases reflectivity of light incident upon the front surface of the semiconductor substrate." Ex.1006-Choi, [0030]. A person of ordinary skill in the art would have understood Choi's reference to "light incident

upon the front surface of the semiconductor substrate” to mean the sun, and therefore that the anti-reflective layer and the front surface of solar cell 100 face the sun during normal operation. Further, as I explained in Section VII.A, IBC solar cells, like Choi’s solar cell 100, often have anti-reflective layers on the front surface that face the sun during normal operation to increase the amount of light that reaches the substrate. Thus, a person of ordinary skill in the art would likewise have recognized that the top side of solar cell 100 in Figure 1 is on the front side of the solar cell and faces the sun during normal operation because it includes an anti-reflective layer.

226. *Third*, Choi teaches that the front surface of the semiconductor substrate is textured to have pyramidal shapes. Ex.1006-Choi, [0027] (“The front surface of the semiconductor substrate 10 is textured to have irregularities having a shape such as a pyramidal shape.”). Figure 1 shows the top side of solar cell 100 having pyramidal shapes. Ex.1006-Choi, Fig.1. Accordingly, a person of ordinary skill in the art would have understood that the top side of the solar cell in Figure 1 is the front surface of solar cell 100. Further, Choi teaches that such texturing reduces the amount of reflection of light incident on the front surface of the solar cell. Ex.1006-Choi, [0027] (“When surface roughness is increased due to irregularities formed on the front surface of the semiconductor substrate 10 through such texturing, reflection of light incident through the front surface of the semiconductor

substrate 10 can be reduced.”). Accordingly, a person of ordinary skill in the art would have understood that light is incident on the top, textured side of Choi’s solar cell 10 (i.e., the front side), and therefore recognized that the front side of solar cell 100 faces the sun during normal operation.

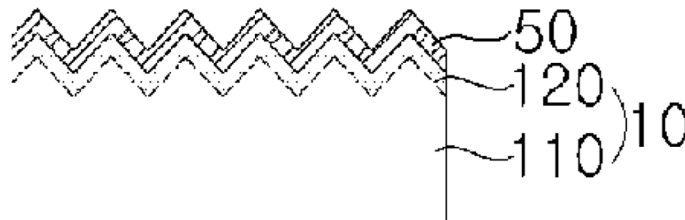
b. Element 10[a]: a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ and wherein the portion of the substrate is formed at the front side of the solar cell;

227. The combination of Choi and Granek or Marvin teaches *a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ and wherein the portion of the silicon substrate is formed at the front side of the solar cell.*

228. Choi teaches a solar cell that includes a “semiconductor substrate 10.” Ex.1006-Choi, [0023] (“[T]he solar cell 100 according to the present embodiment includes a semiconductor substrate”), [0059] (“In the present embodiment, the semiconductor substrate 10 may include silicon having an n-type impurity.”). Choi teaches that the semiconductor substrate can include, for example, a crystalline semiconductor, which Choi teaches can be crystalline silicon. Ex.1006-Choi, [0025] (“The semiconductor substrate 10 may, for example, include a crystalline semiconductor (for example, crystalline silicon) containing a first conductive-type

dopant.”). Choi further teaches that the crystalline semiconductor may be monocrystalline silicon. Ex.1006-Choi, [0025]. A person of ordinary skill in the art would have understood that Choi teaches a *silicon substrate*.

229. Choi teaches that the semiconductor substrate 10 can comprise two portions, a “base area 110” and a “front surface field layer 120,” as shown in Fig.1:



Ex.1006-Choi, Fig.1 (excerpted).

230. Specifically, Choi teaches that the semiconductor substrate can include a “base area” with a low dopant concentration of the “first conductive type dopant.” Ex.1006-Choi, [0024] (“The semiconductor substrate 10 may include a base area 110 containing a low doping concentration of first conductive type dopant.”). Choi further explains that the “first conductive type dopant” can be an n- or p-type dopant. Ex.1006-Choi, [0024] (“[T]he first conductive-type dopant may be, for example, an n-type or p-type dopant.”).

231. Choi also teaches that a front surface field layer can be formed on the front surface of the semiconductor substrate. Ex.1006-Choi, [0029] (“A front

surface field layer 120 may be formed on the front surface of the semiconductor substrate 10 (that is, on the base area 110).”).

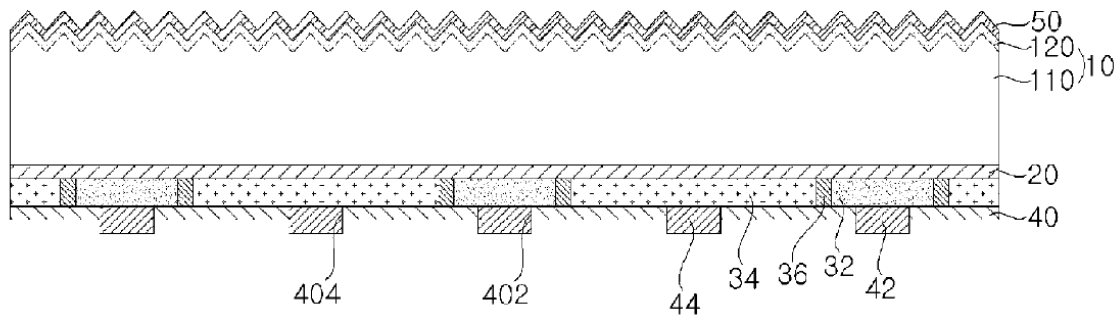
232. For at least two reasons, a person of ordinary skill in the art would have recognized that Choi’s front surface field layer is *a portion of the semiconductor substrate ... formed at the front side of the solar cell*.

233. **First**, as I explained in Sections X.A and XI.A.2.a, Choi teaches that the front surface field layer can be formed by doping the semiconductor substrate, and therefore the front surface field region is formed as a portion of the semiconductor substrate.

234. **Second**, Choi’s Figure 1 illustrates the semiconductor substrate 10 as comprising both the base area 110 and the front surface field layer 120. Figure 1 also shows the front surface field layer 120 is formed at the front side of the solar cell.

FIG. 1

100



Ex.1006-Choi, Fig.1.

235. A person of ordinary skill in the art would have also understood that the front surface field layer is doped with the same dopant type as the semiconductor substrate and thus the base area of the semiconductor substrate. Choi teaches that the front surface field layer can be formed with a dopant of the first conductive type (i.e., the same dopant type as the semiconductor substrate and thus the base area). Ex.1006-Choi, [0024] (“The front surface field layer 120 may be formed by doping a first conductive type dopant. For example, the front surface field layer 120 may be formed by doping the semiconductor substrate 10 with a first conductive type dopant by a variety of methods such as ion implantation or thermal diffusion.”).

236. Choi also teaches that the front surface field is doped with the first conductive type dopant at a higher concentration than the semiconductor substrate. Ex.1006-Choi, [0029] (“The front surface field layer 120 is an area where the first

conductive-type dopant is doped at a concentration higher than the semiconductor substrate 10 and performs similar functions to a back surface field (BSF) layer.”). While Choi teaches that the front surface field layer is doped at a higher dopant concentration than the semiconductor substrate, Choi does not provide a specific value for the dopant concentration.

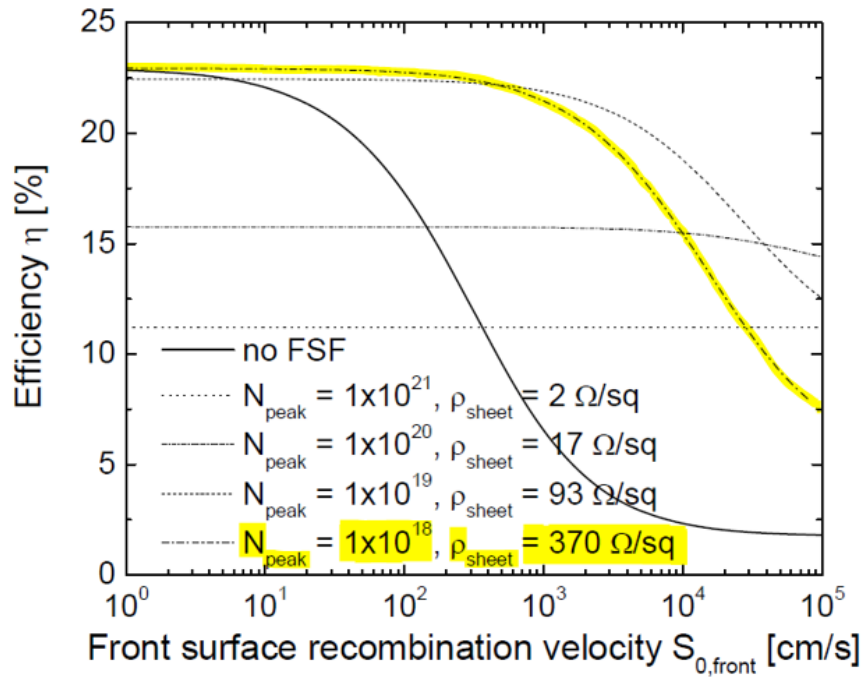
237. Choi, however, teaches that “the base area 110 not including the doping area may have a specific resistance of 0.5 ohm·cm to 20 ohm·cm.” Ex.1006-Choi, [0095]. A person of ordinary skill in the art would have recognized that a specific resistance of 0.5 ohm·cm to 20 ohm·cm corresponds to a silicon substrate dopant concentration of $6.7 \times 10^{14} \text{ cm}^{-3}$ to $3.3 \times 10^{16} \text{ cm}^{-3}$ for a p-type substrate, and $2.2 \times 10^{14} \text{ cm}^{-3}$ to $1.1 \times 10^{16} \text{ cm}^{-3}$ for an n-type silicon substrate. Well before the earliest priority date of the '315 patent, the relationship between specific resistance and doping concentration was well known for uniformly doped silicon, and charts, graphs, and other tools were available to calculate a doping concentration from a specific resistance value. Thus, a person of ordinary skill in the art would have understood that the front surface field region of Choi has a dopant concentration higher than $3.3 \times 10^{16} \text{ cm}^{-3}$ for a p-type substrate and $1.1 \times 10^{16} \text{ cm}^{-3}$ for an n-type substrate.

238. As I explained in Section VII.B.2.a, it was well known by 2014 that recombination would be reduced by optimizing the front surface field dopant

concentration of solar cells, and multiple publications and patents had disclosed that a FSF dopant concentration above $1 \times 10^{18} \text{ cm}^{-3}$ induced Auger recombination. Granek and Marvin specifically disclosed using a dopant concentration of *approximately less than or equal to* $2 \times 10^{18} \text{ cm}^{-3}$ in the front surface field to reduce recombination.

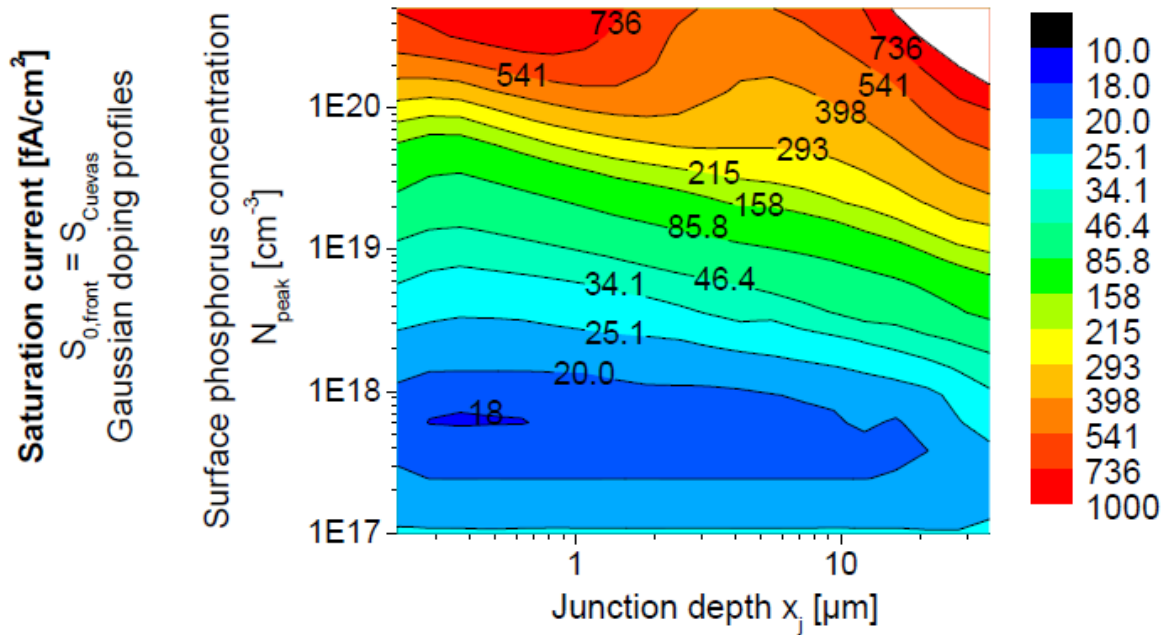
239. As I explained in Section X.C, Granek analyzes the performance of solar cells having different FSF dopant concentrations and teaches that “[a] lowly doped FSF results in high quantum efficiency” because “Auger recombination inside the highly doped region and the surface recombination velocity are low.” Ex.1010-Granek, 14, 117, 120. A person of ordinary skill in the art would have understood that the FSF of Granek is a *portion of the silicon substrate [] formed at the front side of the solar cell*.

240. As I explained in Section X.C, Granek simulates solar cells with dopant concentrations ranging from 1×10^{18} to $1 \times 10^{21} \text{ cm}^{-3}$ and shows that the solar cell having a FSF with a dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ had the highest efficiency. Ex.1010-Granek, 120-122. Figure 7-1 shows the simulated solar cell’s efficiency is highest when the FSF dopant concentration is $1 \times 10^{18} \text{ cm}^{-3}$, in particular for solar cells that have low front surface recombination velocity:



Ex.1010-Granek, 121, Fig.7-1 (annotated). As I explained in Section X.C, well passivated solar cells, like the solar cell taught by Choi, have low front surface recombination velocity, corresponding to the left side of the graph shown in Figure 7-1.

241. As I explained in Section X.C, Figure 7-3 of Granek shows the simulated solar cell's recombination level is lowest when the FSF dopant concentration is approximately $1 \times 10^{18} \text{ cm}^{-3}$.



Ex.1010-Granek, 122 Figure 7-3.

242. A person of ordinary skill in the art would have understood that the FSF with a surface dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ disclosed in Granek is a *portion of the silicon substrate [that] has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$.*

243. As I explained in Section XI.A.1.a, a person of ordinary skill in the art would have been motivated to alter Choi's solar cell in view of Granek and would have had a reasonable expectation of success in doing so. This would have entailed using Granek's FSF dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ in Choi's front surface field layer 120.

244. As I explained in Section X.D, Marvin was a study that evaluated the design of IBC solar cells (i.e., the same type of solar cell taught by Choi) for use in space applications. Ex.1008-Marvin, 5 (“The purpose of this study is to evaluate the IBC cell design for use in space missions.”). Specifically, the study sought to optimize the design of IBC solar cells under different constraints and to assess the effects of specific design parameters on cell performance. Ex.1008-Marvin, 9 (“The purpose of this study is to evaluate the usefulness of Interdigitated Back Contact (IBC) solar cells in space applications. The scope of the study includes optimization of the IBC cell design under several different constraints and assessment of the effects of certain design parameters on cell performance.”).

245. To increase solar cell efficiency, Marvin studied various “critical design parameters” of back-contact solar cells such as doping profiles and concentrations in a front surface field. Ex.1008-Marvin, 5, 9, 16 (this study “assess[es] [] the effects of certain design parameters on cell performance,” and “front surface field doping” was a “design parameter[] [] selected for study”). A person of ordinary skill in the art would have understood that the front surface field discussed in Marvin is a *portion of the silicon substrate [] formed at the front side of the solar cell*.

246. As I explained in Section X.D, Marvin teaches that “[t]he FSF effectiveness is relatively constant over a rather broad range around 1E17 to 1E18 cm⁻³, decreasing below this level due to the weakness of the electric field and decreasing above this level due to increased Auger recombination.” Ex.1008-Marvin, 15. A person of ordinary skill in the art would have understood that the FSF with a peak dopant concentration of 1E17 to 1E18 cm⁻³ disclosed by Marvin is a *portion of the silicon substrate [that] has a dopant concentration of approximately less than or equal to 2×10^{18} cm⁻³.*

247. As I explained in Section XI.A.1.a, a person of ordinary skill in the art would have been motivated to alter Choi’s solar cell in view of Marvin and would have had a reasonable expectation of success in doing so. This would have entailed using Marvin’s dopant concentration of 1E17 to 1E18 cm⁻³ in Choi’s front surface field layer 120.

248. In sum, the combination of Choi and Granek or Marvin teaches *a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal 2×10^{18} cm⁻³ and wherein the portion of the silicon substrate is formed at the front side of the solar cell.*

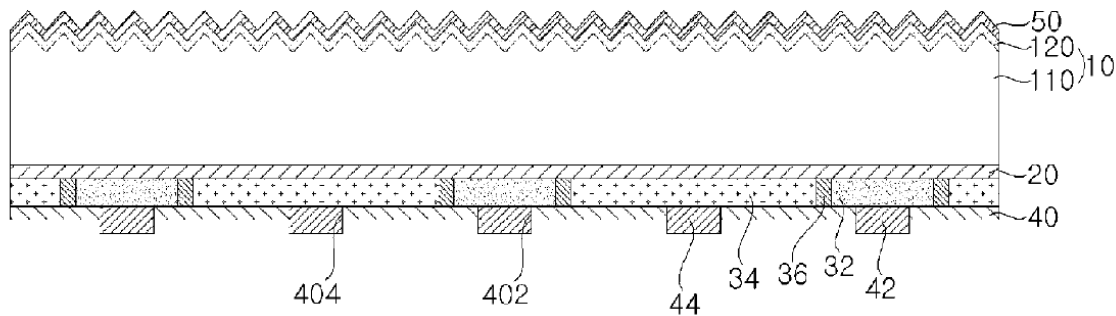
c. Element 10[b]: a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of the solar cell;

249. Choi teaches *a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of the solar cell.*

250. Choi teaches a “tunneling layer 20” formed on the back surface of the semiconductor substrate. Ex.1006-Choi, [0023] (“a tunneling layer 20 formed on one surface (for example, the back surface) of the semiconductor substrate 10”), [0033] (“In the present embodiment, a tunneling layer 20 is formed on the back surface of the semiconductor substrate 10. ... The tunneling layer 20 may be entirely formed on the back surface of the semiconductor substrate 10.”), [0062] (“[A] tunneling layer 20 is formed on the back surface of the semiconductor substrate 10.”). Figure 1 of Choi shows the tunneling layer 20 “formed over” the back side of the semiconductor substrate 10 and “formed over the back side of the solar cell”:

FIG. 1

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Ex.1006-Choi, Fig.1.

251. Figures 3A to 3K show “a method for manufacturing the solar cell.” Ex.1006-Choi, [0058]. Figure 3A shows the preparation of the silicon substrate 10 including a base area 110.” Ex.1006-Choi, [0059]. Figure 3B of Choi shows that subsequently the “tunneling layer 20 is formed on the back surface of the semiconductor substrate 10.” Ex.1006-Choi, [0062]. Choi teaches that “the tunneling layer 20 may be formed by a method such as thermal growth or deposition (for example, plasma-enhanced chemical vapor deposition chemical (PECVD), atomic layer deposition (ALD)) or the like.” Ex.1006-Choi, [0062]. Figures 3A and 3B show the tunneling layer 20 is “formed over” the silicon substrate 10 of Choi and “formed over the back side of the solar cell”:

FIG. 3a

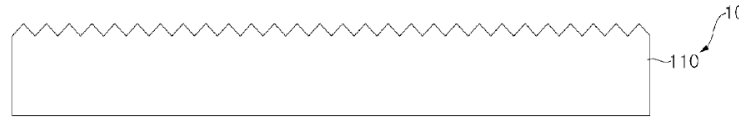
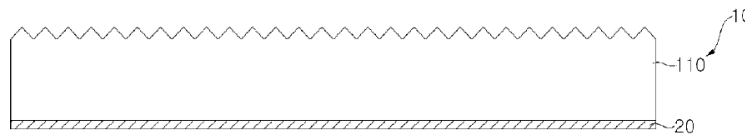


FIG. 3b



Ex.1006-Choi, Figs.3A, 3B.

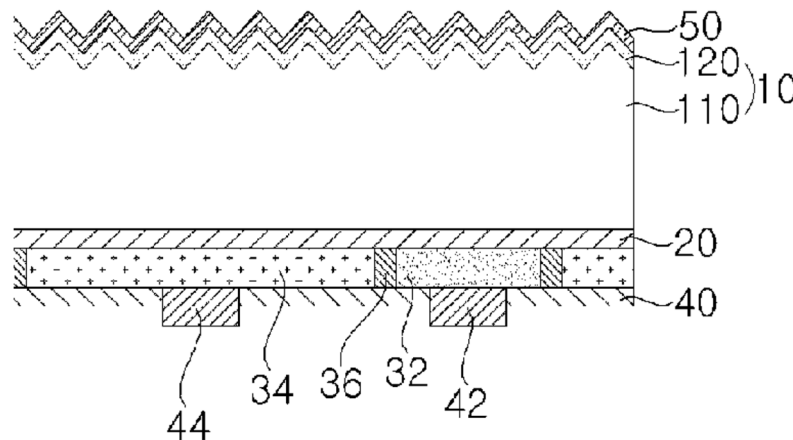
252. Choi teaches that the tunneling layer 20 can “include a variety of materials enabling tunneling of carriers” and specifically teaches oxides, nitrides, and conductive polymers as exemplary materials. Ex.1006-Choi, [0033]. A person of ordinary skill in the art would have understood that oxides and nitrides are dielectric materials. Thus, a person of ordinary skill in the art would have understood that Choi’s tunneling layer can be formed from dielectric materials.

253. A person of ordinary skill in the art would have understood that Choi’s tunneling layer 20 is *a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of the solar cell.*

d. Element 10[c]: a first emitter region having metal impurities formed over the dielectric region; and

254. The combination of Choi and Istratov teaches *a first emitter region having metal impurities formed over the dielectric region.*

255. Choi teaches “a first conductive type area 32 [and] a second conductive type area 34 ... formed on the tunneling layer 20.” Ex.1006-Choi, [0023], [0062]-[0064] (“[A] tunneling layer 20 is formed on the back surface of the semiconductor substrate 10 ... a semiconductor layer 30 is formed on the tunneling layer 20 ... [A] plurality of first conductive type areas 32 [and] second conductive type areas 34...are formed on the semiconductor layer 30.”). Figure 1 of Choi shows the first conductive type area 32 and the second conductive type area 34 are “formed over” the tunneling layer 20:

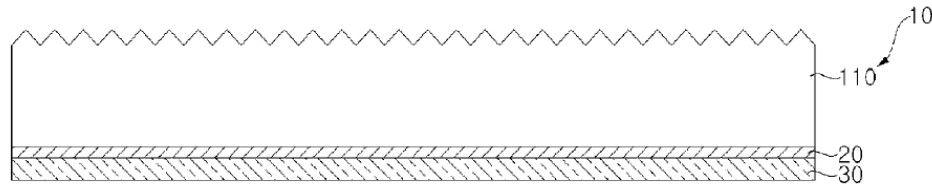


Ex.1006-Choi, Fig.1 (excerpted).

256. Figures 3A to 3K show “a method for manufacturing the solar cell.” Ex.1006-Choi, [0058]. Figure 3C shows “a semiconductor layer 30 [] formed on the tunneling layer 20.” Ex.1006-Choi, [0063]. “The semiconductor layer 30 may be formed by a method, for example, thermal growth, deposition (for example, plasma-

enhanced chemical vapor deposition chemical (PECVD)) or the like.” Ex.1006-Choi, [0063].

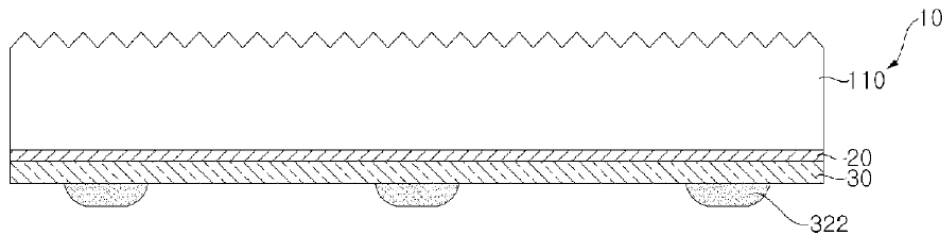
FIG. 3c



Ex.1006-Choi, Fig.3C.

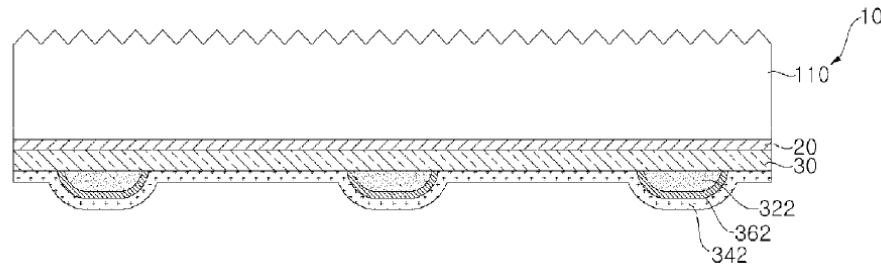
257. Figures 3D to 3G show “a plurality of first conductive type areas 32, a plurality of second conductive type areas 34, and a plurality of barrier areas 36 are formed on the semiconductor layer 30.” Ex.1006-Choi, [0064]. “[A]s shown in [Figure] 3D, a first doping layer 322 is formed in regions corresponding to the first conductive type areas 32.” Ex.1006-Choi, [0065].

FIG. 3d



Ex.1006-Choi, Fig.3D. “[A]s shown in [Figure] 3F, a second doping layer 342 [is] formed on the undoped layer 362 and the semiconductor layer 30.” Ex.1006-Choi, [0069].

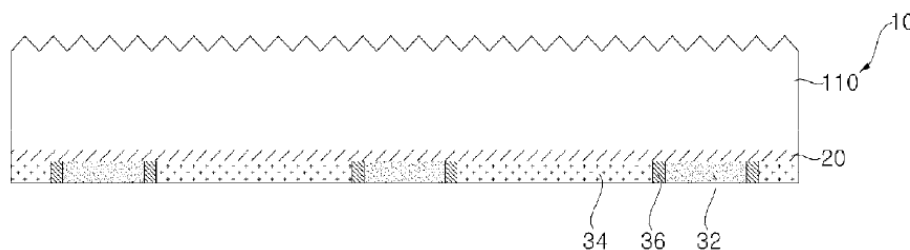
FIG. 3f



Ex.1006-Choi, Fig.3F. “Next, as shown in [Figure] 3G, the first conductive type dopant in the first doping layer 322 is diffused into the semiconductor layer 30 by thermal treatment to form a plurality of first conductive type areas 32, and the second conductive type dopant in the second doping layer 342 is diffused into the semiconductor layer 30 to form a plurality of second conductive type areas 34.”

Ex.1006-Choi, [0070].

FIG. 3g

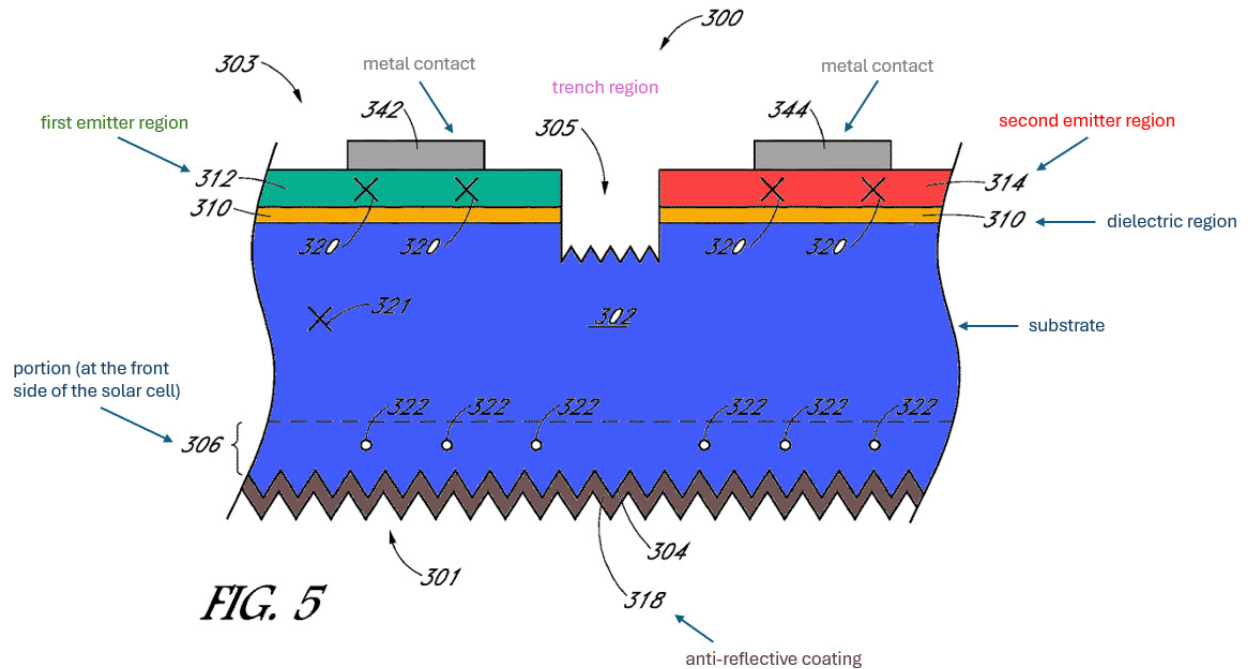


Ex.1006-Choi, Fig.3G. Thus, the first conductive type areas 32 and second conductive type areas 34 of Choi are “formed over” the tunneling layer 20.

258. As explained in Section XI.A.2.c, a person of ordinary skill in the art would have understood that Choi’s tunneling layer 20 is *the dielectric region*. Based

on the disclosures of Choi (e.g., Ex.1006-Choi, [0023], Fig.1), a person of ordinary skill in the art would have understood that Choi's second conductive type area 34 is *formed over the dielectric region*.

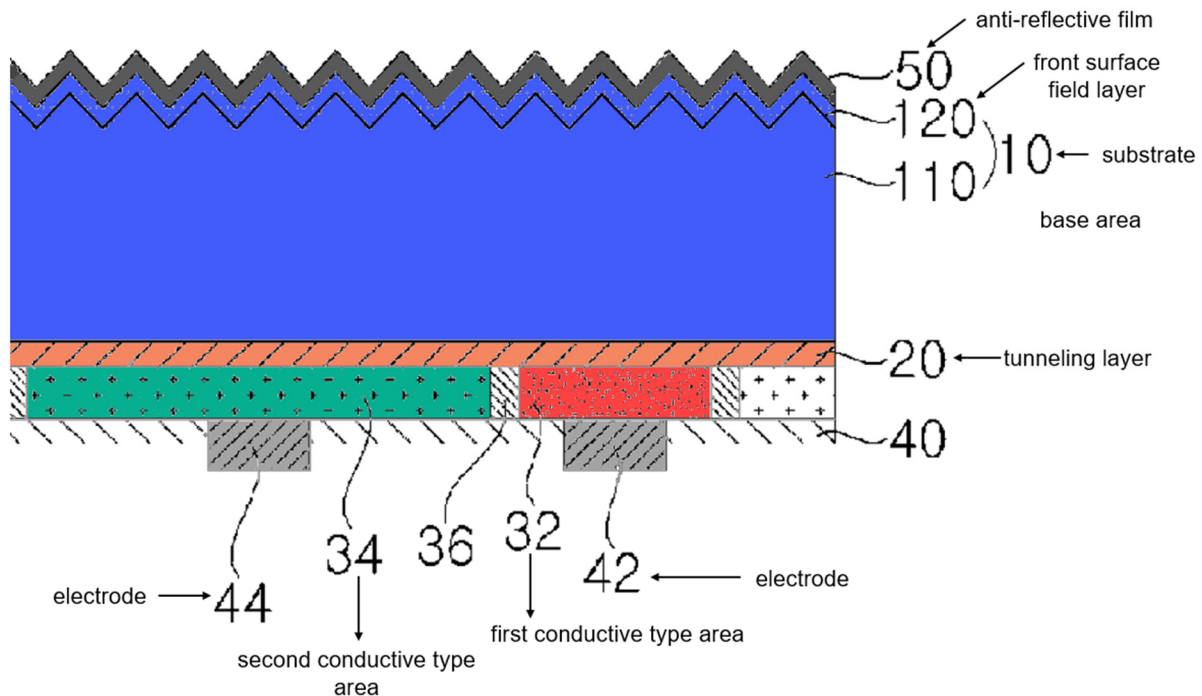
259. As I explained in Section VIII.A.1, the '315 patent refers to the p-type and n-type doped polysilicon regions formed over the **dielectric region 310 (orange)** in its Figure 5 (shown below) as the **first emitter region 312** and the **second emitter region 314**, respectively. Ex.1001-USP315, 6:55-57. In the embodiment of Figure 5, the substrate and "second emitter region" are n-type, and the "first emitter region" is p-type. Ex.1001-USP315, 6:40-57 ("the silicon substrate 302 can be an N-type silicon substrate," and "the first and second emitter regions 312, 314 can be P-type and N-type doped polysilicon regions, respectively"). Regarding the configuration of layers, Figure 5 of the '315 patent shows the **dielectric region 310 (orange)** is formed over the **silicon substrate 302**, and the **first emitter region 312 (green)** and **second emitter region 314 (red)** are formed over the **dielectric region 310 (orange)**. Ex.1001-USP315, 6:50-62.



Ex.1001-USP315, Fig.5 (annotated).

260. Choi teaches the same structures as the first emitter region 312 and the second emitter region 314 of the '315 patent. Like the '315 patent, Choi also teaches p-type and n-type doped structures formed over the dielectric tunneling region 20—“first conductive type area 32” and “second conductive type area 34,” respectively.

Ex.1006-Choi, [0023], Fig.1.



Ex.1006-Choi, Fig.1 (excerpted and annotated).

261. Choi further teaches that the first and second conductive type areas 32, 34 may be “formed by doping ... polycrystalline silicon ... with a [first or second] conductive type dopant.” Ex.1006-Choi, [0036]-[0037]. As I explained in Section VII.A, a person of ordinary skill in the art would have understood that polycrystalline silicon is polysilicon. Ex.1072-Komp, 37-38; Ex.1023-Nelson, 179.

262. Choi also teaches the same arrangement of layers as the '315 patent for the claimed “substrate,” “dielectric region,” and “first emitter region.” As shown in Figure 5 of the '315 patent, the “first emitter region” is “formed over the dielectric region,” and the “dielectric region” is “formed over the silicon substrate” and “the back side of the solar cell.” Ex.1001-USP315, cl.10. The “second conductive type

area 34” of Choi is likewise “formed on the tunneling layer 20,” and the “tunneling layer 20” is “formed on ... the back surface[] of the semiconductor substrate 10.” Ex.1006-Choi, [0023], [0033], [0062], Fig.1.

263. Choi teaches the second conductive type area 34 is the same doping type as the p-type first emitter region 312 of Figure 5 of the '315 patent, and the first conductive type area 32 is the same doping type as the n-type second emitter region 314 of Figure 5. Ex.1001-USP315, 6:40-57. Choi teaches that the substrate and the first conductive type area 32 have the same type doping, which may be “an n-type dopant.” Ex.1006-Choi, [0036] (“the first conductive type area 32” has “a first conductive type dopant,” which may be “an n-type dopant” and may be “the same conductive type as the semiconductor substrate 10”). Choi further teaches that the second conductive type area 34 has the opposite type doping, which may be “a p-type dopant.” Ex.1006-Choi, [0037] (“The second conductive type area 34 may ... hav[e] a conductive type opposite to the semiconductor substrate 10 ... when the second conductive type dopant is a p-type dopant”), [0026] (“the second conductive type area 34 ... may be a p-type”), [0041] (“the base area 110 and the first conductive type area 32 have an n-conductive type and the second conductive type area 34 has a p-conductive type”). Thus, like the first emitter region 312 and the second emitter region 314 of the '315 patent, which are p-type and n-type doped

polysilicon regions, respectively, Choi's first and second conductive type areas 32, 34 are p-type and n-type doped polysilicon regions, respectively.

264. Further, the functions of the first and second conductive type areas 32 and 34 of Choi are the same as the first emitter region 312 and the second emitter region 314 of the '315 patent. As I discussed above in Section VIII.A.1, the '315 patent teaches the first emitter region 312 and the second emitter region 314 are "doped region[s] of a solar cell for collecting positive and negative charge carriers." Ex.1001-USP315, 2:40-42. The '315 patent teaches that, in one embodiment, the substrate is N-type, while the first emitter region is P-type. Ex.1001-USP315, 6:45-46, 6:55-57. As such, the first emitter region forms a PN junction with the silicon substrate.

265. Choi likewise teaches that "the first and second electrodes 42 and 44 [] are connected to first and second conductive type areas 32 and 34, respectively, and collect carriers" "and transport the same to the outside." Ex.1006-Choi, [0023], [0044]. Choi further states: "The second conductive type area 34 forms a tunnel junction with the semiconductor substrate 10 through the tunneling layer 20, thus substantially contributing to photoelectric transformation." Ex.1006-Choi, [0037]. Because Choi's second conductive type area 34 has the opposite type doping to the substrate 10 (Ex.1006-Choi, [0037], [0041]), it forms a PN junction with the

substrate and the resulting electric field directs one type of charge carrier (e.g., holes) to the second electrode 44. Thus, like the first and second emitter regions 312 and 314 of the '315 patent, the first and second conductive type areas 32 and 34 of Choi collect positive and negative charge carriers that are transported to their respective metal contacts. Ex.1001-USP315, 2:40-42.

266. Based on the structure, arrangement, and function of the first emitter region in the '315 patent, a person of ordinary skill in the art would have understood that the claimed “first emitter region” corresponds to Choi’s “second conductive type area 34.” A person of ordinary skill in the art would have understood that Choi’s second conductive type area 34 is *a first emitter region ... formed over the dielectric region*.

267. Choi teaches that each of the first and second conductive type areas 32, 34 may be doped with either p-type or n-type impurities in different embodiments. Ex.1006-Choi, [0026]. Choi further teaches the “first conductive type area 32 ha[s] a first conductive type dopant,” and the “second conductive type area 34 ha[s] a second conductive type dopant.” Ex.1006-Choi, [0035]. Choi explains that “the first conductive-type dopant” may be an “n-type impurity” such as phosphorus, arsenic, bismuth, or antimony (Group III elements), or alternatively, a “p-type

impurity” such as boron, aluminum, gallium, or indium (Group V elements).
Ex.1006-Choi, [0025].

268. A person of ordinary skill in the art would have understood that at least bismuth, aluminum, gallium, and indium are metals. Thus, to the extent that the Patent Owner argues that the claimed invention includes any metal or any source of metal, a person of ordinary skill in the art would have understood that Choi’s first and second conductive type areas 32, 34 *have metal impurities*.

269. Choi in combination with Istratov also teaches and renders obvious *a first emitter region having metal impurities*.

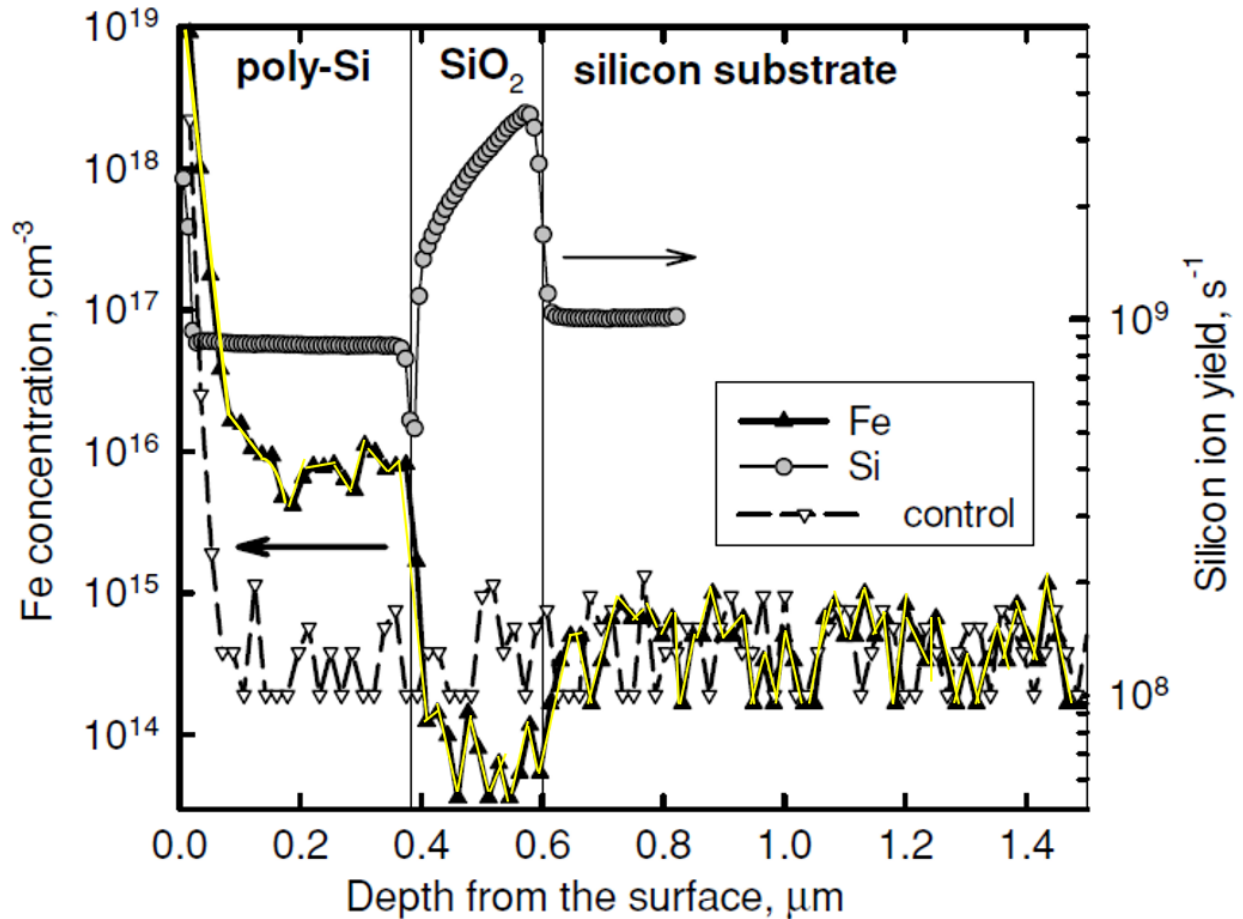
270. As explained in Section VII.B.2.b, gettering to move metal impurities from the substrate into the emitter was well known and described and studied in multiple publications by 2014.

271. Istratov teaches a silicon device structure having the same layers as Choi—specifically, a test structure comprising a silicon substrate, an oxide layer, and a polysilicon layer. Ex.1012-Istratov, 570 (“a poly-Si/SiO₂ structure, which consisted of 197 nm thick thermal oxide grown on a standard 4 in. 10 Ω cm substrate, covered by a 370 nm cap layer of CVD-grown polysilicon”), Fig.2.

272. Istratov further teaches techniques for gettering metal impurities into a polysilicon region. Specifically, Istratov describes results from an experiment that

introduced either iron or copper contamination on the back side of the substrate. Ex.1012-Istratov, 570 (“Iron contamination was performed by scratching the backside of the sample (i.e., the side opposite to the side on which poly-Si/SiO₂ was deposited) with a 99.999% pure iron wire.”), 571 (“Copper contamination was performed by scratching the backside of the wafer with a copper wire.”).

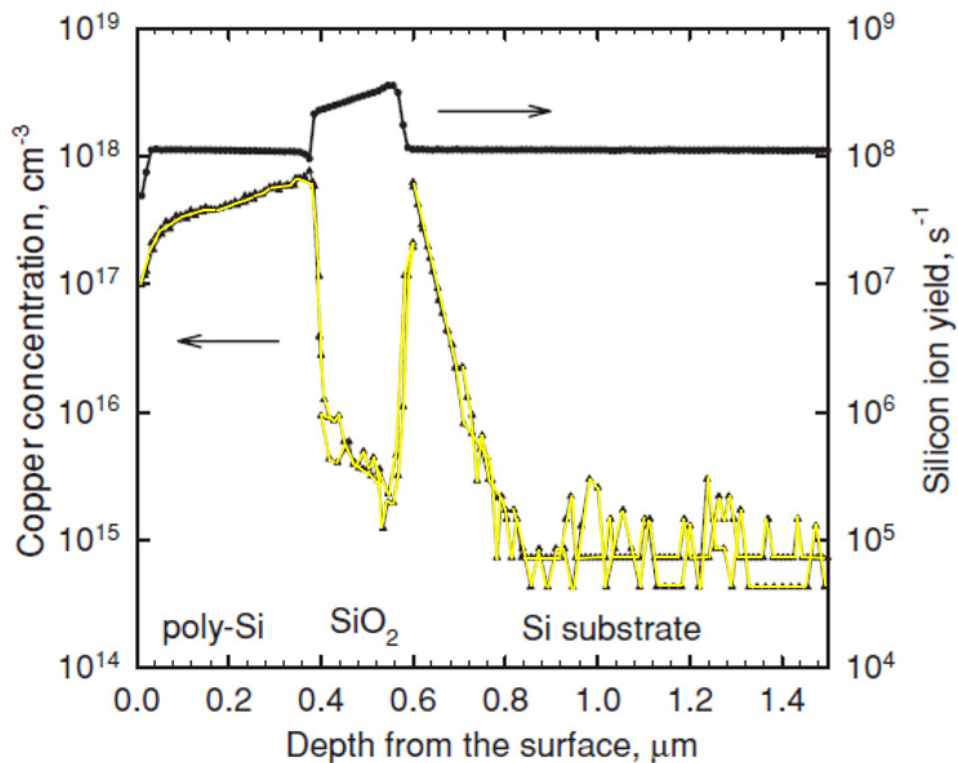
273. After the iron contamination, “annealing for 8 h[ours] at 1020° C” was performed on the test structure, resulting in iron diffusion through the test structure. Ex.1012-Istratov, 570. The iron depth profile was measured after annealing, and the results were presented in Istratov’s Figure 2:



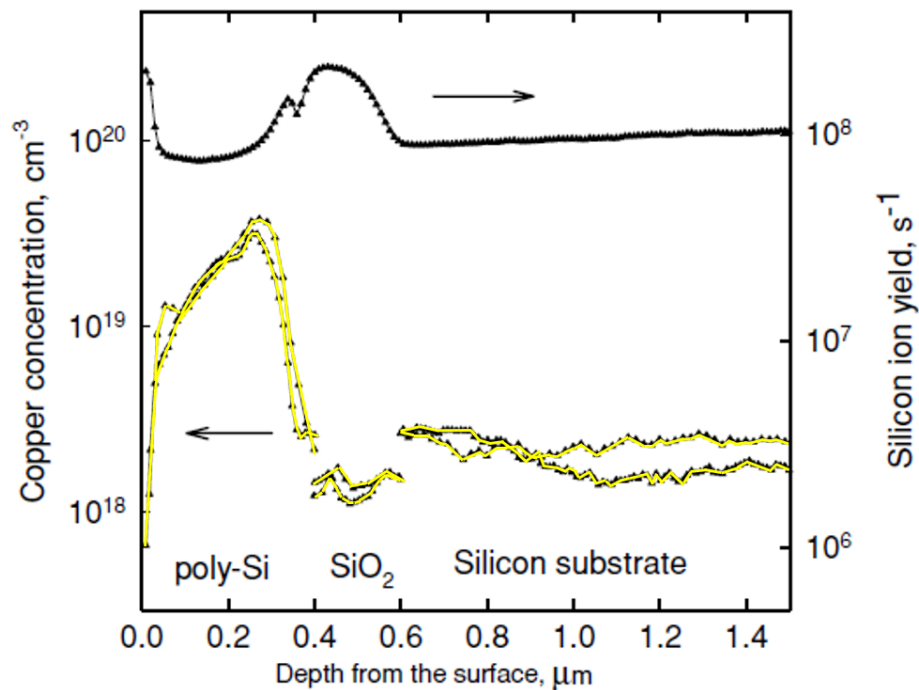
Ex.1012-Istratov, 570, Fig.2 (annotated).

274. Figure 2 shows iron impurities in the polysilicon layer following annealing. Specifically, Figure 2 teaches a higher iron concentration in the polysilicon layer than in the silicon substrate. Ex.1012-Istratov, Fig.2, 570 (in figure 2, “the solubility of iron in poly-silicon ... is more than an order of magnitude higher than in the silicon substrate,” which is “interpret[ed]” “as segregation gettering of iron by the poly-silicon”).

275. After the copper contamination, the test structure was heated either “at 690 °C for 5 h[ours]” or “at 1150 °C for 2 h[ours],” which also resulted in copper diffusion through the test structure. Ex.1012-Istratov, 571. The copper depth profiles after annealing were presented in Istratov’s Figures 4 and 5:



Ex.1012-Istratov, 571, Fig.4 (annotated).



Ex.1012-Istratov, 571, Fig.5 (annotated). Istratov concludes that “[t]he higher concentration of Cu in the poly-silicon layer can be interpreted as segregation of Cu at structural defects in the poly-silicon layer.” Ex.1012-Istratov, 571.

276. As I explained in Section XI.A.1.b, a person of ordinary skill in the art would have been motivated to alter the Choi-Marvin and Choi-Granek solar cells in view of Istratov and would have had a reasonable expectation of success in doing so. Specifically, this combination would have entailed using Istratov’s gettering technique to getter metal impurities from Choi’s substrate into the second conductive type area 34, which a person of ordinary skill in the art would have understood to have the same structure, arrangement, and function as—i.e., to correspond to—the claimed “first emitter region” of the ’315 patent. Choi’s solar cell has the same

layers as the test structure of Istratov, and a person of ordinary skill in the art would therefore have recognized that the combination of Choi with Istratov would have resulted in the relocation of metal impurities such as iron and copper (to the extent these impurities were present in the substrate prior to gettering) to the second conductive type area 34 of Choi. Ex.1012-Istratov, 569-571, Figs.2, 4-5; Ex.1006-Choi, [0023], [0033], [0036]-[0037]. Istratov's disclosure of moving iron or copper metal impurities from the substrate through the silicon dioxide layer and relocating them to the polysilicon layer would have been desirable in the similar solar cell structure of Choi to reduce recombination and improve solar cell efficiency.

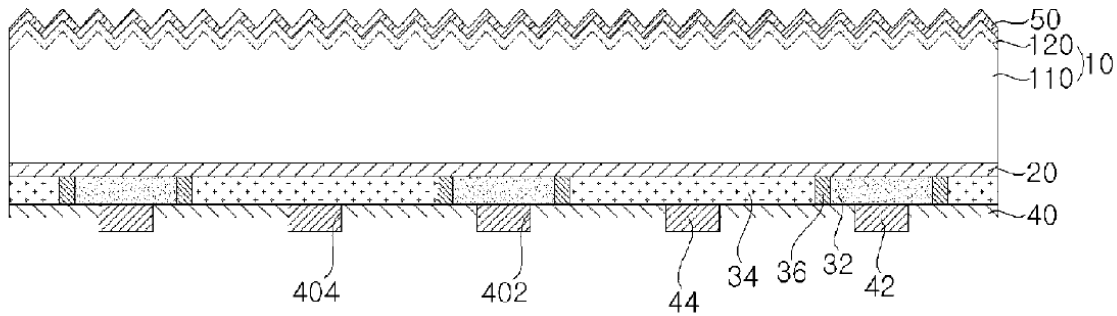
e. Element 10[d]: a first metal contact formed over the first emitter region.

277. Choi teaches *a first metal contact formed over the first emitter region*.

278. Choi teaches "first and second electrodes 42 and 44 which are connected to first and second conductive type areas 32 and 34, respectively," which are shown below in Figure 1. Ex.1006-Choi, [0023], [0044], [0076], Fig.1.

FIG. 1

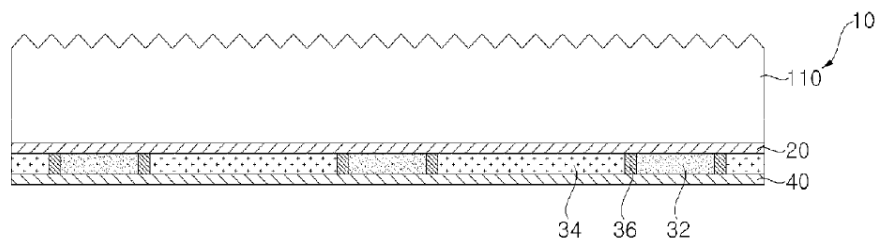
100



Ex.1006-Choi, Fig.1. Figure 1 shows that the second electrode 44 is “formed over” the second conductive type area 34. Ex.1006-Choi, Fig.1.

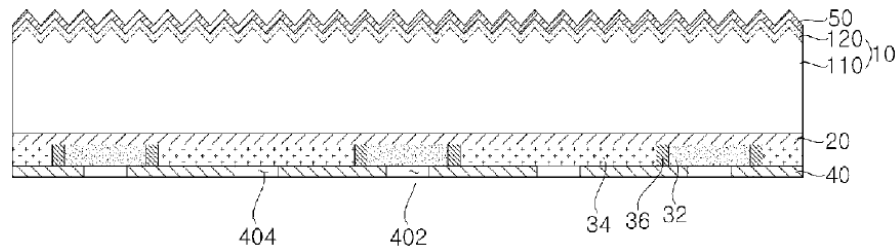
279. As I explained above in Section XI.A.2.d, Figures 3A to 3K show “a method for manufacturing the solar cell.” Ex.1006-Choi, [0058]. After the first and second conductive type areas 32 and 34 are formed, “an insulating layer 40 is formed on the first and second conductive type areas 32 and 34 and the barrier area 36,” as shown in Figure 3H. Ex.1006-Choi, [0070], [0072].

FIG. 3h



Ex.1006-Choi, Fig.3H. Figure 3J shows that “openings 402 and 404 exposing the first and second conductive type areas 32 and [34] are formed.” Ex.1006-Choi, [0076].

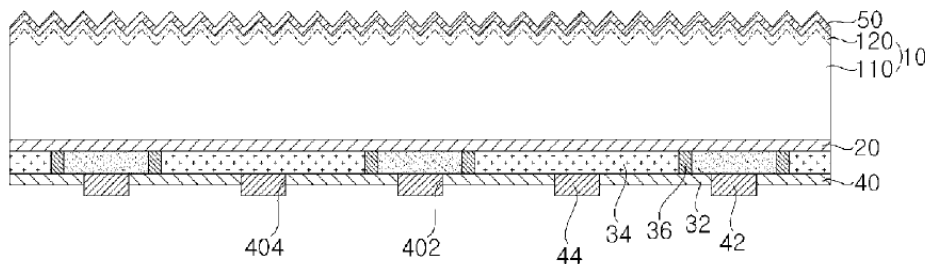
FIG. 3j



Ex.1006-Choi, Fig.3J.

280. Next, “as shown in [Figure]3K, first and second electrodes 42 and 44 electrically connected to the first and second conductive type areas 32 and 34, respectively, are formed ..., for example, ... by a variety of methods such as coating or deposition.” Ex.1006-Choi, [0076].

FIG. 3k



Ex.1006-Choi, Fig.3K. Thus, the first electrode 42 is “formed over” the first conductive type area 32, and the second electrode 44 is “formed over” the second conductive type area 34.

281. As I explained in Section XI.A.2.d, a person of ordinary skill in the art would have understood Choi’s second conductive type area 34 is the *first emitter region*. Thus, a person of ordinary skill in the art would have understood that the second electrode 44 is *formed over the first emitter region*.

282. Choi teaches that the first and second electrodes 42, 44 can include a variety of metal materials, and can be formed by a variety of methods, including coating or deposition. Ex.1006-Choi, [0044], [0076]. A person of ordinary skill in the art would have understood that Choi’s first and second electrodes 42, 44 are *metal contacts*. A person of ordinary skill in the art would have understood that Choi’s second electrode 44 is *a first metal contact formed over the first emitter region*.

3. Claim 11: The solar cell of claim 10, wherein the portion of the silicon substrate comprises N-type dopants.

283. Claim 11 depends from claim 10. Therefore, I incorporate by reference my discussion of claim 10 in Sections XI.A.1.

284. The combination of Choi, Granek or Marvin, and Istratov further teaches *the portion of the silicon substrate comprises N-type dopants*. Choi teaches

a front surface field layer having a “first conductive-type dopant” (i.e., the same dopant type as the semiconductor substrate). Ex.1006-Choi, [0025] (“The semiconductor substrate 10 may, for example, include a crystalline semiconductor ... having a first conductive-type dopant.”), [0029] (“The front surface field layer 120 is an area where the first conductive-type dopant is doped at a concentration higher than the semiconductor substrate 10.”).

285. Choi further teaches that the “first conductive-type dopant” can be an N-type dopant. Ex.1006-Choi, [0025] (“[T]he first conductive-type dopant may be, for example, an n-type impurity.”). Accordingly, Choi teaches *the portion of the silicon substrate comprises N-type dopants*.

4. Claim 12: The solar cell of claim 10, wherein the portion of the silicon substrate comprises phosphorus.

286. Claim 12 depends from claim 10. Therefore, I incorporate by reference my discussion of claim 10 in Section XI.A.2.

287. The combination of Choi, Granek or Marvin, and Istratov further teaches *the portion of the silicon substrate comprises phosphorus*. Choi teaches a front surface field layer having a “first conductive-type dopant” (i.e., the same dopant type as the semiconductor substrate). Ex.1006-Choi, [0025] (“The semiconductor substrate 10 may, for example, include a crystalline semiconductor ... having a first conductive-type dopant.”), [0029] (“The front surface field layer

120 is an area where the first conductive-type dopant is doped at a concentration higher than the semiconductor substrate 10.”).

288. Choi further teaches that the “first conductive-type dopant” can be phosphorus. Ex.1006-Choi, [0025] (“[T]he first conductive-type dopant may be an n-type impurity such as ... phosphorous.”). Accordingly, Choi teaches *the portion of the silicon substrate comprises phosphorus*.

5. Claim 13: The solar cell of claim 10, wherein the portion of the silicon substrate comprises P-type dopants.

289. Claim 13 depends from claim 10. Therefore, I incorporate by reference my discussion of claim 10 in Section XI.A.2.

290. The combination of Choi, Granek or Marvin, and Istratov further teaches *the portion of the silicon substrate comprises P-type dopants*. Choi teaches a front surface field layer having a “first conductive-type dopant” (i.e., the same dopant type as the semiconductor substrate). Ex.1006-Choi, [0025] (“The semiconductor substrate 10 may, for example, include a crystalline semiconductor ... having a first conductive-type dopant.”), [0029] (“The front surface field layer 120 is an area where the first conductive-type dopant is doped at a concentration higher than the semiconductor substrate 10.”).

291. Choi further teaches that the “first conductive-type dopant” can be P-type dopant. Ex.1006-Choi, [0025] (“Alternatively, the first conductive-type dopant

may be, for example, a p-type impurity.”). Accordingly, Choi teaches *the portion of the silicon substrate comprises P-type dopants*.

6. **Claim 14: The solar cell of claim 10, wherein the portion of the silicon substrate comprises boron.**

292. Claim 14 depends from claim 10. Therefore, I incorporate by reference my discussion of claim 10 in Section XI.A.2.

293. The combination of Choi, Granek or Marvin, and Istratov further teaches *the portion of the silicon substrate comprises boron*. Choi teaches a front surface field layer having a “first conductive-type dopant” (i.e., the same dopant type as the semiconductor substrate). Ex.1006-Choi, [0025] (“The semiconductor substrate 10 may, for example, include a crystalline semiconductor ... having a first conductive-type dopant.”), [0029] (“The front surface field layer 120 is an area where the first conductive-type dopant is doped at a concentration higher than the semiconductor substrate 10.”).

294. Choi further teaches that the “first conductive-type dopant” can be boron. Ex.1006-Choi, [0025] (“Alternatively, the first conductive-type dopant may be a p-type impurity such as ... boron.”). Accordingly, Choi teaches *the portion of the silicon substrate comprises boron*.

7. **Claim 15: The solar cell of claim 10, wherein the first emitter region comprises polysilicon.**

295. Claim 15 depends from claim 10. Therefore, I incorporate by reference my discussion of claim 10 in Section XI.A.2.

296. The combination of Choi, Granek or Marvin, and Istratov further teaches *the first emitter region comprises polysilicon*. As I explained in Section XI.A.2.d, a person of ordinary skill in the art would have understood that Choi's second conductive type area 34 is *the first emitter region*.

297. Choi further teaches that the first and second conductive type areas 32 and 34 can comprise polysilicon. Specifically, Choi teaches that the first and second conductive type areas can be formed by doping polysilicon with a first and second dopant type, respectively. Ex.1006-Choi, [0036] (“For example, the first conductive type area 32 may be easily formed by doping amorphous silicon, microcrystalline silicon, polycrystalline silicon or the like with a first conductive type dopant.”), [0037] (“For example, the second conductive type area 34 may be easily formed by doping amorphous silicon, microcrystalline silicon, polycrystalline silicon or the like with a second conductive type dopant.”).

298. Choi further teaches a “barrier 36” disposed between the first and second conductive type areas. Ex.1006-Choi, [0038] (“In addition, the barrier area 36 is disposed between the first conductive type area 32 and the second conductive

type area 34 and separates the first conductive type area 32 from the second conductive type area 34.”). Choi explains that the first and second conductive type areas and the barrier can include an identical semiconductor material, such as polycrystalline silicon. Ex.1006-Choi, [0039] (“In this case, the first and second conductive type areas 32 and 34, and the barrier area 36 are flush with one another and may include an identical semiconductor material (for example, amorphous silicon, microcrystalline silicon or polycrystalline silicon).”). As I explained in Section VII.A, a person of ordinary skill in the art would have understood that “polycrystalline silicon” means polysilicon. Ex.1072-Komp, 37-38; Ex.1023-Nelson, 179.

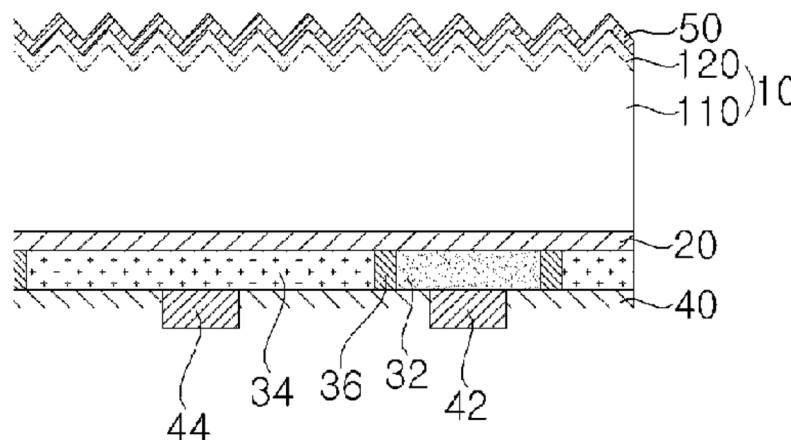
299. Accordingly, Choi teaches *the first emitter region comprises polysilicon.*

8. Claim 16

300. Claim 16 depends from claim 10. Therefore, I incorporate by reference my discussion of claim 10 in Section XI.A.2. The combination of Choi, Granek or Marvin, and Istratov further teaches *a second emitter region having metal impurities formed over the dielectric region; and a second metal contact formed over the second emitter region.*

a. Element 16[a]: The solar cell of claim 10, further comprising: a second emitter region having metal impurities formed over the dielectric region; and

301. Choi teaches “a first conductive type area 32 [and] a second conductive type area 34 ... formed on the tunneling layer 20.” Ex.1006-Choi, [0023], [0062]-[0064] (“[A] tunneling layer 20 is formed on the back surface of the semiconductor substrate 10 ... a semiconductor layer 30 is formed on the tunneling layer 20 ... [A] plurality of first conductive type areas 32 [and] second conductive type areas 34 ... are formed on the semiconductor layer 30.”). Figure 1 of Choi shows the first conductive type area 32 and the second conductive type area 34 are “formed over” the tunneling layer 20:

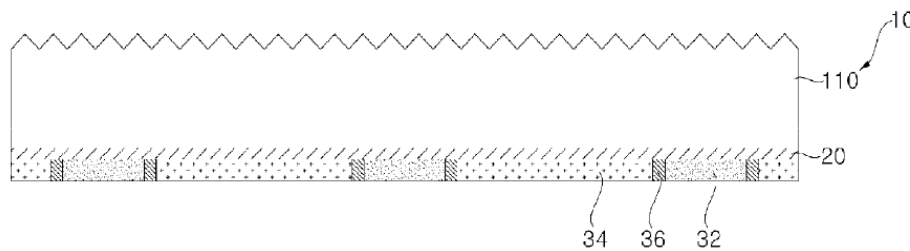


Ex.1006-Choi, Fig.1 (excerpted).

302. As I explained in XI.A.2.d, Figures 3D to 3G of Choi show “a plurality of first conductive type areas 32, [and] a plurality of second conductive type areas

34, ... formed on the semiconductor layer 30.” Ex.1006-Choi, [0064]. “[A]s shown in [Figure] 3G, the first conductive type dopant in the first doping layer 322 is diffused into the semiconductor layer 30 by thermal treatment to form a plurality of first conductive type areas 32, and the second conductive type dopant in the second doping layer 342 is diffused into the semiconductor layer 30 to form a plurality of second conductive type areas 34.” Ex.1006-Choi, [0070].

FIG. 3g



Ex.1006-Choi, Fig.3G. Thus, the first conductive type areas 32 and second conductive type areas 34 of Choi are “formed over” the tunneling layer 20.

303. As I explained in Section XI.A.2.d, a person of ordinary skill in the art would have understood that Choi’s second conductive type area 34 is *the first emitter region*. As I explained in Section XI.A.2.c, a person of ordinary skill in the art would have understood that Choi’s tunneling layer 20 is *the dielectric region*. Based on the disclosures of Choi (e.g., Ex.1006-Choi, [0023], Fig.1), a person of ordinary skill in the art would have understood that Choi’s second conductive type area 34 is *formed over the dielectric region*.

304. As I explained in Sections XI.A.2.d, Choi teaches the first conductive type area 32 has the same structure and the same doping type as the second emitter region 314 of the '315 patent. Like the second emitter region of the '315 patent (Sections VIII.A.1, XI.A.2.d), Choi's first conductive type area 32 is a n-type doped polysilicon region. Ex.1006-Choi, [0036] ("the first conductive type area 32 may be [] formed by doping ... polycrystalline silicon or the like," and "the first conductive type area 32" has "a first conductive type dopant," which may be "an n-type dopant").

305. Choi also teaches the same arrangement of layers as the '315 patent for the claimed "substrate," "dielectric region," and "second emitter region." As shown in Figure 5 of the '315 patent (*see* above Sections VIII.A.1, XI.A.2.c, XI.A.2.d), the "second emitter region" is "formed over the dielectric region," and the "dielectric region" is "formed over the silicon substrate" and "the back side of the solar cell." Ex.1001-USP315, cl.10, 16. The "first conductive type area 32" of Choi is likewise "formed on the tunneling layer 20," and the "tunneling layer 20" is "formed on ... the back surface[] of the semiconductor substrate 10." Ex.1006-Choi, [0023], [0033], [0062], Fig.1.

306. As I explained in Section XI.A.2.d, Choi teaches that the function of the first conductive type area 32 is the same as the second emitter region 314 of the

'315 patent. Ex.1001-USP315, 2:40-42 (“an emitter region can be a doped region of a solar cell for collecting positive and negative charge carriers”); Ex.1006-Choi, [0023], [0044] (“carriers” are “collect[ed]” and “transport[ed] ... to the outside” through the first and second conductive type areas 32 and 34 and the first and second electrodes 42 and 44).

307. Based on the structure, arrangement, and function of the second emitter region in the '315 patent, a person of ordinary skill in the art would have understood that the claimed “second emitter region” corresponds to Choi’s “first conductive type area 32.” A person of ordinary skill in the art would have understood that Choi’s first conductive type area 32 is *a second emitter region ... formed over the dielectric region*.

308. As I explained above (Section XI.A.2.d), to the extent that the Patent Owner argues that the claimed invention includes any metal or any source of metal, a person of ordinary skill in the art would have understood that Choi’s first conductive type area 32 *has metal impurities*.

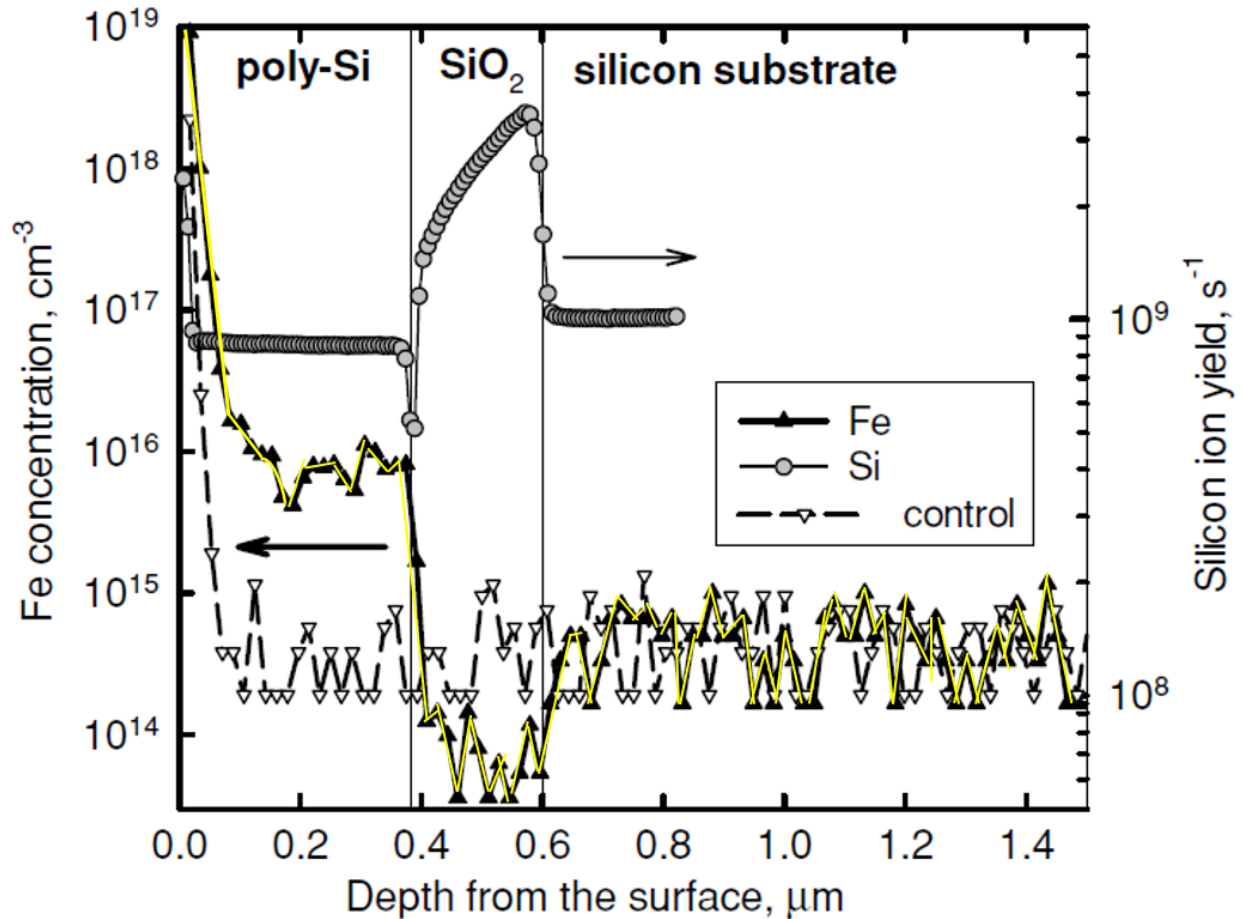
309. Choi in combination with Istratov also teaches or renders obvious *a second emitter region having metal impurities formed over the dielectric region*.

310. For the same reasons I explained with respect to Element 10[c], getting to move metal impurities from the substrate into the emitter was well

known and described and studied in multiple publications by 2014. *See above* Sections XI.A.2.d, VII.B.2.b.

311. As I explained in Section XI.A.1.b, Istratov teaches a silicon device structure having the same layers as Choi—specifically, a test structure comprising a silicon substrate, an oxide layer, and a polysilicon layer. Ex.1012-Istratov, 570 (“a poly-Si/SiO₂ structure, which consisted of 197 nm thick thermal oxide grown on a standard 4 in. 10 Ω cm substrate, covered by a 370 nm cap layer of CVD-grown polysilicon.”), Fig.2.

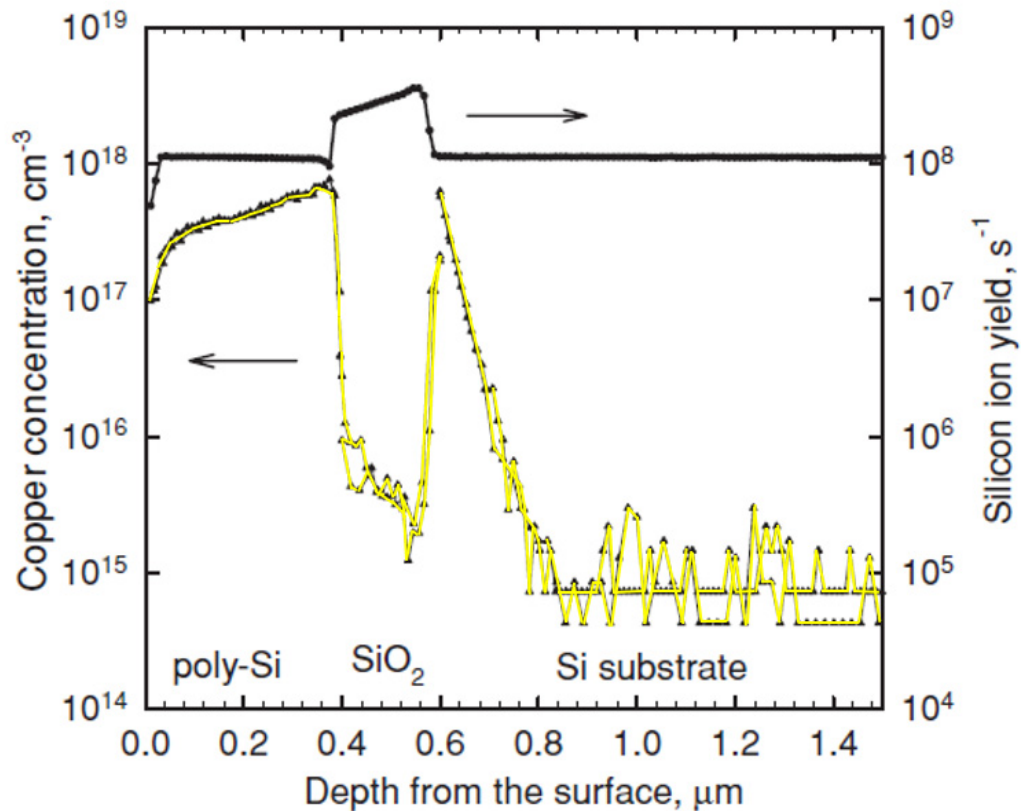
312. Istratov further teaches techniques for gettering metal impurities (iron or copper) into the polysilicon layer. For gettering of iron, Istratov describes results from an experiment in which iron contamination was introduced on the back side of the substrate. Ex.1012-Istratov, 570 (“Iron contamination was performed by scratching the backside of the sample (i.e., the side opposite to the side on which poly-Si/SiO₂ was deposited) with a 99.999% pure iron wire.”), 571 (“Copper contamination was performed by scratching the backside of the wafer with a copper wire.”). After the iron contamination, “annealing for 8 h[ours] at 1020° C” was performed on the test structure, resulting in iron diffusion through the test structure. Ex.1012-Istratov, 570. The iron depth profile was measured after annealing, and the results were presented in Istratov’s Figure 2:



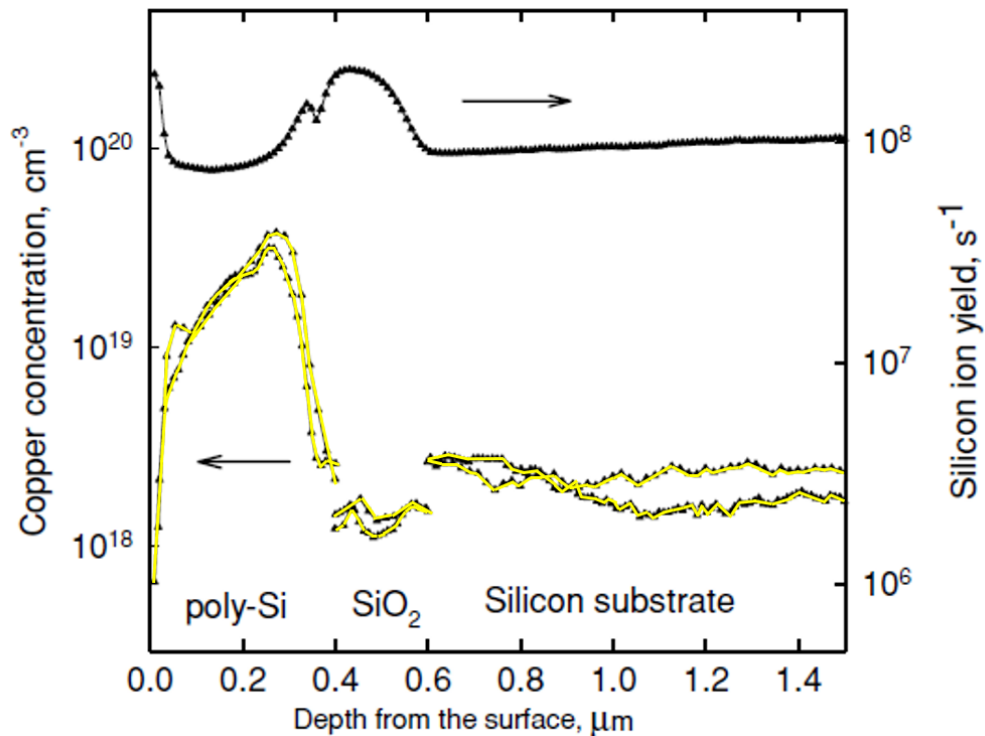
Ex.1012-Istratov, 570, Fig.2 (annotated).

313. Figure 2 shows iron impurities in the polysilicon layer following annealing. Specifically, Figure 2 teaches a higher iron concentration in the polysilicon layer than in the silicon substrate. Ex.1012-Istratov, Fig.2, 570 (in figure 2, “the solubility of iron in poly-silicon ... is more than an order of magnitude higher than in the silicon substrate,” which is “interpret[ed]” “as segregation gettering of iron by the poly-silicon).

314. After the copper contamination, the test structure was heated at either “at 690 °C for 5 h[ours]” or “at 1150 °C for 2 h[ours],” which also resulted in copper diffusion through the test structure. Ex.1012-Istratov, 571. The copper depth profiles after annealing were presented in Istratov’s Figures 4 and 5:



Ex.1012-Istratov, 571, Fig.4 (annotated).



Ex.1012-Istratov, 571, Fig.5 (annotated). Istratov concludes that “[t]he higher concentration of Cu in the poly-silicon layer can be interpreted as segregation of Cu at structural defects in the poly-silicon layer.” Ex.1012-Istratov, 571.

315. As I explained in Section XI.A.1.b, a person of ordinary skill in the art would have been motivated to alter the Choi-Marvin and Choi-Granek solar cells in view of Istratov and would have had a reasonable expectation of success in doing so. Specifically, this combination would have entailed using Istratov’s gettering technique to getter metal impurities from Choi’s substrate into the first conductive type area 32, which a person of ordinary skill in the art would have understood to have the same structure, arrangement, and function as—i.e., to correspond to—the

claimed “second emitter region” of the ’315 patent. Ex.1001-USP315, claim 16; XI.A.2.d. Choi’s solar cell has the same layers as the test structure of Istratov, and a person of ordinary skill in the art would therefore have recognized that the combination of Choi with Istratov would have resulted in the relocation of metal impurities such as iron and copper (to the extent these impurities were present in the substrate prior to gettering) to the first conductive type area 32 of Choi. Ex.1012-Istratov, 569-571, Figs.2, 4-5; Ex.1006-Choi, [0023], [0033], [0036]-[0037]. Istratov’s disclosure of moving iron or copper metal impurities from the substrate through the silicon dioxide layer and relocating them to the polysilicon layer would have been desirable in the similar solar cell structure of Choi to reduce recombination and improve solar cell efficiency.

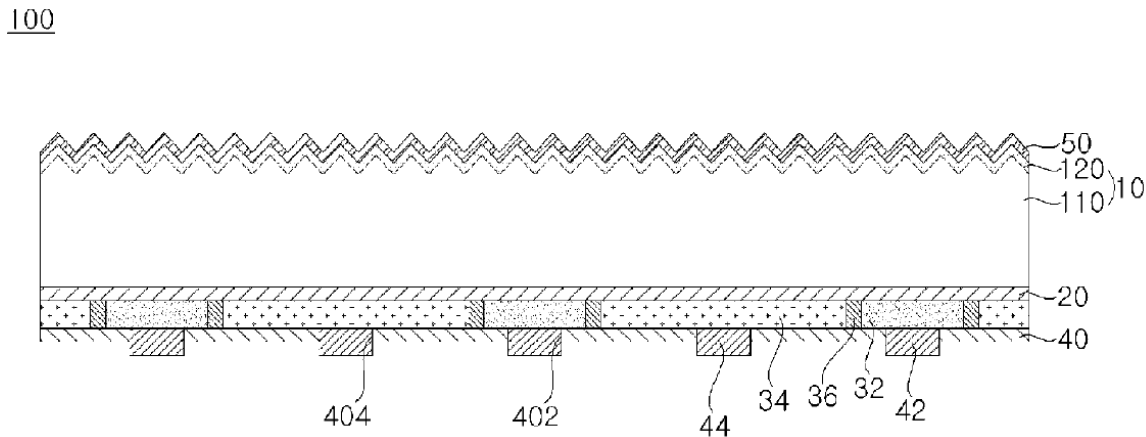
316. Accordingly, the combination of Choi, Granek or Marvin, and Istratov teaches *a second emitter region having metal impurities formed over the dielectric region.*

b. Element 16[b]: a second metal contact formed over the second emitter region.

317. As I explained in Sections XI.A.2.d and XI.A.8.a, a person of ordinary skill in the art would have understood Choi’s first conductive type area 32 is the *second emitter region*. A person of ordinary skill in the art would have understood that the first electrode 42 is *formed over the second emitter region*.

318. Choi teaches “first and second electrodes 42 and 44 which are connected to first and second conductive type areas 32 and 34, respectively,” as shown in Figure 1. Ex.1006-Choi, [0023], [0044], [0076], Fig.1.

FIG. 1

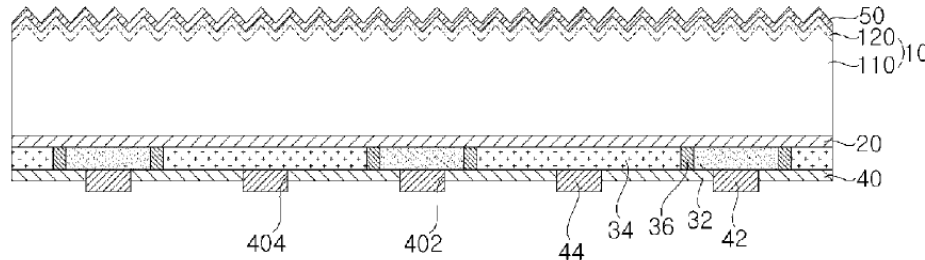


Ex.1006-Choi, Fig.1. Figure 1 shows that the first electrode 42 is “formed over” the first conductive type area 32. Ex.1006-Choi, Fig.1.

319. As I explained above in Section XI.A.2.e, after the first and second conductive type areas 32 and 34 are formed, “an insulating layer 40 is formed on the first and second conductive type areas 32 and 34,” and then “openings 402 and 404 exposing the first and second conductive type areas 32 and [34] are formed.”

Ex.1006-Choi, [0070], [0072], [0076]. Next, “as shown in [Figure] 3K, first and second electrodes 42 and 44 electrically connected to the first and second conductive type areas 32 and 34, respectively, are formed.” Ex.1006-Choi, [0076].

FIG. 3k



Ex.1006-Choi, Fig.3K. Thus, the first electrode 42 is “formed over” the first conductive type area 32, and the second electrode 44 is “formed over” the second conductive type area 34.

320. Choi further teaches that the first and second electrodes 42, 44 can include a variety of metal materials, and can be formed by a variety of methods, including coating or deposition. Ex.1006-Choi, [0044], [0076]. A person of ordinary skill in the art would have understood that Choi’s first and second electrodes 42, 44 are *metal contacts*. Further, a person of ordinary skill in the art would have understood that Choi’s first electrode 42 is *a second metal contact formed over the second emitter region*.

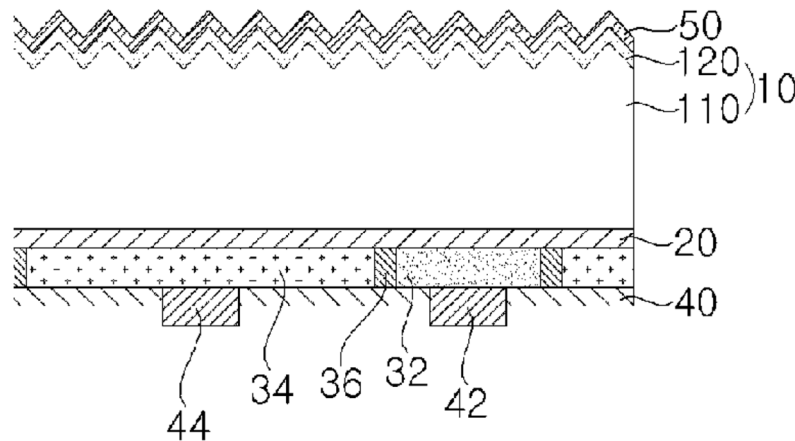
9. **Claim 17: The solar cell of claim 16, wherein the second emitter region is separate from the first emitter region.**

321. Claim 17 depends from claim 16. Therefore, I incorporate by reference my discussion of claim 16 in Section XI.A.8. The combination of Choi, Granek or

Marvin, and Istratov further teaches *the second emitter region is separate from the first emitter region*.

322. As I explained in Sections XI.A.2.d and XI.A.8.a, Choi teaches first and second conductive type areas 32 and 34 that correspond to the '315 patent's second and first emitter regions, respectively.

323. Choi further teaches that the first conductive area 32 is separate from the second conductive area 34. Specifically, Choi teaches a “barrier 36” that is disposed between and separates the first and second conductive type areas. Ex.1006-Choi, [0038] (“[T]he barrier area 36 is disposed between the first conductive type area 32 and the second conductive type area 34 and separates the first conductive type area 32 from the second conductive type area 34.”), [0052] (“[T]he barrier area 36 is interposed between the first conductive type area 32 and the second conductive type area 34 and functions to separate the first conductive type area 32 from the second conductive type area 34.”). Figure 1 shows conductive type areas 32 and 34 and barrier 36:



Ex.1006-Choi, Fig.1 (excerpted).

324. Choi further teaches that a shunt is generated when the first conductive type area contacts the second type area, which deteriorates performance of the solar cell. Ex.1006-Choi, [0038] (“When the first conductive type area 32 contacts the second conductive type area 34, shunt is generated and performance of the solar cell 100 is deteriorated.”). Choi explains that the barrier 36 is interposed between the first and second conductive type areas to prevent an unnecessary shunt. Ex.1006-Choi, [0038].

325. Accordingly, Choi teaches *the second emitter region is separate from the first emitter region.*

10. Claim 19: The solar cell of claim 16, wherein the second emitter region comprises polysilicon.

326. Claim 19 depends from claim 16. Therefore, I incorporate by reference my discussion of claim 16 in Section XI.A.8. The combination of Choi, Granek or Marvin, and Istratov further teaches *the second emitter region comprises polysilicon*.

327. As I explained in Sections XI.A.2.d and XI.A.7, Choi teaches that the first and second conductive type areas 32 and 34 can comprise polysilicon. Specifically, Choi teaches that the first and second conductive type areas can be formed by doping polycrystalline silicon with a first and second dopant type, respectively. Ex.1006-Choi, [0036] (“For example, the first conductive type area 32 may be easily formed by doping amorphous silicon, microcrystalline silicon, polycrystalline silicon or the like with a first conductive type dopant.”), [0037] (“For example, the second conductive type area 34 may be easily formed by doping amorphous silicon, microcrystalline silicon, polycrystalline silicon or the like with a second conductive type dopant.”).

328. Choi further teaches the “barrier 36” disposed between the first and second conductive type areas. Ex.1006-Choi, [0038] (“In addition, the barrier area 36 is disposed between the first conductive type area 32 and the second conductive type area 34 and separates the first conductive type area 32 from the second conductive type area 34.”). Choi explains that the first and second conductive type

areas and the barrier can include an identical semiconductor material, such as polycrystalline silicon. Ex.1006-Choi, [0039] (“In this case, the first and second conductive type areas 32 and 34, and the barrier area 36 are flush with one another and may include an identical semiconductor material (for example, amorphous silicon, microcrystalline silicon or polycrystalline silicon).”).

329. As I explained in Section VII.A, a person of ordinary skill in the art would have understood that “polycrystalline silicon” means polysilicon. Ex.1072-Komp, 37-38; Ex.1023-Nelson, 179.

330. Accordingly, Choi teaches *the second emitter region comprises polysilicon*.

11. **Claim 20: The solar cell of claim 16, wherein the first emitter region comprises a P-type doped polysilicon region and the second emitter region comprises a N-type doped polysilicon region.**

331. Claim 20 depends from claim 16. Therefore, I incorporate by reference my discussion of claim 16 in Section XI.A.8. The combination of Choi, Granek or Marvin, and Istratov further teaches *the first emitter region comprises a P-type doped polysilicon region and the second emitter region comprises a N-type doped polysilicon region*.

332. As I explained in Section XI.A.2.d and XI.A.8.a, Choi teaches first and second conductive type areas 32 and 34 that correspond to the '315 patent's second

and first emitter regions, respectively. Further, as I explained in Section XI.A.2.d, Choi teaches that the first and second conductive type areas can comprise polysilicon. Accordingly, Choi *teaches the first emitter region comprises a ... polysilicon region and the second emitter region comprises a ... polysilicon region.*

333. Choi further teaches that the second conductive area 34 (corresponding to the claimed first emitter region) can be P-type doped and that the first conductive type area 32 (corresponding to the claimed second emitter region) can be N-type doped. In the embodiment disclosed in Choi's Figure 1, Choi teaches that the substrate and the "first conductive type area 32" are n-type, and the "second conductive type area 34" is p-type. Ex.1006-Choi, [0026]. Though not required by the claim, Choi alternatively teaches that the substrate and the "first conductive type area 32" may be p-type and that the "second conductive type area 34" may be n-type. Ex.1006-Choi, [0026].

334. Accordingly, Choi teaches *the first emitter region comprises a P-type doped polysilicon region and the second emitter region comprises a N-type doped polysilicon region.*

B. GROUND II: Claim 18 Is Invalid as Obvious Over Choi, Granek or Marvin, Istratov, and Smith.

335. As detailed below, the combination of Choi, Granek or Marvin, Istratov, and Smith renders claim 18 obvious.

1. **Analogous Art, Motivation to Combine, and Reasonable Expectation of Success**

336. I was informed and I understand that one of the requirements for obviousness is that the references must be analogous art to the claims being challenged. *See* above §III.C. I have been informed and understand that a person of ordinary skill in the art must have had a reason or motivation to combine or modify the relevant teachings in the prior art to obtain the claimed invention, and one of ordinary skill in the art must have had a reasonable expectation of success in doing so. *See* above §III.C. It is my opinion that a person of ordinary skill in the art would have been motivated to combine Choi, Granek or Marvin, Istratov, and Smith with a reasonable expectation of success.

337. As I explained in Sections XI.A.1, XI.A.2, and XI.A.8, a skilled artisan would have found it obvious to combine Choi, Granek or Marvin, and Istratov. It would have been obvious to combine those references with Smith, which teaches “[a] trench structure separate[ing] the P-type doped region from the N-type doped region.” Ex.1011-Smith, [0007].

338. Smith teaches a back-contact solar cell with oppositely doped polysilicon regions separated by a trench for reducing recombination. Ex.1011-Smith, [0007] (“[A] solar cell includes polysilicon P-type and N-type doped regions on a backside of a substrate, such as a silicon wafer. A trench structure separates the

P-type doped region from the N-type doped region ... Among other advantages, the resulting structure increases efficiency by providing isolation between adjacent P-type and N-type doped regions, thereby preventing recombination in a space charge region where the doped regions would have touched.”), [0019] (“As shown in Fig.1, the doped regions 101 and 102 are separated by a trench 104, which serves as a gap between the doped regions 101 and 102.”), Fig.2. It would have been obvious to a person of ordinary skill in the art to add the trench described in Smith to separate the oppositely doped regions in the Choi-Granek-Istratov solar cell or the Choi-Marvin-Istratov solar cell to reduce recombination.

339. **First**, like Choi, Granek, Marvin, and Istratov (*see* above Section XI.A.1.b.i), Smith is analogous art to the Challenged Claims. Choi, Granek, Marvin, and Istratov are in the same field as the Challenged Claims—silicon semiconductor devices including solar cell devices—and are reasonably pertinent to solving the problems purportedly addressed in the Challenged Claims—improving device efficiency by reducing recombination. Ex.1006-Choi, [0003], [0006], [0029], [0035]-[0036], Figs.1, 3k; Ex.1010-Granek, 15-24, 26, 120; Ex.1008-Marvin, 5, 15; Ex.1012-Istratov, 569-570; *see* above Section VIII.A. Smith also addresses improving silicon-based solar cell efficiency. Ex.1011-Smith, [0007] (“Among other advantages, the resulting structure increases efficiency by providing isolation

between adjacent P-type and N-type doped regions, thereby preventing recombination in a space charge region where the doped regions would have touched.”), [0015] (“In solar cells with P-type and N-type doped regions in the substrate, the P-type and N-type doped regions may be formed with separate or abutting perimeters. The inventor discovered, however, that this is not true with polysilicon doped regions because recombination in the space charge region where the polysilicon doped regions touch is very high due to the lifetime of charge carriers in the polysilicon being very low. That is, the inventor discovered that touching polysilicon doped regions adversely affect efficiency.”), [0025] (“The trench structure of Fig.1 addresses the aforementioned issues relating to polysilicon parasitic space charge recombination several ways. Firstly, the trench 104 separates the doped regions 101 and 102 so they are not physically in contact. This prevents the space charge region from existing in either polysilicon film. Secondly, the resulting accumulation layer under the trench 104 repels minority carriers to improve surface passivation.”). Further, like the Challenged Claims, Smith describes a back-contact solar cell. Ex.1011-Smith, [0016] (“In the example of Fig.1, the solar cell is a backside contact solar cell in that its doped regions 101 and 102 are on the backside 106 opposite to the front side 105.”).

340. ***Second***, it is my opinion that a skilled artisan would have had ample motivation to use the trench disclosed in Smith to separate the n-type and p-type conductive type areas of the Choi-Granek-Istratov solar cell or the Choi-Marvin-Istratov solar cell—which, as I explained above (Sections XI.A.2.d, XI.A.8), correspond to the first and second emitter regions recited in the claims of the '315 patent.

341. As I explained in Section XI.A.1, the solar cells created by the combination of Choi with Granek or Marvin are “back-contact” solar cells. The back contacts in those solar cells have positive and negative electrodes. Ex.1006-Choi, [0026] (“Electrons created by photoelectric effect are collected by a first electrode **42** when light is emitted to the tunnel junction, and holes are moved toward the front surface of the semiconductor substrate **10** and are then collected by a second electrode **44**.”). Smith also teaches a back-contact solar cell with interdigitated metal contact fingers connecting to n-type and p-type regions in the substrate. Ex.1011-Smith, [0007] (“[A] solar cell includes polysilicon P-type and N-type doped regions on a backside of a substrate, such as a silicon wafer.”), [0026] (“Referring to Fig.2, interdigitated metal contact fingers 108 and 109 may be formed through the silicon nitride 107 to make an electrical connection to the doped regions 101 and 102, respectively.”).

342. For such back-contact designs with doped polysilicon regions, having n-type and p-type regions that are adjacent to each other can decrease efficiency because “recombination in the space charge region where the polysilicon doped regions touch is very high due to the lifetime of charge carriers in the polysilicon being very low.” Ex.1011-Smith, [0015]. By the earliest possible priority date of the '315 patent, it was well known that back-contact solar cells were prone to shunting caused by contact between opposite polarity doped regions or metal contacts. Ex.1044-Verlinden-1994, 143 (“[T]he closely interdigitated back-side metal [of back-contact solar cells] [] could be prone to shorts.”).

343. Smith presents a solution to this problem with recombination in the form of a trench. Specifically, in Smith, the doped regions are separated by trench 104, shown in Figure 2:

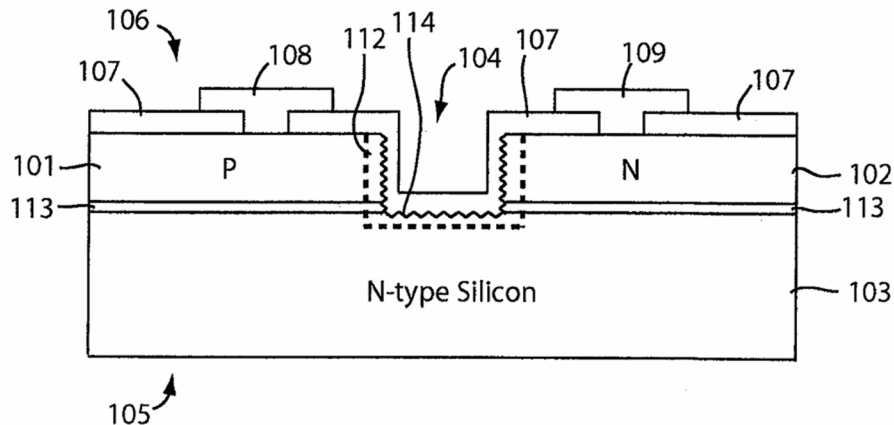


FIG. 2

Ex.1011-Smith, Fig.2. Smith explains that, in this design, “doped regions 101 and 102 are separated by a trench 104, which serves as a gap between the doped regions 101 and 102.” Ex.1011-Smith, [0019], Fig.2.

344. Smith teaches three features of the trench that will increase solar cell efficiency. First, Smith’s trench 104 “prevents the space charge region from existing in either polysilicon film.” Ex.1011-Smith, [0025]. Second, Smith teaches that “the resulting accumulation layer under the trench 104 repels minority carriers to improve surface passivation.” Ex.1011-Smith, [0025]. A person of ordinary skill in the art would have recognized that the ability to repel minority carries by the accumulation layer would provide an additional improvement to the solar cell efficiency compared to the barrier area taught by Choi. Third, “the textured surface 114 in the trench 104 increases solar radiation collection.” Ex.1011-Smith, [0025]. Again, a person of ordinary skill in the art would have recognized that the additional solar radiation that

the solar cell is able to collect when a trench is used—as taught by Smith—would provide an additional improvement to solar cell efficiency compared to using the barrier area taught by Choi. Finally, the trench structure taught by Smith is compatible with the solar cell taught by Choi. Specifically, Smith teaches depositing silicon nitride 107 over the trench to “provide good surface passivation.” Ex.1011-Smith, [0022]. This silicon nitride film used in the trench structure of Smith is equivalent to the insulating layer 40 taught by Choi. The insulating layer 40 of Choi is “formed on the first and second conductive type areas 32 and 34 and the barrier area 34” and can be composed of a variety of insulating materials, including silicon nitride. Ex.1006-Choi, [0042]-[0043]. As such, a person of ordinary skill in the art would have recognized that the formation of the trench structure taught by Smith in the solar cell taught by Choi would not require an extra step of forming the silicon nitride layer over the trench because this silicon nitride can be formed at the same time as the insulating layer covering the first and second conductive type areas (as taught by Choi).

345. In view of these efficiency gains and compatibility, a person of ordinary skill in the art would have had ample motivation to use such a trench to separate the n-type and p-type emitter regions in the Choi solar cell, with the further modifications of Granek or Marvin, combined with Istratov.

346. It is also my opinion that a person of ordinary skill in the art would have been motivated to combine the Choi-Granek-Istratov solar cell or the Choi-Marvin-Istratov solar cell with Smith because the combinations would have merely involved the use of known techniques (using a trench) to a known device (back-contact solar cell) in the same way (silicon semiconductor fabrication processes). Smith makes clear that its trench is equally applicable to a back-contact solar cell such as Choi's. And creating this design would have been well within the capabilities of a person of ordinary skill in the art, as it would have required merely the use of conventional fabrication techniques for semiconductor devices, as disclosed in Smith, of creating the trench either before or after creation of the doped regions. *See* Ex.1011-Smith, [0017], [0019], [0025] [0029]-[0035]. There would be no serious doubts about the success of implementing this design, given the teachings of the respective references and the conventional nature of the design features and required fabrication techniques.

347. ***Third***, it is my opinion that a person of ordinary skill in the art would have been able to readily modify the Choi-Granek-Istratov or the Choi-Marvin-Istratov solar cells with the trench of Smith using standard semiconductor fabrication techniques. Methods for fabricating back-contact solar cells with trenches between oppositely doped regions were well known before the earliest possible priority date.

348. Smith teaches two processes for forming the trench separating the doped regions either before or after formation of the doped regions. *See* Ex.1011-Smith, [0017], [0019], [0025], [0029]. In the first process, Smith teaches diffusing dopants from the silicon dioxide layers to the polysilicon layer with a thermal drive-in step, Ex.1011-Smith, [0030], and etching the silicon dioxide layers, doped regions, and dielectric layer to form a trench. Ex.1011-Smith, [0032]. Alternatively, in a second process, Smith teaches etching the silicon dioxide layers and dielectric layer to form a trench. Ex.1011-Smith, [0034]. Thereafter, a thermal drive-in step is performed to diffuse dopants from the silicon dioxide layers to the polysilicon layer. Ex.1011-Smith, [0035]. Similar to the first process of Smith, Choi teaches a process to etch “silicate or an insulating film” after diffusing dopants into first and second doping layers, 322 and 342. Ex.1006-Choi, [0070]-[0071]. A person of ordinary skill in the art would have understood the “silicate or an insulating film” to include silicon dioxide. Smith merely adds the step of etching a trench in addition to removing the “silicate or [] insulating film.” Ex.1006-Choi, [0071]. Therefore, a person of ordinary skill in the art would have known how to implement these standard techniques for forming the trench taught by Smith in the Choi-Granek-Istratov or the Choi-Marvin-Istratov solar cell.

349. Moreover, it is my opinion that a person of ordinary skill in the art would have had a reasonable expectation of success in implementing Smith's trench due to similarities between the references. Like Smith, the Choi-Granek-Istratov and Choi-Marvin-Istratov solar cells relate to back-contact solar cells, and Smith specifically teaches benefits of adding a trench to solar cells, like Choi's, with polysilicon doped regions. Therefore, a person of ordinary skill in the art would have been motivated to combine their teachings with a reasonable expectation of success.

2. **Claim 18: The solar cell of claim 16, wherein a trench region separates the first emitter region from the second emitter region.**

350. Claim 18 depends from claim 16. Therefore, I incorporate by reference my discussion of claim 16 in Section XI.A.8.

351. The combination of Choi, Granek or Marvin, Istratov, and Smith further teaches *a trench region separates the first emitter region from the second emitter region*.

352. Smith teaches a back-contact structure for a solar cell. Ex.1011-Smith, [0016]-[0022]. Smith teaches doped regions 101 and 102 formed over the back side of a silicon substrate. Ex.1011-Smith, [0016]. Smith further teaches that, in the embodiment of Figures 1 and 2, the substrate and doped region 102 are n-type doped,

and doped region 101 is p-type doped. Ex.1011-Smith, [0017]. Figure 2 is shown below.

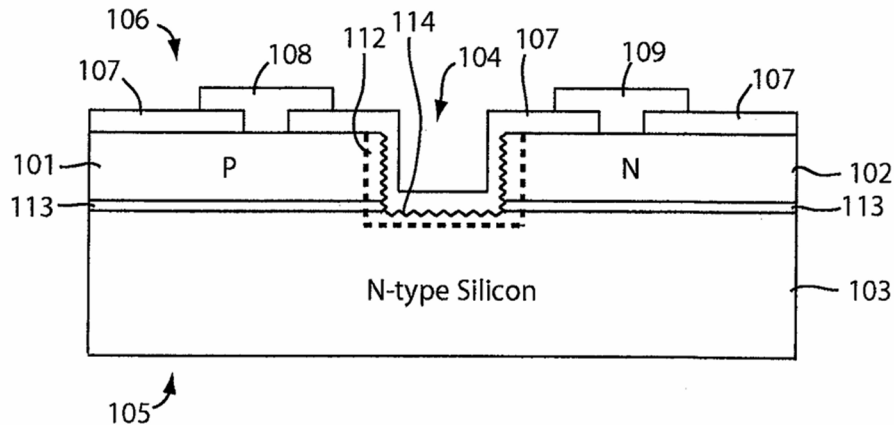


FIG. 2

Ex.1011-Smith, Fig.2.

353. A person of ordinary skill in the art would have recognized that Smith's doped regions 101 and 102 are "emitters" as that term is used in the '315 patent. Specifically, a person of ordinary skill in the art would have understood that the '315 patent's "first emitter region" corresponds to Smith's "doped region 101" because it is oppositely doped from the substrate. Likewise, a person of ordinary skill in the art would have understood that the '315 patent's "second emitter region" corresponds to Smith's "doped region 102" because it has the same type doping as the substrate. Ex.1001-USP315, 3:36-41 ("the silicon substrate can be a N-type silicon substrate"), 6:50-62 ("the first and second emitter regions 312, 314 can be P-type and N-type doped polysilicon regions, respectively").

354. Smith also teaches a trench 104 that separates the doped regions 101 and 102, “which serves as a gap between the doped regions 101 and 102,” as shown in Figure 1 of Smith. Ex.1011-Smith, [0019], [0029] (“The trench separating the doped regions may be formed before formation of the doped regions in a first trench formation process or after formation of the doped regions in a second trench formation process.”), [0036] (“In both the first and second trench formation processes, the trench 304 serves as a gap physically separating the P-type doped region 301 from the N-type doped region 302.”), [0041] (“The polysilicon layer where the doped regions are formed may be etched to form a trench separating the P-type doped region from the N-type doped region (step 602).”).

355. Accordingly, Smith teaches *a trench region separates the first emitter region from the second emitter region*.

C. GROUND III: Claims 10-15 Are Invalid as Obvious Over Cousins, Granek or Marvin, and Istratov.

356. As detailed below, the combination of Cousins, Granek or Marvin, and Istratov renders claims 10-15 obvious.

1. Analogous Art, Motivation to Combine and Reasonable Expectation of Success

357. I was informed and I understand that one of the requirements for obviousness is that the references must be analogous to the claims being challenged.

See above §III.C. I was informed and understand that a person of ordinary skill in the art must have been motivated to combine the references with a reasonable expectation of success. *See* above §III.C. It is my opinion that each requirement is met here.

358. As I explained in Sections XI.A.1, XI.A.2, and XI.A.8, it would have been obvious to combine the techniques of Choi, Granek, Marvin, and Istratov together to reduce recombination to improve efficiency of solar cells. For similar reasons, it also would have been obvious to combine the techniques of Cousins, Granek, Marvin, and Istratov together to reduce recombination to improve efficiency of solar cells. The references are analogous, are directed to the same kinds of problems, and would have been combined with a reasonable expectation of success.

a. Cousins with Granek or Marvin

i. Analogous Art

359. ***First***, it is my opinion that Cousins, Granek, and Marvin are in the same field as the Challenged Claims of the '315 patent—namely, solar cell devices—and are also relevant to the problem of improving the efficiency of such solar cells by reducing the recombination of electrons and holes. Ex.1007-Cousins, 1:15-18, 2:22-23, 2:49-58; Ex.1010-Granek, Abstract; Ex.1008-Marvin, 5, 15; *see* Section VIII.A.

360. Cousins—like the '315 patent, as well as Granek and Marvin—discloses a substrate with a doped front portion, “N-type doped region 105.” Ex.1007-Cousins, 2:49-54 (disclosing an “N-type doped region 105 [that] provides low front surface recombination and improves lateral conductivity”); *see above* §§X.C-X.D. The both-sides-contacted solar cell of Cousins has an n-type substrate. Ex.1007-Cousins, 2:39-55 (“[T]he solar cell 100 includes ... the N-type silicon substrate 101 servings [sic] as an N-type diffusion region.”), 2:48-53 (“The front side surface of the substrate 101 ... includes an N-type doped region 105 formed in the substrate ... The N-type doped region 105 provides low front surface recombination and improves lateral conductivity”), Fig.1. Thus, Cousins, Granek, and Marvin each disclose a solar cell having a doped front region for reducing recombination.

361. Similar to Choi, Cousins also discloses “diffus[ing] N-type dopants into the front side of the substrate 101 to form the N-type doped region 105.” Ex.1007-Cousins, 5:48-53; Ex.1006-Choi, [0074].

ii. Motivation to Combine

362. ***Second***, a person of ordinary skill in the art would have had ample motivation to use the dopant concentrations disclosed in Granek and Marvin in Cousins’ front “N-type doped region 105.” While Cousins provides a range “of 100

to 500 Ω/sq ” for the sheet resistance of the N-type doped region 105, it leaves the selection of other parameters (*e.g.*, dopant concentration) to a person of ordinary skill in the art’s skill and discretion. Ex.1007-Cousins, 2:49-55 (“The N-type doped region 105 may have a sheet resistance of 100 to 500 Ω/sq .”). The lack of a precise dopant concentration in the Cousins reference indicates that Cousins thought that a person of ordinary skill in the art would be able to select a dopant concentration from a selection of appropriate values and would have consulted references such as Granek or Marvin in selecting the dopant concentration.

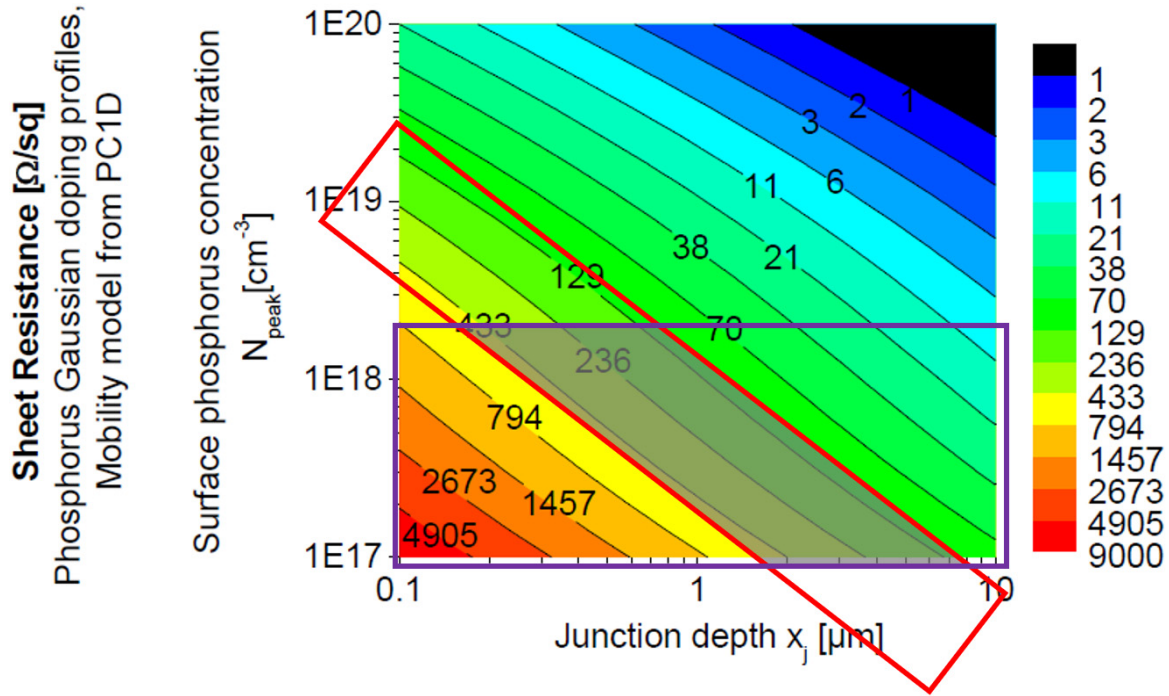
363. Similar to my discussion of the combinations of Choi with Granek or Marvin in Section XI.A.1.a.ii, it is my opinion that, for Cousins, a skilled artisan would have been motivated to turn to a reference such as Granek or Marvin to identify a concentration that would minimize recombination (as detailed in Granek and Marvin). Granek and Marvin both describe techniques for reducing recombination. Ex.1010-Granek, 117-136; Ex.1008-Marvin, 3-5.

364. Both Granek and Marvin teach the use of front surface fields in back-contact solar cells for similar purposes. Granek discloses that a dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ is desirable, and Marvin discloses that dopant concentrations of $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$ are suitable. Ex.1010-Granek, 121-122 (Figs.7-1, 7-3); Ex.1008-Marvin, 15. Both Granek and Marvin explain that the front

surface field dopant concentration level must be high enough to achieve a reduction in surface recombination, while low enough to avoid the increased recombination rates associated with higher doping levels (*i.e.*, Auger recombination). Ex.1010-Granek, 117-136; Ex.1008-Marvin, 3-5, Fig.1.

365. Furthermore, in light of Cousins' teaching that "[t]he N-type doped region 105 may have a sheet resistance of 100 to 500 Ω/sq ," a person of ordinary skill in the art would have recognized from Figure 7-4 of Granek that, for practical FSF depths, the sheet resistance of 100 to 500 Ω/sq is compatible with Granek's teaching of a FSF dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$. Ex.1007-Cousins, 2:49-55; Ex.1010-Granek, 123 (Fig.7-4). For example, Granek explored FSFs with FSF depths ranging from 0.38 μm to 1.44 μm . Ex.1010-Granek, 126. As a person of ordinary skill in the art would have understood, as the depth (*i.e.*, thickness) of the FSF decreases, it becomes more impractical to form. As shown in Figure 7-4 of Granek, across all the FSF depths considered by Granek, a FSF with a dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ would have resulted in a sheet resistance of 100 to 500 Ω/sq . Moreover, a person of ordinary skill in the art would have recognized from Figure 7-4 of Granek that, for practical FSF depths, more likely than not, Cousins used a dopant concentration of around $1 \times 10^{18} \text{ cm}^{-3}$. Figure

7-4 of Granek shows sheet resistance as a function of N_{peak} and junction depth (assuming a Gaussian diffusion):



Ex.1010-Granek, 123 (Fig.7-4) (annotated). The red box in the annotated figure above shows the dopant concentration and FSF depth combinations that would result in a sheet resistance of 100 to 500 Ω/sq taught by Cousins. The purple box in the annotated figure above shows the portion of the graph corresponding to a dopant concentration of less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$. Given the substantial overlap between the red box and the purple box (as shown by the shaded region in the annotated figure above), in particular for practical FSF depths, it would have been obvious for a person of ordinary skill in the art, in view of the teachings of Granek,

to try—with a reasonable expectation of success—FSF dopant concentration values of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$. In particular, it would have been obvious for a person of ordinary skill in the art to use Granek’s teaching of a FSF dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ or Marvin’s teaching of a FSF dopant concentration of $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$ in Cousins’ N-type doped region to achieve a sheet resistance of 100 to 500 Ω/sq .

iii. Reasonable Expectation of Success

366. *Third*, it is my opinion that a person of ordinary skill in the art would have had a reasonable expectation of success in using the Granek and Marvin surface dopant concentrations for Cousins’ front “N-type doped region 105.” Such an implementation would merely have involved known diffusion methods to achieve an identified dopant concentration—a task well within the capabilities of a skilled artisan. Specifically, it would have been straightforward to apply the dopant concentration from Granek or Marvin to the front doped region of Cousins.

367. Cousins explains that the front “N-type doped region 105” may be created through diffusion of “N-type dopants into the front side of the substrate 101” using conventional techniques (*e.g.*, exposing the region “to phosphorus in [a] diffusion furnace”). Ex.1007-Cousins, 5:49-6:13. For a skilled artisan, such diffusion methods would have been familiar and uncomplicated, and it would have

taken only ordinary skill to use those methods to apply a specific FSF dopant concentration (such as the concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ and 1×10^{17} to $1 \times 10^{18} \text{ cm}^{-3}$ specified in Granek or Marvin, respectively) to the front “N-type doped region 105” of Cousins.

b. Cousins with Granek or Marvin and Istratov

i. Analogous Art

368. *First*, as explained in Section XI.A.1.b.i, Istratov relates to silicon-based semiconductor devices—a field that encompasses solar cell devices—and skilled artisans in solar cells frequently learned from and adopted microelectronics technologies. Ex.1012-Istratov, 570 (Istratov teaches “a poly-Si/SiO₂ structure.”); Ex.1075-Green-1995, 218 (“To achieve design objectives in [surface passivation,] full advantage had to be taken of developments in microelectronics”). Cousins, Granek, and Marvin are directed to solar cell devices specifically. *See* above Sections X.B-X.D. It is my opinion that Cousins, Granek, Marvin, and Istratov are in the same field as the Challenged Claims—namely, silicon semiconductor devices including solar cell devices.

369. Additionally, Cousins, Granek, Marvin, and Istratov are all relevant to the problem of improving the efficiency of such solar cells by reducing the recombination of electrons and holes (matching the issue to which the claimed

inventions are purportedly directed). Ex.1007-Cousins, 1:15-18, 2:22-23, 2:49-58; *see above* §§VIII.A and XI.A.1.a. Specifically, Cousins, Granek, and Marvin each disclose improvements to the efficiency of silicon-based solar cells. In a complementary way, Istratov—which is directed to a gettering process to reduce metal impurities in a semiconductor structure—presents a solution directly applicable to solar cells. Ex.1012-Istratov, 569-70.

ii. Motivation to Combine

370. ***Second***, combining Cousins and Granek (“Cousins-Granek”) or Cousins and Marvin (“Cousins-Marvin”) with Istratov would have involved nothing more than applying known techniques (gettering of metal impurities) to a known device (a both-sides-contacted solar cell with a doped front portion) in the same way (using the same semiconductor manufacturing techniques). The solar cell structure of Cousins has a front surface facing the sun, a substrate including an N⁺ doped region, a polysilicon emitter layer, and front and back contacts. Ex.1007-Cousins, 2:31-38, 3:12-13, Fig.1. The front area of Cousins’ solar cell structure is readily modifiable by using a doped portion having the particular dopant concentrations specified in Granek and Marvin. Ex.1010-Granek, 120-121; Ex.1008-Marvin, 15.

371. Moreover, the back area of Cousins’ solar cell structure is readily modifiable by Istratov, which teaches gettering of metal impurities through an oxide

layer to a polysilicon region, for the reasons I explained in Section XI.A.1. Ex.1012-Istratov, 570-571; *see above* §§X.D-X.E.

iii. Reasonable Expectation of Success

372. *Third*, and similar to the reasons I described in Section XI.A.1.b, it is my opinion that a person of ordinary skill in the art would have had a reasonable expectation of success in adding Istratov’s gettering process to the Cousins-Granek or Cousins-Marvin solar cell to trap impurities in the emitter. Specifically, these combinations would have yielded a straightforward solar cell design—a solar cell with a front doped portion with a dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ or $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$, respectively, along with an emitter region that has had metal impurities gettered into it. The combination of Cousins, Granek or Marvin, and Istratov represents a straightforward implementation of a dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ or $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$ in the doped front portion and gettering of metal impurities into the emitter region.

373. Istratov discloses a gettering process to relocate the impurities to a polysilicon layer, where they are less likely to cause recombination. Ex.1012-Istratov, 570-571; *see above* §§X.D-X.E. Cousins teaches a “polysilicon layer 108” that is “formed on a thin dielectric layer 107” and “has an emitter saturation current of about $10 \text{ fA} \cdot \text{cm}^{-2}$.” Ex.1007-Cousins, 2:42-44, 3:12-13. Thus, like Choi,

Cousins' solar cell structure includes a substrate and a polysilicon layer into which metal impurities from the substrate would be gettered using the process of Istratov. *See above §§XI.A.1.*

374. Therefore, a person of ordinary skill in the art would have been motivated to apply Istratov's gettering technique to the Cousins-Granek solar cell or the Cousins-Marvin solar cell to further improve solar cell efficiency through the trapping of metal impurities in the emitter, as expressly taught by Istratov.

2. Claim 10

- a. Element 10[Pre]: A solar cell, the solar cell having a front side which faces the sun during normal operation and a back side opposite the front side, the solar cell comprising:**

375. Cousins teaches *a solar cell, the solar cell having a front side which faces the sun during normal operation and a back side opposite the front side.*

376. Cousins teaches a solar cell (100) having a "front side" that "faces the sun during normal operation to collect solar radiation" and a back side opposite to the front side, as shown in Figure 1 of Cousins. Ex.1007-Cousins, 2:31-38 ("The front side, which is opposite the backside, faces the sun during normal operation to collect solar radiation. The front side of the solar cell includes layers formed on the front side surface of a substrate 101, and the backside of the solar cell includes layers formed on the backside surface of the substrate 101."), Fig.1.

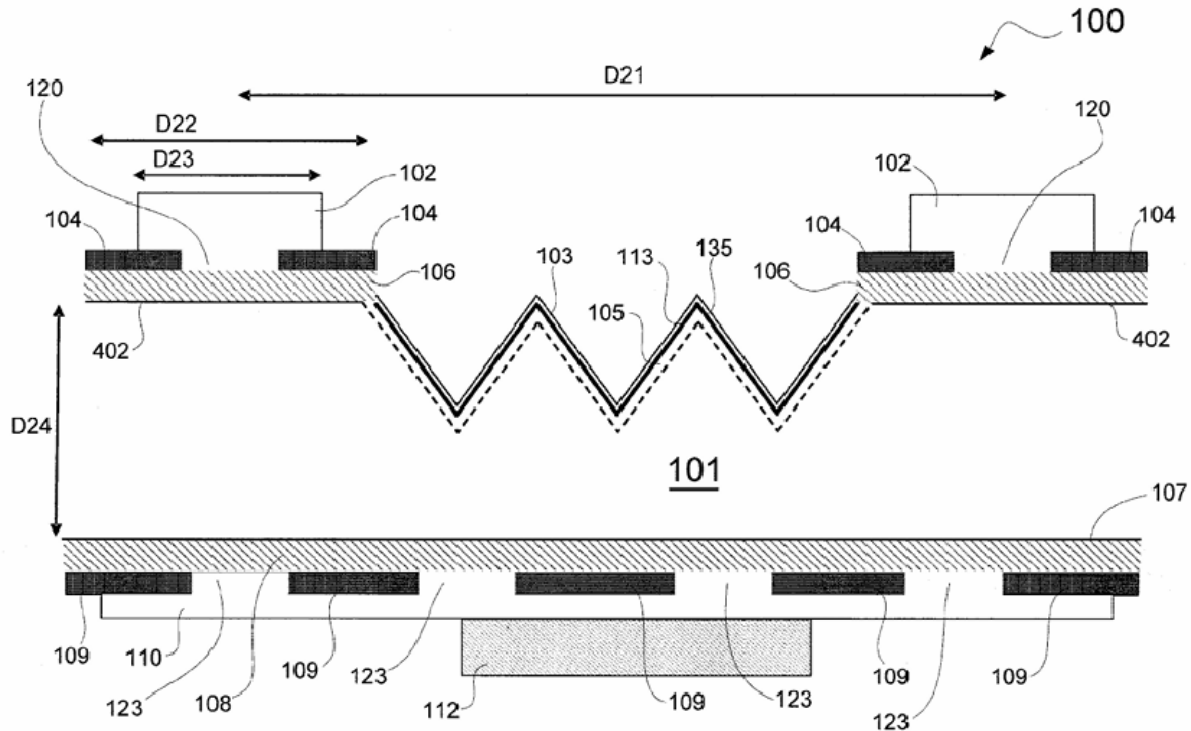


FIG. 1

Ex.1007-Cousins, Fig.1.

- b. Element 10[a]: a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ and wherein the portion of the substrate is formed at the front side of the solar cell;**

377. The combination of Cousins and Granek or Marvin teaches *a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal $2 \times 10^{18} \text{ cm}^{-3}$ and wherein the portion of the silicon substrate is formed at the front side of the solar cell.*

378. Cousins' solar cell 100 includes a substrate 101, as shown in Figure 1. Ex.1007-Cousins, 2:35-38, Figs.1, 12. "The front side of the solar cell includes layers formed on the front side surface of a substrate 101, and the backside of the solar cell includes layers formed on the backside surface of the substrate 101." Ex.1007-Cousins, 2:35-38, Figs.1, 12.

379. At the front side of the substrate, Cousins has a "doped region 105 formed in the substrate." Ex.1007-Cousins, 2:49-55, Figs.1, 12. A person of ordinary skill in the art would have understood that the doped region 105 is the *portion of the silicon substrate [] formed at the front side of the solar cell.*

380. Cousins teaches that the silicon substrate 101 and the doped region 105 are both n-type doped. Ex.1007-Cousins, 2:39-55 (referencing "N-type silicon substrate" and "N-type doped region 105 formed in the substrate"). A person of ordinary skill in the art would have understood that doped region 105 is doped with the same dopant type as substrate 101.

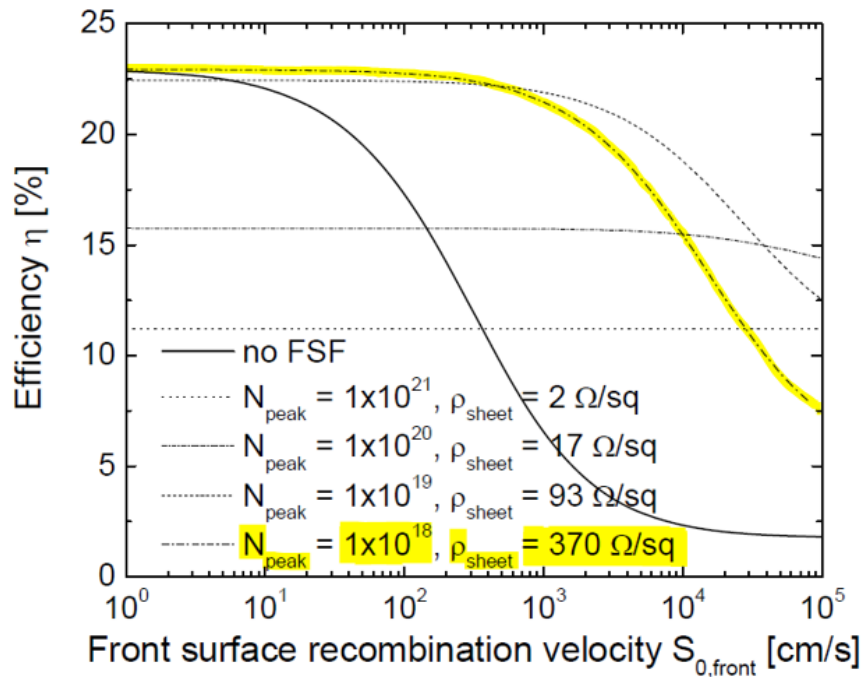
381. Cousins teaches the "doped region 105 provides low front surface recombination and improves lateral conductivity." Ex.1007-Cousins, 2:49-55. Cousins' doped region 105 is "formed in the substrate" and at the front side of the substrate. Ex.1007-Cousins, 2:49-51.

382. The doped region 105 is formed by diffusing “dopants into the front side of the substrate 101.” Ex.1007-Cousins, 5:48-53. Cousins teaches driving n-type dopants into the front side of an n-type silicon substrate 101 to form an n-type doped region 105. Ex.1007-Cousins, 2:44-55, 5:48-53. Cousins does not specify the specific dopant concentration of the doped region 105.

383. As I explained in Section VII.B.2.a, it was well known by 2014 that Auger recombination would be reduced by optimizing the front surface field dopant concentration of solar cells, and multiple publications and patents had disclosed that a FSF dopant concentration above $1 \times 10^{18} \text{ cm}^{-3}$ induced Auger recombination. Granek and Marvin specifically disclosed using a dopant concentration of *approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$* in the front surface field to reduce recombination.

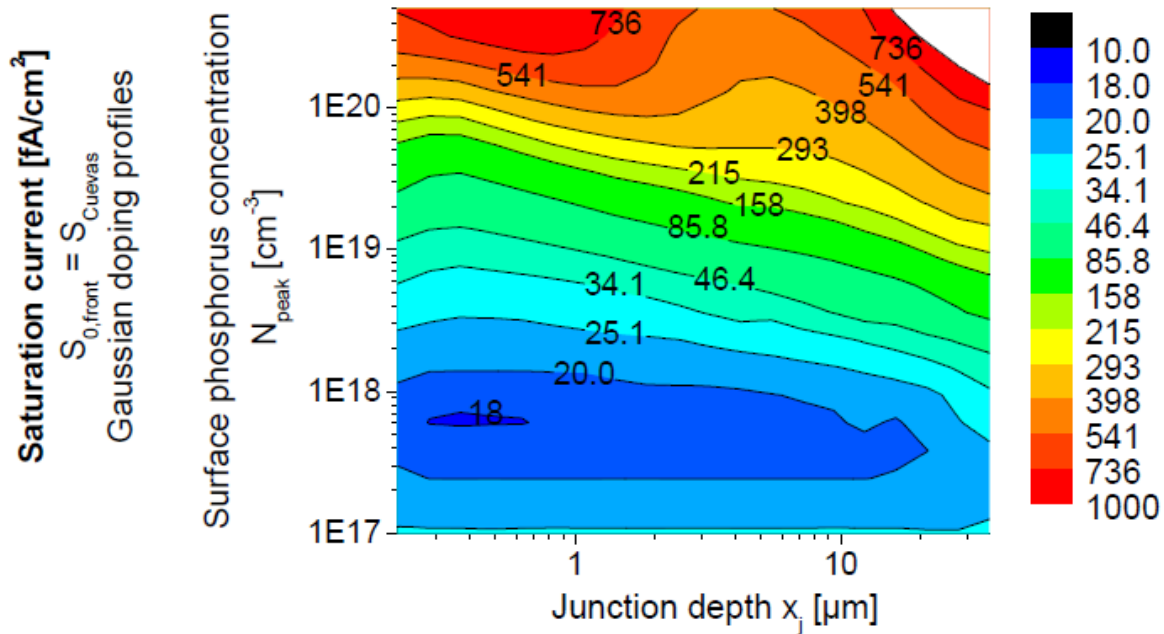
384. As I explained in Section X.C, Granek analyzed the performance of solar cells having different FSF dopant concentrations and teaches that “[a] lowly doped FSF results in high quantum efficiency” because “Auger recombination inside the highly doped region and the surface recombination velocity are low.” Ex.1010-Granek, 14, 117, 120. A person of ordinary skill in the art would have understood that the FSF of Granek is *a portion of the silicon substrate [] formed at the front side of the solar cell.*

385. As I explained in Section X.C, Granek simulates solar cells with dopant concentrations ranging from 1×10^{18} to $1 \times 10^{21} \text{ cm}^{-3}$ and shows that the solar cell having a FSF with a dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ had the highest efficiency. Ex.1010-Granek, 120-122. Figure 7-1 shows the simulated solar cell's efficiency is highest when the FSF dopant concentration is $1 \times 10^{18} \text{ cm}^{-3}$, in particular for solar cells that have low front surface recombination velocity:



Ex.1010-Granek, 121, Fig.7-1 (annotated). As I explained in Section X.C, well passivated solar cells, like the solar cell taught by Cousins, have low front surface recombination velocity, corresponding to the left side of the graph shown in Figure 7-1.

386. As I explained in Section X.C, Figure 7-3 of Granek shows the simulated solar cell's recombination level is lowest when the FSF dopant concentration is approximately $1 \times 10^{18} \text{ cm}^{-3}$.



Ex.1010-Granek, 122 Fig.7-3.

387. A person of ordinary skill in the art would have understood that the FSF dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ disclosed in Granek is a *portion of the silicon substrate [that] has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$.*

388. As I explained in Section XI.C.1, a person of ordinary skill in the art would have been motivated to alter Cousins' solar cell in view of Granek and would have had a reasonable expectation of success in doing so. This would have entailed

using Granek's FSF dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ in Cousins' doped region 105.

389. As I explained in Section X.D, Marvin states that front surface field structures have been known since as late as “the mid 1980s.” Ex.1008-Marvin, 3. To increase solar cell efficiency, Marvin studied various “critical design parameters” of back-contact solar cells such as doping profiles and concentrations in a front surface field. Ex.1008-Marvin, 5, 9, 16 (this study “assess[es] [] the effects of certain design parameters on cell performance,” and “front surface field doping” was a “design parameter[] [] selected for study”). A person of ordinary skill in the art would have understood that the front surface field discussed in Marvin is a *portion of the silicon substrate [] formed at the front side of the solar cell*.

390. As I explained in Section X.D, Marvin teaches that “[t]he FSF effectiveness is relatively constant over a rather broad range around $1\text{E}17$ to $1\text{E}18 \text{ cm}^{-3}$, decreasing below this level due to the weakness of the electric field and decreasing above this level due to increased Auger recombination.” Ex.1008-Marvin, 15. A person of ordinary skill in the art would have understood that the FSF with a peak dopant concentration of $1\text{E}17$ to $1\text{E}18 \text{ cm}^{-3}$ disclosed by Marvin is a *portion of the silicon substrate [that] has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$* .

391. As I explained in Section XI.C.1, a person of ordinary skill in the art would have been motivated to alter Cousins' solar cell in view of Marvin and would have had a reasonable expectation of success in doing so. This would have entailed using Marvin's dopant concentration of $1\text{E}17$ to $1\text{E}18\text{ cm}^{-3}$ in Cousins' doped region 105.

392. In sum, the combination of Cousins and Granek or Marvin teaches *a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal $2 \times 10^{18}\text{ cm}^{-3}$ wherein the portion of the silicon substrate is formed at the front side of the solar cell.*

c. Element 10[b]: a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of the solar cell;

393. Cousins teaches *a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of the solar cell.*

394. Cousins teaches a "thin dielectric layer 107" formed "on the backside surface of the substrate 101" that "may comprise silicon dioxide thermally grown to a thickness of about 10 to 50 Angstroms." Ex.1007-Cousins, 3:12-20, 4:36-41, Fig.1. Figure 1 of Cousins shows the thin **dielectric layer 107 (orange)** "formed over" the silicon substrate 101:

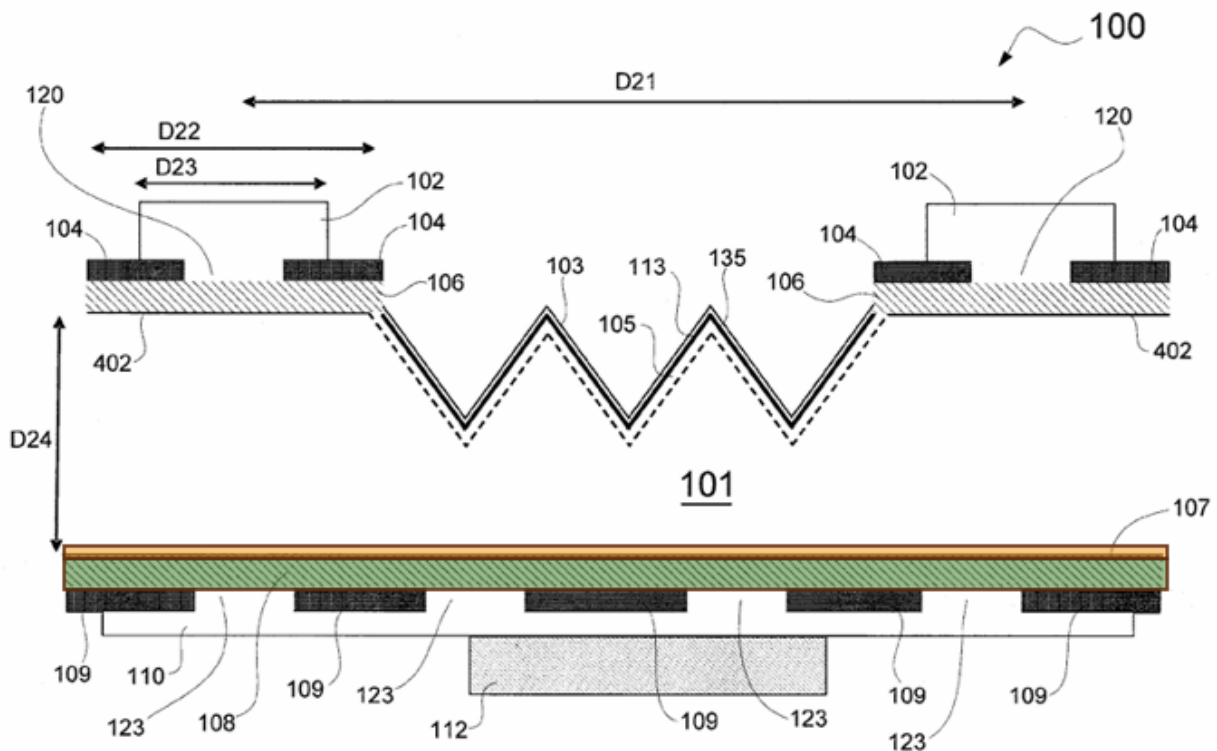


FIG. 1

Ex.1007-Cousins, Fig.1 (annotated).

395. Figures “4-19” of Cousins “schematically illustrate the fabrication of the solar cell 100.” Ex.1007-Cousins, 4:20-22. Figure 4 shows “an N-type silicon substrate 101 is prepared for processing into a solar cell.” Ex.1007-Cousins, 4:23-25.

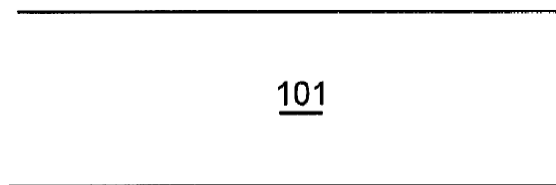
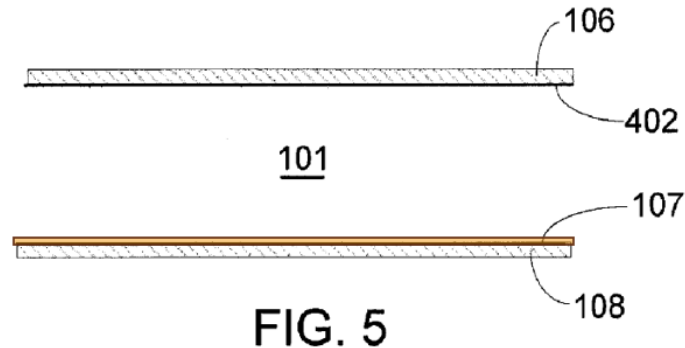


FIG. 4

Ex.1007-Cousins, Fig.4. Next, Figure 5 shows the thin **dielectric layer 107** (**orange**) is “formed on the ... back surface, ... of the substrate 101.” Ex.1007-Cousins, 4:36-46.



Ex.1007-Cousins, Fig.5 (annotated). “The thin dielectric layer[] ... 107 may comprise silicon dioxide thermally grown to a thickness of about 10 to 50 Angstroms on the surfaces of the N-type silicon substrate 101.” Ex.1007-Cousins, 4:36-46. Thus, a person of ordinary skill in the art would have understood that Cousins’ thin dielectric layer 107 is “formed over” the N-type silicon substrate 101.

396. A person of ordinary skill in the art would have understood that Cousins’ dielectric layer 107 is *a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of the solar cell.*

d. Element 10[c]: a first emitter region having metal impurities formed over the dielectric region; and

397. The combination of Cousins and Istratov teaches *a first emitter region having metal impurities formed over the dielectric region.*

398. Cousins teaches that “polysilicon layer 108 is formed on a thin dielectric layer 107.” Ex.1007-Cousins, 3:12-13, 4:41-46, Fig.1. Figure 1 of Cousins shows the polysilicon layer 108 (green) formed over the dielectric layer 107 (orange):

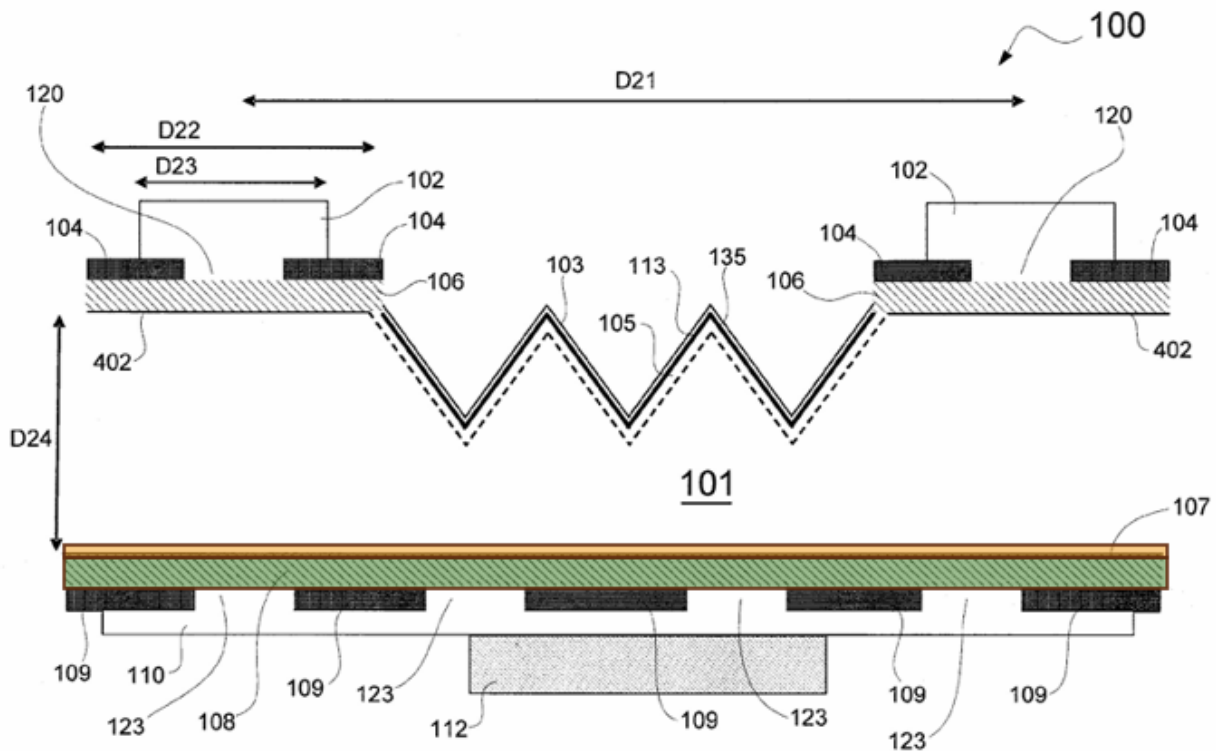
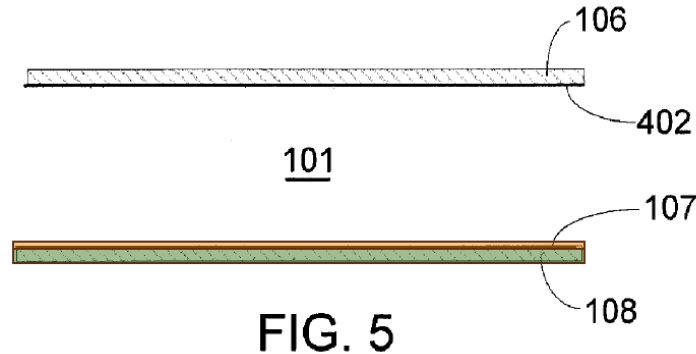


FIG. 1

Ex.1007-Cousins, Fig.1 (annotated).

399. As I explained in Section XI.C.2.c, Figures “4-19” of Cousins “schematically illustrate the fabrication of the solar cell 100.” Ex.1007-Cousins, 4:20-22. After the **thin dielectric layer 107 (orange)** is formed over the N-type silicon substrate 101, “[a] layer of polysilicon is then formed on the thin dielectric layer[] ... 107 to form ... the polysilicon layer 108 on the backside,” as shown in Figure 5. Ex.1007-Cousins, 4:36-46.

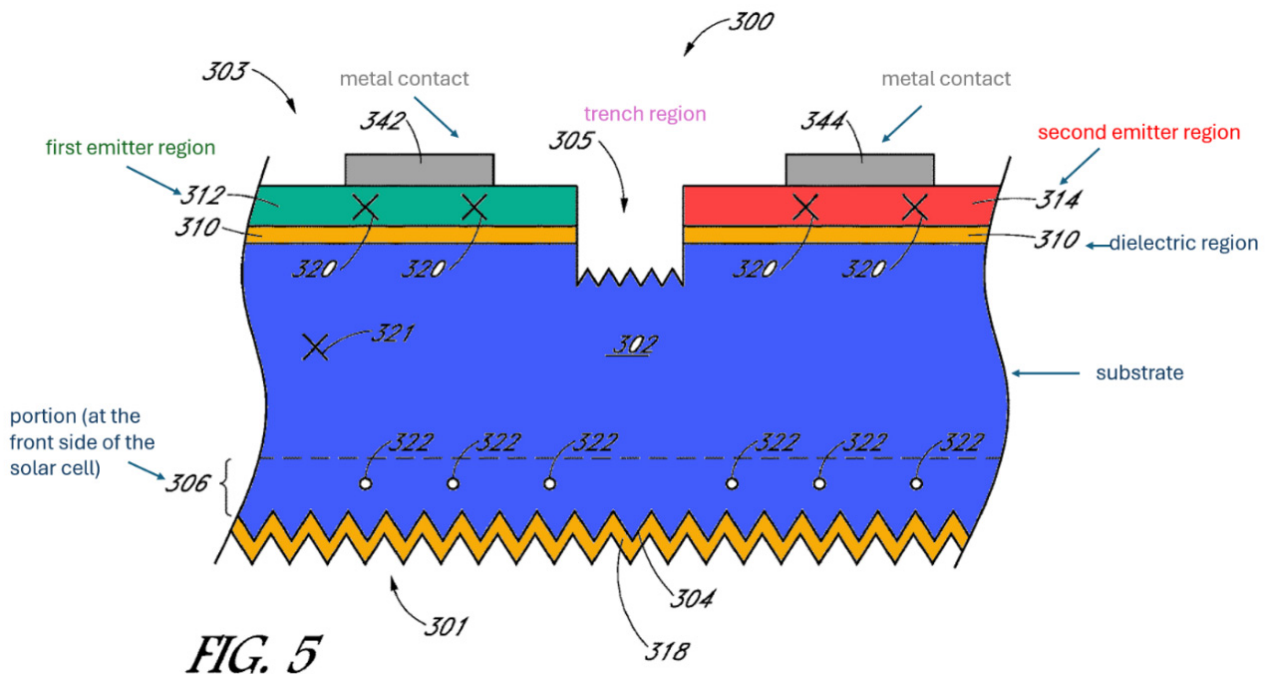


Ex.1007-Cousins, Fig.5 (annotated). “[T]he polysilicon layer 108 may be formed to a thickness of about 1000 to 2000 Angstroms by CVD.” Ex.1007-Cousins, 4:36-46. Thus, the **polysilicon layer 108 (green)** of Cousins is formed over the **dielectric layer 107 (orange)**.

400. As I explained in Section XI.C.2.c, a person of ordinary skill in the art would have understood that Cousins’ dielectric layer 107 is a *dielectric region*. Based on the disclosures of Cousins (e.g., Ex.1007-Cousins, 3:12-13, 4:41-46,

Fig.1), a person of ordinary skill in the art would have understood that Cousins' polysilicon layer 108 is *formed over the dielectric region*.

401. The '315 patent refers to the “P-type and N-type doped polysilicon regions” formed over dielectric region 310 as “first and second emitter regions 312, 314.” Ex.1001-USP315, 6:55-57. In the embodiment of Figure 5, the “first emitter region” is a p-type doped polysilicon region. Ex.1001-USP315, 6:40-57. Figure 5 of the '315 patent shows the dielectric region 310 (orange), first emitter region 312 (green), and second emitter region 314 (red):



Ex.1001-USP315, Fig.5 (annotated).

402. Cousins teaches that the polysilicon layer 108 has the same structure, arrangement, and doping type as the '315 patent's claimed "first emitter region."

Cousins teaches that the polysilicon layer 108 “may be formed by forming a layer of polysilicon by Chemical Vapor Deposition (CVD), such as Low Pressure CVD (LPCVD) or Plasma Enhanced CVD (PECVD), and thermal anneal.” Ex.1007-Cousins, 3:12-17. Cousins further teaches that the polysilicon layer 108 is P-type doped, and the “silicon substrate 101” is N-type doped. Ex.1007-Cousins, 2:39-44. Thus, like the “first emitter region” of the ’315 patent (Ex.1001-USP315, 6:40-57), Cousins’ polysilicon layer 108 is a p-type doped polysilicon region.

403. Cousins also teaches the same arrangement of layers as the ’315 patent for the claimed “substrate,” “dielectric region,” and “first emitter region.” As shown in Figure 5 of the ’315 patent (*see* above Section VIII.A.1), the “first emitter region” is “formed over the dielectric region,” and the “dielectric region” is “formed over the silicon substrate” and “the back side of the solar cell.” Ex.1001-USP315, cl.10. The polysilicon layer 108 of Cousins is likewise “formed on a thin dielectric layer 107,” and the “thin dielectric layer 107” is formed “on the backside surface of the substrate 101.” Ex.1007-Cousins, 3:12-20, Fig.1.

404. Further, the function of the polysilicon layer 108 of Cousins is the same as the ’315 patent’s claimed “first emitter region.” As I discussed above in Section VIII.A.1, the ’315 patent teaches the first emitter region is a “doped region of a solar cell for collecting positive ... charge carriers.” Ex.1001-USP315, 2:40-42. The ’315

patent teaches that, in one embodiment, the substrate is N-type, while the first emitter region is P-type. Ex.1001-USP315, 6:45-46, 6:55-57. As such, the first emitter region forms a PN junction with the silicon substrate.

405. Cousins likewise teaches the “P-type doped polysilicon layer 108 serv[es] as a P-type diffusion region.” Ex.1007-Cousins, 2:39-42. Cousins teaches that the polysilicon layer 108 forms a backside junction with the silicon substrate 101. Ex.1007-Cousins, 1:44-46, 2:39-42 (“the solar cell 100 includes a backside junction formed by a P-type doped polysilicon layer 108 serving as a P-type diffusion region and the N-type silicon substrate 101 servings *[sic]* as an N-type diffusion region”). Further, Cousins teaches “the polysilicon layer 108 has an emitter saturation current [density] of about $10 \text{ fA} \cdot \text{cm}^{-2}$.” Ex.1007-Cousins, 2:42-44. Because Cousins’ P-type polysilicon layer 108 has the opposite type doping to the N-type silicon substrate 101, it forms a PN junction with the substrate that establishes an electric field that directs one type of charge carrier (e.g., holes) to metal contacts 110. *See above* §VII.A.2 . Thus, like the ’315 patent’s claimed “first emitter region,” the P-type polysilicon layer 108 of Cousins collects positive charge carriers that are transported to metal contacts.

406. Based on the structure, arrangement, and function of the first emitter region in the ’315 patent, a person of ordinary skill in the art would have understood

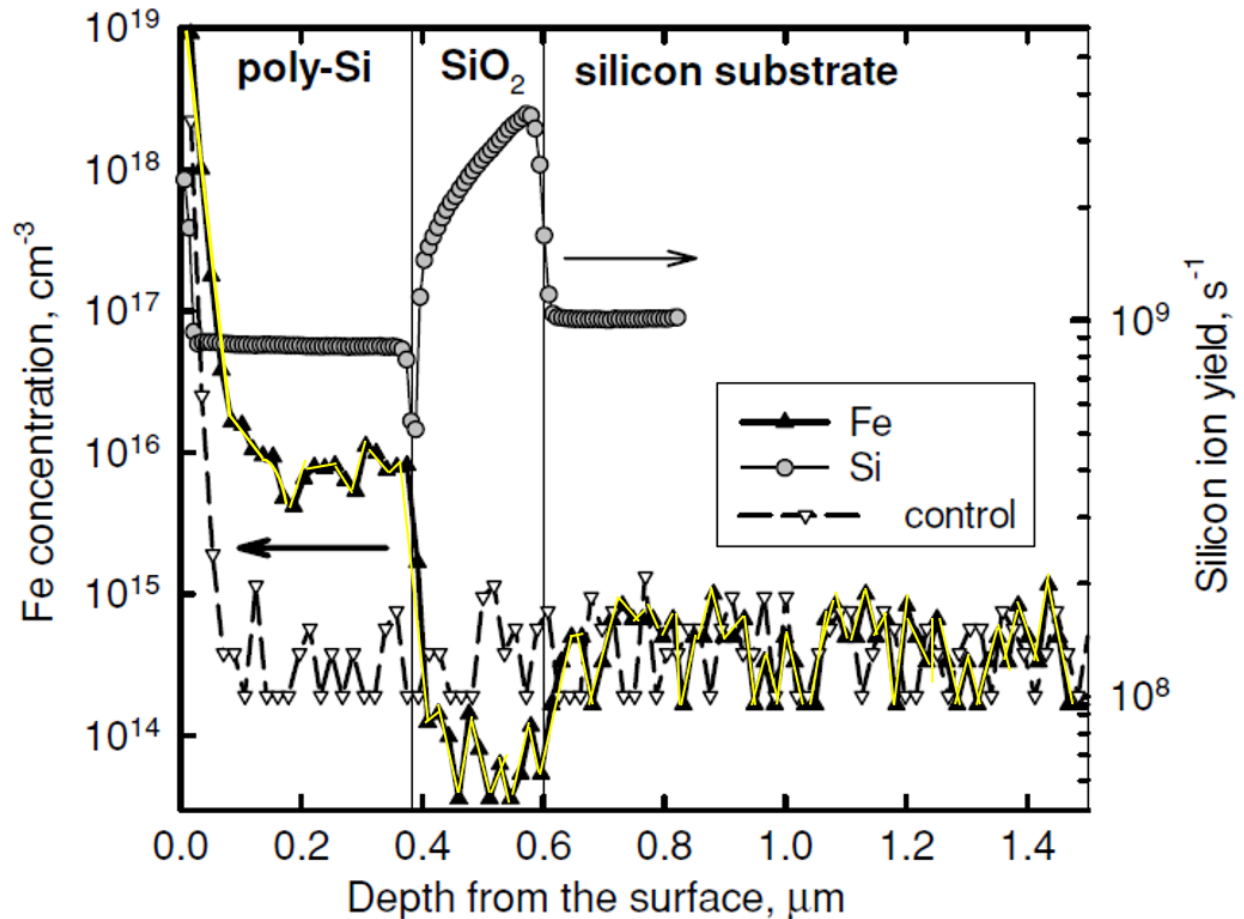
that Cousins' polysilicon layer 108 is *a first emitter region formed over the dielectric region*.

407. As explained in Section VII.B.2.b, gettering to move metal impurities from the substrate into the emitter was well known and described and studied in multiple publications by 2014.

408. Istratov teaches a "test structure" having an oxide layer formed over a silicon substrate and a polysilicon layer formed over the oxide layer. Ex.1012-Istratov, 570 (Fig.2). Istratov's structure has the same layers as Cousins and the '315 patent. Specifically, like Istratov, Cousins has a thin dielectric layer formed over the substrate and a polysilicon layer formed over the thin dielectric layer. Ex.1007-Cousins, 2:63-67. Similarly, like Istratov, the '315 patent has a dielectric region formed over the substrate and a polysilicon region (which the '315 patent calls a "first emitter region") formed over the dielectric region. Ex.1001-USP315, 6:50-62; Ex.1012-Istratov, 569-571, Figs.2, 4-5.

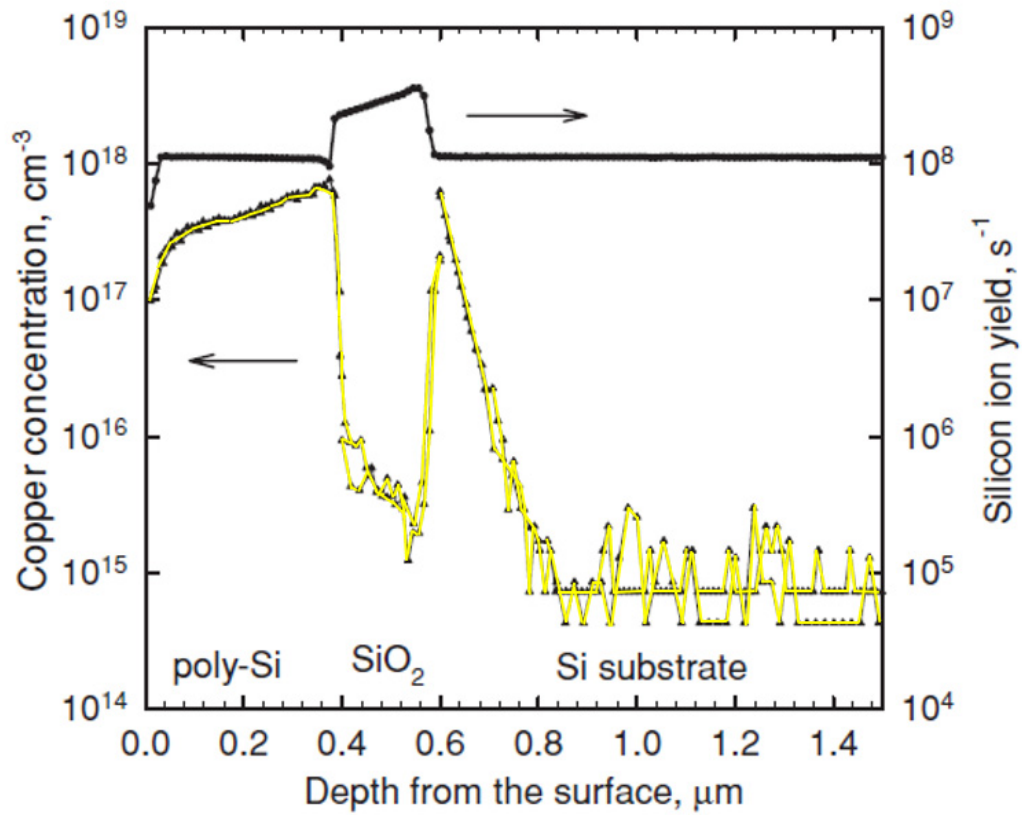
409. Istratov also teaches techniques for gettering metal impurities (iron or copper) into a polysilicon region. For gettering iron, Istratov teaches the accumulation of iron in the polysilicon layer following "annealing for 8 h[ours] at 1020° C." Ex.1012-Istratov, 570. Istratov's Figure 2 shows a higher iron

concentration in the polysilicon layer (left side) than in the silicon substrate (right side) after the annealing step. Ex.1012-Istratov, 570, Fig.2.

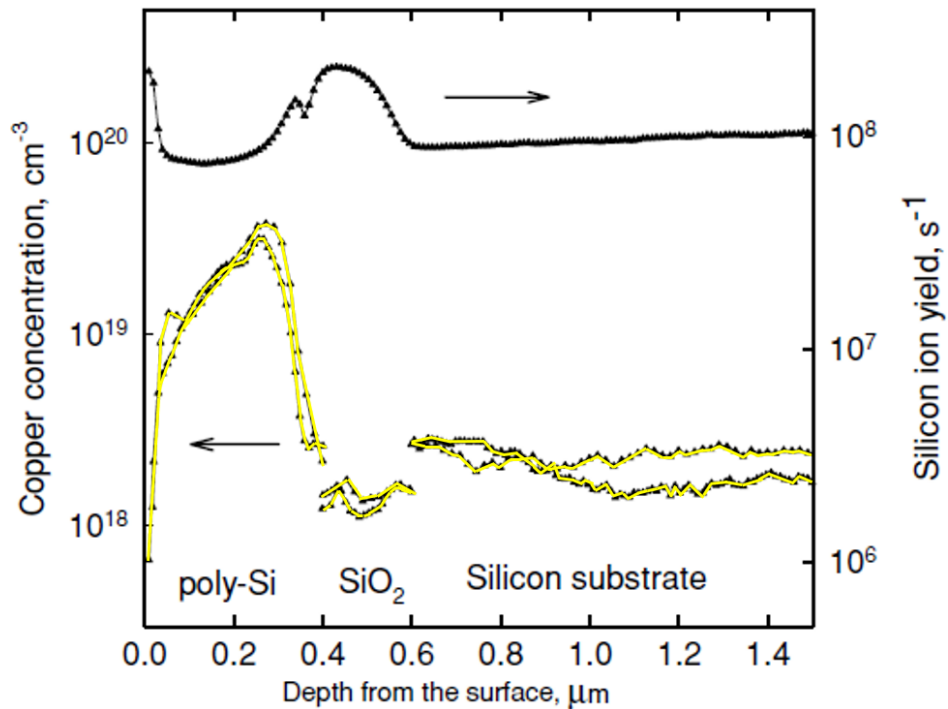


Ex.1012-Istratov, 570, Fig.2 (annotated).

410. For gettering copper, Istratov teaches the accumulation of copper in the polysilicon layer following heating “at 690 °C for 5 h[ours]” or “at 1150 °C for 2 h[ours],” as shown in Figures 4 and 5. Ex.1012-Istratov, 571.



Ex.1012-Istratov, 571, Fig.4 (annotated).



Ex.1012-Istratov, 571, Fig.5 (annotated).

411. A person of ordinary skill in the art would have understood that Istratov teaches a gettering technique that would result in *a first emitter region having metal impurities*.

412. As I explained in Section XI.C.1, a person of ordinary skill in the art would have been motivated to alter Cousins' solar cell in view of Istratov and would have had a reasonable expectation of success in doing so. This would have entailed using Istratov's gettering technique to getter metal impurities from Cousins' substrate 101 to Cousins' polysilicon layer 108.

413. In sum, the combination of Cousins and Istratov teaches *a first emitter region having metal impurities formed over the dielectric region*.

416. As I explained in Sections XI.C.2.c and XI.C.2.d, Figures “4-19” of Cousins “schematically illustrate the fabrication of the solar cell 100.” Ex.1007-Cousins, 4:20-22. After the polysilicon layer 108 (green) of Cousins is formed over the dielectric layer 107 (orange) (Ex.1007-Cousins, 4:36-46, Fig.5), “the metal contact 110 is formed ... [to] make electrical connection to the polysilicon layer 108,” as shown in Figure 17. Ex.1007-Cousins, 6:38-45.

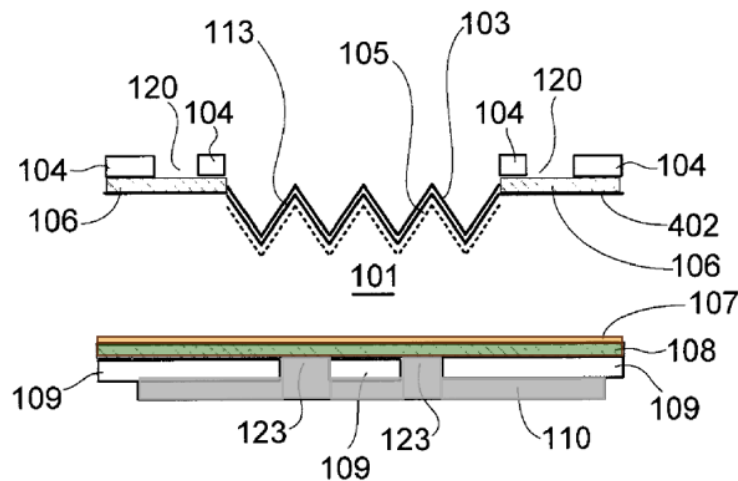


FIG. 17

Ex.1007-Cousins, Fig.17 (annotated). “The metal contact 110 may be formed using a printing process, such as screen printing.” Ex.1007-Cousins, 6:38-45. Thus, the metal contact 110 of Cousins is “formed over” the polysilicon layer 108.

417. A person of ordinary skill in the art would have understood that Cousins' metal contact 110 is *a first metal contact formed over the first emitter region*.

3. **Claim 11: The solar cell of claim 10, wherein the portion of the silicon substrate comprises N-type dopants.**

418. Claim 11 depends from claim 10. Therefore, I incorporate by reference my discussion of claim 10 in Sections XI.C.1-XI.C.2.

419. The combination of Cousins, Granek or Marvin, and Istratov further teaches *the portion of the silicon substrate comprises N-type dopants*. Cousins discloses that the silicon substrate 101 and the doped region 105 are both doped n-type. Ex.1007-Cousins, 2:44-55 (“The N-type silicon substrate 101 may comprise a long lifetime (*e.g.*, 2 to 5 ms) N-type silicon wafer. ... The front side surface of the substrate 101 may be randomly textured (labeled as 113) and includes an N-type doped region 105 formed in the substrate.”). Thus, Cousins teaches *the portion of the silicon substrate comprises N-type dopants*.

4. **Claim 12: The solar cell of claim 10, wherein the portion of the silicon substrate comprises phosphorus.**

420. Claim 12 depends from claim 10. Therefore, I incorporate by reference Sections XI.C.1-XI.C.2.

421. The combination of Cousins, Granek or Marvin, and Istratov further teaches *the portion of the silicon substrate comprises phosphorus*. As I explained in Section XI.C.2.b, a person of ordinary skill in the art would have understood that the doped region 105 of Cousins is the *portion of the silicon substrate [] formed at the*

front side of the solar cell (element 10[a]). Cousins further discloses that the “N-type doped region 105 may be formed by exposing [the solar cell] to phosphorus in the diffusion furnace during the drive-in step.” Ex.1007-Cousins, 5:60-63. Thus, Cousins teaches *the portion of the silicon substrate comprises phosphorus*.

5. **Claim 13: The solar cell of claim 10, wherein the portion of the silicon substrate comprises P-type dopants.**

422. Claim 13 depends from claim 10. Therefore, I incorporate by reference Sections XI.C.1-XI.C.2.

423. The combination of Cousins, Marvin, and Istratov further teaches *the portion of the silicon substrate comprises P-type dopants*. As I explained in Section XI.C.2.b (element 10[a]), Cousins teaches a front side that has a “doped region 105 formed in the substrate.” Ex.1007-Cousins, 2:49-55, Figs.1, 12. A person of ordinary skill in the art would have understood that Cousins’ doped region 105 is the *portion of the silicon substrate [] formed at the front side of the solar cell*.

424. Cousins teaches the silicon substrate 101 and the doped region 105 are both n-type doped. Ex.1007-Cousins, 2:39-55. By 2014, a person of ordinary skill in the art would have understood that the teachings of Cousins are applicable to solar cells with both n-type substrates and p-type substrates. *See, e.g.*, Ex.1042-Cotter, 1896 (“The DSBC solar cell design, which is shown in Fig.5, is ideal for making a direct comparison of solar cell terminal characteristics of solar cells made side-by-

side on n-type and p-type silicon wafers. The DSBC processing sequence can be applied to either p-type or n-type wafers without significant changes in the processing sequence—diffusions, oxidations, and even metallization processes can be applied with good effect to both types of wafers processed in split batches.”). A person of ordinary skill in the art would have understood that a solar cell may be equally fabricated on a p-type substrate (“p-type solar cell”) or an n-type substrate (“n-type solar cell”). Ex.1042-Cotter, 1896. Specifically, a person of ordinary skill in the art would have understood that the design of an n-type solar cell can be translated to be a p-type solar cell by changing the doping type of each of the layers in the n-type solar cell. That is, the n-type regions of the n-type solar cell (including the substrate) become p-type regions, and the p-type regions of the n-type solar cell become n-type regions.

425. As I explained in Sections XI.C.1 and XI.C.2.b, a person of ordinary skill in the art would have been motivated to use Marvin’s FSF dopant concentration of $1\text{E}17$ to $1\text{E}18\text{ cm}^{-3}$ in Cousins’ doped region 105 and would have had a reasonable expectation of success in doing so.

426. Marvin further teaches “that the front surface field (FSF) is a heavily doped region, p^+ in the present case, which covers the entire front face of the solar cell.” Ex.1008-Marvin, 15. As I explained in Section VII.B.2.a, a person of ordinary

skill in the art would have understood that “p+” means a higher concentration of P-type dopants in the p-type substrate. A person of ordinary skill in the art would have understood that the FSF region of Marvin is *the portion of the silicon substrate compris[ing] P-type dopants*.

427. A person of ordinary skill in the art would have been motivated to modify Cousins’ doped region 105 to comprise p-type dopants, as taught by Marvin, with a reasonable expectation of success. Silicon wafers can be either n-type or p-type, and as of the earliest possible priority date of the ’315 patent, p-type silicon wafers were more common and less expensive than n-type silicon wafers. The modification of Cousins’ doped region 105 and substrate 101 from n-type to p-type would have been a design choice (e.g., made to reduce costs or broaden a supply chain), straightforward to implement and within the level of skill of a person of ordinary skill in the art. *See* Ex.1042-Cotter, 1896 (“The DSBC processing sequence can be applied to either p-type or n-type wafers without significant changes in the processing sequence—diffusions, oxidations, and even metallization processes can be applied with good effect to both types of wafers processed in split batches.”).

428. Thus, the combination of Cousins and Marvin teaches *the portion of the silicon substrate comprises P-type dopants*.

6. **Claim 14: The solar cell of claim 10, wherein the portion of the silicon substrate comprises boron.**

429. Claim 14 depends from claim 10. Therefore, I incorporate by reference Sections XI.C.1-XI.C.2.

430. The combination of Cousins, Marvin, and Istratov further teaches *the portion of the silicon substrate comprises boron*. As I explained in Section XI.C.2.b (element 10[a]), Cousins teaches a front side that has a “doped region 105 formed in the substrate.” Ex.1007-Cousins, 2:49-55, Figs.1, 12. A person of ordinary skill in the art would have understood that Cousins’ doped region 105 is the *portion of the silicon substrate [] formed at the front side of the solar cell*.

431. As I explained in Section XI.C.5, a person of ordinary skill in the art would have been motivated to modify Cousins’ doped region 105 to comprise p-type dopants, as taught by Marvin, with a reasonable expectation of success.

432. Cousins further discloses a common doping technique, diffusion, for driving dopants into a silicon wafer. *See* above §VII.A.1. Cousins teaches that a “P-type dopant source 403 provides a source of P-type dopants for diffusion into” a layer of the solar cell, and that “the P-type dopant source 403 comprises BSG (borosilicate glass).” Ex.1007-Cousins, 4:47-60. As I explained above in Section VII.A.1, it was well known prior to 2014 that boron was commonly used as a dopant to create p-type regions or layers. Ex.1023-Nelson, 181-182. As I explained above

in Section VII.A.1, borosilicate glass (BSG) diffusion was a common technique for diffusing boron into a silicon wafer or polysilicon layer. A person of ordinary skill in the art would have understood that the borosilicate glass is a layer of silicon oxide doped with boron that is deposited or formed over a solar cell substrate or layer. A person of ordinary skill in the art would have understood that the borosilicate glass is used to dope a region or layer of the solar cell with boron atoms.

433. Cousins teaches that “the P-type dopant source 403 provides a source of P-type dopants for diffusion into the polysilicon layer 108.” Ex.1007-Cousins, 4:47-51. As I explained in Section VII.A.1, diffusion was commonly used during solar cell fabrication to dope the regions of a substrate or layer. A person of ordinary skill in the art would have understood that the diffusion doping technique disclosed in Cousins could have been used for either the polysilicon layer or the silicon substrate. Thus, a person of ordinary skill in the art would have understood that Cousins contemplates diffusing P-type dopants using borosilicate glass (BSG) into the doped region 105.

434. As I explained in Section VII.A.1, techniques for doping solar cell layers with boron were well-established by 2014. A person of ordinary skill in the art would have known that there are a limited number of elements that can be used to dope a silicon region p-type—namely elements from Group III of the periodic

table. Consequently, it would have been obvious for a person of ordinary skill in the art to try boron as the p-type dopant to dope the front side of the substrate 101 of Cousins. Moreover, as I explained in Section VII.A.1, the use of BSG was a well-known technique to introduce boron dopants into a silicon region. When implementing the doped region 105 with p-type dopants, a person of ordinary skill in the art would have been motivated to look to well known doping steps, including the borosilicate glass technique disclosed by Cousins. Ex.1007-Cousins, 4:54-60.

435. Thus, the combination of Cousins and Marvin teaches *the portion of the silicon substrate comprises boron*.

7. **Claim 15: The solar cell of claim 10, wherein the first emitter region comprises polysilicon.**

436. Claim 15 depends from claim 10. Therefore, I incorporate by reference Sections XI.C.1-XI.C.2.

437. The combination of Cousins, Granek or Marvin, and Istratov further teaches *the first emitter region comprises polysilicon*. As I explained in Section XI.C.2.b-XI.C.2.d, a person of ordinary skill in the art would have understood that Cousins' polysilicon layer 108 is *the first emitter region*. Cousins teaches that the polysilicon layer 108 “may be formed by forming a layer of polysilicon by Chemical Vapor Deposition (CVD), such as Low Pressure CVD (LPCVD) or Plasma

Enhanced CVD (PECVD), and thermal anneal.” Ex.1007-Cousins, 3:12-17. Thus, Cousins teaches *the first emitter region comprises polysilicon*.

XII. SECONDARY CONSIDERATIONS

438. As I explained in Section III.C, I understand that secondary considerations may support or rebut the obviousness of a claim. I am not aware of any secondary considerations that support that the claims of the '315 patent are nonobvious. To the extent Patent Owner argues that secondary considerations are relevant here, I reserve the right to respond.

XIII. AVAILABILITY FOR CROSS-EXAMINATION

439. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

XIV. RIGHT TO SUPPLEMENT

440. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to take into account new information as it becomes available to me.

XV. JURAT

441. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: August 8, 2024


/s/ _____
Zachary C. Holman, Ph.D.

APPENDIX A

ZACHARY CHARLES HOLMAN

Professor and Vice Dean

School of Electrical, Computer, and Energy Engineering
Arizona State University
Tempe, AZ 85287-5706

Phone: (480) 965-9959
Fax: (480) 965-3837
zachary.holman@asu.edu

APPOINTMENTS

08/2023–	Vice Dean for Research and Innovation Ira A. Fulton Schools of Engineering, Arizona State University (Tempe, Arizona)
08/2023–	Professor School of Electrical, Computer, and Energy Engineering, Arizona State University (Tempe, Arizona)
08/2019–07/2023	Associate Professor School of Electrical, Computer, and Energy Engineering, Arizona State University (Tempe, Arizona)
08/2019–06/2023	Director of Faculty Entrepreneurship Ira A. Fulton Schools of Engineering, Arizona State University (Tempe, Arizona)
06/2021–	Cofounder Beyond Silicon, Inc. (Chandler, Arizona)
03/2020–	Cofounder Sunflex Solar LLC (Phoenix, Arizona)
07/2016–	Cofounder and Chief Technology Officer Swift Coat, Inc. (Tempe, Arizona)
03/2013–07/2019	Assistant Professor School of Electrical, Computer, and Energy Engineering, Arizona State University (Tempe, Arizona)
07/2014–08/2014	Visiting Professor Photovoltaics and Thin-Film Electronics Laboratory, Institute of Microengineering, Ecole Polytechnique Fédérale de Lausanne (Neuchâtel, Switzerland)
10/2010–03/2013	Postdoctoral Researcher Photovoltaics and Thin-Film Electronics Laboratory, Institute of Microengineering, Ecole Polytechnique Fédérale de Lausanne (Neuchâtel, Switzerland)

EDUCATION

10/2010	Doctor of Philosophy Mechanical Engineering; Nanoparticle Science and Engineering (minor), University of Minnesota (Minneapolis, Minnesota) Dissertation: <i>Germanium nanocrystal solar cells</i> ; Advisor: Prof. Uwe Kortshagen
05/2005	Bachelor of Arts Physics, Reed College (Portland, Oregon) Thesis: <i>Electron transport in amorphous silicon</i> ; Advisor: Prof. John Essick

RESEARCH INTERESTS

Broad research interests span the fields of solar cells, coatings, nanotechnology, semiconductors, plasmas, and aerosols. Specific interests include silicon-based tandem solar cells, contacts to solar cells, light management

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in solar cells, novel uses of nanoparticles in devices, semiconductor nanoparticles, optical and electronic properties of nanoscale materials, plasma synthesis of powders, and deposition of powders and thin films.

AWARDS & HONORS

2023	ASU Fulton Schools of Engineering Top 5% Teaching Award
2022	Hopkins Professorship
2021	American-Made Perovskite Startup Prize Winner
2020	American-Made Solar Prize Winner
2019	IEEE Stuart R. Wenham Young Professional Award
2019	NSF CAREER Award
2018	Gordon and Betty Moore Foundation Inventor Fellowship
2018	Fulton Entrepreneurial Professorship
2017	ASU Fulton Schools of Engineering Top 5% Teaching Award
2016	Trustees of ASU Professorship
2016	Joseph C. Palais Distinguished Faculty Scholar Award
2016	Fulton Outstanding Assistant Professor Award
2015	ASU Fulton Schools of Engineering Top 5% Teaching Award
2014	ASU Senior Sustainability Scientist
2013	3 rd International Conference on Crystalline Silicon Photovoltaics top 5% of papers
2010	NSF EAPSI Fellowship at the Tokyo Institute of Technology
2010	University of Minnesota Doctoral Dissertation Fellowship
2008	Particle Society of Minnesota Scholarship
2007	18 th International Symposium on Plasma Chemistry Best Paper Award
2005	NSF IGERT Fellowship at the University of Minnesota

AWARDS WON BY STUDENTS AND POSTDOCS

2023	Bernard Henry AIMCAL-SVC Scholarship (Zach Leuty)
2022	ARCS (Achievement Awards for College Scientists) Award (David Quispe)
2022	Hool Coury Law Tech Venture Challenge Winner (Wahab Alasfour, Zach Leuty, David Quispe)
2021	ASU Presidential Graduate Assistantship (Vidya Krishnan)
2021	NSF Graduate Research Fellowship (David Quispe)
2021	American-Made Perovskite Startup Prize Winner (Jason Yu, Wahab Alasfour, Zach Leuty, David Quispe)
2020	American-Made Solar Prize Winner (Kate Fisher, Jason Yu, Barry Hartweg)
2020	ASU Dean's Fellowship (Mason Mahaffey)
2020	NSF Graduate Research Fellowship (Justin Huxel)
2020	QESST Best Paper Award (Zachary Leuty)
2019	SiliconPV Best Poster Award (William Weigand and Jason Yu)
2018	ASU Dean's Fellowship (Barry Hartweg)
2018	Palais' Outstanding Doctoral Student Award (Jason Yu)
2018	Venture Madness Hardware Tech Winner (Peter Firth)

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2017	European PV Solar Energy Conference and Exhibition Student Award (Jason Yu)
2017	IEEE Photovoltaic Specialists Conference Most Outstanding Technical Contribution (Jason Yu)
2017	MRS Graduate Student Silver Award (Jason Yu)
2017	Rice Business Plan Competition Department of Energy Cleantech University Prize (Peter Firth and Jonathan Bryan)
2017	ASU Innovation Open SRP Innovation Award (Peter Firth)
2017	SiliconPV Award (Jason Yu)
2017	SiliconPV Award (Mathieu Boccard)
2017	ASU Graduate and Professional Student Association Research Award (Jason Yu)
2017	ThinkSwiss Research Scholarship (Nathan Rodkey)
2017	ARCS (Achievement Awards for College Scientists) Award (Peter Firth)
2017	Zero Mass Water Materials Award (Peter Firth)
2017	DOE Science Undergraduate Laboratory Internship at NREL (Nathan Rodkey)
2017	Rhodes Scholarship (Ngoni Mugwisi)
2016	Palais Senior Design Prize (Heliovation senior design team)
2016	Arizona Student Energy Conference Distinguished Poster Award (Jason Yu)
2016	IEEE Photovoltaic Specialists Conference Best Paper Award (Mathieu Boccard)
2016	IEEE Photovoltaic Specialists Conference Best Poster Award (Mathieu Boccard)
2016	ASU Dean's Fellowship (Will Weigand)
2016	ASU Dean's Fellowship (Jonathan Bryan)
2016	ASU New Venture Challenge Winner (Peter Firth)
2016	ARCS (Achievement Awards for College Scientists) Award (Peter Firth)
2016	Micron Technology Team Prize (Hall Effect senior design team)
2015	IEEE Photovoltaic Specialists Conference Best Poster Award (Jason Yu)
2015	Harold and Lucille Dunn Memorial Engineering Scholarship (Jason Yu)
2015	Barrett Electronic Materials Fellowship (Peter Firth)
2015	ASU Dean's Fellowship (Peter Firth)
2015	Arizona Student Energy Conference Distinguished Poster Award (Priyaranga Koswatta)
2015	NSF Graduate Research Fellowship (Joe Carpenter)
2014	NSF Integrative Graduate Education and Research Traineeship (Michael Bernstein)
2014	NSF Integrative Graduate Education and Research Traineeship (Joe Carpenter)
2014	University Graduate Fellowship (Salman Manzoor)

PROFESSIONAL ACTIVITIES & OUTREACH

- Editor of the IEEE Journal of Photovoltaics (2022–)
- Member of the Industry Liaison Committee for the World Conference on Photovoltaic Energy Conversion (2022)
- Member of the Program Committee for the IEEE Photovoltaic Specialists Conference (2020)
- Member of the Organizing Committee for the International Workshop on Silicon Heterojunction Solar Cells (2019, 2020)
- Symposium Organizer for the E-MRS Spring Meeting (2017)
- Symposium Organizer for the IEEE Photovoltaic Specialists Conference (2016, 2017, 2018, 2021)
- Symposium Organizer or Lead Symposium Organizer for the MRS Spring Meeting (2015, 2016, 2018)

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- Session Chair for IEEE Photovoltaic Specialists Conference, MRS Spring Meeting, SiliconPV (2013–)
- Member of the Fulton Schools of Engineering Dean’s Research Committee (2017–2019)
- Member of the Fulton Schools of Engineering Master Mentors (2019–)
- Co-leader of Thrust 2 of the Quantum Energy and Sustainable Solar Technology ERC (2015–2020)
- Member of the ASU Goldwater Materials Science Facility Steering Committee (2014–2016)
- Member of the ASU Leadership Academy Materials Team (2015–2016)
- Member of the ASU University Undergraduates Standards Committee (2015–2017)
- Member of the ASU Instrument Design and Fabrication Board (2016–2019; 2020–)
- Member and Chair of the ASU Advanced Electronics and Photonics Core Facility Board (2020–)
- Member of the ASU Solar Fabrication Core Facility Board (2021–)
- Member of the ASU Eyring Materials Center Board (2017–2021)
- Member or Chair of an ASU ECEE Faculty Search Committee (2015, 2018, 2020, 2021, 2022)
- Member of the ASU ECEE Website Design Committee (2015, 2019)
- Member of the ASU Faculty Working Group for the MS degree in Innovation and Venture Development
- Designer and instructor of a new course entitled *EEE 598: Manuscript Writing for Engineers*
- Reviewer for funding bodies, including NSF and DOE, and journals, including *Journal of Applied Physics*, *ACS Nano*, *Solar Energy Materials and Solar Cells*, *Thin Solid Films*, *Nanotechnology*, *IEEE Journal of Photovoltaics*
- Volunteer Scientist for ASU’s Night of The Open Door, ASU’s Summer Transportation Institute, Cesar Chavez High School, Minnesota FIRST LEGO League, and the Science Museum of Minnesota

FUNDING

11/2023–10/2028	NSTXL Microelectronics Commons, “Southwest Advanced Prototyping (SWAP) Hub,” (Co-PI)
10/2023–05/2027	DOE SETO, “TEAMUP: Tandems for efficient and advanced modules using ultrastable perovskites,” (Co-PI)
07/2023–04/2024	DOE BES SBIR, “Development of new metallization pastes for front-side tunnel oxide passivated contact crystalline silicon solar cells,” (Co-PI)
07/2023–06/2024	TSMC, confidential project, (PI)
04/2023–03/2024	Applied Materials, confidential project, (PI)
10/2022–10/2023	DOE SETO, “PV Foundry: Increasing manufacturing innovation and capabilities in the US,” (PI)
09/2022–08/2024	US Department of State, “GIST Innovates the Balkans,” (Co-PI)
11/2021–10/2026	USAID, “Center of Excellence for Energy,” (Co-PI)
11/2021–10/2022	AZ New Economy Initiative, “Suns-ERE: A characterization tool to accelerate the learning cycle of thin-film photovoltaics,” (PI)
10/2021–09/2024	EDA Build to Scale, “Arizona semiconductor industry startup entrepreneurial development project,” (Co-PI)
10/2021–11/2025	DOE SETO, “Manufacturing 27%-efficient perovskite/silicon tandem photovoltaic cells using slot die coating at >5000 wafers per hour,” (Co-PI)
04/2021–03/2024	DOE SETO, “The role of hydrogen in the performance and long-term stability of high-efficiency silicon cells and modules,” (Co-PI)

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01/2021–12/2022	Sunflex Solar, “Scaling Sunfoil solar modules,” (PI)
08/2020–08/2020	Corporate gift (PI)
04/2020–03/2023	DOE SETO, “Sonic Wafering™ of III-V substrates for high efficiency cells: A path to <\$0.50/W,” (Co-PI)
10/2019–09/2020	US Government, “Flexible and advanced solar panel technologies,” (PI)
08/2019–07/2021	NSF, “Center to center (C2C) international collaboration on advanced photovoltaics: Electrode manufacturing and indoor power applications,” (Co-PI)
08/2019–07/2022	DOE SETO, “Scalable manufacturing of efficient perovskite/silicon tandem modules,” (Co-PI)
03/2019–02/2024	NSF CAREER, “CAREER: Transparent, passivating, and carrier-selective heterojunction contacts for silicon and cadmium telluride solar cells,” (PI)
01/2019–12/2021	DOE SETO, “Diagnosing and overcoming recombination and resistive losses in non-silicon solar cells using a silicon-inspired characterization platform,” (PI)
01/2019–12/2021	DOE SETO, “Bringing high-efficiency silicon solar cells with heterojunction contacts to market with a new, versatile deposition technique,” (PI)
01/2019–06/2020	DOE SETO, “Wide-bandgap polycrystalline III-Vs as transparent, carrier-selective heterojunction contacts for silicon photovoltaics,” (Co-PI)
01/2019–12/2020	NREL, “ASU-NREL joint silicon solar cell research: passivated contacts, metallization, and bulk defects,” (PI)
01/2019–12/2021	ARPA-E DAYS, “Solid state thermal battery,” (Co-PI)
01/2019–12/2019	FSE/CLAS/AMI Seed, “MRSEC planning and preliminary data collection,” (Co-PI)
10/2018–09/2020	Fulton Entrepreneurial Professors Program, “Aerosol impaction-driven assembly of functional nanomaterial coatings,” (PI)
10/2018–09/2021	Moore Foundation Inventor Fellowship, “Aerosol impaction-driven assembly of functional nanomaterial coatings,” (PI)
10/2018–09/2019	FSE/CLAS/AMI Seed, “Diamond and III-nitride integration for ultra-gap devices,” (PI)
06/2018–05/2019	NSF SBIR, “Non-thermal plasma source for functional metal-oxide nanoparticle coatings,” (Co-PI)
02/2018–09/2018	NREL, “PERC and SHJ silicon solar modules with high infrared reflectance,” (Co-PI)
01/2018–01/2021	ARENA, “Hydrogenated and hybrid heterojunction p-type silicon PV cells R&D project,” (Co-PI)
10/2017–09/2020	DOE PVRD-II, “Perovskite-on-silicon tandem solar cells,” (Co-PI)
10/2017–05/2020	DOE DuraMAT, “Silicon IBC modules with copper foil electrodes: Failure mechanisms of electrically conductive adhesive bonds between cells and foil,” (PI)
10/2017–09/2018	BAPVC, “Low capex solar manufacturing enabled by perovskite semiconductors,” (Co-PI)
08/2017–01/2019	ACAP, “P-type hybrid heterojunction solar cells,” (Co-PI)
05/2017–04/2019	NSF EAGER, “Collaborative research: 30%-efficient, stable perovskite/silicon monolithic tandem solar cells,” (PI)

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02/2017–04/2017	NSF SBIR, “The aerosol-spray deposition of photoluminescent quantum-dot coatings on substrates,” (Co-PI)
01/2017–12/2019	ARPA-E SHIELD, “Single-pane windows with insulating sprayed particulate coatings,” (PI)
12/2016–11/2017	NSF SBIR, “Low damage sputter magnetron for silicon heterojunction PV production,” (Co-PI)
11/2016–10/2018	DOE NextGen-III, “Developing efficient silicon cells for perovskite/silicon tandem devices,” (Co-PI)
09/2016–08/2017	American Jobs Project, “Arizona’s advanced energy landscape,” (PI)
08/2016–07/2019	DOE PVRD, “Monolithic silicon module manufacturing at < 0.40 \$/W,” (PI)
08/2016–07/2018	DOE PVRD, “15%-efficiency (Mg,Zn)CdTe solar cells with 1.7 eV bandgap for tandem applications,” (PI)
08/2016–07/2017	SolarReserve, “Hybrid heliostat development,” (PI)
07/2016–01/2017	FSE Technology Innovation Laboratory, “Advanced manufacturing of nanoparticle-based coatings,” (PI)
06/2016–05/2017	DOE PVRD SIPS, “A new class of tandems: Optically coupled III-V/silicon module with outdoor efficiency exceeding 30%,” (PI)
05/2016–11/2016	FSE Technology Innovation Laboratory, “Hybrid heliostat for combined photovoltaic and solar thermal power plants,” (PI)
04/2016–03/2019	NSF REU Site, “Solar energy research for the Terawatt Challenge,” (PI)
01/2016–12/2018	DOE SuNLaMP, “Overcoming bottlenecks to low-cost, high-efficiency Si PV and industrially relevant, ion implanted interdigitated back passivated contact cell development,” (Co-PI)
09/2015–08/2018	NSF Energy for Sustainability, “Collaborative research: 30%-efficient III-V/silicon tandem solar cells,” (PI)
08/2015–07/2020	NSF ERC, “Nano-Enabled Water Treatment: NEWT,” (Co-PI)
06/2015–05/2020	USAID, “U.S.-Pakistan Centers for Advanced Studies in Energy,” (Co-PI)
05/2015–04/2016	ARPA-E I-Corps Supplement, “PVMirror: Cost competitive solar with storage,” (PI)
02/2015–01/2017	RCSA Scialog, “Scalable tandem architecture for solar water splitting,” (PI)
06/2014–05/2017	ARPA-E FOCUS, “PVMirror: A solar concentrator mirror incorporating PV cells,” (PI)
09/2013–08/2016	DOE FPACE-II, “Thin silicon solar cells: A path to 35% Shockley-Queisser limits,” (Co-PI)
08/2011–07/2021	NSF/DOE ERC, “Quantum Energy and Sustainable Solar Technologies: QESST,” (Co-PI)
06/2010–08/2010	NSF EAPSI, “Novel solar cells using silicon nanocrystals synthesized in an atmospheric-pressure plasma,” (PI)

STUDENTS, POSTDOCS, AND STAFF ADVISED

• Ph.D.:	Ashling Leilaoui (2013–2018)	Jianwei Shi (2013–2018)
	Jason Yu (2014–2018)	Salman Manzoor (2014–2019)
	Joe Carpenter (2014–2020)	Peter Firth (2015–)

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- | | | |
|---------------------|---|--|
| | Jonathan Bryan (2016–2021) | William Weigand (2016–2023) |
| | Barry Hartweg (2018–2023) | Warda Mushtaq (2018–) |
| | Zachary Leuty (2019–) | Abdulwahab Alasfour (2019–) |
| | David Quispe (2019–) | Mark Li (2019–) |
| | Alan Wu (2019–2021) | Mason Mahaffey (2020–) |
| | Vidya Krishnan (2021–) | Maria Garcia (2021–) |
| | Jason Ro (2022–) | |
| • M.S.: | Salman Manzoor (2013–2014) | Prateek Garg (2013–2015) |
| | Priyaranga Koswatta (2013–2016) | Peter Firth (2014–2015) |
| | Michael Bernstein (2014–2016) | Alec Jackson (2014–2016) |
| | Trent Hoffman (2016–2017) | Sujyot Mony (2018–2019; MORE) |
| | Sagnik Dasgupta (2019–2020) | |
| • Undergraduate: | Claire Block (2017–2018) | Joe Carpenter (2013–2014; FURI) |
| | Christopher Chen (2017–2019) | Angelo Delluomo (2015–2016; FURI) |
| | Angelica Guzman (2018–2019; FURI) | Justin Huxel (2017–2019; FURI) |
| | Sanketh Kamath (2013–2015; FURI) | Mark Kapron (2017–2018; FURI) |
| | Ngoni Mugwisi (2016–2017; Barrett) | Corbin Ott (2017–2018; FURI) |
| | Marcial Rodarte (2016–2017) | Nathan Rodkey (2015–2018; FURI, Barr.) |
| | Kari Sanford (2015–2017; FURI, Barrett) | Nicholas Scheenstra (2015–2016; FURI) |
| | Daniel Sinclair (2017–2018; FURI) | Marshall Styers (2015–2016) |
| | Brian Wu (2018–2019; FURI) | John Hsu (2021–2021; SURI) |
| • Postdoc: | Mathieu Boccard (2014–2016) | Drew Swanson (2016–2017) |
| | Martyn Fisher (2016–2018) | Arthur Onno (2017–2020) |
| | Shaline Kavadiya (2018–2020) | Shannon Poges (2018–2020) |
| | Salman Manzoor (2019–2020) | Joe Carpenter (2020–2020) |
| | Thomas Fiducia (2021–2023) | |
| • Staff: | Kathryn Fisher (2014–) | Nathan Rodkey (2018–2019) |
| | Albert Victoria (2019–) | Mark George (2020–) |
| | Juan Venegas (2021–2022) | John Hsu (2021–) |
| • Research faculty: | Jason Yu (2018–) | Arthur Onno (2020–2022) |
| • REU visitor: | Emily Dafflon (2013) | Ethan Bendau (2015) |
| | Juan Asencio (2018) | William Firth (2015) |
| | Culver McWhirter (2016) | Amine El Mahati (2016) |
| | Jones Ou (2016) | Matthew Warner (2016) |
| | Jakob Häusele (2017) | Noemi Mundhaas (2017) |
| | Stefan Mercado (2017) | Syeda Mohsin (2017) |
| | Tien Ngo (2017) | Yuji Okamoto (2017) |
| | David Quispe (2017) | Mateo Estrada (2018) |
| | Jewel Haik (2018) | Richelle Javier (2018) |
| | Xingyi Wang (2019) | Alexa Cetta (2019) |
| | Jorge Almeida (2019) | Maria Garcia (2019) |
| • PCASE visitor: | Saleem Ahmed (2016) | Asad Ali (2016) |
| | Asghar Ali (2016) | Waqar Ali (2016) |
| | Farah Qazi (2016) | Ijaz Husnain (2016) |
| | Mahmood Jamil (2016) | Mehwish Javed (2016) |
| | Syeda Qudsia (2016) | Warda Mushtaq (2016) |
| | Maham Akhlaq (2017) | Kamran Alam (2017) |
| | Maoz (2017) | Asma Shamim (2017) |

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Hira Rehman (2017)
Maria Kanwal (2018)
Fazal Subhan (2018)
Qandeel Rehman (2019)
Muneeza Ahmad (2019)

Shah Naveed (2017)
Sundas Khan (2018)
Mudasar Rashid (2019)
Kashan Ahmad (2019)
Saddam Hussain (2019)

COURSES TAUGHT

- EEE 352: Properties of Electronic Materials (F15, F16, F17, F18)
- EEE 436/591: Fundamentals of Solid State Devices (F13, F14, S16)
- EEE 465/591: Photovoltaic Energy Conversion (S15)
- EEE 498/591: Solar Energy (S14)
- EEE 536: Semiconductor Characterization (S17)
- EEE 565: Solar Cells (F22)
- EEE 598: Manuscript Writing for Engineers (F14, F15, F17, F18, F19, F20, F21, F22)
- ASU 101: The ASU Experience (F14)
- IVD 561: Innovation Studio II: Problem Reframing (F21)
- IVD 562: Innovation Studio III: Explore, Fail, Solve (S21, S22)

PEER-REVIEWED PUBLICATIONS

(ASU students in red; ASU postdocs and staff in orange)

111. Z. Leuty, M. George, M. Garcia, Z. Yu, and Z. Holman, "High mobility soft sputtered ITO coatings by dual gas-flow sputtering," (submitted).
110. Z. Leuty, W. Weigand, J. Ochoa, J. Carpenter, Z. Yu, M. Bertoni, and Z. Holman, "Ultra-high throughput inline deposition of silicon oxide for polycrystalline silicon passivating contacts," (submitted).
109. G. Yang, Z. Yu, M. Wang, Z. Shi, Z. Ni, H. Jiao, C. Fei, A. Wood, A. Alasfour, B. Chen, Z. Holman, and J. Huang, "Shunt mitigation toward efficient large-area perovskite-silicon tandem solar cells," *Cell Reports Phys. Sci.* **4**, 101628 (2023).
108. M. Mahaffey, A. Onno, C. Reich, A. Danielson, W. Sampath, and Z. Holman, "Measuring the absorber doping concentration of Si, CdSeTe, and perovskite solar cells using injection-dependent quasi-steady-state photoluminescence," *IEEE J. Photovoltaics* **13**, 800–807 (2023).
107. B. Hartweg, K. Fisher, J. Ro, and Z. Holman, "Qualification of laser-weld interconnection of aluminum foil to back-contact silicon solar cells," *Sol. Energy Mater. Sol. Cells* **266**, 112647 (2023).
106. D. Quispe, B. Eng, M. Kim, A. Onno, B. Coppa, Z. Yu, M. Lee, and Z. Holman, "Optical constants of polycrystalline $\text{Al}_{0.25}\text{Ga}_{0.75}\text{P}$ and $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$ determined by variable-angle spectroscopic ellipsometry," *J. Appl. Phys.* **134**, 073104 (2023).
105. J. Levi, S. Guo, S. Kavadiya, Y. Luo, C.-S. Lee, H. Jacobs, Z. Holman, M. Wong, S. Garcia-Segura, C. Zhou, b. Rittmann, and P. Westerhoff, "Comparing methods to deposit Pd-In catalysts on hydrogen-permeable hollow-fiber membranes for nitrate reduction," *Water Res.* **235**, 119877 (2023).
104. G. Yang, M. Wang, C. Fei, H. Gu, Z. Yu, A. Alasfour, Z. Holman, and J. Huang, "Recycling silicon bottom cells from end-of-life perovskite-silicon tandem solar cells," *ACS Energy Lett.* **8**, 1639–1644 (2023).

103. A. Bothwell, C. Reich, A. Danielson, [A. Onno](#), [Z. Holman](#), W. Sampath, and D. Kuciauskas, “Charge carrier lifetime determination in graded absorber solar cells using time-resolved photoluminescence simulations and measurements,” *Solar RRL*, 2201029 (2023).
102. A. Danielson, C. Reich, R. Pandey, A. Munshi, [A. Onno](#), [W. Weigand](#), D. Kuciauskas, S. Li, A. Bothwell, J. Guo, M. Murugeson, J. McCloy, R. Klie, [Z. Holman](#), and W. Sampath, “Electro-optical characterization of arsenic-doped CdSeTe and CdTe solar cell absorbers doped in-situ during close space sublimation,” *Sol. Energy Mater. Sol. Cells* **251**, 112110 (2023).
101. [B. Hartweg](#), [K. Fisher](#), [S. Niverty](#), N. Chawla, and [Z. Holman](#), “Analysis of electrically conductive adhesives in shingled solar modules by X-ray imaging techniques,” *Microelectron. Reliab.* **136**, 114627 (2022).
100. B. Chen, Z. Yu, [A. Onno](#), [Z. Yu](#), S. Chen, J. Wang, [Z. Holman](#), and J. Huang, “Bifacial all-perovskite tandem solar cells,” *Sci. Adv.* **8**, eadd0377 (2022).
99. G. Yang, Z. Ni, [Z. Yu](#), Z. Yu, B. Larson, B. Chen, [A. Alasfour](#), X. Xiao, J. Luther, [Z. Holman](#), and J. Huang, “Defect engineering in wide bandgap perovskites for efficient perovskite-silicon tandem solar cells,” *Nature Photonics* **16**, 588–594 (2022).
98. H. Bauser, M. Foley, M. Phelan, [W. Weigand](#), D. Needell, [Z. Holman](#), and H. Atwater, “Amorphous silicon carbide high contrast gratings as highly efficient spectrally selective visible reflectors,” *Opt. Express* **30**, 26787–26793 (2022).
97. [A. Onno](#), C. Reich, S. Li, A. Danielson, [W. Weigand](#), A. Bothwell, S. Grover, J. Bailey, G. Xiong, D. Kuciauskas, W. Sampath, and [Z. Holman](#), “Understanding what limits the voltage of polycrystalline CdSeTe solar cells,” *Nature Energy*, **7**, 400–408 (2022).
96. K. Chen, [B. Hartweg](#), M. Woodhouse, H. Guthrey, W. Nemeth, S. Theingi, M. Page, [Z. Holman](#), P. Stradins, S. Agarwal, and D. Young, “Self-aligned selective area front contacts on poly-Si/SiO_x passivating contact c-Si solar cells,” *IEEE J. Photovoltaics* **12**, 678–689 (2022).
95. N. Liew, [Z. Yu](#), [Z. Holman](#), and H.-J. Lee, “Parametric study about performances of a solar photovoltaic/thermal hybrid using a spectral beam splitting technique,” *J. Renew. Sustain. Energy* **14**, 013701 (2022).
94. [J. Ding](#), [C. Campbell](#), [J. Becker](#), [C.-Y. Tsai](#), [S. Schaefer](#), [T. McCarthy](#), [M. Boccard](#), [Z. Holman](#), and Y.-H. Zhang, “Monocrystalline 1.7-eV MgCdTe solar cells,” *J. Appl. Phys.* **131**, 023107 (2022). [[Editor’s Pick](#)].
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PATENTS

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APPENDIX B

Appendix B: Materials Considered

No.	Description
1001	U.S. Patent No. 11,251,315 B2 (“USP315”)
1002	File History for U.S. Patent No. 11,251,315 B2 (App. No. 16/877,255) (“USP315FH”)
1006	U.S. Patent App. Pub. No. 2014/0311567 (“Choi”)
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Appendix B (Materials Considered)

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APPENDIX C

Appendix C: Challenged Claims

Claim 10	
Element	Claim Language
10[pre]	A solar cell, the solar cell having a front side which faces the sun during normal operation and a back side opposite the front side, the solar cell comprising:
10[a]	a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ and wherein the portion of the silicon substrate is formed at the front side of the solar cell;
10[b]	a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of the solar cell;
10[c]	a first emitter region having metal impurities formed over the dielectric region; and
10[d]	a first metal contact formed over the first emitter region.

Claim 11
The solar cell of claim 10, wherein the portion of the silicon substrate comprises N-type dopants.

Claim 12
The solar cell of claim 10, wherein the portion of the silicon substrate comprises phosphorus.

Claim 13
The solar cell of claim 10, wherein the portion of the silicon substrate comprises P-type dopants.

Claim 14

The solar cell of claim 10, wherein the portion of the silicon substrate comprises boron.

Claim 15

The solar cell of claim 10, wherein the first emitter region comprises polysilicon.

Claim 16

Element	Claim Language
16[pre]	The solar cell of claim 10, further comprising:
16[a]	a second emitter region having metal impurities formed over the dielectric region; and
16[b]	a second metal contact formed over the second emitter region.

Claim 17

The solar cell of claim 16, wherein the second emitter region is separate from the first emitter region.

Claim 18

The solar cell of claim 16, wherein a trench region separates the first emitter region from the second emitter region.

Claim 19
The solar cell of claim 16, wherein the second emitter region comprises polysilicon.

Claim 20
The solar cell of claim 16, wherein the first emitter region comprises a P-type doped polysilicon region and the second emitter region comprises a N-type doped polysilicon region.