

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HANWHA SOLUTIONS CORPORATION,

Petitioner,

v.

MAXEON SOLAR PTE. LTD.,

Patent Owner.

Case No. IPR2024-01198

U.S. Patent No. 11,251,315

**PETITION FOR *INTER PARTES* REVIEW
OF CLAIMS 10-20 OF
U.S. PATENT NO. 11,251,315
UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104**

Table of Contents

I.	INTRODUCTION	1
II.	MANDATORY NOTICES	2
	A. Real Parties in Interest.....	2
	B. Related Matter	2
	C. Counsel	3
	D. Service Information	4
III.	CERTIFICATION OF GROUNDS FOR STANDING	4
IV.	OVERVIEW OF CHALLENGE AND RELIEF REQUESTED	5
	A. Prior Art.....	5
	B. Grounds for Challenge	7
V.	TECHNOLOGY BACKGROUND.....	7
	A. Solar Cells	7
	B. Solar Cell Efficiency	14
	1. Recombination	14
	2. Methods of Reducing Recombination	16
VI.	THE '315 PATENT	18
	A. Brief Description	18
	B. Prosecution History	22
VII.	PERSON OF ORDINARY SKILL IN THE ART	23
VIII.	CLAIM CONSTRUCTION	24
IX.	OVERVIEW OF THE ASSERTED PRIOR ART	25
	A. Choi	25
	B. Cousins	27
	C. Granek	28
	D. Marvin	31

E.	Istratov	32
F.	Smith.....	33
X.	SPECIFIC GROUNDS FOR UNPATENTABILITY	35
A.	Ground I: Claims 10-17 and 19-20 Are Invalid as Obvious Over Choi, Granek or Marvin, and Istratov.	35
1.	Motivation to Combine and Reasonable Expectation of Success.....	35
2.	Claim 10.....	47
3.	Claim 11	56
4.	Claim 12.....	56
5.	Claim 13	57
6.	Claim 14.....	57
7.	Claim 15	58
8.	Claim 16.....	58
9.	Claim 17	60
10.	Claim 19.....	61
11.	Claim 20	61
B.	Ground II: Claim 18 Is Invalid as Obvious Over Choi, Granek or Marvin, Istratov, and Smith.....	62
1.	Motivation to Combine and Reasonable Expectation of Success.....	62
2.	Claim 18	66
C.	Ground III: Claims 10-15 Are Invalid as Obvious Over Cousins, Granek or Marvin, and Istratov.	67
1.	Motivation to Combine and Reasonable Expectation of Success.....	67
2.	Claim 10.....	72
3.	Claim 11	76
4.	Claim 12.....	76
5.	Claim 13	76
6.	Claim 14.....	77

7.	Claim 15	78
XI.	DISCRETIONARY DENIAL IS NOT WARRANTED.....	79
A.	<i>General Plastic</i>	79
B.	35 U.S.C. § 325(d).....	83
C.	<i>Fintiv</i>	84
XII.	CONCLUSION.....	85

I. INTRODUCTION

U.S. Patent No. 11,251,315 (“’315 patent”) claims a combination of solar cell features well known in the prior art. Challenged claims 10-20 recite a solar cell having a silicon substrate with a portion having a specific dopant concentration on the front side, and an emitter having metal impurities on the back side of the cell. These conventional features would have been easily combined within a solar cell before the ’315 patent.

By the earliest alleged priority date, it was well known that doping a portion near the cell surface with a higher dopant concentration than the rest of the substrate would decrease undesirable carrier recombination. Similarly, it was well known that detrimental levels of metal impurities in the substrate cause undesirable recombination and that gettering the impurities into a polysilicon emitter reduces such recombination. Solar cells using doped portions and gettering of metal impurities into polysilicon emitters were known to increase efficiency.

As explained below, claims 10-20 recite these common solar cell features, combined in a conventional way to achieve predictable results. The claims recite nothing inventive and should be canceled.

II. MANDATORY NOTICES

A. Real Parties in Interest

Pursuant to 37 C.F.R. §42.8(b)(1), Petitioner certifies that Hanwha Solutions Corporation is the real party-in-interest.

B. Related Matter

Pursuant to 37 C.F.R. §42.8(b)(2), Petitioner discloses that Patent Owner has asserted U.S. Patent Nos. 8,222,516 (“’516 patent”), 8,878,053 (“’053 patent”), and 11,251,315 (“’315 patent”) against Petitioner in *Maxeon Solar Pte. Ltd. v. Hanwha Solutions Corporation and Hanwha Energy Corporation*, No. 2:24-cv-00262 (E.D. Tex.). Ex.1005-Complaint.

Patent Owner has also asserted these patents in the following proceedings:

- *Maxeon Solar Pte. Ltd. v. Canadian Solar Inc.*, No. 2:24-cv-00210 (E.D. Tex.); and
- *Maxeon Solar Pte. Ltd. v. REC Solar Holdings AS*, No. 2:24-cv-00260 (E.D. Tex.).

On June 24, June 25, and July 19, 2024, Canadian Solar Incorporated (“CSI”) filed *inter partes* review (“IPR”) petitions challenging a subset of claims of the ’516, ’053, and ’315 patents:

Challenged Patent	Challenged Claims	Case No.
8,222,516	9-12	IPR2024-01039
8,878,053	9-20	IPR2024-01040
11,251,315	10-15 16, 19	IPR2024-01038 IPR2024-01194

Petitioner is concurrently filing IPR petitions challenging all claims of the '516 and '053 patents:

Challenged Patent	Challenged Claims	Case No.
8,222,516	1-12	IPR2024-01203
8,878,053	1-20	IPR2024-01199

C. Counsel

Lead Counsel: David Cavanaugh (Reg. No. 36,476)

Backup Counsel: Mark Selwyn (*pro hac vice* to be filed)

John Hobgood (Reg. No. 61,540)

Jorge Kina (Reg. No. 74,241)

Abigail Lubow (Reg. No. 75,839)

Robert Stiller (Reg. No. 76,751)

Nora Xu (Reg. No. 79,739)

Alexander J. Nemtzow (Reg. No. 82,130)

Gilbert Smolenski (Reg. No. 78,549)

D. Service Information

Email: David.Cavanaugh@wilmerhale.com

Mark.Selwyn@wilmerhale.com

John.Hobgood@wilmerhale.com

Jorge.Kina@wilmerhale.com

Abigail.Lubow@wilmerhale.com

Robert.Stiller@wilmerhale.com

Nora.Xu@wilmerhale.com

Alex.Nemtsov@wilmerhale.com

Gilbert.Smolenski@wilmerhale.com

WHMaxeonIPRService@wilmerhale.com

Post & Hand Delivery: Wilmer Cutler Pickering Hale and Dorr LLP

2100 Pennsylvania Avenue NW

Washington, DC 20037

Tel: (202) 663-6000, Facsimile: (202) 663-6363

Petitioner agrees to accept service by email.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies that the '315 patent is available for IPR, and Petitioner is

not barred or estopped from requesting IPR on the grounds identified herein.

IV. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

Petitioner requests cancellation of claims 10-20 (“Challenged Claims”).

A. Prior Art

The ’315 patent was filed on May 18, 2020, and claims priority to U.S. Pat. App. No. 14/579,935, filed on December 22, 2014. Ex.1001-USP315, Cover. Petitioner relies on the following prior art:¹

1. U.S. Patent Publication No. 2014/0311567 (“Choi,” Ex.1006-Choi), published October 23, 2014, and filed on April 22, 2014, is prior art under at least 35 U.S.C. §§102(a)(1),102(a)(2). Choi claims priority to KR10-2013-0044982 filed on April 23, 2013, a translation of which is provided as Ex.1065-982. Because the disclosure of Choi and KR10-2013-0044982 is substantively identical, Choi can claim priority to April 23, 2013. Because KR10-2013-0044982 was filed more than a year before the earliest alleged priority date of the ’315 patent of December 22, 2014, Patent Owner cannot exclude Choi as prior art under any 35 U.S.C. §102(b) exception. Petitioner reserves the right to respond should Patent Owner argue that an exception applies.

¹ The America Invents Act (“AIA”) statutory framework applies.

2. U.S. Patent No. 8,207,444 (“Cousins,” Ex.1007-Cousins), published June 26, 2012, is prior art under at least §102(a)(1).

3. “High-Efficiency Back-Contact Back-Junction Silicon Solar Cells” (“Granek,” Ex.1010-Granek), published July 31, 2009, is prior art under at least §102(a)(1). Granek was publicly available over one year before December 2014. Ex.1004-Munford-Decl. ¶¶16, 38-56.

4. “Interdigitated Back Contact Solar Cell Analysis and Design Recommendations for Space Use” (“Marvin,” Ex.1008-Marvin), published April 11, 1990, is prior art under at least §102(a)(1). As the Declaration of June Munford (“Munford Declaration,” Ex.1004-Munford-Decl.) explains, Marvin was publicly available over one year before December 2014. Ex.1004-Munford-Decl. ¶¶16, 24-37; *Telefonaktiebolaget LM Ericsson v. TCL Corp.*, 941 F.3d 1341, 1346-47 (Fed. Cir. 2019).

5. U.S. 2013/0240029 (“Smith,” Ex.1011-Smith), published September 19, 2013, is prior art under at least §102(a)(1).

6. “Gettering in silicon-on-insulator wafers: experimental studies and modelling” (“Istratov,” Ex.1012-Istratov), published April 15, 2005, is prior art under at least §102(a)(1). Istratov was publicly available over one year before December 2014. Ex.1004-Munford-Decl. ¶¶16, 18-23.

B. Grounds for Challenge

Petitioner requests cancellation of the Challenged Claims as unpatentable under 35 U.S.C. §103. The grounds are:

Ground	35 U.S.C. §	Claims	Reference(s)
I	103	10-17, 19-20	Choi in view of Granek or Marvin in further view of Istratov
II	103	18	Choi in view of Granek or Marvin in further view of Istratov in further view of Smith
III	103	10-15	Cousins in view of Granek or Marvin in further view of Istratov

This Petition, supported by the declaration of Dr. Zachary Holman (“Holman Declaration,” Ex.1003-Decl.), demonstrates a reasonable likelihood that Petitioner will prevail with respect to at least one challenged claim. 35 U.S.C. §314(a). Petitioner respectfully requests institution.

V. TECHNOLOGY BACKGROUND

A. Solar Cells

A solar cell converts solar radiation (sunlight) into electricity. An individual cell, when exposed to sunlight, generates a flow of electricity for external circuits. To generate usable amounts of energy, multiple cells are connected—forming a solar module:



Ex.1054-BP-MSX-120, 1. Ex.1003-Decl., ¶42.

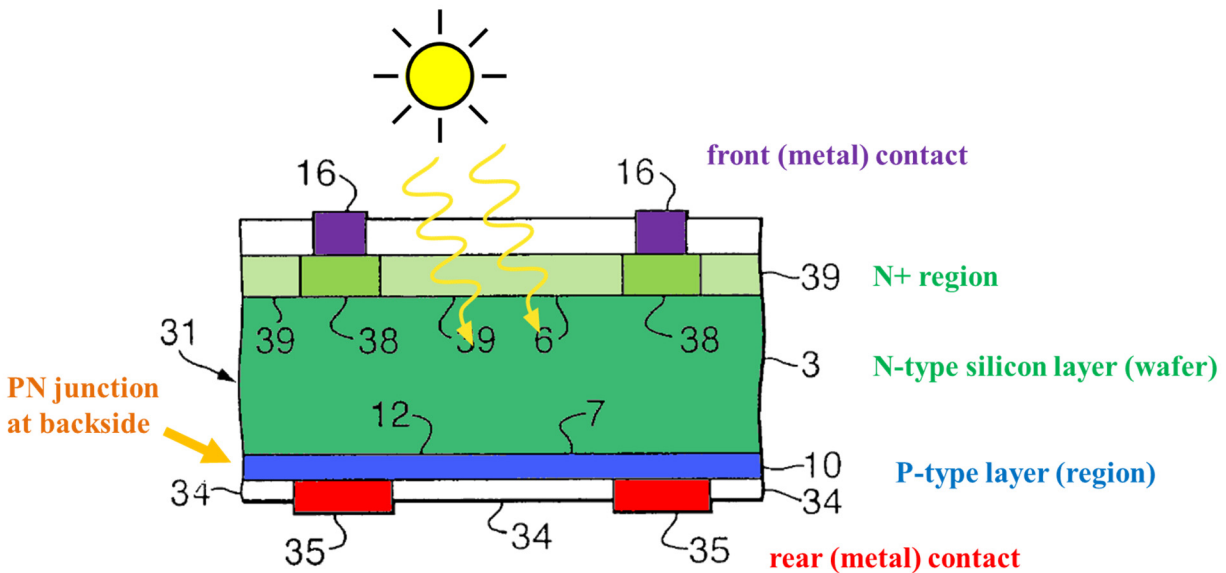
Persons of ordinary skill in the art (“POSITAs”) have studied the structure and manufacture of solar cells for decades. A cell typically has multiple silicon layers. Two variants of silicon are commonly used: (i) silicon, which has a monocrystalline lattice; and (ii) polysilicon, which has multiple crystalline regions that are not aligned with each other. Amorphous silicon, which has a non-crystalline lattice, is sometimes utilized. Ex.1003-Decl., ¶43.

In a standard solar cell, a chemical element, typically boron or phosphorus, is introduced in a process is known as “doping.” Techniques for doping silicon and polysilicon layers were well-established by 2014. A common doping technique involved forming a glass layer with dopants over a silicon or polysilicon layer and

then subjecting the combined materials to high temperatures to drive dopants from the glass into the silicon or polysilicon. Boron was commonly used to create “p-type” layers, and phosphorus was commonly used to create “n-type” layers. Ex.1003-Decl., ¶¶44-55.

For a solar cell to create energy, an interface between the n-type and p-type layers must be formed, which was commonly known as the “PN” junction. When solar radiation reaches a cell, the solar energy causes the release of an electron-hole pair in the cell. Specifically, photons cause electrons to leave their bonds, leaving a positively charged “hole.” The separated electrons and holes are mobile and move through the solar cell. The electrons and holes migrate to their respective electrodes, either positive or negative, creating a voltage differential between the n-type and p-type layers and generating the current flow. The PN junction facilitates this movement. Ex.1003-Decl., ¶¶56-62.

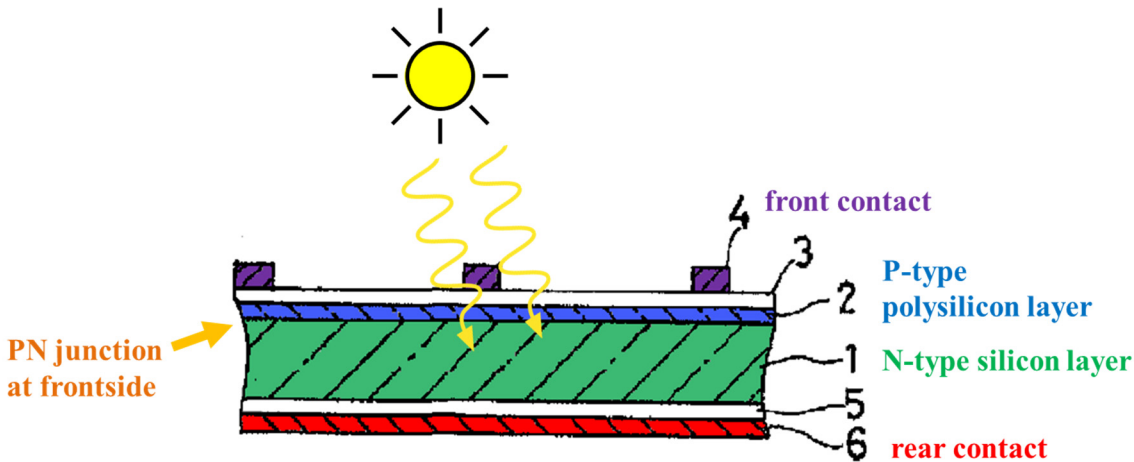
An exemplary solar cell is below. It includes an **n-type silicon layer**, known as the “substrate.” It also includes a **p-type layer** on the **silicon layer’s** back side. The PN junction exists at the interface of the n-type and p-type layers, and the layer that is oppositely doped from the substrate is known as the “emitter.”



Ex.1013-Froitzheim, Fig.3.² Ex.1003-Decl., ¶58.

It was well known that the PN junction could be located at the cell’s “front side” or “back side.” In a backside configuration (above), the **substrate** is closer to the sun such that the PN junction is formed on the **substrate’s** backside. Ex.1003-Decl., ¶¶58-59. In a frontside configuration (below), the **emitter** (p-type) would be closer to the sun such that the PN junction is formed on the **substrate’s** (n-type) frontside.

² All annotations and emphasis added unless otherwise noted.

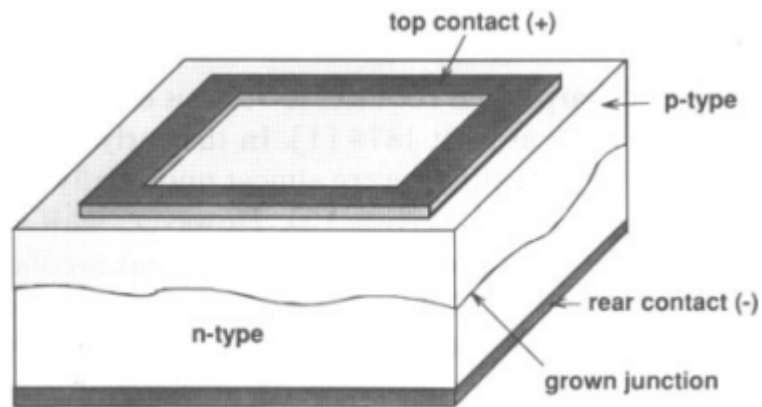


Ex.1014-Okayasu, Fig.1. The manufacturing process (*i.e.*, layer creation and doping processes) for frontside or backside configurations was similar. Ex.1003-Decl., ¶¶59-62.

The solar cells of Froitzheim and Okayasu are called N-type cells, after their n-type substrates, while P-type cells have p-type substrates. N-type cells have P-type emitters, while P-type cells have N-type emitters. Ex.1003-Decl., ¶¶58-60.

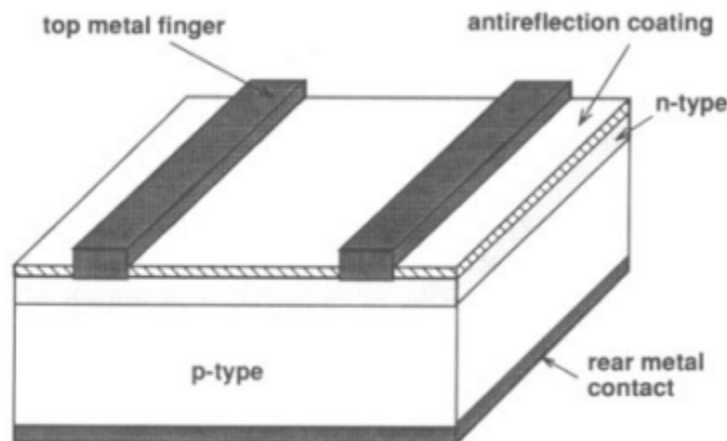
It was also well known that solar cells have metal contacts for connecting multiple solar cells together and to external circuits. For example, the solar cells shown above include at least one **front metal contact** and **rear metal contact**. Ex.1003-Decl., ¶¶44, 58-60.

Both-sides-contacted cells were known well before 2014. A 1941 photovoltaic device (below) had both top and rear contacts.



Ex.1046-Green, Fig.2. Ex.1003-Decl., ¶94.

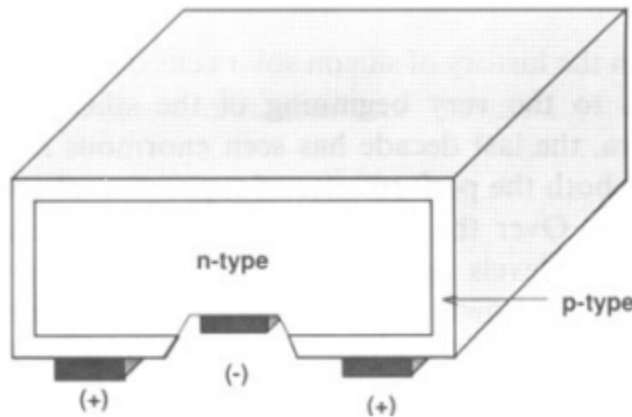
During the 1960s, solar cells developed for space applications positioned the metal contacts on both the top and bottom surfaces:



Ex.1046-Green, Fig.4. Ex.1003-Decl., ¶95.

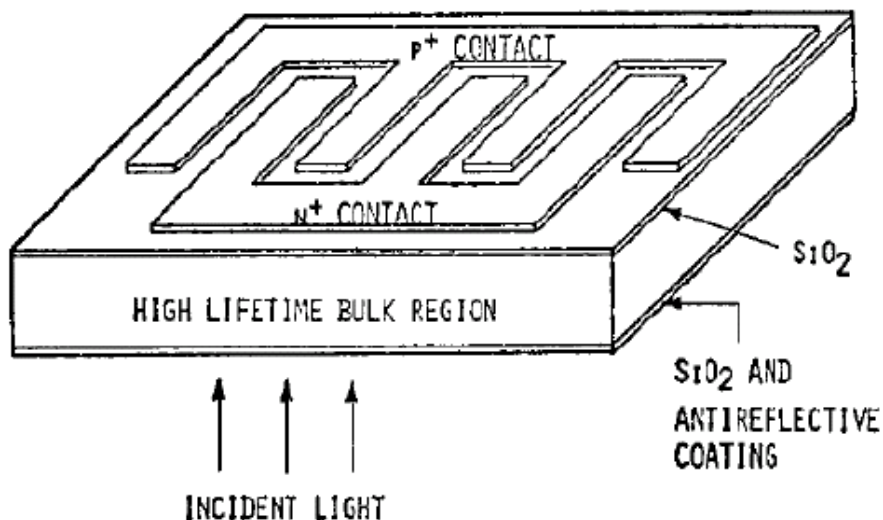
Back-contact cells were also known well before 2014. Ex.1051-Lammert, 337-338; Ex.1010-Granek, 18. In contrast to both-sides-contacted cells, back-contact cells position both metal contacts on only the back side, with the PN junction

on that side. Ex.1010-Granek, 17; Ex.1008-Marvin, 3. The figure below shows a cell from 1954—the “first modern [solar] cell”—featuring a “dual rear contact structure” with both contacts on the back:



Ex.1046-Green, Fig.3. Ex.1003-Decl., ¶¶99-101.

Interdigitated back-contact (“IBC”) cells, dating from as early as 1977, are a subset of back-contact cells, named after the interdigitated n and p contacts:



Ex.1051-Lammert, 337-338, Fig.1; Ex.1008-Marvin, 3-4. Ex.1003-Decl., ¶¶102-103.

B. Solar Cell Efficiency

Skilled artisans have worked for decades to improve solar cell efficiency. Solar cell efficiency, more precisely “power conversion efficiency,” measures the amount of electrical work done by electrical charge delivered to an external circuit per light-generated photon incident on the cell. Ex.1023-Nelson, 289. Because cells generate electricity through creation and movement of electron-hole pairs, it was well known that maximizing the number of electrons and holes exiting a cell via metal contacts improves efficiency. Ex.1003-Decl., ¶¶63-65.

1. Recombination

One known way to increase the number of electrons and holes exiting a cell is to prevent them from “recombining” before exiting. “Recombination” annihilates electrons and holes, preventing them from contributing to the output current and reducing efficiency. Ex.1024-Pierret, 105; *see* Ex.1023-Nelson, 99. A measure of recombination is saturation current, J_0 . Ex.1023-Nelson, 289. Ex.1003-Decl., ¶¶66-67.

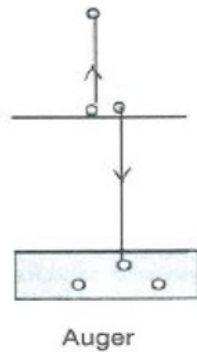
Long before 2014, it was well known that recombination would limit solar cell efficiency. It was also known that electrons and holes recombine in several

ways, including Shockley-Read-Hall (“SRH”) recombination and Auger recombination. Ex.1003-Decl., ¶¶66-72.

(1) **SRH recombination** is common in silicon semiconductors. Ex.1023-Nelson, 106-107. In substrates with metal impurities or lattice defects, SRH recombination involves: (1) trapping of an electron or hole in an energy level created by a defect, and (2) movement of an opposite-charged hole or electron to the defect energy level—resulting in recombination and the release of heat. *Id.*; Ex.1026-Hu, 48. Ex.1003-Decl. ¶70.

One form of SRH recombination is “surface recombination,” whereby electrons or holes recombine at surfaces or interfaces between materials. For example, broken bonds at the surface of the silicon substrate or its interface with many other materials (*e.g.*, metals) introduce defect states for recombination. Ex.1023-Nelson, 110; Ex.1010-Granek, 117-118. Ex.1003-Decl., ¶71.

(2) **Auger recombination** occurs when two electrons (or two holes) collide, exciting one electron (or hole) to a higher energy level. The other electron (or hole) recombines with a hole (or electron), releasing energy as heat. Ex.1023-Nelson, 105; Ex.1024-Pierret, 107. Auger recombination is common at high dopant levels, which make it more likely that electron-hole pairs can transfer their energy to an available carrier. Ex.1023-Nelson, 105; Ex.1026-Hu, 48.



Ex.1023-Nelson, 100, Fig.4.7; *see* Ex.1025-Fonash, 37-38. Ex.1003-Decl., ¶72.

2. Methods of Reducing Recombination

i. Surface Passivation

It was well known by the earliest alleged priority date that surface passivation techniques could be used to reduce recombination. Ex.1010-Granek, 117-119. One such technique involves doping a front region of the substrate to reduce the concentration of one carrier type. *Id.* Without both carrier types present, recombination decreases. *Id.* In a back-side-contacted cell, this doped front portion is called a front surface field (“FSF”), but the same concept applies to other solar cell structures. Ex.1003-Decl., ¶¶73-75.

By 1978, FSFs were a well-known way to reduce recombination near the cell surface. Ex.1027-von Roos, 1119-1120; Ex.1008-Marvin, 3. An FSF is the result of doping a region near the substrate’s surface to a level above the substrate’s background dopant concentration. Ex.1027-von Roos, 1119-1120. The increased doping creates an electric field between the more heavily doped region and the rest

of the substrate, forming an energetic barrier preventing electrons and holes from moving toward the recombination-active front surface of the wafer. *Id.*, 1119. The FSF thus helps move charge carriers to the appropriate contacts, generating current. *Id.* Ex.1003-Decl., ¶¶76-78.

Well before 2014, it was well known that Auger recombination limited FSF dopant concentrations; FSF dopant concentrations above $1 \times 10^{18} \text{ cm}^{-3}$ induced Auger recombination, reducing efficiency. Ex.1008-Marvin, 15; Ex.1021-King, 365-368; Ex.1030-Swanson-352, 4:38-51; Ex.1040-Procel, 1. Ex.1003-Decl., ¶¶79-82.

ii. Gettering

By the 1960s, it was known that gettering was used in silicon-based semiconductor fabrication processes to reduce deleterious effects of metal impurities. Ex.1060-Goetzberger, 1822-1824; Ex.1061-Ing, 533-534; Ex.1062-Mets, 422-424. It was known that wafer manufacturing and device fabrication could introduce metal impurities into the devices. Ex.1047-Istratov-2000, 491-493. Gettering of solar cells was well known by 2014. Ex.1031-Bultman, 72-73; Ex.1033-Perichaud, 315-318; Ex.1035-Gupta, [0037]. Ex.1003-Decl., ¶¶83-93.

Gettering decreases unwanted electron-hole recombination in semiconductor devices such as solar cells. Ex.1033-Perichaud, 316-318. Gettering involves heating the cell to a high temperature to release metal impurities, which diffuse through the

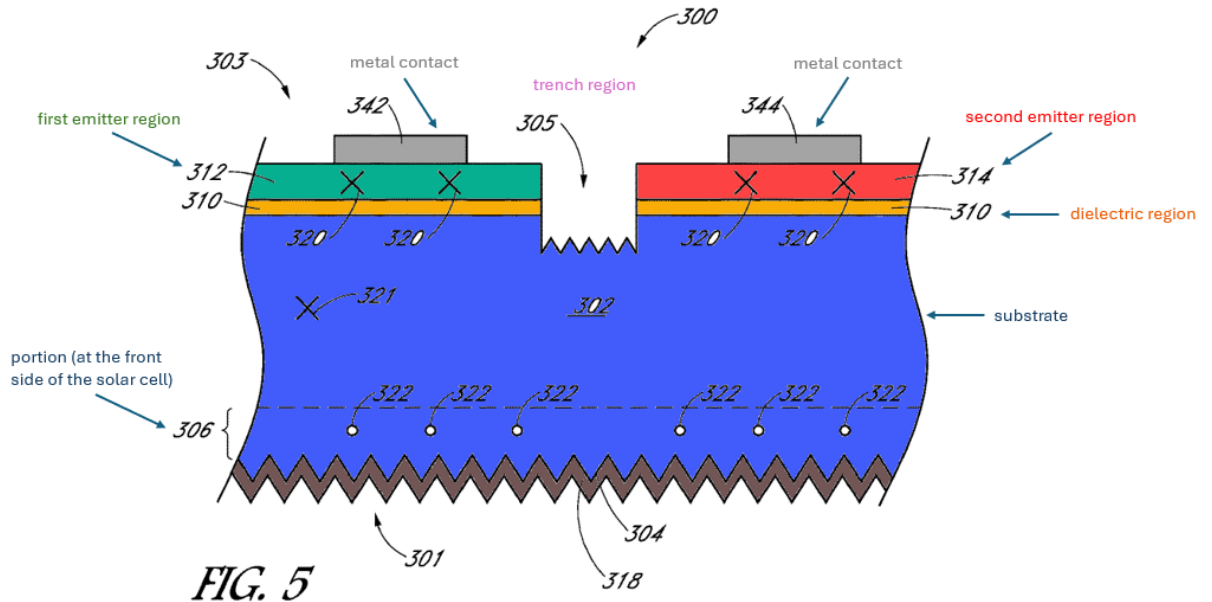
semiconductor toward a front or back surface where they are captured at a gettering trap site. *Id.* Highly defective materials, such as polysilicon, have many trap sites, acting as a sponge for impurities. Ex.1053-Nippon, 11-12, 16; Ex.1062-Mets, 422-424; Ex.1052-Lysacek, 1-2. In solar cells with significant metal impurity levels in the wafer, gettering was performed well before 2014 to move metal impurities from the substrate into the emitter, where they cause less recombination. Ex.1033-Perichaud, 315-318; Ex.1035-Gupta, [0037]; Ex.1031-Bultman, 72. Ex.1003-Decl., ¶¶83-93.

VI. THE '315 PATENT

A. Brief Description

The '315 patent claims two concepts that purportedly improve solar cell efficiency. First, to reduce recombination near the surface, the patent describes creating a front side, doped portion with a higher dopant concentration than the background dopant concentration of the substrate. Ex.1001-USP315, 4:55-64; *see supra* §V.B.2.i. Second, to reduce recombination caused by metal impurities in the substrate, the patent describes gettering to migrate the impurities from the substrate to the emitter, where they do not cause, or cause less, recombination. Ex.1001-USP315, 5:1-18; *see supra* §V.B.2.ii.

Figure 5, annotated below, illustrates elements from claims 10-20. Figure 5 shows a solar cell (300) having a front side (301) facing the sun and a back side (303). Ex.1001-USP315, 6:40-49, Fig.5. The solar cell (300) has a silicon substrate (302). *Id.* The silicon substrate (302) has a portion (306) at the front side of the solar cell with a dopant concentration (322) of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$. *Id.* Figure 5 also shows a dielectric region (310) formed over the silicon substrate, first and second emitter regions (312, 314) formed over the dielectric region, and metal contacts (342, 344) formed over the first and second emitter regions. *Id.*, 6:50-62. The first and second emitter regions (312, 314) can be doped either p-type and n-type or vice versa. *Id.* In the embodiment of Figure 5, the silicon substrate and second emitter region are n-type, and the first emitter region is p-type. *Id.*, 6:40-57. Finally, a trench region (305) separates the first and second emitter regions (312, 314). *Id.*, 6:65-67.



Ex.1001-USP315, Fig.5. Ex.1003-Decl., ¶¶106-109.

The '315 patent purports to improve efficiency by, first, doping a portion near the surface of the cell at approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ and, second, gettering the metal impurities into the emitter at a temperature above 900°C . Ex.1001-USP315, 8:40-45. The specification describes a series of experiments—Example Processes A, B, C, and D—with two variables: temperature and dopant concentration. *Id.*, 8:35-50, Fig.11. These processing parameters and “output results” (e.g., “Gettering Location,” “Efficiency”) are summarized in Figure 11:

Example Process	Temp	Surface Dopant Conc.	Gettering Location	Surface Passivation	Lifetime	Efficiency
A	≤ 900 deg-C	$2 \times 10^{18} \text{ cm}^{-3}$	non-poly	2 fA/cm^2	$\sim 3 \text{ msec}$	Baseline
B	≤ 900 deg-C	$4 \times 10^{18} \text{ cm}^{-3}$	non-poly	5 fA/cm^2	$\sim 10 \text{ msec}$	Baseline
C	≤ 900 deg-C	$2 \times 10^{18} \text{ cm}^{-3}$	poly	2 fA/cm^2	$\sim 10 \text{ msec}$	+0.5 % abs.
D	≤ 900 deg-C	$4 \times 10^{18} \text{ cm}^{-3}$	poly	5 fA/cm^2	$\sim 10 \text{ msec}$	Baseline

Table 1. Example Processes for Solar Cell Fabrication

FIG. 11

Id., Fig.11.³ Ex.1003-Decl., ¶¶110-111.

In Processes A and B, the cells were heated to a temperature of less than or equal to 900°C, failing to drive impurities into the polysilicon emitter (indicated by “non-poly” in “Gettering Location” column). Ex.1001-USP315, 8:51-9:13, Fig.11. Thus, purported efficiency improvements achieved by gettering were not realized. *See id.*; *supra* §V.B.2.ii. Conversely, in Processes C and D, the cells were heated to

³ Figure 11 appears to contain typographical errors. Though the second column (“Temp”) shows Processes C and D occurring at less than or equal to 900°C, the specification states Processes C and D involved “a temperature *above* 900 degrees Celsius.” Ex.1001-USP315, 8:40-45, 9:1-9. Fig.11. Ex.1003-Decl., ¶111 n.5.

above 900°C, and gettering into the polysilicon emitter was purportedly successful (indicated by “poly” in the “Gettering Location” column). Ex.1001-USP315, 8:51-9:13, Fig.11. Ex.1003-Decl., ¶¶112-113.

Processes A, B, C, D also varied the dopant concentration, using either “approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ ” or “approximately $4 \times 10^{18} \text{ cm}^{-3}$.” Ex.1001-USP315, 8:40-9:13, Fig.11. Processes B and D, using a concentration of “approximately $4 \times 10^{18} \text{ cm}^{-3}$,” yielded “no considerable” efficiency improvement. *Id.* Process C, which heated the cell to above 900°C and doped “a portion near the surface, of a silicon substate ... at approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$,” realized the highest efficiency increase. *Id.*, 8:40-50, Fig.11. Ex.1003-Decl., ¶¶114-116.

B. Prosecution History

The '315 patent issued from U.S. 16/877,255 (“’255 Application”), filed on May 18, 2020. The '255 Application is a continuation of U.S. 16/228,165, a division of U.S. 15/876,927, which is further a continuation of 15/213,273, which is further a continuation of U.S. 14/579,935. The same Examiner reviewed all five applications. Ex.1003-Decl., ¶¶117-119.

The Examiner allowed the claims of the '255 Application without any rejection under 35 U.S.C. §§ 102 and/or 103. *See generally* Ex.1002-USP315FH.

In the Notice of Allowance, the Examiner stated he believed that “none of the prior art ... teach[es] ... claim 10.” Ex.1002-USP315FH, 207. However, as shown below, the prior art does disclose the Challenged Claims. Ex.1003-Decl., ¶¶120-121.

The Examiner did not consider Choi, Granek, Marvin, Istratov, or Smith during prosecution of the '255 Application or the four parent applications. During prosecution of the parent '935 Application, the Examiner's search history included Cousins, but the Examiner made no reference to the contents of Cousins during prosecution of the five applications. *See* Ex.1036-USPA935FH, 184-187. Ex.1003-Decl., ¶¶121-122.

VII. PERSON OF ORDINARY SKILL IN THE ART

A POSITA at the earliest alleged priority date (December 22, 2014) would have had (1) an advanced degree in electrical engineering, mechanical engineering, applied physics, chemistry, materials science, or a related discipline and (2) at least one year of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. Alternatively, a POSITA would have had (1) a bachelor's degree in one of the aforementioned disciplines and (2) at least two years of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. Less work experience may be

compensated for by a higher level of education, and vice versa. Ex.1003-Decl., ¶¶37-41.

VIII. CLAIM CONSTRUCTION

Claim construction is not necessary to resolve the issues presented in this Petition. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). But Petitioner reserves the right to propose or respond to claim constructions in the district court litigation and respond to any claim construction Patent Owner advances here or raised by the Board. Trial Practice Guide, §II.B.6. Petitioner does not waive any argument in this or any other proceeding that claim terms in the '315 patent are indefinite or otherwise invalid.

Regarding the “approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ ” limitation of claim 10, the Board need not construe the outer bounds because the prior art cited herein discloses embodiments within the scope of the claims under any reasonable construction. The specification’s description is consistent with the “plain and ordinary meaning” of “approximately”—*i.e.*, “reasonably close to” and “comes near.” *Bausch & Lomb Inc. v. Vitamin Health, Inc.*, 13-CV-6498T, 2015 WL 13574354, at *6 (W.D.N.Y. Jan. 15, 2015); *Bausch & Lomb Inc. v. SBH Holdings LLC*, C.A. No. 20-1463-GBW-CJB, 2024 WL 489355, at *5 (D. Del. Feb. 8, 2024). Ex.1003-Decl., ¶¶123-127.

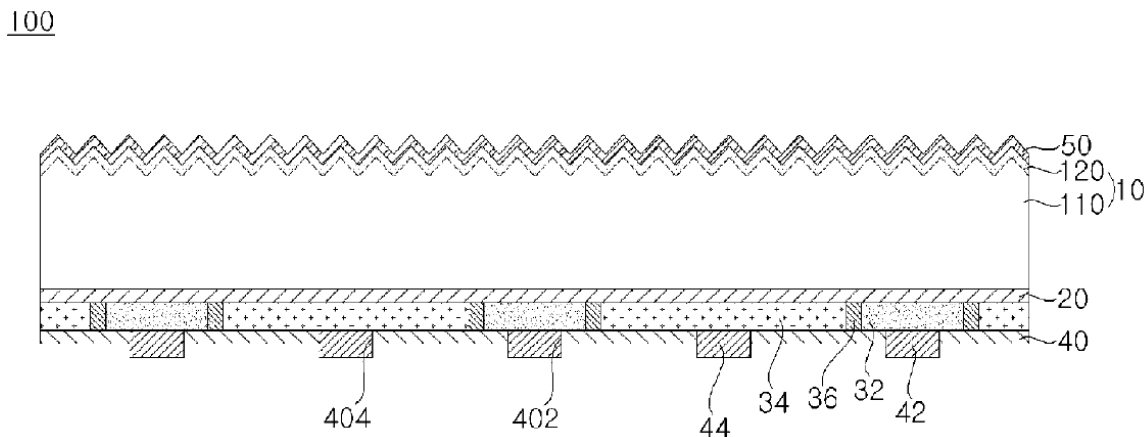
IX. OVERVIEW OF THE ASSERTED PRIOR ART

Choi, Cousins, Granek, Marvin, Istratov, and Smith disclose the limitations the Examiner believed were missing from the prior art.

A. Choi

Choi teaches a back-contact solar cell including the same layers recited in claim 10:

FIG. 1



Ex.1006-Choi, Fig.1. Ex.1003-Decl., ¶¶129-136.

Choi teaches a solar cell (100) comprising a semiconductor substrate (10) formed from “crystalline silicon” and “containing a first conductive-type dopant.” Ex.1006-Choi, [0023], [0025]. The “first conductive-type dopant” can be either “n-type” or “p-type.” *Id.*, [0025]. Ex.1003-Decl., ¶131.

At the front side, Choi teaches a “front surface field layer 120” “where the first conductive-type dopant is doped at a concentration higher than the

semiconductor substrate 10.” Ex.1006-Choi, [0029]. “[T]he front surface field layer 120 prevents electrons and holes separated by incident light from being recombined and then decay on the front surface of the semiconductor substrate 10.” *Id.* Ex.1003-Decl., ¶132.

Choi teaches “a tunneling layer 20” that “may be entirely formed on the back surface of the semiconductor substrate 10” and “may include” “oxides” which is a “material[] enabling tunneling of carriers.” Ex.1006-Choi, [0033]. Ex.1003-Decl., ¶133.

Choi further teaches first and second conductive type areas 32, 34 “formed on the tunneling layer 20.” Ex.1006-Choi, [0023], [0035]. Choi explains that “[t]he second conductive type area 34 may include a semiconductor (for example, silicon) having a conductive type opposite to the semiconductor substrate 10,” such that it “forms a tunnel junction with the semiconductor substrate 10 through the tunneling layer 20.” *Id.*, [0037]. Moreover, Choi teaches that “[t]he first conductive type area 32 may include a semiconductor (for example, silicon) having the same conductive type as the semiconductor substrate 10” and “forms a back surface field structure and thereby functions to prevent carrier loss through recombination on the surface of the semiconductor substrate 10.” *Id.*, [0036]. Ex.1003-Decl., ¶¶134-135.

Choi also teaches “first and second electrodes 42 and 44 which are connected to first and second conductive type areas 32 and 34, respectively” and “collect produced carriers and transport the same to the outside.” Ex.1006-Choi, [0023], [0044]. Choi does not limit itself to a particular application (*e.g.*, space or terrestrial environments). Ex.1003-Decl., ¶¶136, 202.

B. Cousins

Cousins teaches a bipolar, both-sides-contacted solar cell and includes the same layers recited in independent claim 10:

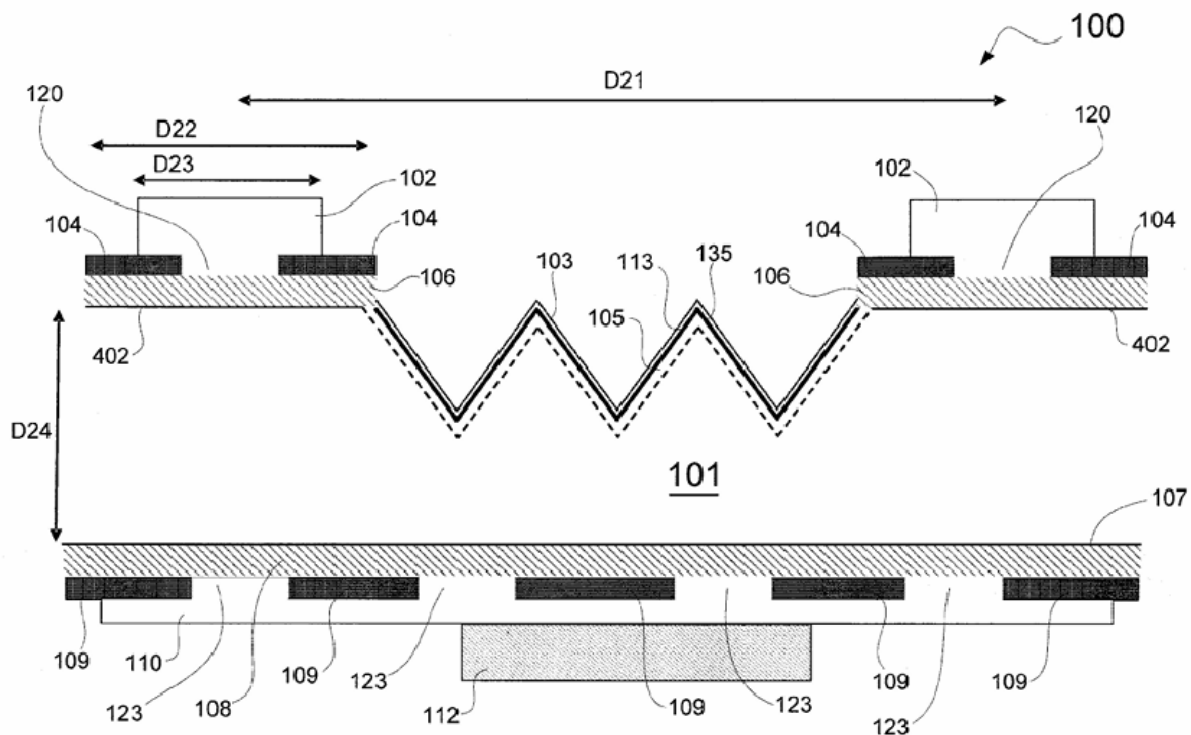


FIG. 1

Ex.1007-Cousins, Fig.1. Ex.1003-Decl., ¶¶137-142.

Cousins teaches a solar cell (100) having a substrate (101) that may be an “N-type silicon substrate.” Ex.1007-Cousins, 2:35-49. At the front side, Cousins teaches a “doped region 105” that “provides low front surface recombination and improves lateral conductivity.” *Id.*, 2:49-55. The doped region 105 may be an n-type doped region. *Id.* Ex.1003-Decl., ¶¶138-139.

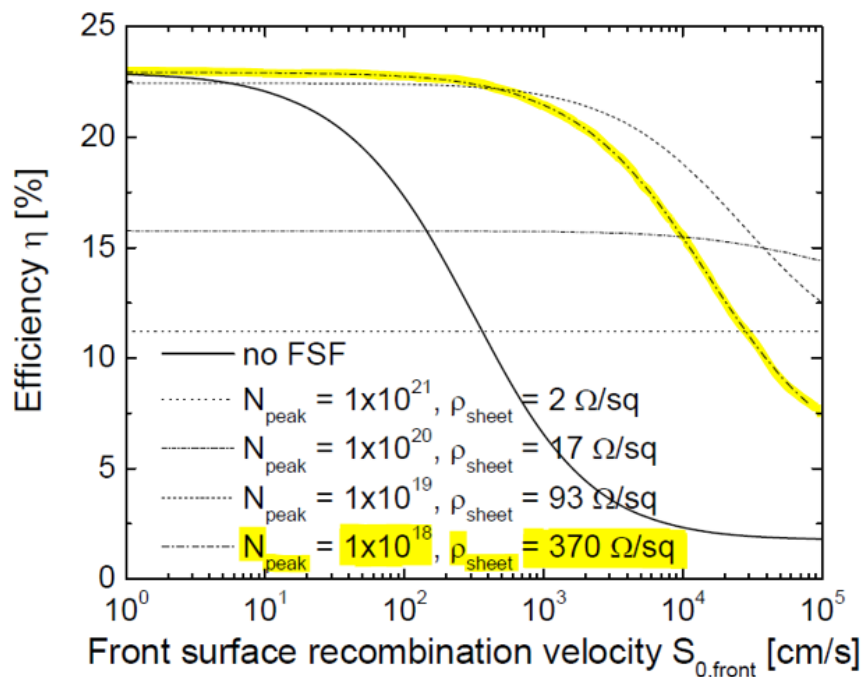
Cousins teaches a “thin dielectric layer 107” that “may comprise silicon dioxide ... on the back side surface of the substrate 101.” Ex.1007-Cousins, 3:12-21. A “polysilicon layer 108” is formed over the thin dielectric layer 107 and forms a back side junction with the substrate 101. *Id.*, 2:39-42, 3:12-13. The polysilicon layer 108 may have an “emitter saturation current of about $10 \text{ fA}\cdot\text{cm}^{-2}$.” *Id.*, 2:42-44. Finally, Cousins teaches a “metal contact 110” that “electrically connects to the polysilicon layer 108 through contact holes 123.” *Id.*, 3:19-24. Ex.1003-Decl., ¶¶140-142.

C. Granek

Granek analyzes the performance of solar cells having different FSF diffusion profiles. Ex.1010-Granek, 117. Granek teaches that a “lowly doped FSF results in high quantum efficiency” because “Auger recombination inside the highly doped region and the surface recombination velocity are low.” *Id.*, 120. Granek concludes that “[a] proper choice of the front surface field profile is therefore one of the most

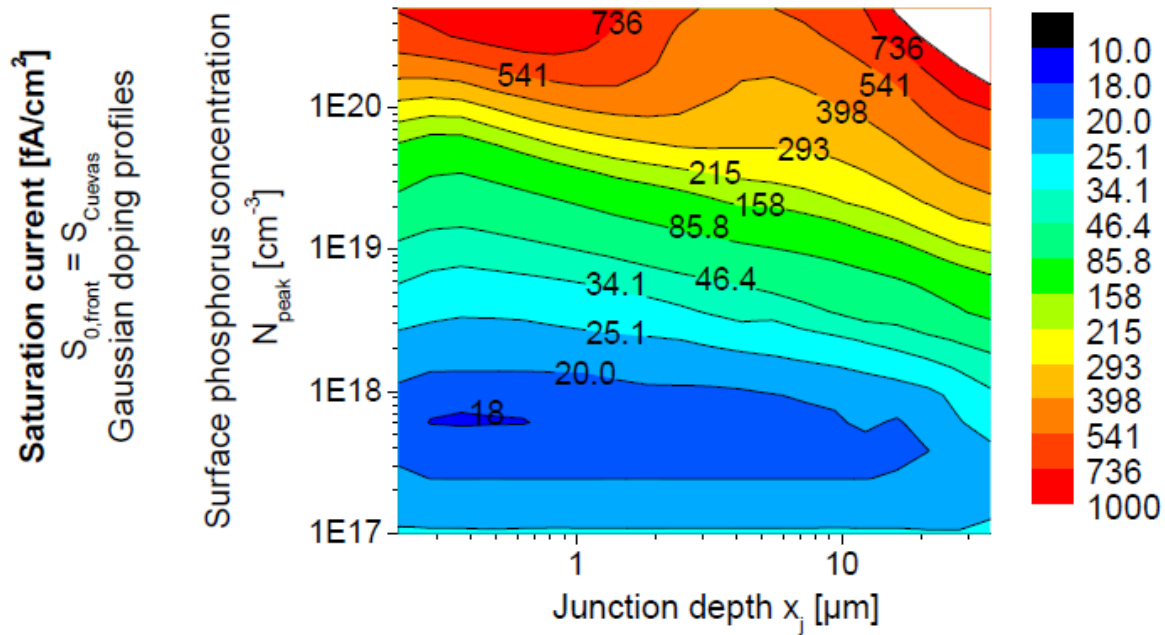
critical points in the design of the back-contact, back-junction solar cell device.” *Id.*
 Ex.1003-Dec1., ¶¶143-145.

Granek simulates cells with dopant concentrations ranging from 1×10^{18} to $1 \times 10^{21} \text{ cm}^{-3}$. Ex.1010-Granek, 120. As shown in Figure 7-1, the simulated solar cell’s efficiency is highest when the FSF dopant concentration is $1 \times 10^{18} \text{ cm}^{-3}$.



Id., 121, Fig.7-1 (annotated). Ex.1003-Dec1., ¶¶146-148.

Figure 7-3 (shown below) illustrates simulated “saturation current” density, as a function of junction depth (X-axis) and FSF dopant concentration (Y-axis). Saturation current density measures recombination in the cell. As shown, as the doping level decreases, saturation current decreases from higher (red-orange) values at $1 \text{E}20 \text{ cm}^{-3}$ to the lowest values (dark blue) at approximately $1 \text{E}18 \text{ cm}^{-3}$:



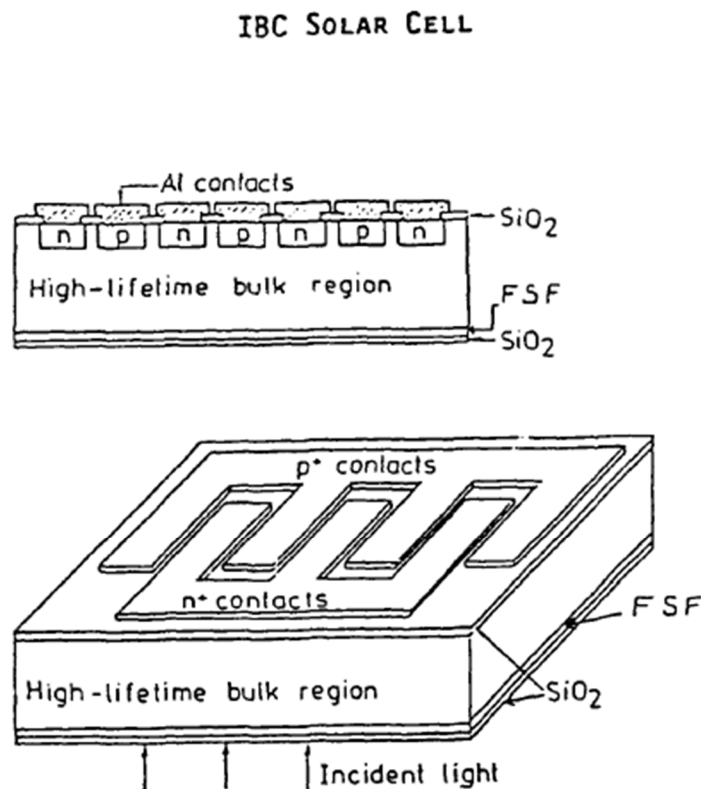
Ex.1010-Granek, Fig.7-3. Granek shows the simulated recombination level is lowest with an FSF dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ or lower.

Ex.1003-Decl., ¶¶149-150.

Granek also includes experimental results, using fabricated cells to study the effect of various FSF dopant concentrations on performance. Ex.1010-Granek, 124-126. Of the fabricated cells, the best-performing had the lowest FSF doping level, with a concentration of $3.8 \times 10^{18} \text{ cm}^{-3}$ —demonstrating that this value was preferable to higher values and that lower concentrations further improve performance. *Id.* Ex.1003-Decl., ¶¶151-153.

D. Marvin

Marvin “evaluate[s] the IBC cell design for use in space missions” and assesses “the effects of certain design parameters on cell performance” such as “front surface field (FSF) parameters.” Ex.1008-Marvin, 5, 9, 16. Like the ’315 patent, Marvin teaches an IBC silicon solar cell with a doped portion on the front side (a “front surface field”) and p- and n-type doped regions on the back side, with metal contacts formed over the back-side doped regions:



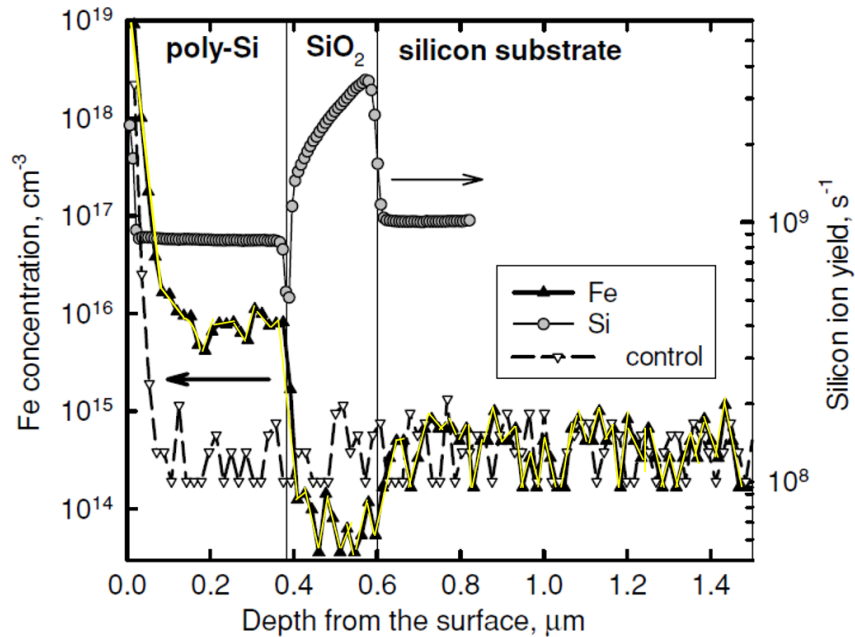
Id., 4 (Fig.1). Ex.1003-Decl., ¶¶154-156.

Marvin explains the FSF “provide[s] an electric field that repels one carrier type away from the front surface,” thereby “reduc[ing] the surface recombination velocity.” Ex.1008-Marvin, 15. “The FSF effectiveness is relatively constant over a rather broad range around $1\text{E}17$ to $1\text{E}18\text{ cm}^{-3}$, decreasing below this level due to the weakness of the electric field and decreasing above this level due to increased Auger recombination.” *Id.* Ex.1003-Decl., ¶¶155-160.

E. Istratov

Istratov tested a structure consisting of an oxide layer (“SiO₂”) grown on a silicon substrate covered by polysilicon (“poly-Si”). Ex.1012-Istratov, 569-570. Istratov performed experiments with iron and copper contamination, followed by annealing “for 8 h[ours] at 1020 °C” for the iron experiment and “at 690 °C for 5 h[ours]” or “at 1150 °C for 2 h[ours]” for the copper experiments. *Id.*, 570-571. Ex.1003-Decl., ¶¶161-168.

Figure 2 shows the depth profile of iron concentration after heating and diffusion of iron (“Fe”) within the test structure:



Ex.1012-Istratov, 570, Fig.2. Istratov concludes “from Figure 2 that the solubility of iron in poly-silicon ... is more than an order of magnitude higher than in the silicon substrate,” interpreted as “segregation gettering of iron by poly-silicon.” *Id.*, 570. From the copper experiments, Istratov similarly found that the concentration of copper was higher in the poly-silicon layer than in silicon substrate. *Id.*, 571, Figs.4-5. Ex.1003-Decl., ¶¶161-168.

F. Smith

Smith teaches a backside-contact solar cell with polysilicon doped regions (101, 102) on a dielectric layer (113) on the backside (106) of a solar cell. Ex.1011-Smith, [0016]-[0024]. “[I]nterdigitated metal contact fingers 108 and 109 ... make an electrical connection to the doped regions 101 and 102.” *Id.*, [0024].

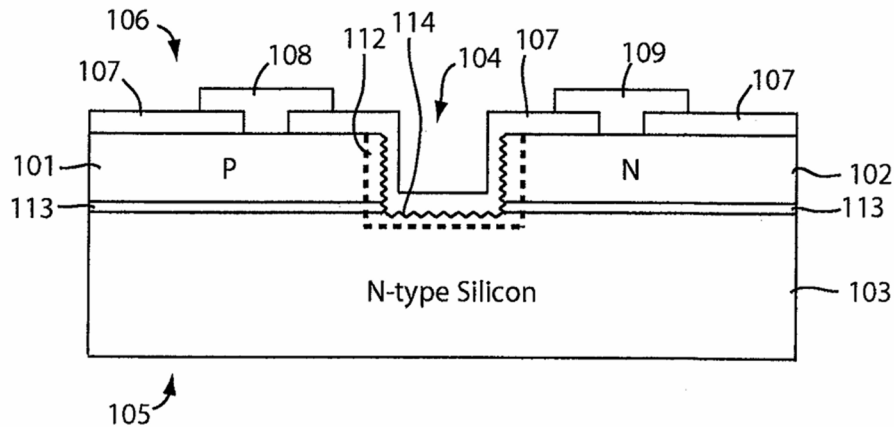


FIG. 2

Id., Fig.2. Smith explains that “touching polysilicon doped regions adversely affect efficiency.” *Id.*, [0015]. Specifically, “recombination in the space charge region where the polysilicon doped regions touch is very high due to the lifetime of charge carriers in the polysilicon being very low.” *Id.* Smith teaches a “trench 104, which serves as a gap between the doped regions,” and which “addresses the aforementioned issues” in “several ways,” *id.*, [0019], [0025]. First, “the trench 104 separates the doped regions 101 and 102 so they are not physically in contact,” which “prevents the space charge region from existing in either polysilicon film.” *Id.* Second, “the resulting accumulation layer under the trench 104 repels minority carriers to improve surface passivation.” *Id.* Finally, “the textured surface 114 in the trench 104 increases solar radiation collection,” all of which Smith teaches increase solar cell efficiency. *Id.* Ex.1003-Decl., ¶¶169-174.

X. SPECIFIC GROUNDS FOR UNPATENTABILITY

Pursuant to Rule 42.104(b)(4)-(5), and as confirmed in the Holman Declaration, the prior art references render obvious all Challenged Claims.⁴

A. Ground I: Claims 10-17 and 19-20 Are Invalid as Obvious Over Choi, Granek or Marvin, and Istratov.

1. Motivation to Combine and Reasonable Expectation of Success

Obviousness requires that the prior art references be “analogous to the claims being challenged,” and that a POSITA would have been motivated to combine the references with a reasonable expectation of success. *See Corephotonics, Ltd. v. Apple Inc.*, 84 F.4th 990, 1004 (Fed. Cir. 2023). Each requirement is met here. Ex.1003-Decl., ¶¶177-215.

Choi discloses the claimed structure of a silicon solar cell having an FSF, substrate, dielectric layer, and a polysilicon layer. *Supra* §IX.A. As is common in the field, Choi is directed to reducing recombination to increase efficiency, and Granek, Marvin, and Istratov each teach techniques to reduce recombination.

⁴ Any attempt by Patent Owner to rely on alleged secondary considerations of nonobviousness cannot overcome the showing of obviousness detailed herein. *E.g., Tokai Corp. v. Easton Enters., Inc.*, 632 F.3d 1358, 1371 (Fed. Cir. 2011).

Ex.1006-Choi, [0029]; Ex.1010-Granek, 117-136; Ex.1008-Marvin, 3-5; Ex.1012-Istratov, 569-570. A POSITA would have found it obvious to use the techniques of Granek, Marvin, and Istratov to further the goal of reducing recombination to improve efficiency. Ex.1003-Decl., ¶¶178-182.

i. Choi with Granek or Marvin

Analogous Art: Choi, Granek, and Marvin are analogous art to the Challenged Claims because they are in the same field as the Challenged Claims (solar cell devices) and are reasonably pertinent to solving the problems purportedly addressed in those claims (improving device efficiency by reducing recombination). Ex.1006-Choi, [0003], [0006], [0029]; Ex.1010-Granek, Abstract; Ex.1008-Marvin, 5, 15; Ex.1001-USP315, 1:21-39, 4:55-64, 5:1-25, claims 10-20. Like the '315 patent, Choi, Granek, and Marvin specifically teach back-contact solar cell structures with FSFs. *Id.* Ex.1003-Decl., ¶183.

Motivation to Combine: A POSITA would have been motivated to use Granek's or Marvin's dopant concentration in Choi's FSF region. Choi discloses a back-contact solar cell with either an n-type or p-type substrate and an FSF region used to reduce recombination. Ex.1006-Choi, [0026], [0029]. While Choi discloses the FSF region has a higher dopant concentration than the semiconductor substrate to reduce recombination (*id.*)—as was well known in the art (*supra* §V.B.2.i)—Choi

leaves the precise concentration to a POSITA's skill and discretion. Ex.1003-Decl., ¶¶185-185.

A POSITA implementing Choi would have therefore been motivated to look to other references, like Granek and Marvin, for details regarding the FSF field region dopant concentration. Granek and Marvin each teach the FSF dopant concentration is an important parameter for cell efficiency, and each teach specific ranges. Ex.1010-Granek, 120-122; Ex.1008-Marvin, 5, 9, 15. Granek discloses that a back-contact solar cell with an FSF dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ achieves the highest efficiency. Ex.1010-Granek, Abstract, 120-122; *supra* §IX.C. Similarly, Marvin teaches a back-contact solar cell (similar to Choi's) with an FSF dopant concentration from 1×10^{17} to $1 \times 10^{18} \text{ cm}^{-3}$. Ex.1008-Marvin, 5, 15. Marvin teaches that this concentration balances two key techniques for reducing recombination, therefore improving efficiency. *Id.* Specifically, the FSF dopant concentration must be high enough to reduce surface recombination, while low enough to minimize Auger recombination. Ex.1008-Marvin, 15; *supra* §IX.D. Therefore, a POSITA would have found it obvious to look to Granek and Marvin to determine the FSF dopant concentration for the cell disclosed in Choi. Granek's and Marvin's dopant concentrations are within the claimed range of "approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$." Ex.1003-Decl., ¶¶184-194.

Further, combining Choi with Granek (“Choi-Granek”) or Choi with Marvin (“Choi-Marvin”) would have involved only applying known techniques (using a specific FSF dopant concentration) to a known device (a back-contact solar cell) in the same way. Choi’s cell structure has a front surface facing the sun, a base area including an FSF, and back contacts. Ex.1006-Choi, [0026]-[0029], [0035], Figs.1, 3k. Choi teaches the FSF region is “doped at a concentration higher than the semiconductor substrate” and is created by “doping a first conductive type dopant”; “[f]or example, the front surface field layer 120 may be formed by doping the semiconductor substrate 10 with a first conductive type dopant by a variety of methods such as ion implantation or thermal diffusion.” Ex.1006-Choi, [0029], [0074]. The FSF of Choi’s cell structure is readily modifiable using Granek’s and Marvin’s specific dopant concentrations. Granek teaches adding an FSF by phosphorus (thermal) diffusion. Ex.1010-Granek, 117, 119, 124. Marvin states that “the FSF is generally introduced by heavier doping in a thin layer near the surface.” Ex.1008-Marvin, 15. A POSITA would have recognized that the dopant concentrations taught by Granek and Marvin would have equal application to Choi and would have been motivated to use those concentrations to reduce recombination, thereby improving efficiency. Ex.1003-Decl., ¶¶184-194.

Moreover, an FSF dopant concentration of “approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ ” was widely disclosed in the prior art well before the ’315 patent’s priority date. *See, e.g.,* Ex.1021-King, 369; Ex.1030-Swanson-352, 4:43-51; Ex.1040-Procel, 1; Ex.1041-Hermle, 5-6. A POSITA thus would have had “good reason to pursue the known option[]” of the FSF dopant concentration, given the need to solve problems with recombination and the availability of an identified, predictable solution. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007). Ex.1003-Decl., ¶¶184-194.

Reasonable Expectation of Success: A POSITA would have had a reasonable expectation of successfully combining Choi with Granek or Marvin. The combinations represent straightforward implementations of a dopant concentration of approximately $1 \times 10^{18}/\text{cm}^3$ or $1 \times 10^{17}/\text{cm}^3$ to $1 \times 10^{18}/\text{cm}^3$, respectively, in the FSF. Choi teaches “[t]he front surface field layer 120 ... is doped at a higher concentration than the semiconductor substrate 10” to “prevent[] electrons and holes separated by incident light from being recombined and then decay[ing] on the front surface of the semiconductor substrate 10.” Ex.1006-Choi, [0029]. Choi teaches that “the front surface field layer 120 may be formed ... by a variety of methods such as ion implantation and diffusion.” *Id.*, [0073]-[0074]. Back-contact solar cells are manufactured using a standard set of semiconductor fabrication processes known to

a POSITA by 2014. Indeed, the '315 patent specification discloses that the deposition process for forming the dopant region on the surface of the silicon substrate was “conventional.” Ex.1001-USP315, 4:32-41, Fig.1. Ex.1003-Decl., ¶¶195-202.

Choi, Granek, and Marvin each teach solar cells with similar structures, suggesting that techniques from one disclosure can be applied to another. For example, Granek discloses a desired dopant concentration of approximately $1 \times 10^{18}/\text{cm}^3$, and that the FSF is phosphorus-doped—the same n-type dopant disclosed by Choi. Ex.1010-Granek, 117, 121-122, Figs.7.1, 7-3.⁵ Granek’s experimental results support this finding. Similarly, Marvin teaches a back-contact solar cell with an FSF like Choi’s, an FSF dopant concentration of $1 \times 10^{17}/\text{cm}^3$ to $1 \times 10^{18}/\text{cm}^3$, and that “FSF is generally introduced by heavier doping in a thin layer

⁵ Granek separately discloses experimental results for solar cells that were fabricated and tested; of those cells, the one with the lowest dopant concentration ($3.8 \times 10^{18}/\text{cm}^3$) performed best. Ex.1010-Granek, 124-133. A POSITA would have expected, based on Granek’s experiments, that further decreasing the concentration to approach the simulation result of $1.0 \times 10^{18}/\text{cm}^3$ would have further improved performance. Ex.1003-Decl., ¶153.

near the interface.” Ex.1008-Marvin, 15. Given the similarity between the references and disclosed manufacturing techniques, a POSITA would have readily implemented the doping methods disclosed by Choi (such as ion implantation and diffusion) to dope the FSF of Choi’s cell to the dopant concentrations disclosed by Granek and Marvin. Moreover, Choi’s lack of disclosure as to a particular dopant concentration suggests that Choi thought that a POSITA would be able to select from known dopant concentrations to fabricate a solar cell. Ex.1003-Decl., ¶¶195-202.

Further, a POSITA would have known that fabricating Choi’s cell with Granek’s and Marvin’s dopant concentrations would have involved a minor adjustment to one fabrication step. Assuming the Choi cell did not already have the disclosed dopant concentration, only minor adjustments to the processing parameters of the dopant-diffusion process (such as heating time and temperature) would be required. No other steps would be affected, and no additional steps would be needed. Doping the FSF of a silicon substrate to a particular concentration near the surface would have been within the ordinary skill of the POSITA. Ex.1003-Decl., ¶199.

Furthermore, Marvin teaches that the doping range applies regardless of the environment in which the cell is deployed. Marvin states that an FSF doping range of $1 \times 10^{17}/\text{cm}^3$ to $1 \times 10^{18}/\text{cm}^3$ reduces recombination while also avoiding Auger

recombination occurring at higher concentrations, and specifically mentions this range in relation to the 1 sun, “BOL” conditions. Ex.1008-Marvin, 15. Under 1 sun conditions in a space environment, sunlight spectrum and intensity are similar to terrestrial conditions. *Id.*, 5, 14-15; Ex.1046-Green, 2. In addition, beginning of life (“BOL”) is the condition of the solar cell before it has been damaged by solar radiation in space. Ex.1008-Marvin, 11, 15-16. Therefore, findings at BOL under 1 sun conditions can be applied to space or terrestrial environments. Choi is not directed to any specific environment, whether space or terrestrial. Thus, a POSITA would have understood that, like Marvin, Choi’s cells are applicable to both space and terrestrial environments. Ex.1003-Decl., ¶¶201-202.

ii. Choi and Granek or Marvin with Istratov

Analogous Art: Choi, Granek, Marvin, and Istratov are analogous art to the Challenged Claims. Istratov is in the field of silicon semiconductor devices, from which POSITAs frequently adopted processing technologies. Choi, Granek, Marvin, and Istratov are in the same field as the Challenged Claims: silicon semiconductor devices (including solar cell devices). *Supra* §X.A.1.i; Ex.1012-Istratov, 569-570. Choi, Granek, and Marvin each disclose solar cell structures, and Istratov is in the field of silicon semiconductor devices, which encompasses solar cells. Ex.1012-Istratov, 570. Moreover, Choi, Granek, Marvin, and Istratov are

reasonably pertinent to solving the problems purportedly addressed in the Challenged Claims—reducing recombination to improved efficiency. *Supra* §X.A.1.i; Ex.1012-Istratov, 569-570. Choi, Granek, and Marvin all describe ways of improving the performance and efficiency of silicon-based solar cells. Istratov describes a way to improve a silicon structure directly applicable to improving solar cells. Ex.1012-Istratov, 569-570. Ex.1003-Decl., ¶¶203-204.

Motivation to Combine: Upon identifying detrimental levels of metal impurities in a solar cell substrate, a POSITA would have been motivated to add Istratov’s gettering process to the Choi-Granek or Choi-Marvin cell to trap impurities in the polysilicon layer—*i.e.*, an emitter—thereby reducing recombination. Choi discloses a back-contact silicon solar cell and adding features (*e.g.*, an FSF) to reduce recombination and improve efficiency. Ex.1006-Choi, [0006]-[0007], [0031]. Istratov teaches reducing recombination in a silicon-based device through gettering. Gettering of solar cells to relocate metal impurities from the silicon substrate to a polysilicon layer or emitter was widely disclosed in the prior art well before 2014. *Supra* §V.B.2.ii. Istratov teaches a test structure having a polysilicon layer over a silicon dioxide layer, layered in turn on a silicon substrate. Ex.1012-Istratov, 569-571, Figs.2, 4-5. As Istratov describes, the gettering process moves metal impurities (*e.g.*, iron, copper) from the substrate through an oxide layer

to a polysilicon layer, where they remain. *Id.*, 569-571, Figs.2, 4-5. By 2014, it was widely known that gettering of metal impurities through this structure would reduce recombination, improving solar cell efficiency. *See* Ex.1064-Istratov-2004, 4473. Ex.1003-Decl., ¶¶83-92, 205-209.

Therefore, a POSITA would have been motivated to apply Istratov's gettering technique to the Choi-Granek or the Choi-Marvin cell to further improve efficiency by trapping impurities in the polysilicon region (as Istratov expressly teaches), where such impurities would have been less likely to cause recombination. Ex.1003-Decl., ¶¶205-209.

Combining Choi-Granek or Choi-Marvin with Istratov would have involved nothing more than applying a known technique (gettering of metal impurities) to a known device (a back-contact solar cell with a precise FSF dopant concentration) in the same way, by using the same manufacturing techniques. Choi's cell includes the same layers as the test structure in Istratov—*i.e.*, a silicon substrate, followed by a dielectric region (*e.g.*, the silicon dioxide of Istratov), followed by conductive type areas 32, 34 (*e.g.*, the polysilicon layer of Istratov). *Infra* §IX.A; Ex.1012-Istratov, 569-571, Figs.2, 4-5. Choi teaches that a tunneling layer 20 can be made of oxides or nitrides and located on the back surface of the semiconductor substrate. Ex.1006-Choi, [0033]. A POSITA would have understood this tunneling layer to be a

dielectric, consistent with the '315 patent's teaching that the dielectric can be made of silicon dioxide and located on the back side of the cell. Ex.1001-USP315, 3:31-41, Fig.1, Claim 10. Further, Choi's conductive type areas 32, 34 can be made of polysilicon, are connected to the metal contacts, and collect charge carriers. *Supra* §IX.A; Ex.1006-Choi, [0023] [0036]-[0037], [0044]. A POSITA would have understood that Choi's conductive type areas 32, 34 correspond to the '315 patent's emitter regions, also described as doped polysilicon regions for collecting charge carriers. Ex.1001-USP315, 2:40-42. A POSITA would have therefore recognized that Istratov's removal of metal impurities from the substrate, through diffusion into the silicon dioxide and the polysilicon layer, would have been desirable in Choi's similar structure to reduce recombination, thus improving efficiency. Ex.1003-Decl., ¶¶205-209.

Reasonable Expectation of Success: A POSITA would have had a reasonable expectation of successfully combining Choi-Granek or Choi-Marvin with Istratov—a straightforward implementation of heating the silicon solar cell to a temperature high enough to cause gettering through an oxide layer to a polysilicon layer. Ex.1012-Istratov, 570. Choi teaches a thermal-treatment step during doping of the first and second conductive type areas, which can be made of polycrystalline silicon, but without specifying the temperature used. Ex.1006-Choi, [0036]-[0037],

[0070]. A POSITA would have recognized that this step would have been used to getter metals from the substrate to the first and second conductive type areas, through heating the cell to a sufficiently high temperature. Ex.1064-Istratov-2004, 4473. To the extent that Choi's processing temperature was not high enough, a POSITA would have used Istratov's instructions or merely selected a higher temperature and heated the cell for enough time to induce gettering. Ex.1003-Decl., ¶¶210-215.

Istratov teaches specific conditions that result in gettering of iron and copper. For iron, Istratov teaches that heating for "8 h[ours]" "at 1020°C" was "sufficient to equilibrate the iron through the SiO₂ layer." Ex.1012-Istratov, 570, Fig.2. For copper, Istratov teaches that heating "at 690 °C for 5 h[ours]" and "at 1150 °C for 2 h[ours]" resulted in copper diffusion from the silicon substrate to the polysilicon layer. Ex.1012-Istratov, 571, Figs.4-5. Ex.1003-Decl., ¶¶161-168, 212.

Moreover, a POSITA would have recognized the modular nature of solar cells and therefore would have understood that combining the Choi-Granek or Choi-Marvin cell with Istratov would reduce recombination. Such cells can be thought of as modular, *i.e.*, the front side and back side of the cell can be designed and optimized separately. Ex.1043-Glunz, 365. After considering processing sequence and thermal and chemical compatibility of materials, the modifications introduced

by combining Istratov with the Choi-Granek or Choi-Marvin cell would not have affected the cell's front area. Ex.1003-Decl., ¶¶214-215.

2. Claim 10

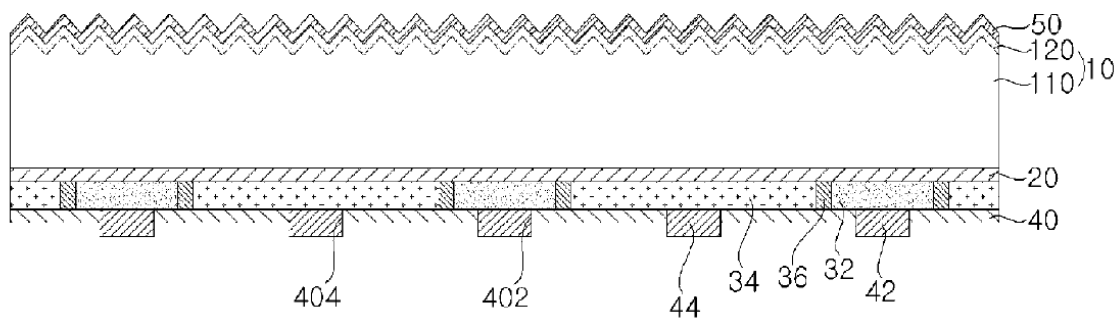
i. Claim 10[preamble]

To the extent the preamble is limiting, Choi teaches *a solar cell, the solar cell having a front side which faces the sun during normal operation and a back side opposite the front side.*

Choi teaches a “solar cell 100” that “includes a semiconductor substrate 10” having a “base area 110,” and a “front surface field layer 120” that is formed on the front side of the substrate. Ex.1006-Choi, [0023], [0029].

FIG. 1

100



Id., Fig.1.

A POSITA would have recognized that the top of Figure 1 is a “front side” of solar cell 100 (because Choi describes the layers at the top of the cell as “front”

layers) and that the bottom is a “back side opposite the front side” (because Choi describes the bottom layers as being on the substrate’s “back surface”). Thus, Choi teaches a “solar cell ... having a front side ... and a back side opposite the front side,” as claimed. Ex.1003-Decl., ¶¶216-226.

A POSITA also would have recognized that the top (front) side of solar cell 100 “faces the sun during normal operation.” Choi teaches that “first” and “second” “conductive type areas” 32, 34 are formed on the tunneling layer 20, and that “the first conductive type area 32” may “serv[e] as an emitter causing photoelectric transformation through [the] junction with the base area 110.” Ex.1006-Choi, [0023], [0026]. A POSITA would have recognized the structure of Choi’s Fig.1 as a back-contact solar cell, the front surface of which faces the sun during normal operation. Ex.1003-Decl., ¶¶217-223.

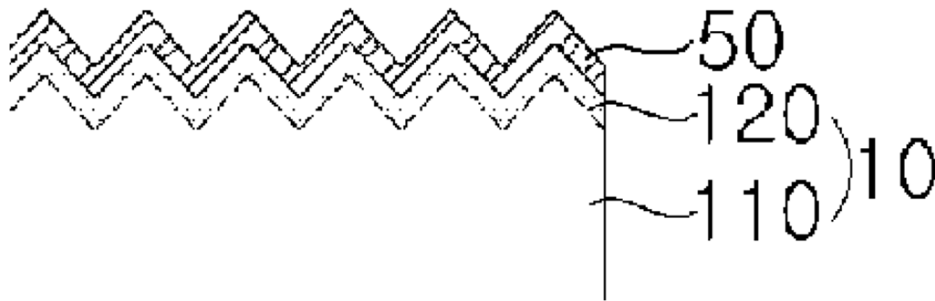
Further, Choi teaches an “anti-reflective film 50” (top of Figure 1) that “may be entirely formed over the front surface” of substrate 10. Ex.1006-Choi, [0030]. A POSITA would have recognized that Choi’s anti-reflective film 50 on the front surface faces incident light (*i.e.*, the sun) during normal operation. Ex.1003-Decl., ¶¶225-226.

ii. Claim 10[a]

The combination of Choi and Granek or Marvin teaches *a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal $2 \times 10^{18} \text{ cm}^{-3}$ and wherein the portion of the silicon substrate is formed at the front side of the solar cell.*

Choi explains that the semiconductor substrate 10, shown in Figure 1, may be “crystalline silicon.” Ex.1006-Choi, [0023], [0025], Fig.1. Thus, Choi teaches “a silicon substrate” as claimed.

Choi also teaches that semiconductor substrate 110 “may include a base area 110 containing a low doping concentration” of “first conductive type dopant,” and a “front surface field 120” that may be “formed” on the front side of the semiconductor substrate. Ex.1006-Choi, [0024], [0029]. Choi teaches that the FSF layer “may be formed by doping the semiconductor substrate 10 with a first conductive type dopant.” *Id.*, [0074]. A POSITA would have recognized that the FSF 120 is a “portion” of semiconductor substrate 10 because Fig. 1 teaches that semiconductor substrate 10 includes both the base area 110 and the FSF layer 120:



Id., Fig.1 (excerpted). Thus, Choi teaches “a portion of the silicon substrate ... wherein the portion of the silicon substrate is formed at the front side of the solar cell” as claimed. Ex.1003-Decl., ¶¶227-237.

A POSITA would also have understood that FSF layer 120 is doped with the same dopant type as semiconductor substrate 110. Choi teaches the FSF layer 120 “is an area where the first conductive-type dopant is doped at a concentration higher than the semiconductor substrate 10.” Ex.1006-Choi, [0029]. Ex.1003-Decl., ¶¶235-236.

As discussed in §X.A.1.i, Granek teaches that an FSF with a dopant concentration of approximately 1×10^{18} provided the highest solar cell efficiency of all the dopant concentrations analyzed. Ex.1010-Granek, 120-122; *supra* §IX.C. Similarly, Marvin found that “[t]he FSF effectiveness is relatively constant over a rather broad range around $1E17$ to $1E18$ cm^{-3} , decreasing below this level due to the weakness of the electric field and decreasing above this level due to increased Auger recombination.” Ex.1008-Marvin, 15; *supra* §IX.D. A POSITA would have been

motivated to combine Granek's or Marvin's FSF dopant concentration with Choi's FSF to dope a solar cell with the claimed dopant concentration with a reasonable expectation of success. Ex.1003-Decl., ¶¶238-248; *supra* §X.A.1.i.

iii. Claim 10[b]

Choi teaches *a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of the solar cell.*

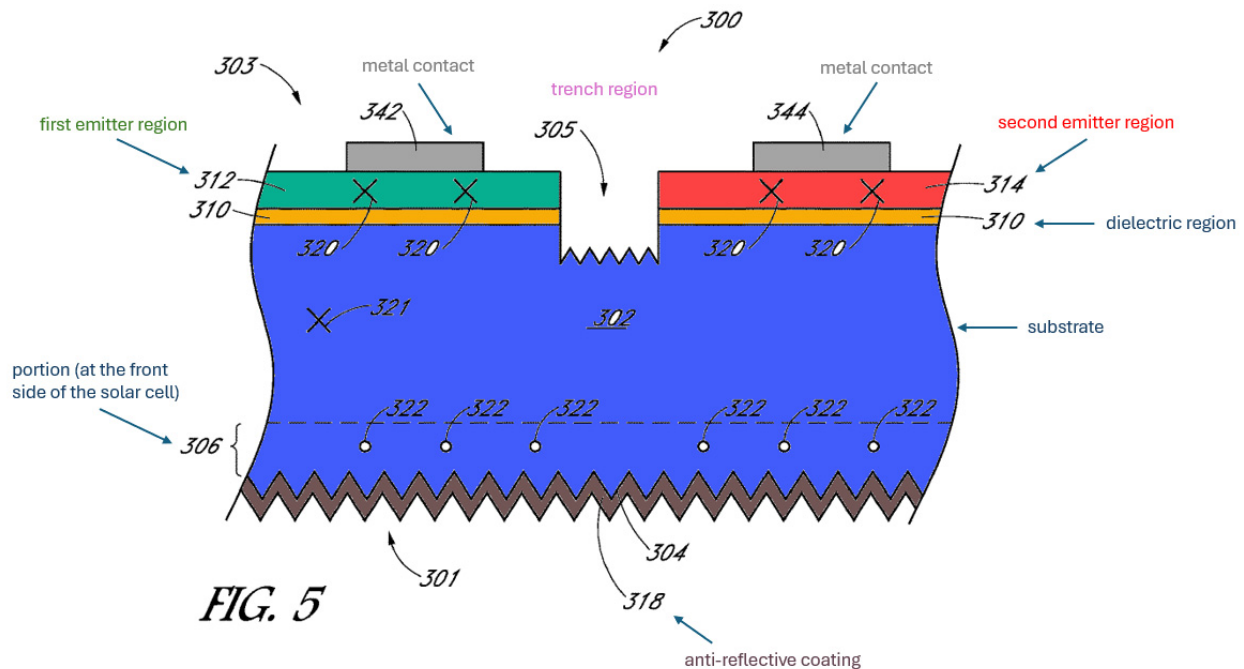
Choi teaches a “tunneling layer 20,” shown in Fig.1, “formed on the back surface of the semiconductor substrate 10” that “improves interface properties of the back surface of the semiconductor substrate 10 and enables produced carriers to be efficiently transferred through tunneling effect.” Ex.1006-Choi, [0033], Fig.1. Choi teaches that the tunneling layer 20 “may include a variety of materials enabling tunneling of carriers,” including “oxides, nitrides and conductive polymers.” *Id.* A POSITA would have understood that these materials are dielectric materials. Ex.1003-Decl., ¶¶249-253.

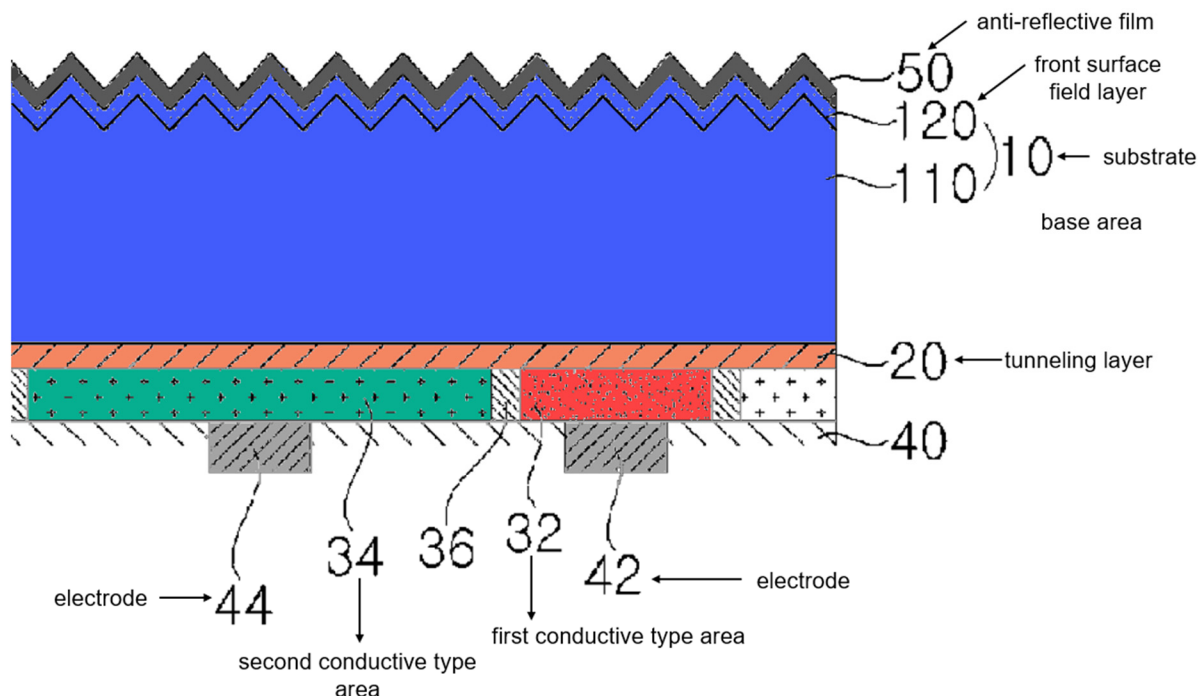
iv. Claim 10[c]

Choi alone or in combination with Istratov teaches *a first emitter region having metal impurities formed over the dielectric region.*

The '315 patent refers to the “P-type and N-type doped polysilicon regions” formed over dielectric region 310 in Figure 5 (shown below on right-side) as “first

and second emitter regions 312, 314,” respectively. Ex.1001-USP315, 6:55-57. The ’315 patent teaches the first and second emitter regions 312, 314 are “doped region[s] of a solar cell for collecting positive and negative charge carriers.” Ex.1001-USP315, 2:40-42.





Ex.1001-USP315, Fig.5 (top); Ex.1006-Choi, Fig.1 (excerpted) (bottom).

Choi teaches the same structures, arrangement of layers, and functions as the '315 patent's claimed "first and second emitter regions." Like the '315 patent, Choi teaches p-type and n-type doped structures—*i.e.*, the "second conductive type area 34" and the "first conductive type area 32"—formed over "the tunneling layer 20." Ex.1006-Choi, [0023], [0036]-[0037], Fig.1. Choi further discloses the first and second conductive type areas 32, 34 may be "formed by doping ... polycrystalline silicon ... with a [] conductive type dopant." *Id.*, [0036]-[0037]. Choi likewise teaches that electrodes 42 and 44, "which are connected to first and second conductive types area 32 and 34, "collect carriers" "and transport the [carriers] to the outside." Ex.1006-Choi, [0023], [0044]. Ex.1003-Decl., ¶¶259-266.

A POSITA would have recognized the claimed “first emitter region” corresponds to Choi’s second conductive area 34 and that the claimed “second emitter region” corresponds to Choi’s first conductive type area 32. As explained above (§X.A.2.iii), Choi’s tunneling layer 20 is the claimed “dielectric region.” Thus, Choi teaches “a first emitter region ... formed over the dielectric region” as claimed. Ex.1003-Decl., ¶¶254-266.

To the extent Patent Owner argues that the claimed invention includes any metal or any source of metal, Choi also teaches a first emitter region “having metal impurities.” Choi teaches a semiconductor substrate 10 “containing a first conductive-type dopant.” Ex.1006-Choi, [0025]. Choi explains that “the first conductive-type dopant” may be an “n-type impurity” (*e.g.*, phosphorus, arsenic, bismuth, antimony), or alternatively, a “p-type impurity” (*e.g.*, boron, aluminum, gallium, indium) (*id.*)—which are Group III and V elements. Further, as discussed above (§IX.A), Choi teaches that each of the first and second conductive type areas 32, 34 is doped with either p- or n-type impurities in different embodiments. Ex.1006-Choi, [0026], [0036]-[0037]. Thus, because a POSITA would have understood that at least bismuth, aluminum, gallium, and indium are metals, a POSITA would have understood that Choi’s first and second conductive type areas 32, 34 are doped with metal impurities. Thus, Choi teaches “a first emitter region

having metal impurities formed over the dielectric region” as claimed. Ex.1003-Decl., ¶¶267-268.

To the extent Patent Owner contends that the claimed “metal impurities” must be elements other than Group III or V elements, Choi in combination with Istratov teaches and renders obvious a first emitter having metal impurities. As discussed above (§§IX.E, X.A.1.ii), Istratov teaches a device structure with the same layers as Choi and the ’315 patent. Specifically, Istratov teaches a “test structure” with an oxide layer formed over a silicon substrate and a polysilicon layer formed over the oxide layer. Ex.1012-Istratov, 570, Fig.2. Ex.1003-Decl., ¶¶269-271.

Istratov also teaches metal impurities in the polysilicon region. Specifically, Istratov teaches the accumulation of iron and copper in the polysilicon layer during a heating step, and Istratov’s figures show higher iron and copper concentrations in the polysilicon layer than in the silicon substrate and oxide layers after heating. Ex.1012-Istratov, 570-571, Figs.2, 4-5. As discussed above (§X.A.1.ii), a POSITA would have been motivated to combine Choi with Istratov with a reasonable expectation of success. Ex.1003-Decl., ¶¶272-276.

v. Claim 10[d]

Choi teaches *a first metal contact formed over the first emitter region.*

As explained above (§X.A.2.iv), a POSITA would have recognized that the claimed “first emitter region” corresponds to Choi’s second conductive area 34. Choi teaches a second electrode 44, which “may include a variety of metal materials,” is “connected to” the second conductive type area 34, as shown in Figure 1. Ex.1006-Choi, [0023], [0044], Fig.1.

Choi further teaches that second electrode 44 “may be formed ... by a variety of methods such as coating or deposition” or alternatively “by applying a paste.” Ex.1006-Choi, [0076]-[0077]. A POSITA would have recognized that the claimed “first metal contact” corresponds to Choi’s second electrode 44. Ex.1003-Decl., ¶¶277-282.

3. Claim 11

Claim 11 depends from claim 10. Petitioner incorporates Section X.A.2.

Choi further teaches *the portion of the silicon substrate comprises N-type dopants*. Choi teaches the FSF layer 120 “is an area where the first conductive-type dopant is doped at a concentration higher than the semiconductor substrate 10” and the “first conductive-type dopant may be an n-type impurity.” Ex.1006-Choi, [0025], [0029]. Ex.1003-Decl., ¶¶283-285.

4. Claim 12

Claim 12 depends from claim 10. Petitioner incorporates Section X.A.2.

Choi further teaches *the portion of the silicon substrate comprises phosphorus*. Choi teaches that the FSF layer 120 “is an area where the first conductive-type dopant is doped at a concentration higher than the semiconductor substrate 10” and that “the first conductive-type dopant may be an n-type impurity ... including phosphorous.” Ex.1006-Choi, [0025], [0029]. Ex.1003-Decl., ¶¶286-288.

5. Claim 13

Claim 13 depends from claim 10. Petitioner incorporates Section X.A.2.

Choi further teaches *the portion of the silicon substrate comprises P-type dopants*. Choi teaches that the FSF layer 120 “is an area where the first conductive-type dopant is doped at a concentration higher than the semiconductor substrate 10” and that the “first conductive-type dopant may be a p-type impurity.” Ex.1006-Choi, [0025], [0029]. Ex.1003-Decl., ¶¶289-291.

6. Claim 14

Claim 14 depends from claim 10. Petitioner incorporates Section X.A.2.

Choi further teaches *the portion of the silicon substrate comprises boron*. Choi teaches that the FSF layer 120 “is an area where the first conductive-type dopant is doped at a concentration higher than the semiconductor substrate 10” and

that “the first conductive-type dopant may be a p-type impurity ... including boron.” Ex.1006-Choi, [0025], [0029]. Ex.1003-Decl., ¶¶292-294.

7. Claim 15

Claim 15 depends from claim 10. Petitioner incorporates Section X.A.2.

Choi further teaches *the first emitter comprises polysilicon*. Choi teaches that the second conductive type area 34—which a POSITA would have recognized corresponds to the claimed “first emitter” (§X.A.2.iv)—can be “formed by doping ... polycrystalline silicon ... with a second conductive type dopant.” Ex.1006-Choi, [0037]. Additionally, Choi teaches the second conductive type area “may include ... polycrystalline silicon.” *Id.*, [0039]. A POSITA would have understood Choi’s references to “polycrystalline silicon” to mean “polysilicon.” Ex.1003-Decl., ¶¶295-299.

8. Claim 16

Claim 16 depends from claim 10. Petitioner incorporates Section X.A.2.

i. Claim 16[a]

The combination of Choi and Istratov further teaches the additional limitation of claim 16[a] (*a second emitter region having metal impurities formed over the dielectric region*).

As discussed above for limitation 10[c] (§X.A.2.iv), Choi teaches the “first conductive type area 32” has the same structure, doping type, and function as the claimed “second emitter region.” Ex.1006-Choi, [0023], [0036]-[0037], Fig.1. A POSITA would have recognized that the claimed “second emitter region” corresponds to Choi’s first conductive type area 32, and that tunneling layer 20 is the claimed “dielectric region.” *Supra* §§X.A.2.iii, iv. Thus, Choi teaches “a second emitter region ... formed over the dielectric region” as claimed. Further, as explained above (§X.A.2.iv), to the extent Patent Owner argues that the claimed invention includes any metal or any source of metal, a POSITA would also have understood that Choi’s second conductive type area 34 is doped with metal impurities. Thus, Choi teaches limitation 16[a]. Ex.1003-Decl., ¶¶300-308.

To the extent that Patent Owner contends that the claimed “metal impurities” must be elements other than Group III or V elements, Choi in combination with Istratov teaches and renders obvious a second emitter having metal impurities, and a POSITA would have been motivated to make the combination with a reasonable expectation of success, for the same reasons explained above for limitation 10[c]. *Supra* §§X.A.1.ii, X.A.2.iv. Istratov teaches the accumulation of iron and copper (metal impurities) in the polysilicon layer during a heating step. *Supra* §§IX.E,

X.A.1.ii, X.A.2.iv. Thus, Choi in combination with Istratov teaches and renders obvious limitation 16[a]. Ex.1003-Decl., ¶¶309-316.

ii. Claim 16[b]

Choi further teaches the additional limitation of claim 16[b] (*a second metal contact formed over the second emitter region*). As explained above (§§X.A.2.iv, X.A.8.i), a POSITA would have recognized that the claimed “second emitter region” corresponds to Choi’s first conductive type area 32.

Choi teaches that a “first electrode[] 42,” which “may include a variety of metal materials,” is “connected to” the first conductive type area 32, as shown in Figure 1. Ex.1006-Choi, [0023], [0044], Fig.1.

Choi further teaches that first electrode 42 “may be formed ... by a variety of methods such as coating or deposition” or alternatively “by applying a paste.” Ex.1006-Choi, [0076]-[0077]. A POSITA would have recognized that the claimed “second metal contact” corresponds to Choi’s first electrode 42. Ex.1003-Decl., ¶¶317-320.

9. Claim 17

Claim 17 depends from claim 16. Petitioner incorporates Section X.A.8.

Choi further teaches *the second emitter region is separate from the first emitter region*. Choi teaches a “barrier area 36” that is “disposed between” and

“separate[s] the first conductive type area 32 from the second conductive type area 34.” Ex.1006-Choi, [0038], [0052]. Choi explains that “[w]hen the first conductive type area 32 contacts the second conductive type area 34, [a] shunt is generated and [the] performance of the solar cell 100 is deteriorated.” *Id.*, [0038]. Barrier area 36 is thus interposed between the conductive type, “preventing unnecessary shunt.” *Id.* Ex.1003-Decl., ¶¶321-325.

10. Claim 19

Claim 19 depends from claim 16. Petitioner incorporates Section X.A.8.

Choi further teaches *the second emitter region comprises polysilicon*. Choi teaches that the first conductive type area 32—which a POSITA would have recognized corresponds to the claimed “second emitter region” (*supra* §§X.A.2.iv, X.A.8)—can be “formed by doping ... polycrystalline silicon ... with a first conductive type dopant.” Ex.1006-Choi, [0036]. Additionally, Choi teaches the first conductive type area 32 “may include ... polycrystalline silicon.” *Id.*, [0039]. A POSITA would have understood Choi’s references to “polycrystalline silicon” to mean “polysilicon.” Ex.1003-Decl., ¶¶326-330.

11. Claim 20

Claim 20 depends from claim 16. Petitioner incorporates Section X.A.8.

Choi further teaches *the first emitter region comprises a P-type doped polysilicon region and the second emitter region comprises an N-type doped polysilicon region*. As discussed above (§§X.A.7, X.A.10), Choi teaches first and second emitter regions comprising polysilicon. Further, Choi teaches that the first and second conductive type layers 32 and 34—which a POSITA would have recognized correspond to the claimed “second emitter region” and “first emitter region,” respectively—are n-type and p-type, respectively, but that, in an alternative embodiment, “the base area 110 and the first conductive type area 32 may be a p-type while the second conductive type area 34 may be an n-type.” Ex.1006-Choi, [0026]. Ex.1003-Decl., ¶¶331-334.

B. Ground II: Claim 18 Is Invalid as Obvious Over Choi, Granek or Marvin, Istratov, and Smith.

1. Motivation to Combine and Reasonable Expectation of Success

As discussed above (§X.A.1.ii), it would have been obvious to combine Choi, Granek or Marvin, and Istratov. Further, Smith teaches “a trench region separates the first emitter region from the second emitter region” as recited by claim 18. Smith discloses a solar cell having positive and negative metal contacts on the cell’s back surface and that “the doped regions 101 and 102 are separated by a trench 104, which serves as a gap between the doped regions.” Ex.1011-Smith, [0019], [0024], Fig.2.

A POSITA would have found it obvious to use a trench, as taught by Smith, to isolate the P-type and N-type emitter regions in the Choi-Granek-Istratov or Choi-Marvin-Istratov cell. Ex.1003-Decl., ¶¶335-338.

Analogous Art: Choi, Granek, Marvin, Istratov, and Smith are analogous art to the Challenged Claims. As explained above (§X.A.1.ii), Choi, Granek, Marvin, and Istratov are in the same field as the Challenged Claims. Smith is also directed to improving silicon-based solar efficiency. Ex.1011-Smith, [0007], [0015], [0025]. Further, like the claims, Smith describes a back-contact solar cell. *Id.*, [0016]. Ex.1003-Decl., ¶339.

Motivation to Combine: A POSITA would have been motivated to implement the Choi-Granek-Istratov or Choi-Marvin-Istratov cell with a trench as taught by Smith to improve efficiency. As discussed above (§X.A.1), the Choi-Granek and Choi-Marvin cells are back-contact cells. The back contacts of the Choi-Granek and Choi-Marvin cells have positive and negative electrodes. Ex.1006-Choi, [0026]. Smith teaches that, for cells with polysilicon doped regions (*e.g.*, Choi's), directly abutting p-type and n-type doped regions adversely affect efficiency because "recombination in the space charge region where the polysilicon doped regions touch is very high due to the lifetime of charge carriers in the polysilicon being very

low.” Ex.1011-Smith, [0015]. Smith expressly teaches adding a trench 104 to serve as a gap between the doped regions, which is shown in Figure 2. *Id.* at [0019].

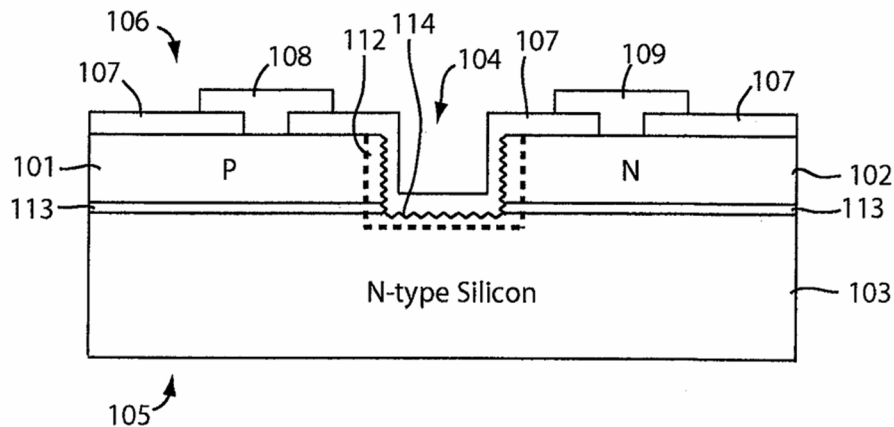


FIG. 2

Id., Fig.2. Ex.1003-Decl., ¶¶340-345.

Smith teaches that a trench addresses known adverse effects on efficiency from directly touching doped regions in three ways. First, it “prevents the space charge region from existing in either polysilicon film.” Ex.1011-Smith, [0025]. Second, “the resulting accumulation layer under the trench 104 repels minority carriers to improve surface passivation.” *Id.* Finally, “the textured surface 114 in the trench 104 increases solar radiation collection,” all of which, Smith teaches, increase solar cell efficiency. *Id.* A POSITA would therefore have been motivated by Smith’s express teaching to add a trench to the Choi-Granek-Istratov or the Choi-Marvin-Istratov cell. Ex.1003-Decl., ¶¶344-345.

Combining Choi-Granek-Istratov or Choi-Marvin-Istratov with Smith would have involved nothing more than applying a known technique (using a trench) to a known device (a back-contact solar cell) in the same way. As discussed above (§IX.F), Smith discloses a back-contact solar cell having a trench to electrically separate oppositely doped polysilicon regions. Ex.1011-Smith, [0016], [0019], [0024]. A POSITA would have been able to integrate the trench into the Choi-Granek-Istratov or Choi-Marvin-Istratov cell to create a cell with improved efficiency. Ex.1003-Decl., ¶¶346-349.

Reasonable Expectation of Success: Modification of the Choi-Granek-Istratov or Choi-Marvin-Istratov cell to include the trench of Smith would have been readily implemented by a POSITA using standard semiconductor fabrication techniques. Smith discloses standard techniques for forming the trench. *See* Ex.1011-Smith, [0017], [0019], [0025]. Smith teaches two processes for forming the trench separating the doped regions. Ex.1011-Smith, [0029]-[0035]. These standard techniques for forming the trench taught by Smith would have been within the level of skill of a POSITA. Ex.1003-Decl., ¶¶347-348.

A POSITA would have had a reasonable expectation of success in implementing Smith's trench, given similarities to other references: the Choi-Granek-Istratov and Choi-Marvin-Istratov cells relate to back-contact solar cells, as

does Smith, which also describes benefits of adding a trench to cells (like Choi's) with polysilicon doped regions. *Supra* §IX.F. Accordingly, a POSITA would have been motivated to combine their teachings with a reasonable expectation of success. Ex.1003-Decl., ¶349.

2. Claim 18

Claim 18 depends from claim 16. Petitioner incorporates Section X.A.8.

The combination of Choi and Smith further teaches *a trench region separates the first emitter region from the second emitter region*. As discussed above (§§X.A.2.iv, X.A.8), Choi teaches a *first emitter region* and a *second emitter region*.

Smith teaches doped regions 101 and 102 formed over the back side of a silicon substrate, as shown in Figure 2 (*supra* §IX.F). Ex.1011-Smith, [0016], Fig.2. Smith teaches that doped region 101 is a p-type doped region, while doped region 102 is an n-type doped region, and the substrate 103 is an n-type silicon wafer. *Id.*, [0017]. A POSITA would have recognized doped regions 101 and 102 as first and second “emitters” as that term is used in the '315 patent. *See supra* §X.A.2.iv; Ex.1003-Decl., ¶353.

Smith further teaches a trench 104, “serv[ing] as a gap between the doped regions 101 and 102.” Ex.1011-Smith, [0019], [0029], [0041]. Smith explains that “in both the first and second trench formation processes,” “the trench [] serves as a

gap physically separating the P-type doped region [] from the N-type doped region.” *Id.*, [0036]. Thus, Smith teaches first and second emitter regions, “wherein a trench region separates the first emitter region from the second emitter region.” Ex.1003-Decl., ¶¶350-355.

C. Ground III: Claims 10-15 Are Invalid as Obvious Over Cousins, Granek or Marvin, and Istratov.

1. Motivation to Combine and Reasonable Expectation of Success

As explained above (§X.A.1), a POSITA would have been motivated to combine Choi with Granek or Marvin and Istratov with a reasonable expectation of success. It would also have been obvious to combine Cousins with Granek or Marvin and Istratov for similar reasons.

i. Cousins with Granek or Marvin

Analogous Art: Cousins, Granek, and Marvin are in the same field as the Challenged Claims (solar cell devices) and also reasonably pertinent to solving the problems purportedly addressed in the Challenged Claims (improving device efficiency by reducing recombination). Ex.1007-Cousins, 1:15-18, 2:22-23, 2:49-58; *supra* §X.A.1.i. Similar to the ’315 patent, Granek, and Marvin, Cousins discloses a doped front portion in the substrate, which is an “N-type doped region 105 [that] provides low front surface recombination and improves lateral

conductivity.” Ex.1007-Cousins, 2:49-54; *supra* §§IX.B, X.A.1.i. Ex.1003-Decl., ¶¶359-361.

Motivation to Combine: A POSITA would have been motivated to use Granek’s or Marvin’s dopant concentration in Cousins’ doped front portion. Cousins teaches a both-sides-contacted solar cell having an n-type substrate 101 and an n-type “doped region 105” formed on the front side of the substrate 101 to provide “low front surface recombination.” Ex.1007-Cousins, 2:39-55, 2:48-53, Fig.1. Thus, like Choi, Granek, and Marvin, Cousins discloses a solar cell having a doped front portion for reducing recombination. *Supra* §IX.B. While Cousins provides a range “of 100 to 500 Ω/sq ” for the sheet resistance of the n-type doped region 105, which is compatible with the claimed dopant concentration, it leaves the selection of other parameters (*e.g.*, dopant concentration) to a POSITA’s skill and discretion. *See* Ex.1007-Cousins, 2:49-55. Ex.1003-Decl., ¶¶362-365.

For reasons similar to those explained in §X.A.1.i, a POSITA would have found it obvious to look to Granek’s and Marvin’s disclosed FSF dopant concentration to implement into Cousins’ solar cell. A POSITA would have been motivated to look to Granek and Marvin to fill in the implementation details regarding the dopant concentration of Cousins’ doped region 105. Further, a POSITA would have understood from Figure 7-4 of Granek that, for practical FSF

depths, Cousins' sheet resistance of 100 to 500 Ω/sq is consistent with the FSF dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ from Granek. Ex.1007-Cousins, 2:49-55; Ex.1010-Granek, 123 (Fig.7-4). Ex.1003-Decl., ¶¶362-365.

Reasonable Expectation of Success: A POSITA would have had a reasonable expectation of successfully combining Cousins with Granek ("Cousins-Granek") or Marvin ("Cousins-Marvin"). The combinations represent a straightforward implementation of a dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ in the doped front portion. Cousins teaches that "[t]he N-type doped region 105" may be "form[ed]" by "diffus[ing] N-type dopants into the front side of the substrate 101," for example, by exposing "to phosphorus in [a] diffusion furnace." Ex.1007-Cousins, 5:49-6:13. A POSITA would have readily implemented these diffusion methods to dope the front portion of Cousins' cell to the concentration disclosed by Granek and Marvin. Doping the front portion of a silicon substrate to a particular concentration near the surface would have been within a POSITA's ordinary skill. Ex.1003-Decl., ¶¶366-367.

ii. Cousins and Granek or Marvin with Istratov

Analogous Art: Cousins, Granek, Marvin, and Istratov are analogous art to the Challenged Claims. Cousins, Granek, Marvin, and Istratov are in the same field as the Challenged Claims (silicon semiconductor devices including solar cell

devices) and are reasonably pertinent to solving the problems purportedly addressed in the Challenged Claims (improving device efficiency by reducing recombination). Ex.1007-Cousins, 1:15-18, 2:22-23, 2:49-58; *supra* §X.A.1.ii. Cousins, Granek, and Marvin teach solar cell structures, and Istratov is in the field of silicon semiconductor devices, which encompasses solar cells. Ex.1012-Istratov, 570. Moreover, Cousins, Granek, Marvin, and Istratov are reasonably pertinent to solving the problems purportedly addressed in the Challenged Claims—improving device efficiency by reducing recombination. Ex.1007-Cousins, 1:38-41, 2:49-55; *supra* §X.A.1.ii. Cousins, Granek, and Marvin all describe ways of improving the performance and efficiency of silicon-based solar cells. Istratov describes a way of improving a silicon structure that is directly applicable to improving solar cells. Ex.1012-Istratov, 569-570. Ex.1003-Decl., ¶¶368-369.

Motivation to Combine: A POSITA would have also been motivated to add Istratov’s gettering process to the Cousins-Granek or Cousins-Marvin cell to trap impurities in the emitter and thus reduce recombination for the same reasons explained in §X.A.1.ii. Ex.1003-Decl., ¶¶370-371.

Combining Cousins-Granek or Cousins-Marvin with Istratov would have involved nothing more than the application of known techniques (gettering of metal impurities) to a known device (a both-sides-contacted cell with a doped front

portion), in the same way, using the same manufacturing techniques. The back area of the cell in Cousins is readily modifiable using Istratov's gettering into the polysilicon region. Ex.1012-Istratov, [0019]. Ex.1003-Decl., ¶¶370-371.

Reasonable Expectation of Success: A POSITA would have had a reasonable expectation of successfully combining Cousins-Granek or Cousins-Marvin with Istratov for the same reasons explained in §X.A.1.ii. Combining Cousins-Granek or Cousins-Marvin with Istratov would be a straightforward implementation of a dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ and $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$, respectively, in the doped front portion and gettering of metal impurities into the emitter region. Ex.1003-Decl., ¶¶356-374.

Cousins teaches a “polysilicon layer 108” that is “formed on a thin dielectric layer 107” and “has an emitter saturation current of about $10 \text{ fA} \cdot \text{cm}^{-2}$.” Ex.1007-Cousins, 2:42-44, 3:12-13. Thus, Cousins' cell structure (like Choi's) includes a substrate and an emitter region (“polysilicon layer 108”) into which metal impurities from the substrate would be gettered using the Istratov process to getter impurities into a polysilicon layer of the solar cell. *Supra* §X.A.1.ii. A POSITA would have been motivated to apply Istratov's gettering technique to the Cousins-Granek or Cousins-Marvin cell to further improve efficiency by trapping impurities in the emitter, as Istratov taught. Ex.1003-Decl., ¶¶356-374.

2. Claim 10

i. Claim 10[preamble]

To the extent the preamble is limiting, Cousins teaches *a solar cell, the solar cell having a front side which faces the sun during normal operation and a back side opposite the front side*. Cousins teaches a solar cell having a front side that “faces the sun during normal operation to collect solar radiation” and a back side opposite the front side. Ex.1007-Cousins, 2:31-38; Ex.1003-Decl., ¶¶375-376.

ii. Claim 10[a]

Cousins in combination with Granek or Marvin teaches and renders obvious *a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal $2 \times 10^{18} \text{ cm}^{-3}$ and wherein the portion of the silicon substrate is formed at the front side of the solar cell*.

Cousins teaches a doped region 105 that “provides low front surface recombination and improves lateral conductivity.” Ex.1007-Cousins, 2:44-55. Doped region 105 is formed on the front side of substrate 101, as shown in Figure 1, and may have a sheet resistance of 100 to 500 Ω/sq . *Id.* Doped region 105 is formed by diffusing dopants into the front side of substrate 101. *Id.*, 5:48-53.

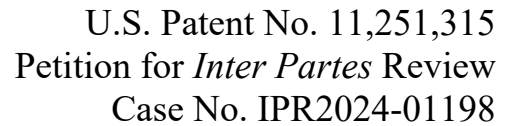


FIG. 1

Ex.1007-Cousins, Fig.1. A POSITA would have recognized that Cousins' doped region 105 is the claimed "portion of the silicon substrate [] formed at the front side of the solar cell." Ex.1003-Decl., ¶¶377-379.

A POSITA would have understood that doped region 105 and substrate 101 have the same dopant type, and Cousins teaches driving n-type dopants to the front side of n-type silicon substrate 101 to form n-type doped region 105. Ex.1007-Cousins, 2:44-49, 5:48-53. Ex.1003-Decl., ¶¶380-382.

As discussed in §X.A.1.i, Granek teaches that an FSF with a dopant concentration of approximately 1×10^{18} provided the highest solar cell efficiency of all the concentrations analyzed. Ex.1010-Granek, 120-122; *supra* §IX.C. Similarly, Marvin found that “[t]he FSF effectiveness is relatively constant over a rather broad

range around $1\text{E}17$ to $1\text{E}18\text{ cm}^{-3}$, decreasing below this level due to the weakness of the electric field and decreasing above this level due to increased Auger recombination.” Ex.1008-Marvin, 15; *supra* §IX.D. A POSITA would have been motivated to combine Granek’s or Marvin’s FSF dopant concentration with Cousins’ doped region 105 to dope a solar cell with the claimed dopant concentration with a reasonable expectation of success. Ex.1003-Decl., ¶¶383-392; *supra* §X.C.1.i.

iii. Claim 10[b]

Cousins teaches *a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of the solar cell*. Cousins teaches a thin dielectric layer 107 formed over the back surface of the substrate 101 that “may comprise silicon dioxide thermally grown to a thickness of about 10 to 50 Angstroms.” Ex.1007-Cousins, 3:12-21, Fig.1. Ex.1003-Decl., ¶¶393-396.

iv. Claim 10[c]

Cousins in combination with Istratov teaches and renders obvious *a first emitter region having metal impurities formed over the dielectric region*.

Cousins teaches a “polysilicon layer 108” (Ex.1007-Cousins, 3:12-13), which has the same structure, arrangement, and function as the ’315 patent’s claimed “first emitter region.” *Supra* §X.A.2.iv. The polysilicon layer 108 is P-type doped and “formed on a thin dielectric layer 107,” as shown in Figure 1, and “has an emitter

saturation current of about $10 \text{ fA} \cdot \text{cm}^{-2}$.” Ex.1007-Cousins, 2:39-44, 3:12-13, Fig.1. Further, the polysilicon layer 108 “serv[es] as a P-type diffusion region” and forms a back side junction with the silicon substrate 101. *Id.*, 1:44-46, 2:39-42. Cousins thus teaches “a first emitter region ... formed over the dielectric region.” Ex.1003-Decl., ¶¶397-406.

As discussed above (§IX.E), Istratov teaches the accumulation of iron and copper (metal impurities) in the polysilicon layer during a heating step. As discussed above (§X.C.1.ii), a POSITA would have been motivated to combine Cousins with Istratov with a reasonable expectation of success. Ex.1003-Decl., ¶¶407-413.

v. Claim 10[d]

Choi teaches *a first metal contact formed over the first emitter region*. As explained above (§X.C.2.iv), a POSITA would have recognized that the claimed “first emitter region” corresponds to Cousins’ “polysilicon layer 108.” Cousins teaches a “metal contact 110” that “electrically connects to the polysilicon layer 108 through contact holes 123.” Ex.1007-Cousins, 3:20-24, Fig.1. As shown in Figure 1, metal contact 110 is formed over the polysilicon layer 108. *Id.*, Fig.1. A POSITA would have recognized the “metal contact 110” corresponds to the claimed “first metal contact.” Ex.1003-Decl., ¶¶414-417.

3. Claim 11

Claim 11 depends from claim 10. Petitioner incorporates Section X.C.2.

Cousins further teaches *the portion of the silicon substrate comprises N-type dopants*. As explained above (§X.C.2.ii), a POSITA would have recognized that Cousins’ doped region 105 is the claimed “portion of the silicon substrate.” Cousins further teaches that the silicon substrate 101 and the doped region 105 are both doped n-type. Ex.1007-Cousins, 2:44-55. Ex.1003-Decl., ¶¶418-419.

4. Claim 12

Claim 12 depends from claim 10. Petitioner incorporates Section X.C.2.

Cousins further teaches *the portion of the silicon substrate comprises phosphorus*. Cousins teaches that the “N-type doped region 105 may be formed by exposing [the solar cell] to phosphorus in the diffusion furnace during the drive-in step.” Ex.1007-Cousins, 5:60-63. Ex.1003-Decl., ¶¶420-421.

5. Claim 13

Claim 13 depends from claim 10. Petitioner incorporates Section X.C.2.

The combination of Cousins and Marvin further teaches *the portion of the silicon substrate comprises P-type dopants*. A POSITA would have understood that the teachings of Cousins are applicable to both n-type and p-type solar cells. Ex.1003-Decl., ¶¶422-424.

Marvin further teaches that the FSF region can be a heavily doped p⁺ region. Ex.1008-Marvin, 15. A POSITA would have understood that using a p-type FSF with a p-type substrate, as opposed to using an n-type FSF, is simply a design choice. Moreover, as of the filing date of the '315 patent, p-type wafers were more common and cheaper than n-type wafers. Thus, based on at least Marvin's teachings of a p-type FSF, and the common knowledge that a solar cell may be equally fabricated on a p-type or an n-type substrate, a POSITA would have been motivated to modify Cousins with Marvin's p-type front region with a reasonable expectation of success. The combination of Cousins and Marvin teaches and renders obvious claim 13. Ex.1003-Decl., ¶¶425-428.

6. Claim 14

Claim 14 depends from claim 10. Petitioner incorporates Section X.C.2.

As discussed in Section X.C.5, it would have been obvious to implement a p-type front region in Cousins' solar cell with a reasonable expectation of success. A POSITA would have understood that a p-type substrate may be fabricated by doping the substrate with boron, the most common dopant for p-type silicon. Ex.1003-Decl., ¶¶429-435.

Cousins further teaches *the portion of the silicon substrate comprises boron*. Cousins teaches diffusion of a p-type dopant source, borosilicate glass, into a layer

of the solar cell, the polysilicon layer 108. Ex.1007-Cousins, 4:54-55. A POSITA would have understood that using a p-type FSF with a p-type substrate, as opposed to using an n-type FSF, is simply a design choice. Moreover, as of the filing date of the '315 patent, p-type wafers were more common and cheaper than n-type wafers. Furthermore, a POSITA would have understood that boron is one of a limited number of elements for doping a region p-type. A POSITA would have understood that borosilicate glass diffusion, as in Cousins, was commonly used to dope regions of solar cell substrates with boron atoms, resulting in a substrate comprising boron. A POSITA would therefore have been motivated to modify Cousins by doping the front region of its silicon substrate with boron with a reasonable expectation of success. The combination of Cousins and Marvin teaches and renders obvious claim 14. Ex.1003-Decl., ¶¶429-435.

7. Claim 15

Claim 15 depends from claim 10. Petitioner incorporates Section X.C.2.

Cousins further teaches *the first emitter comprises polysilicon*. Cousins teaches that the “polysilicon layer 108” forms a back side junction with the silicon substrate 101 and “may be formed by forming a layer of polysilicon by Chemical Vapor Deposition ... and thermal anneal.” Ex.1007-Cousins, 1:44-46, 2:39-42, 3:12-17. Ex.1003-Decl., ¶¶436-437.

XI. DISCRETIONARY DENIAL IS NOT WARRANTED

A. *General Plastic*

Petitioner has diligently and independently prepared this Petition in response to Patent Owner’s recent patent infringement complaint against Petitioner. That complaint is part of an ongoing litigation campaign by Patent Owner. In response to another, earlier-filed lawsuit in this campaign, another accused infringer—CSI—filed separate IPR petitions challenging the ’315 patent. There is no basis for discretionarily denying this Petition based on CSI’s earlier-filed petitions because no relationship exists between Petitioner and CSI, this Petition raises different prior art and arguments, minimal time separates Petitioner and CSI’s petitions, and the petitions are timely, independent responses to Patent Owner’s litigation activities. As detailed below, each *General Plastics* factor weighs against discretionary denial or is neutral at best. *General Plastics Industrial Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19, at 9-10 (P.T.A.B. Sept. 6, 2017).

Factor 1 weighs strongly against denial. Petitioner did not file the previous petitions directed to the same patent. Nor is there any current relationship or communication about the asserted patents between Petitioner and CSI. Under these circumstances, discretionary denial is unwarranted unless supported by the other factors or if a “significant relationship” exists between the filers. *Illumina v. Ravgen*,

IPR2021-01271, Paper 12, at 14-15 (P.T.A.B. Jan. 26, 2022). Here there is no relationship—let alone a significant one—between CSI and Petitioner. Petitioner and CSI are competitors. The fact that Patent Owner has brought district court actions against both Petitioner and CSI does not support considering them related filers for purposes of discretionary denial. *Id.*, 16-17; *Signify N. Am. Corp. v. Cao Lighting, Inc.*, IPR2023-00214, Paper 4, 21 (P.T.A.B. June 15, 2023) (factor 1 “strongly weighs against discretionary denial” when subsequent petitioner has no relationship to first filer).

CSI and Petitioner are “direct competitors” and “unrelated companies,” and Patent Owner sued CSI and Petitioner in separate cases “over different alleged infringing products.” *Xilinx, Inc. v. Arbor Global Strategies LLC*, IPR2020-01568, Paper 12 at 9-10 (PTAB Mar. 5, 2021); *Twitter, Inc. v. Palo Alto Research Ctr. Inc.*, IPR2021-01459, Paper 11 at 33 (PTAB Apr. 6, 2022). This factor further “favors not exercising discretionary denial” because Petitioner and CSI did not coordinate in any way “in their respective petitions.” *Twitter* at 33. Petitioner did not seek to join CSI’s petitions (*Xilinx* at 9-10; *Twitter* at 32); in fact, joinder would not have been possible given that, as explained below, Petitioner has presented materially different challenges here. *See Facebook, Inc. v. Windy City Innovations, LLC*, 953 F.3d 1313, 1325 (Fed. Cir. 2020).

This Petition is based on different prior art and arguments than CSI's petitions, which did not cite five of the six references that form the bases for Petitioner's obviousness grounds here. *Compare* Ex.1063-CSI-1038-Petition, 5, *and* Ex.1076-CSI-1194-Petition, 3-4, *with* §§IX-X. For example, for limitation 10[d] (requiring, *inter alia*, "a first emitter region" having "metal impurities"), CSI relied on inherent obviousness based on a prior art reference disclosing heating above 900°C, which CSI argued results in "gettering of metal impurities." Ex.1063-CSI-1038-Petition, 45. This Petition instead relies on an explicit disclosure in the prior art of an emitter having metal impurities to meet limitation 10[d]. *Supra* §§X.A.2.iv, X.C.2.iv. Petitioner has also challenged additional claims (*i.e.*, claims 17, 18, and 20) that CSI's petitions did not challenge, another fact weighing against discretionary denial. *See Xilinx* at 10.

Factor 2 is neutral. When the second petition is filed by a different entity, as here, this "factor is inapplicable...and, therefore, is neutral." *Videndum Production Sols., Inc. v. Rotolight Ltd.*, IPR2023-01218, Paper 9, 11-12 (P.T.A.B. Jan. 25, 2024).

Factor 3 weighs against denial. Patent Owner has not submitted preliminary responses to CSI's petitions, nor has the Board issued institution decisions. Petitioner cannot have tailored its petition to either Patent Owner's arguments in CSI

petitions or reasoning by the Board. Thus, this factor weighs against denial. *Illumina*, Paper 12, 22-23.

Factors 4-5 weigh against denial. Petitioner’s timeliness in filing this petition after being accused of patent infringement strongly weighs against denial. Since learning of Patent Owner’s complaint, Petitioner moved expeditiously (and independently of CSI) to file this Petition. Where the Patent Owner sues multiple independent entities, “a few-months gap between the first Petition and the [second] Petition is not unreasonable,” even if Petitioner should have known about the prior art cited in CSI’s petition. *Illumina*, Paper 12, 21. Less than one month separates CSI’s latest petition and this Petition, even though Patent Owner sued CSI a month before Petitioner. Additionally, these factors should be given less weight because Petitioner is a different party than the earlier petitioner. *Illumina*, Paper 12, 20.

Factors 6-7 weigh against denial. The Board has adequate resources to timely address this Petition. Considering this Petition now will allow the Board to develop relevant substantive knowledge and minimize the resources needed to consider Petitioner’s and CSI’s distinct grounds. *Signify*, Paper 4, 23-24.

Moreover, “[d]enial of the Petition...w[ould] prejudice the Petitioner in this proceeding should the [CSI petitions] be resolved by settlement.” *Lowes Cos. Inc. v. Nichia Corp.*, IPR2017-02011, Paper 13, 19 (PTAB Mar. 12, 2018). This

potential prejudice weighs against denial. *Samsung Elecs. Co., v. Iron Oak Techs., LLC*, IPR2018-01554, Paper 9, 29 (PTAB Feb. 13, 2019).

Finally, the Board has recognized that discretionary denial is inappropriate when, as here, the filing of “multiple petitions...against the same patent is a direct result of Patent Owner’s litigation activity.” *Samsung*, IPR2018-01554, Paper 9, 29, 31. Accordingly, discretionary denial in view of CSI’s Petitions is improper.

B. 35 U.S.C. § 325(d)

Discretionary denial under § 325(d) is unwarranted because each *Advanced Bionics* factor weighs against denial. *Advanced Bionics v. MED-EL*, IPR2019-01469, Paper 6, 8-9 (P.T.A.B. Feb. 13, 2020). The Examiner erred during examination, and arguments presented in this Petition justify reconsideration of the claims. As discussed above (§VI.B), the Challenged Claims were immediately deemed allowable during prosecution without prior art rejections, remarks, or amendments to refine the scope of protection. Careful vetting of the ’315 patent did not occur during prosecution, and it is consistent with the AIA’s purpose to do so now.

Advanced Bionics factor 1 weighs against denial because this Petition presents prior art and arguments that were not previously considered. References introduced in this Petition—Choi, Cousins, Granek, Marvin, Istratov, and Smith—were not

disclosed or considered during prosecution of the '255 Application from which the '315 patent issued. Further, Choi, Granek, Marvin, Istratov, and Smith were not cited during prosecution of any of the four parent applications to the '255 Application.

Cousins was included in the Examiner's search history in a parent application (§VI.B), but that is not evidence that "the Examiner specifically addressed the substance of [that reference] during prosecution." *Google Inc. v. Blackberry Ltd.*, IPR2017-00912, Paper 7 at 21 (PTAB Aug. 30, 2017). There is no evidence in the record that Cousins was substantively evaluated during prosecution.

Even if *Advanced Bionics* factor 2 applies (it does not), it weighs against denial. This Petition presents additional evidence—Dr. Holman's declaration and other evidence regarding the scope of the prior art and knowledge of a POSITA—that was not previously before the Office. This evidence contextualizes the prior art in this Petition and explains why this art renders the Challenged Claims unpatentable. It thus weighs against denial. *TwinStrand Biosciences, Inc. v. Huardant Health, Inc.*, IPR2022-01400, Paper 9, 11 (P.T.A.B. Feb. 8, 2023).

C. *Fintiv*

No *Fintiv* factor favors discretionary denial. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 (P.T.A.B. May 13, 2020). The countdown to Petitioner's

one-year deadline for filing this Petition began only two weeks ago, on July 25, 2024, when the district court granted the parties' unopposed motion for waiver of foreign service. Petitioner filed this Petition expeditiously less than four months after Patent Owner filed suit in district court. Petitioner's response to the complaint is not due until November 22, 2024, and there is no current case schedule or trial date in the litigation. This Petition presents compelling merits, favoring institution.

XII. CONCLUSION

The Challenged Claims are rendered obvious by the foregoing grounds. Petitioner requests institution of *inter partes* review and cancellation of the Challenged Claims.

Respectfully submitted,

By: /David L. Cavanaugh/
David L. Cavanaugh
Registration No. 36,476

Counsel for Petitioner

Appendix of Claims

Claim 10	
Limitation	Claim Language
10[pre]	A solar cell, the solar cell having a front side which faces the sun during normal operation and a back side opposite the front side, the solar cell comprising:
10[a]	a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ and wherein the portion of the silicon substrate is formed at the front side of the solar cell;
10[b]	a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of solar;
10[c]	a first emitter region having metal impurities formed over the dielectric region; and
10[d]	a first metal contact formed over the first emitter region.

Claim 11
The solar cell of claim 10, wherein the portion of the silicon substrate comprises N-type dopants.

Claim 12
The solar cell of claim 10, wherein the portion of the silicon substrate comprises phosphorus.

Claim 13

The solar cell of claim 10, wherein the portion of the silicon substrate comprises P-type dopants.

Claim 14

The solar cell of claim 10, wherein the portion of the silicon substrate comprises boron.

Claim 15

The solar cell of claim 10, wherein the first emitter region comprises polysilicon.

Claim 16	
Limitation	Claim Language
16[pre]	The solar cell of claim 10, further comprising:
16[a]	a second emitter region having metal impurities formed over the dielectric region; and
16[b]	a second metal contact formed over the second emitter region.

Claim 17
The solar cell of claim 16, wherein the second emitter region is separate from the first emitter region.

Claim 18
The solar cell of claim 16, wherein a trench region separates the first emitter region from the second emitter region.

Claim 19
The solar cell of claim 16, wherein the second emitter region comprises polysilicon.

Claim 20
The solar cell of claim 16, wherein the first emitter region comprises a P-type doped polysilicon region and the second emitter region comprises a N-type doped polysilicon region.

CERTIFICATE OF COMPLIANCE

I hereby certify that the foregoing, Petition for *Inter Partes* Review, contains 13,975 words as measured by the word processing software used to prepare the document, in compliance with 37 C.F.R. §42.24(d), excluding the parts of the Petition exempted from the word count by 37 C.F.R. §42.24(a)(1).

/Alexander J. Nemtzow/
Alexander J. Nemtzow
Registration No. 82,130

CERTIFICATE OF SERVICE

Pursuant to an agreement between Petitioner and Patent Owner, I hereby certify that, on August 8, 2024, I caused a true and correct copy of the following materials:

- Petition for *Inter Partes* Review of U.S. Patent No. 11,251,315
- Appendix of Claims
- Petitioner's Table of Exhibits
- Exhibits 1001-1008, 1010-1049, 1051-1054, 1057-1066, 1068-1070, 1072-1084
- Certificate of Compliance Regarding Word Count
- Fee Authorization
- Power of Attorney

to be served on the Patent Owner's correspondence address listed on Patent Center (Schwabe Williamson & Wyatt/Maxeon, Pacwest Center, Suite 1900, 112 SW Fifth Avenue, Portland, OR 97204) via electronic mail to:

- | | |
|-----------------------|----------------------|
| • ccessna@velaw.com | • jswigart@velaw.com |
| • eshallman@velaw.com | • pwright@velaw.com |
| • hpreston@velaw.com | • eklein@velaw.com |

/Alexander J. Nemtzow/
Alexander J. Nemtzow
Registration No. 82,130

Petitioner’s Table of Exhibits

No.	Description
1001	U.S. Patent No. 11,251,315 B2 (“USP315”)
1002	File History for U.S. Patent No. 11,251,315 B2 (App. No. 16/877,255) (“USP315FH”)
1003	Declaration of Dr. Zachary Holman Regarding U.S. Patent No. 11,251,315
1004	Declaration of June Munford
1005	Complaint for Patent Infringement, <i>Maxeon Solar Pte. Ltd. v. Hanwha Solutions Corp., et al.</i> , Civil Action No. 2:24-cv-262 (E.D. Tex. Apr. 19, 2024), ECF No. 1 (“Complaint”)
1006	U.S. Patent App. Pub. No. 2014/0311567 (“Choi”)
1007	U.S. Patent No. 8,207,444 (“Cousins”)
1008	D.C. Marvin, S.L. Froedege, Interdigitated Back Contact Solar Cell Analysis and Design Recommendations for Space Use,” Space Systems Division Air Force Systems Command, Report 88D-TR-90-04 (“Marvin”)
1009	RESERVED
1010	F. Granek, High-Efficiency Back Contact Back-Junction Silicon Solar Cells (2009) (Ph.D. Dissertation, Fraunhofer Institute for Solar Energy Systems ISE) (“Granek”)
1011	U.S. Patent App. Pub. No. 2013/0240029 (“Smith”)
1012	A.A. Istratov, H. Väinölä, W. Huber, E. R. Weber, “Gettering in silicon-on-insulator wafers: experimental

No.	Description
	studies and modelling,” <i>Semicond. Sci. Technol.</i> 20: 568–575 (April 2005) (“Istratov”)
1013	EP1732142A1 (“Froitzheim”)
1014	JP07-106611 (“Okayasu”) (Translation)
1015	Translation Declaration for Okayasu
1016	N. G. Tarr, “A polysilicon emitter solar cell,” <i>IEEE Electron Device Letters</i> , vol. 6, no. 12, pp. 655-658, Dec. 1985 (“Tarr”)
1017	U.S. Patent No. 6,262,359 (“Meier”)
1018	Zachary C. Holman, <i>Electron Transport in Amorphous Silicon</i> (May 2005) (Thesis Presented to The Division of Mathematics and Natural Sciences, Reed College) (“Holman-Thesis”)
1019	P.J. Verlinden, R.A. Sinton, K. Wickham, R.A. Crane, and R.M. Swanson, “Backside-contact silicon solar cells with improved efficiency for the ’96 world solar challenge,” in <i>Proceedings of the 14th European Photovoltaic Solar Energy Conference</i> , Barcelona, Spain, 96-9 (1997) (“Verlinden”)
1020	R.A. Sinton and R.M. Swanson, “Simplified backside-contact solar cells,” <i>IEEE Transactions on Electron Devices</i> , 37 (2), 348-52, (1990) (“Sinton”)
1021	R.R. King, R.A. Sinton, R.M. Swanson, “Studies of Diffused Phosphorous Emitters: Saturation Current, Surface Recombination Velocity, and Quantum Efficiency,” <i>IEEE Transactions On Electron Devices</i> , Vol. 37, No. 2 (Feb. 1990) (“King”)

No.	Description
1022	W.P. Mulligan, D.H. Rose, M.J. Cudzinovic, D.M. De Ceuster, K.R. McIntosh, D.D. Smith, and R.M. Swanson, Manufacture of solar cells with 21% efficiency, in Proceedings of the 19th European Photovoltaic Solar Energy Conference, Paris, France, 387-90 (2004) (“Mulligan”)
1023	J. Nelson, The Physics of Solar Cells, Imperial College Press, Chapters 1, 3, 4, 7, 9, 10 (2003) (“Nelson”)
1024	R. F. Pierret, Semiconductor Device Fundamentals, Addison-Wesley Publishing Company, Inc., Excerpts from Chapters 1-4 (1996) (“Pierret”)
1025	S.J. Fonash, Solar Cell Device Physics, Elsevier, Excerpts from Chapter 2 (2d Ed. 2010) (“Fonash”)
1026	C. Hu, R.M. White, Solar Cells: From Basics to Advanced Systems, McGraw-Hill, Chapter 3 (1983) (“Hu”)
1027	O. von Roos, B. Anspaugh, “The Front Surface Field Solar Cell, A New Concept,” Proceedings of the 13th IEEE PVSEC, pp. 1119-1120 (1978) (“von Roos”)
1028	E. van Kerschaver, G. Beaucarne, “Back-contact Solar Cells: A Review,” Prog. Photovolt: Res. Appl. 14:107-123 (2005) (“van Kershaver”)
1029	U.S. Patent No. 8,222,516 B2 (“USP516”)
1030	U.S. Patent No. 4,234,352 (“Swanson-352”)
1031	J. Bultman, I. Cesar, B. Geerligs, Y. Komatsu, W. Sinke, “Methods of emitter formation for crystalline silicon solar cells,” Photovoltaics International 6, pp. 69-80 (2012) (“Bultman”)

No.	Description
1032	U.S. Patent No. 5,444,001 (“Tokuyama”)
1033	I. Perichchaud, “Gettering of impurities in solar silicon,” Solar Energy Materials & Solar Cells 72:315–326 (2002) (“Perichchaud”)
1034	Mark John Kerr, Surface, Emitter and Bulk Recombination in Silicon and Development of Silicon Nitride Passivated Solar Cells (2002) (Ph.D. Thesis, The Australian National University) (“Kerr”)
1035	U.S. Patent App. Pub. No. 2012/0006392 (“Gupta”)
1036	File History for US 9,520,507 B2 (App. No. 14/579,935) (“USPA935FH”)
1037	File History for US 9,899,542 B2 (App. No. 15/213,273) (“USPA273FH”)
1038	File History for US 10,170,642 B2 (App. No. 15/876,927) (“USPA927FH”)
1039	File History for US 10,658,525 B2 (App. No. 16/228,165) (“USPA165FH”)
1040	P. Procel, V. Maccaronio, F. Crupi, G. Cocorullo, M. Zanuccoli, “Analysis of the Impact of Rear Side Geometry on Performance of Back-Contact Back-Junction Solar Cells,” 2014 Fotonica AEIT Italian Conference on Photonics Technologies, Naples, Italy, 2014, pp. 1-4, IEEE (2014) (“Procel”)
1041	M. Hermle, F. Granek, O. Schultz, S. W. Glunz, “Analyzing the effects of front-surface fields on back-junction silicon solar cells using the charge-collection

No.	Description
	probability and the reciprocity theorem,” J. Appl. Phys. 103, 054507 (2008) (“Hermle”)
1042	J. E. Cotter, J. H. Guo, P. J. Cousins, M. D. Abbott, F. W. Chen, K. C. Fisher, “P-Type Versus n-Type Silicon Wafers: Prospects for High-Efficiency Commercial Silicon Solar Cells,” IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 8, (Aug. 2006) (“Cotter”)
1043	S.W. Glunz, R. Preu, D. Biro, “Chapter 1.16: Crystalline Silicon Solar Cells – State-of-the-Art and Future Developments,” Comprehensive Renewable Energy, Elsevier (2012)
1044	P.J. Verlinden, R. M. Swanson, R. A. Crane, “7000 High-efficiency Cells for a Dream,” Progress In Photovoltaics Research and Applications, VOL 2. 143-152 (1994) (“Verlinden-1994”)
1045	U.S. Patent No. 4,665,277 (“Sah”)
1046	M. Green, “Silicon solar cells: evolution, high-efficiency design and efficiency enhancements,” Semiconductor Science & Technology 8 (1993) (“Green”)
1047	A.A. Istratov, H. Hieslmair, E.R.Weber, “Iron contamination in silicon technology,” Appl. Phys. A 70, 489–534 (2000) (“Istratov-2000”)
1048	A. Metz, R. Meyer, B. Kuhlmann, M. Grauvogl, R. Hezel, 18.5% Efficient First-Generation MIS Inversion-Layer Silicon Solar Cells, 26th PVSC (1997) (“Metz”)
1049	D. De Ceuster, P. Cousins, D. Rose, D. Vicente, P. Tipones, W. Mulligan, “Low Cost, High Volume Production of >22% efficiency silicon solar cells,” 22nd European

No.	Description
	Photovoltaic Solar Energy Conference, 3-7 September 2007, Milan, Italy, pp. 816-819 (“De Ceuster”)
1050	RESERVED
1051	M.D. Lammert and R.J. Schwartz, “The interdigitated back contact solar cell: a silicon solar cell for use in concentrated sunlight,” IEEE Transactions on Electron Devices, ED-24 (4), 337-42, (1977) (“Lammert”)
1052	D. Lysáček, M. Lorenc, L. Válek, “Structure and gettering properties of polycrystalline silicon layers,” Proceedings of the 16th Joint Seminar Development of Materials Science in Research and Education, Czechoslovak Association for Crystal Growth, published by Czech and Slovak Crystallographic Association, Praha 2006 (ISBN 80-901748-7-6) p. 40-41 (“Lysacek”)
1053	K. Ishisaka, H. Tanaka, T. Nakashizu, “Gettering Properties of Silicon Wafer Covered by Polysilicon,” NIPPON STEEL TECHNICAL REPORT No. 59 (Oct. 1993) (“Nippon”)
1054	BP Solar Global Marketing, BP-MSX-120, 120-Watt Multicrystalline Photovolataic Module (“BP-MSX-120”)
1055 – 1056	RESERVED
1057	P. Stradins, A. Dameron, S. Essig, V. Lasalvia, B. Lee, Y. Liu, J. Luo, W. Nemeth, A. Norman, M. Page, “Passivated Tunneling Contacts to N-Type Wafer Silicon and Their Implementation into High Performance Solar Cells,” NREL Conference Paper (Dec. 2014) (“Stradins”)
1058	D. M. Chapin, C. S. Fuller, G. L. Pearson, “A New Silicon p-n Junction Photocell for Converting Solar Radiation into

No.	Description
	Electrical Power,” Journal of Applied Physics 25, 676 (1954) (“Chapin”)
1059	W. Shockley, H. J. Queisser, “Detailed Balance Limit of Efficiency of pn Junction Solar Cells,” J. Appl. Phys. 32, 510 (1961) (“Shockley”)
1060	A. Goetzberger, W. Shockley, “Metal Precipitates in Silicon p-n Junctions,” J. Appl. Phys. 31, 1821–1824 (1960) (“Goetzberger”)
1061	S.W. Ing, Jr., R.E. Morrison, L.L. Alt, R. W. Aldrich, “Gettering of Metallic Impurities from Planar Silicon Diodes,” J. Electrochem. Soc. Vol. 110, No. 6 pp. 533-537 (1963) (“Ing”)
1062	E. J. Mets, “Poisoning and Gettering Effects in Silicon Junctions,” J. Electrochem. Soc. Vol. 112, No. 4, pp. 420-425 (1965) (“Mets”)
1063	Petition for Inter Partes Review of U.S. Patent No. 11,251,315, Canadian Solar Inc. v. Maxeon Solar Pte. Ltd., Case No. IPR2024-01038, Paper 1 (June 25, 2024) (“CSI-1038-Petition”)
1064	A. A. Istratov, W. Huber, E. R. Weber, “Experimental evidence for the presence of segregation and relaxation gettering of iron in polycrystalline silicon layers on silicon,” Appl. Phys. Lett. 85, 4472–4474 (2004) (“Istratov-2004”)
1065	KR1020130044982 (“Choi-982”) (Translation)
1066	Translation Declaration for Choi-982
1067	RESERVED

No.	Description
1068	U.S. Patent No. 6,998,288 (“Smith-288”)
1069	CN 1949545A to Li (“Li”) (Translation)
1070	Translation Declaration for Li
1071	RESERVED
1072	R. J. Komp, Practical Photovoltaics Electricity From Solar Cells, 3rd Ed., Chapters 1-3, 6 (2002) (“Komp”)
1073	T. Krygowski, A. Rohatgi, D. Ruby, Simultaneous P and B Diffusion, IN-SITU Surface Passivation, Impurity Filtering and Gettering for High-Frequency Silicon Solar Cells, 26 IEE Photovoltaic Specialists Conf. 29 September - 03 October, 1997 Anaheim, CA (1997) (“Krygowski”)
1074	J. Benick, J. Rentsch, Ch. Schetter, C. Voyer, D. Biro, R. Preu, PECVD PSG as a Dopant Source for Industrial Solar Cells, Presented at the 21st European Photovoltaic Solar Energy Conference, September 4-8, 2006, Dresden (2CV.4.26) (“Benick”)
1075	M. Green, Silicon Solar Cells Advanced Principles & Practice, Centre for Photovoltaic Devices and Systems, Chapters 2, 10 (1995) (“Green-1995”)
1076	Petition for Inter Partes Review of U.S. Patent No. 11,251,315, Canadian Solar Inc. v. Moxeon Solar Pte. Ltd., Case No. IPR2024-01194, Paper 1 (July 19, 2024) (“CSI-1194-Petition”)
1077	B. Paudyal, Y. H. Yoon, D. Cornwell, P. Shaw, F. Machuca, “Identification of metal impurities in crystalline silicon wafers,” IEEE (2011)

No.	Description
1078	S. Pizzini, M. Acciarri, S. Binetti, “From electronic grade to solar grade silicon: chances and challenges in photovoltaics,” <i>phys. stat. sol. (a)</i> 202, No. 15, 2928–2942 (2005) (“Pizzini”)
1079	U.S. Patent No. 9,496,437 (“Harley”)
1080	U.S. Pat. App. Pub. No. 2013/0164879 (“Cousins-2011”)
1081	“Cypress Announces Investment In Designer and Manufacturer Of Ultra-High-Efficiency Silicon Solar Cells” available at https://investors.sunpower.com/static-files/103bae51-d5a4-46f3-ae4c-efc7d65b968a (last accessed Aug. 6, 2024) (“Sunpower-2002”)
1082	“SunPower Announces World’s Most Efficient, Low-Cost Silicon Solar Cell” available at https://investors.sunpower.com/static-files/4e352cd3-71ed-45ca-a441-165e996c8222 (last accessed Aug. 6, 2024) (“Sunpower-2003”)
1083	D.P. Fenning, A.S. Zuschlag, M.I. Bertoni, B. Lai, G. Hahn and T. Buonassisi, Improved iron gettering of contaminated multicrystalline silicon by high-temperature phosphorus diffusion, <i>Journal of Applied Physics</i> , 113, 214504 (2013) (“Fenning”)
1084	D.H. Neuhaus and A. Munzer, “Industrial Silicon Wafer Solar Cells,” <i>Advances in OptoElectronics</i> , Vol. 2007, Article ID 24521, 1-15 (2007) (“Neuhaus”)