

IMPACT OF METAL CONTAMINATION OF 7.0nm GATE OXIDES ON VARIOUS SUBSTRATE MATERIALS

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ABSTRACT

Metal contamination level will be decreased in order to maintain a device reliability according to device size reduction. Metal contamination from various processes are surveyed. The influence of metal contamination for 7-15nm thick gate oxides is discussed in order to clarify the critical concentration to gate oxides. NIG(Non Intrinsic Gettering) substrates are used in a worst case for gettering. Fe contamination with $4 \times 10^{10} \text{ cm}^{-2}$ strongly affects the TDDM characteristics, although there is no serious influence in the breakdown voltage even at the concentration of $5 \times 10^{11} \text{ cm}^{-2}$. The same tendency is observed for Cu contaminant and the critical concentration for TDDDB characteristics is around $3 \times 10^{11} \text{ cm}^{-2}$. High energy B implantation is carried out to form gettering sites near device region. Breakdown voltage and TDDDB characteristics are almost the same as epitaxial substrates at Fe concentration up to $1 \times 10^{12} \text{ cm}^{-2}$. Detailed examination such as SIMS, C-t and DLTS measurements is also supported the effectiveness in high energy gettering.

INTRODUCTION

In sub-quarter micron devices or below, critical metal contamination level to affect device performance will become lower because of thinner gate oxide films, increase of local stress, etc. In order to overcome this, not only the reduction of metal contamination from processes but also the improvement of gettering must be done.

In this paper, firstly, metal contamination level introduced and/or affected from process machines, materials and chemicals will be surveyed. Metal influences to devices will be discussed using non-intrinsic gettering(NIG) substrates for the worst case. Then, metal gettering effect using high energy implantation will be presented.

METAL CONTAMINATION LEVEL

The source of metal contaminants are mainly categorized in three factors; process machines, materials and chemicals & gases. In the process machines, most possible process for metal contamination are ion implantation, CVD and dry etching and metal contamination level exists around 2×10^{10} to $1 \times 10^{11} \text{ cm}^{-2}$ for Fe, Cu and Ni. For materials, metal contamination level was examined in photoresist[1]. Metals such as Fe, Cu, Cr and Ni existed on Si surfaces at a level below $2 \times 10^{10} \text{ cm}^{-2}$ just after ashing and ashing +cleaning. For chemicals, metal contamination in chemicals is quite low and the level is about 0.01ppb for SC-1 solution. This level itself is not so serious in chemical solutions, instead the problem is the recontamination to wafers from chemical solutions, because metals are piled-up in the chemical solutions after wafer cleaning. This influence was examined in details[2]. When Fe existed in SC-1 solutions at a level of 0.1ppb and 1ppb, Fe concentration on Si surfaces was around $1 \times 10^{11} \text{ cm}^{-2}$ and $1 \times 10^{12} \text{ cm}^{-2}$, respectively. According to this result, metal concentration is estimated to be a level of about 0.4ppb in solutions after cleaning of 25 wafers of 8 inch in 40 liter solution, when Fe atoms with the concentration of $1 \times 10^{13} \text{ cm}^{-2}$ are soluble in the solution. This corresponds to a level of about $5 \times 10^{11} \text{ cm}^{-2}$. However, when SC-2 or HF solution is used instead of the SC-1 solution, surface concentration is constant and low at the level of $1 \times 10^{10} \text{ cm}^{-2}$ for metal concentration ranging from 0.1 to 100ppb in the solution. Thus, metal recontamination from chemical solutions can be reduced by the combination of chemical cleaning process using different pH solutions. Since metal contamination from materials and chemicals is not so serious at this moment from these results, metal contamination from process machines should be reduced in order to maintain reliability in advanced devices.

INFLUENCE OF METAL CONTAMINATION TO DEVICES

Metal contaminants induce the degradation of device performance such as gate oxide, junction leakage current and carrier life time. Since the gate oxide thickness will become thinner below 6nm, metal contamination will be crucial because of tunneling through metal state. In junction leakage current, the influence of local stress will be increased by the change of the isolation structure from LOCOS to trench. In this paper, gate oxide reliability is focused.

In order to clarify the influence of metal contaminants, gate oxide reliability was examined using 6 inch p-type NIG(Non Intrinsic Gettering) substrates with resistivity of $15 \Omega \text{ cm}$. Since NIG substrates have weak or no gettering capability, metal contaminants influence is evaluated directly, so this evaluation is the worst case for the influence of metal contaminants. Breakdown voltage and TDDB characteristics were measured in the 8-15nm thick gate oxide films, which were formed just after intentional metal contamination by dipping. The control of metal concentration on Si surfaces is very important, especially at a low concentration level. In order to control the metal concentration on Si surfaces, wafers were pre-oxidized(sacrificial oxidation) and then, the oxide films were removed by HF solutions. Then, pH controlled solutions including Fe or Cu were used at room temperature in order to

control low metal concentration. pH control in the solution was carried out by adjusting ammonia and nitric acid. Surface metal concentration was quantified using Vapor-Phase-Decomposition Atomic-Absorption-Spectroscopy(VPD-AAS). By using this technique, the Fe or Cu concentration ranging from $1 \times 10^{10} \text{ cm}^{-2}$ to $1 \times 10^{12} \text{ cm}^{-2}$ can be controlled by the pH controlled chemical solution[3]. After, gate oxide films were grown at the thickness of 8nm, phosphorous doped poly-Si films were fabricated for gate materials. 1 mm^2 diodes from 100 chips/wafer were evaluated for breakdown voltage with breakdown current of 0.1 mA/cm^2 and 0.1 mm^2 diodes from 80 chips/wafer were used for TDDB measurement at room temperature with stress current of $-10 \mu \text{ A/cm}^2$.

Gate oxide breakdown voltage and TDDB characteristics were evaluated[3] for intentional Fe contamination. Figure 1 shows the results on the breakdown voltage at the gate oxide thickness of 8 and 15nm. The results of breakdown voltage seems to be good at the concentration below $5 \times 10^{11} \text{ cm}^{-2}$.

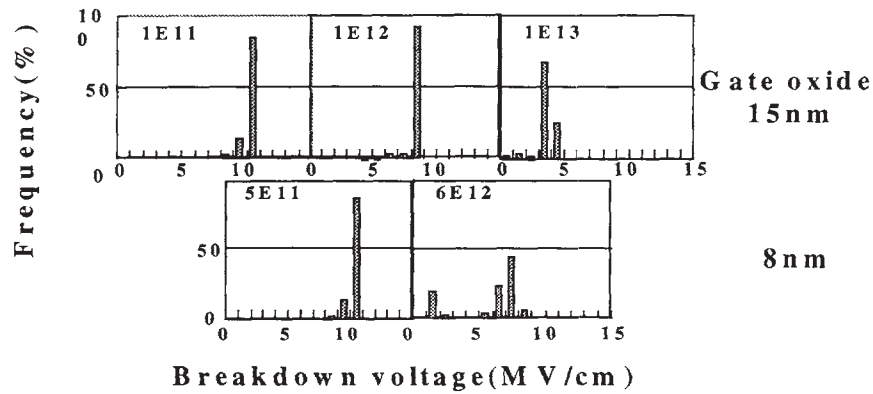


Figure1. Evaluation of gate oxide breakdown voltage.

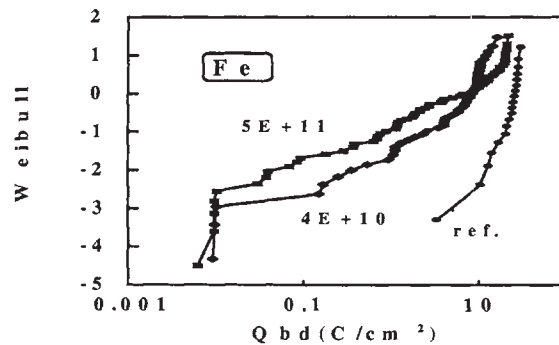


Figure2. TDDB characteristics of 8nm thick gate oxide films.

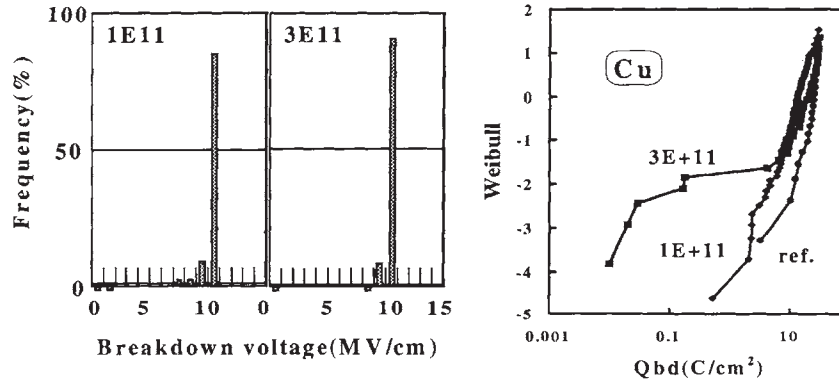


Figure 3. Evaluation of 8nm thick gate oxide for Cu contamination.

However, TDDB measurement indicates the degradation of thin gate oxide films even at the concentration of $4 \times 10^{10} \text{ cm}^{-2}$, as shown in Fig.2. Characteristics of breakdown voltage is quite good even at the concentration of $5 \times 10^{11} \text{ cm}^{-2}$, nevertheless TDDB characteristics becomes worse and worse, according to the Fe concentration increases. This means that Fe concentration of $4 \times 10^{10} \text{ cm}^{-2}$ is not acceptable for 8nm thick gate oxide films, when gettering is not effective in the use of NIG substrates. So, Fe contaminant should be decreased for safety. On the other hand, the influence of Cu contamination seems to be different for Fe contamination. Figure 3 shows the results of breakdown voltage and TDDB characteristics for Cu contamination. Characteristics of breakdown voltage is quite good even at the Cu concentration below $3 \times 10^{11} \text{ cm}^{-2}$. Degradation of TDDB characteristics is observed at the concentration above $3 \times 10^{11} \text{ cm}^{-2}$. Critical concentration to affect the gate oxide performance is quite different for metals and it seems to exist around $4 \times 10^{10} \text{ cm}^{-2}$ and $3 \times 10^{11} \text{ cm}^{-2}$ for

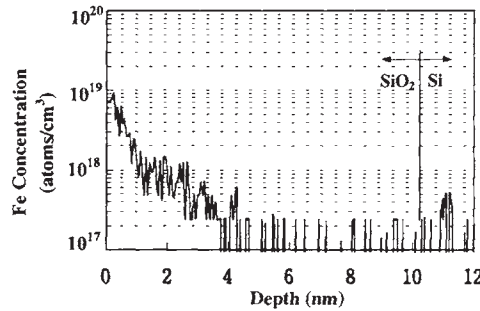


Figure 4. Fe SIMS profile in the gate oxide for Fe contamination.

Fe and Cu contamination, respectively. One possible reason for different critical concentration for different metals is the existence of metal in the gate oxide films. Figure 4 shows the SIMS profile of Fe in the gate oxide film formed just after Fe dipped wafer at the concentration of $1 \times 10^{12} \text{ cm}^{-2}$. Fe atoms existed at the top of the gate oxide film. This suggests that oxidation of Si surface occurred through Fe atoms, and thus Fe atoms existed at the top of the gate oxide film. On the other hand, Cu atoms can not be observed in the gate oxide film. This suggests that Cu atoms diffuses and does not pile up at the gate oxide film.

HIGH ENERGY GETTERING

When there does not exist gettering sites in Si Substrates, metal contamination is very critical even at a low metal concentration. In order to improve and increase a critical concentration, gettering is effective and controllable depending on device processes. In the advanced devices, thermal stress will be reduced to suppress the dopant diffusion, metal reaction, etc. And also, the use of larger diameter wafer such as 300mm diameter will be considered. Thus, introduction of RTA and low temperature process in heating cycles is strongly required. In this case, diffusion of contaminated metal atoms are strictly limited and the chance to getter at the sites decreases. Therefore, gettering sites formation near device region is important in the near future. One of the method is to use high energy implantation for the formation of gettering sites[4] in Si substrates.

Figure 5 shows the schematic diagram of the structure used for high energy gettering[5]. High energy B ions were implanted in Fz substrates(oxygen concentration is low and gettering sites does not exist at all) at 2.4 MeV with a dose of $1 \times 10^{15} \text{ cm}^{-2}$, followed by annealing at 950°C for 30 minutes and then, MOS capacitors were fabricated using standard LOCOS process. Before gate oxide formation, Fe ions were implanted at 500keV with a dose of $1 \times 10^{12} \text{ cm}^{-2}$ in Fz substrates from backside of the

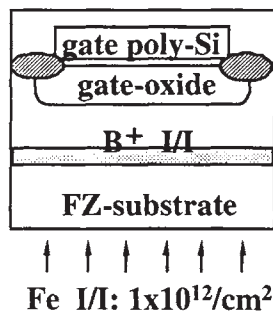


Figure 5. Schematic diagram of sample structure

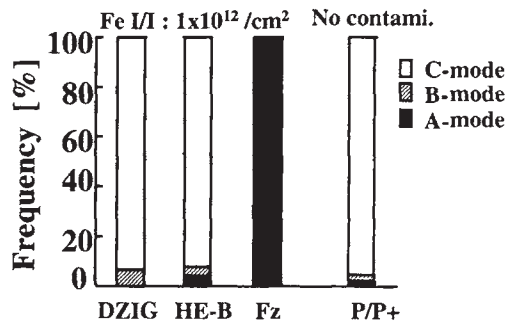


Figure 6. Yield of breakdown voltage

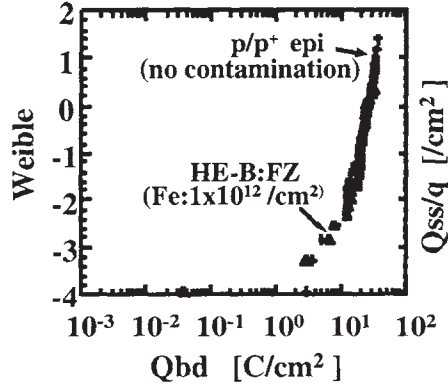


Figure 7. TDDM characteristics

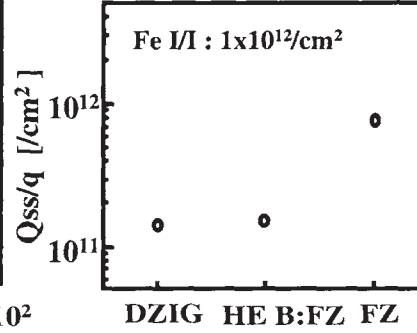


Figure 8. Interface state density for Fe contamination

wafers, followed by annealing at 1000°C for 1 hour to diffuse Fe atoms entirely in substrates. Then, 7 nm thick gate oxide films were formed. Figure 6 shows the yield of A-mode ($\leq 3\text{MeV}$), B-mode (3-8MeV) and C-mode ($\geq 8\text{MeV}$) in the gate oxide breakdown voltage. Four kind of different substrates were used; DZIG, Fz and Fz with high energy B implant in case of Fe contamination and also P on P⁺ epi in case of an uncontaminated reference. In Fz wafers, 100% A-mode failure was obtained for Fe concentration of $1 \times 10^{12}\text{cm}^{-2}$, because of no gettering sites in Si Substrates. On the other hand, yield of DZIG and high energy implanted Fz substrates for Fe contamination is the same as that of uncontaminated, clean epi substrates. In order to evaluate the gate oxide characteristics in detail, TDDM measurement was carried out for high energy implanted Fz substrates and clean, uncontaminated epi substrates. The result is shown in Fig.7. No difference is observed in the TDDB

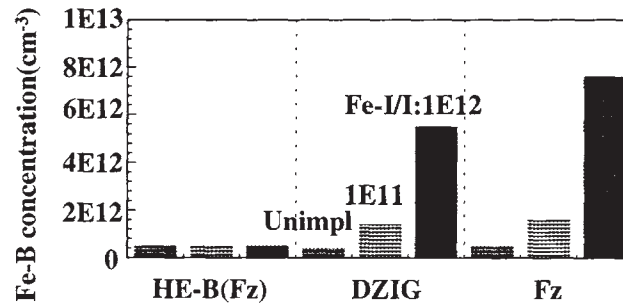


Figure 9. Fe-B pair concentration measured by DLTS

characteristics. From these results, the performance of high energy implanted Fz substrates seems to be the same as that of epi substrates. In Fz substrates contaminated by Fe implant, SIMS measurement suggests that Fe atoms existed around the gate oxide films and thus, gate oxide thickness increased to about 10nm. This is the main cause of A-mode failure. Figure 8 shows the interface state density at the gate oxides for Fe contamination using C-t method. High interface state density was observed in Fz substrates, although one order of magnitude smaller interface state density was obtained in DZIG and high energy implanted Fz substrates. This means that Fe atoms were effectively gettered in substrates. In order to show this more clearly, DLTS measurement was carried out, as shown in Fig.9. In Fz substrates, Fe-B pair concentration for Fe unimplantation is the background level and the concentration increases according to the increase of Fe concentration. Therefore, some of Fe atoms were gettered in the substrates by pairing with B. The same tendency was observed in DZIG substrates. Since the excess Fe atoms above solid solubility can be gettered in DZIG substrates, soluble Fe atoms are gettered by Fe-B pair. On the other hand, background level of Fe-B pair concentration is observed at the Fe concentration up to $1 \times 10^{12} \text{cm}^{-2}$ in the high energy B implanted Fz substrates, because Fe atoms are gettered in the implanted B to form Fe-B pairs. This is the same tendency as p/p⁺ epitaxial substrates. These results suggest that high energy B implanted substrates has a strong gettering capability and the electrical performance of gate oxides in high energy B implant is the same as epitaxial substrates.

CONCLUSIONS

Metal contamination during semiconductor processes was surveyed. The influence of metal contaminants to the gate oxide was examined in detail and critical metal concentration was estimated using NIG substrates. Critical concentration For Fe and Cu was around 4×10^{10} and $3 \times 10^{11} \text{cm}^{-2}$, respectively for 8nm thick gate oxide films. Effective gettering method using high energy implantation was proposed. Breakdown voltage and TDDB characteristics in high energy B implanted Fz substrates with Fe contamination of $1 \times 10^{12} \text{cm}^{-2}$ were the same as that in p/p⁺ epitaxial uncontaminated substrates. The detailed experiment using SIMS, C-t and DLTS measurements suggests the effective gettering in high energy B implanted substrates.

ACKNOWLEDGMENTS

Authors gratefully acknowledge T.Hayashi, M.Tanaka, S.Yamasaki, M.Nakamori and N.Aoto for sample fabrication, measurement and discussions. Authors also thank to Drs.O.Mizuno, K.Okada, M.Nakamae, K.Ikeda and M.Fukuma for discussions and encouragement.

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