

UNITED STATES PATENT AND TRADEMARK OFFICE

- - -

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Hanwha Solutions Corporation

v.

Maxeon

Inter Partes Review

No. IPR2024-01198

U.S. Patent No. 11,251,315

Petitioner's Oral Argument – December 3, 2025

Proposed Agenda

- Grounds
- Challenged Claims of the '315 Patent
- Claim 10 – Issues
 1. Claim Construction of “Metal Impurities”
 2. Gettering of “Metal Impurities”
 3. Dopant Concentration
- Dependent Claims 13-14 & 18 – Issues

Grounds

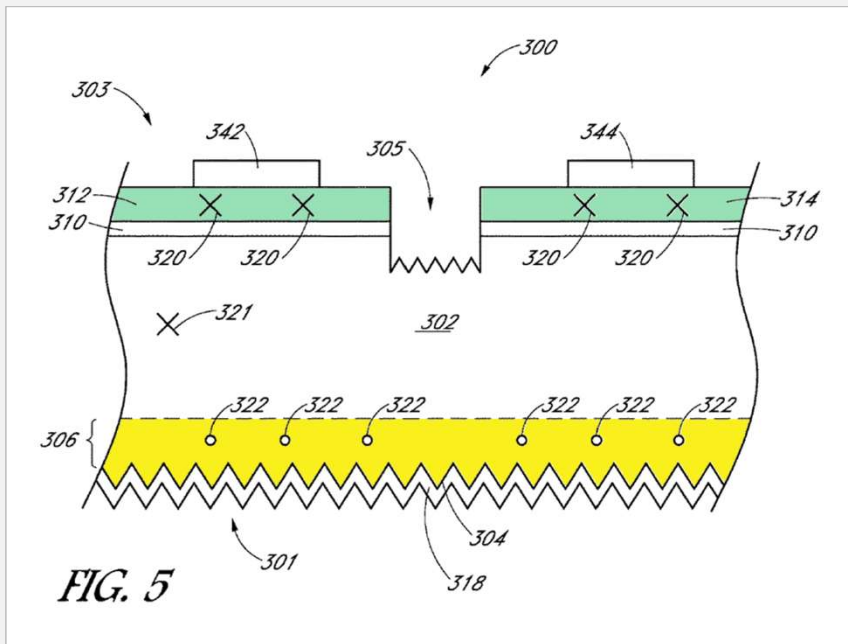
IPR Grounds and Challenged Claims

Claims(s) Challenged	35 U.S.C. §	Reference(s)/Basis
10-17, 19-20	103	Choi, Granek or Marvin, Istratov
18	103	Choi, Granek or Marvin, Istratov, Smith
10-15	103	Cousins, Granek or Marvin, Istratov

Paper 3 (Petition), 7, 35-78

Claim 10 of the '315 Patent

First Emitter Region – Metal Impurities and Dopant Concentration



10. A solar cell, the solar cell having a front side which faces the sun during normal operation and a back side opposite the front side, the solar cell comprising:

a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ and wherein the portion of the silicon substrate is formed at the front side of the solar cell;

a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of solar;

a first emitter region having metal impurities formed over the dielectric region; and

a first metal contact formed over the first emitter region.

Ex.1001-USP315, Claim 10 & Fig.5 (annotated)

Disputed Issues (Grounds I & III)

“Metal impurities” limitation:

- 1 Claim construction for “metal impurities” (Ground I)
 - 2 Obviousness of implementing gettering to move “metal impurities” into “emitter regions” (Grounds I & III)
-

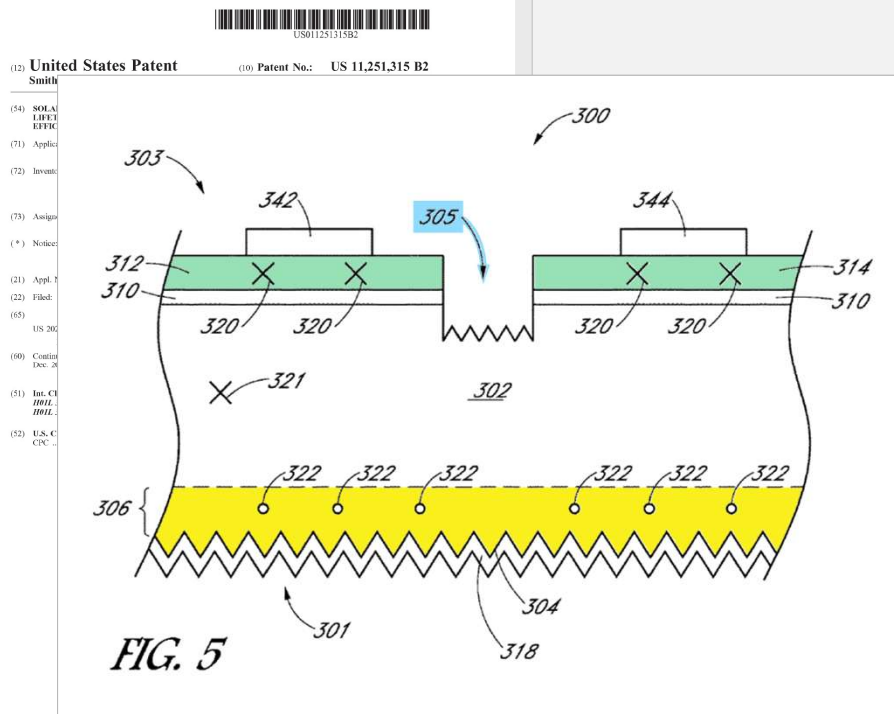
“Dopant concentration” limitation:

- 3 Obviousness of implementing claimed “dopant concentration” in “front” “portion of silicon substrate” (Grounds I & III)

Dependent Claims of the '315 Patent

Dependent Claims – Second Emitter Region and Trench

'315 Patent



13. The solar cell of claim 10, wherein the portion of the silicon substrate comprises P-type dopants.

14. The solar cell of claim 10, wherein the portion of the silicon substrate comprises boron.

16. The solar cell of claim 10, further comprising:
a second emitter region having metal impurities formed over the dielectric region; and
a second metal contact formed over the second emitter region.

18. The solar cell of claim 16, wherein a trench region separates the first emitter region from the second emitter region.

Ex.1001-USP315, Claims 13, 14, 16, 18 & Fig.5 (annotated)

Disputed Issues for Dependent Claims 13, 14, 18

1. **Obviousness of implementing p-type dopants**
(Claims 13, 14) (Grounds I & III)
2. **Obviousness of implementing a trench**
(Claim 18) (Ground II)

Differences Between Hanwha IPR and Canadian Solar IPR Nos. 2024-01038, -01194

- Different arguments: inherency of metal impurities
- No overlapping primary references
- Non-overlapping claims 17, 18, and 20
- Only one overlapping secondary reference

“Metal Impurities” Limitation

Choi Discloses “Metal Impurities” Under the Plain and Ordinary Meaning

(19) United States
(12) Patent Application Publication
Choi et al.

(10) Pub. No.: US 2014/0311567 A1
(45) Pub. Date: Oct. 23, 2014

(54) SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

(71) Applicant: LG Electronics Inc., Seoul (KR)

(72) Inventors: Minho Choi, Seoul (KR); Hyunjung Park, Seoul (KR); Jongbeom Choi, Seoul (KR)

(73) Assignee: LG Electronics Inc., Seoul (KR)

(21) Appl. No.: 14/258,638

(22) Filed: Apr. 22, 2014

(30) Foreign Application Priority Data
Apr. 23, 2013 (KR) 10-2013-0044982

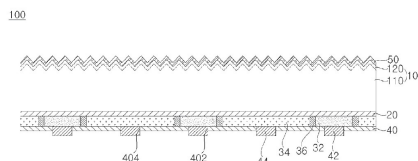
Publication Classification

(51) Int. Cl. H01L 31/0216 (2006.01)
H01L 31/18 (2006.01)

(52) U.S. Cl. H01L 31/02167 (2013.01); H01L 31/18 (2013.01)
CPC 136/258; 136/252; 136/261; 438/57

USPC

(57) ABSTRACT
A solar cell includes a semiconductor substrate, a tunneling layer on one surface of the semiconductor substrate, a first conductive type area on the tunneling layer, a second conductive type area on the tunneling layer such that the second conductive type area is separated from the first conductive type area, and a barrier area interposed between the first conductive type area and the second conductive type area such that the barrier area separates the first conductive type area from the second conductive type area.



HANWHA 1006

[0037] The second conductive type area **34** may include a semiconductor (for example, silicon) having a conductive type opposite to the semiconductor substrate **10**. The second

In this case, the second conductive type dopant may be any impurity having a conductive type opposite to the semiconductor substrate **10**. That is, when the second conductive type dopant is a p-type dopant, a Group III element such as boron (B), aluminum (Al), gallium (Ga) or indium (In) may be used. When the second conductive type dopant is an n-type dopant, a Group V element such as phosphorus (P), arsenic (As), bismuth (Bi) or antimony (Sb) may be used. The second

Ex.1006-Choi, ¶[0037] (annotated)

Paper 3 (Pet.), 54-55, 59; Ex.1003-Decl., ¶¶ 267-68;
Paper 36 (Reply), 2-10; Ex.1089-Reply-Decl., ¶¶ 41-42

Choi Discloses “Metal Impurities” Under the Plain and Ordinary Meaning



Fred Schubert, Ph.D.
Maxeon's Expert

- Q. You would agree that in Paragraphs 36 and 37, Choi discloses intentional foreign metallic atoms in the first and second conductive type areas, correct?
- A. I would say it discloses doping atoms. I'm not sure if I would call it – you know, **you can call it foreign atoms, if you wish**. But I think in order to use a terminology that is constructive, that is helpful, it would be better if you would say that **Choi discloses doping impurities, and some of these doping impurities are metals, specifically aluminum and gallium and indium**. I think that is a fair characterization.

Ex.1090-Schubert-Tr., 94:20-95:10

Claim Construction for “Metal Impurities” (Ground I)

Claim 10 – Issues

1. Claim Construction of “Metal Impurities”

2. Gettering of Metal Impurities

3. Dopant Concentration

The Plain Meaning of “Impurities” Includes Intentionally Introduced Dopants

Dr. Holman

For example, in a silicon wafer, a POSITA at the time of the alleged invention would have understood the term “impurity” to mean any non-silicon atom, including intentionally introduced dopants. Ex.2037-Holman-Tr., 110:19-111:4; 113:18-

Case No. IPR2024-01198
U.S. Patent No. 11,251,315

REPLY DECLARATION OF DR. ZACHARY HOLMAN
REGARDING U.S. PATENT NO. 11,251,315

HANWHA v. MAXEON
IPR2024-01198
HANWHA 1089

Ex.1089-Reply-Decl., ¶23 (annotated)

Dr. Schubert

Doping in III-V Semiconductors

E. Fred Schubert
AT&T Bell Laboratories



Thus, the term ‘impurities’ is used for unintentional as well as intentional foreign atoms in the semiconductor, while the term ‘dopants’ is used exclusively for deliberately added impurities.

CAMBRIDGE
UNIVERSITY PRESS

Page 1 of 10

Published online by Cambridge University Press

HANWHA v. MAXEON
IPR2024-01198
HANWHA 1105

Ex.1105-Schubert-1993, at xvi (annotated)

Paper 36 (Reply), 3

The Plain Meaning of “Impurities” Includes Intentionally Introduced Dopants

WILEY ELECTRICAL AND
ELECTRONICS ENGINEERING
DICTIONARY

impurity 1. A substance whose presence within another reduces or eliminates the purity of the latter ... 2. An **impurity (1)** which is introduced into a semiconductor material. Such an impurity may be an acceptor impurity, which makes for a p-type semiconductor, or it may be a donor impurity, which makes for an n-type semiconductor ... **Also called dopant, or semiconductor dopant.**

Ex.1109-Wiley-Dictionary,
363-364 (annotated)

McGraw-Hill
Dictionary
of
SCIENTIFIC

impurity [SCI TECH] An undesirable foreign material in a pure substance.
[SOLID STATE] A substance that, when diffused into semiconductor metal in small amounts, either provides free electrons to the metal or accepts electrons from it.

Sixth Edition

Ex.2030-McGraw-Hill-Dictionary,
1058 (annotated)

A Dictionary of
**Electronics
and Electrical**

impurities Foreign atoms in a semiconductor that are either naturally occurring **or deliberately introduced**. Impurities have a fundamental effect on the type and amount of conductivity of the semiconductor.

OXFORD
UNIVERSITY PRESS
HANWHA v. MAXEON
IPR2024-01198
HANWHA 1108

Ex.1108-EE-Dictionary, 299 (annotated)

Paper 36 (Reply), 2-3

“Impurities” Should Be Given Its Plain and Ordinary Meaning



Fred Schubert, Ph.D.

Maxeon's Expert

Q. Your belief is that the term impurities, as used in the '315 patent, should be construed according to its plain and ordinary meaning, correct?

A. **I believe that the term should be construed by its plain and ordinary meaning in the context of the '315 patent.**

Ex.1090-Schubert-Tr., 81:12-18

Paper 36 (Reply), 4 n.2

The '315 Patent Applicant Did Not Dispute That Intentionally Introduced Metallic Dopants Are “Metal Impurities”

PTQSB413C 005-113

Claim 1, Yelundur , (figs. 1 – 6 and all relevant texts), the solar cell (solar cell 5, fig. 5), discloses a solar cell having a front side which faces the sun during normal operation (side facing light) and a back side (45) opposite the front side, the solar cell comprising: a dielectric region over a silicon substrate ([0026, 0027]), wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ ("10E14 – 10E17" [0040, 0053]); a first emitter region (layer 15 [0055, 0061]) having me

The information is required to obtain a debt collection benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 hours (and, by the applicant, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and any suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form call 1-800-PTO-9199 and select extension 2.

HANWHA 1036

Ex.1036-USPA935FH, 76
Paper 36 (Reply), 6-7

		 US 2013027991A1	
(18) United States Patent Application YELIUNDELL FABRICATION		(36) Pub. No.: US 2013/0274981 A1 (44) Pub. Date: Sep. 26, 2013	
(54) SOLAR CELL FABRICATION USING A PRE-DOPED DIELECTRIC LAYER		(52) U.S. CL. USPC 438/256; 438/259; 438/257; 438/121	
(57) Inventors: YILIAO YELIUNDELL, CANTON, GA (US); ATEEL GOPPA, INDIANAPOLIS, IN (US); JASSEN MOFFITT, INDIANAPOLIS, IN (US); CHRIS, GA (US)		ABSTRACT	
(51) Assignee: SUNIVA, INC., NORCROSS, GA (US)		Solar cells, solar modules, and methods for their manufacture	

[0040] According to the embodiment of FIG. 5, the substrate may be doped with **impurities** of a first conductivity type. For example, in some embodiments, p-type **impurities** may be used to create a p-type base layer **10**. The p-type base layer **10** may be doped with boron (B), **gallium (Ga)**, **indium (In)**, **aluminum (Al)**, or possibly another Group III element to produce p-type conductivity. In other embodiments, the substrate may be doped with phosphorus (P), antimony (Sb), arsenic (As) or other Group V element to induce n-type conductivity, thereby forming an n-type base layer **10**. In some embodiments, the dopant concentration may be in a range from 10^{14} to 10^{17} atoms per cubic centimeter (atoms/cm³) for a p-type base layer **10** or in a range from 10^{13} to 10^{17} atoms per cubic centimeter (atoms/cm³) for an n-type base layer **10**.

Ex.1110-Yelundur, $\nabla[0040]$ (annotated)

The '315 Does Not Define “Metal Impurities” in Claims 10 and 16 to Mean Only “Contaminants”

In an example, impurities and/or contaminants 520, e.g. metal impurities and/or contaminants, can be located in the

In an example, impurities and/or contaminants 420, e.g. metal impurities and/or contaminants, can be located in the

of the solar cell. In an embodiment, the heating can include gettering contaminants, e.g. metal impurities and/or metal contaminants, from the substrate to the emitter region. In an example, the metal impurities and/or metal contaminants can be iron, nickel and/or chromium among others.

Ex.1001-USP315, 5:35-39, 7:48-49, 8:15-16 (annotated)
Paper 36 (Reply), 4-5

(12) United States Patent
Smith et al.

(10) Patent No.: US 11,251
(45) Date of Patent: Feb.

(54) SOLAR CELLS WITH IMPROVED
LIFETIME, PASSIVATION AND/OR
EFFICIENCY

(58) Field of Classification Search
CPC 1101.31/020006; 1101.31/0804; 1101.31/1872; 1101.31/1864; 1101.31/5068; 1101.31/5069

(71) Applicant: SunPower Corporation, San Jose, CA (US)

(56) References Cited
U.S. PATENT DOCUMENTS

(72) Inventors: David D. Smith, Campbell, CA (US); Tim Dennis, Canton, TX (US); Roselle De Jesus Tabajorda, Buñic, Cebu (PH)

7,718,888 B2 5/2010 Comins
7,757,397 B2 6/2010 Comins
(Continued)

(73) Assignee: SunPower Corporation, San Jose, CA (US)

FOREIGN PATENT DOCUMENTS

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) for 13 days.

CN 102604077 8/2012
JP 2011-146021 A 8/2011

(21) Appl. No.: 16/877,255

OTHER PUBLICATIONS

(22) Filed: May 18, 2020

Pre-Interview Office Action for U.S. Appl. No. 14/ Jan. 11, 2016, 4 pgs.

(65) Prior Publication Data

(Continued)

US 2021/0043782 A1 Feb. 11, 2021

Primary Examiner — Long K Tran
(74) Attorney, Agent, or Firm — Schwabe, Williamson & Wyatt, P.C.

Related U.S. Application Data

(57) ABSTRACT

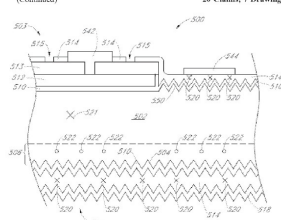
(60) Continuation of application No. 16/228,165, filed on Dec. 28, 2018, now Pat. No. 10,058,525, which is a (Continued)

A method of fabricating a solar cell can include dielectric regions on a silicon substrate. The method includes forming an emitter region over the dielectric regions and forming a deposit region on a surface of the silicon substrate at a temperature above 400°C to getter impurities to the emitter region from the deposit region to a portion of the substrate.

(51) Int. Cl. (2006.01)

(52) U.S. Cl. (2013.01); 1101.31/020006 (2013.01); 1101.31/020167 (2013.01); (Continued)

20 Claims, 7 Drawing Sheets



Maxeon's Lexicography and Disavowal Arguments in Its Sur-Reply Are Waived and Incorrect

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HANWHA SOLUTIONS CORPORATION,
Petitioner

v.

MAXEON SOLAR PTE. LTD.,
Patent Owner

Case IPR2024-01198
U.S. Patent No. 11,251,315

PATENT OWNER'S SUR-REPLY

“contaminants” is not a plain and ordinary meaning of “impurities.” Although Petitioner is mistaken for the preceding reasons, even if it were correct, then the ’315 patent clearly and unambiguously **disclaimed** the portion of “impurities” that covers dopants. “[T]he specification may reveal an intentional disclaimer, or

interchangeably.” Ex. 1001, 5:8-9. Through this clear statement, the inventors manifested their intent that the terms have the same meaning. *See Aortic Innovations LLC v. Edwards Lifesciences Corp.*, No. 1:21-cv-1377, 2023 WL 7545328, at *10 (D. Del. May 9, 2023) (“[T]he inventor has acted as his own **lexicographer** to give the same definitions to [three terms] through consistent interchangeable use of the terms.”). On the other hand, just as contaminants and

Paper 41 (Patent Owner's Sur-Reply), 7-8 (annotated); see also Paper 36 (Reply), 2-7

The Claims Would Not Recite Maxeon's "Key Purpose" Even Under Its Own Construction of "Metal Impurities"

Claim 10: A solar cell, the solar cell having a front side which faces the sun during normal operation and a back side opposite the front side, the solar cell comprising:

a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ and wherein the portion of the silicon substrate is formed at the front side of the solar cell;

a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of the solar cell;

an emitter region having **undesired foreign metals** formed over the dielectric region; and

a first metal contact former over the first emitter region.

Paper 36 (Reply), 6

Hanwha Consistently Applied the Plain and Ordinary Meaning of “Impurities”

Petition

UNITED
BEFORE

Claim construction is not necessary to resolve the issues presented in this
Petition. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013,
1017 (Fed. Cir. 2017). But Petitioner reserves the right to propose or respond to
claim constructions in the district court litigation and respond to any claim
construction Patent Owner advances here or raised by the Board. Trial Practice

MAXEON SOLAR PTE. LTD.,

Patent Owner.

Case No. IPR2024-01198

U.S. Patent No. 11,251,315

PETITION FOR *INTER PARTES* REVIEW

OF CLAIMS 10-20 OF

U.S. PATENT NO. 11,251,315

UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104

Paper 3 (Pet.), 24

Petitioner's Reply

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HANWHA SOLUTIONS CORPORATION,

Petitioner,

v.

MAXEON SOLAR PTE. LTD.,

Patent Owner.

II. “METAL IMPURITIES” SHOULD BE GIVEN ITS PLAIN AND ORDINARY MEANING

As the Petition explains, no claim construction is necessary because the issues
can be resolved based on plain and ordinary meaning of “metal impurities.” Pet.,

Paper 36 (Reply), 2; *see also, id.* at 8-10

Choi/Cousins + Istratov (Grounds I & III)

Claim 10 – Issues

1. Claim Construction of “Metal Impurities”

2. Gettering of Metal Impurities

3. Dopant Concentration

Gettering Was Known Well Before 2014



Fred Schubert, Ph.D.
Maxeon's Expert

Q. Gettering was one known way to reduce the metal impurities concentration in silicon wafers as of December 2014, correct?

A. Yes.

Ex.1090-Schubert-Tr., 118:17-20



David Carroll, Ph.D.
Maxeon's Expert

Q. And by 2014, gettering was a known way to remove metal impurities from silicon semiconductors, right?

A. Yes. Thermal gettering, uh-huh.

Ex.1092-Carroll-CSI-Tr., 71:8-10

Paper 3 (Pet.), 17-18; Ex.1003-Decl., ¶¶84-92; Paper 36 (Reply), 10-11; Ex.1089-Reply-Decl., ¶¶63-64

Solar Cell Fabrication Before 2014 Typically Used Gettering

- “Low-cost crystalline silicon materials are increasingly used for main-stream photovoltaic applications. ... Hence, the incorporation of gettering steps into the processing scheme is a prerequisite for the production of efficient solar cells.” – Ex.1095-Seibt, 696
- “It is needful to remove these impurities and external gettering techniques must be used because solar cells are volume devices.” – Ex.1033-Perichaud, 317
- “[As of the 1960s], one or more gettering steps are usually incorporated in the process to prevent introduction of undesirable metal impurities into the junction region or to remove any metal impurities that may be already there.” – Ex.1061-Ing, 533
- “[As of 2004,] [g]ettering of transition metals by a layer of polycrystalline silicon (polysilicon) deposited on the back side of silicon wafers has been widely used by the silicon industry as a means to remove transition metals from the wafer and improve the minority carrier lifetime.” – Ex.1064-Istratov-2004, 4472

Paper 3 (Pet.), 17-18; Ex.1003-Decl., ¶¶84, 89-93; Paper 36 (Reply), 11-12; Ex.1089-Reply-Decl., ¶¶63-65

Solar Cell Fabrication Before 2014 Typically Used Gettering



David Carroll, Ph.D.
Maxeon's Expert

"Today, most really high-quality silicon is gobbled up by the semiconductor industry. In order to accommodate that, the silicon solar industry typically uses a lower grade of silicon, and so post processing is necessary in order to make these materials perform better. ... In 2014 you would have used a lower-quality silicon to make the panels."

* * *

Q. ... [T]he post processing you referred to, I believe you said that would include a gettering step, correct?

A. Yes. So typically it's a gettering step that is driven by heating in some way.

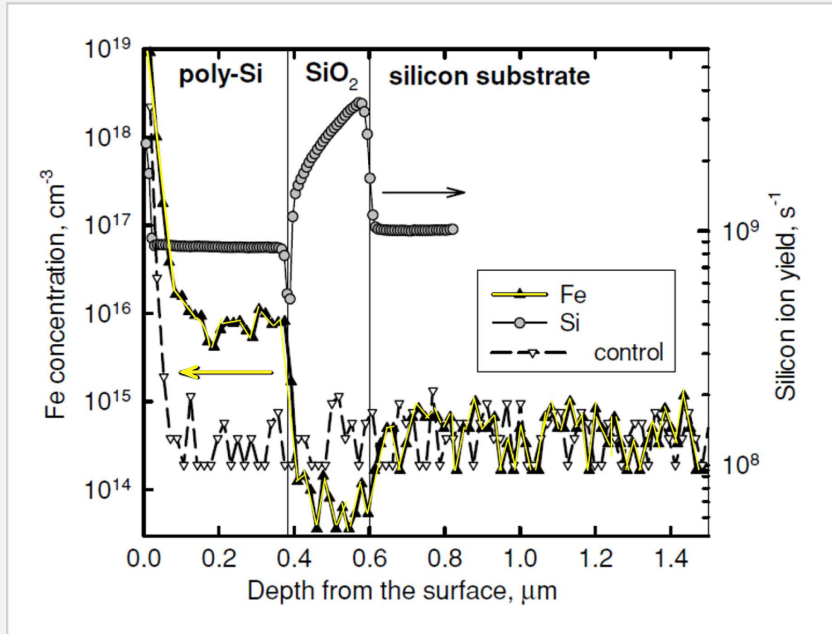
Q. And could that heating take place as part of the solar cell fabrication process?

A. It almost always does.

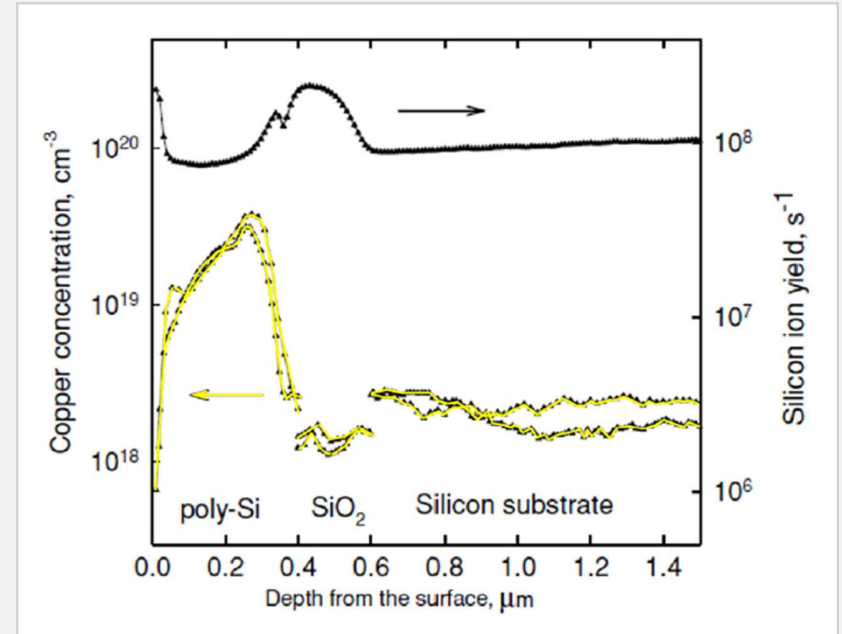
Ex.1092-Carroll-CSI-Tr., 25:2-26:18 (emphasis added); *id.* at 26:19-27:4 (emphasis added)

Paper 3 (Pet.), 17-18; Ex.1003-Decl., ¶¶84, 89-93; Paper 36 (Reply), 11-12; Ex.1089-Reply-Decl., ¶¶65-66

Istratov Teaches Effectively Gettering



Ex.1012-Istratov, 570, Fig.2 (annotated)

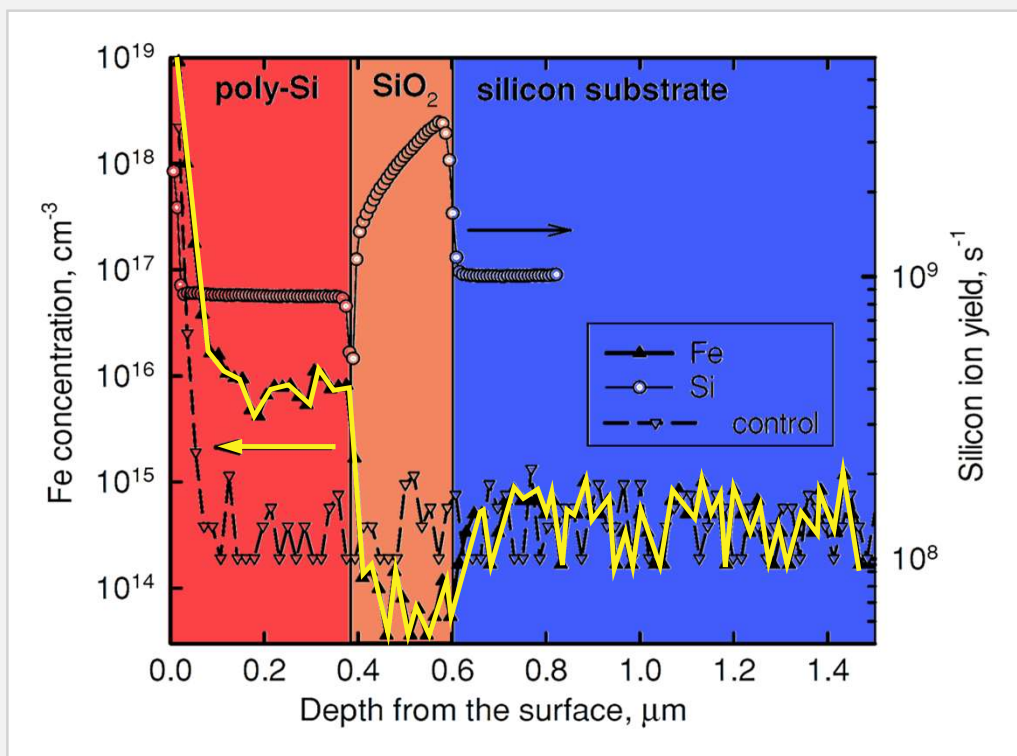


Ex.1012-Istratov, 571, Fig.5 (annotated)

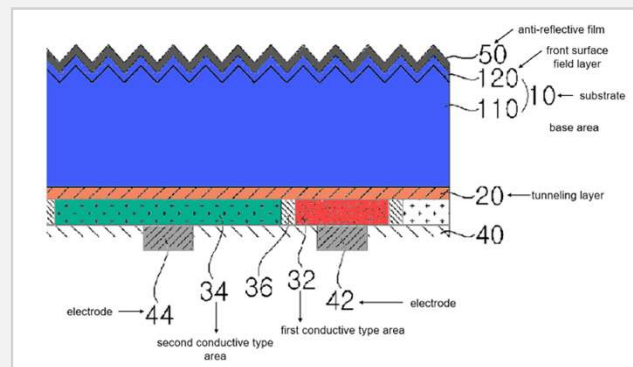
Istratov's gettering of iron and copper from the silicon substrate through the silicon dioxide layer and into the polysilicon region

Paper 3 (Pet.), 33, 43-45, 55; Ex.1003-Decl., ¶¶164-168, 206; Paper 36 (Reply), 15; Ex.1089-Reply-Decl., ¶¶74-75

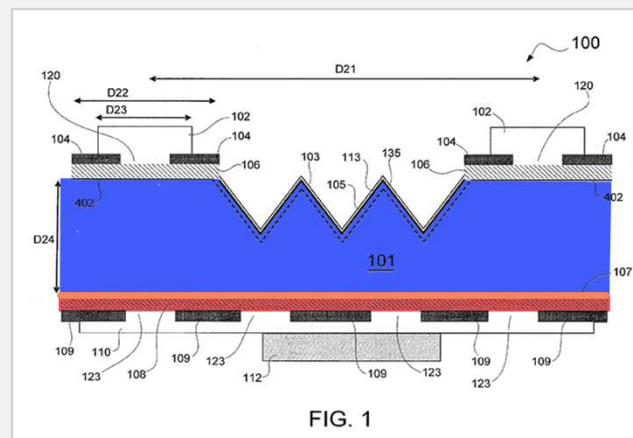
All of Choi, Cousins, and Istratov's Structures Have a Silicon Substrate, Silicon Dioxide Layer, and Polysilicon Layer



Ex.1012-Istratov, 570, Fig.2 (annotated)



Ex.1006-Choi, Fig.1 (excerpted and annotated)



Ex.1007-Cousins, Fig.1 (annotated)

Paper 3 (Pet.), 44-45; Ex.1003-Decl., ¶¶207, 373

Gettering Would Not Be Detrimental to Choi or Cousins

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HANWHA SOLUTIONS CORPORATION,

Petitioner,

v.

MAXEON SOLAR PTE. LTD.,

Patent Owner.

Case No. IPR2024-01198

U.S. Patent No. 11,251,315

REPLY DECLARATION OF DR. ZACHARY HOLMAN
REGARDING U.S. PATENT NO. 11,251,315

HANWHA v. MAXEON
IPR2024-01198
HANWHA 1089

80. A POSITA would have adapted Istratov's gettering process for Choi's solar cell structure by lowering the temperature and/or processing time to avoid any detrimental impacts. Ex.2037-Holman-Tr., 85:3-86:2. A POSITA would have known to lower the temperature and/or processing time because the oxide layer through which metal impurities are gettered is much thinner in Choi's solar cell (*see* above ¶78). As Dr. Schubert acknowledges, "Choi's tunnel oxide thicknesses are 40 to 2,600 times thinner than Istratov's [] oxide [layer] thicknesses." Ex.2028-Schubert-Decl., ¶62. A thinner oxide layer such as Choi's requires less thermal energy to diffuse through.

Ex.1089-Reply-Decl., ¶80

Paper 3 (Pet.), 46; Paper 36 (Reply), 16

A POSITA Would Calculate a Time-Temperature Combination to Effect Gettering in Choi and Cousins

3rd World Conference on Photovoltaic Energy Conversion May 11-18, 2003 Osaka, Japan

4P-A8-42

A GETTERING SIMULATOR: EVALUATING CONTAMINATION AND GETTERING PROCESSES

C. del Cañizo, L.J. Caballero, R. Esteban and A. Luque

Instituto de Energía Solar – Universidad Politécnica de Madrid

Ciudad Universitaria s/n - 28040 Madrid. Spain. Fax: 34 1 5446341, email: canizo@ies-def.upm.es

ABSTRACT

A software tool that simulates contamination and gettering processes is presented. It is based on a quantitative model that takes into account impurity diffusion and segregation, interaction with point defects, precipitation and trapping. It also relates impurity content with lifetime. The simulator is a helpful tool to study dependence of impurity content with temperature, evolution with process duration and influence of parameters on gettering efficiency. A friendly interface facilitates the control on the choice of parameters and the obtention of values and graphics. Some examples of application are shown.

3rd World Conference on Photovoltaic Energy Conversion May 11-18, 2003 Osaka, Japan

4P-A8-42

A GETTERING SIMULATOR: EVALUATING CONTAMINATION AND GETTERING PROCESSES

C. del Cañizo, L.J. Caballero, R. Esteban and A. Luque
Instituto de Energía Solar – Universidad Politécnica de Madrid
Ciudad Universitaria s/n - 28040 Madrid. Spain. Fax: 34 1 5446341, email: canizo@ies-def.upm.es

ABSTRACT

A software tool that simulates contamination and gettering processes is presented. It is based on a quantitative model that takes into account impurity diffusion and segregation, interaction with point defects, precipitation and trapping. It also relates impurity content with lifetime. The simulator is a helpful tool to study dependence of impurity content with temperature, evolution with process duration and influence of parameters on gettering efficiency. A friendly interface facilitates the control on the choice of parameters and the obtention of values and graphics. Some examples of application are shown.

1. INTRODUCTION

Gettering steps are simply implemented in most of silicon solar cell fabrication processes to counteract unavoidable contamination. A gettering process removes lifetime-killing impurities from the bulk, transporting them to regions where their recombination activity is reduced [1].

Determining specific gettering mechanisms is rather complex. One reason is the variety of impurities to be removed, and also their different behavior depending on their position in the silicon matrix: interstitial, substitutional, precipitated or trapped in a crystalline defect. Interaction with point defects (self-interstitials and vacancies) can also play an important role in certain cases.

We have developed a quantitative model that includes several of the mechanisms suspected to prevent or occur in a gettering process. The model is described by a set of differential equations for the dynamics of a single impurity. Impurity evolution throughout the wafer depth with process duration is deduced, and impact on lifetime calculated. Details can be found in Ref [2]. We think our model can be useful for the understanding and interpretation of gettering mechanisms.

To offer a friendly interface to simulate a process and analyze results, a software tool in Visual Basic has been prepared. It solves the set of differential equations transferring them in a finite difference equation system, with main parameters defined by the user. Impurity concentration depending on position, and their evolution during a thermal process, are presented.

The software tool, called "Gettering Simulator", is described in the paper. The different options, screens for data input and presentation of results are explained. Several specific processes have been simulated as examples, showing the kind of conclusions that can be expected from the use of the tool.

2. "GETTERING SIMULATOR" TOOL

Figure 1 shows a picture of the main screen. Main parameters are defined: temperature and time of process, type of impurity (substitutional or interstitial) and initial concentration; options exist to define initial concentrations also for precipitated and trapped impurities, and even to establish non-uniform initial profiles for them. A "simplified model" is applied in the absence of crystalline defects and precipitates, while a "complete model" applies if they exist.

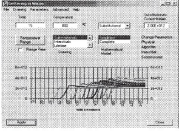


Fig. 1: Gettering simulator main screen.

There are several additional screens to define parameters:

-Physical: those regarding point and crystalline defects behavior.

-Algorithm: mainly time and spatial intervals.

-Intermittent/Substitutional: those defining impurity behavior.

As example for a substitutional impurity is shown in Fig. 2. Diffusion coefficient, solid solubility, velocity rate and equilibrium constants for kick-out and Frank-Turnbull reactions are defined, as well as parameters related to precipitates, segregation to the sink layer, influence in lifetime and pollution from the environment (which will be mentioned in more detail in section 3.1).

The choice of parameters to be used is of great importance. Default values based on experimental results and on those reported on literature are given. Nevertheless, the user can easily change parameter values and experience with new ones. In this way, a comparison of simulator results with experimental ones can help in discriminating some parameters whose values are still in controversy.

HANWHA V. MAXEON
IPR2024-01198
HANWHA 1125

Poster 993

Authorized licensed use limited to: Arizona State University. Downloaded on August 04, 2025 at 04:14:28 UTC from IEEE Xplore. Restrictions apply.

Ex.1125-delCanizo-2003, 993, 995 (annotated);
see also, Ex.1126-Hofstetter-2010

Paper 36 (Reply), 16-17; Ex.1089-Reply-Decl., ¶¶81-82

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Istratov Is Analogous Art



“Two criteria have evolved for determining whether prior art is analogous:

- (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and
- (2) if the reference is not within the field of the inventor’s endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved.”

In re Clay, 966 F.2d 656, 658–59 (Fed. Cir. 1992)

Paper 3 (Pet.), 42, 69-70; Ex.1003-Decl., ¶¶203-204, 368-369; Paper 36 (Reply), 13; Ex.1089-Reply-Decl., ¶¶70-77

Istratov Is Analogous Art: Same Field as '315 Patent



Fred Schubert, Ph.D.

Maxeon's Expert

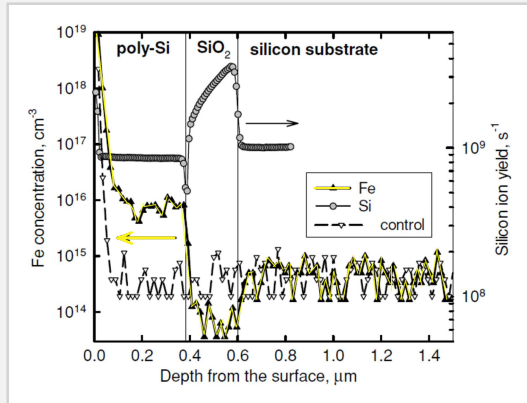
“And solar field is a sub-field of the semiconductor field. So I don’t see these as, you know, two separate fields. One is the sub-field of the other.”

* * *

Q. Okay. Why is knowledge in the semiconductor field applicable to solar cells?

A. Because solar cells are made of semiconductors.

Istratov Teaches Gettering From the Silicon Substrate Into the Polysilicon Region



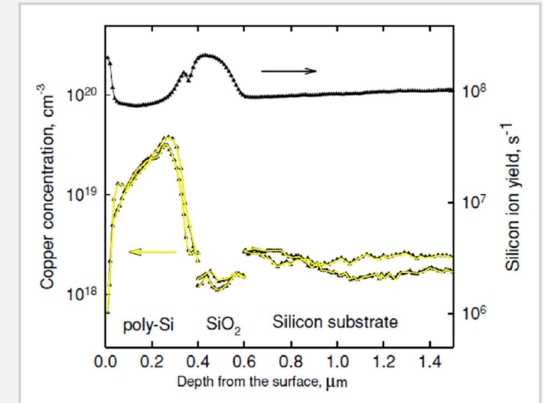
Ex.1012-Istratov, 570, Fig.2 (gettering of iron)
(annotated)



Fred
Schubert,
Ph.D.

- Q. So iron contamination was introduced into Istratov's test structure on the side opposite to the poly-silicon layer; is that right?
- A. **Correct ...**
- Q. And iron contamination was introduced into Istratov's test structure in the silicon substrate, correct?
- A. **Yes ...**
- Q. Figure 2 of Istratov shows that iron moved from the silicon substrate through the silicon dioxide, and then into the polysilicon region, right?
- A. **Yes.**

Ex.1090-Schubert-Tr., 139:6-140:16 (emphasis added)



Ex.1012-Istratov, 571, Fig.5 (gettering of copper)
(annotated)

- Q. So copper contamination was introduced into Istratov's test structure on the back side of the silicon substrate, correct?
- A. **Correct. ...**
- Q. And Figure 5 of Istratov shows that copper moved from the silicon substrate through the silicon dioxide and into the polysilicon region, right?
- A. **Correct.**

Ex.1090-Schubert-Tr., 141:2-143:1
(emphasis added)

Paper 36 (Reply), 14-15

Istratov Is Analogous Art: Pertinent to the Particular Problem of the '315 Patent



Fred
Schubert,
Ph.D.

Q. Would you agree that Istratov is directed to using gettering techniques to improve efficiency in those devices?

A. Microprocessor devices, **yes.**

Ex.1090-Schubert-Tr., 137:8-11 (emphasis added)

... metal impurities can be sources of recombination resulting in lower solar cell efficiency ... a goal of the '315 patent is to increase efficiency by “getter[ing] impurities to the emitter region.”

Ex.2028-Schubert-Decl., ¶45 (emphases added)

Paper 36 (Reply), 13

Istratov Teaches Gettering From the Silicon Substrate Into the Polysilicon Region

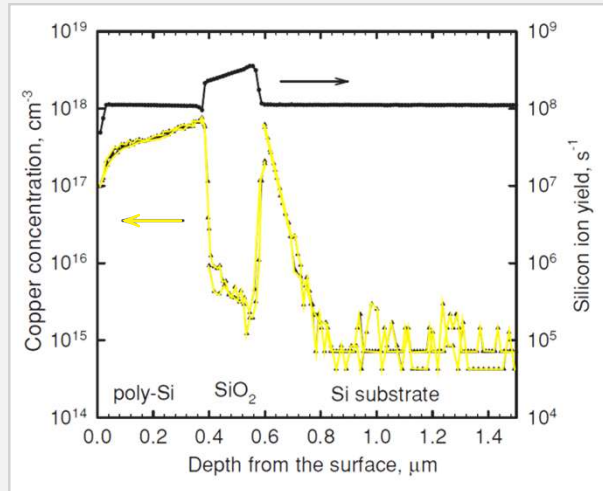


Fred Schubert, Ph.D.

Q. ... In Istratov's Figure 4, some copper has moved through the silicon dioxide layer into the poly-silicon layer, right?

A. Yes.

Ex.1090-Schubert-Tr., 150:5-10



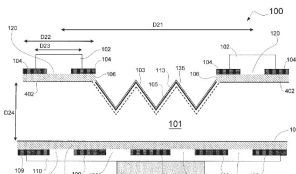
Ex.1012-Istratov, 571, Fig.4 (gettering of copper) (annotated)

90. It was well known by the earliest possible priority date that materials that are highly defective, such as polysilicon, make for good gettering trap sites for metal impurities, effectively acting as a sponge for impurities. Ex.1053-Nippon, 11-12, 16; Ex.1062-Mets, 422-424; Ex.1052-Lysacek, 1-2. Polysilicon is inherently a structurally defective material—that is, polysilicon has high defect density due to its grain boundaries (interfaces between different lattice regions of the polysilicon) that heat treatment does not cure. Ex.1053-Nippon, 11-12; Ex.1025-Fonash, 10-11.

Ex.1003-Decl., ¶90 (annotated)

Cousins Discloses Its Substrate Contains Metal Impurities

	
(12) United States Patent Cousins	(10) Patent No.: US 8,207,444 B2 (45) Date of Patent: Jun. 26, 2012
(54) FRONT CONTACT SOLAR CELL WITH FORMED ELECTRICALLY CONDUCTING LAYERS ON THE FRONT SIDE AND BACKSIDE	5,399,201 A 11/1994 Swanson 5,620,306 A 6/1997 Banika 5,641,362 A 6/1997 Meier 5,691,575 A * 12/1997 Nakashiki et al. 438,770 6,262,559 B1 * 7/2000 Meier et al. 136,256 6,754,465 B1 8/2000 VanDusen et al. 6,813,395 B1 11/2000 Crane et al. 6,933,457 B1 12/2000 Mulligan et al. 6,937,281 B1 1/2002 VanDusen et al. 6,997,726 B1 5/2002 VanDusen et al. (Continued)
(75) Inventor: Peter John Cousins, Menlo Park, CA (US)	
(73) Assignee: SunPower Corporation, San Jose, CA (US)	
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 144 days.	FOREIGN PATENT DOCUMENTS WO WO 2008/094791 * 1/2008 OTHER PUBLICATIONS (Continued) Muehle et al., High Quality Passivation for Heterojunction Solar Cells by Hydrogenated Amorphous Si on Suboxide Films, Applied Physics Letters, vol. 92, pp. 1-5, Jan. 23, 2008.*
(21) Appl. No.: 12/166,266	
(22) Filed: Jul. 1, 2008	
(65) Prior Publication Data US 2010/0009597 A1 Jun. 7, 2010	
(51) Int. Cl. H01L 31/068 (2006.01) DOI: 10.1082 (2006.01)	
(52) U.S. Cl. 136/258; 136/252; 136/256; 136/261; 438/57	
(58) Field of Classification Search 136/240-265 See application file for complete search history.	
(56) References Cited U.S. PATENT DOCUMENTS 3,961,297 A 6/1976 Chu 4,977,776 A 5/1990 Swanson 5,000,285 A * 7/1991 Swanson et al. 136,256 5,055,083 A 10/1991 Swanson 5,057,439 A * 10/1991 Swanson et al. 438,598 5,164,019 A 11/1992 Swanson 5,177,539 A 6/1993 Franz et al. 5,560,990 A 11/1994 Swanson	ABSTRACT (57) A bipolar solar cell includes a backside junction formed by a silicon substrate and a first doped layer of a first dopant type on the backside of the solar cell. A second doped layer of a second dopant type makes an electrical connection to the substrate from the front side of the solar cell. A first metal contact of a first electrical polarity electrically connects to the first doped layer on the backside of the solar cell, and a second metal contact of a second electrical polarity electrically connects to the second doped layer on the front side of the solar cell. An external electrical circuit may be electrically connected to the first and second metal contacts to be powered by the solar cell.



HANWHA 1007

In FIG. 4, an N-type silicon substrate **101** is prepared for processing into a solar cell by undergoing a damage etch step. The substrate **101** is in wafer form in this example, and is thus typically received with damaged surfaces due to the sawing process used by the wafer vendor to slice the substrate **101** from its ingot. The substrate **101** may be about 100 to 250 microns thick as received from the wafer vendor. In one embodiment, the damage etch step involves removal of about 10 to 20 μm from each side of the substrate **101** using a wet etch process comprising potassium hydroxide. The damage etch step may also include cleaning of the substrate **101** to remove metal contamination.

Ex.1007-Cousins, 4:23-35 (annotated)

Paper 36 (Reply), 29; Ex.1089-Reply-Decl., ¶155

Cousins's Substrates Contain Metal Impurities Below the Surface

handlers. Ex.1047-Istratov-2000, 491, 493; Ex.1122-Saito, 82. During wafer manufacturing, silicon ingots are cut into blocks and then wafers, typically with a wire saw. Ex.1120-Coletti-2011, 8. This sawing process causes mechanical damage to the wafer surface and can introduce metal impurities below the surface. Ex.1120-Coletti-2011, 8. Additionally, “[c]ross contamination from wafer to wafer, or from

Istratov-2000, 491. After the wafers are cut, etching is used to remove impurities from the surface of the wafer. Ex.1120-Coletti-2011, 8. If surface impurities are not properly removed, they can “contaminate chemical baths employed in solar cell manufacturing,” resulting in cross contamination of the wafers. Ex.1119-Coletti-2012, 84. Gas delivery systems were also known sources of metal impurities.

Ex.1089-Reply-Decl., ¶¶59-60 (annotated)

It was known that both sawing processes and etching processes could introduce metal impurities into silicon solar cell devices. Ex.1047-Istratov-2000, 491; see above ¶¶59-60. Cousins describes the “remov[al of] metal contamination” from “the substrate 101,” which a POSITA would have understood were present in silicon wafers and introduced through solar cell processing through steps such as sawing and etching.

Ex.1089-Reply-Decl., ¶155 (annotated)

After the ingots have been produced they are cut into blocks and wafers with a typical size of $156 \times 156 \text{ mm}^2$. The consumables used for the squaring/blocking and wafering, such as slurries, SiC particles, as well as the wires and blades themselves, are sources of contamination that are not necessarily only superficial. Indeed the mechanical damage, even at a microscopic scale, can introduce impurities below the surface of the wafers. If these impurities are not thoroughly removed by proper etching procedures they can diffuse deep into the wafers during the following high-temperature processes, or contaminate the chemical baths employed in solar-cell manufacturing.

Ex.1119-Coletti-2012, 84-85 (annotated);
see also Ex.1120-Coletti-2011, 8 (same)

The Combination of Cousins and Istratov Teaches the “Emitter Region[s] Having Metal Impurities”



“A finding of obviousness, however, cannot be overcome by attacking references individually where the rejection is based upon the teachings of a combination of references.”

Bradium Techs. LLC v. Iancu, 923 F.3d 1032, 1050 (Fed. Cir. 2019) (internal quotations and citation omitted)

Paper 3 (Pet.), 70-71, 74-75

Cousins' Teaching of a N-Type Substrate With a "Long Lifetime (e.g., 2 to 5 ms)"

saturation current of about $10 \text{ fA}\cdot\text{cm}^{-2}$. The N-type silicon substrate **101** may comprise a long lifetime (e.g., 2 to 5 ms) N-type silicon wafer and may have a thickness of about 100 to 250 μm as measured from the backside surface to a tip of the textured front side surface of the substrate (see dimension D24). The front side surface of the substrate **101** may be

Ex.1007-Cousins, 2:44-49 (annotated)

new argument is incorrect. Indeed, Cousins discloses a substrate with miniscule levels of iron impurities. Specifically, Cousins discloses that its silicon wafer has a "long lifetime," for example, a lifetime of 2 to 5 milliseconds. Ex. 1007, 2:44-46.

Paper 41 (Patent Owner's Sur-Reply), 11 (annotated)



**Zachary
Holman, Ph.D.**

Hanwha's Expert

"So Cousins at least teaches the possibility of the n-type silicon substrate for silicon solar cells having a lifetime of between 2 and 5 milliseconds. Cousins doesn't say whether that is the lifetime measured of the incoming wafer or at the end of fabrication, for example, after post-gettering, but does indicate that at some time, the wafer may have 2 to 5 millisecond lifetimes."

Ex.2040-Holman-Reply-Tr., 96:18-97:15 (emphasis added)

Cousins' Teaching of a N-Type Substrate With a "Long Lifetime (e.g., 2 to 5 ms)"

In another study, the lifetime was measured for mono-crystalline p-type wafers with different bulk contamination levels. Figure 7 shows the recombination lifetime versus Fe concentration for 10 Ωcm p-type wafers. A linear lifetime decrease with increasing bulk Fe contamination is obtained. At the bulk Fe concentration of $1\text{E}11$ atoms/ cm^3 , a lifetime of almost 200 μs could be measured.

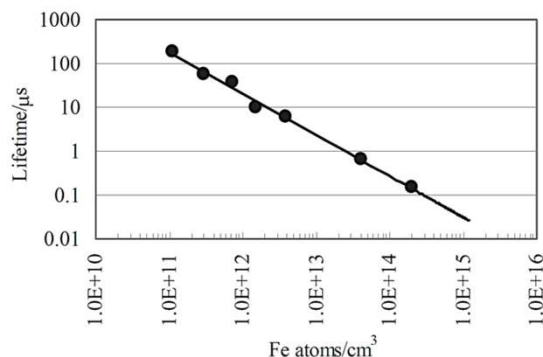
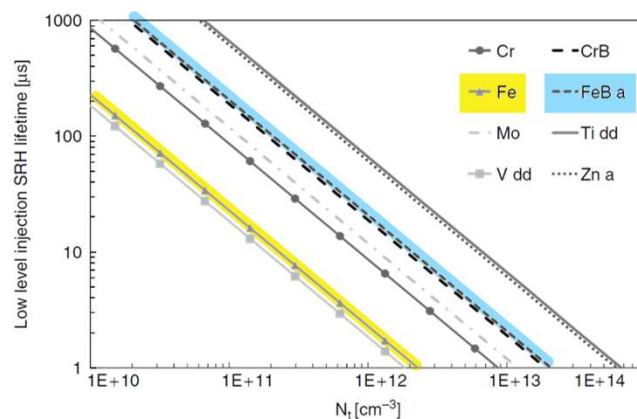


Fig. 7 Recombination lifetime versus Fe concentration for 10 Ωcm p-type wafers.

Ex.1139-Shabani, 189, (Fig.7 (annotated))



In Figure 3.7 the lifetime predicted by the SRH theory for several impurities is plotted as a function of their concentration. The lifetime is calculated at low injection level ($\Delta n \ll p_0, n_0, \Delta n \ll n_1$) for a p-type silicon with a bulk resistivity of $1\Omega\text{ cm}$.

Ex.1119-Coletti-2012, 94-95, Fig.3.7 (annotated)

Paper 41 (Patent Owner's Sur-Reply), 11-12

Reasons for the interest in n-type silicon ... [include] the lower sensitivity to impurities of n-type silicon compared to p-type silicon.

Ex.1031-Bultman, 69

"Shabani's Figure 7 is for p-type wafers, not n-type wafers, which is what Cousins is referring to. And n-type wafers tend to have higher lifetime than p-type wafers, everything else being the same."

* * *

Q. And what type of wafer is Coletti, Exhibit 1119?

A. ... I believe it's a p-type wafer ...

Ex.2040-Holman-Reply-Tr., 97:16-98:4; 98:5-10 (emphasis added)

Silicon Substrates Have High Levels of Metal Impurities

- “For instance, relatively recent studies of the silicon wafers for solar cells, ... revealed **iron concentrations** of about 1 ppb ($2.5 \times 10^{13} \text{ cm}^{-3}$).” – Ex.1047-Istratov-2000, 492 (emphases added)
- “Recent neutron activation analysis (NAA) studies revealed **metal concentrations** in ingot-cast multicrystalline silicon (mc-Si) materials [solar cell wafer production] as high as $10^{13} - 10^{16} \text{ cm}^{-3}$.” – Ex.1100-Buonassisi, 402 (emphases added)
- “Recent investigations of the **metal impurity content** of silicon solar cell materials have shown surprisingly high concentrations, e.g. $10^{14} - 10^{16} \text{ cm}^{-3}$ **iron** in different multicrystalline materials.” – Ex.1095-Seibt, 696 (emphases added).
- “[I]n most mc-Si materials [for silicon solar cell processing] total as-grown **Fe concentrations** as high as $10^{14} - 10^{16} \text{ cm}^{-3}$ are usually found.” – Ex.1127-Hofstetter-2011, 158 (emphases added)
- “Maximum concentrations of 3.83×10^{14} , 3.73×10^{12} , and $2.83 \times 10^{15} \text{ cm}^{-3}$ were detected near the top of [a photovoltaic-grade multicrystalline silicon] ingot for **Fe, Co, and Cu**, respectively.” – Ex.1094-Macdonald, 033523-6 (emphases added)

Table 2. Metal concentration levels in the top, middle and bottom of three different types of crystal.

Element atoms/cm ³	Solar grade multi-crystal silicon			Solar grade mono crystal silicon			Microelectronic silicon		
	Top	Middle	Bottom	Top	Middle	Bottom	Top	Middle	Bottom
Al	8.0E+12	5.5E+12	6.8E+12	3.9E+15	7.2E+15	1.7E+16	<1.0E+11	<1.0E+11	<1.0E+11
Cr	8.8E+11	3.8E+11	1.7E+11	1.9E+11	2.8E+11	8.1E+11	<1.0E+10	<1.0E+10	<1.0E+10
Mn	4.5E+11	3.5E+11	1.9E+11	4.9E+11	8.4E+11	3.7E+12	<1.0E+10	<1.0E+10	<1.0E+10
Fe	7.8E+12	3.5E+12	3.0E+12	7.7E+13	1.4E+14	5.2E+14	<1.0E+10	<1.0E+10	<1.0E+10
Co	1.3E+11	1.7E+11	1.4E+11	1.0E+10	1.0E+10	1.0E+10	<1.0E+10	<1.0E+10	<1.0E+10
Ni	1.1E+14	7.3E+13	3.4E+13	1.3E+12	2.4E+12	1.4E+13	<1.0E+10	<1.0E+10	<1.0E+10
Cu	3.4E+14	4.6E+14	5.4E+14	2.1E+13	3.8E+13	3.2E+14	<1.0E+10	<1.0E+10	<1.0E+10
Zn	3.2E+10	7.6E+10	1.9E+10	1.0E+10	1.0E+10	1.0E+10	<1.0E+10	<1.0E+10	<1.0E+10
Ti	3.6E+12	3.4E+12	3.7E+12	1.1E+12	2.3E+12	5.8E+12	<1.0E+11	<1.0E+11	<1.0E+11
Ga	3.0E+10	5.3E+10	4.7E+10	2.0E+12	3.8E+12	1.1E+13	<1.0E+10	<1.0E+10	<1.0E+10
Mo	1.9E+10	1.3E+11	1.4E+10	1.0E+10	1.0E+10	1.6E+11	<1.0E+10	<1.0E+10	<1.0E+10
Sn	5.4E+11	7.8E+11	6.9E+11	2.3E+13	3.4E+13	1.1E+14	<1.0E+10	<1.0E+10	<1.0E+10

Ex.1139-Shabani, 183, Table 2
(excerpted and annotated)

Paper 3 (Pet.), 17; Ex.1003-Decl., ¶¶ 83-84; Paper 36 (Reply), 10-13; Ex.1089-Reply-Decl., ¶¶ 52, 56-57

Maxeon's Expert: Metal Impurity Concentrations $> 10^{15} \text{ cm}^{-3}$



David Carroll, Ph.D.

Maxeon's Expert

Q. We were talking about in ... 2014, for terrestrial purposes, the solar industry typically starting with ... low-quality silicon substrates. Do you recall that?

A. I do recall that. ...

Q. Sure. And do you have knowledge of what the typical me[tal] impurity concentration would be in those low-quality substrates?

A. I do not have a direct memory of the numbers for the concentrations, other than to say something greater than 10 to the 15 or so. However, that's an overall number.

* * *

Q. Do you have a recollection of what the highest level of concentration on an atomic basis was that you observed in that 2010-to-2015 time frame?

A. I do not remember exactly. I know that it was over 10 to the 15, but that – beyond that, I don't remember exactly what the number was in front of the 10 to the 15.

Ex.1092-Carroll-CSI-Tr., 28:18-29:18 (emphases added); *id.* at 152:22-153:16

Paper 36 (Reply), 11

Metal Impurities Were a Pressing Concern in the Solar Industry



Fred Schubert, Ph.D.

Maxeon's Expert

Q. Do you agree that a POSITA, as of December 2014, would have understood that metal impurities are **sources of recombination**?

A. **Yes. Contaminating metal impurities, such as iron, nickel ... or chromium can serve as recombination centers.**

Q. You agree, a POSITA, as of December 2014, would have understood that **metal impurities can lead to poor lifetime and lower solar cell efficiency**, right?

A. **Yes. I agree.**

Ex.1090-Schubert-Tr., 117:4-16;

see also *id.* at 45:22-46:3; Ex.2028-Schubert-Decl., ¶157

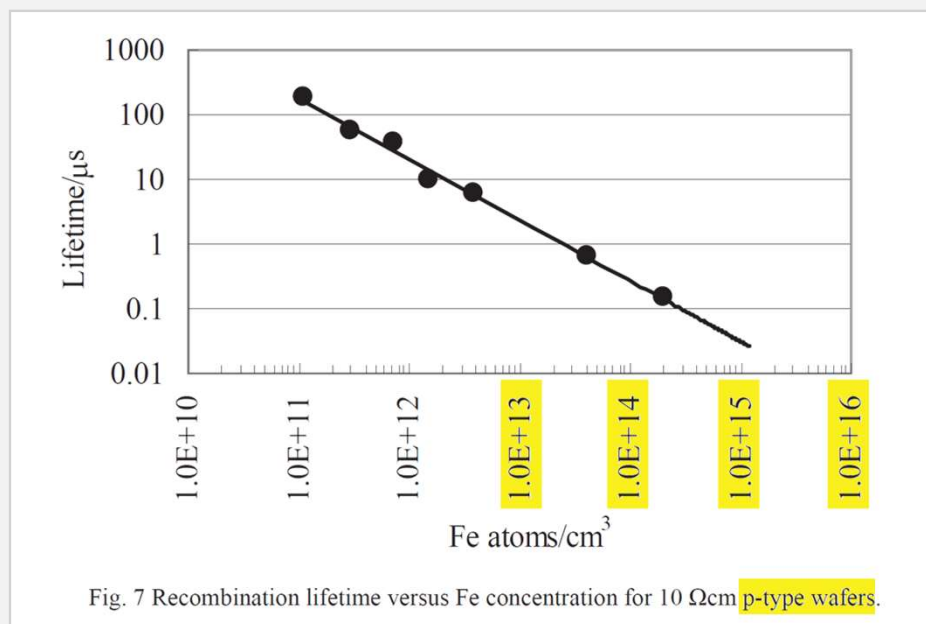


Fig. 7 Recombination lifetime versus Fe concentration for 10 Ωcm p-type wafers.

In another study, the lifetime was measured for mono-crystalline p-type wafers with different bulk contamination levels. Figure 7 shows the recombination lifetime versus Fe concentration for 10 Ωcm p-type wafers. A linear lifetime decrease with increasing bulk Fe contamination is obtained. At the bulk Fe concentration of 1E11 atoms/cm³, a lifetime of almost 200 μs could be measured.

Ex.1139-Shabani, 189, Fig.7 (annotated)

Paper 36 (Reply), 11; Ex.1003-Decl., ¶¶84-85; Ex.1089-Reply-Decl., ¶¶52-54

Solar Industry Used Lower-Quality Silicon Substrates



Zachary Holman, Ph.D.

Hanwha's Expert

“... the solar industry ... [needed] to use less expensive silicon than, for example, the semiconductor industry, which pushed them towards wafers that often had metal impurities such as iron.”

Ex.2037-Holman-Tr., 163:20-164:14



David Carroll, Ph.D.

Maxeon's Expert

- A. ... Today, most really high-quality silicon is gobbled up by the semiconductor industry. In order to accommodate that, the silicon solar industry typically uses a lower grade of silicon, and so post processing is necessary in order to make these materials perform better. You don't have to do that. You can use the higher-quality stuff, but it will cost you more. And since the primary driver in the solar industry today is the dollars per watt, then it doesn't make sense to use really expensive silicon. This changed sometime in ... the early 2000s, where we began to go to lower and lower quality silicon and using more and more post processing. So today, if you go and you buy one, the silicon that you begin with is not very high quality. But it is made to perform like a high-quality silicon boule because of the post processing
- Q. ... The tendency towards lower and lower quality silicon for the solar industry, you said that applies today and it started sometime in the ... mid 2000s. So it sounds like that would have been true in 2014, as well. Is that correct?
- A. Yes, that's right. In 2014 you would have used a lower-quality silicon to make the panels.

Ex.1092-Carroll-CSI-Tr., 25:2-26:18 (emphases added)

Paper 36 (Reply), 12; Ex.1089-Reply-Decl., ¶51

Solar Cell Fabrication Introduced High Levels of Metal Impurities

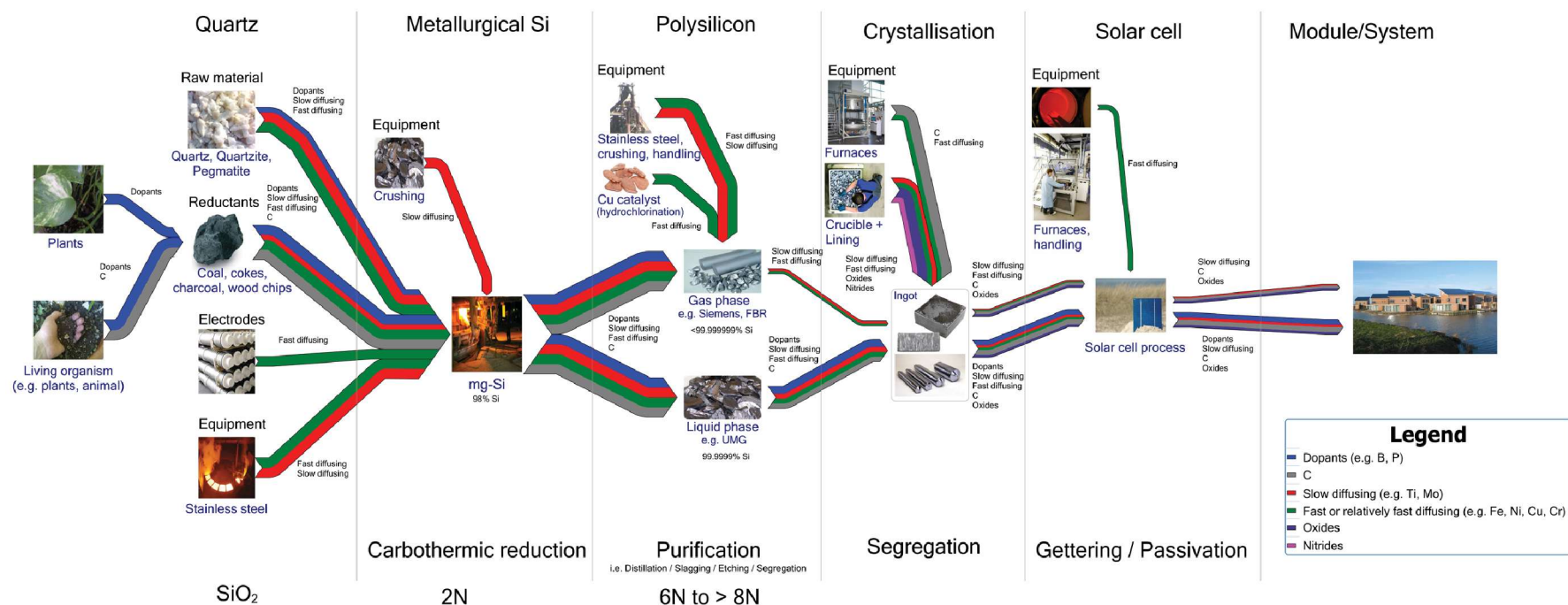


Figure 1.1 Impurity sources and refinement scheme.

Ex.1120-Coletti-2011, 3-4, Fig.1.1;
see also Ex.1119-Coletti-2012, 81, Fig.3.1

Paper 36 (Reply), 12; Ex.1003-Decl., ¶¶83; Paper 36
(Reply), 12; Ex.1089-Reply-Decl., ¶¶47, 58-62

Choi/Cousins + Granek or Marvin (Grounds I & III)

Claim 10 – Issues

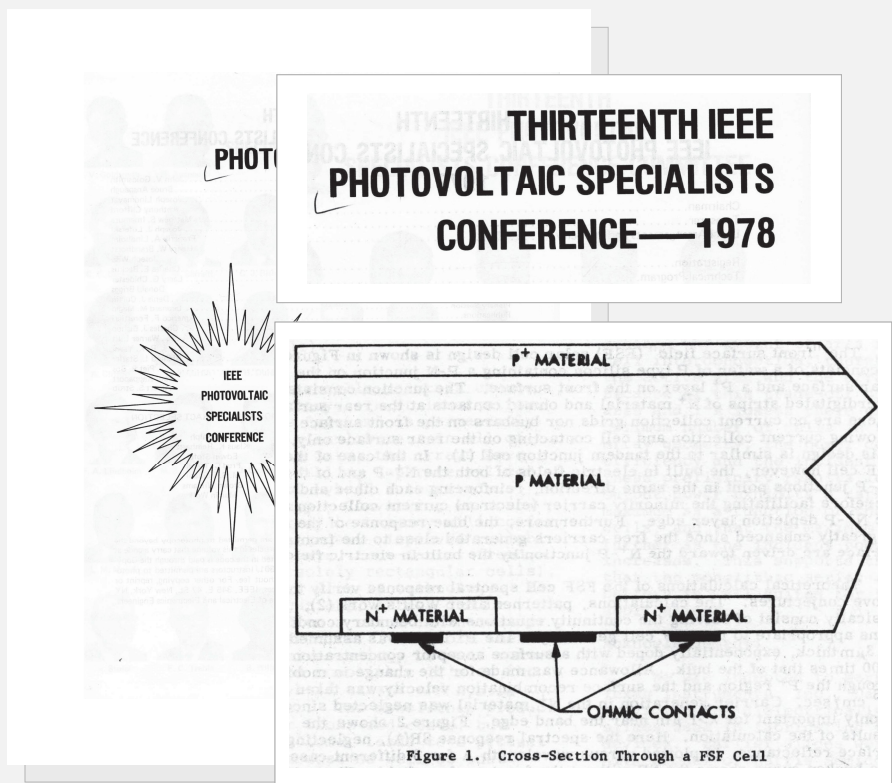
1. Claim Construction of “Metal Impurities”
2. Gettering of Metal Impurities
3. Dopant Concentration



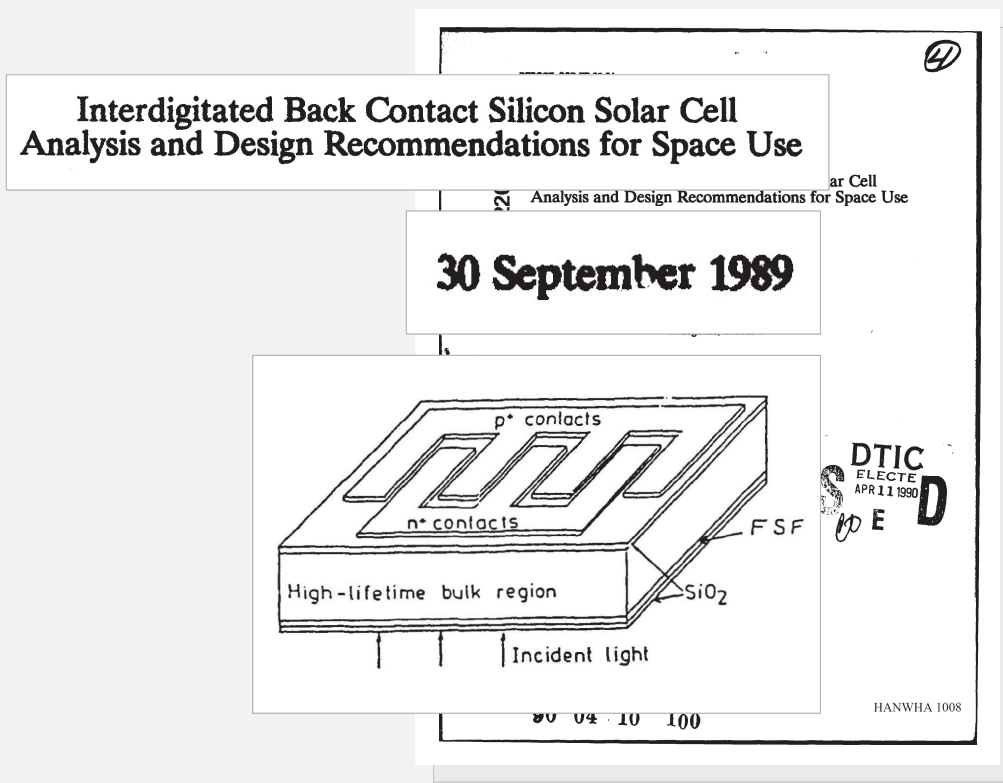
a first metal contact formed over the first emitter region.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Surface Passivation Was Well-Known Before 2014



Ex.1027-von Rouse, 1120, Fig.1



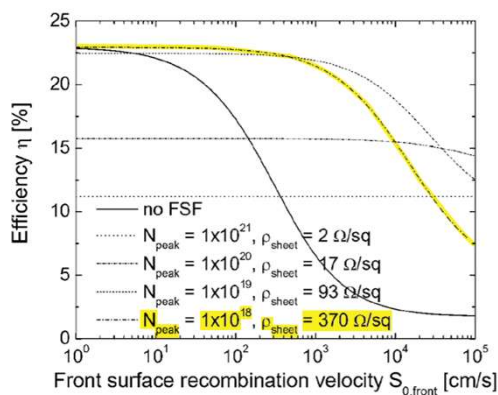
Paper 3 (Pet.), 16; Ex.1003-Decl., ¶ 76

Ex.1008-Marvin, 4, Fig.1

Claimed Dopant Concentration Was Widely Disclosed by 2014

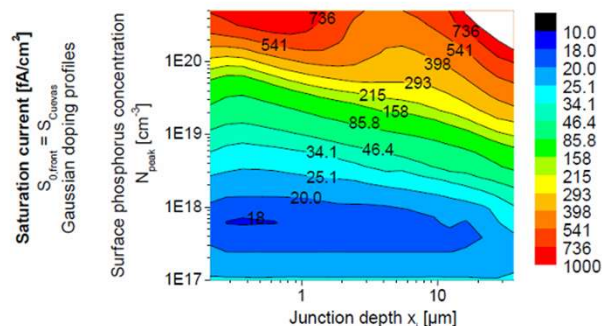
HIGH-EFFICIENCY
CONTACT BACK
SILICON SOLAR CELL

Dissemination
zur Erlangung eines
der Technischen
der Albert-Ludwigs-Universität
vorgetragen



Elites Granek

Fraunhofer



Ex.1010-Granek, 120-122, Figs.7-1, 7-3 (annotated);
Paper 3 (Pet.), 29-30; Ex.1003-Decl., ¶¶ 146-153

REPORT SSD-TR-90-04

DTIC FILE COPY

Interdigitated Back Contact Silicon Solar Cell
Analysis and Design Recommendations for Space Use

Prepared by
D. C. MARVIN and S. L. FROEDGE

The effects of FSF thickness and doping level were studied for the baseline cell geometry at BOL. For thicknesses of 0.25, 0.5, and 1.0 μm at $1\text{E}18$ doping, no significant effect was observed at 1 sun. The FSF effectiveness is relatively constant over a rather broad range around $1\text{E}17$ to $1\text{E}18 \text{ cm}^{-3}$, decreasing below this level due to the weakness of the electric field and decreasing above this level due to increased Auger recombination. As will be shown in the next section, the FSF doping level becomes very important for a graded FSF.

APPROVED FOR PUBLIC RELEASE:
DISTRIBUTION UNLIMITED

90 04 10 100

HANWHA 1008

Ex.1008-Marvin, 15 (annotated);
Paper 3 (Pet.), 32; Ex.1003-Decl., ¶¶ 159-160

Claimed Dopant Concentration Was Widely Disclosed by 2014

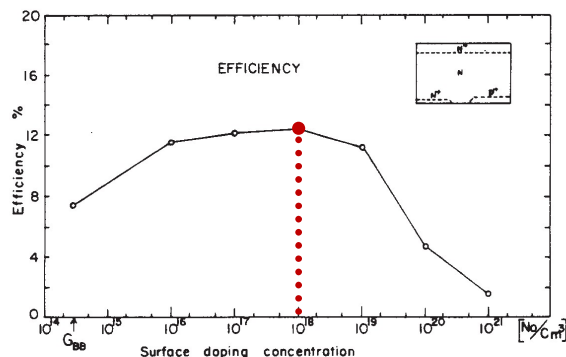


Fig. 9. The conversion efficiency of a front doping gradient IBC cell vs surface doping concentration showing that the optimum surface doping is about $10^{18}/\text{cm}^3$, at 1 sun AMO, $s_0 = 1000 \text{ cm/sec}$.

Ex.1103-Chin, 111 (Abstract), 113-114, Fig.9 (annotated)

II. SIMULATION METHODOLOGY

Fig. 1 shows the sketch of the symmetry element of the simulated solar cells. In this work we considered a FZ-Si n-type doped $200\mu\text{m}$ -thick wafer featuring resistivity $2 \Omega\text{-cm}$. The doping profiles in back surface field (BSF), front surface field (FSF) and emitter are gaussian functions of the spatial coordinate featuring the peak located at the edge of the interface and junction depth of $2\mu\text{m}$ for BSF and emitter and of $0.5\mu\text{m}$ for FSF region. Peak concentration doping is $4.16 \times 10^{19} \text{ cm}^{-3}$ for emitter, $4.16 \times 10^{19} \text{ cm}^{-3}$ for BSF and $1 \times 10^{18} \text{ cm}^{-3}$ for FSF [5].

Ex.1040-Procel, 15 (annotated)

Two solar cell design cases may illustrate how these plots can be put to use. In the case of a back-contacted cell in which the sunside diffusion is used mainly to reduce surface recombination, not to collect current, the optimum emitter is the one with the lowest J_0 . For untextured surfaces, this corresponds an emitter with $N_{D, \text{surf}} \approx 1 \times 10^{18} \text{ cm}^{-3}$ that is as thin as possible. Fig. 3 shows an emitter with these specifications is probably near optimum in J_0 when it has a textured front surface, as well. Other considerations such as resistance to ultraviolet-induced degradation may play a dominant role in selecting the best emitter of this type [9].

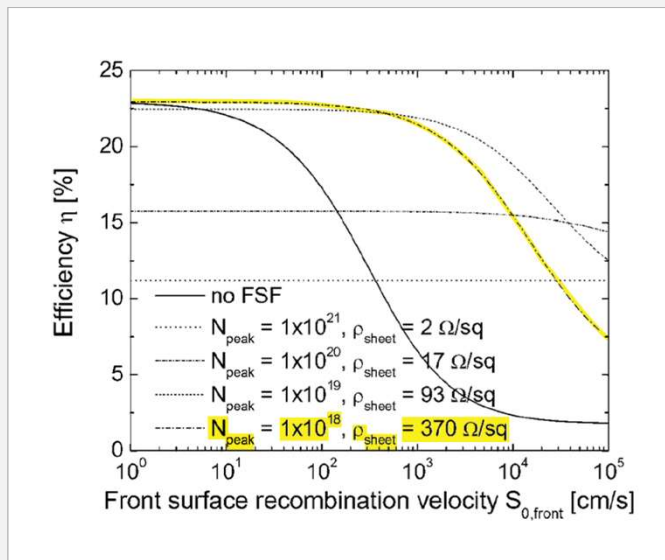
Ex.1021-King, 369 (annotated)

Paper 3 (Pet.), 17, 39; Ex.1003-Decl., ¶¶ 79-82;
Paper 36 (Reply), 17; Ex.1089-Reply-Decl., ¶83

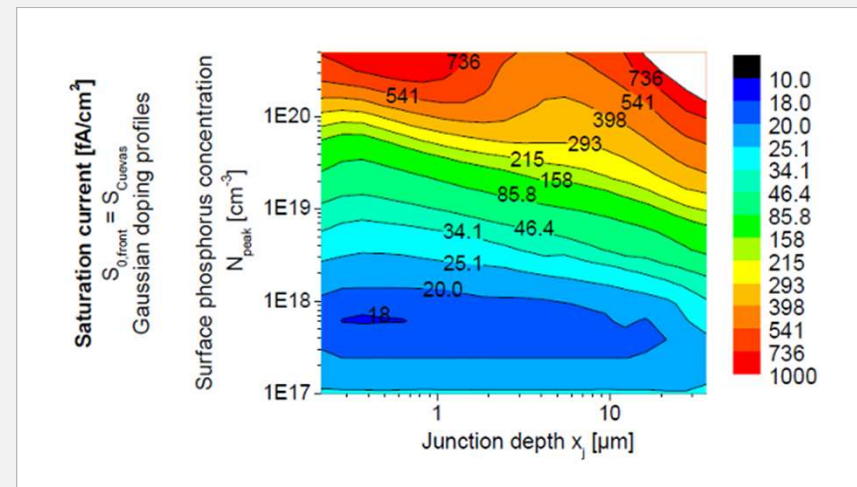
Choi/Cousins + Granek (Grounds I & III)

Granek Teaches the Claimed Dopant Concentration Results in Highest Efficiency and Lowest Recombination

Granek teaches “wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ and wherein the portion of the silicon substrate is formed at the front side of the solar cell”



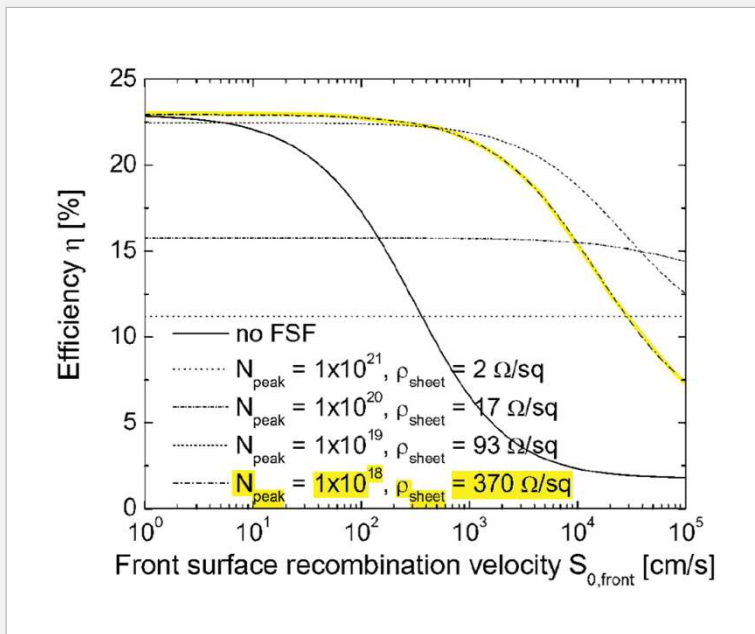
Ex.1003-Decl., ¶147; Ex.1010-Granek, 121, Fig.7-1 (annotated)



Ex.1003-Decl., ¶149; Ex.1010-Granek, 122, Fig.7-3

Paper 3 (Pet.), 28-30, 50-51, 73-74; Paper 36 (Reply), 22-24

Institution Decision: Granek's Figure 7-1 Teaches $1 \times 10^{18} \text{ cm}^{-3}$ Results in Highest Efficiency



Ex.1010-Granek, 121, Fig.7-1 (annotated)

On this record, we are persuaded that Petitioner sufficiently establishes that the combination of Choi and Granek teaches “a portion of the silicon substrate has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ ” as recited in claim 10. In particular, Granek teaches that “[a] lowly doped FSF results in high quantum efficiency,” and Granek’s Figure 7-1, reproduced below, shows that the highest efficiencies are expected when the dopant concentration is $1 \times 10^{18} \text{ cm}^{-3}$. Ex. 1010, 120–121.

Paper 17 (Institution Decision), 14 (annotated)

diffusion profiles. *Id.* at 122. From these simulations, Granek concludes that “for the well passivated surfaces, an optimal diffusion profile is lowly doped and shallow.” *Id.* at 123.

Paper 17 (Institution Decision), 16 (annotated)

Paper 3 (Pet.), 29; Paper 36 (Reply), 22-23; Ex.1003-Decl., ¶147

Institution Decision: Granek's Figure 7-3 Teaches $1 \times 10^{18} \text{ cm}^{-3}$ Results in Lowest Recombination

Trials@uspto.gov
571-272-7822

Paper 17
Date: February 26, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

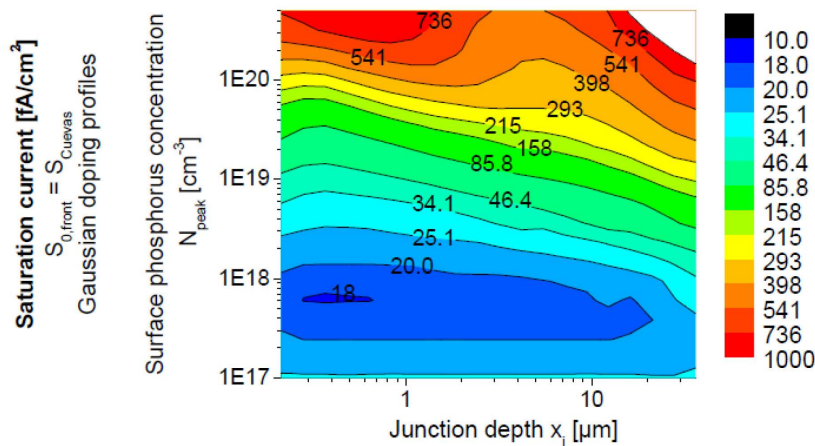
dimensional PC1D simulations).” Ex. 1010, 121. Granek’s Figure 7-3, reproduced below, similarly shows that the amount of recombination is lowest at dopant concentration values around $1 \times 10^{18} \text{ cm}^{-3}$.

IPR2024-01198
Patent 11,251,315 B2

diffusion profiles. *Id.* at 122. From these simulations, Granek concludes that “for the well passivated surfaces, an optimal diffusion profile is lowly doped and shallow.” *Id.* at 123.

35 U.S.C. § 314

HIGH-EFFICIENCY BACK-CONTACT BACK-JUNCTION SILICON SOLAR CELLS



HANWHA 1010

Ex.1010-Granek, 122, Fig.7-3

Paper 17 (Institution Decision), 15-16 (annotated)

Ex.1003-Decl., ¶149; Paper 36 (Reply), 23-24; Ex.1089-Reply-Decl., ¶¶ 115-117

A POSITA Would Have Implemented Cousins's and Choi's FSFs with Granek's Dopant Concentration of $1 \times 10^{18} \text{ cm}^{-3}$

Trials@uspto.gov
571-272-7822

Paper 17
Date: February 26, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HANWHA SOLUTIONS CORPORATION,
Petitioner,

v.

MAXEON SOLAR PTE. LTD.,
Patent Owner.

IPR2024-01198
Patent 11,251,315 B2

Before JO-ANNE M. KOKOSKI, JEFFREY W. ABRAHAM, and
AVELYN M. ROSS, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

At this stage of the proceeding, Petitioner, with supporting testimony from Dr. Holman, provides adequate reasons why using the front portion doping concentration of $1 \times 10^{18} \text{ cm}^{-3}$ or less taught in Granek with Choi's back contact solar cell would have been a "predictable use of prior art elements according to their established functions." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007); *see* Pet. 39–41 (and evidence cited therein).

- Cousins and Choi both disclose solar cells with FSFs. However, they do not specify a dopant concentration for the FSF
- Granek provides a value for the dopant concentration that increases the efficiency of the solar cell
- Granek's "experimental" results validate his simulation results

Paper 17 (Institution Decision), 18

Paper 3 (Pet.), 39-41; Paper 36 (Reply), 23-24

Maxeon's Criticisms That Granek's Dopant Concentration of $1 \times 10^{18} \text{ cm}^{-3}$ Is Not Preferred Are Inapposite



“[The] law does not require that a particular combination must be the preferred, or the most desirable, combination described in the prior art.”

In re Fulton, 391 F.3d 1195, 1200 (Fed. Cir. 2004)

Paper 36 (Reply), 17

Institution Decision: Granek's Experimental Results Validate His Simulation Results



Zachary Holman, Ph.D.

Hanwha's Expert

Trials@uspto.gov
571-272-7822

Paper 17
Date: February 26, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HANWHA SOLUTIONS CORPORATION,
Petitioner,

v.

MAXEON SOLAR PTE. LTD.,
Patent Owner.

IPR2024-01198
Patent 11,251,315 B2

Before JO-ANNE M. KOKOSKI, JEFFREY W. ABRAHAM, and
AVELYN M. ROSS, *Administrative Patent Judges*,
KOKOSKI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

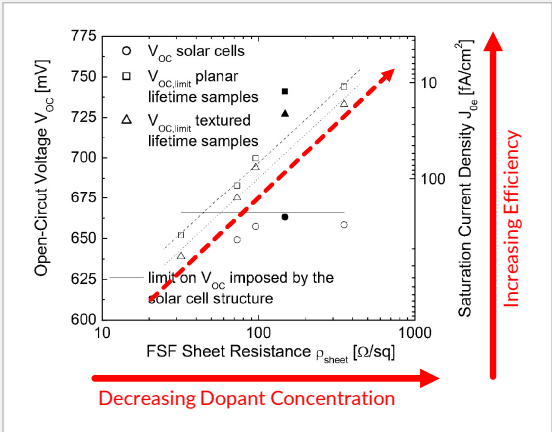
Dr. Holman credibly testifies:

Based on my own experience, it is difficult to predict the final dopant concentration of a semiconductor layer when performing an experiment varying diffusion conditions, and Granek does not explain why lower dopant concentrations were not studied experimentally. Although Granek's experiment resulted in an FSF dopant concentration of $3.8 \times 10^{18} \text{ cm}^{-3}$, Granek's experimental results validate his simulation results that a low FSF dopant concentration is desirable. Moreover, a person of ordinary skill in the art, looking at both Granek's simulation results and experimental results in conjunction, would have expected that a FSF dopant concentration of about $1.0 \times 10^{18} \text{ cm}^{-3}$ would have achieved a higher efficiency.

Paper 17 (Institution Decision), 16

Paper 36 (Reply), 23-24

Granek's Experimental Results Corroborate His Simulation Results



Ex.1089-Reply-Decl, ¶104;
Ex.1010-Granek, 133, Fig.7-10
(annotated)

Profile	Type	ρ_{sheet} [Ω/sq]	N_S [cm ⁻³]
FSF1	erfc	32	6.0×10^{20}
FSF2	erfc	73	4.0×10^{20}
FSF3	erfc	96	3.2×10^{20}
FSF4	erfc	353	4.5×10^{19}
FSF5	Gauss	148	3.8×10^{18}

Ex.1010-Granek, 126, Table 7-1
(excerpted and annotated)

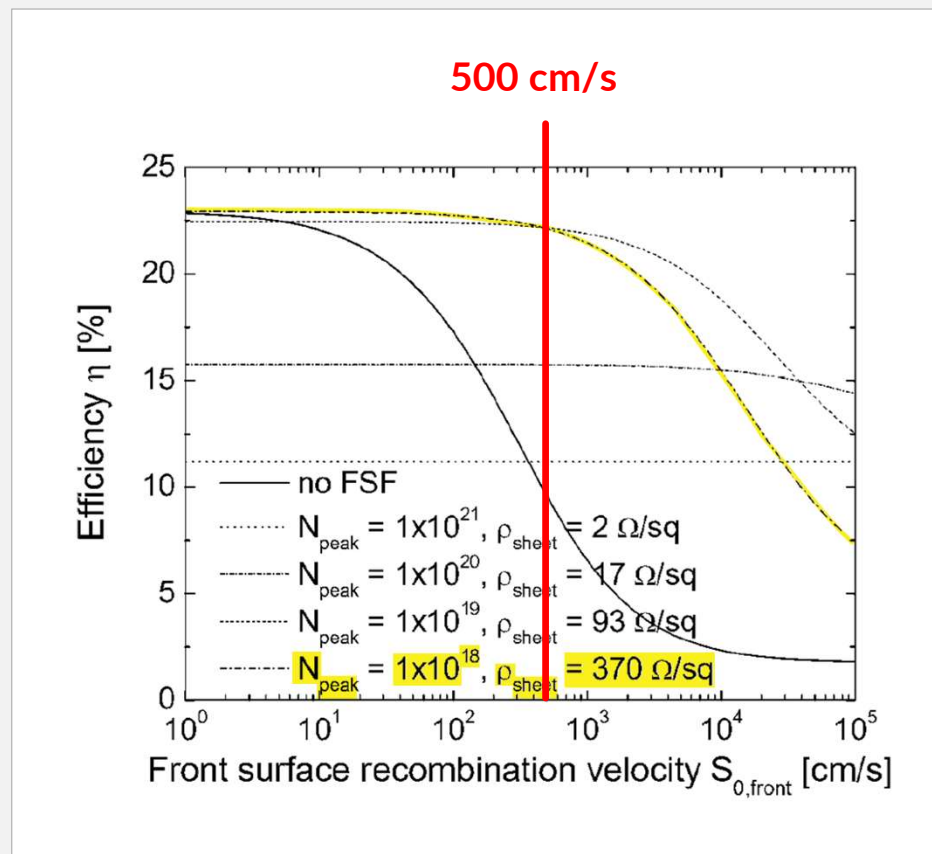
FSF Profile	Type	ρ_{sheet} [Ω/sq]	η [%]
FSF2	erfc	73	18.0
FSF3	erfc	96	19.5
FSF4	erfc	353	20.0
FSF5	Gauss	148	20.8
no FSF	-	-	19.7

Ex.1010-Granek, 132, Table 7-5
(excerpted and annotated)

- Like with his simulation results, Granek's experimental results show that reducing the FSF dopant concentration results in increased solar cell efficiency.
- Although Granek's lowest fabricated FSF dopant concentration was $3.8 \times 10^{18} \text{ cm}^{-3}$, Granek's experimental results suggest that further lowering the dopant concentration will result in increased solar cell efficiency.

Paper 36 (Reply), 23-24; Ex.1089-Reply-Decl, ¶¶101-105

Granek's Dopant Concentration for Surface Recombination Velocities Below 500 cm/s Apply to Choi and Cousins



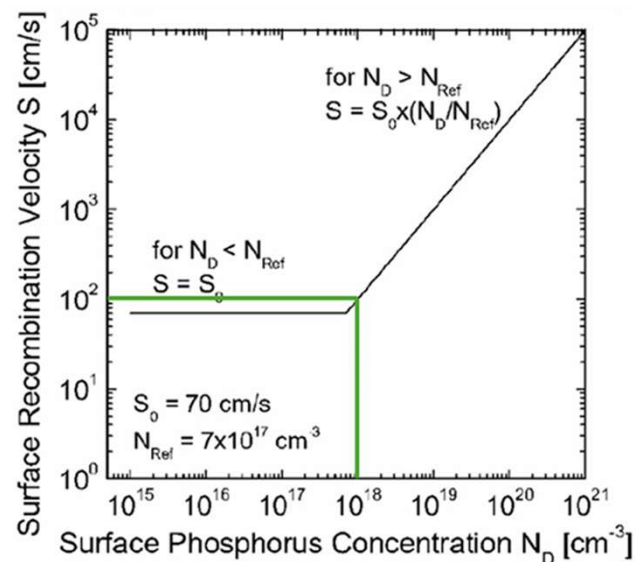
Ex.1010-Granek, 121, Fig.7-1 (annotated)

Paper 36 (Reply), 22

Granek's Dopant Concentration for Surface Recombination Velocities Below 500 cm/s Apply to Choi and Cousins

recombination velocity. Ex.1090-Schubert-Tr., 188:14-189:6. For instance, Choi explains that the “anti-reflective film 50 decreases reflectivity of light incident upon the front surface of the semiconductor substrate 10 and *passivates defects present on the surface or in the bulk of the front surface field layer 120.*” Ex.1006-Choi, [0030]. Similarly, Cousins discloses forming a “passivating oxide” on the front side surface of the solar cell. Ex.1007-Cousins, 3:7-11. Front surface recombination velocities for well-passivated front surfaces were lower than 500 cm/s in 2014. Ex.2037-Holman-Tr., 52:10-53:8; *see also, e.g.,* Ex.1118-Aberle-2000, 447; Ex.1041-Hermle, 1; Ex.1008-Marvin, 16-17.

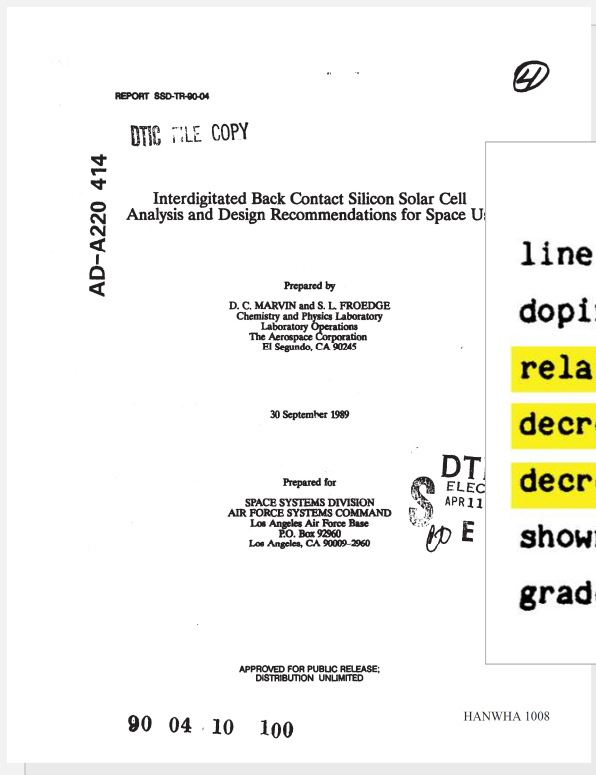
Ex.1089-Reply-Decl, ¶106



Ex.1010-Granek, 42, Fig.3-6 (annotated)

Paper 36 (Reply), 22

Marvin Teaches the Claimed Front Dopant Concentration



The effects of FSF thickness and doping level were studied for the base-line cell geometry at BOL. For thicknesses of 0.25, 0.5, and 1.0 μm at $1\text{E}18$ doping, no significant effect was observed at 1 sun. The FSF effectiveness is relatively constant over a rather broad range around $1\text{E}17$ to $1\text{E}18 \text{ cm}^{-3}$, decreasing below this level due to the weakness of the electric field and decreasing above this level due to increased Auger recombination. As will be shown in the next section, the FSF doping level becomes very important for a graded FSF.

Ex.1008-Marvin, 15 (annotated)

Paper 36 (Reply), 18

Marvin's Teachings for Beginning-of-Life Are Applicable to Choi's and Cousins' Solar Cells



Fred Schubert, Ph.D.

Maxeon's Expert

Q. What does beginning of life conditions mean?

A. In the context of space applications, it's ***before the cell is subjected to cosmic rays, cosmic radiation. ...***

Q. ***Beginning of life is the state of the solar cells when first made, right?***

A. **Yes.** That's a fair statement.

Marvin Teaches a Higher Dopant Concentration of $5 \times 10^{18} \text{ cm}^{-3}$ for Space Use

REPORT SSD-TR-80-04
DTIC FILE COPY
AD-A220 414
Interdigitated Back Contact Silicon Solar Cell
Analysis and Design Recommendations for Space Use
Prepared by
D. C. MARVIN and S. L. FROEDGE
Chemistry and Physics Laboratory
Laboratory Operations
The Aerospace Corporation
El Segundo, CA 90245
30 September 1989
Prepared for
SPACE SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
Los Angeles Air Force Base
P.O. Box 50260
Los Angeles, CA 90009-2660
APPROVED FOR PUBLIC RELEASE
DISTRIBUTION UNLIMITED
90 04 10 100

Table 2. Baseline Cell Design

p ⁺ width	35 μm
n ⁺ width	145 μm
p ⁺ thickness	1.0 μm
n ⁺ thickness	0.3 μm
p thickness	50 μm
τ _n in base	136 μs 1.10 μs ^(a) 0.32 μs ^(b)
τ _n in p ⁺ contact	0.128 μs 78 ns ^(a) 78 ns ^(b)
τ _p in n ⁺ contact	32.6 ns 12 ns ^(a) 12 ns ^(b)
FSF doping	5E18 p type
FSF thickness	0.5 μm

HANWHA 1008

For space use, where radiation is present, EOL performance must be considered. The baseline cell parameters are near optimum for EOL efficiency.

IV. CONCLUSION

The design of IBC solar cells for space use has been investigated using 2-dimensional computer simulations. Near-optimal designs have been presented for missions using either planar or 100 sun concentration for arrays, under high or negligible radiation fluences. In the low radiation environment, the minority and majority carrier collection regions should be of comparable width, with thicknesses of 0.9 μm and 3.0 μm, respectively. The FSF should be an approximately 0.5 μm step with doping concentration of $5 \times 10^{18} \text{ cm}^{-3}$. These parameters are much more critical for 100 sun operation. The 1 sun efficiency of IBC cells exceeds 15%, which makes them competitive with conventional design silicon cells. The 100 sun efficiency is nearly 19%, which greatly exceeds the conventional silicon cell capability. It is also in the expected efficiency range of GaAs concentrator cells, although the operating temperature of each is quite important in comparing efficiencies.

Ex.1008-Marvin, 10, 16, 25 (emphases added)

Paper 36 (Reply), 19-20

Institution Decision: A POSITA Would Not Have Chosen Lamers and Desa's Higher Dopant Concentrations Over Granek's Dopant Concentration of $1 \times 10^{18} \text{ cm}^{-3}$

Trials@uspto.gov
571-272-7822

Paper 17
Date: February 26, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HANWHA SOLUTIONS CORPORATION,
Petitioner,

v.

MAXEON SOLAR PTE. LTD.,
Patent Owner.

IPR2024-01198
Patent 11,251,315 B2

Before JO-ANNE M. KOKOSKI, JEFFREY W. ABRAHAM, and
AVELYN M. ROSS, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

We also disagree, on this record, with Patent Owner that a POSITA would not have found it obvious to modify Choi based on Granek's teachings because Lamers² and Desa³ have "similar passivation structures as Choi's" and "disclose optimum dopant concentrations for highly effective solar cells higher than the claimed 'dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$.'" Prelim. Resp. 21–22. Lamers reports that "the optimum doping level was found to be $[3 \times 10^{18} \text{ cm}^{-3}]$ " and "high-efficiency IBC cells" have "a top efficiency of 19.1%." Ex. 2002, 2, 4. Desa teaches that "[w]ith optimized cell parameters, an efficiency of 19% can be achieved," and shows that this efficiency is achieved with a dopant concentration around $1 \times 10^{19} \text{ cm}^{-3}$. Ex. 2003, 73, 76 (Fig. 5(c)). Granek reports a higher solar cell efficiency (20.8%) than both Lamers (19.1%) and Desa (19%). Ex. 1010, 141; Ex. 2002, 4; Ex. 2003, 73. Moreover, as set forth above, the record indicates that Choi and Granek have similar structures, which undermines Patent Owner's argument that a POSITA would have considered Lamers and Desa instead of Granek due to having "surface passivation structures similar to Choi's." Prelim. Resp. 21–22.

Paper 17 (Institution Decision), 17-18 (emphases added)

Paper 36 (Reply), 24-25

Lamers' Teaching of Dopant Concentration of $3 \times 10^{18} \text{ cm}^{-3}$ Does Not Apply to Choi

26th European Photovoltaic Solar Energy Conference and Exhibition, 5-9 September 2011, Hamburg, Germany

TOWARDS 21% EFFICIENT N-CZ IBC BASED ON SCREEN PRINTING

M.W.P.E. Lamers¹, A.A. Mew¹, I.G. Romijn¹, E.E. Bende¹, V. Komuro², M. Koppes¹,
D. Morecroft¹, M. Casam¹, F.J. Casanovi², A.W. Weeber¹, I. Cesar¹
¹ECN Solar Energy, P.O. Box 1, NL-1755 ZG Petten, The Netherlands
²Stellen Renewable Energy, Departament d'RD, Ciudad Politécnica de la Innovación - UPV,
Camino de Vera, 14 46100 Valencia, Spain.
Tel.: +31 224 566217; Fax: +31 224 56 8214; Email: Cesar@ecn.nl

ABSTRACT: Interdigitated Back Contact (IBC) cells have been fabricated at ECN laboratories with a best cell efficiency of 19.1%, using n-type Cz material and a process flow based on all-screen-printed patterning and metallization. Excellent current collection due to an optimized FSF is demonstrated by a μ_{sc} value as high as 41.5 mA/cm², corrected for spectral mismatch, and a V_{oc} of 641 mV. The results show high Pseudo Fill Factors (PFF) of above 81% but lower Fill Factors (FF) of below 72%.

Keywords: back contact, silicon solar cell, high efficiency

1 INTRODUCTION

Driven by market pressure to increase cell efficiencies and decrease production costs, we have developed a process flow for Interdigitated Back Contact (IBC) cells that is compatible with low-cost industrial processes. The process flow comprises conventional screen-printing steps for patterning and metallization, avoiding more expensive approaches such as lithography [1-3].

High efficiencies (>20%) can be achieved in IBC cells mainly because all current collection contacts are located at the rear, which eliminates the problem of front shading losses. A schematic cross section of the IBC cell can be seen in figure 1. Although optical shading losses are eliminated, recombination losses occur in the regions without emitter as the transport towards the emitter becomes comparable to the local diffusion length. This effect is referred to as electrical shading [4]. To reach the high cell efficiencies, the device structure requires excellent surface passivation at the front and rear sides, as well as patterning of both n- and p-type regions at the rear of the cell and a high bulk lifetime (>1 ms). Narrow and abrupt contact areas will result in reduced resistive and lateral losses. These losses are determined by the minimum feature size, which is limited by the patterning method used. The top-down solution of lithography is able to achieve close to ideal contact regions but the current process is too expensive for high-volume manufacturing. On the bottom-up end, screen-printing is well demonstrated in PV manufacturing and it is therefore important to evaluate the limits in the efficiencies of IBC cells fabricated using this approach.

Since the emitter in IBC cells is located at the rear, an almost ideal surface passivation is required at the front as most charge carriers are created close to that interface. The formation of a high-quality Front Surface Field (FSF) is necessary, which should provide a shielding field effect with no added Auger recombination and can be passivated using a dielectric layer.

In this paper we present the IBC cell made at ECN using tube furnace diffusion, wet-chemical, PECVD and screen-printing (patterning and metallization) process steps alone. The efficiency limits of the fabrication process presented are evaluated by studying the influence of the pitch and emitter fraction, and the effect of unpassivated contacts.

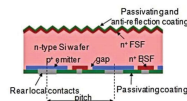


Figure 1: Schematic of an IBC cell, indicating the Front Surface Field (FSF), n+ Back Surface Field (BSF), p+ emitter, contacts and passivating layers. The definition of pitch and gap are also included. All contacts are located at the rear.

2 SOLAR CELL AND PROCESS DESCRIPTION

In figure 2 the process flow used to fabricate the IBC cells at ECN is shown. To enable optimal light confinement, the front surface of the cells is textured (random pyramids) using alkaline etching while the rear surface is smoothed which also improves passivation. This wet-chemical process is followed by the FSF diffusion, mainly to reduce the recombination at the front side [5]. After FSF diffusion, the steps include masking, diffusion and patterning of the front emitter and phosphorus BSF at the rear surface. The emitter and BSF are separated by a non-diffused gap, to avoid shading.

To ensure high efficiencies, front and rear side passivation needs to be excellent. The IBC cells require a rear surface passivation solution for three different surfaces: the highly doped p-type emitter, the highly doped n-type back surface field and the lightly doped n-type base. For this, the full rear side is passivated using a stack of SiO₂/SiN_x/H. The front side is passivated using SiN_x/H coating on top of the FSF. Subsequently, metallization on the BSF and emitter regions is done by screen printing and contacting of both regions is achieved simultaneously by a short high temperature firing step. All patterning and metallization steps were executed using low-cost screen-printing methods. Contacting was achieved by so-called firing-through using an inline belt furnace. The metallization fraction on the rear side was varied between 7.5 and 11.3%, excluding busbars, depending on the pitch.

Maxeon EX2002
Hanwha v. Maxeon
IPR2024-01198

The function of the front surface is to reduce the recombination at the front side and improve lateral transport. Recombination in the FSF should be minimal and the optimal doping level was found to be $3.10^{18} \text{ atoms/cm}^2$ [6-8]. Improved lateral transport by the FSF becomes increasingly important for larger pitches and higher base resistivity. For this, the optimal resistance was found to be $150 \text{ } \Omega/\text{sq}$ for the FSF. These specifications indicate that the FSF profile should be deep, close to $1 \mu\text{m}$. In order to fabricate this by diffusion in an industrial process, a long process time is required which is undesired. For moderate to low bulk resistances

Ex.2002-Lamers, 2 (annotated)

Paper 36 (Reply), 24-25

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Desa Has a Floating Junction, Not a Front Surface Field



Ex.2003-Desa, 80, Table 1 (annotated)

TABLE I SOLAR CELL PARAMETERS USED FOR SIMULATION OF SCREEN PRINTED IBC SOLAR CELL			
Serial No.	Parameters	Value	
1.	Wafer	Thickness	200µm
		Type	p-type
		Resistivity	2Ω.cm
2.	Front Surface Field (Floating Junction)	Width	3000µm
		Dopants	Phosphorous
		Concentration	Varied
3.	Emitter	Dopants	Phosphorous
		Concentration	Varied
		Width	1000µm
4.	Back Surface Field (BSF)	Dopants	Aluminum
		Concentration	Varied
		Width	1000µm
5.	Back Surface Recombination Velocity (BSRV)	Value	1000cm/s
6.	Front Surface Recombination Velocity(SRV)	Value	500cm/s

Paper 36 (Reply), 25

Procel Later Selected a FSF Dopant Concentration of $1 \times 10^{18} \text{ cm}^{-3}$

Analysis of the Impact of Rear Side Geometry on Performance of Back-Contact Back-Junction Solar Cells

Paul Procel, Vincenzo Maccaronio, Felice Crupi,
Giuseppe Cocorullo
Dipartimento di Ingegneria Informatica, Modellistica,
Elettronica e Sistemistica, Università della Calabria
Rende (CS), Italy

Mauro Zanuucoli
Advanced Research Center on Electronic Systems and the
Department of Electrical, Electronic, and Information
Engineering, University of Bologna
Cesena (FC), Italy

Abstract—In this work, we performed a study of rear side geometry of a back-contact back-junction solar cell parameters: the emitter, the back surface field (BSF) and their gap distance by exploiting two-dimensional TCAD numerical simulations. All figures of merit have been considered in order to understand the impact of the dominant ones. Higher efficiency are lead by higher emitter width/pitch ratios, lower pitches, and minimum BSF and gap widths. The impact of emitter is explained in terms of lower recombination in bulk due to a larger p-n junction, the impact of BSF and gap dimensions are explained in terms of surface recombination losses at back interface and the impact of pitch in terms of higher series resistance.

Keywords—solar cell; photovoltaics; back-contact solar cell; numerical simulation; dark analysis

I. INTRODUCTION

High efficiency Silicon-based back-contact back-junction (BCBJ) solar cells have been demonstrated particularly promising in order to improve the light conversion efficiency (currently more than 24% [1]). The absence of front contact allows simultaneously the simplification of cell interconnection at module level and the elimination of optical shadowing losses. However, the location of both contacts in the rear side leads to a reduction of the emitter size that means a smaller p-n junction. In this way, photogenerated minority carriers are more difficult to collect because of the presence of an horizontal component in the arrival path to the junction, and consequently increased recombination.

Some works have been developed to study the impact of BCBJ rear geometry over the figures of merit compared for different bulk lifetime and surface recombination velocities by Kim [2], and an extensive study of short circuit current density has been developed by Ritzel *et al.* [3] by analysing collection probability produced by electrical shadow effects.

The aim of this work is to improve the physical understanding of the impact of different rear geometries on the performance of BCBJ solar cells by a systematic simulation analysis under light conditions to understand the losses [4] that influence the overall figures of merit: short circuit current density (J_{sc}), open circuit voltage (V_{oc}) and fill factor (FF).

II. SIMULATION METHODOLOGY

Fig. 1 shows the sketch of the symmetry element of the simulated solar cells. In this work we considered a FZ-Si n-type doped 200μm-thick wafer featuring resistivity 2 Ω-cm. The doping profiles in back surface field (BSF), front surface field (FSF) and emitter are gaussian functions of the spatial coordinate featuring the peak located at the edge of the interface and junction depth of 2μm for BSF and emitter and of 0.5μm for FSF region. Peak concentration doping is $4.16 \times 10^{19} \text{ cm}^{-3}$ for emitter, $4.16 \times 10^{19} \text{ cm}^{-3}$ for BSF and $1 \times 10^{18} \text{ cm}^{-3}$ for FSF[5].

The front surface is coated by a double-layer anti reflective coating (ARC), without texturing. In order to achieve realistic predictions, physical models and parameters has been calibrated by means of state-of-the-art parameterizations [6]. Fermi-Dirac statistics is enabled to correctly deal with large doping concentrations. Bandgap narrowing model (BGN) by Schenk is used to account for realistic values of intrinsic carrier density ($n_i = 9.65 \times 10^9 \text{ cm}^{-3}$ at $T = 300 \text{ K}$) [7]. The model proposed by Klassen in [8] has been adopted in order to model the doping dependent carrier mobility. Recombination losses due to trap-assisted recombination is modeled by assuming the single-level trap model by Shockley-Read-Hall (SRH); the doping-dependent carrier lifetimes in phosphorus-doped FZ-Si are calculated according to [3]. Auger recombination model has been parameterized according to Altermat *et al.* [9]. Surface recombination velocity (SRV) at passivated interfaces has been modeled according to semiempirical models proposed in Cuevas [10]. The surface velocity at electrodes is set to $1 \times 10^6 \text{ cm/s}$.

II. SIMULATION METHODOLOGY

Fig. 1 shows the sketch of the symmetry element of the simulated solar cells. In this work we considered a FZ-Si n-type doped 200μm-thick wafer featuring resistivity 2 Ω-cm. The doping profiles in back surface field (BSF), front surface field (FSF) and emitter are gaussian functions of the spatial coordinate featuring the peak located at the edge of the interface and junction depth of 2μm for BSF and emitter and of 0.5μm for FSF region. **Peak concentration doping is $4.16 \times 10^{19} \text{ cm}^{-3}$ for emitter, $4.16 \times 10^{19} \text{ cm}^{-3}$ for BSF and $1 \times 10^{18} \text{ cm}^{-3}$ for FSF[5].**

Ex.1040-Procel, 15 (annotated)

Paper 36 (Reply), 25

Obviousness of Implementing P-Type Dopants (Claim 13-14)

Dependent Claims 13 and 14 – P-Type Dopants


US011251315B2

(12) United States Patent
Smith et al.

(10) Patent No.: US 11,251,315 B2
(45) Date of Patent: Feb. 15, 2022

10. A solar cell, the solar cell having a front side which faces the sun during normal operation and a back side opposite the front side, the solar cell comprising:

- a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of approximately less than or equal to $2 \times 10^{18} \text{ cm}^{-3}$ and wherein the portion of the silicon substrate is formed at the front side of the solar cell;
- a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of solar;
- a first emitter region having metal impurities formed over the dielectric region; and
- a first metal contact formed over the first emitter region.

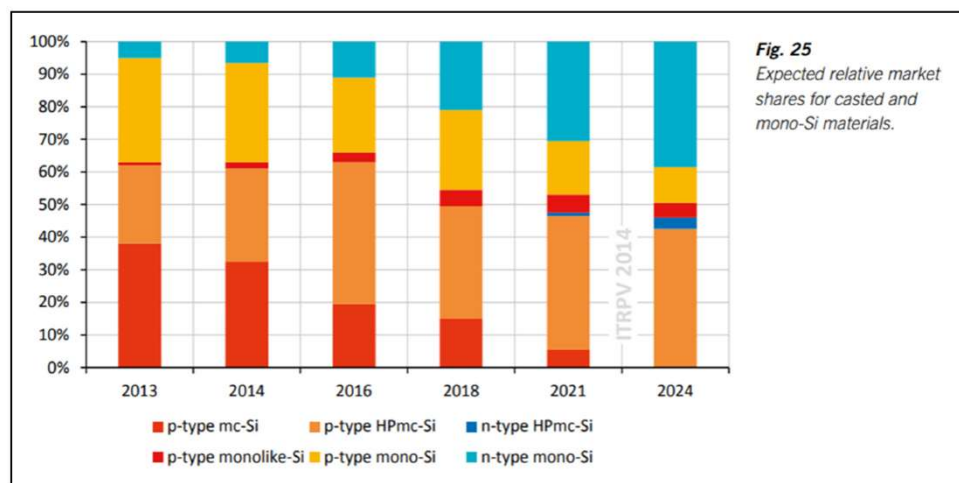
13. The solar cell of claim 10, wherein the portion of the silicon substrate comprises P-type dopants.

14. The solar cell of claim 10, wherein the portion of the silicon substrate comprises boron.

Ex.1001-USP315, Claims 10, 13, 14 (annotated)

A POSITA Would Have Been Motivated to Use Granek's Dopant Concentration in Choi's P-Type FSF

- **Maxeon does not separately argue** these claims based on the Choi+Marvin combination
- **Maxeon cannot dispute** that p-type silicon accounted for 95% of the market and that p-type silicon was cheaper than n-type silicon in 2014.



Ex.1115-ITRPV, 28, Fig.25

“Furthermore, n-type wafers are expected to be **more expensive** than p-types, at least **until 2018**. This makes it difficult to predict if the share of high efficiency n-type mono crystalline silicon will materialize as forecast in Fig. 25.”

Ex.1115-ITRPV, 27 (emphases added)
Paper 36 (Reply), 27; Ex.1089-Reply-Decl., ¶139

A POSITA Would Have Understood That Granek's Dopant Concentration Could Be Used For P-Type FSFs

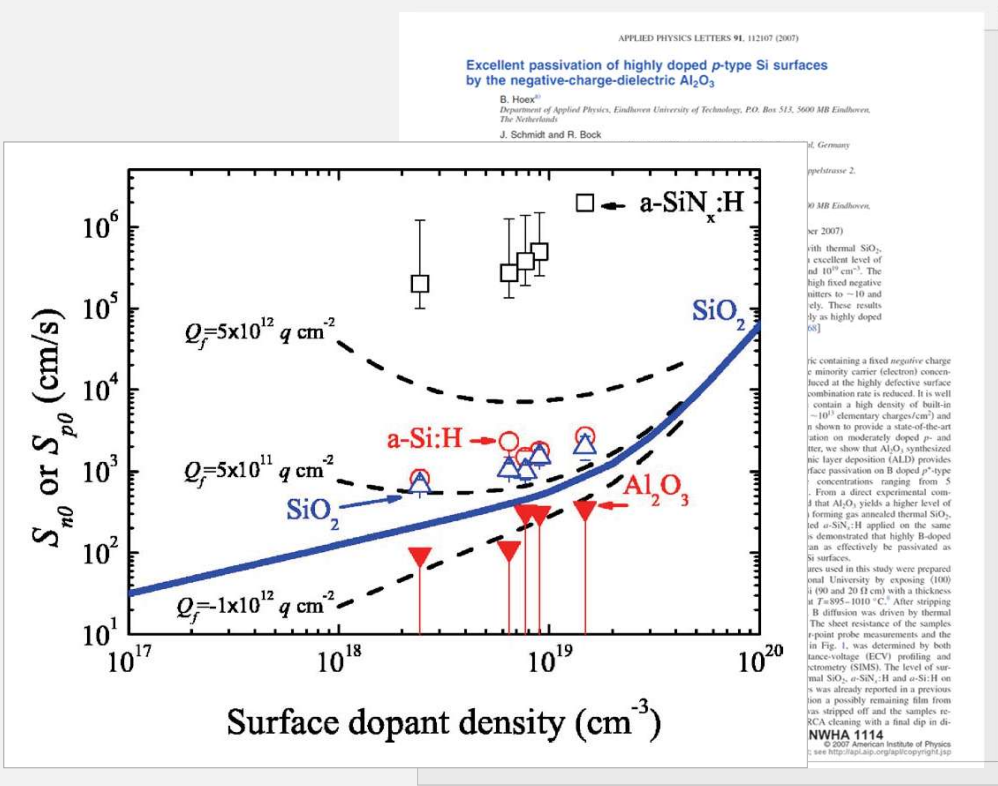
UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

2008). In fact, a 2007 paper demonstrates that “highly doped p-type surfaces can as effectively be passivated as highly-doped n-type [surfaces].” Ex.1114-Hoex-2007, 112107-3. As shown in Figure 4, Hoex-2007 extrapolates a surface recombination velocity of approximately 20 cm/s for a boron-doped surface (e.g., an FSF) with a surface dopants density of $1 \times 10^{18} \text{ cm}^{-3}$ (intersection of annotated green lines):

HANWHA v. MAXEON
IPR2024-01198
HANWHA 1089

Ex.1089-Reply-Decl., ¶80

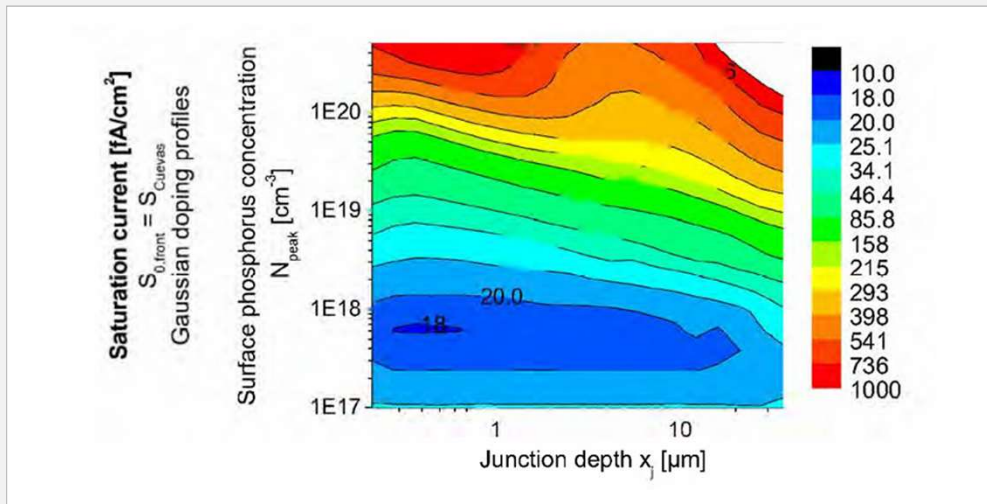


Ex.1114-Hoex-2007, Fig.4

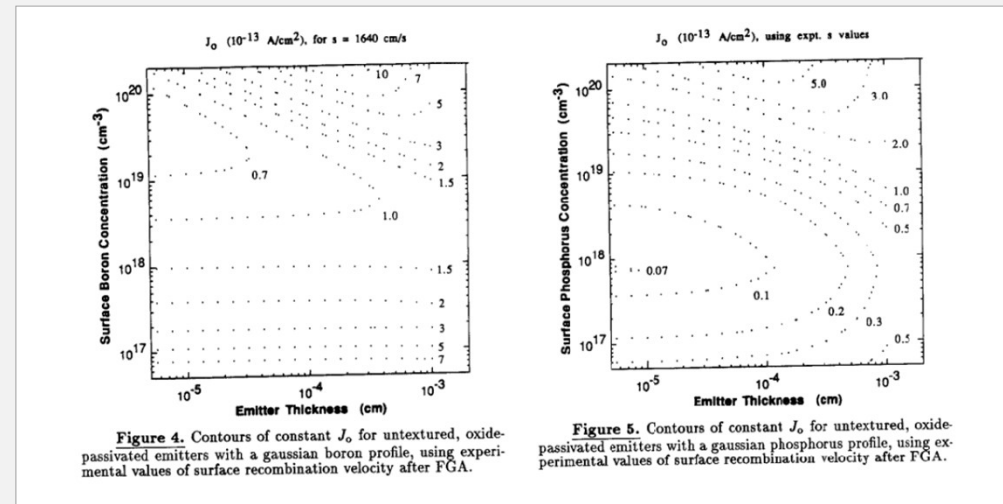
Paper 36 (Reply), 26-27

Implementing Granek's Dopant Concentration With a P-Type FSF Would Have Been a Straightforward Design Choice

- The '315 patent discloses only one dopant concentration for both n- and p-type
- Dopant concentration, recombination velocity, and saturation current were well-understood for both n- and p-type doped surfaces



Ex.1010-Granek, 122, Fig. 7-3



Ex.1111-King-1990, 230, Figs. 4, 5
Paper 36 (Reply), 26; Ex.1089-Reply-Decl., ¶142

Obviousness of Implementing a Trench (Claim 18)

(19) **United States**

(12) **Patent Application Publication**

(13) **SMITH**

(10) Pub. No.: **US 2013/0240029 A1**

(43) Pub. Date: **Sep. 19, 2013**

(54) **TRENCH PROCESS AND STRUCTURE FOR BACKSIDE CONTACT SOLAR CELLS WITH POLYSILICON DOPED REGIONS**

(71) Applicant: **David D. SMITH**

(72) Inventor: **David D. SMITH**

(21) Appl. No.: **13/893,085**

(22) Filed: **May 13, 2013**

Related U.S. Appl. No. **13/893,085**

(63) Continuation of applicant's U.S. Pat. No. **13/893,085**

Publication Classification

(51) Int. Cl. **H01L 31/052**

(52) U.S. CL. **H01L 31/05281** (2013.01)

CPC **H01L 31/05281** (2013.01)

USPC **136/255**

[0025] The trench structure of FIG. 1 addresses the aforementioned issues relating to polysilicon parasitic space charge recombination several ways. Firstly, the trench **104** separates the doped regions **101** and **102** so they are not physically in contact. This prevents the space charge region from existing in either polysilicon film. Secondly, the resulting accumulation layer under the trench **104** repels minority carriers to improve surface passivation. Thirdly, the textured surface **114** in the trench **104** increases solar radiation collection. These advantageously help increase solar cell efficiency.

Paper 3 (Pet.), 62-67; Ex.1003-Decl., ¶¶335-355;
Paper 36 (Reply), 27-29; Ex.1089-Reply-Decl., ¶¶145-153