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PTO/SB/413C (05-11)
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REQUEST FOR FIRST ACTION INTERVIEW (FULL PILOT PROGRAM)

Attorney Docket Number: 10031.004211	Application Number (if known):	Filing date: 10/02/2014
First Named Inventor: Peter John COUSINS	Title: FRONT CONTACT SOLAR CELL WITH FORMED EMITTER	

APPLICANT HEREBY REQUESTS A FIRST ACTION INTERVIEW IN THE ABOVE-IDENTIFIED APPLICATION. See Instruction Sheet on page 2.

1. The application must contain three (3) or fewer independent claims and twenty (20) or fewer total claims.

2. The application must not contain any multiple dependent claims.

3. By filing this request:

   Applicant is agreeing to make an election without traverse if the Office determines that the claims are not obviously directed to a single invention; and

   Applicant is agreeing not to request for a refund of the search fee and any excess claims fee paid in the application after the mailing or notification of the pre-interview communication prepared by the examiner

4. Other attachments: _____

Signature /Patrick D. Benedicto/	Date October 2, 2014
Name (Print/Typed) PATRICK D. BENEDICTO	Registration Number 40,110

Note. *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

■ *Total of 1 forms are submitted

The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Attorney Docket No. 10031.004211

FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

Inventor: Peter John Cousins

REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. Application No. 13/495,577, filed on June 13, 2012, which is a divisional of U.S. Application No. 12/070,742, filed on February 20, 2008, now U.S. Patent No. 8,222,516. The just-mentioned disclosures are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to solar cells, and more particularly but not exclusively to solar cell fabrication processes and structures.

2. Description of the Background Art

Solar cells are well known devices for converting solar radiation to electrical energy. They may be fabricated on a semiconductor wafer using semiconductor processing technology. A solar cell includes P-type and N-type diffusion regions that form a junction. Solar radiation impinging on the solar cell creates electrons and holes that migrate to the diffusion regions, thereby creating voltage differentials between the diffusion regions. In a backside contact solar cell, both the diffusion regions and the metal contacts coupled to them are on the backside of the solar cell. The metal

contacts allow an external electrical circuit to be coupled to and be powered by the solar cell.

In a front contact solar cell, at least one of the metal contacts making an electrical connection to a diffusion region is on the front side of the solar cell. The front side of the solar cell, which is opposite the backside, faces the sun during normal operation to collect solar radiation. While backside contact solar cells have an aesthetic advantage over front contact solar cells due to the absence of metal contacts on the front side, and are thus preferred for residential applications, aesthetics is not a major requirement for power plants and other applications where power generation is the main concern. Disclosed herein are structures for a relatively efficient and cost-effective front contact solar cell and processes for manufacturing same.

SUMMARY

A bipolar solar cell includes a backside junction formed by an N-type silicon substrate and a P-type polysilicon emitter formed on the backside of the solar cell. An antireflection layer may be formed on a textured front surface of the silicon substrate. A negative polarity metal contact on the front side of the solar cell makes an electrical connection to the substrate, while a positive polarity metal contact on the backside of the solar cell makes an electrical connection to the polysilicon emitter. An external electrical circuit may be connected to the negative and positive metal contacts to be powered by the solar cell. The positive polarity metal contact may form an infrared reflecting layer with an underlying dielectric layer for increased solar radiation collection.

These and other features of the present invention will be readily apparent to persons of ordinary skill in the art upon reading the entirety of this disclosure, which includes the accompanying drawings and claims.

DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically shows a cross-section of a solar cell in accordance with an embodiment of the present invention.

FIG. 2 is a plan view schematically showing the front side of the solar cell of FIG. 1.

FIG. 3 is a plan view schematically showing the backside of the solar cell of FIG. 1.

FIG. 4, which comprises FIGS. 4A-4M, schematically illustrates the fabrication of the solar cell of FIG. 1 in accordance with an embodiment of the present invention.

The use of the same reference label in different figures indicates the same or like components. The figures are not drawn to scale.

DETAILED DESCRIPTION

In the present disclosure, numerous specific details are provided, such as examples of apparatus, process parameters, materials, process steps, and structures, to provide a thorough understanding of embodiments of the invention. Persons of ordinary skill in the art will recognize, however, that the invention can be practiced

without one or more of the specific details. In other instances, well-known details are not shown or described to avoid obscuring aspects of the invention.

FIG. 1 schematically shows a cross-section of a solar cell 100 in accordance with an embodiment of the present invention. The solar cell 100 has a front side where a metal contact 102 is located and a backside on a same side as the metal contact 110. The front side faces the sun during normal operation to collect solar radiation.

In the example of FIG. 1, the solar cell 100 includes a backside junction formed by a P-type doped polysilicon emitter 108 serving as a P-type diffusion region and an N-type silicon substrate 101 servings as an N-type diffusion region. The N-type silicon substrate 101 may comprise a long lifetime (e.g., 2 to 5ms) N-type silicon wafer and may have a thickness of about 100 to 250 μm as measured from the backside surface to a tip of the textured front side surface of the substrate. The front side surface of the substrate 101 is randomly textured (labeled as 113) and includes N-type doped regions 105 and 106 formed in the substrate. The N-type doped region 105 provides low front surface recombination and improves lateral conductivity whilst not compromising the blue response of the solar cell. The region 106, which may be a phosphorus diffusion, provides low contact resistance and minimizes contact recombination. The region 106 is also referred to as an "N-dot" because, in one embodiment, it forms a dot-shape to minimize the area of heavily diffused regions on the front surface. The N-type doped region 105 may have a sheet resistance of 100 to 500 Ω/sq, whilst the n-type doped region 106 may have a sheet resistance of 10 to 50 Ω/sq.

An antireflective coating (ARC) of silicon nitride layer 103 is formed on the textured front side surface of the substrate 101. The texture front side surface and the

silicon nitride layer 103 help improve solar radiation collection efficiency. A passivating oxide 124 may comprise silicon dioxide thermally grown to a thickness of about 10 to 250 Angstroms on the front side surface of the substrate 101.

In one embodiment, the polysilicon emitter 108 is formed on a tunnel oxide layer 107. The polysilicon emitter 108 may be formed by forming a layer of polysilicon using Chemical Vapor Deposition (CVD), such as Low Pressure CVD (LPCVD) or Plasma Enhanced CVD (PECVD), and thermal anneal. The polysilicon emitter 108 may have a sheet resistance of 100 Ω/sq, and a thickness of 1000 to 2000 Angstroms. The tunnel oxide layer 107 may comprise silicon dioxide thermally grown to a thickness of about 10 to 50 Angstroms on the backside surface of the substrate 101. A metal contact 110 electrically connects to the polysilicon emitter 108 through contact holes 123 formed through a dielectric comprising a silicon dioxide layer 109. The metal contact 110 provides a positive polarity terminal to allow an external electrical circuit to be coupled to and be powered by the solar cell 100. The silicon dioxide layer 109 provides electrical isolation and allows the metal contact 110 to serve as an infrared reflecting layer for increased solar radiation collection. In one embodiment, the metal contact 110 comprises silver having a conductance of about 5-25 mΩ.cm and a thickness of about 15-35μm.

On the front side of the solar cell 100, the metal contact 102 electrically connects to the region 106 through a contact hole 120 formed through the silicon nitride layer 103. The metal contact 102 provides a negative polarity terminal to allow an external electrical circuit to be coupled to and be powered by the solar cell 100. In one embodiment, the metal contact 102 comprises silver having a sheet resistance of about

5mΩ.cm and a thickness of about 15μm. The pitch between adjacent metal contacts 102 may be about 1 to 4 mm. In one embodiment, the metal contacts 102 are spaced at 400 to 1000 μm along each metal contact 102 (see FIG. 2).

In the example of FIG. 1, the edge isolation trench 111 is formed through the silicon dioxide layer 109, the polysilicon emitter 108, and a portion of the substrate 101 to provide edge electrical isolation.

FIG. 2 is a plan view schematically showing the front side of the solar cell 100. In the example of FIG. 2, two bus bars 201 run parallel on the front side of the substrate 101. The contact holes 120, in which the metal contacts 102 are formed, may each have a diameter of about 50 to 200 μm. A plurality of metal contacts 102 is formed perpendicular to the bus bars 201. Each metal contact 102 may have a width of about 60-120μm.

FIG. 3 is a plan view schematically showing the backside of the solar cell 100. In the example of FIG. 3, two bus bars 301, which are electrically coupled to metal contacts 110, run parallel on the backside. In practice, the bus bars 201 and 301 will be electrically connected to corresponding bus bars of adjacent solar cells to form an array of solar cells.

Solar cells have gained wide acceptance among energy consumers as a viable renewable energy source. Still, to be competitive with other energy sources, a solar cell manufacturer must be able to fabricate an efficient solar cell at relatively low cost. With this goal in mind, a process for manufacturing the solar cell 100 is now discussed with reference to FIGS. 4A-4M.

FIG. 4, which comprises FIGS. 4A-4M, schematically illustrates the fabrication of the solar cell 100 in accordance with an embodiment of the present invention.

In FIG. 4A, an N-type silicon substrate 101 is prepared for processing into a solar cell by undergoing a damage etch step. The substrate 101 is in wafer form in this example, and is thus typically received with damaged surfaces due to the sawing process used by the wafer vendor to slice the substrate 101 from its ingot. The substrate 101 may be about 100 to 200 microns thick as received from the wafer vendor. In one embodiment, the damage etch step involves removal of about 10 to 20 μm from each side of the substrate 101 using a wet etch process comprising potassium hydroxide. The damage etch step may also include cleaning of the substrate 101 to remove metal contamination.

In FIG. 4B, tunnel oxides 402 and 107 are formed on the front and back surfaces, respectively, of the substrate 101. The tunnel oxides 402 and 107 may comprise silicon dioxide thermally grown to a thickness of about 10 to 50 Angstroms on the surfaces of the N-type silicon substrate 101. A layer of polysilicon is then formed on the tunnel oxides 402 and 107 to form the polysilicon layer 401 and the polysilicon emitter 108, respectively. Each of the polysilicon layer 401 and the polysilicon emitter 108 may be formed to a thickness of about 1000 to 2000 Angstroms by CVD.

In FIG. 4C, a P-type dopant source 461 is formed on the polysilicon emitter 108. As its name implies, the P-type dopant source 461 provides a source of P-type dopants for diffusion into the polysilicon emitter 108 in a subsequent dopant drive-in step. A dielectric capping layer 462 is formed on the P-type dopant source 461 to prevent dopants from escaping from the backside of the solar cell during the drive-in step. In

one embodiment, the P-type dopant source comprises BSG (borosilicate glass) deposited to a thickness of about 500 to 1000 Angstroms by atmospheric pressure CVD (APCVD) and has a dopant concentration of 5 to 10% by weight, while the capping layer 462 comprises undoped silicon dioxide formed to a thickness of about 2000 to 3000 Angstroms also by APCVD.

In FIG. 4D, the edge isolation trench 111 is formed near the edge of the substrate 101 on the backside. The trench 111 is relatively shallow (e.g., 10 μm deep into the substrate 101) and provides edge electrical isolation. In one embodiment, the trench 111 is formed by cutting through the capping layer 462, the P-type dopant source 461, the polysilicon emitter 108, the tunnel oxide 107, and into a shallow portion of the substrate 101 using a laser.

In FIG. 4E, exposed regions on the front surface of the substrate 101 is randomly textured to form the textured surface 113. In one embodiment, the front surface of the substrate 101 is textured with random pyramids using a wet etch process comprising potassium hydroxide and isopropyl alcohol.

In FIG. 4F, an N-type dopant source 412 is formed on regions of the textured surface 113 where contact holes 120 (see FIG. 1) will be subsequently formed to allow subsequently formed metal contacts 102 to electrically connect to the substrate 101. As its name implies, the N-type dopant source 412 provides a source of N-type dopants for diffusion into the front side of the substrate 101. In one embodiment, the N-type dopant source 412 is formed by inkjet printing the dopant material directly onto the substrate 101.

In one embodiment, the N-type dopant source 412 comprises silicon dioxide doped with phosphorus. Only one N-type dopant source 412 is shown in FIG. 4F for clarity of illustration. In practice, there are several dot-shaped N-type dopant sources 412, one for each region where a contact hole 120 is to be formed (see FIG. 2). This allows formation of several dot shaped N-type doped regions 106 (see FIG. 1) after a subsequently performed drive-in step now discussed with reference to FIG. 4G.

In FIG. 4G, a dopant drive-in step is performed to diffuse N-type dopants from the N-type dopant source 412 into the substrate 101 to form the N-type dope region 106, to diffuse P-type dopants from the P-type dopant source 461 to the polysilicon emitter 108, and to diffuse N-type dopants into the front side of the substrate 101 to form the N-type doped region 105. Silicon dioxide layer 109 represents layers 461 and 462 after the drive-in step. The polysilicon emitter 108 also becomes a P-type doped layer after the drive-in step. The N-type doped region 105 may be formed by exposing the sample of FIG. 4G to phosphorus in a diffusion furnace, for example. The use of the N-type dopant source 412 allows for a more controlled and concentrated N-type diffusion to the N-type doped region 106. The thin thermal silicon dioxide layer 124 may be grown on the textured surface 113 during the drive-in process.

The drive-in step to dope the polysilicon emitter 108 on the backside and to form the N-type doped regions 105 and 106 on the front side may be formed in-situ, which in the context of the present disclosure means a single manual (i.e., by fabrication personnel) loading of the substrate 101 in a furnace or other single chamber or multi-chamber processing tool. In one embodiment, the drive-in step is performed in a

diffusion furnace. The preceding sequence of steps leading to the drive-in step allows for in-situ diffusion, which advantageously helps in lowering fabrication cost.

It is to be noted that the step of using an N-type dopant source 412 to diffuse dopants into the N-type doped region 106 may be omitted in some applications. That is, in an alternative process, the formation of the N-type dopant source 412 in FIG. 4F may be omitted. In that case, the N-type doped regions 105 and 106 will be both doped by introduction of an N-type dopant in the diffusion furnace during the drive-in step. All other process steps disclosed herein remain essentially the same.

In FIG. 4H, the antireflective coating of silicon nitride layer 103 is formed over the textured surface 113 after removal of the N-type dopant source 412. Besides being an antireflective coating, the silicon nitride layer 103 also advantageously serves as a dielectric, enabling the selective contacts to be formed on the front surface to reduce front surface recombination. The silicon nitride layer 103 may be formed to a thickness of about 450 Angstroms by PECVD, for example.

In FIG. 4I, a front contact mask 420 is formed on the silicon nitride layer 103 to create a pattern 421 defining the contact holes 120 (see FIG. 1). The mask 420 may comprise an acid resistance organic material, such as a resist, and formed using a printing process, such as screen printing or inkjet printing.

In FIG. 4J, a back contact mask 422 is formed on the silicon dioxide layer 109 to create patterns 423 defining the contact holes 123 (see FIG. 1). Similar to the mask 420, the mask 422 may comprise an organic material formed using a printing process.

In FIG. 4K, contact holes 120 and 123 are formed by removing exposed portions of the silicon nitride layer 103 and the silicon dioxide 109 in a contact etch step. In one embodiment, the contact holes 120 are formed by using a selective etch process that removes exposed portions of the silicon nitride layer 103 and stops on the substrate 101. The same etch process removes exposed portions of the silicon dioxide 109 and stops on the polysilicon emitter 108. In one embodiment, the etch process comprises a BOE (buffered oxide etch).

In FIG. 4L, the metal contact 110 is formed on the silicon dioxide layer 109 to fill the contact holes 123 and make electrical connection to the polysilicon emitter 108. The metal contact 110 may be formed using a printing process. The metal contact 110 may comprise silver, which, together with the silicon dioxide layer 109, makes an excellent backside infrared reflector. Other metals may also be used as a metal contact 110, such as aluminum, for example.

In FIG. 4M, the metal contact 120 is formed on the silicon nitride layer 103 to fill the contact holes 120 and make electrical connection to the substrate 101. The metal contact 120 may comprise silver and formed using a printing process.

Formation of the metal contacts 110 and 102 may be followed by a firing step. The firing step is applicable when using screen printed silver paste as metal contacts, but not when using other processes or metals. The solar cell 100 may then be visually inspected and tested.

While specific embodiments of the present invention have been provided, it is to be understood that these embodiments are for illustration purposes and not limiting. Many additional embodiments will be apparent to persons of ordinary skill in the art

reading this disclosure.

CLAIMS

What is claimed is:

1. A solar cell, comprising:
a substrate;
a first tunnel dielectric disposed over the substrate;
an emitter disposed over the first tunnel dielectric;
a front electrode disposed over a front surface of the substrate; and
a back electrode disposed over a back surface of the substrate.

2. The solar cell of claim 1, wherein the emitter is a polysilicon emitter.

3. The solar cell of claim 1, wherein the substrate is a monocrystalline silicon substrate.

4. The solar cell of claim 1, wherein the first tunnel dielectric is a tunnel oxide.

5. The solar cell of claim 1, wherein the emitter is disposed over the back surface of the substrate.

6. The solar cell of claim 1, further comprising a second tunnel dielectric disposed on an opposite side of the substrate than the first tunnel dielectric.

7. The solar cell of claim 1, wherein the back electrode includes silver.

8. The solar cell of claim 1, further comprising an antireflective layer disposed over the front surface of the substrate.

9. A solar cell, comprising:
a substrate;
an emitter over a back surface of the substrate;

a first dielectric between the emitter and back surface;
a front electrode disposed on a front surface of the solar cell; and
a back electrode disposed on a back surface of the solar cell.

10. The solar cell of claim 9, wherein the emitter is a polysilicon emitter.

11. The solar cell of claim 9, wherein the substrate is a monocrystalline silicon substrate.

12. The solar cell of claim 9, wherein the first dielectric is an oxide.

13. The solar cell of claim 9, further comprising a second dielectric disposed on an opposite side of the substrate than the first dielectric.

14. The solar cell of claim 9, wherein the back electrode includes silver.

15. A method of fabricating a solar cell, the method comprising:
forming a first tunnel dielectric on a front surface of a substrate;
forming a second tunnel dielectric on a back surface of the substrate;
forming an emitter over the first or second tunnel dielectric;
forming a front side electrode on a front surface of the solar cell; and
forming a back side electrode on a back surface of the solar cell.

16. The method of claim 15, wherein said forming the emitter comprises forming a polysilicon emitter.

17. The method of claim 15, wherein said forming the emitter comprises forming a first silicon layer on the second tunnel dielectric.

18. The method of claim 17, further comprising forming a second silicon layer on the first tunnel dielectric

19. The method of claim 18, wherein forming the first and second silicon layers comprises forming first and second polysilicon layers, respectively.

20. The method of claim 15, wherein said forming the second tunnel dielectric comprises forming an oxide.

ABSTRACT

A bipolar solar cell includes a backside junction formed by an N-type silicon substrate and a P-type polysilicon emitter formed on the backside of the solar cell. An antireflection layer may be formed on a textured front surface of the silicon substrate. A negative polarity metal contact on the front side of the solar cell makes an electrical connection to the substrate, while a positive polarity metal contact on the backside of the solar cell makes an electrical connection to the polysilicon emitter. An external electrical circuit may be connected to the negative and positive metal contacts to be powered by the solar cell. The positive polarity metal contact may form an infrared reflecting layer with an underlying dielectric layer for increased solar radiation collection.

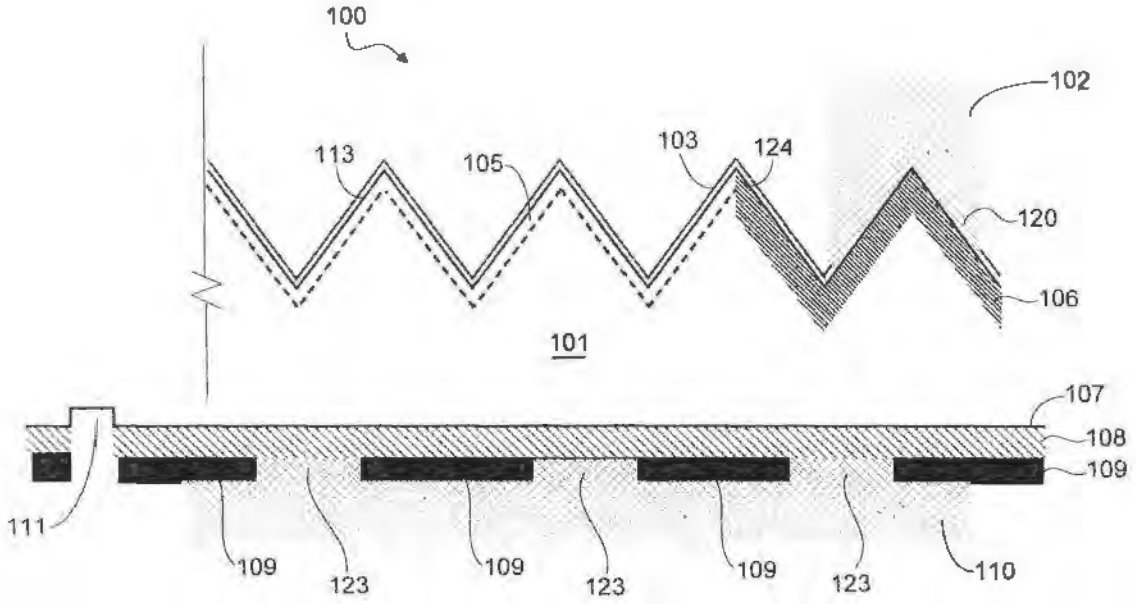

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FIG. 1

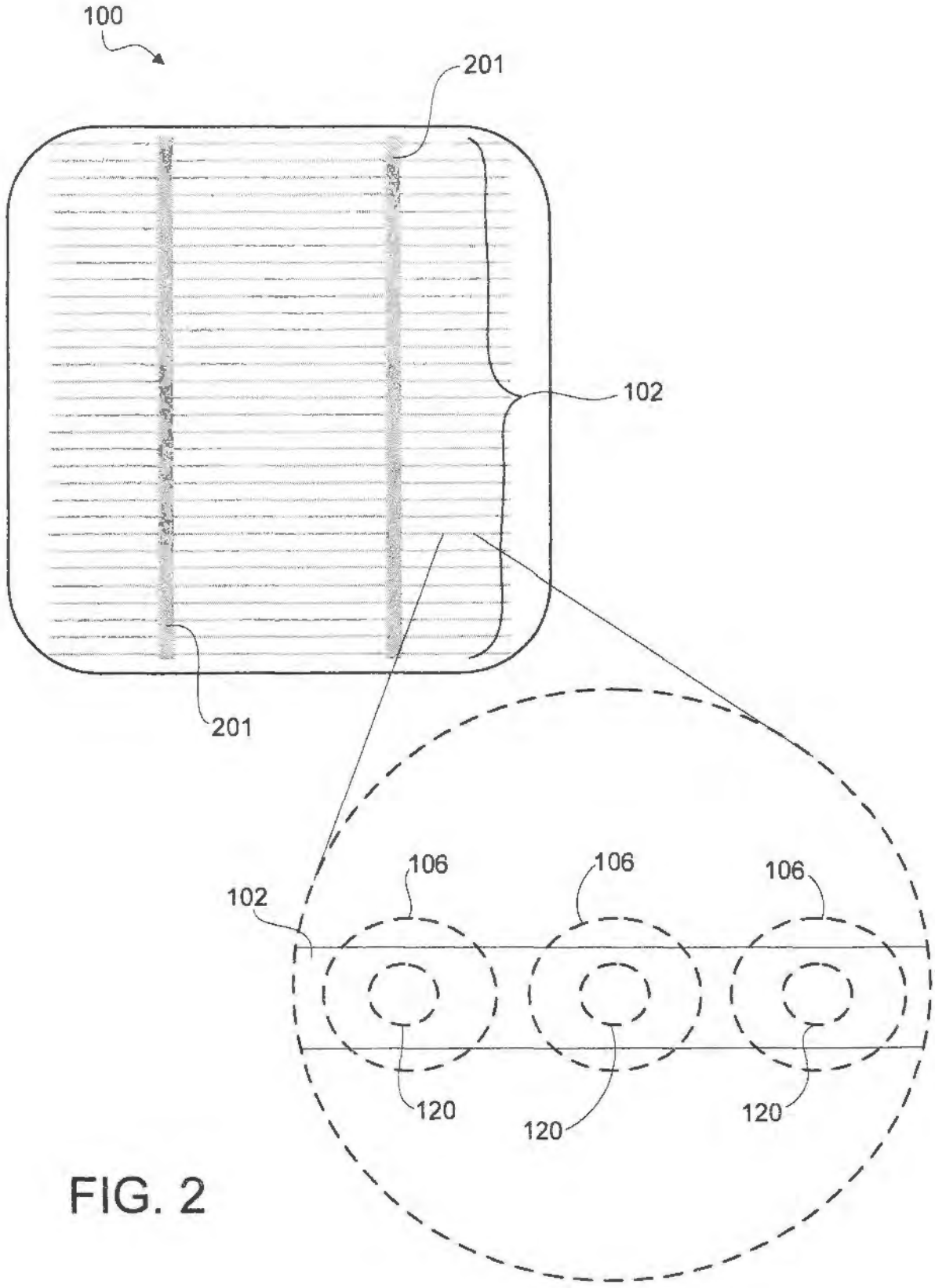


FIG. 2

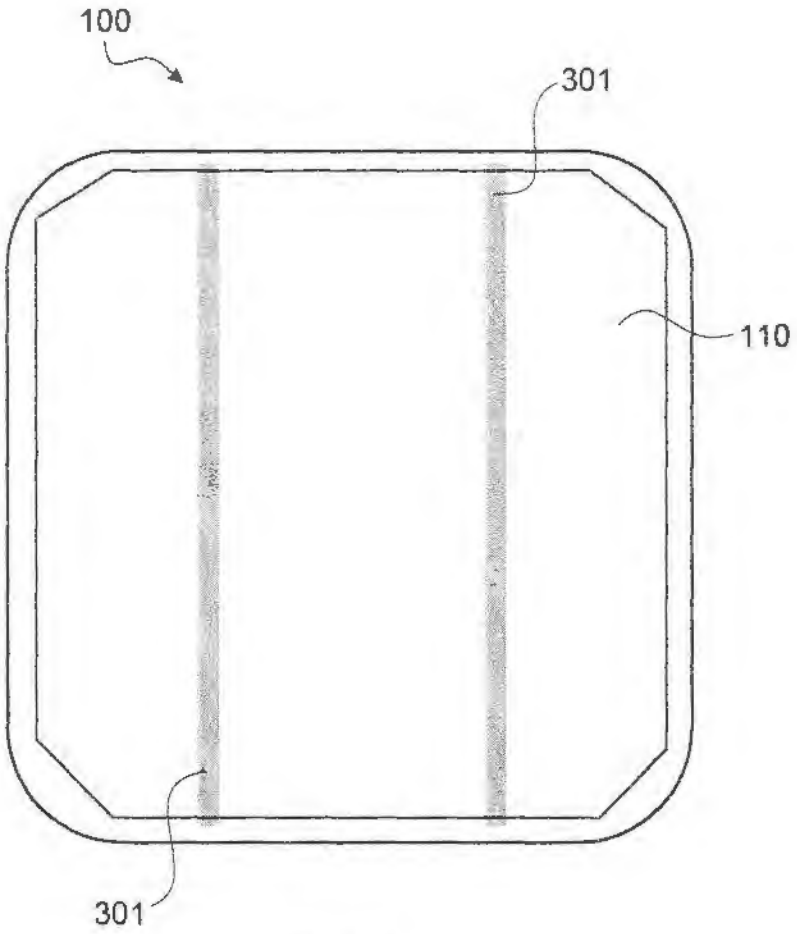


FIG. 3



FIG. 4A

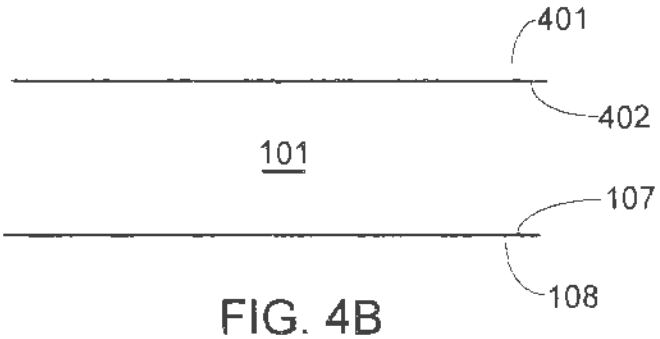


FIG. 4B

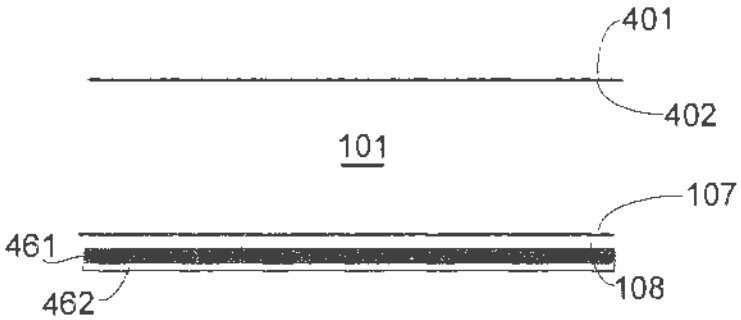


FIG. 4C

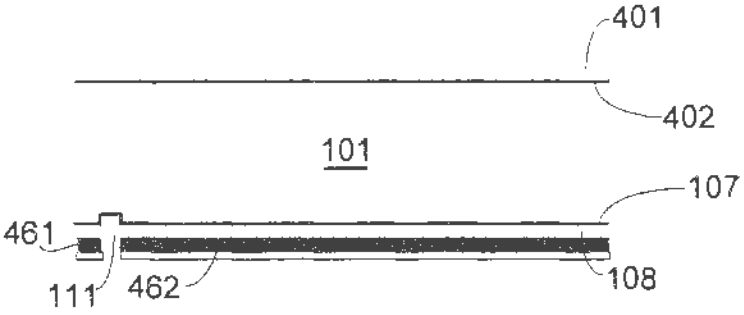


FIG. 4D

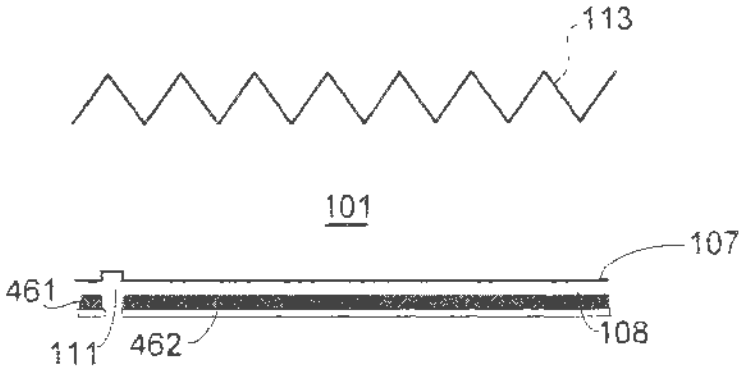


FIG. 4E

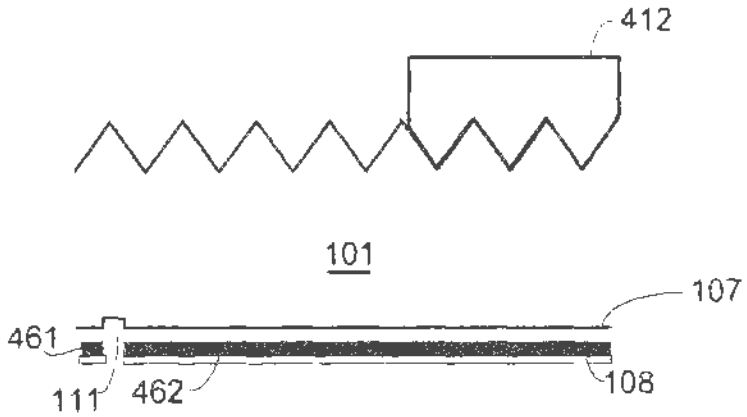


FIG. 4F

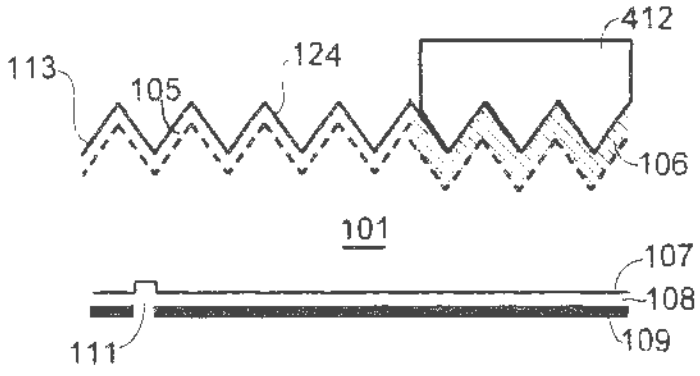


FIG. 4G

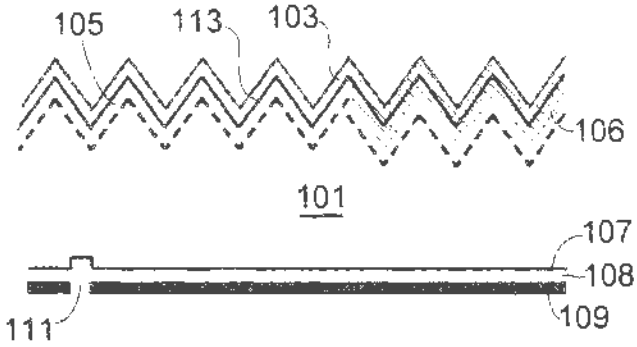


FIG. 4H

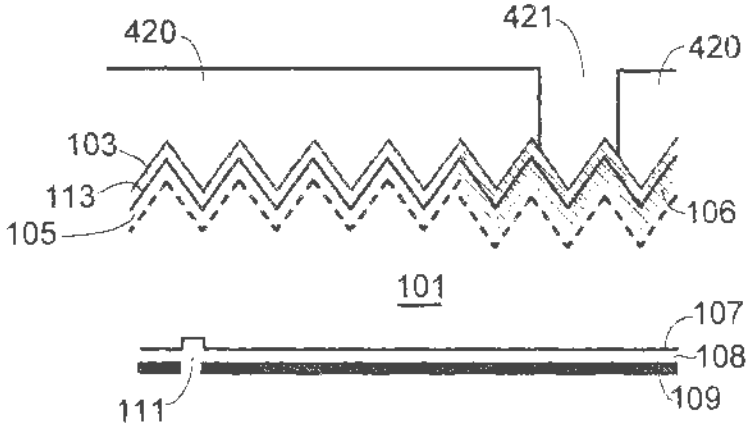


FIG. 4I

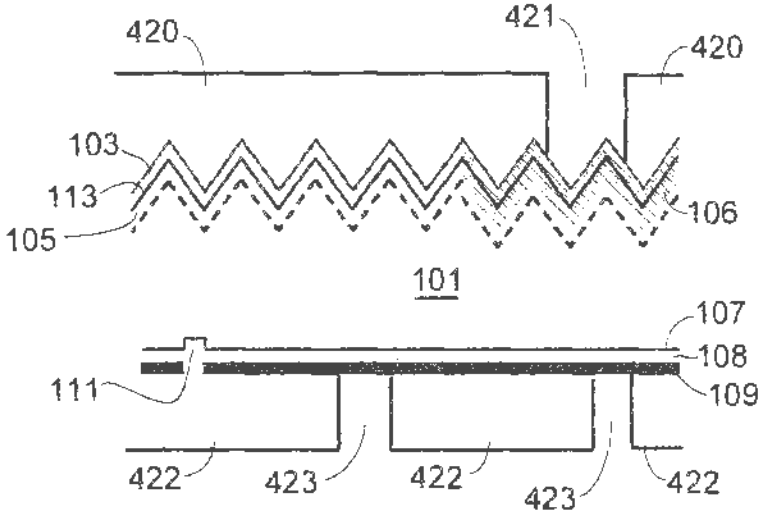


FIG. 4J

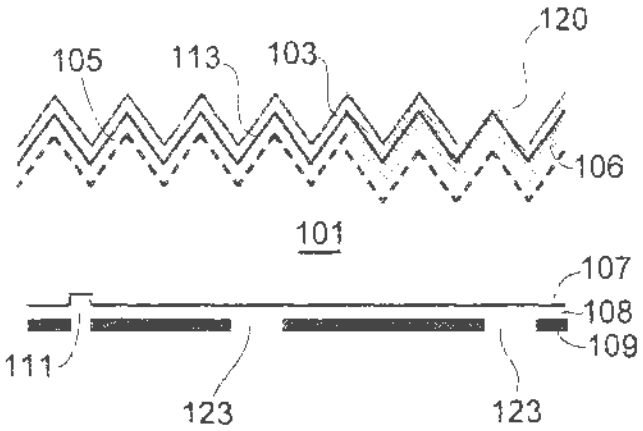


FIG. 4K

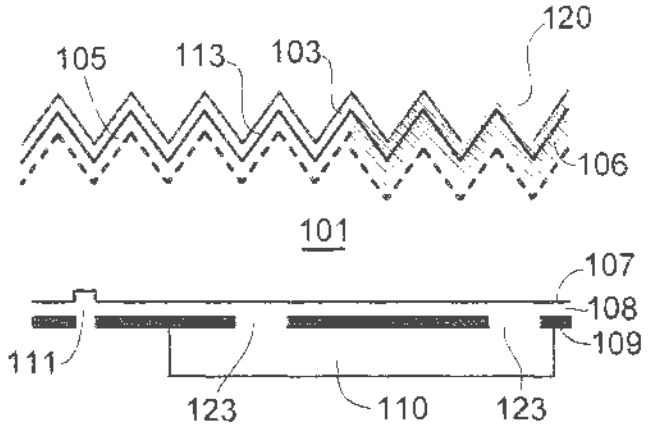


FIG. 4L

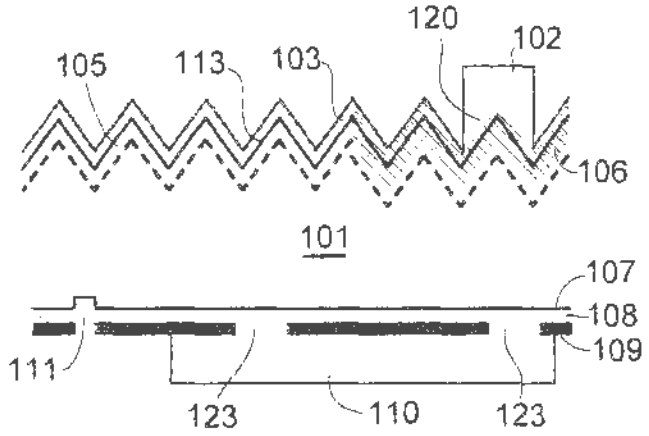


FIG. 4M

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	FRONT CONTACT SOLAR CELL WITH FORMED EMITTER
First Named Inventor/Applicant Name:	Peter John COUSINS
Filer:	Patrick D. Benedicto/jina mangaoang
Attorney Docket Number:	10031.004211

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Late Filing Fee for Oath or Declaration	1051	1	140	140
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	1740

PTO/AIA/14 (12-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10031.004211
	Application Number	
Title of Invention	FRONT CONTACT SOLAR CELL WITH FORMED EMITTER	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Peter	John	COUSINS	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Menlo Park	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	SunPower Corporation
Address 2	77 Rio Robles

City	San Jose	State/Province	CA
Postal Code	95134	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	74254		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	FRONT CONTACT SOLAR CELL WITH FORMED EMITTER		
Attorney Docket Number	10031.004211	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	7	Suggested Figure for Publication (if any)	

Filing By Reference :

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10031.004211
	Application Number	
Title of Invention	FRONT CONTACT SOLAR CELL WITH FORMED EMITTER	

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country i

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	74254		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	13/495577	2012-06-13

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/495577	Division of	12/070742	2008-02-20	8222516	2012-07-17

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10031.004211
	Application Number	
Title of Invention	FRONT CONTACT SOLAR CELL WITH FORMED EMITTER	

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10031.004211
	Application Number	
Title of Invention	FRONT CONTACT SOLAR CELL WITH FORMED EMITTER	

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(•) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. [X]

Organization Name	SunPower Corporation		
Mailing Address Information:			
Address 1	77 Rio Robles		
Address 2			
City	San Jose	**State/Province**	CA
Country [i]	US	Postal Code	95134
Phone Number		Fax Number	

PTO/AIA/14 (12-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10031.004211
	Application Number	
Title of Invention	FRONT CONTACT SOLAR CELL WITH FORMED EMITTER	

Email Address	

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	SunPower Corporation

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Remove

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Patrick D. Benedicto, Reg. No. 40,909/			Date (YYYY-MM-DD)	2014-10-02
First Name	PATRICK D.	Last Name	BENEDICTO	Registration Number	40909

Additional Signature may be generated within this form by selecting the Add button. Add

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Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10031.004211
	Application Number	
Title of Invention	FRONT CONTACT SOLAR CELL WITH FORMED EMITTER	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14504771
Filing Date	2014-10-02
First Named Inventor	Peter JOhn COUSINS
Art Unit	1757
Examiner Name	
Attorney Docket Number	10031.004211

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8222516		2012-07-17	Cousins	
	2	8878053		2014-11-04	Cousins	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2002539625	JP		2002-11-19	EBARA SOLAR, INC.		☐
	2	2009535845	JP		2009-10-01	SUNPOWER CORPORATION		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14504771
	Filing Date	2014-10-02
	First Named Inventor	Peter JOhn COUSINS
	Art Unit	1757
	Examiner Name	
	Attorney Docket Number	10031.004211

	3	H07106611	JP		1995-04-21	TONEN CORP		☐
	4	WO0055923	WO	A1	2000-09-21	EBARA SOLAR, INC.		☐
	5	WO2007130188	WO	A2	2007-11-15	SUNPOWER CORPORATION		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1		☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14504771
	Filing Date	2014-10-02
	First Named Inventor	Peter JOhn COUSINS
	Art Unit	1757
	Examiner Name	
	Attorney Docket Number	10031.004211

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Patrick D. Benedicto/	Date (YYYY-MM-DD)	2015-06-11
Name/Print	PATRICK D. BENEDICTO	Registration Number	40909

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

(19)日本国特許庁（ＪＰ）　(12) **公表特許公報（Ａ）**　(11)特許出願公表番号
特表2002－539625
（P2002－539625A）
(43)公表日　平成14年11月19日(2002.11.19)

(51)Int.Cl.'	識別記号	ＦＩ	ﾃｰﾏｺｰﾄﾞ(参考)
Ｈ０１Ｌ　31/04		Ｈ０１Ｌ　31/04	Ａ　５Ｆ０５１

審査請求　未請求　予備審査請求　有　（全 26 頁）

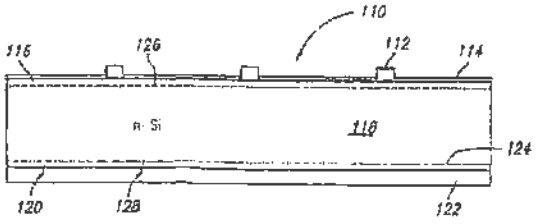
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(54)【発明の名称】　アルミニウム合金背面接合太陽電池およびその製造プロセス

(57)【要約】
太陽電池を製造するプロセスが望まれる。本プロセスは、ベース層（１１８）を設けるステップと、ベース層の非照射面（１２８）と同じ側にｐ型導電性のエミッタ層（１２０）を形成して、濃くドープされたｐ型エミッタ層およびｎ型ベース層（１１８）とｐ型エミッタ層（１２０）の間のｐ－ｎ接合（１２４）を設けるステップとを含む。本発明のベース層はｎ型導電性を有し、照射面（１２６）および照射面の反対側に在る非照射面（１２８）によって区画される。



【特許請求の範囲】

【請求項１】　ｎ型導電性のドーパント原子を含み、太陽電池が光エネルギーに曝されたとき光エネルギーが入射する照射面とその照射面の反対側にある非照射面によって区画されるベース層と、

アルミニウム合金コンタクトを含み、ｐ型導電性の層として作用する背面エミッタ層と、

ベース層の非照射面と背面エミッタ層の間に配置されたｐ－ｎ接合層とを備える太陽電池。

【請求項２】　ベース層の照射面に隣接して配置された濃くドープされたｎ型層をさらに備える請求項１に記載の太陽電池。

【請求項３】　濃くドープされたｎ型層がリン原子を含む請求項２に記載の太陽電池。

【請求項４】　濃くドープされたｎ型層に隣接して配置された反射防止膜層をさらに備える請求項２に記載の太陽電池。

【請求項５】　反射防止膜を貫通して濃くドープされたｎ型層にとどく金属コンタクトをさらに備える請求項４に記載の太陽電池。

【請求項６】　金属コンタクトが銀を含み、ベース層に対するオーム接触として作用する請求項５に記載の太陽電池。

【請求項７】　金属コンタクトが１μｍ～２０μｍの厚さを有する請求項５に記載の太陽電池。

【請求項８】　ベース層を通るホールの拡散長がベース層の厚さよりもわずかに短い請求項１に記載の太陽電池。

【請求項９】　ベース層を通るホールの拡散長がベース層の厚さにほぼ等しい請求項８に記載の太陽電池。

【請求項１０】　ベース層を通るホールの拡散長がベース層の厚さを超える請求項９に記載の太陽電池。

【請求項１１】　ｎ型ベース層が、方向性凝固によって結晶化される鋳造シリコン、エッジ確定膜供給成長、ストリング・リボン成長、チョクラルスキー、フロートゾーン、ブリッジマン、およびデンドライト・ウェブ成長から成るグル

ープから選択された１つの技法を用いて形成される請求項１０に記載の太陽電池。

【請求項１２】　ｎ型ベース層がデンドライト・ウェブ・シリコン層である請求項１１に記載の太陽電池。

【請求項１３】　ｎ型ベース層が約５Ω・ｃｍ～約１０００Ω・ｃｍの抵抗率を有する請求項１２に記載の太陽電池。

【請求項１４】　ｎ型ベース層が約２０Ω・ｃｍの抵抗率を有する請求項１２に記載の太陽電池。

【請求項１５】　ｎ型ベース層の厚さが約３０μｍ～約２００μｍである請求項１２に記載の太陽電池。

【請求項１６】　ｎ型ベース層の厚さが約１００μｍである請求項１５に記載の太陽電池。

【請求項１７】　アルミニウム合金層がエミッタ層の非照射面に対して自動位置調整コンタクトとして作用する請求項１に記載の太陽電池。

【請求項１８】　アルミニウム合金層がアルミニウム・シリコン共晶金属層である請求項１７に記載の太陽電池。

【請求項１９】　アルミニウム・シリコン共晶金属層が約１μｍ～約３０μｍの厚さを有する請求項１７に記載の太陽電池。

【請求項２０】　アルミニウム合金層がベース層の非照射面をほぼ覆う請求項１７に記載の太陽電池。

【請求項２１】　アルミニウム合金層がベース層の非照射面を部分的に覆う請求項１７に記載の太陽電池。

【請求項２２】　アルミニウム合金層がベース層の非照射面を部分に分かれた方法で部分的に覆い、互いに入り込むｎ型金属コンタクトが部分に分かれたアルミニウム合金層間の隙間に配置される請求項２１に記載の太陽電池。

【請求項２３】　ベース層への接続を容易にするために、

金属コンタクトに隣接する濃くドープされたｎ型層をさらに備える請求項２２に記載の太陽電池。

【請求項２４】　太陽電池を製造するプロセスであって、

太陽電池が光エネルギーに曝されたとき光エネルギーが入射する照射面と、その照射面の反対側にある非照射面とによって区画され、ｎ型導電性を有するベース層を用意するステップと、

ベース層の非照射面と同じ側に濃くドープされたｐ型エミッタ層を形成し、かつｎ型ベース層とｐ型エミッタ層の間にｐ－ｎ接合を形成するためにｐ型導電性のエミッタ層を形成するステップとを含むプロセス。

【請求項２５】　ベース層を用意するステップが、チョクラルスキー、フロートゾーン、ブリッジマン、方向性凝固によって結晶化される鋳造シリコン、エッジ確定膜供給成長（ＥＦＧ）、ストリング・リボン成長、およびデンドライト・ウェブ成長から成るグループから選択された１つの技法を用いてｎ型導電性の単結晶シリコン基板を製造するステップを含む請求項２４に記載のプロセス。

【請求項２６】　ベース層を用意するステップが、デンドライト・ウェブ成長を用いてｎ型導電性の単結晶シリコン基板を製造するステップを含む請求項２５に記載のプロセス。

【請求項２７】　エミッタ層を形成するステップが、

アルミニウム層をベース層の非照射面上に設けるステップと、

ベース層の一部をエミッタ層に変換するために背面からのアルミニウムをベース層の少なくとも一部と混合して合金にするステップとを含む請求項２４に記載のプロセス。

【請求項２８】　ベース層がシリコンを含み、合金にするステップが、アルミニウム原子をｐ型ドーパントとして含むエミッタ層、およびアルミニウム・シリコン合金を含むエミッタ層の背面に対する自動位置調整コンタクト層を形成する請求項２７に記載のプロセス。

【請求項２９】　アルミニウムを形成するステップが、

ベース層の非照射面上にアルミニウムをスクリーン印刷するステップを含む請求項２８に記載のプロセス。

【請求項３０】　合金にするステップが、約７００℃～約１０００℃の温度で実施される請求項２８に記載のプロセス。

【請求項３１】　合金にするステップが、温度を約１分～約３０分の間保持

することによって実施される請求項２８に記載のプロセス。

【請求項３２】　ベース層の照射面が、約０．１μｍ～約１μｍの厚さを有するリンがドープされた層によって不活性化される請求項２８に記載のプロセス。

【請求項３３】　２酸化チタニウムを含む反射防止膜を形成するステップ、または窒化シリコンがリンかドープされた層上に形成されるステップをさらに備える請求項３２に記載のプロセス。

【請求項３４】　ｎ型金属コンタクトがベース層の上に形成されて、ベース層に対するオーム接触を形成させる請求項３３に記載のプロセス。

【請求項３５】　ｎ型金属コンタクトがベース層の下に形成されて、ベース層に対するオーム接触を形成させる請求項３４に記載のプロセス。

【請求項３６】　アルミニウム層を形成するステップが、合金にするステップで形成されたアルミニウム合金層がエミッタ層の裏側をほぼ覆うように、アルミニウムを供給するステップを含む請求項２７に記載のプロセス。

【請求項３７】　アルミニウム層を形成するステップが、

合金ステップがベース層の非照射面を部分に分かれた方法で覆うエミッタ層を形成するように、ベース層の非照射面を部分的に覆うアルミニウム層を供給するステップを含む請求項２７に記載のプロセス。

【請求項３８】　部分に分かれたアルミニウム合金層間の隙間に配置された、かつ互いに入り込むｎ型金属コンタクトを形成するステップをさらに含む請求項３７に記載のプロセス。

【請求項３９】　ベース層のほぼすべての露出された照射面および非照射面を誘電層で不活性化するステップをさらに含む請求項２４に記載のプロセス。

【発明の詳細な説明】

【０００１】

（発明の背景）

本発明は改良型太陽電池およびその製造プロセスに関する。より詳細には、本発明は太陽電池の非照射面付近に配置されたｐ－ｎ接合を含む太陽電池およびその製造プロセスに関する。

【０００２】

太陽電池は太陽のような光源からの容易にアクセスできるエネルギーを電力に変換して、電気的に駆動される装置、例えば、家庭で使用される計算器、コンピュータおよびヒータを動作させるので、それらは広く使用されている。図１が従来のシリコン太陽電池１０を構成する層状スタックの断面を示す。従来のシリコン太陽電池１０は、通常ｐ型ベース層１８とｎ型層１６にはさまれたｐ－ｎ接合２４を含み、これは照射面（前面）１１付近に配置される。ここで用いられる用語「照射面」は、太陽電池が能動的すなわち動作中である場合に光エネルギーに曝される従来の太陽電池の表面を指す。したがって、用語「非照射面」は照射面の反対側の表面を指す。ｐ－ｎ接合２４の基本構造が、照射面１１またはその付近に、かつ中ぐらいにドープされた（約$10^{17}cm^{-3}$）ｐ型ベース層（ｐ）１８の上に配置された、濃くドープされた（約$10^{19}cm^{-3}$）ｎ型エミッタ（ｎ＋）１６を含む。従来の太陽電池の商用の実施形態は、通常、任意の反射防止膜１４およびｐ型ベース層１８とｐ型シリコン・コンタクト２２の間に形成されたｐ＋層２０を含む。

【０００３】

ｐ－ｎ接合２４のｎ＋エミッタ層１６の上からの典型的な深さは約０．５μｍである。少数キャリアの収集を促進するために、浅い上面のｐ－ｎ接合２４が望まれる。ｐ型ベース層１８中に浸透しベース層１８によって吸収される光の各フォトンが、そのエネルギーを結合状態（共有結合）に在る電子に与えて、それを自由にする。この自由電子、およびそれが後に残した共有結合中のホール（ホールも動ける）が、太陽電池から流れる電流の潜在的な要素を構成する。この電流に寄与するために、電子およびホールは再結合できず、むしろｐ－ｎ接合２４に

関連する電界によって分離される。これが起きた場合は、電子はｎ型シリコン・コンタクト１２に移動し、ホールはｐ型シリコン・コンタクト２２に移動するであろう。

【０００４】

太陽電池電流に寄与するために、光によって発生された少数キャリア（ｎ　エミッタ層内のホールとｐ型ベース層内の電子）は、それらが収集されるｐ－ｎ接合２４に拡散によって移動できるように、十分に長い時間存在する必要がある。少数キャリアが多数キャリアと再結合することによって失われずに移動できる平均距離が、少数キャリア拡散長と呼ばれる。少数キャリア拡散長は、一般にシリコン結晶中の欠陥（例えば、再結合中心）の密度およびシリコン中のドーパント原子の濃度のような要因に依存する。欠陥またはドーパント原子のどちらか一方の密度が大きくなるにつれて、少数キャリア拡散長は短くなる。したがって、濃くドープされたｎ　エミッタ層１６内のホールに対する拡散長が、中ぐらいにドープされたｐ型ベース層１８内の電子に対する拡散長よりもかなり短い。

【０００５】

ｎ＋エミッタ層１６は、エミッタ層１６中で生成された少数電荷キャリアがｐ－ｎ接合２４まで再結合によって失われずに拡散することがほとんどできないほぼ「空の層」であることを当業者が認識するだろう。様々な理由で、浅い、またはできるだけエミッタ層１６の表面に近いｎ　エミッタ層１６を有することが望ましい。例として、浅いエミッタ層によって比較的少数のフォトンがｎ　エミッタ層１６中で吸収され得る。さらに、ｎ＋エミッタ層１６中で生成された、かつ結果として生じた光によって発生された少数キャリアが、ｐ－ｎ接合２４の十分近くに在るので、収集される可能性がある（拡散長≧接合深さ）。

【０００６】

あいにく、従来の太陽電池の設計では、ｎ＋エミッタ層の深さが制限され、望むとおりに浅くすることができない。エミッタ・コンタクト１２、特にスクリーン印刷および焼成によって形成されたコンタクトからの金属が、ｐ－ｎ接合２４内に浸透し、それを破壊または劣化することがある。ｐ－ｎ接合２４内の金属の存在は接合を「短絡」または「シャント接続」する。したがって、電池によって

生成された電流を増進するためには、浅いかつ薄くドープされたｎ＋エミッタ層１６が望まれるが、しかし実際に、ｎ＋エミッタ層１６は、ｐ－ｎ接合２４をシャント接続するのを避けるために必要とされるよりも比較的より深くかつより濃くドープされている。その結果、従来の太陽電池では、深いｎ　エミッタ層１６によって電池によって生成された電流の量を損なう。

【０００７】

必要とされるものは、長い少数キャリア拡散長を有し、ｐ－ｎ接合のシャント接続を排除し、そして生成された電流の量を損なわないシリコン太陽電池を製造する構造およびプロセスである。

【０００８】

（発明の概要）

１つの態様において、本発明は太陽電池を提供する。太陽電池はｎ型導電性のドーパント原子を有し、照射面および非照射面によって区画された基本層を含む。太陽電池が光エネルギーに曝され，かつ非照射面が照射面の反対側に在る場合に、照射面はそれに当たる光エネルギーを有する。太陽電池は、ｐ型導電性の層として作用させるアルミニウム合金から作られる背面エミッタ層をさらに含む。太陽電池は、ベース層の非照射面と背面層の間に配置されたｐ－ｎ接合層をさらに含む。

【０００９】

別の態様において、本発明は太陽電池を製造するプロセスを提供する。プロセスは、（１）ベース層を設けるステップと、（２）ベース層の非照射面と同じ側にｐ型導電性のエミッタ層を形成して、濃くドープされたｐ型エミッタ層およびｎ型ベース層とｐ型エミッタ層の間のｐ－ｎ接合を形成するステップとを含む。本発明のベース層はｎ型導電性を有し、照射面および非照射面によって区画されている。太陽電池が光エネルギーに曝され、かつ非照射面が照射面の反対側に在る場合に、照射面はそれに当たる光エネルギーを有する。

【００１０】

本発明のこれらの特徴および他の特徴が、本発明の詳細な記述で、かつ次の図と共に以下により詳しく説明されるだろう。

【００１１】

本発明を限定的ものではなく，例示的なものとして添付の図面に示す。

【００１２】

（好ましい実施形態の説明）

次いで、添付の図面に示す現在好ましい実施形態を参照して、本発明を詳細に説明する。以下の説明では、本発明の完全な理解を提供するために、多数の特定の細部を説明する。しかし本発明は、これらの特定の細部の一部または全部を用いずに実施できることは当業者には明らかであろう。他の例では、周知のプロセス・ステップおよび／または構造は、本発明を不必要に分かりにくくしてしまわないために、詳細には説明していない。

【００１３】

所与のドーピング濃度に対して，少数キャリア電子拡散長（すなわちｐ型シリコン中の電子）は、一般に少数キャリア・ホール拡散長（すなわちｎ型シリコン中のホール）とは異なるということを念頭におくことは重要である。この差は、結晶欠陥の性質に依存する可能性があり，この結晶欠陥は、再結合中心として作用する可能性がある。例えばデンドライト・ウェブ・シリコンでは，主欠陥は、転位核上に核形成する酸化シリコンの沈殿物である。酸化シリコン沈殿物と周囲のシリコンとの間の界面は、その２つの材料の原子構造の不整合のために、正電荷を搬送する。負荷電少数キャリア電子は、そのような正荷電界面に引き寄せられる。そのような欠陥は，多数の多数キャリア・ホールのうちの１つがその欠陥によって移動し、そのとき電子が再結合事象でホールに落ち込むまで、電子を捕獲し，保持する可能性がある．

【００１４】

したがって本発明では．太陽電池基板層に関して．ｐ型ドーピングで得られる少数キャリア拡散長よりも高い少数キャリア拡散長を達成するためにｎ型ドーピングが望ましいことが理解される．ｎ型導電性を有する太陽電池基板は．ｎ型ベース層を必要とする。したがってｐ－ｎ接合は、ホウ素を含む照射側で，ｎ型ベース層およびエミッタ層を使用して製造される。ホウ素は，ｐ型ドーパントとして実際的な選択である。

【００１５】

残念ながら、ホウ素拡散は、しばしば、ホウ素－シリコン化合物の形成のために、汚染されたシリコン表面を残すことが判明した。そのような汚染は、太陽電池の表面の外観を重大に低下させる。ホウ素汚染は、汚染した表面を熱酸化し、その後熱酸化物を化学的に除去するなど、追加の、かつ望ましくない処理ステップという代償を払うことで除去することができる。したがって、本発明の発見により、ｎ型ドーピングの方がｐ型ドーピングよりも高い少数キャリア拡散長を与えるシリコン材料に対して、正面のｐ－ｎ接合の望ましさは、ｐ型エミッタ層のホウ素汚染の存在によって相殺される。

【００１６】

図１に戻ると、市販の太陽電池１０はｎ　ｐｐ　構造を有する。ｎ型エミッタ層１６は、リン拡散（リンでは汚染は問題ではない）を用いて一般に作成され、シリコン基板はｐ型にドープされ、背面シリコン表面２０は、一般に、コンタクト金属層２２とのオーム接触を促進するようにｐ　にドープされる。オーム接触は低抵抗を有する。オーム接触間に発生する電圧は、そのコンタクトを通って流れる電流と線形の関係を有する。それとは対照的に、整流接触間に発生する電圧は、そのコンタクトを通って流れる電流と非線形の関係を有する。アルミニウム－シリコン合金を使用して、ｐ　ドーピングおよび背面金属コンタクトを得ることができる。より重要なことに、市販の太陽電池１０は、セルの正面に位置するｐ－ｎ接合２４を有する。したがって前述の通り、ｎ＋エミッタ層１６は、正面の接合のシャント接続を回避するために望まれる深さよりも深くされる。ｎ型ドーピングで優れた少数キャリア拡散長を有するシリコン材料を正面のｐ－ｎ接合として使用すべき場合、ｐ型エミッタ層は、実用的なものとするためにホウ素ドープされる。前述のように、ホウ素ドーピングは、汚染した表面を与え、それによってセル外観が低下し、追加の、かつ望ましくない処理を用いなければ除去することができない。

【００１７】

したがって、本発明は、太陽電池の背面に位置するｐ－ｎ接合を設ける。図２は、本発明の一実施形態による太陽電池層スタック１１０を示す。この太陽電池

層スタック１１０は背面（ベース層の非照射面近く）に位置するｐ－ｎ接合を有する。したがって正面の金属コンタクト１１２がｐ－ｎ接合をシャント接続することは不可能である。シリコンｐ＋層中のドーパントとしてアルミニウムが好まれるので、アルミニウムが接合をシャント接続することも不可能である。

【００１８】

太陽電池スタック１１０は、ｎ型導電性のベース層１１８を含み、ベース層１１８は、照射面（正面または上面）１２６および非照射面（背面または底面）１２８によって区画される。ベース層１１８の照射面１２６近くの部分は、シリコン層中へのリン拡散によって一般に形成される浅いｎ＋層１１６によって不活性化される。したがってこの実施形態は、従来のｎ＋層の利点を実現し、しかもホウ素汚染の影響を受けない。任意選択の反射防止（ＡＲ）膜１１４が、ｎ＋層１１６の上端に配置される。この被覆が図２に示すように存在する場合、銀コンタクト１１２がＡＲ被覆１１４を貫通し、ｎ＋シリコン層１１６の表面に達する。

【００１９】

ｐ－ｎ接合１２４は、非照射面１２８、またはベース層１１８とアルミニウム・ドープト・シリコン層１２０との間の界面で形成される。アルミニウム・ドープト・シリコン層１２０は、本発明の太陽電池層スタック中でｐ＋エミッタ層としての働きをする。アルミニウムがシリコンと合金化されるときに得られるアルミニウム－シリコン共晶金属層１２２が、ｐ＋層１２０の下に配置され、ｐ＋エミッタ層１２０への自己整合型コンタクトとしての働きをする。ホウ素ドーピングが図２の太陽電池構造に存在せず、その結果正面の外観を損なうホウ素汚染がないことは注目に値する。

【００２０】

セル１１０の背面側でのｐ－ｎ接合の配置は、図２に示す太陽電池１１０の独自の特徴である。他の現在のシリコン太陽電池の設計には、そのようなアルミニウム合金背面接合を使用しているものはないことに留意されたい。さらに、ｐ－ｎ接合１２４がセル１１０の背面側にあるので、ｎ＋層１１６の深さは、シャント接続に関して実際に何の関係もない。

【００２１】

一実施形態によれば、ｎ型ベース層１１８は、一般に約５Ω・ｃｍ～約１００Ω・ｃｍの間の固有抵抗を有し、好ましくは約２００Ω・ｃｍの固有抵抗を有するデンドライト・ウェブ・シリコン結晶である。このデンドライト・ウェブ・シリコン基板結晶の厚さは、一般に約３０μｍ～約２００μｍの間にあり、好ましくは約１００μｍである。セル１１０を実用的なエネルギー変換効率レベルで動作させるために、この実施形態の１つの実施では、ｎ型ベース層１１８中のホール拡散長は、ベース層１１８の厚さよりもわずかに小さい。しかし好ましい実装では、ホール拡散長はベース層１１８の厚さにほぼ等しく、ベース層１１８の厚さを超えることがより好ましい。

【００２２】

セルの正面近くではなく、セルの背面近くにｐ－ｎ接合を位置付けることは、当技術分野の技術者にとって直感に反することである。単位深さあたり吸収される光子の数が照射面から背面に向かって進むにつれて減少するので、セルの正面近くにｐ－ｎ接合を有することが通常は望ましい。例えば、約５２％の入射光子が、ベース層の初めの照射面から５μｍ内で吸収され、約１０％が第２の５μｍスライス深さ内で吸収され、約６％が第３の５μｍスライス内で吸収される。実際に、約７５％の入射光子がベース層の上部の３０μｍ内で吸収される。

【００２３】

光子の吸収によって電子－ホール対が生成され、対の少数キャリア・メンバが、収集されるために接合に拡散するので、ｐ－ｎ接合を照射面近くに配置することは合理的である。大まかではあるが、接合からある拡散長を超えて生み出されるこれらの少数キャリアは収集されず、したがって太陽電池の光電流に寄与しないことになる。

【００２４】

図３Ａ～３Ｄに、本発明の一実施形態による、製造工程の様々な段階で形成される重要な中間の太陽電池構造を示す。ここに示す本発明の工程の実施形態は、周知の従来技法、例えばチョクラルスキー、フロートゾーン、ブリッジマン、エッジ確定膜供給成長成長（ｅｄｇｅ　ｄｅｆｉｎｅｄ　ｆｉｌｍ－ｆｅｄ　ｇｒｏｗｔｈ：ＥＦＧ）、ストリング・リボン成長（ｓｔｒｉｎｇ　ｒｉｂｂｏｎ

ｇｒｏｗｔｈ）、方向性凝固によって結晶化された鋳造シリコン、およびデンドライト・ウェブ成長を用いてｎ型導電性の単結晶シリコン基板を製造することによって開始することができる。しかし好ましい実施形態では、デンドライト・ウェブ成長技法を実施して、ｎ型単結晶基板を生成することができる。

【００２５】

図３Ａを参照すると、ｎ型単結晶は、後で下側に太陽電池のｐ－ｎ接合が形成されるベース層２１８としての働きをする。次のステップでは、半導体および太陽電池製造技術分野の技術者に周知の拡散処理ウェルを用いて、ベース層２１８の上端に濃くドープされたｎ型層２１６（以下で「ｎ　層」と呼ぶ）が形成される。本発明の一実施形態によれば、リンを含む層がベース層２１８の上面に付着され、リン原子が何らかの熱源によってベース層２１８中に拡散される。このリン層は、スクリーン印刷ペーストまたは液体ドーパントから作成されることが好ましく、熱源は、約７５０℃～約１０５０℃の間の温度に維持され、好ましくは約９５０℃に維持される急速熱処理（ＲＴＰ）ユニットまたはベルト炉である。これらの温度では、拡散時間は一般に約３０秒～約３０分の間であり、好ましくは約５分である。その結果、一般に約０．１μｍ～約１μｍの間の厚さを有し、好ましくは約０．３μｍを有し、かつ一般に約１０Ω／ｓｑｕａｒｅ～約２００Ω／ｓｑｕａｒｅのシート抵抗を有し、好ましくは約４０Ω／ｓｑｕａｒｅを有するリンがドープされたｎ　不活性化層が形成される。

【００２６】

あるいは、別の実施形態では、ベース層２１８の上面をリン・イオン注入にさらし、ベース層の上面近くの部分をｎ　層２１６に変換する。

【００２７】

別の実施形態では、ベース層２１８がかなりの正または負電荷を持った透明な誘電体層で不活性化させてもよい。この実施形態の１つの実施では、ベース層は、約５０Å～約５００Åの間の厚さを有し、好ましくは約１５０Åの厚さを有する熱的に成長した二酸化シリコンの層で不活性化される。この実施形態では、ベース層２１８の不活性化は、一般に約８００℃～約１０５０℃の間の温度の、好ましくは約１０００℃の温度の急速熱処理ユニットで実施することができる。そ

のような熱処理は、一般に約３０秒～約３０分間、好ましくは約５０秒間実施される。ｎ層がどのように不活性化されるか、またはｎ´層が不活性化されるかどうかに関わらず、ｎ´層２１６の形成の終わりに、高－低接合（ｎ´ｎ）がベース層２１８の上端側に形成されることを当業者は理解されよう。

【００２８】

次いで、図３Ｂに示すように、ｎ´層２１６の上に反射防止膜２１４を付着させることができる。例として、窒化シリコンのプラズマ増速化学蒸着（ＰＥＣＶＤ）または二酸化チタンの大気圧化学蒸着（ＡＰＣＶＤ）を実施して、反射防止膜２１４を形成する。

【００２９】

次に、従来の技法を使用して、ベース層２１８の底面または非照射面上にアルミニウム層２２２を堆積させることができる。本発明の一実施形態によれば、純粋アルミニウム・ペーストをベース層２１８の底面にスクリーン印刷することによってアルミニウムを堆積させる。この実施形態の１つの実施では、一般に約５μｍ～約３０μｍの間の厚さに、好ましくは約１５μｍの厚さにセルのほぼ背面全体にわたってスクリーン印刷することによって、アルミニウム層２２２が堆積する。次いで部分的に製造された太陽電池は、層２２２からの少なくとも一部のアルミニウムがベース層２１８と合金化するように、アルミニウム－シリコン共融温度約５７７℃よりも十分上の温度、例えば一般に約７００℃～１０００℃の間の温度、好ましくは約８００℃の温度で、十分長い期間、例えば一般に約０．１分～約１０分の間、好ましくは約２分の間放射加熱ベルト炉中で熱せられる。合金化工程の間、ベルト炉内の温度処理は、アルミニウムが効果的にシリコンを溶解するのに十分高い温度である。そのような高温では、アルミニウム層の約１／３の厚さのベース層の部分は効果的に溶解し、図３Ｃに示すｐ＋層２２０が生み出される。例として、約８００℃では、１５μｍ厚のアルミニウム層２２２はシリコン・ベース層の５μｍの部分を溶解する。したがって、ｐ＋層２２０は、アルミニウムがドープされたシリコンで、コンタクト層２２２は、重量約８８％のアルミニウムと、重量約１２％のシリコンとの共融組成物である合金である。

【００３０】

ｐ　エミッタ層は以下に説明するように生み出される。シリコンが冷えるにつれて、シリコンは、下にあるシリコン上で凝固または成長し続け、立方センチメートルあたりアルミニウム原子約１０^{18}～約１０^{19}個程度の中程度の量のアルミニウム・ドーパントも取り込む。アルミニウム原子の濃度は、シリコン原子の濃度よりも著しく小さく、シリコン原子の濃度は、立方センチメートルあたり約５×１０^{22}個と約１００００倍大きい。図３Ｃに示すように、この層を冷却した後、非照射面近くのベース層２１８の一部は、液相エピタキシによって、濃くドープされたｐ型層２２０（以下では「ｐ　層」と呼ぶ）に変換される。溶解したシリコンの一部は、アルミニウムーシリコン共晶層２２２の部分となる。アルミニウムによって溶解されなかったシリコンは、シリコン結晶がエピタキシアルに再成長したときにシリコン結晶を再構築するためのテンプレートとしての働きをする。

【００３１】

アルミニウムーシリコン共晶金属層２２２は、良好な導体であり（低電気抵抗を有し）、太陽電池への自己整合型型金属層コンタクトとしての働きをする。アルミニウムーシリコン共晶金属層２２２の厚さは、一般に約１μｍ～約３０μｍの間にあり、好ましくは約１５μｍである。

【００３２】

図３Ｄに、金属コンタクトを付着し、任意選択の反射防止膜を貫通した後の構造を示す。例として、銀層は、ｎ　層２１６上にスクリーン印刷され、格子型に正面の約７％をカバーする。銀は、スクリーン印刷によって一般に約５μｍ～約２０μｍの間の厚さ、好ましくは約１０μｍの厚さまで堆積させることができる。次いで得られる部分的に製造された太陽電池構造は、一般に約７００℃～約９００℃の間の温度に、好ましくは約７６０℃の温度に維持されるベルト炉を通り抜ける。炉を通り抜ける時間は、銀ペースト中の不純物がシリコン中に拡散することを回避するために短くされる。本発明の一実施形態では、セルがベルト炉を通り抜ける時間は０．１分～約１０分の間である。しかし、好ましい実施形態では、この時間は約４０秒である。銀のｎ$^{+}$層２１６へのオーム接触２１２の厚さは、一般に約１μｍ～約２０μｍの間であり、好ましくは約１０μｍである。任

意選択の反射防止膜を堆積させる場合、銀層はその膜を貫通する。（反射防止膜を有する操作と有さない操作の）どちらの操作も、放射加熱ベルト炉中で実行することができる。本発明の製造ステップは、高スループットおよび低コストの製造を実現する。

【００３３】

図４に、本発明のフル背面金属カバレッジを有する、アルミニウム合金背面接合デンドライト・ウェブ・シリコン太陽電池についての光エネルギーから電気エネルギーへの変換効率が約１２．５％であることを示すＩ－Ｖ曲線を示す。図４に示すデータを得るために使用した太陽電池は、約１００μｍの通常の厚さを有し、約２５ｃｍ^{2}の領域を有する。他のパラメータには、短絡電流密度約２８．２ｍＡ／ｃｍ^{2}、開路電圧約０．５９５Ｖ、および充填率約０．７４７が含まれる。曲線のニー（ｋｎｅｅ）は、V_{mp}が約０．４８０ＶかつI_{mp}が約０．６５３Ａである所で最大電力点を示す。

【００３４】

図５に、図４の太陽電池についてのスペクトル反射率（濃い三角）５１０、外部量子効率（白抜きの四角）５１２、および内部量子効率（濃い四角）５１４の測定結果を示す。測定した反射率により、長波長（＞９５０ｎｍ）光の約４７％が、背面のアルミニウム－シリコン共晶金属層から反射されることが示される。次いでこの反射光は、シリコンを通過する第２経路を得て、全体の効率に加算される。１次元有限要素モデルＰＣ１Ｄを用いた内部量子効率の計算により、このセルのベース中のホール拡散長約２００μｍが示される。これは、良好な性能のために必要なセル厚の２倍である。内部量子効率曲線は、ｐ－ｎ接合がセルの背面にあることを示す、約５００ｎｍ～約８５０ｎｍの範囲にわたる正の傾きを有し、このことも注目に値する。従来の太陽電池では、内部量子効率曲線は、ｐ－ｎ接合がセルの正面であることを示す、負の傾きを示す。

【００３５】

図６に、本発明の別の実施形態による太陽電池層スタック３００を示す。太陽電池３００は、ｐ型層に変換され、金属でカバーされる背面の部分だけが異なること以外、図２の太陽電池１１０とほぼ同じである。したがって、太陽電池３０

０は、背面全体が金属でカバーされている図２の太陽電池１１０に示すような「フル」金属カバレッジとは対照的に、「部分的」金属カバレッジを有していると呼ばれる。図６の部分的金属カバレッジ設計は、共融温度約５７７℃から冷却する際の、シリコンとアルミニウム－シリコン共晶層との間の異なる熱収縮に起因する薄いセルのそりをなくする。そのようなそりはフル背面カバレッジを使用するときに生じることがあることを念頭におくことは重要である。セグメント化された金属は、やはりアルミニウムのコストを低減する。かなりのエネルギー変換効率を得る目的で、背面の金属アイランドの間の露出したｎ型ベース層面３３０を不活性化することができる。例として、この不活性化ステップは、アルミニウム合金化ステップの後に、急速熱処理ユニットで約１０００℃で約５０秒間、約１１５Åの厚さの熱酸化物を成長させることによって実行することができる。この準備活動で反射防止膜を適用することはできない。スクリーン印刷された金属を有するが、反射防止膜を有さない２５ｃｍ² のデンドライト・ウェブ・シリコン・セルに対して、最大約６．８％の効率が得られる。反射防止膜での期待される効率は、約９．９％である。

【００３６】

図７に、本発明の別の実施形態による太陽電池層スタック４００を示す。太陽電池４００は、ｎ型ベース層へのｎ型コンタクト４１２をセルの正面からセルの背面に移動させて金属層４２２と相互に配置したこと以外、図６の太陽電池３００とほぼ同じである。

【００３７】

この図７に示す構造は、正面をコンタクトによって覆うことをゼロに減少させるという追加の利点を有する。モジュール中のセルを相互接続することも、表面マウント技術を使用することができるという点で、セルの背面側上の両方のコンタクトでより単純となることが期待される。別のステップで銀コンタクト４１２に隣接するｎ＋領域４２４を形成することもできる。あるいは、このｎ型ドーパントの源は、純粋の銀ではなく、銀－アンチモン合金などの自己ドーパント・コンタクト金属を使用する場合、コンタクト材料自体でもよい。スクリーン印刷された金属、二酸化チタン反射防止膜、および約２．５ｃｍ² の領域を有するこの

タイプのプロトタイプ・デンドライト・ウェブ・シリコン太陽電池は、約１０．４％の効率を有した。

【００３８】

本発明をシリコン結晶基板およびアルミニウムによって説明したが、他の基板および導電性材料を同様に使用することができない理由はない。したがってさらに、アルミニウム合金背面接合太陽電池を製造するための、新しい新規の構造および工程が説明されたことを理解されよう。本明細書の教示が与えられると、本明細書で開示された発明を組み込む多数の代替方法および均等物が存在することを、当業者は理解されよう。その結果、本発明は、前述の例示的実施形態によって制限されず、添付の請求の範囲によってのみ制限される。

【図面の簡単な説明】

【図１】

従来の太陽電池の断面図である。

【図２】

本発明の実施形態による太陽電池の断面図である。

【図３】

図２の太陽電池についての、本発明の一実施形態による様々な製造段階を示す図である。

【図４】

アルミニウム合金背面接合デンドライト・ウェブ太陽電池の測定Ｉ－Ｖ曲線のグラフを示す図である。

【図５】

アルミニウム合金背面接合デンドライト・ウェブ太陽電池の内部量子効率のグラフを示す図である。

【図６】

太陽電池の裏側に部分的金属カバレッジを備える、本発明の別の実施形態による太陽電池の断面図である。

【図７】

ベース層へのコンタクトが、セルの背面での相互嵌合式のコンタクトである、

本発明の別の実施形態による太陽電池の断面図である。

【図１】

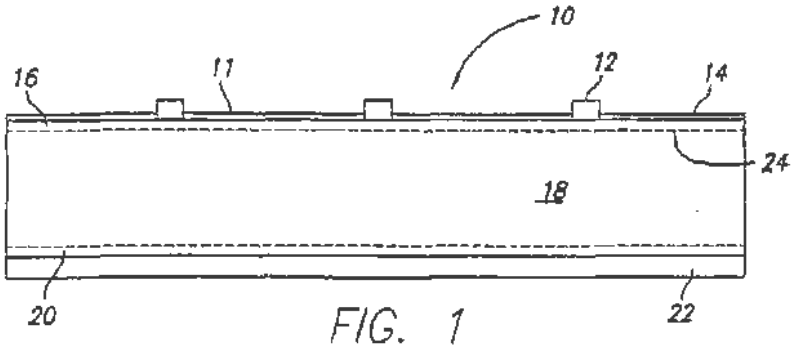


FIG. 1
PRIOR ART

【図２】

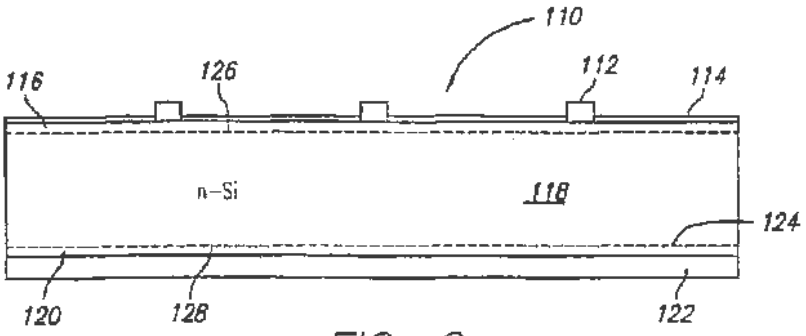


FIG. 2

【図３Ａ】

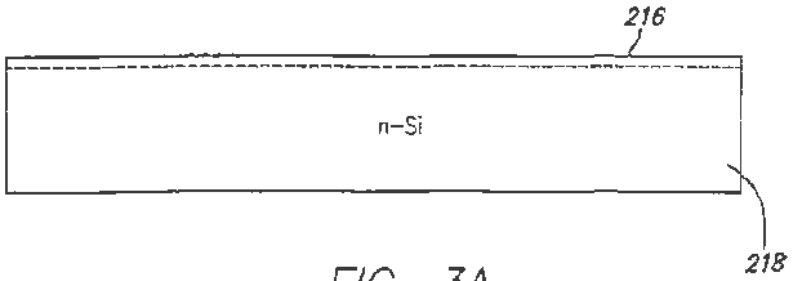


FIG. 3A

【図３Ｂ】

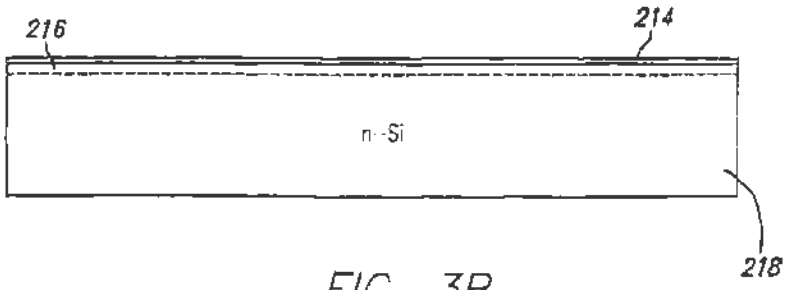


FIG. 3B

【図３Ｃ】

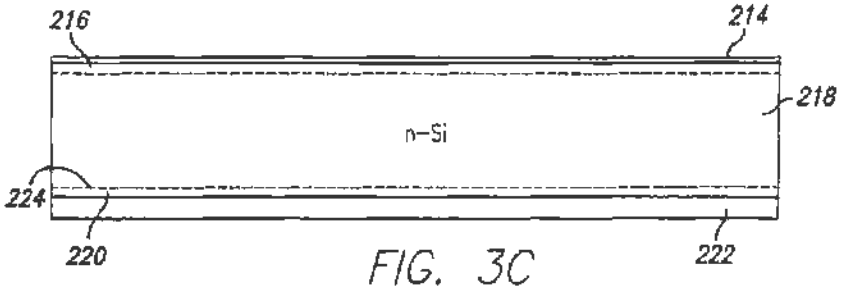


FIG. 3C

【図３Ｄ】

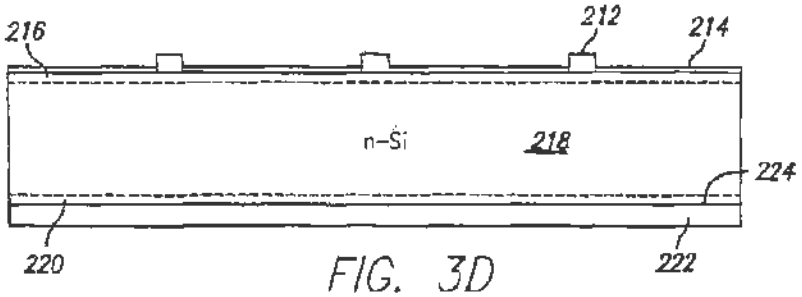
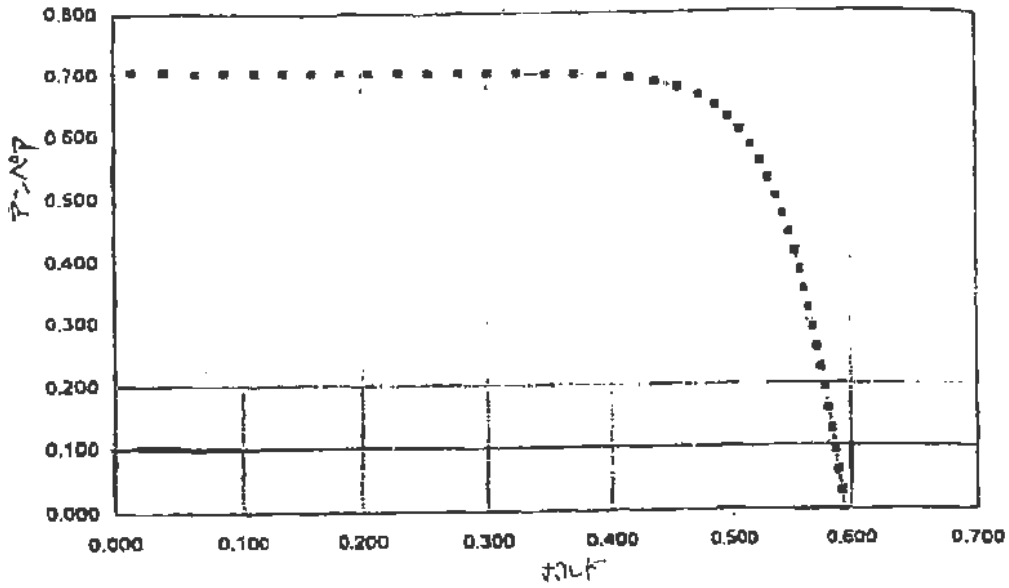
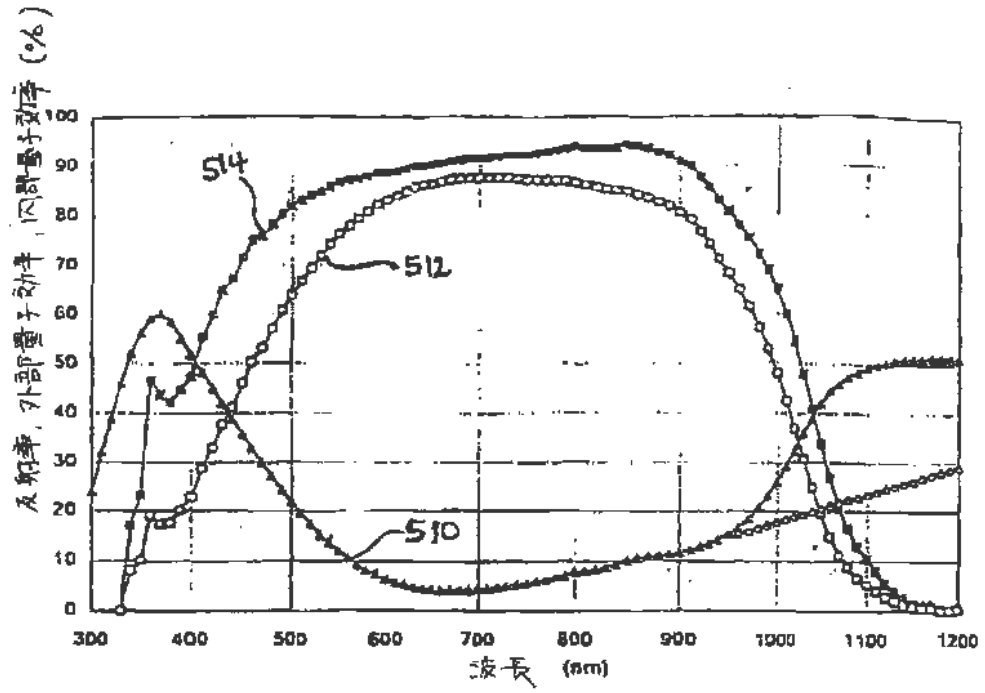


FIG. 3D

【図４】


0.800
0.700
0.600
0.500
0.400
0.300
0.200
0.100
0.000
アノード
0.000
0.100
0.200
0.300
0.400
0.500
0.600
0.700
ボルト

【図５】


反射率，外部量子効率，内部量子効率（%）
100
90
80
70
60
50
40
30
20
10
0
514
512
510
300
400
500
600
700
800
900
1000
1100
1200
波長（nm）

【図６】

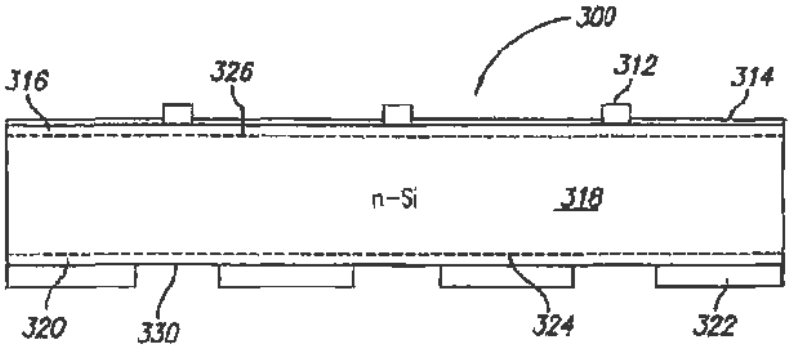


FIG. 6

【図７】

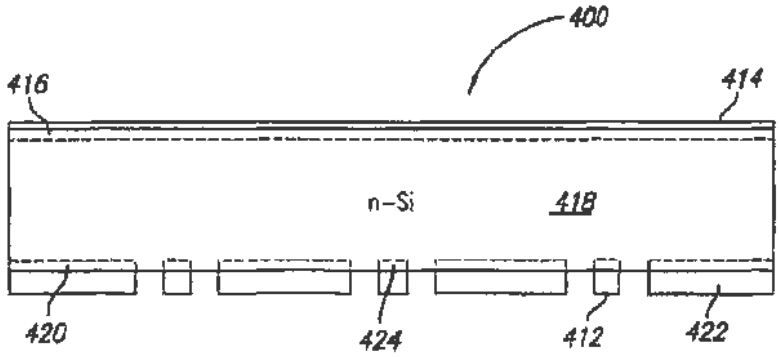


FIG. 7

【国際調査報告】

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 00/02609

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L31/068 H01L31/0352 H01L31/0224

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, COMPENDEK, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category '	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 776 051 A (EBARA SOLAR INC) 28 May 1997 (1997-05-28)	1-4, 8-33,35, 37,38
Y	the whole document	5-7,34, 36,39
Y	WO 97 13280 A (EBARA SOLAR INC ;SALAMI JALAL (US); SHIBATA AKIO (US); MEIER DANIE) 10 April 1997 (1997-04-10) figure 1	5-7,34, 36,39

-/--

[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

' Special categories of cited documents :

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'E' earlier document but published on or after the international filing date
'L' document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
'O' document referring to an oral disclosure, use, exhibition or other means
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'&' document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 July 2000	24/07/2000

Name and mailing address of the ISA
European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer
Werner, A

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INTERNATIONAL SEARCH REPORT

Inter ional Application No
PCT/US 00/02609

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	SALAMI J ET AL: "Self-aligned locally diffused emitter (SALDE) silicon solar cell" SOLAR ENERGY MATERIALS AND SOLAR CELLS,NL,ELSEVIER SCIENCE PUBLISHERS, AMSTERDAM, vol. 48, no. 1-4, 1 November 1997 (1997-11-01), pages 159-165, XP004111846 ISSN: 0927-0248 figure 1	
A	US 4 916 503 A (UEMATSU TSUYOSHI ET AL) 10 April 1990 (1990-04-10) figure 2B	

Form PCT/ISA/210 (continuation of second sheet)(July 1992)

INTERNATIONAL SEARCH REPORT

information on patent family members

Inter　nal Application No
PCT/US 00/02609

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		US 5928438 A	27-07-1999
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		JP 2732524 B	30-03-1998

Form PCT/ISA/210 (patent family annex) (July 1992)

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(81)指定国 EP(AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OA(BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG), AP(GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), EA(AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW

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(P2009-535845A)
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H01L 31/04	*(2006.01)*	H01L 31/04	H	5F051

審査請求　未請求　予備審査請求　未請求　（全10頁）

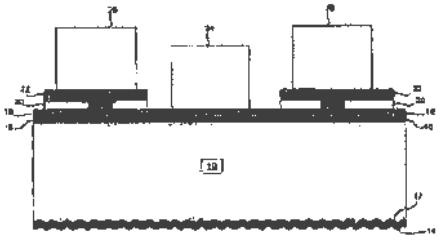
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(86)(22)出願日　平成19年2月9日(2007.2.9)
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(33)優先権主張国　米国(US)

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(74)代理人　100076680
弁理士　溝部　孝彦
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フィリピン国１７８０マンティンルパ・シティ，アラバング，アヤラ・アラバング，アポ・ストリート３０２

最終頁に続く

(54)【発明の名称】トーピングされた半導体ヘテロ接合電極を有する太陽電池

(57)【要約】
シリコン太陽電池は、シリコン基板の表面におけるトンネルシリコン酸化物層上に形成されたドープドアモルファスシリコン電極を有する。太陽電池の製造において、高温処理が不要である。
【選択図】図１



【特許請求の範囲】
【請求項１】
ａ）第１及び第２の対向する主面を有する半導体の本体と、
ｂ）前記第１の表面上の第１の誘電体層、及び前記第２の表面上にあり、トンネル酸化物からなる第２の誘電体層と、
ｃ）前記第２の表面における前記トンネル酸化物上の第１のパターンのアクセプタドープド半導体材料、及び前記第２の表面における前記トンネル酸化物上にあり、前記第１のパターンと交互配置されている第２のパターンのドナードープド半導体材料と、
ｄ）前記アクセプタドープド半導体材料を相互接続する第１の導電性パターン、及び前記ドナードープド半導体材料を相互接続する第２の導電性パターンとを含む、太陽電池。
【請求項２】
前記半導体材料が、アモルファスシリコン、シリコンーゲルマニム、及びIII－Ｖ族化合物半導体からなるグループから選択される、請求項１に記載の太陽電池。
【請求項３】
前記半導体材料が、アモルファスシリコンからなる、請求項２に記載の太陽電池。
【請求項４】
前記アクセプタドープドアモルファスシリコンが、ホウ素をドーピングされている、請求項３に記載の太陽電池。
【請求項５】
前記ドナードープドアモルファスシリコンが、リンをドーピングされている、請求項１に記載の太陽電池。
【請求項６】
前記第１の主面がテクスチャード加工されている、請求項５に記載の太陽電池。
【請求項７】
前記半導体の本体が、シリコンからなり、前記トンネル酸化物が酸化ケイ素からなる、請求項６に記載の太陽電池。
【請求項８】
前記第１及び第２の導電性パターンが、アルミニウム及び銅からなるグループから選択される、請求項７に記載の太陽電池。
【請求項９】
前記半導体の本体がシリコンからなり、前記トンネル酸化物が酸化ケイ素からなる、請求項３に記載の太陽電池。
【請求項１０】
前記第１及び第２の導電性パターンが、アルミニウム及び銅からなるグループから選択される、請求項９に記載の太陽電池。
【請求項１１】
放射線の入射により、可動キャリヤがシリコン基板に生成され得る太陽電池において、可動キャリヤを受け取るための電極が、前記基板の表面上のトンネル酸化物、及び前記トンネル酸化物上のドープド半導体材料層を含む、電極。
【請求項１２】
前記半導体材料が、アモルファスシリコン、シリコンーゲルマニム、及びIII－Ｖ族化合物半導体からなるグループから選択される、請求項１１に記載の電極。
【請求項１３】
前記半導体材料が、アモルファスシリコンからなる、請求項１２に記載の電極。
【請求項１４】
前記トンネル酸化物が酸化ケイ素からなる、請求項１３に記載の電極。
【請求項１５】
前記酸化ケイ素が、１～２ｎｍ（１０～２０オングストローム）の範囲内の厚みを有する、請求項１４に記載の電極。
【請求項１６】

前記アモルファスシリコンが、ドナードーパントでドーピングされている、請求項１４に記載の電極。
【請求項１７】
前記ドナードーパントがリンである、請求項１６に記載の電極。
【請求項１８】
前記アモルファスシリコンが、アクセプタドーパントでドーピングされている、請求項１４に記載の電極。
【請求項１９】
前記アクセプタドーパントがホウ素である、請求項１８に記載の電極。
【請求項２０】
シリコン太陽電池を製造する方法において、キャリヤアクセプタ電極を製造するステップが、
ａ）第１及び第２の対向する主面を有するシリコン基板を準備し、
ｂ）前記第１の主面上にトンネルシリコン酸化物層を形成し、
ｃ）前記トンネルシリコン酸化物上にドープドアモルファスシリコン層を形成することを含む、方法。
【請求項２１】
前記ドープドアモルファスシリコンが、10^{19}原子／cm^3を超えるドーパントを有する、請求項２０に記載の方法。
【請求項２２】
前記ドーパントがドナードーパントである、請求項２１に記載の方法。
【請求項２３】
前記ドーパントがリンからなる、請求項２２に記載の方法。
【請求項２４】
前記ドーパントがアクセプタドーパントである、請求項２１に記載の方法。
【請求項２５】
前記ドーパントがホウ素からなる、請求項２４に記載の方法。
【請求項２６】
前記トンネルシリコン酸化物が、約１～２ｎｍ（１０～２０オングストローム）の厚みを有する、請求項２０に記載の方法。
【発明の詳細な説明】
【技術分野】
【０００１】
発明の背景
本発明は概して、太陽光電池に関し、より具体的には本発明は、動作が効率的で、且つ製造が経済的な太陽電池構造に関する。
【０００２】
太陽放射を電気エネルギーに直接的に変換するための光電池（太陽電池）の使用は、例えば、Swansonによる米国特許第４，２３４，３５２号のように良く知られている。簡単に言うと、光電池は、内部に画定されたｐ－ｎ接合を有する半導体材料の基板からなる。平面シリコンのセル（cell：太陽電池）において、入射する放射線を受け取る基板の表面近くに、ｐ－ｎ接合が形成される。放射された光子が可動キャリヤ（正孔と電子）を生成し、基板がそれらをセルの外側の電気回路に送ることができる。少なくとも最小エネルギーレベル（例えば、シリコンの場合、１．１電子ボルト）有する光子だけが、半導体対において電子正孔対を生成することができる。より少ないエネルギーを有する光子は、吸収されないか、又は熱として吸収され、１．１電子ボルトのエネルギーよりも多い超過エネルギーを有する光子（例えば、１．１μｍ及びそれ未満の波長を有する光子）は、熱を生成する。これら及び他の損失は、太陽エネルギーの電気への直接的な変換において、シリコン光電池の効率を３０％未満に制限する。
【０００３】

セルの背面に反対の極性の互いにかみ合う（相互嵌合）電極を有する太陽電池が、知られており、前側金属グリッド及びブランケット、又はグリッド金属化裏面電極を有する従来の太陽電池に比べて多くの利点を有し、係る利点には、前面グリッドの遮光を取り除いたことによる改善された光生成、より低減されたグリッドの直列抵抗、及び前面電極（コンタクト）が存在しないことから、前面の高濃度ドーピングが前面電極の抵抗を最小限にする必要がないという理由による改善された「青色」の光応答が含まれる。性能の利点に加えて、裏面電極のセル構造により、共平面電極に起因して簡略化されたモジュールアセンブリが可能になる。例えば、Swansonによる米国特許第４，９２７，７７０号を参照されたい。

【０００４】

相互嵌合裏面電極（interdigitated back contact：IBC）の太陽電池が製造されたが、コスト的検討によってＩＢＣ太陽電池の商品化が制限されていた。これまで、裏面拡散、従来のマイクロエレクトロニクスのフォトリソグラフィにより製造された電極および金属線、薄膜メタライゼーション、及びエッチングプロセスの使用を含む、従来のマイクロエレクトロニクス（集積回路）の処理は、ＩＢＣ太陽電池の製造に利用されてきた。この製造プロセスは、高い効率の太陽電池を製造することができるが、そのプロセスは、従来の低コストな平板型太陽電池パネルの応用形態に対して費用効率が悪い。このプロセスによるＩＢＣ太陽電池の実用化に伴う重要課題は、エッチング、ドーピング、及びマスクアライメント、並びに真空蒸着またはスパッタリングによる厚い金属導体の堆積の使用を含む、製造に関する高いコストである。更に、処理は、クリーンルーム環境で実行されなければならない。従って、これらの方法を用いて製造されるＩＢＣ太陽電池は、高集積の太陽電池の用途または非常に高価な１つの太陽の応用形態（one-sun applications）に限定されていた。

【０００５】

米国同時係属出願第１１／３０６，５１０号は、半導体基板をアクセプタ及びドナーのポリマー電極と結合し、経済的に製造される太陽電池を提供する。重要な点は、太陽電池の製造が、コストにおいて改善され、従来技術の太陽電池で必要とされたようなフォトレジストのマスキング、エッチング、及びドーパントの拡散とアニーリングを必要とせずに、ポリマー電極のインクジェットの応用形態を使用することによる低減された温度サイクルにおいて改善される。

【０００６】

本発明は、容易に且つコスト効率良く製造され得るシリコン太陽電池において、ドナー電極およびアクセプタ電極としてアモルファスシリコンのような半導体を利用する。

【０００７】

発明の概要

本発明は、シリコン太陽電池においてドナー電極またはアクセプタ電極として、ドーピングされた（ドープド）アモルファスシリコン、Ｓｉ－Ｇｅ、又はIII－Ｖ族化合物を利用する。電極の材料は、ドナー又はアクセプタの応用形態の必要に応じて、ドーパントと共に堆積される蒸気とすることができる。本明細書で使用される場合、「アモルファス」シリコンは、「多結晶」シリコンを含む。

【０００８】

単結晶シリコン基板に堆積される場合、最初にトンネル酸化物が成長されて、堆積されたアモルファスシリコンを基板から分離し、アモルファスシリコンの再結晶化を防止する。

【０００９】

相互嵌合裏面電極（interdigitated back contact：IBC）のセルにおいて、前面は、化学的アブレーションまたは物理的アブレーションによりテクスチャード加工されて、窒化ケイ素、ドーピングされた（ドープド）炭化ケイ素のような反射防止保護膜、又はアモルファスシリコンの薄い膜を有する放射線捕獲表面をテクスチャード加工された表面上に提供することができる。

【００１０】
本発明および本発明の目的と利点は、図面に関連して参酌された場合に、以下の詳細な説明および添付の特許請求の範囲からより容易に明らかになるであろう。
【００１１】
好適な実施形態に関する詳細な説明
本発明の一実施形態に従って、第１と第２の対向する主面を有するシリコン半導体の本体からなる相互嵌合裏面電極（interdigitated back contact：IBC）太陽電池は、第１の表面を通じて放射線を受け取り、放射された光子によりシリコン基板に生成された電子と正孔のキャリヤを受け取るために、第２の表面、即ち裏面に、それぞれドーピングされた（ドープド）アモルファスシリコンのアクセプタとドープドアモルファスシリコンのドナーの第１と第２のパターンを有する。構造体は、放射線により生成された正孔と電子を受け取るために基板に形成されたドープドＰ型およびＮ型導電性電極を利用する従来技術の裏面電極太陽電池に類似する。しかしながら、基板にドープドＰ型およびＮ型電極を使用することは、太陽電池の製造において、フォトレジストマスキング、エッチング、ドーパント拡散、及び高温処理を必要とする。本発明の一実施形態に従って、基板にアクセプタ及びドナーアモルファスシリコン電極を使用することにより、フォトレジストマスキング及びドーパント拡散、並びに拡散されたドーパントをアニーリングする際に必要な高温処理の必要性が無くなる。トンネルシリコン酸化物が、電極と基板との間に配置されて、基板上のアモルファスシリコンのエピタキシャル成長が防止され得る。
【００１２】
ここで、図１を検討すると、図１は、本発明の一実施形態による相互嵌合裏面電極（ＩＢＣ）太陽電池の断面の側面図である。セルは、放射線を受け取る前面、及びテクスチャード加工された表面を有するライトＮ型単結晶または多結晶基板１０を含み、そのテクスチャード加工された表面には、薄い（例えば、１～１５ｎｍ（１０～１５０オングストローム））トンネルシリコン酸化物層１２が形成され、窒化ケイ素、ドープド炭化ケイ素、又はドープドアモルファスシリコン層からなることができるパッシベーション（保護）膜１４が、トンネル酸化物１２上にある。
【００１３】
基板１０の裏面に、第２のトンネル酸化物層１６があり、その上にＰ＋アモルファスシリコン電極１８が形成されている。酸化ケイ素２０のような誘電体が、Ｎ＋アモルファスシリコン２２からＰ＋アモルファスシリコン１８を分離し、Ｎ＋アモルファスシリコン２２は、Ｐ＋アモルファスシリコン層１８を貫通する開口内に形成され、トンネル酸化物１６と接触する。アモルファスシリコン層１８、２２は低温蒸着により形成されるが、トンネル酸化物１６がシリコン基板１０からのエピタキシャル成長によるアモルファスシリコンの任意の再結晶化を防止する。金属電極２４がＰ＋アモルファスシリコン層１８に係合し、金属電極２６がＮ＋アモルファスシリコン層２２に係合する。
【００１４】
裏面電極ヘテロ接合は、トンネル酸化物１６を包含させることによる太陽電池の背面パッシベーション、アモルファスシリコン電極により提供されるヘテロ接合領域、及び電極のパッシベーションを強化する。以下で更に説明されるように、デバイスを製作する際のプロセスの利点は、高温でドーパントを打ち込む必要が無い点である。
【００１５】
図２Ａ～図２Ｄは、製造中の図１の太陽電池を示す断面図である。最初に、図２Ａに示されるように、真性またはライトドープされたものとすることができるシリコン基板１０は、その上に成長された薄いトンネル酸化物１６を有し、そのトンネル酸化物１６は例えば、１～２ｎｍ（１０～２０オングストローム）の厚みを有することができる。次いで、アモルファスシリコン層１８が、ホウ素のドーパントと共に、10^{19}～10^{21}又は１０Ｅ２０～１０Ｅ２１原子／ｃｍ^{3}のドーパント濃度で５０ｎｍから２００ｎｍ（５００～２０００オングストローム）の厚みまで堆積される。蒸着によるドープドシリコン層の成長は、既知のシリコンプロセスである。ＰＩＮ構造が望ましい場合には、Ｐ型ドープド

シリコン層の下に真性層を含めるように形成され得る。

【００１６】

その後、酸化ケイ素の絶縁層２０が、低圧化学蒸着（ＬＰＣＶＤ、ＰＥＣＶＤ、ＡＰＣＶＤ）により、又はスピンオンガラスのプロセスにより堆積される。酸化ケイ素層１６は、この例示的な実施形態において、５０～１００ｎｍ（５００～１０００オングストローム）である。

【００１７】

その後、図２Ｂに示されるように、基板１０の前面は、化学的アブレーションまたは機械的アブレーションによりテクスチャード加工される。このプロセス工程は、必要に応じて、図２Ａのプロセス工程に先行することができる。次いで、フォトレジストマスクが基板１０の裏面に形成され、基板１０まで酸化ケイ素層２０とアモルファスシリコン１８を貫通する開口を形成するためにエッチングされる。また、薄いトンネル酸化物も、エッチングプロセスで除去され、次いでトンネルシリコン酸化物の新たな層が、エッチングされた開口を介して、化学成長により基板１０の露出した表面に付着される。図２Ｂのトンネル酸化物１６の形成において、トンネル酸化物層１２は、前面に同時に形成され得る。エッチングされた開口において、再び１～２ｎｍ（１０～２０オングストローム）の厚みまで薄いトンネル酸化物を成長させた後、図２Ｃに示されるように、Ｎ＋ドープドアモルファスシリコン層２２が裏面の上に堆積される。

【００１８】

層２２は、10^{19}～10^{21}又は１０Ｅ２０～１０Ｅ２１原子／ｃｍ^{3}の濃度でリンのようなＮ型ドーパントでドーピングされる。これは、プラズマ化学気相成長法（ＰＥＣＶＤ、ＬＰＣＶＤ、ＡＰＣＶＤ）を用いて堆積され得る。次いで、Ｎ＋アモルファスシリコン２２がマスキングされて選択的にエッチングされ、金属電極を受容するために、下にあるＰ＋アモルファスシリコン１８を露出する。図２Ｄにおいて、金属電極２４と２６は、金属堆積ならびにフォトレジストマスキング及びエッチングにより、Ｐ＋アモルファスシリコン１８及びＮ＋アモルファスシリコン２２に形成される。電極は、アルミニウム又は銅のような導電性金属のシード（seed：種）層を最初にまき散らし（scattering）、厚みを増すようにシード金属をパターンめっきすることにより形成され得る。次いで、セルは、窒化ケイ素、ドープド炭化ケイ素、又はＮ＋ドープドアモルファスシリコンを用いて、基板１０の前面におけるトンネル酸化物１２上に保護（パッシベーション）層１４を堆積することにより完成する。

【００１９】

本発明による、ドープドアモルファスシリコン電極を用いるヘテロ接合太陽電池は、高温処理を必要とせずに、従来の半導体処理技術を用いて容易に製造される。本発明は、Ｐ＋電極およびＮ＋電極の双方を利用する相互嵌合裏面電極太陽電池に関連して説明されてきたが、本発明は、裏面に単一のドープドアモルファスシリコンを有する太陽電池に適用され得る。更に、ヘテロ接合がアモルファスシリコンにより提供されるが、ゲルマニウムーシリコン合金、ドープド炭化ケイ素、又はIII－Ｖ族化合物材料のような他の高いバンドギャップの材料が、電極構造に利用されてもよい。従って、本発明は特定の実施形態に関連して説明されてきたが、その説明は本発明の例示であり、本発明を制限するものとして解釈されるべきではない。様々な修正形態および応用形態が、添付の特許請求の範囲により定義されるような本発明の思想および範囲から逸脱せずに、当業者に想起され得る。

【図面の簡単な説明】

【００２０】

【図１】本発明の一実施形態による、ドーピングされたアモルファス電極を含む相互嵌合裏面電極太陽電池の断面の側面図である。

【図２Ａ】製造中の図１の太陽電池を示す断面の側面図である。

【図２Ｂ】製造中の図１の太陽電池を示す断面の側面図である。

【図２Ｃ】製造中の図１の太陽電池を示す断面の側面図である。

【図２Ｄ】製造中の図１の太陽電池を示す断面の側面図である。

【図１】

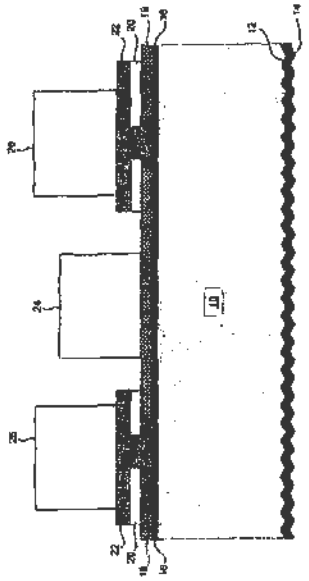


FIG. 1

【図２Ａ】

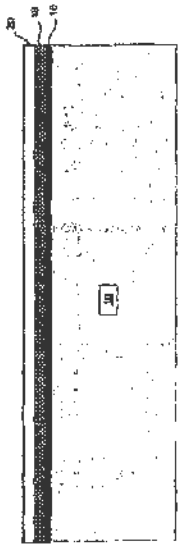


FIG. 2A

【図２Ｂ】

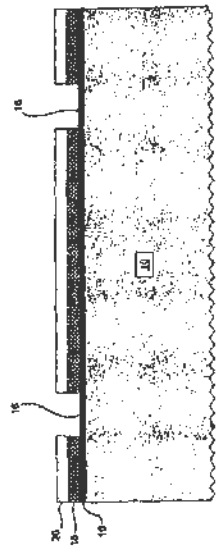


FIG. 2B

【図２Ｃ】

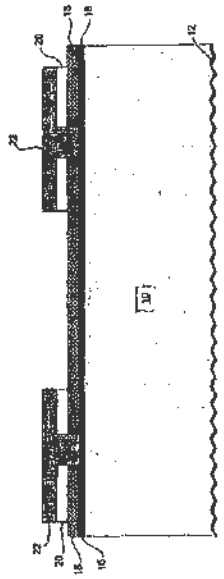


FIG. 2C

【図２Ｄ】

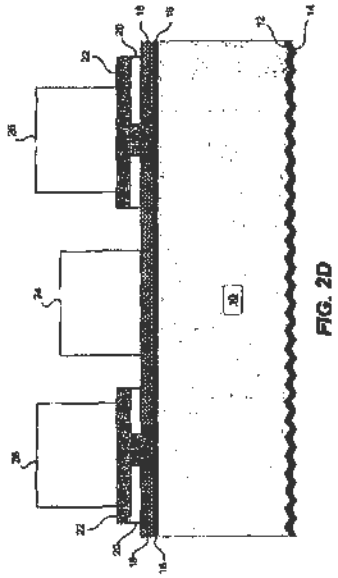


FIG. 2D

【国際調査報告】

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US07/00449

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 31/20 (2007.01)
USPC - 136/256
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 31/04,042,20 (2007.01)
USPC - 136/258; 257/431-466; 438/67,96,97

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO EAST System (US, USPG-PUB, EPO, JPO, FPRS, DERWENT), GoogleScholar, DialogPro, IEEExplore

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X — Y	US 4,272,641 A (HANAK) 09 June 1981 (09.06.1981) entire document	11-20,26 — 21-25
Y	US 4,200,473 A (CARLSON) 29 April 1980 (29.04.1980) column 3, lines 31-36	21-25
Y	US 2004/0043528 A1 (KRUHLER) 04 March 2004 (04.03.2004) entire document	1-10
Y	US 4,000,505 A (EPSTEIN et al) 28 December 1976 (28.12.1976) column 2, lines 20-23	1-10
Y	US 4,315,097 A (SOLOMON) 09 February 1982 (09.02.1982) column 3, lines 10-13, column 3, lines 25-28	8-8,10

☐ Further documents are listed in the continuation of Box C. ☐

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Date of the actual completion of the international search	Date of mailing of the international search report
10 July 2007	08 APR 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

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Fターム(参考) 5F051 AA02 AA03 DA07 FA08 FA15 GA04 GA14

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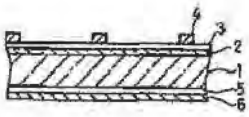
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(22)Date of filing	29.09.1993
(71)Applicant	TONEN CORP
(72)Inventor	SAGAWA YASUNORI OKAYASU YOSHINORI



(54)FABRICATION OF BSF SOLAR CELL

(57)Abstract

PURPOSE: To realize a a BSF type solar cell having high photoelectric conversion efficiency by forming an n+ poly-Si layer by thermal CVD using B2H6/SiH4/SiF4 as a material gas thereby improving the quality of n+ poly-Si layer.

CONSTITUTION: A material gas of B2H6/SiH4/SiF4=0.1/10/500 is introduced into a filming chamber evacuated to 1x10-5 Torr by a thermal CVD system thus depositing a p type polysilicon layer 2 on one side of an n single crystal silicon substrate at 700°C and an n+ polysilicon layer 5 of PH3/SiH4/ SiF4=0.1/10/330 on the opposite side thereof. An ITO is further deposited on the p type polysilicon layer 2 to form an antireflection layer 3 and an interdigital electrode 4 is formed of a silver paste on the surface thereof whereas a rear electrode 6 is formed on the rear side of the n+ polysilicon layer 5. Since a high quality n+or p+ silicon layer can be formed on an n-type or a p type silicon substrate under low film deposition temperature, a BSF solar cell having high photoelectric conversion efficiency can be realized.

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		7376-4M	H01L 31/04	A

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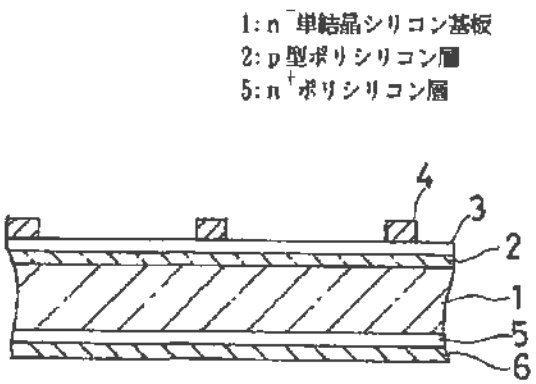
(74)代理人　弁理士　久保田　耕平　（外１名）

(54)【発明の名称】ＢＳＦ型太陽電池の製造方法

(57)【要約】

【目的】　光電変換効率の高いＢＳＦ型太陽電池を安定して製造できる方法を提供すること。

【構成】　n⁻単結晶シリコン（以下、Si）基板１と、この光入射側面に設けられたｐ型のポリSi層２と、反対側面に設けられSi基板との間でＨＬ接合を形成するn⁺ポリSi層５を備えるＢＳＦ型太陽電池の製造方法であり、上記ｎ⁺ポリSi層をB_2H_6／SiH_4／SiF_4を原料ガスとする熱ＣＶＤ法により形成することを特徴とする。この方法によれば、ハロゲン原子を放出するSiF_4を適用しているにも拘らず製膜室内における浮遊異物の発生を防止でき、かつ、熱ＣＶＤ法を適用しているにも拘らず基板加熱温度の低減を図ることが可能となるため、n⁺ポリSi層の膜質が改善されて光電変換効率の高いＢＳＦ型太陽電池を安定して製造できる効果を有している。



1

【特許請求の範囲】

【請求項１】ｎ型又はｐ型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でｐｎ接合を形成するｐ型又はｎ型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でＨＬ接合を形成するｎ⁺又はｐ⁺シリコン層とを備えるＢＳＦ型太陽電池の製造方法において、

ｎ型又はｐ型シリコン基板を配置した製膜室内にシリコン原子が含まれる製膜ガスとＳｉＦ₄ガス及びｎ型又はｐ型のドーパントガスを供給し、かつ、上記供給ガスを加熱されたシリコン基板近傍で熱分解させると共に、熱分解された製膜ガスのラジカル成分と上記ＳｉＦ₄ガスとの反応により生じたフッ素系ラジカルをエッチング成分として作用させながらｎ型又はｐ型シリコン基板面に上記ｎ⁺又はｐ⁺シリコン層を形成することを特徴とするＢＳＦ型太陽電池の製造方法。

【請求項２】ｎ型又はｐ型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でｐｎ接合を形成するｐ型又はｎ型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でＨＬ接合を形成するｎ　又はｐ　シリコン層とを備えるＢＳＦ型太陽電池の製造方法において、

ｎ型又はｐ型シリコン基板を配置した製膜室内に水素化珪素を主成分とする製膜ガスとSiH_mF_{4-m}（但しｍは１～３）で示されるフッ素化シランガス及びｎ型又はｐ型のドーパントガスを供給し、かつ、上記供給ガスを加熱されたシリコン基板近傍で熱分解させると共に、フッ素化シランガスの熱分解により生じたフッ素系ラジカル、及び、熱分解された製膜ガスのラジカル成分が上記フッ素化シランガスと反応して生じたフッ素系ラジカルをエッチング成分として作用させながらｎ型又はｐ型シリコン基板面に上記ｎ　又はｐ　シリコン層を形成することを特徴とするＢＳＦ型太陽電池の製造方法。

【請求項３】製膜室内に配置されたｎ型又はｐ型シリコン基板近傍の空間部位に上記基板が覆われるように網状の発熱部材を配置したことを特徴とする請求項１又は２記載のＢＳＦ型太陽電池の製造方法。

【請求項４】ｎ型又はｐ型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でｐｎ接合を形成するｐ型又はｎ型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でＨＬ接合を形成するｎ　又はｐ　シリコン層とを備えるＢＳＦ型太陽電池の製造方法において、

加熱されたシリコン基板面に上記ｎ⁺又はｐ⁺シリコン層を光ＣＶＤ法により形成することを特徴とするＢＳＦ型太陽電池の製造方法。

【請求項５】ｎ型又はｐ型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でｐｎ接合を形成するｐ型又はｎ型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でＨＬ接合を形成するｎ⁺又はｐ⁺シリコン層とを備えるＢＳＦ型太陽電池の製造方法において、

ｎ型又はｐ型シリコン基板を配置した製膜室内にSiH_mF_{4-m}（但しｍは１～３）で示されるフッ素化シランガス又はＳｉＦ₄ガスを供給し、かつ、このフッ素化シランガス又はＳｉＦ₄ガスが存在する条件下においてイオンプレーティング法により加熱されたシリコン基板面に上記ｎ⁺又はｐ⁺シリコン層を形成することを特徴とするＢＳＦ型太陽電池の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明はＢＳＦ（Back Surface Field）型太陽電池の製造方法に係り、特に、光電変換効率の高いＢＳＦ型太陽電池を安定して製造できるＢＳＦ型太陽電池の製造方法に関するものである。

【０００２】

【従来の技術】この種のＢＳＦ型太陽電池としては、例えば、図７～８に示すようにｐ型単結晶シリコン基板ａと、このシリコン基板ａの光入射側面に設けられシリコン基板ａとの間でｐｎ接合を形成するｎ⁺シリコン層ｂと、このｎ⁺シリコン層ｂ上に一様に成膜されたＩＴＯ（酸化インジウム錫）の反射防止層ｃと、この反射防止層ｃ上に設けられた櫛歯状電極ｄと、上記シリコン基板ａの反対側面に設けられシリコン基板ａとの間でＨＬ（High-Low）接合を形成するｐ⁺シリコン層ｅと、このｐ　シリコン層ｅの背面側に一様に設けられた裏面電極ｆとでその主要部が構成され、光入射に伴って発生したエレクトロンとホールが上記電極ｄ、ｆから電流として取出される構造のものが知られている。

【０００３】尚、図９はこのＢＳＦ型太陽電池の構造をモデル的に記載した構造概念図であり、また、図１０はこの構造を有するＢＳＦ型太陽電池のエネルギーバンド図を示している。

【０００４】そして、ｐ⁺シリコン層ｅを具備しない構造の太陽電池と較べてこのＢＳＦ型太陽電池においては、ＨＬ接合ｇを形成するシリコン基板ａとｐ⁺シリコン層ｅ間に存在する内蔵電界が少数キャリア（この場合、エレクトロン）の裏面電極ｆへの拡散の障壁となり見掛け上エレクトロンの拡散長が増加し、かつ上記ｐ⁺シリコン層ｅがホールに対して低抵抗のオーム性電極になるためシリーズ抵抗が低下し、従って、その光電変換効率を向上できる利点を有するものであるとされていた。

【０００５】ところで、開放電圧を上昇させる上記ｐ⁺シリコン層ｅについては、従来『熱拡散法』により形成されていた。すなわち、Ｂ（ボロン）等を含むｐ型ドーパントガスで満たされた反応室内に上記単結晶シリコン基板ａを導入し、このドーパントガスをシリコン基板ａ内に１０００℃前後の高温条件下で熱拡散させて形成したり、単結晶シリコン基板ａ面にＡｌ（アルミニウム）

等のｐ型ドーパント層を積層しこれを１０００℃前後の高温条件下で焼成してｐ⁺シリコン層ｅを形成していた。

【０００６】しかし、この『熱拡散法』によりｐ　シリコン層ｅを形成した場合、ｐ⁺シリコン層ｅの厚み制御が難しくその層厚が数百オングストローム～数μｍと大きくなり易く、かつ、熱的条件の僅かなばらつきでＢ、Ａｌ等ドーパントガスの拡散距離が変動し易いためシリコン基板ａの特性がばらつき易い欠点があった。

【０００７】更に、上記『熱拡散法』ではドーパントガスの回り込みも起こり易く、シリコン基板との間でｐｎ接合を形成するｎ　シリコン層ｂ内へも上記ドーパントガスが熱拡散してしまうことがあり、また、シリコン基板が１０００℃前後の高温に晒されることから基板の熱劣化を引起こす等の欠点もあった。

【０００８】このような技術的背景の下、本出願人は上記ｎ型又はｐ型シリコン基板との間でＨＬ接合を形成するｎ⁺シリコン層又はｐ⁺シリコン層をプラズマＣＶＤ法により形成するＢＳＦ型太陽電池の製造方法を既に提案している。すなわち、この製造方法によれば、従来の熱拡散法による場合に較べてｎ⁺シリコン層又はｐ⁺シリコン層形成時における熱的条件が緩和されるためシリコン基板の特性劣化が起こり難くなると共に、上記ｎ⁺シリコン層又はｐ⁺シリコン層の厚さを従来より薄い数十オングストローム～数百オングストローム程度に形成することが可能になるためその光電変換効率の向上が図れる利点を有する方法であった。

【０００９】

【発明が解決しようとする課題】ところで、プラズマＣＶＤ法を適用した上記製造方法においてはｎ⁺シリコン層又はｐ⁺シリコン層の低温製膜とその薄膜化が図れることから上述した利点を有していたが、その反面、上記ｎ　シリコン層又はｐ　シリコン層の製膜工程中において粉状の浮遊異物が製膜室内に多量に発生し易く、この浮遊異物が製膜途上のｎ⁺シリコン層又はｐ　シリコン層内に混入されてその膜特性を劣化させてしまう欠点があった。

【００１０】すなわち、プラズマＣＶＤ法を適用したこの製造方法においては製膜室内のプラズマ形成領域にプラズマ化された原料ガスが一様に分布しかつこのプラズマ化された原料ガスは励起状態にあるため、製膜室内の任意の空間において原料ガスが互いに反応してシリコンの粉状体を生成したり、基板以外の部位すなわち製膜室の内壁面においてプラズマ化された原料ガスが反応してシリコンが析出しこれが粉状体となって剥離する等粉状の浮遊異物が多量に発生し易い状態にある。

【００１１】また、プラズマＣＶＤ法においては製膜ガスであるＳｉＨ₄ガス等に加えてハロゲンガスを配合する場合があり、このハロゲン原子のエッチング作用により製膜室の内壁面や内部治具表面が腐食され易いためこの腐食面が剥離して上記浮遊異物に加わることになる。

【００１２】このため、プラズマＣＶＤ法を適用した上記製造方法においては上述した利点を有している反面、良質なｎ⁺シリコン層又はｐ　シリコン層を形成することが困難なためこれに起因して得られたＢＳＦ型太陽電池の光電変換効率も一定の限界を有する問題点があった。

【００１３】本発明はこのような問題点に着目してなされたもので、その課題とするところは、低温製膜条件で良質なｎ⁺シリコン層又はｐ⁺シリコン層が形成できる熱ＣＶＤ法、光ＣＶＤ法、及び、イオンプレーティング法を選択することにより光電変換効率が更に向上したＢＳＦ型太陽電池を安定して製造できる方法を提供することにある。

【００１４】

【課題を解決するための手段】すなわち、請求項１に係る発明は、ｎ型又はｐ型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でｐｎ接合を形成するｐ型又はｎ型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でＨＬ接合を形成するｎ　又はｐ　シリコン層とを備えるＢＳＦ型太陽電池の製造方法を前提とし、ｎ型又はｐ型シリコン基板を配置した製膜室内にシリコン原子が含まれる製膜ガスとＳｉＦ₄ガス及びｎ型又はｐ型のドーパントガスを供給し、かつ、上記供給ガスを加熱されたシリコン基板近傍で熱分解させると共に、熱分解された製膜ガスのラジカル成分と上記ＳｉＦ₄ガスとの反応により生じたフッ素系ラジカルをエッチング成分として作用させながらｎ型又はｐ型シリコン基板に上記ｎ⁺又はｐ⁺シリコン層を形成することを特徴とするものであり、また、請求項２に係る発明は、ｎ型又はｐ型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でｐｎ接合を形成するｐ型又はｎ型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でＨＬ接合を形成するｎ⁺又はｐ　シリコン層とを備えるＢＳＦ型太陽電池の製造方法を前提とし、ｎ型又はｐ型シリコン基板を配置した製膜室内に水素化珪素を主成分とする製膜ガスとSiH_mF_{4-m}（但しｍは１～３）で示されるフッ素化シランガス及びｎ型又はｐ型のドーパントガスを供給し、かつ、上記供給ガスを加熱されたシリコン基板近傍で熱分解させると共に、フッ素化シランガスの熱分解により生じたフッ素系ラジカル、及び、熱分解された製膜ガスのラジカル成分が上記フッ素化シランガスと反応して生じたフッ素系ラジカルをエッチング成分として作用させながらｎ型又はｐ型シリコン基板に上記ｎ⁺又はｐ⁺シリコン層を形成することを特徴とするものである。

【００１５】そして、請求項１に係る発明においてはハロゲン原子を放出するガスとして熱分解を受け難いＳｉＦ₄ガスが適用されており、また、請求項２に係る発明においてはハロゲン原子を放出するガスとして上記製膜

ガスよりその熱分解温度が高いフッ素化シランガスを適用しているため、製膜室内の基板から離れた温度分布の低い領域においてはSiF₄及びフッ素化シランガスの熱分解が起り難く、その分、この領域のフッ素系ラジカル濃度は低い状態になっている。

【0016】従って、プラズマCVD法を適用した従来の製造方法に較べて、製膜室内の任意の空間において上記製膜ガスがフッ素系ラジカルと反応してシリコン粉状体を生成したり、あるいは、製膜室の内壁面や内部治具表面が上記フッ素系ラジカルの作用を受けて腐食される可能性が低いため、ハロゲン原子を放出するSiF₄又はフッ素化シランガスを適用しているにも拘らず製膜室内における浮遊異物の発生を防止することが可能となる。

【0017】一方、請求項1に係る発明において上記SiF₄ガスは熱分解を受けにくい反面、熱分解されたシラン化合物等製膜ガスのラジカル成分との反応によりその熱分解が促進されるため、上記ラジカル成分の多い領域、すなわちn型又はp型シリコン基板近傍領域において分解を受け易くこの領域に高濃度のフッ素系ラジカルが偏在することになる。また、請求項2に係る発明においも上記SiH₂F₂等フッ素化シランガスはn型又はp型シリコン基板近傍の高温領域において熱分解を受け易いと共に、熱分解された製膜ガスのラジカル成分（SiH₂ラジカル、H系ラジカル等）との反応によりその分解が促進されるため、基板近傍領域に高濃度のフッ素系ラジカルが偏在することになる。

【0018】従って、このフッ素系ラジカルの作用によりn型又はp型シリコン基板上若しくは成長中のn⁺又はp⁺シリコン層に混入された不純物のみが選択的にエッチングを受けて取除かれることになるため、本来、この不純物を取除くための高温加熱処理が必要となる熱CVD法を適用しているにも拘らず請求項1又は2に係る発明においては基板加熱温度の低減が図れる。

【0019】尚、請求項1又は2に係る発明において製膜室内の基板近傍の空間部位に上記基板を加熱する発熱手段を設けると、製膜ガスの熱分解が促進されるため基板加熱温度を更に低減することが可能となる。請求項3に係る発明はこのような技術的理由に基づきなされている。

【0020】すなわち、請求項3に係る発明は、請求項1又は2記載の発明に係るBSF型太陽電池の製造方法を前提とし、製膜室内に配置されたn型又はp型シリコン基板近傍の空間部位に上記基板が覆われるように網状の発熱部材を配置したことを特徴とするものである。

【0021】そして、n型又はp型シリコン基板近傍の空間部位に配置される上記発熱部材とは、基板全面を覆うように配置されてもn⁺又はp⁺シリコン層の製膜に支障を来さないような形状を備え、かつ水素化珪素等の製膜ガスを基板近傍領域で熱分解させる程度に発熱する材料で構成されているもので、具体例としてタングステン、トリウムタングステン等から成る網状の熱フィラメントが挙げられる。

【0022】また、請求項1～3に係る発明の熱CVD法においては、製膜処理中にこの製膜室内の真空度を略一定に維持するためその下流側において継続して排気処理を行っており、エッチング作用に供されたフッ素系ラジカルあるいは余剰のフッ素系ラジカルは上記排気処理により製膜室から外部へ排除されている。

【0023】ここで、請求項1～3に係る発明においてn型又はp型シリコン基板との間でHL接合を形成するn⁺シリコン層又はp⁺シリコン層としては、n型又はp型ドーパントガスが導入されたアモルファスシリコン層、ポリシリコン層、あるいは、単結晶シリコン層が適用できる。この場合、内部低抗を下げる観点からポリシリコン層よりはその抵抗値の低い単結晶シリコン層が望ましく、また、アモルファスシリコン層よりはその抵抗値の低いポリシリコン層が望ましい。

【0024】尚、n型のドーパントガスとしては元素周期率表第III族のSb（アンチモン）、As（ひ素）、及び、P（リン）等を含む化合物が適用でき、具体例としては、SbH_3、$SbCl_3$、AsH_3、As_4H_4、及び、PH_3等が挙げられる。また、p型のドーパントガスとしては元素周期率表第V族のGa（ガリウム）、B（ボロン）In（インジウム）、及び、Al（アルミニウム）等を含む化合物が適用でき、具体例としては、B_2H_6、$Ga(CH_3)_3$、$In(CH_3)$、及び、$Al(CH_3)_3$等が挙げられる。

【0025】また、請求項1又は3に係る発明においてシリコン原子が含まれる上記製膜ガスとしては、熱分解され易いSiH_4、Si_2H_6、及び、Si_3H_8等の水素化珪素やSiH_mX_{4-m}（但し、mは1～3、好ましくは2～3、XはCl又はF原子、好ましくはF原子である）で示されるハロゲン化シラン等が適用できる。尚、この製膜ガス内に水素ガスを添加してもよい。この水素系ラジカルもSiF_4ガスに作用してその分解を促進させるからである。ここで、製膜ガスとして後者のハロゲン化シランガスを適用した場合、このハロゲン化シランガスの配合割合が高過ぎると製膜室内に上述した浮遊異物が生ずることがある。従って、SiH_2X_2で示されるハロゲン化シランガスを適用する場合にはその配合割合を上記SiF_4より少なく設定することが望ましい。

【0026】また、請求項2又は3に係る発明において上記製膜ガスの主要部を構成する水素化珪素としては、SiH_4、Si_2H_6、及び、Si_3H_8等が適用できる。また、請求項1又は3に係る発明と同様、上記製膜ガス内に水素ガスを添加してもよい。この水素系ラジカルも上記SiH_2F_2等のフッ素化シランガスと反応しその熱分解を促進させるからである。

【0027】尚、請求項1～3に係る発明において上記

製膜ガス中に希釈ガスとして、ヘリウム、ネオン、アルゴン等の不活性ガスを加えてもよい。

【００２８】そして、請求項１～３記載の発明に係るＢＳＦ型太陽電池の製造方法においては、製膜開始前における製膜室の真空度をこの製膜室内に不純物が若干残留する程度（10^{-5}Ｔｏｒｒ程度）に設定し、かつ、配置されたｎ型又はｐ型シリコン基板の温度を５００℃～７００℃程度に設定した後、少なくとも上記製膜ガスとＳｉＦ$_4$ガス及びｎ型又はｐ型のドーパントガスを供給するか、あるいは、少なくとも上記製膜ガスとＳｉＨ$_m$Ｆ$_{4-m}$（但しｍは１～３）で示されるフッ素化シランガス及びｎ型又はｐ型のドーパントガスを供給して上記ｎ型又はｐ型シリコン基板上にｎ$^+$又はｐ$^+$シリコン層を形成する。このとき、基板加熱温度を５００℃～７００℃程度の低温条件に設定しても上記フッ素系ラジカルのエッチング作用により不純物は選択的に除去され、また、浮遊異物の発生も殆ど起らずｎ$^+$又はｐ$^+$シリコン層内への混入が起こり難いため上記ｎ$^+$又はｐ$^+$シリコン層の膜特性に悪影響を及ぼす可能性がほとんどない。

【００２９】従って、光電変換効率が更に向上したＢＳＦ型太陽電池を安定して製造できる利点を有している。

【００３０】次に、請求項４～５に係る発明は、請求項１～３に係る発明において　ｎ$^+$又はｐ$^+$シリコン層の製膜に適用された熱ＣＶＤ法に代えて光ＣＶＤ法及びイオンプレーティング法を適用したＢＳＦ型太陽電池の製造方法に関する。

【００３１】まず、請求項４に係る発明は、ｎ型又はｐ型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でｐｎ接合を形成するｐ型又はｎ型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でＨＬ接合を形成するｎ　又はｐ　シリコン層とを備えるＢＳＦ型太陽電池の製造方法を前提とし、加熱されたシリコン基板面に上記ｎ　又はｐ$^+$シリコン層を光ＣＶＤ法により形成することを特徴とするものである。

【００３２】すなわち、この光ＣＶＤ装置は、図５に示すように製膜室１１と、この製膜室１１内に石英窓３０を介し配設された紫外線照射ランプ３１と、この紫外線照射ランプ３１の対向側に設けられヒータ１５が組込まれた基板ホルダー１３と、製膜室１１内へＳｉＨ$_4$等の製膜ガスと、適宜ドーパントガスと、水素ガス等を供給するガス供給源１６、１７と、調圧弁１９を介して接続された減圧ポンプ１８とでその主要部が構成されており、上記製膜室１１内にｎ型又はｐ型シリコン基板１４を配置すると共に、このシリコン基板１４を５００～６００℃程度に加熱した後、上記ガス供給源１６、１７から製膜ガス、ドーパントガス等を供給し、かつ、紫外線を照射して上記ｎ型又はｐ型シリコン基板１４上にｎ又はｐ$^+$シリコン層を形成する方法である。

【００３３】そして、この請求項４記載の発明に係る製造方法によれば、低温製膜条件で膜質良好なｎ　又はｐシリコン層をｐ型シリコン基板１４上に形成できるため、請求項１～３に係る発明と同様，光電変換効率が更に向上したＢＳＦ型太陽電池を安定して製造できる利点を有している。

【００３４】次に、請求項５に係る発明は、ｎ型又はｐ型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でｐｎ接合を形成するｐ型又はｎ型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でＨＬ接合を形成するｎ$^+$又はｐ$^+$シリコン層とを備えるＢＳＦ型太陽電池の製造方法を前提とし、ｎ型又はｐ型シリコン基板を配置した製膜室内にＳｉＨ$_m$Ｆ$_{4-m}$（但しｍは１～３）で示されるフッ素化シランガス又はＳｉＦ$_4$ガスを供給し、かつ、このフッ素化シランガス又はＳｉＦ$_4$ガスが存在する条件下においてイオンプレーティング法により加熱されたシリコン基板面に上記ｎ$^+$又はｐ　シリコン層を形成することを特徴とするものである。

【００３５】すなわち、このイオンプレーティング装置は、図６に示すように製膜室１１と、この製膜室１１内の下方側に設けられ製膜材料であるドーパント混入のＳｉターゲットが収容された抵抗加熱蒸発源４０と、この抵抗加熱蒸発源４０の上方側空間部に設けられたＲＦコイル４１と、上記抵抗加熱蒸発源４０からの供給量を調整するシャッター４２と、製膜室１１内の上方側に設けられシリコン基板１４を６００～７００℃程度に加熱する基板ホルダー４３とでその主要部が構成されており、かつ、ＲＦコイル４１には高周波電源４４が、また、基板ホルダー４３には正の高圧電源（図示せず）が接続されている。そして，上記製膜室１１内にｎ型又はｐ型シリコン基板１４を配置し、かつ、この製膜室１１内にフッ素化シランガス又はＳｉＦ$_4$ガスを供給すると共に，上記シリコン基板１４を６００～７００℃程度に加熱した後、抵抗加熱蒸発源４０からドーパントとシリコンを蒸発させてｎ型又はｐ型シリコン基板１４上にｎ$^+$又はｐ$^+$シリコン層を形成する方法である。

【００３６】この請求項５に係る発明においても、請求項１～３に係る発明と同様、ハロゲン原子を放出するガスとして熱分解を受け難いフッ素化シランガス又はＳｉＦ$_4$ガスが適用されているためｎ型又はｐ型シリコン基板近傍領域において高濃度のフッ素系ラジカルが偏在することになる。すなわち、ｎ型又はｐ型シリコン基板の近傍領域においては熱分解されたシリコン分子のラジカル成分が遍在しているため、このラジカル成分と上記フッ素化シランガス又はＳｉＦ$_4$ガスとの反応により高濃度のフッ素系ラジカルが偏在している。そして、このフッ素系ラジカルの作用によりｎ型又はｐ型シリコン基板上若しくは成長中のｎ　又はｐ$^+$シリコン層に混入された不純物のみが選択的にエッチングを受けて取除かれることになるため、低温製膜条件で膜質良好なｎ　又はｐ$^+$シ

リコン層をｎ型又はｐ型シリコン基板上に形成することが可能となり、請求項１～４に係る発明と同様、光電変換効率が更に向上したＢＳＦ型太陽電池を安定して製造できる利点を有している。

【００３７】

【作用】請求項１に係る発明によれば、ハロゲン原子を放出するガスとして熱分解を受け難いＳｉＦ₄ガスが適用されており、このガスが熱分解され難い分、製膜室内におけるフッ素系ラジカル濃度は低い状態になっているため、プラズマＣＶＤ法を適用した従来の製造方法に較べて製膜室内の任意の空間において製膜ガスがフッ素系ラジカルと反応してシリコン粉状体を生成したり、あるいは、製膜室の内壁面や内部治具表面が上記フッ素系ラジカルの作用を受けて腐食される可能性が極端に低くなり、ハロゲン原子を放出するＳｉＦ₄ガスを適用しているにも拘らず製膜室内における浮遊異物の発生を確実に防止することが可能となる。

【００３８】一方、上記ＳｉＦ₄ガスは製膜ガスのラジカル成分（ＳｉＨₓラジカル、Ｈ系ラジカル等）との反応によりその熱分解が促進されることからこのラジカル成分の多いｎ型又はｐ型シリコン基板近傍領域に高濃度のフッ素系ラジカルが偏在し易くなり、このフッ素系ラジカルの作用により上記基板上若しくは成長中のｎ⁺又はｐ⁺シリコン層に混入された不純物のみが選択的にエッチンを受けて取除かれるため、本来、この不純物を取除くための高温加熱処理が必要となる熱ＣＶＤ法を適用しているにも拘らず基板加熱温度の低減を図ることが可能となる。

【００３９】また、請求項２に係る発明によれば、ハロゲン原子を放出するガスとして上記製膜ガスよりその熱分解温度が高いフッ素化シランガスを適用しており、製膜室内の基板から離れた温度分布の低い領域においては上記製膜ガスに較べてこのフッ素化シランガスの熱分解が起り難くフッ素系ラジカル濃度は低い状態になっているため、プラズマＣＶＤ法を適用した従来の製造方法に較べて製膜室内の任意の空間において製膜ガスがフッ素系ラジカルと反応してシリコン粉状体を生成したり、あるいは、製膜室の内壁面や内部治具表面が上記フッ素系ラジカルの作用を受けて腐食される可能性が低くなり、ハロゲン原子を放出するフッ素化シランガスを適用しているにも拘らず製膜室内における浮遊異物の発生を防止することが可能となる。

【００４０】一方、上記フッ素化シランガスはｎ型又はｐ型シリコン基板近傍の高温領域において熱分解を受け易いと共に熱分解された製膜ガスのラジカル成分（ＳｉＨₓラジカル、Ｈ系ラジカル等）との反応によりその分解が促進されることからｎ型又はｐ型シリコン基板近傍領域に高濃度のフッ素系ラジカルが偏在し易くなり、このフッ素系ラジカルの作用により上記基板上若しくは成長中のｎ⁺又はｐ⁺シリコン層に混入された不純物のみが選択的にエッチンを受けて取除かれるため、請求項１に係る発明と同様、熱ＣＶＤ法を適用しているにも拘らず基板加熱温度の低減を図ることが可能となる。

【００４１】更に、請求項３に係る発明によれば、製膜室内に配置されたｎ型又はｐ型シリコン基板近傍の空間部位に上記基板が覆われるように網状の発熱部材を配置していることから、この発熱部材が発する熱エネルギの作用により上記基板近傍領域においては製膜ガスの熱分解が著しく促進されているため、上記フッ素系ラジカルのエッチング作用と相乗して基板加熱温度を更に低減させることが可能となる。

【００４２】次に、請求項４に係る発明によれば、加熱されたシリコン基板面にｎ⁺又はｐ⁺シリコン層を光ＣＶＤ法により製膜しているため、低温製膜条件で膜質良好なｎ⁺又はｐ⁺シリコン層を上記ｎ型又はｐ型シリコン基板上に形成することが可能となる。

【００４３】また、請求項５に係る発明によれば、フッ素化シランガス又はＳｉＦ₄ガスが存在する条件下においてイオンプレーティング法により加熱されたシリコン基板面に上記ｎ⁺又はｐ⁺シリコン層を製膜しているため、低温製膜条件で膜質良好なｎ⁺又はｐ⁺シリコン層を上記ｎ型又はｐ型シリコン基板上に形成することが可能となる。

【００４４】

【実施例】以下、本発明の実施例について詳細に説明するとこの実施例に係るＢＳＦ型太陽電池は、従来同様、図１に示すようにｎ⁺単結晶シリコン基板（１００記向、比抵抗１～１０Ω・ｃｍ）１と、このシリコン基板１の光入射側面に設けられシリコン基板１との間でｐｎ接合を形成するｐ型アモルファスシリコン又はポリシリコン層２と、このｐ型アモルファスシリコン又はポリシリコン層２上に一様に成膜されＩＴＯ（酸化インジウム錫）にて形成された反射防止層３と、この反射防止層３上に設けられ銀ペーストにて形成された櫛歯状電極４と、上記シリコン基板１の反対側面に設けられシリコン基板１との間でＨし接合を形成するｎ⁺アモルファスシリコン又はポリシリコン層５と、このｎ⁺アモルファスシリコン又はポリシリコン層５の背面側に一様に設けられアルミニウムにて形成された裏面電極６とでその主要部が構成されているものである。

【００４５】そしてこのＢＳＦ型太陽電池は以下の工程に従って製造されたものである。

【００４６】［実施例１］図３はこの実施例で適用された熱ＣＶＤ装置の概略構成を示した説明図で、図中１１は製膜室、１３はヒータ１５が組込まれた基板ホルダー、１４はこの基板ホルダー１３に取付けられたｎ⁺単結晶シリコン基板、１６、１７は原料ガスの供給源、及び、１８は調圧弁１９を介し製膜室１１に接続された減圧ポンプをそれぞれ示している。

【００４７】まず、この製膜室１１を排気して１×１０

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$^{-5}$Ｔｏｒｒの真空にし、次いで、この製膜室１１内に下記原料ガスを導入すると共に下記の製膜条件に従ってその一面側にｐ型ポリシリコン層２を、他方の面にｎ$^{+}$ポリシリコン層５をそれぞれ製膜した（図２Ａ参照）。

【００４８】（ｐ型ポリシリコン層２の製膜条件）

原料ガスの種類と組成：B_2H_6／ＳｉＨ$_4$／ＳｉＦ$_4$＝０．１／１０／５００

原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ

原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ

ｎ$^{+}$単結晶シリコン基板の加熱温度：７００℃

（ｎ$^{+}$ポリシリコン層５の製膜条件）

原料ガスの種類と組成：ＰＨ$_3$／ＳｉＨ$_4$／ＳｉＦ$_4$＝０．１／１０／３３０

原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ

原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ

ｎ$^{+}$単結晶シリコン基板の加熱温度：７００℃

次に、図２（Ｂ）に示すようにスパッタリング法にてｐ型ポリシリコン層２上にＩＴＯを着膜させて反射防止層３を形成し、かつ、この面上に銀ペーストにより櫛歯状電極４を形成すると共に、ｎ$^{+}$ポリシリコン層５の背面側にスパッタリング法によりアルミニウムを一様に製膜して裏面電極６を形成し実施例に係るＢＳＦ型太陽電池を求めた（図１参照）。

【００４９】そして、この電池の特性を調べたところ、ｎ$^{+}$ポリシリコン層の製膜手段にプラズマＣＶＤ法を適用した従来のものの特性が０．５７Ｖ～０．５８Ｖ、３５ｍＡ～３７ｍＡであったのに対し、この実施例に係るＢＳＦ型太陽電池の特性は０．５９Ｖ～０．６０Ｖ、３７ｍＡ～３９ｍＡであった。

【００５０】［実施例２］ｐ型ポリシリコン層２とｎ$^{+}$ポリシリコン層５に代えてｐ型アモルファスシリコン層とｎ$^{+}$アモルファスシリコン層を適用し、かつ、その製膜条件が下記である点を除き実施例１と略同一である。

【００５１】そして、この実施例に係るＢＳＦ型太陽電池においてもその特性が０．５９Ｖ～０．６０Ｖ、３７ｍＡ～３９ｍＡであり従来例に較べて良好であった。

【００５２】（ｐ型アモルファスシリコン層２の製膜条件）

原料ガスの種類と組成：B_2H_6／ＳｉＨ$_4$／ＳｉＦ$_4$／Ｈ$_2$＝０．１／１０／１００／４００

原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ

原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ

ｎ$^{+}$単結晶シリコン基板の加熱温度：６００℃

（ｎ$^{+}$アモルファスシリコン層５の製膜条件）

原料ガスの種類と組成：ＰＨ$_3$／ＳｉＨ$_4$／ＳｉＦ$_4$／Ｈ$_2$＝０．１／１０／１００／４００

原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ

原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ

ｎ$^{+}$単結晶シリコン基板の加熱温度：６００℃

［実施例３］ｐ型アモルファスシリコン層２とｎ アモルファスシリコン層５の製膜条件が下記である点を除き実施例２と略同一である。

【００５３】そして、この実施例に係るＢＳＦ型太陽電池においてもその特性が０．５８Ｖ～０．５９Ｖ、３６ｍＡ～３８ｍＡであり従来例に較べて良好であった。

【００５４】（ｐ型アモルファスシリコン層２の製膜条件）

原料ガスの種類と組成：Ｉｎ（ＣＨ$_3$）$_3$／ＳｉＨ$_4$／ＳｉＨ$_2$Ｆ$_2$／アルゴン＝０．１／１０／１００／４００

原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ

原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ

ｎ$^{+}$単結晶シリコン基板の加熱温度：６５０℃

（ｎ$^{+}$アモルファスシリコン層５の製膜条件）

原料ガスの種類と組成：ＳｂＣｌ$_3$／ＳｉＨ$_4$／ＳｉＨ$_2$Ｆ$_2$／アルゴン＝０．１／１０／１００／４００

原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ

原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ

ｎ$^{+}$単結晶シリコン基板の加熱温度：６５０℃

［実施例４］ｐ型アモルファスシリコン層２とｎ アモルファスシリコン層５の製膜条件が下記である点を除き実施例２と略同一である。

【００５５】そして、この実施例に係るＢＳＦ型太陽電池においてもその特性が０．５８Ｖ～０．５９Ｖ、３６ｍＡ～３８ｍＡであり従来例に較べて良好であった。

【００５６】（ｐ型アモルファスシリコン層２の製膜条件）

原料ガスの種類と組成：Ａｌ（ＣＨ$_3$）$_3$／ＳｉＨ$_4$／ＳｉＨ$_2$Ｆ$_2$／Ｈ$_2$／アルゴン＝０．１／１０／１００／３００／１００

原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ

原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ

ｎ 単結晶シリコン基板の加熱温度：７００℃

（ｎ アモルファスシリコン層５の製膜条件）

原料ガスの種類と組成：ＰＨ$_3$／ＳｉＨ$_4$／ＳｉＨ$_2$Ｆ$_2$／Ｈ$_2$／アルゴン＝０．１／１０／１００／３００／１００

原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ

原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ

ｎ$^{+}$単結晶シリコン基板の加熱温度：７００℃

［実施例５］図３に示された装置に代えて図４に示すように基板近傍の空間部位にタングステンの熱フィラメント２０が配置された熱ＣＶＤ装置を適用すると共に、上記ｐ型ポリシリコン層２とｎ ポリシリコン層５の製膜条件が下記である点を除き実施例１と略同一である。

【００５７】そして、この実施例に係るＢＳＦ型太陽電池においてもその特性が０．５９Ｖ～０．６０Ｖ、３７ｍＡ～３９ｍＡであり従来例に較べて良好であった。

【００５８】（ｐ型ポリシリコン層２の製膜条件）

原料ガスの種類と組成：Ｇａ（ＣＨ$_3$）$_3$／ＳｉＨ$_4$／ＳｉＦ$_4$／Ｈ$_2$＝０．１／１０／１００／４００

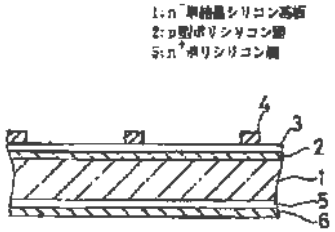
原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ
原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ
ｎ⁻単結晶シリコン基板の加熱温度：６５０℃
（ｎ ポリシリコン層５の製膜条件）
原料ガスの種類と組成：AsH_3／SiH_4／SiF_4／H_2＝０．１／１０／１００／４００
原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ
原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ
ｎ⁻単結晶シリコン基板の加熱温度：６５０℃
［実施例６］図４に示された熱ＣＶＤ装置を適用した点と、ｐ型ポリシリコン層２とｎ⁻ポリシリコン層５の製膜条件が下記である点を除き実施例１と略同一である。
【００５９】そして、この実施例に係るＢＳＰ型太陽電池においてもその特性が０．５８Ｖ～０．５９Ｖ、３６ｍＡ～３８ｍＡであり従来例に較べて良好であった。
【００６０】（ｐ型ポリシリコン層２の製膜条件）
原料ガスの種類と組成：B_2H_6／SiH_4／SiH_2F_2／H_2／アルゴン＝０．１／１０／１００／４００／１００
原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ
原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ
ｎ⁻単結晶シリコン基板の加熱温度：６５０℃
（ｎ⁻ポリシリコン層５の製膜条件）
原料ガスの種類と組成：PH_3／SiH_4／SiH_2F_2／H_2／アルゴン＝０．１／１０／１００／４００／１００
原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ
原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ
ｎ 単結晶シリコン基板の加熱温度：６５０℃
［実施例７］図５に示された光ＣＶＤ装置を適用した点と、ｐ型アモルファスシリコン層２とｎ アモルファスシリコン層５の製膜条件が下記である点を除き実施例２と略同一である。
【００６１】そして、この実施例に係るＢＳＦ型太陽電池においてもその特性が０．５９Ｖ～０．６０Ｖ、３７ｍＡ～３９ｍＡであり従来例に較べて良好であった。
【００６２】（ｐ型アモルファスシリコン層２の製膜条件）
製膜室内の圧力：１～１０ｍＴｏｒｒ
原料ガスの種類と組成：B_2H_6／SiH_4／H_2＝０．１／１０／３００
原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ
原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ
紫外光の照射光源：Ｈｇランプ
ｎ⁻単結晶シリコン基板の加熱温度：６００℃
（ｎ⁻アモルファスシリコン層５の製膜条件）
製膜室内の圧力：１～１０ｍＴｏｒｒ
原料ガスの種類と組成：PH_3／SiH_4／H_2＝０．１／１０／３００
原料ガスの供給速度：５ｓｃｃｍ～１００ｓｃｃｍ

原料ガスの圧力：５０ｍｔｏｒｒ～１ｔｏｒｒ
紫外光の照射光源：Ｈｇランプ
ｎ⁻単結晶シリコン基板の加熱温度：６００℃
［実施例８］図６に示されたイオンプレーティング装置を適用し、かつ、このイオンプレーティング装置内にSiF_4ガスを供給した点と、ｐ型ポリシリコン層２とｎ ポリシリコン層５の製膜条件が下記である点を除き実施例１と略同一である。
【００６３】そして、この実施例に係るＢＳＦ型太陽電池においてもその特性が０．５８Ｖ～０．５９Ｖ、３６ｍＡ～３８ｍＡであり従来例に較べて良好であった。
【００６４】（ｐ型ポリシリコン層２の製膜条件）
製膜室内の圧力：１～１０ｍＴｏｒｒ
ターゲット：B_2H_6がドープされたＳｉ
ＲＦコイルへの投入電力：５０～２００Ｗ
ｎ⁻単結晶シリコン基板の加熱温度：７００℃
（ｎ⁻ポリシリコン層５の製膜条件）
製膜室内の圧力：１～１０ｍＴｏｒｒ
ターゲット：PH_3がドープされたＳｉ
ＲＦコイルへの投入電力：５０～２００Ｗ
ｎ⁻単結晶シリコン基板の加熱温度：７００℃
【００６５】
【発明の効果】請求項１～２に係る発明によれば、ハロゲン原子を放出するSiF_4ガスあるいはフッ素化シランガスを適用しているにも拘らず製膜室内における浮遊異物の発生を確実に防止でき、かつ熱ＣＶＤ法を適用しているにも拘らず基板加熱温度の低減を図ることが可能となる。
【００６６】また、請求項３に係る発明によれば、製膜室内に配置されたｎ型又はｐ型シリコン基板近傍の空間部位に設けられた発熱部材の作用により製膜ガスの熱分解が著しく促進されるため、フッ素系ラジカルのエッチング作用と相乗して基板加熱温度を更に低減させることが可能となる。
【００６７】従って、低温製膜条件で膜質良好なｎ 又はｐ シリコン層をｎ型又はｐ型シリコン基板上に形成することが可能になるため、光電変換効率の高いＢＳＦ型太陽電池を安定して製造できる効果を有している。
【００６８】次に、請求項４に係る発明によれば、加熱されたシリコン基板面に上記ｎ⁻又はｐ⁻シリコン層を光ＣＶＤ法により製膜し、また、請求項５に係る発明によれば、フッ素化シランガス又はSiF_4ガスが存在する条件下においてイオンプレーティング法により加熱されたシリコン基板面に上記ｎ⁻又はｐ⁻シリコン層を製膜しているため、請求項１～３に係る発明と同様、低温製膜条件で膜質良好なｎ 又はｐ シリコン層をｎ型又はｐ型シリコン基板上に形成することが可能となり、光電変換効率の高いＢＳＦ型太陽電池を安定して製造できる効果を有している。
【図面の簡単な説明】

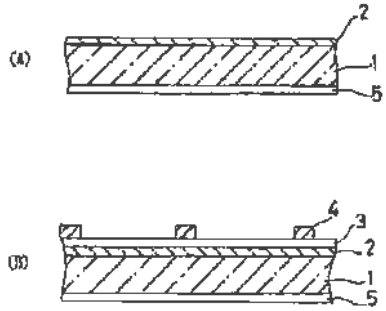
15　　16

【図１】実施例に係るＢＳＦ型太陽電池の断面図。
【図２】図２（Ａ）～（Ｂ）はＢＳＦ型太陽電池の製造工程図。
【図３】実施例１において適用された熱ＣＶＤ装置の説明図。
【図４】実施例５において適用された熱ＣＶＤ装置の説明図。
【図５】実施例７において適用された光ＣＶＤ装置の説明図。
【図６】実施例８において適用されたイオンプレーティング装置の説明図。
【図７】従来の太陽電池の斜視図。
【図８】従来の太陽電池の断面図。
【図９】従来の太陽電池の構造をモデル的に記載した構造概念図。
【図１０】従来の太陽電池のエネルギーバンド図。
【符号の説明】
1　　n⁺単結晶シリコン基板
2　　p型ポリシリコン層
5　　n⁺ポリシリコン層

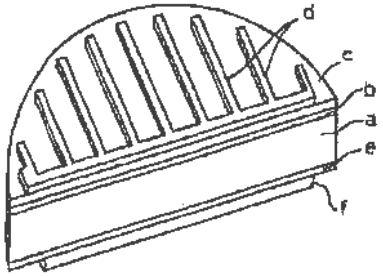
【図１】



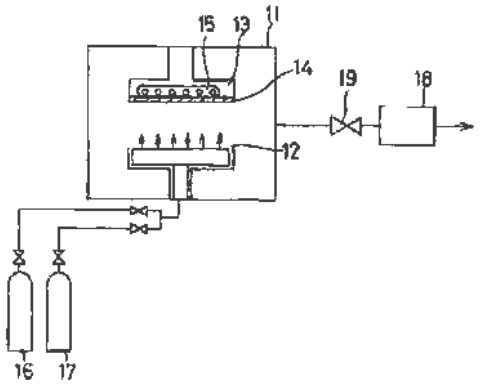
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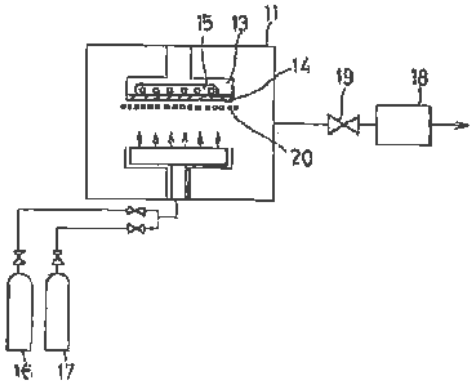
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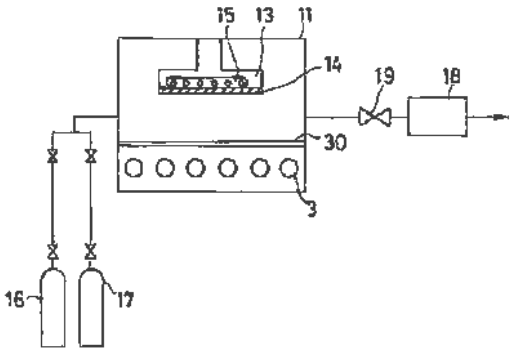
【図３】



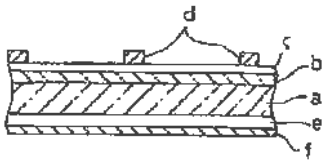
【図４】



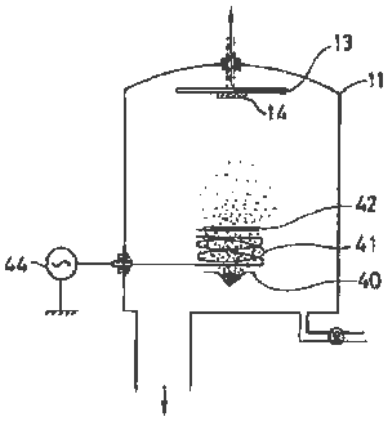
【図５】



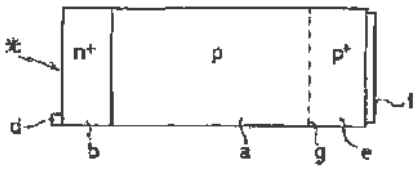
【図８】



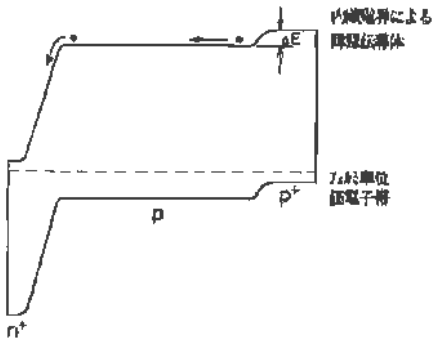
【図６】



【図９】



【図１０】



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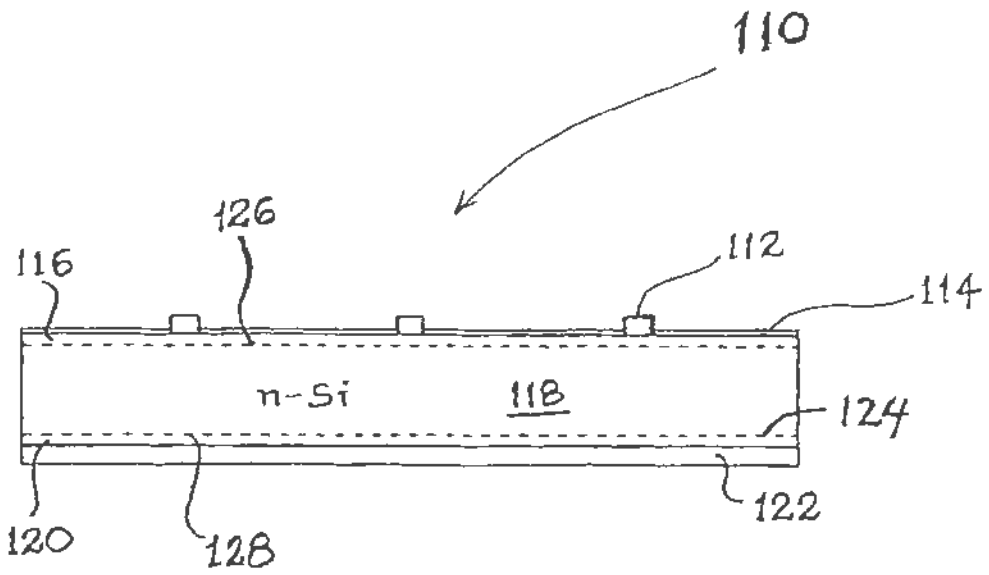
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(57) Abstract

A process for fabricating a solar cell is described. The process includes: providing a base layer (118), and fabricating an emitter layer (120) of p–type conductivity on a same side as the non–illuminated surface (128) of the base layer to provide a strongly doped p–type emitter layer and a p–n junction (124) between the n–type base layer (118) and the p–type emitter layer (120). The base layer of the present invention has n–type conductivity and is defined by an illuminated surface (126) and a non–illuminated surface (128) which is opposite to the illuminated surface.

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AN ALUMINUM ALLOY BACK JUNCTION SOLAR CELL AND A PROCESS FOR FABRICATION THEREOF

BACKGROUND OF THE INVENTION

The present invention relates to an improved solar cell and a process for fabricating thereof. More particularly, the present invention relates to a solar cell including a p-n junction located near a non-illuminated surface of the solar cell and a process for fabricating thereof.

Solar cells are widely used because they convert easily accessible energy from a light source, such as the sun, to electrical power to operate electrically driven devices, e.g., calculators, computers, and heaters used in homes. Figure 1 shows a cross-sectional view of a layered stack that makes up a conventional silicon solar cell 10. Conventional silicon solar cell 10 typically includes a p-n junction 24 sandwiched between a p-type base layer 18 and an n-type layer 16, which is located near an illuminated (front) surface 11. The term "illuminated surface," as used herein refers to the surface of a conventional solar cell that is exposed to light energy when the solar cell is active or under operation. Thus, the term "non- illuminated surface" refers to a surface that is opposite the illuminated surface. The basic structure of p-n junction 24 includes a heavily-doped (about 10^{20} cm^{-3}) n-type emitter layer (n^+) 16 at or near the illuminated surface 11 and disposed above a moderately-doped (about 10^{15} cm-

^{3}) p-type base layer (p) 18. Commercial embodiments of conventional solar cells typically include an optional anti-reflective coating 14 and a p^{+} layer 20 that is formed between p-type base layer 18 and p-type silicon contact 22.

A typical depth of p-n junction 24 from the top of the n^{+} emitter layer 16 measures about 0.5μm. A shallow front p-n junction 24 is desired in order to facilitate the collection of minority carriers that are created on both sides of p-n junction 24. Each photon of light that penetrates into p-type base layer 18 and is absorbed by base layer 18 surrenders its energy to an electron in a bound state (covalent bond) and thereby frees it. This mobile electron, and the hole in the covalent bond it left behind (which hole is also mobile), comprise a potential element of electric current flowing from the solar cell. In order to contribute to this current, the electron and hole cannot recombine, but rather are separated by the electric field associated with p-n junction 24. If this happens, the electron will travel to n-type silicon contact 12 and the hole will travel to p-type silicon contact 22.

In order to contribute to the solar cell current, photogenerated minority carriers (holes in the n^{+} emitter layer and electrons in the p-type base layer) should exist for a sufficiently long time so that they are able to travel by diffusion to p-n junction 24 where they are collected. The average distance over which minority carriers can travel without being lost by recombining

with a majority carrier is called the minority carrier diffusion length. The minority carrier diffusion length generally depends on such factors as the concentration of defects in the silicon crystal (i.e. recombination centers) and the concentration of dopant atoms in the silicon. As the concentration of either defects or dopant atoms increases, the minority carrier diffusion length decreases. Thus, the diffusion length for holes in the heavily-doped n^+ emitter layer 16 is much less than the diffusion length for electrons in moderately-doped p-type base layer 18.

Those skilled in the art will recognize that the n^+ emitter layer 16 is nearly a "dead layer" in that few minority charge carriers created in emitter layer 16 are able to diffuse to p-n junction 24 without being lost by recombination. It is desirable to have n^+ emitter layer 16 that is shallow or as close to surface of emitter layer 16 as possible for various reasons. By way of example, a shallow emitter layer allows relatively few photons to be absorbed in n^+ emitter layer 16. Furthermore, the resulting photogenerated minority carriers created in n^+ emitter layer 16 find themselves close enough to p-n junction 24 to have a reasonable chance of being collected (diffusion length $\geq$ junction depth).

Unfortunately, in the conventional solar cell design, the depth of n^+ emitter layer is limited and cannot be as shallow as desired. Metal from

emitter contacts 12, especially those formed by screen-printing and firing, can penetrate into p-n junction 24 and ruin or degrade it. The presence of metal in the p-n junction 24 "shorts" or "shunts" the junction. Therefore, although a shallow and lightly-doped n^+ emitter layer 16 is desired in order to enhance the current produced by the cell, in practice, however, n^+ emitter layer 16 is relatively deeper and more heavily-doped than desired to avoid shunting p-n junction 24. Consequently, in conventional solar cells, the deep location of n^+ emitter layer 16 compromises the amount of current produced by the cell.

What is needed is a structure and process for fabricating a silicon solar cell, which has a high minority carrier diffusion length, eliminates shunting of the p-n junction and does not compromise the amount of current produced.

SUMMARY OF THE INVENTION

In one aspect, the present invention provides a solar cell. The solar cell includes a base layer having dopant atoms of n-type conductivity and being defined by an illuminated surface and a non-illuminated surface. The illuminated surface has light energy impinging thereon when the solar cell is exposed to the light energy and the non-illuminated surface is opposite the illuminated surface. The solar cell further includes a back surface emitter layer that is made from an aluminum alloy to serve as a layer of p-

type conductivity. The solar cell further still includes a p-n junction layer disposed between the non-illuminated surface of the base layer and the back surface layer.

In another aspect, the present invention provides a process for fabricating a solar cell. The process includes: (1) providing a base layer, (2) fabricating an emitter layer of p-type conductivity on a same side as the non-illuminated surface of the base layer to provide a strongly doped p-type emitter layer and a p-n junction between the n-type base layer and the p-type emitter layer. The base layer of the present invention has n-type conductivity and is defined by an illuminated surface and a non-illuminated surface. The illuminated surface has light energy impinging thereon when the solar cell is exposed to the light energy and the non-illuminated surface is opposite the illuminated surface.

These and other features of the present invention will be described in more detail below in the detailed description of the invention and in conjunction with the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which:

Figure 1 shows a cross-sectional view of a conventional solar cell.

Figure 2 shows a cross-sectional view of a solar cell, in accordance with an embodiment of the present invention.

Figures 3A-3D show various stages of fabrication, according to one embodiment of the present invention, for the solar cell of Figure 2.

Figure 4 shows a graph of a measured I-V curve of an aluminum alloy back junction dendritic web solar cell.

Figure 5 shows a graph of internal quantum efficiency of an aluminum alloy back junction dendritic web solar cell.

Figure 6 shows a cross-sectional view of a solar cell, in accordance with another embodiment of the present invention, with partial metal coverage on the back side of the solar cell.

Figure 7 shows a cross-sectional view of a solar cell, in accordance with yet another embodiment of the present invention, whose contacts to the base layer are at the back of the cell in interdigitated fashion.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described in detail with reference to the presently preferred embodiments as illustrated in accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps and/or structures have not been described in detail in order to not unnecessarily obscure the present invention.

It is important to bear in mind that a minority carrier electron diffusion length (i.e. electrons in p-type silicon) is generally different from a minority carrier hole diffusion length (i.e. holes in n-type silicon) for a given doping concentration. This difference may depend on the nature of the crystalline defect, which may act as a recombination center. In dendritic web silicon, for example, the primary defects are precipitates of silicon oxide which nucleate on dislocation cores. The interface between the silicon oxide precipitate and the surrounding silicon carries a positive charge because of the mismatch of the atomic structure of the two materials. A negatively charged minority carrier electron is attracted to such a positively charged interface. Such a defect can capture and hold an electron until one of the numerous majority

carrier holes wanders by the defect whereupon the electron can fall into the hole in a recombination event.

The present invention therefore recognizes that for a solar cell substrate layer, n-type doping may be desirable to achieve a higher minority carrier diffusion length than that obtained with p-type doping. A solar cell substrate having n-type conductivity requires an n-type base layer. A p-n junction was, therefore, fabricated employing the n-type base layer and an emitter layer at the illuminated side that includes boron, which is a practical choice for a p-type dopant.

Unfortunately, it was found that boron diffusions frequently leave a stained silicon surface because of the formation of boron-silicon compounds. Such a stain seriously degrades the appearance of the surface of a solar cell. Boron stains may be removed at the expense of additional and unwanted processing steps such as thermal oxidation of the stained surface followed by chemically removing the thermal oxide. Thus, according to the findings of the present invention, for silicon materials in which n-type doping gives higher minority carrier diffusion length than does p-type doping, the desirability of a front p-n junction is offset by the presence of a boron stain for the p-type emitter layer.

Referring back to Figure 1, commercial solar cells 10 have an n^+pp^+

structure. The n-type emitter layer 16 is commonly made using phosphorus diffusion (in which staining is not a problem), the silicon substrate is doped p-type, and back silicon surfacc 20 is typically doped p^+ to promote ohmic contact with contact metal layer 22. An ohmic contact has a low resistance. The voltage developed across an ohmic contact has a linear relationship to the current flowing through the contact. In contrast, the voltage developed across a rectifying contact has a non-linear relationship to the current flowing through the contact. An aluminum-silicon alloy may be used to provide the p^+ doping and the back metal contact. More importantly, the commercial solar cell 10 has p-n junction 24 located at the front of the cell. As explained above, therefore, n^+ emitter layer 16 is forced to be deeper than desired to avoid shunting the front junction. If a silicon material with superior minority carrier diffusion length with n-type doping is to be used with a front p-n junction, p-type emitter layer is boron-doped to be practical. Boron doping, as explained above, gives a stained surface, which degrades cell appearance and which can only be removed with additional and unwanted processing.

The present invention, therefore, provides a p-n junction located at the back end of the solar cell. Figure 2 shows a solar cell layer stack 110, according to one embodiment of the present invention, that has the p-n junction located at the back end (near the non-illuminated surface of the base

layer), so it is impossible for the front metal contacts 112 to shunt the p-n junction. Since aluminum may be the choice of dopant in the silicon p^+ layer, it is also impossible for the aluminum to shunt the junction.

Solar cell layer stack 110 includes a base layer 118 of n-type conductivity, which is defined by an illuminated surface (front or top surface) 126 and a non-illuminated surface (back or bottom surface) 128. A portion of base layer 118 near illuminated surface 126 is passivated by a shallow n^+ layer 116, which is typically formed by phosphorus diffusion into a silicon layer. This embodiment, therefore, realizes the advantage of the conventional n^+ layer and does not suffer from boron staining. An optional anti-reflective (AR) coating 114 is disposed atop n^+ layer 116. If the coating is present as shown in Figure 2, silver contacts 112 fire through AR coating 114 to reach the surface of n^+ silicon layer 116.

A p-n junction 124 is formed at non-illuminated surface 128 or the interface between base layer 118 and an aluminum doped silicon layer 120, which functions as a p^+ emitter layer in the solar cell layer stack of the present invention. An aluminum-silicon eutectic metal layer 122, which results when aluminum is alloyed with silicon, is disposed beneath p^+ layer 120 and serves as a self-aligned contact to p^+ emitter layer 120. It is noteworthy that boron

doping is absent from the solar cell structure of Figure 2, so that there is no boron stain to compromise the appearance of the front surface.

The placement of the p-n junction at the back side of cell 110 is a unique feature of solar cell 110 shown in Figure 2. It should be borne in mind that no other current silicon solar cell design employs such an aluminum alloy back junction. Furthermore, the depth of n^+ layer 116 is of no real concern regarding shunting because p-n junction 124 is at the back of cell 110.

In accordance with one embodiment, n-type base layer 118 is a dendritic web silicon crystal having a resistivity that is generally between about 5 Ω-cm and about 100 Ω-cm, and preferably about 20 Ω-cm. The thickness of the dendritic web silicon substrate crystal is generally between about 30 μm and about 200 μm, and preferably about 100 μm. In order for the cell 110 to operate at a practical energy conversion efficiency level, the hole diffusion length in n-type base layer 118 is, in one implementation of this embodiment, slightly less than the thickness of base layer 118. In a preferred implementation, however, the hole diffusion length is substantially equal to the thickness of base layer 118 and more preferably exceeds the thickness of base layer 118.

Locating the p-n junction near the back of the cell instead of near the front of the cell is counterintuitive to one skilled in the art. It is normally

desirable to have the p-n junction near the front of the cell because the number of photons absorbed per unit depth decreases as one proceeds from the illuminated surface toward the back surface. For example, about 52% of the incident photons are absorbed within the first 5 μm of the base layer from the illuminated surface, while about 10% are absorbed within the second 5 μm slice of depth, and about 6% are absorbed within the third 5 μm slice. In fact, about 75% of the incident photons are absorbed within the top 30 μm of the base layer.

Since the absorption of photons results in the generation of electron-hole pairs, and since the minority carrier members of the pairs diffuse to the junction in order to be collected, placing the p-n junction near the illuminated surface is reasonable. As a rule of thumb, those minority carriers created beyond one diffusion length from the junction will not be collected and so will not contribute to the solar cell photocurrent.

Figures 3A-3D show important intermediate solar cell structures formed at different stages of a fabrication process, according to one embodiment of the present invention. The illustrated embodiment of the inventive processes may begin when a single crystal silicon substrate of n-type conductivity is fabricated using well-known conventional techniques, e.g., Czochralski, Float-zone, Bridgman, edge defined film-fed growth (EFG), string ribbon growth,

cast silicon crystallized by directional solidification, and dendritic web growth. In a preferred embodiment, however, the dendritic web growth technique may be implemented to produce an n-type single crystal substrate.

Referring to Figure 3A, the n-type single crystal serves as a base layer 218, below which a p-n junction of the solar cell is subsequently formed. In a next step, a strongly doped n-type layer 216 (hereinafter referred to as an "n^+ layer") may be formed atop base layer 218 using diffusion processes well known to those skilled in the semiconductor and solar cell fabrication art. In accordance with one embodiment of the present invention, a layer containing phosphorous is applied to the top surface of base layer 218 and the phosphorous atoms are driven into base layer 218 from any heat source. The phosphorous layer is preferably from a screen printed paste or from a liquid dopant, and the heat source is a rapid thermal processing (RTP) unit or a belt furnace maintained at a temperature that is between about 750 °C and about 1050 °C and preferably about 950 °C. At these temperatures, the diffusion time may generally be between about 30 seconds to about 30 minutes and preferably be about 5 minutes. As a result, there is formed a phosphorus-doped n^+ passivating layer having a thickness that is generally between about 0.1 μm and about 1 μm, preferably about 0.3 μm, with a sheet resistance of generally between about 10 Ω/square and about

200 Ω/square and preferably about 40 Ω/square.

Alternatively, in another embodiment, the top surface of base layer 218 is subjected to phosphorous ion implantation and a portion near the top surface of base layer is transformed into n^+ layer 216.

In accordance with yet another embodiment, base layer 218 is passivated with a transparent dielectric layer which may have an appreciable positive or negative charge. In one implementation of this embodiment, the base layer is passivated with a layer of thermally grown silicon dioxide having a thickness of between about 50 Å and about 500 Å, and preferably about 150 Å. In this embodiment, the passivation of base layer 218 may be carried out in a rapid thermal processing unit at temperatures that are generally between about 800 °C and about 1050 °C and preferably about 1000 °C. Such temperature treatment is carried out for times that are generally between about 30 seconds and about 30 minutes and preferably about 50 seconds. Regardless of how the n^+ layer is passivated, or whether it is passivated those skilled in the art will recognize that at the conclusion of forming n^+ layer 216, a high-low junction (n^+n) is formed at the top of base layer 218.

An anti-reflective coating 214 may then be deposited on top of n^+ layer 216, as shown in Figure 3B. By way of example, plasma-enhanced chemical

vapor deposition (PECVD) of silicon nitride or atmospheric pressure chemical vapor deposition (APCVD) of titanium dioxide is carried out to form anti-reflective coating 214.

Next, conventional techniques may be employed to deposit an aluminum layer 222 on a bottom surface or non-illuminated surface of base layer 218. According to one embodiment of the present invention, aluminum is deposited by screen printing a pure aluminum paste onto bottom surface of base layer 218. In one implementation of this embodiment, aluminum layer 222 is deposited by screen-printing over nearly the entire back of the cell to a thickness that is generally between about 5 μm and about 30 μm, and preferably about 15 μm. The partially fabricated solar cell is then heated in a radiantly-heated belt furnace to a temperature comfortably above the aluminum-silicon eutectic temperature of about 577 °C, e.g., that may generally be between about 700 °C and about 1000 °C and preferably about 800 °C, for a long enough duration, e.g., generally between about 0.1 minute and about 10 minutes and preferably about 2 minutes, to facilitate alloying of at least some aluminum from layer 222 with base layer 218. During the alloying process, the temperature treatment inside the belt furnace is high enough so that aluminum may effectively dissolve silicon. At such high temperatures, a portion of the base layer that measures approximately one-

third the thickness of the aluminum layer is effectively dissolved to create p^+ layer 220 shown in Figure 3C. By way of example, at about 800 °C, a 15 μm thick aluminum layer 222 dissolves a 5 μm portion of a silicon base layer. Consequently, p^+ layer 220 is silicon doped with aluminum and contact layer 222 is an alloy that is about 88% aluminum by weight and about 12% silicon by weight the eutectic composition.

The p^+ emitter layer is created as described hereinafter. As the silicon cools, it continues to solidify or grow onto the underlying silicon, also incorporating a modest amount of the aluminum dopant, on the order of between about 10^{18} and about 10^{19} aluminum atoms per cubic centimeter. The concentration of aluminum atoms is significantly less than the concentration of silicon atoms, which is about 10,000 times larger at about $5x10^{22}$ atoms per cubic centimeter. As shown in Figure 3C, after cooling the layers, a portion of base layer 218 near the non-illuminated surface is transformed to a strongly doped p-type layer 220 (hereinafter referred to as a "p^+ layer"), by liquid phase epitaxy. Some of the silicon that was dissolved becomes part of the aluminum-silicon eutectic layer 222. The silicon that was not dissolved by the aluminum acts as a template for restructuring the silicon crystal as it is epitaxially regrown.

The aluminum-silicon eutectic metal layer 222 is a good conductor (has

a low electrical resistance), and serves as a self-aligned metal contact to the solar cell. The thickness of aluminum-silicon eutectic metal layer 222 is generally between about 1 μm and about 30 μm and preferably about 15 μm.

Figure 3D shows the structure resulting after depositing metal contacts and firing through the optional anti-reflective coating. By way of example, a silver layer is screen-printed onto the n^+ layer 216, covering about 7% of the front surface in a grid pattern. Silver may be deposited by screen-printing to a thickness that is generally between about 5 μm and about 20 μm and preferably about 10 μm. The resulting partially fabricated solar cell structure is then run through a belt furnace maintained at a temperature that is generally between about 700 °C and about 900 °C and preferably about 760 °C. The time for running the cell through the furnace is short in order to avoid allowing impurities in the silver paste from diffusing into the silicon. In one embodiment of the present invention, the time for running the cell through the belt furnace is between about 0.1 minutes and about 10 minutes. In a preferred embodiment, however, the time is about 40 seconds. The thickness of silver ohmic contacts 212 to n^+ layer 216 is generally between about 1 μm and about 20 μm and preferably about 10 μm. If an optional anti-reflective coating is deposited, then the silver layer is fired through the coating. Both operations may (with or without anti-reflective coating) be performed in a

radiantly-heated belt furnace. The fabrication steps of the present invention realize high-throughput and low-cost manufacturing.

Figure 4 depicts an I-V curve, which shows a light energy to electrical energy conversion efficiency of about 12.5% for an aluminum alloy back junction dendritic web silicon solar cell with full back metal coverage of the present invention. The solar cell employed to obtain the data shown in Figure 4 has a nominal thickness of about 100 μm and an area of about 25 cm^2. Other parameters include a short-circuit current density of about 28.2 mA/cm^2, open-circuit voltage of about 0.595 V, and fill factor of about 0.747. The knee of the curve shows a maximum power point, where V_{mp} is about 0.480V and I_{mp} is about 0.653A.

Figure 5 depicts measurements of spectral reflectivity (solid triangles) 510, external quantum efficiency (open squares) 512, and internal quantum efficiency (solid squares) 514 for the solar cell of Figure 4. Measured reflectivity indicates that about 47% of the long wavelength (> 950 nm) light is reflected from the aluminum-silicon eutectic metal layer at the back surface. This reflected light then gets a second pass through the silicon and adds to the overall efficiency. Calculation of the internal quantum efficiency using the one-dimensional finite element model PC1D indicates a hole diffusion length of about 200 μm in the base of this cell. This is double the cell thickness, as

required for good performance. The internal quantum efficiency curve has a positive slope over the range of about 500 nm to about 850 nm, indicating that the p-n junction is at the back of the cell, which is also noteworthy. In a conventional solar cell, the internal quantum efficiency curve would show a negative slope, indicating that the p-n junction is at the front of the cell.

Figure 6 shows a solar cell layer stack 300, in accordance with another embodiment of the present invention, that is substantially similar to the solar cell 110 of Figure 2, except that solar cell 300 has only part of the back surface converted to a p-type layer and covered with metal. Thus, solar cell 300 is referred to as having "partial" metal coverage on the back side as opposed to have "full" metal coverage, as shown in Figure 2 for solar cell 110, where the entire back surface is covered with metal. The partial metal coverage design of Figure 6 eliminates bowing of the thin cells, which results from a differential thermal contraction between the silicon and the aluminum-silicon eutectic metal layer upon cooling from the eutectic temperature of about 577 °C. It is important to bear in mind that such bowing sometimes occurs when full back metal coverage is used. The segmented metal also reduces the cost of aluminum. The exposed n-type base layer surfaces 330 between metal islands at the back may be passivated in order to obtain respectable energy conversion efficiency. By way of example, the

passivation step may be performed after the aluminum alloying step by growing a thermal oxide of about 115 Å thickness in a rapid thermal processing unit at about 1000 °C for about 50 seconds. An anti-reflective coating may not be applied in this preliminary effort. Efficiencies up to about 6.8% were obtained for 25 cm^2 dendritic web silicon cells with screen-printed metals but without anit-reflective coating. The expected efficiency with an anti-reflective coating is about 9.9%.

Figure 7 depicts a solar cell layer stack 400, according to yet another embodiment of the present invention, that is substantially similar to the solar cell 300 of Figure 6, except that solar cell 400 has n-type contacts 412 to the n-type base layer moved from the front of the cell to the back of the cell in an interdigitated fashion.

This structure shown in Figure 7 has the added advantage of reducing to zero the shadowing of the front surface by contacts. Interconnecting cells in a module is also expected to be simpler with both contacts on the back side of the cell in that surface mount technology can be used. The n^+ regions 424 adjacent silver contacts 412 may be formed in a separate step. Alternatively, the source of this n-type dopant can be the contact material itself if a self-doping contact metal, such as a silver-antimony alloy, is used rather than pure silver. A prototype dendritic web silicon solar cell of this type with

screen-printed metals, titanium dioxide anti-reflective coating and about 2.5 cm^2 area had an efficiency of about 10.4%.

It is noteworthy that although the present invention is described in terms of a silicon crystal substrate and aluminum, there is no reason why other substrate and conductive materials cannot be similarly employed. Furthermore, it can therefore be appreciated that new and novel structure and processes for fabricating an aluminum alloy back junction solar cell has been described. It will be appreciated by those skilled in the art that, given the teaching herein, numerous alternatives and equivalents will be seen to exist which incorporate the invention disclosed hereby. As a result, the invention is not to be limited by the foregoing exemplary embodiments, but only by the following claims.

CLAIMS

What is claimed is:

1. A solar cell, comprising:

a base layer including dopant atoms of n-type conductivity and being defined by an illuminated surface and a non-illuminated surface, said illuminated surface having light energy impinging thereon when said solar cell is exposed to said light energy and said non-illuminated surface is opposite said illuminated surface;

a back surface emitter layer including an aluminum alloy contact and serving as a layer of p-type conductivity; and

a p-n junction layer disposed between said non-illuminated surface of said base layer and said back surface layer.

2. The solar cell of claim 1, further comprising a strongly doped n-type layer that is disposed adjacent the illuminated surface of the base layer.

3. The solar cell of claim 2, wherein the strongly doped n-type layer includes phosphorous atoms.

4. The solar cell of claim 2, further comprising an anti-reflective coating layer that is disposed adjacent the strongly doped n-type layer.

5. The solar cell of claim 4, further comprising metal contacts that fire through the anti-reflective coating to reach the strongly doped n-type layer.

6. The solar cell of claim 5, wherein the metal contacts include silver and serve as ohmic contacts to the base layer.

7. The solar cell of claim 5, wherein the metal contacts have a thickness of 1 μm to 20 μm.

8. The solar cell of claim 1, wherein a diffusion length of a hole through said base layer is slightly less than a thickness of the base layer.

9. The solar cell of claim 8, wherein the diffusion length of the hole through said base layer is substantially equal to the thickness of said base layer.

10. The solar cell of claim 9, wherein the diffusion length of the hole through the base layer exceeds the thickness of the base layer.

11. The solar cell of claim 10, wherein the n-type base layer is fabricated using one technique selected from the group consisting of cast silicon crystallized by directional solidification, edge-defined film-fed growth, string ribbon growth, Czochralski, Float-zone, Bridgman and dendritic web growth.

12. The solar cell of claim 11, wherein the n-type base layer is a dendritic web silicon layer.

13. The solar cell of claim 12, wherein the n-type base layer has a resistivity that is between about 5 Ω-cm and about 100 Ω-cm.

14. The solar cell of claim 12, wherein the n-type base layer has a resistivity that is about 20 Ω-cm.

15. The solar cell of claim 12, wherein a thickness of the n-type base layer is between about 30 μm and about 200 μm.

16. The solar cell of claim 15, wherein a thickness of the n-type base layer is about 100 μm.

17. The solar cell of claim 1, wherein the aluminum alloy layer acts as a self-aligned contact for the non-illuminated surface of the emitter layer.

18. The solar cell of claim 17, wherein the aluminum alloy layer is an aluminum-silicon eutectic metal layer.

19. The solar cell of claim 17, wherein the aluminum-silicon eutectic metal layer has a thickness that is between about 1 μm and about 30 μm.

20. The solar of claim 17, wherein the aluminum alloy layer substantially covers the non-illuminated surface of the base layer.

21. The solar cell of claim 17, wherein the aluminum alloy layer partially covers the non-illuminated surface of the base layer.

22. The solar cell of claim 21, wherein the aluminum alloy layer partially covers the non-illuminated surface of the base layer in a segmented fashion and interdigitated n-type metal contacts are disposed in spaces between the segmented aluminum alloy layer.

23. The solar cell of claim 22, further comprising a strongly doped n-type layer adjacent the metal contacts to facilitate connection to the base layer.

24. A process for fabricating a solar cell, comprising:

providing a base layer, said base layer having n-type conductivity and being defined by an illuminated surface and a non-illuminated surface, said illuminated surface having light energy impinging thereon when said solar cell is exposed to said light energy and said non-illuminated surface is opposite said illuminated surface;

fabricating an emitter layer of p-type conductivity on the same side as said non-illuminated surface of said base layer to provide a strongly doped p-type emitter layer and a p-n junction between said n-type base layer and said p-type emitter layer.

25. The process of claim 24, wherein said providing the base layer includes fabricating a single crystal silicon substrate of n-type conductivity using one technique selected from a group consisting of Czochralski, Float-zone, Bridgman, cast silicon crystallized by directional solidification, edge-defined film-fed growth (EFG), string ribbon growth, and dendritic web growth.

26. The process of claim 25, wherein said providing the base layer includes fabricating a single crystal silicon substrate of n-type conductivity using dendritic web growth.

27. The process of claim 24, wherein said fabricating said emitter layer includes:

providing an aluminum layer on said non-illuminated surface of said base layer; and

alloying said aluminum from said back with at least a portion of said base layer to transform said portion of said base layer into said emitter layer.

28. The process of claim 27, wherein the base layer includes silicon and said alloying forms the emitter layer which includes aluminum atoms as p-

type dopant and a self-aligned contact layer for a back surface of the emitter layer that includes an aluminum-silicon alloy.

29. The process of claim 28, wherein said providing aluminum includes screen-printing aluminum on the non-illuminated side of the base layer.

30. The process of claim 28, wherein said alloying is accomplished at a temperature of between about 700°C and about 1000°C.

31. The process of claim 28, wherein said alloying is accomplished by maintaining said temperature for a time that is between about 1 minute and about 30 minutes.

32. The process of claim 28, wherein the illuminated surface of the base layer is passivated by a phosphorus-doped layer having a thickness of between about 0.1 μm and about 1 μm.

33.The process of claim 32, further comprising forming an anti-reflective coating that includes preferably titanium dioxide or silicon nitride is formed above the phosphorus-doped layer.

34. The process of claim 33, wherein n-type metal contacts are formed above the base layer to provide ohmic contact to the base layer.

35. The process of claim 34, wherein n-type metal contacts are formed

below the base layer to provide ohmic contact to the base layer.

36. The process of claim 27, wherein said providing aluminum layer includes providing aluminum such that said aluminum alloy layer formed in said alloying substantially covers the back side of the emitter layer.

37. The process of claim 27, wherein said providing aluminum layer includes providing an aluminum layer that partially covers the non-illuminated surface of the base layer such that said alloying forms an emitter layer that covers the non-illuminated surface of the base layer in a segment fashion.

38. The process of claim 37, further comprising forming interdigitated n-type metal contacts that are disposed in spaces between the segmented aluminum alloy layer.

39. The process of claim 24, further comprising passivating substantially all exposed illuminated and non-illuminated surfaces of the base layer with a dielectric layer.

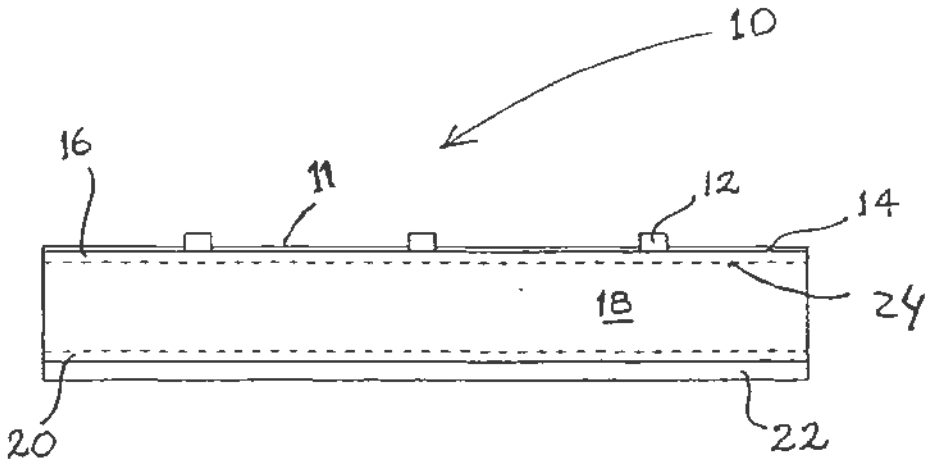


FIGURE 1

PRIOR ART

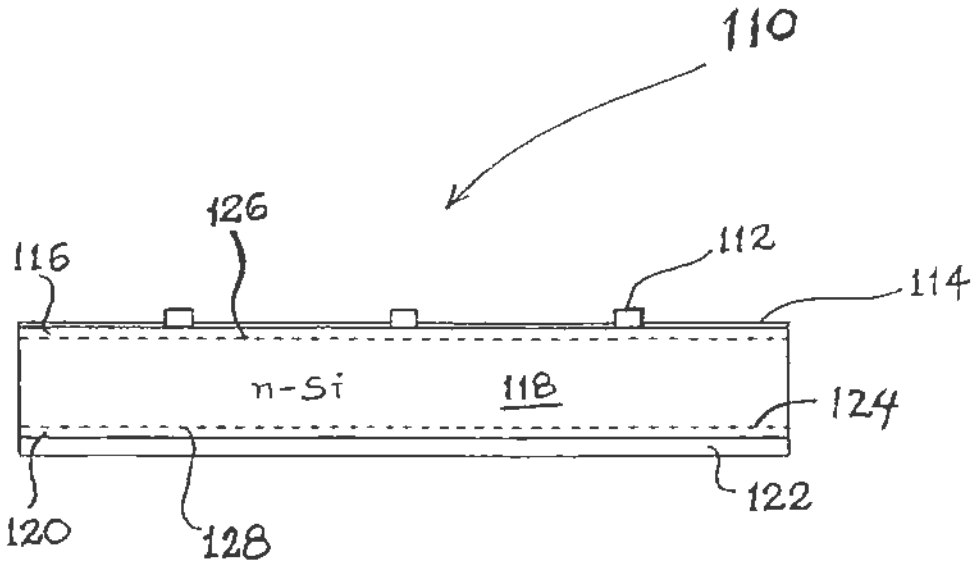


FIGURE 2

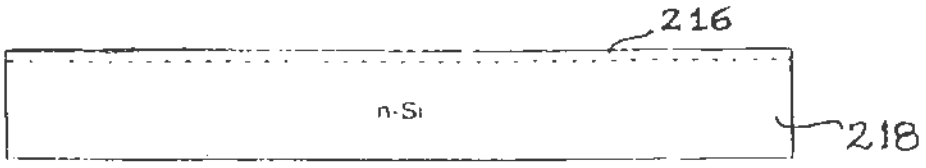


FIGURE 3A

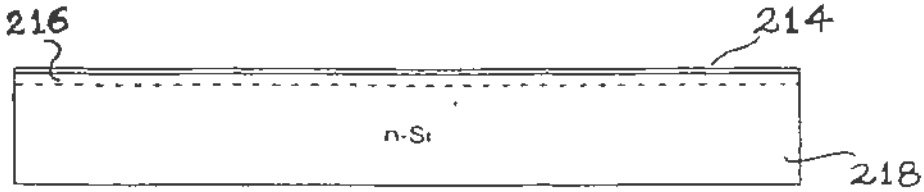


FIGURE 3B

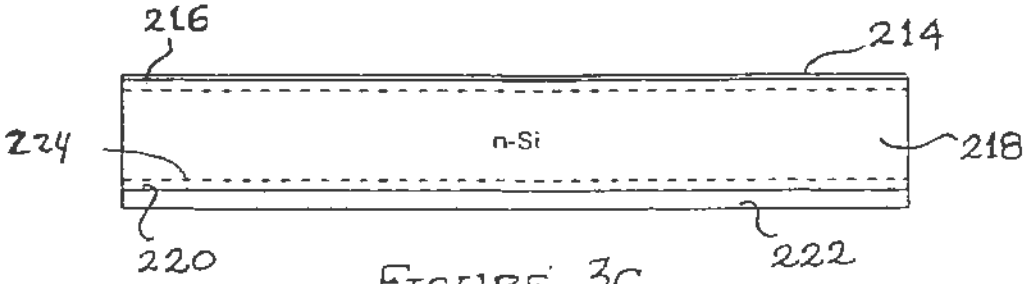


FIGURE 3C

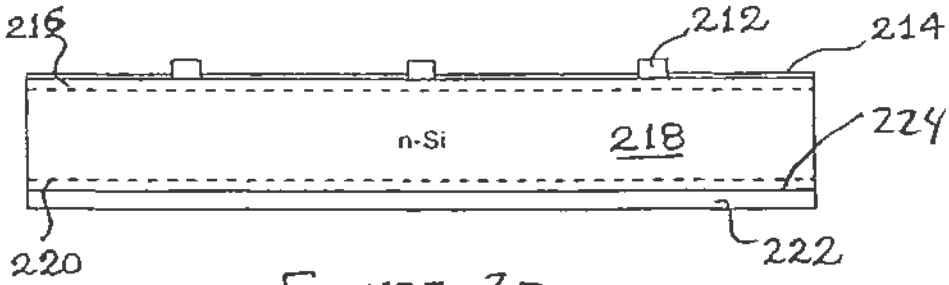


FIGURE 3D

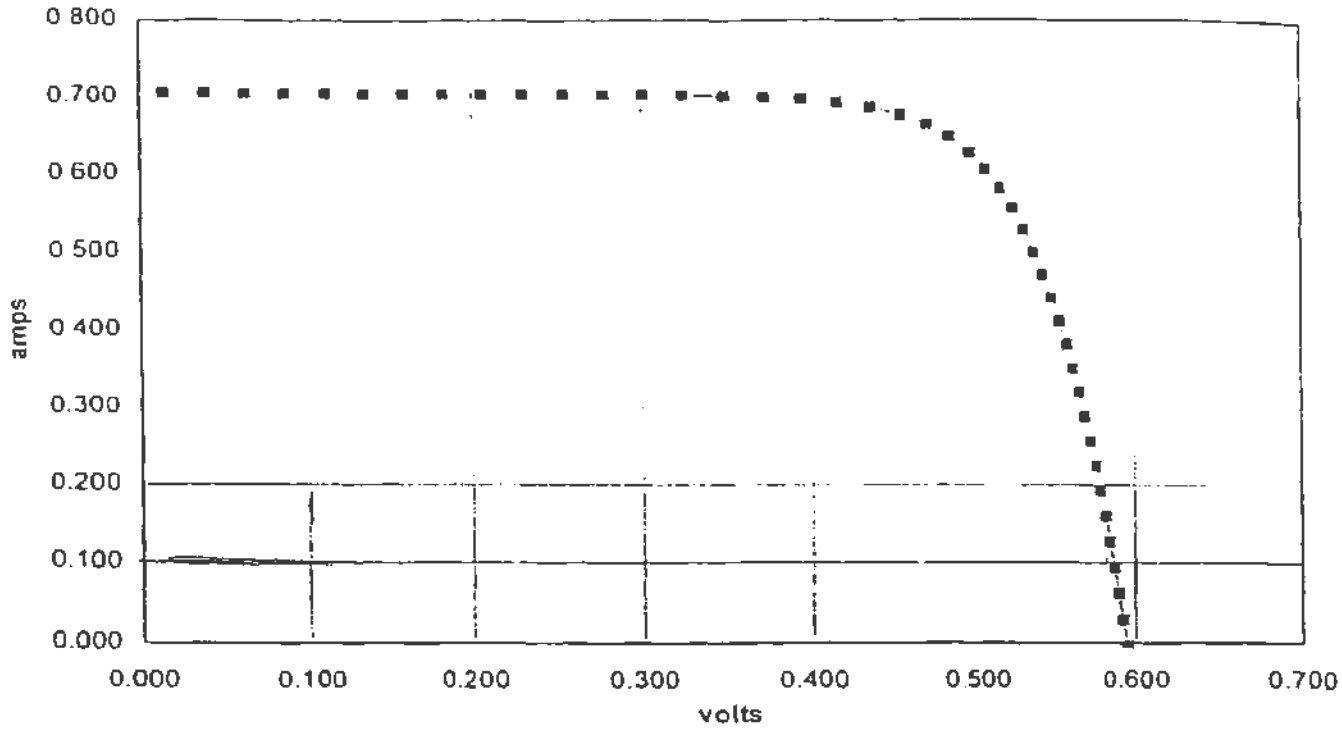

0 800
0.700
0 600
0 500
0 400
0.300
0.200
0.100
0.000
amps
0.000
0.100
0.200
0.300
0.400
0 500
0.600
0.700
volts

FIGURE 4

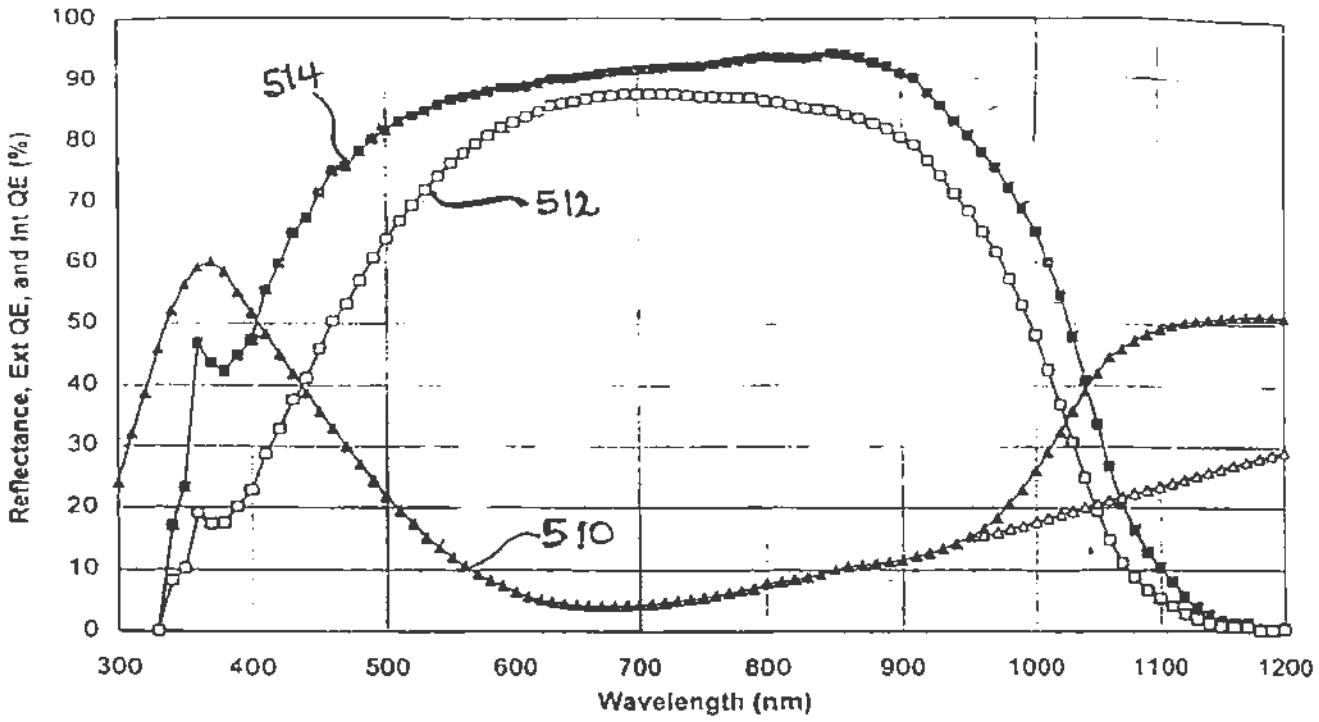

514
512
510
Reflectance, Ext QE, and Int QE (%)
Wavelength (nm)
0
10
20
30
40
50
60
70
80
90
100
300
400
500
600
700
800
900
1000
1100
1200

FIGURE 5

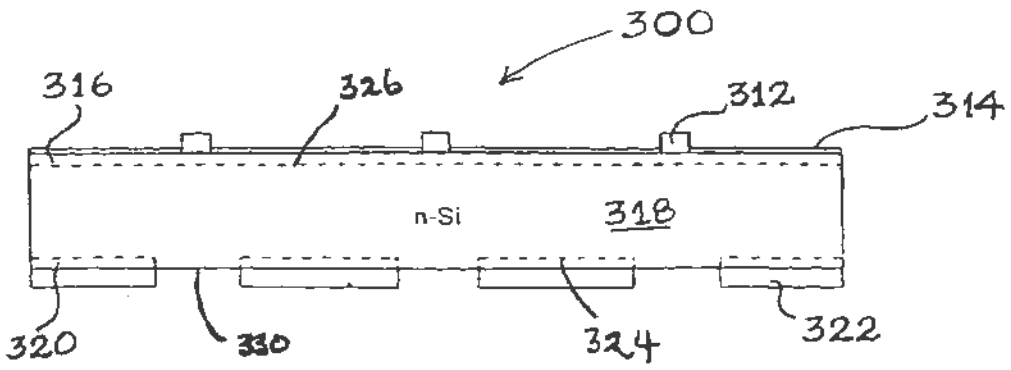


FIGURE 6

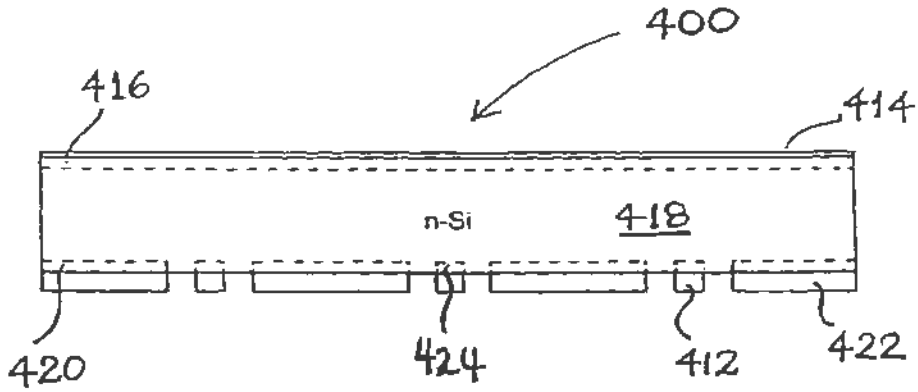


FIGURE 7

INTERNATIONAL SEARCH REPORT

Inter onal Application No
PCT/US 00/02609

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L31/068 H01L31/0352 H01L31/0224

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, COMPENDEX, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	EP 0 776 051 A (EBARA SOLAR INC) 28 May 1997 (1997-05-28) the whole document	1-4, 8-33,35, 37,38 5-7,34, 36,39
Y	WO 97 13280 A (EBARA SOLAR INC ;SALAMI JALAL (US); SHIBATA AKIO (US); MEIER DANIE) 10 April 1997 (1997-04-10) figure 1	5-7,34, 36,39

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 July 2000	24/07/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Werner, A

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inter ›nal Application No
PCT/US 00/02609

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	SALAMI J ET AL: "Self-aligned locally diffused emitter (SALDE) silicon solar cell" SOLAR ENERGY MATERIALS AND SOLAR CELLS,NL,ELSEVIER SCIENCE PUBLISHERS, AMSTERDAM, vol. 48, no. 1-4, 1 November 1997 (1997-11-01), pages 159-165, XP004111846 ISSN: 0927-0248 figure 1 ---	
A	US 4 916 503 A (UEMATSU TSUYOSHI ET AL) 10 April 1990 (1990-04-10) figure 2B -----	

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Information on patent family members

Inter ional Application No
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(10) International Publication Number
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(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
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(72) Inventor; and
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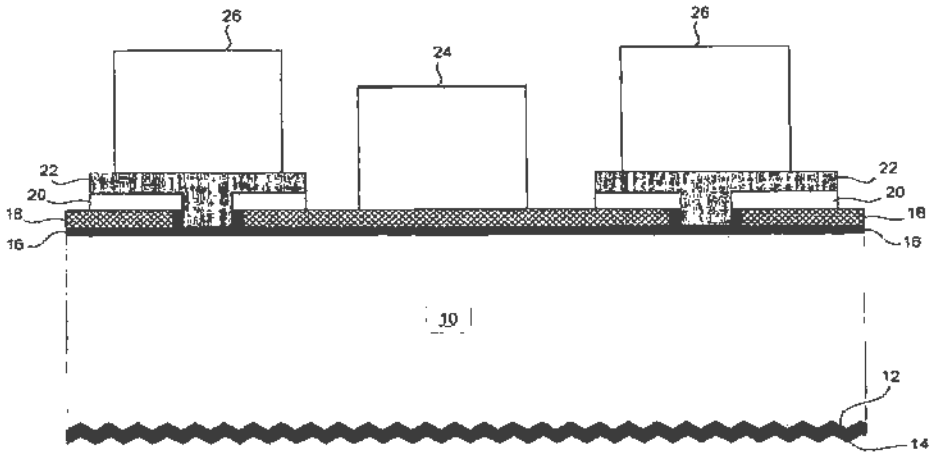
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(54) Title: SOLAR CELL HAVING DOPED SEMICONDUCTOR HETEROJUNCTION CONTACTS



(57) Abstract: A silicon solar cell has doped amorphous silicon contacts formed on a tunnel silicon oxide layer on a surface of a silicon substrate. High temperature processing is unnecessary in fabricating the solar cell.

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SOLAR CELL HAVING DOPED SEMICONDUCTOR HETEROJUNCTION CONTACTS

BACKGROUND OF THE INVENTION

[0001] This invention relates generally to photovoltaic solar cells, and more particularly the invention relates to a solar cell structure which is efficient in operation and economical to manufacture.

[0002] The use of photovoltaic cells for the direct conversion of solar radiation into electrical energy is well known, see Swanson, U.S. Patent No. 4,234,352 for example. Briefly, the photovoltaic cell comprises a substrate of semiconductive material having a p-n junction defined therein. In the planar silicon cell the p-n junction is formed near a surface of the substrate which receives impinging radiation. Radiated photons create mobile carriers (holes and electrons) and the substrate which can be directed to an electrical circuit outside of the cell. Only photons having at least a minimum energy level (e.g., 1.1 electron volt for silicon) can generate an electron-hole pair in the semiconductor pair. Photons having less energy are either not absorbed or are absorbed as heat, and the excess energy of photons having more than 1.1 electron volt energy (e.g. photons have a wavelength of 1.1 μm and less) create heat. These and other losses limit the efficiency of silicon photovoltaic cells in directly converting solar energy to electricity to less than 30%.

[0003] Solar cells with interdigitated contacts of opposite polarity on the back surface of the cell are known and have numerous advantages over conventional solar cells with front side metal grids and blanket or grid metallized backside contacts, including improved photo-generation due to elimination of front grid shading, much reduced grid series resistance, and improved "blue" photo-response since heavy front surface doping is not required to minimize front contact resistance because there are no front contacts. In addition to the performance advantages, the back-contact cell structure allows simplified module assembly due to coplanar contacts. See Swanson U.S. Patent No. 4,927,770 for example.

[0004] While interdigitated back-contact (IBC) solar cells have been fabricated, cost considerations have limited commercialization of the IBC solar cell. Heretofore, conventional microelectronics (integrated circuit) processing has been employed in

fabricating IBC solar cells, including the use of backside diffusions, contacts, and metal lines fabricated by conventional microelectronics photolithography, thin film metallization, and etching processes. This fabrication process is capable of producing high efficiency solar cells, but the process is not cost effective for application in conventional low-cost, flat-plate solar panels. The key problem with practical realization of an IBC solar cell by this process is the high cost of fabrication, including etching, doping and mask alignment, and the use of thick metal conductor deposition by vacuum evaporation or sputtering. Further, the processing must be carried out in a clean room environment. Thus IBC solar cells fabricated using these methods have been restricted to application in high concentration solar cells or in very high value one-sun applications.

[0005] Copending application serial no. 11/306,510 combines a semiconductor substrate with acceptor and donor polymer contacts to provide a solar cell which is economically fabricated. Importantly, fabrication of the solar cell, is improved in cost and in reduced temperature cycling through use of inkjet application of the polymer contacts without the need for photoresist masking, etching, and dopant diffusion and annealing as is required in prior art solar cells.

[0006] The present invention utilizes a semiconductor such as amorphous silicon as donor and acceptor contact in a silicon solar sell which can be readily and cost effectively fabricated.

SUMMARY OF THE INVENTION

[0007] The invention utilizes doped amorphous silicon, Si-Ge, or III - V compounds as a donor or an acceptor contact in silicon solar cell. The contact material can be vapor deposited along with the dopant as necessary for donor or acceptor application. As used herein, "amorphous" silicon includes "poly crystalline" silicon.

[0008] When deposited on a single crystal silicon substrate, a tunnel oxide is first grown and separates a deposited amorphous silicon from the substrate to prevent re-crystallization of the amorphous silicon.

[0009] In an interdigitated back contact (IBC) cell, the front surface can be textured by chemical or physical abrasion to provide a radiation capturing surface with an anti-reflective and passivating coating such as silicon nitride, doped silicon carbide, or a thin coating of amorphous silicon over the textured surface.

[0010] The invention and object and features thereof will be more readily apparent from the following detailed description and appended claims when taken with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Fig. 1 is a side view in section of an interdigitated back contact solar cell including doped amorphous contact in accordance with one embodiment of the invention.

[0012] Figs 2A - 2D are side views in section illustrating the solar cell of Fig. 1 during fabrication.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0013] In accordance with one embodiment of the invention, an interdigitated back contact (IBC) solar cell comprising a silicon semiconductor body having first and second opposing major surfaces receives radiation through the first surface and has first and second patterns of acceptor doped amorphous silicon and donor doped amorphous silicon, respectively, on the second or back surface for receiving electron and hole carriers created in the silicon substrate by radiated photons. The structure is similar to prior art back contact solar cells which utilize doped P and N conductivity contacts formed in the substrates for receiving the holes and electrons created by radiation. However, the use doped P and N contacts in the substrate requires photoresist masking, etching, dopant diffusion, and high temperature processing in the fabrication of the solar cell. The use of acceptor and donor amorphous silicon contacts on the structure, in accordance with an embodiment of the invention, obviates the need for photoresist masking and dopant diffusion and the high temperature processing required in annealing the diffused dopants. A tunnel silicon oxide can be placed between the contacts and the substrate to prevent epitaxial growth of the amorphous silicon on the substrate.

[0014] Consider now Fig. 1 which is a side view in section of an interdigitated back contact (IBC) solar cell in accordance with one embodiment of the invention. The cell includes a light n-type monocrystalline or polycrystalline substrate 10 having a front surface which receives radiation and a textured surface on which is formed a thin (e.g. 10-150 angstrom) tunnel silicon oxide layer 12 with a passivation coating 14 over tunnel oxide 12 which can comprise silicon nitride, doped silicon carbide, or a doped amorphous silicon layer.

[0015] On the back surface of substrate 10 is a second tunnel oxide layer 16 over which is formed P+ amorphous silicon contacts 18. A dielectric such as silicon oxide 20 separates P+ amorphous silicon 18 from N+ amorphous silicon 22 which is formed in openings through P+ amorphous silicon layer 18 and in contact with tunnel oxide 16. While the amorphous silicon layers 18, 22 are formed by low temperature vapor deposition, tunnel oxide 16 prevents any re-crystallization of the amorphous silicon by epitaxial growth from silicon substrate 10. Metal contact 24 engages P+

amorphous silicon layer 18, and metal contacts 26 engage N+ amorphous silicon layers 22.

[0016] The back contact heterojunction enhances the rear passivation of the solar cell by the inclusion of tunnel oxide 16, heterojunction field provided by the amorphous silicon contacts, and contact passivation. As will be described further herein below, a process benefit in making the device is that high temperature dopant drive is not required.

[0017] Figs. 2A-2D are section views illustrating the solar cell of Fig. 1 during fabrication. Initially, as shown in Fig. 2A, silicon substrate 10, which can be either intrinsic or light doped, has a thin tunnel oxide 16 grown thereon which can have a thickness of from 10-20 angstrom, for example. Amorphous silicon layer 18 is then deposited with a boron dopant and a dopant concentration of 10^{20}-10^{21} or 10E20 - 10E21 atoms per cubic centimeter and to a thickness of 500 to 2000 angstroms. The growth of a doped silicon layer by vapor deposition is a known silicon process. Inclusion of an intrinsic layer under the p-type doped silicon layer can be made if a PIN structure is desired.

[0018] Thereafter, an insulating layer of silicon oxide 20 is deposited by low pressure chemical vapor deposition (LPCVD, PECVD, APCVD), or by a spin on glass process. Silicon oxide layer 16 is 500 to 1000 angstroms in this illustrative embodiment.

[0019] Thereafter, as illustrated in Fig. 2B, the front surface of substrate 10 is textured by chemical or mechanical abrasion. This process step can precede the process steps of Fig. 2A, if desired. A photoresist mask is then formed on the back surface of the substrate 10 and etched to form openings through silicon oxide layer 20 and amorphous silicon 18 to substrate 10. The thin tunnel oxide is removed in the etching process also, and a new layer of tunnel silicon oxide is then applied on the exposed surface of substrate 10 through the etched openings by chemical growth. In forming tunnel oxide 16 in Fig. 2B, tunnel oxide layer 12 can be simultaneously formed on the front surface. Following the growth of the thin tunnel oxide in the etched openings, again to a thickness of 10-20 angstroms, an N+ doped amorphous silicon layer 22 is deposited over the back surface, as shown in Fig. 2C.

[0020] The layer 22 is doped with an N dopant such as phosphorous with a concentration of 10^{20}-10^{21} or 10E20 -10E21 atoms per cubic centimeter. This can be deposited using plasma enhanced chemical vapor deposition (PECVD, LPCVD, APCVD). N+ amorphous silicon 22 is then masked and selectively etched to expose the underlying P+ amorphous silicon 18 for reception of metal contacts. In Fig. 2D, metal contacts 24 and 26 are made to P+ amorphous silicon 18 and N+ amorphous silicon 22 by metal deposition and photoresist masking and etching. The contacts can be formed by first scattering a seed layer of a conductive metal such as aluminum or copper and then pattern plating the seed metal to increase thickness. The cell is then completed by depositing a passivating layer 14 on tunnel oxide 12 on the front surface of substrate 10 using silicon nitride, doped silicon carbide, or N+ doped amorphous silicon.

[0021] A heterojunction solar cell in accordance with the invention, using doped amorphous silicon contacts is readily fabricated using conventional semiconductor processing techniques without the for high temperature processing. While the invention has been described with reference to an interdigitated back contact solar cell in which both P+ and N+ contacts are employed, the invention can be applied to solar cells having a single doped amorphous silicon on the back surface. Further, while the heterojunction is provided by amorphous silicon, other high band gap material such as germanium-silicon alloy, doped silicon carbide, or other III-V compound material can be employed in the contact structures. Thus, while the invention has been described with reference to specific embodiments, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications and applications may occur to those skilled in the art without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS

What is claimed is:

1. A solar cell comprising:

a) a semiconductor body having first and second opposing major surfaces,

b) a first dielectric layer on the first surface and a second dielectric layer on the second surface, the second dielectric layer comprising a tunnel oxide,

c) a first pattern of acceptor doped semiconductor material over the tunnel oxide on the second surface, and a second pattern of donor doped semiconductor material over the tunnel oxide on the second surface and interleaved with the first pattern, and

d) a first conductive pattern interconnecting the acceptor doped semiconductor material and a second conductive pattern interconnecting the donor doped semiconductor material.

2. The solar cell as defined by claim 1 wherein the semiconductor material is selected from the group consisting of amorphous silicon, silicon-germanium, and III - V compound semiconductors.

3. The solar cell as defined by claim 2 wherein the semiconductor material comprises amorphous silicon.

4. The solar cell as defined by claim 3 wherein the acceptor doped amorphous silicon is boron doped.

5. The solar cell as defined by claim 4 wherein the donor doped amorphous silicon is phosphorous doped.

6 The solar cell as defined by claim 5 wherein the first major surface is textured.

7. The solar cell as defined by claim 6 wherein the semiconductor body comprises silicon and the tunnel oxide comprises silicon oxide.

8. The solar cell as defined by claim 7 wherein the first and second conductive patterns are selected from the group consisting of aluminum and copper.

9. The solar cell as defined by claim 3 wherein the semiconductor body comprises silicon and the tunnel oxide comprises silicon oxide.

10. The solar cell as defined by claim 9 wherein the first and second conductive patterns are selected from the group consisting of aluminum and copper.

11. In a silicon solar cell in which mobile carriers can be created in a silicon substrate by impinging radiation, a contact for receiving mobile carriers comprising a tunnel oxide on a surface of the substrate, and a doped semiconductor material layer on the tunnel oxide.

12. The contact as defined by claim 11 wherein the semiconductor material is selected from the group consisting of amorphous silicon, silicon-germanium, and III - V compounds semiconductors.

13. The contact as defined by claim 12 wherein the semiconductor material comprises amorphous silicon.

14. The contact as defined by claim 13 wherein the tunnel oxide comprises silicon oxide.

15. The contact as defined by claim 14 wherein the silicon oxide has a thickness in the range of 10-20 angstroms.

16. The contact as defined by claim 14 wherein the amorphous silicon is doped with a donor dopant.

17. The contact as defined by claim 16 wherein the donor dopant is phosphorous.

18. The contact defined by claim 14 wherein the amorphous silicon is doped with an acceptor dopant.

19. The contact as defined by claim 18 wherein the acceptor dopant is boron.

20. In a method of fabricating a silicon solar cell, the steps of fabricating carrier acceptor contacts comprising:

a) providing a silicon substrate having first and second opposing major surfaces,

b) forming a tunnel silicon oxide layer on the first major surface, and

c) forming a doped amorphous silicon layer on the tunnel silicon oxide.

21. The method steps of claim 20 wherein the doped amorphous silicon has dopant in excess of 10^{19} atoms per cc.

22. The method steps of claim 21 wherein the dopant is a donor dopant.

23. The method steps of claim 22 wherein the dopant comprises phosphorus.

24. The method steps of claim 21 wherein the dopant is an acceptor dopant.

25. The method steps of claim 24 wherein the dopant comprises boron.

26. The method steps of claim 20 wherein the tunnel silicon oxide has a thickness on the order of 10-20 angstroms.

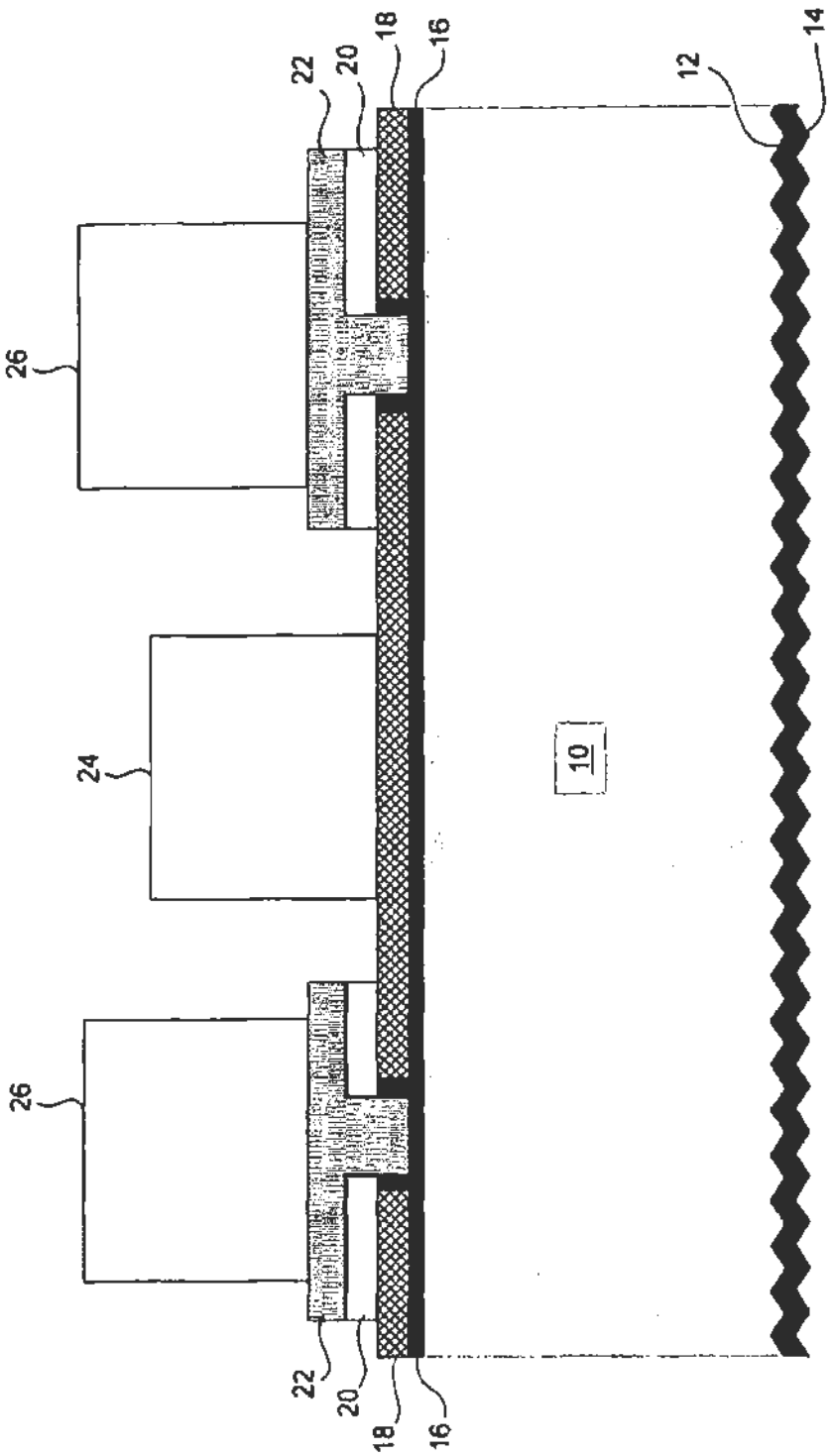


FIG. 1

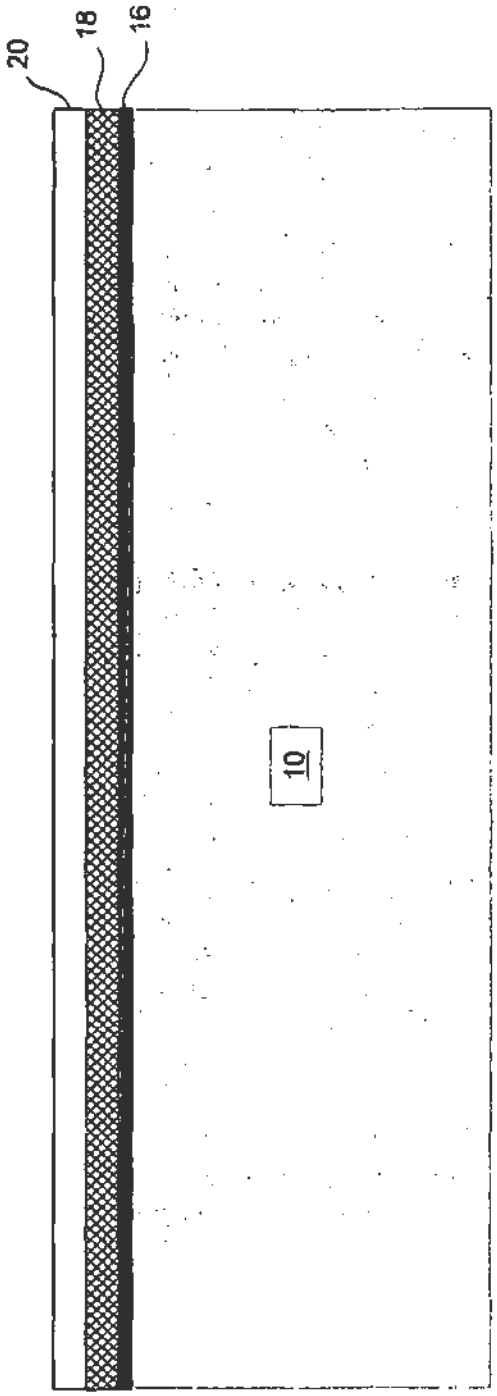


FIG. 2A

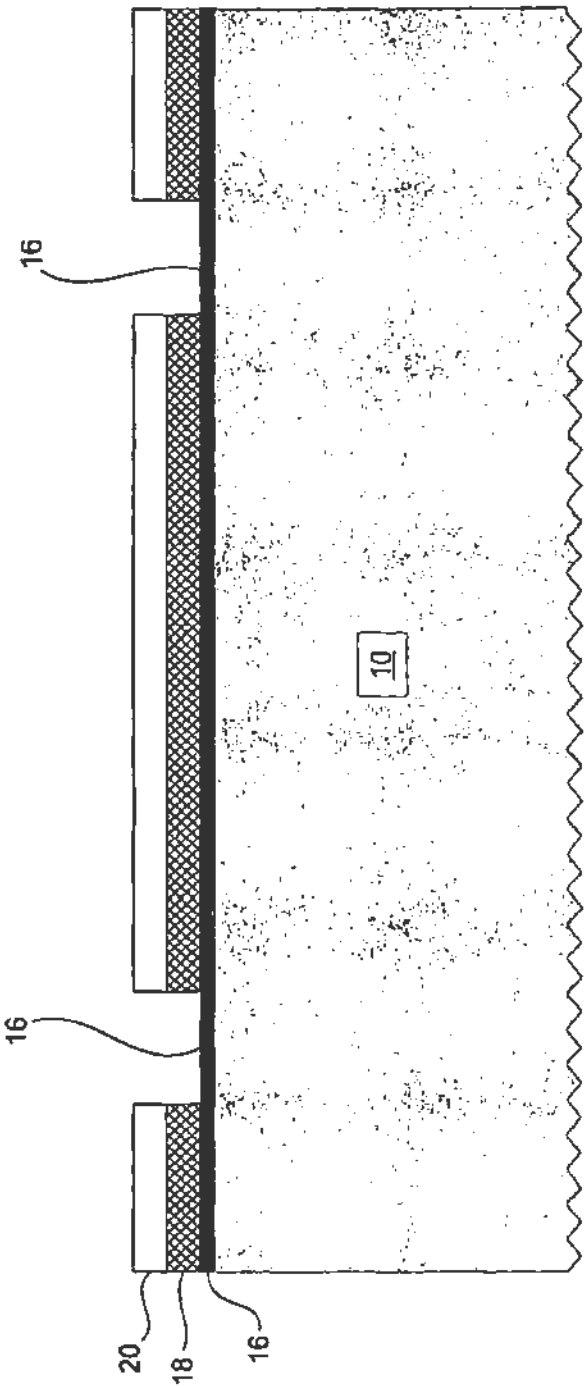


FIG. 2B

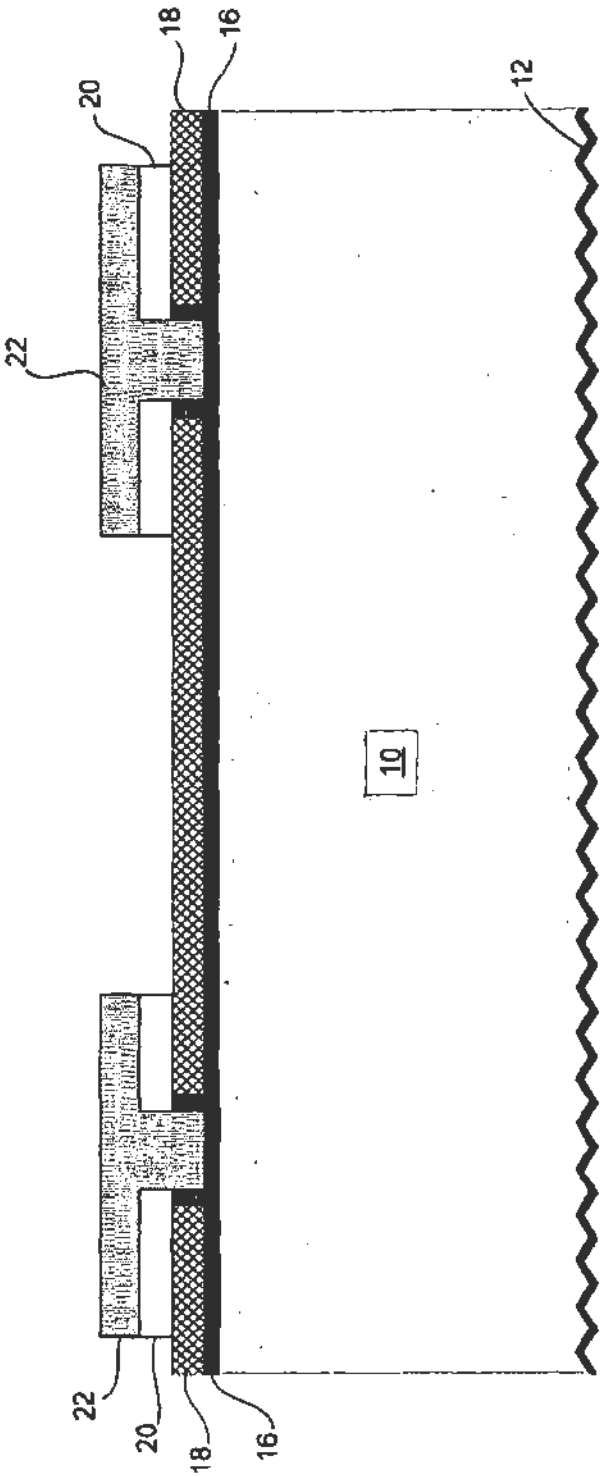


FIG. 2C

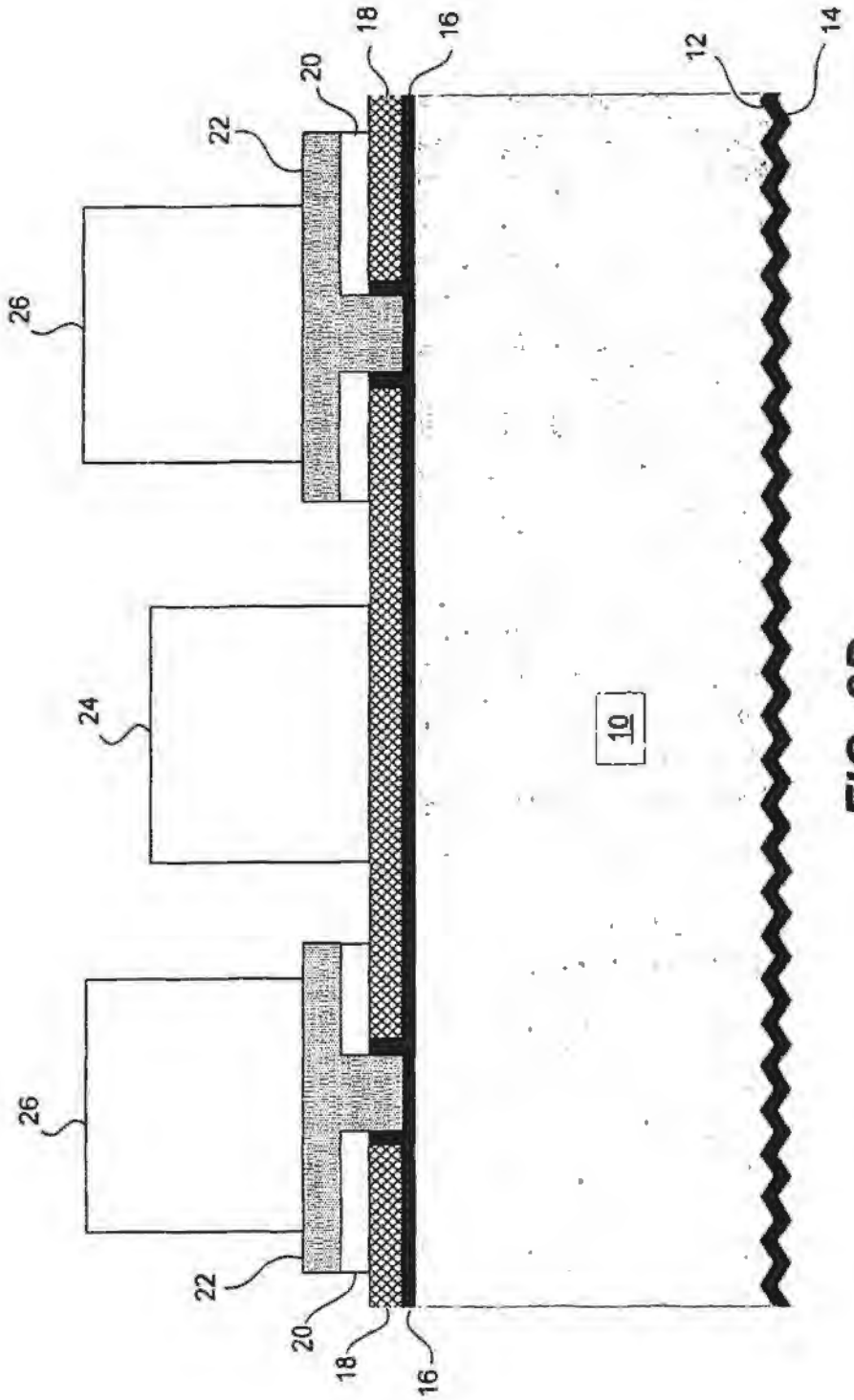


FIG. 2D

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Application Number	14504771
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First Named Inventor	Peter John COUSINS
Art Unit	1757
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	1	R. KOPECEK, ET AL "Large-Area Screen Printed N-Type Silicon Solar Cells with Rear Aluminum Emitter: Efficiencies Exceeding 16%", May 2006, pages 1044-1047, IEEE 4th World Conference on Photovoltaic Energy Conversion.	☐
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	4	J.Y. GAN, ET AL "Polysilicon Emitters for Silicon Concentrator Solar Cells", May 1990, pages 245-250, Proceedings of the 21st IEEE-PVSC.	☐
	5	The extended European Search Report for Application No. EP 09 71 3116, 22-Oct-2015 [22.10.15], 10 sheets.	☐

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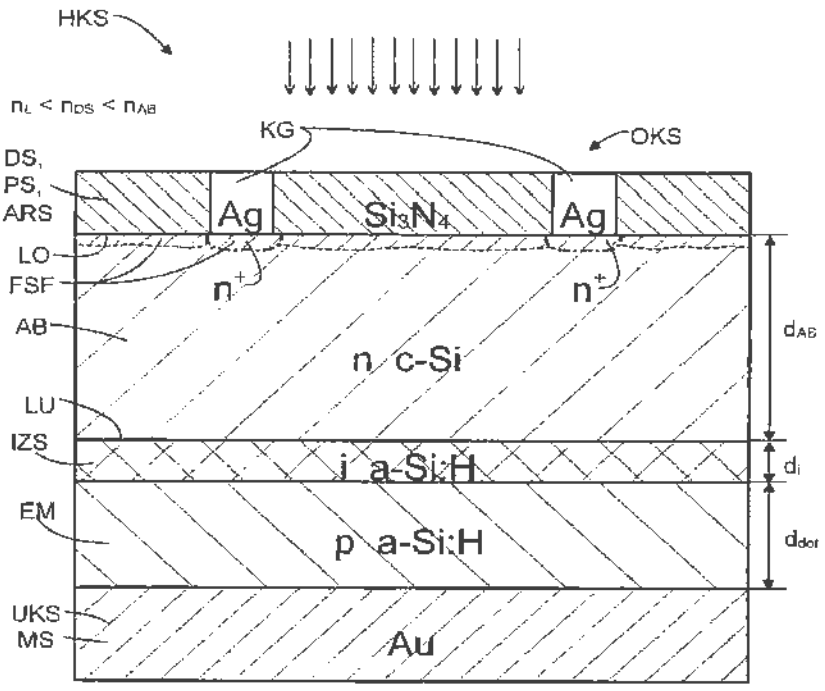
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(54) Title: HETEROCONTACT SOLAR CELL WITH INVERTED GEOMETRY OF ITS LAYER STRUCTURE

(54) Bezeichnung: HETEROKONTAKTSOLARZELLE MIT INVERTIERTER SCHICHTSTRUKTURGEOMETRIE



(57) Abstract: The amorphous emitter of known heterocontact solar cells is arranged on the top of the crystalline absorber facing the light and absorbs incident light which therefore cannot contribute to the generation of charge carriers in the absorber. A transparent conductive oxide layer (TCO) as the cover layer which has a negative effect on the pn transition, can be avoided. The inventive heterocontact solar cell (HKS) has an inverted geometry of its layer structure and thus an inverted heterocontact. The amorphous emitter (EM) is arranged on the bottom (LU) of the crystalline absorber (AB) facing away from the light. The absorber (AB) is only covered by a transparent antireflection coating (ARS) on its top (LO) facing the light, said coating, due to the material chosen, is at the same time the electrically effective passivation layer (PS), thereby avoiding absorption losses. The energy recuperation time regarding the material, time and energy requirements can be reduced by the low-temperature production of the emitter (EM) and the antireflection coating (ARS) by plasma CVD processes at 250 °C to 350 °C. The upper contact structure (OKS) penetrates the transparent antireflection coating (ARS) digitately, the lower contact structure (UKS) is configured as a thin large-surface metal layer (MS).

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GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), eurasisches (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), europäisches (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Veröffentlicht:

— *mit internationalem Recherchenbericht*

Zur Erklärung der Zweibuchstaben-Codes und der anderen Abkürzungen wird auf die Erklärungen ("Guidance Notes on Codes and Abbreviations") am Anfang jeder regulären Ausgabe der PCT-Gazette verwiesen.

(57) Zusammenfassung: Bei bekannten Heterokontaktsolarzellen ist der amorphe Emitter auf der lichtzugewandten Oberseite des kristallinen Absorbers angeordnet und absorbiert einfallendes Licht, das somit nicht mehr im Absorber zur Ladungsträgererzeugung beitragen kann. Eine transparente leitfähige Oxidschicht (TCO) als Deckschicht, die sich negativ auf den pn-Übergang auswirkt, kann vermieden werden. Die erfindungsgemäße Heterokontaktsolarzellen (HKS) weist eine invertierte Schichtstrukturgeometrie und damit einen invertierten Heterokontakt auf. Der amorphe Emitter (EM) ist auf der lichtabgewandten Unterseite (LU) des kristallinen Absorbers (AB) angeordnet. Der Absorber (AB) wird auf der lichtzugewandten Oberseite (LO) nur von einer transparenten Antireflexschicht (ARS) abgedeckt, die aufgrund ihrer Material wähl gleichzeitig als elektrisch wirkende Passivierungsschicht (PS) arbeitet. Somit werden die Absorptionsverluste minimiert. Die Energierücklaufzeit bezüglich Material-, Zeit- und Energieeinsatz kann durch die niedertemperierte Herstellung von Emitter (EM) und Antireflexschicht (ARS) durch Plasma-CVD-Prozesse bei 250°C bis 350°C verringert werden. Die obere Kontaktierungsstruktur (OKS) durchdringt die transparente Antireflexschicht (ARS) fingerförmig, die untere Kontaktierungsstruktur (UKS) ist großflächig als dünne Metallschicht (MS) ausgebildet.

Heterokontaktsolarzelle mit invertierter Schichtstrukturgeometrie

Beschreibung

Die Erfindung bezieht sich auf eine Heterokontaktsolarzelle in Schichtstruktur mit einem Absorber aus p- oder n-typ dotiertem kristallinem Halbleitermaterial, einem Emitter aus einem zum Absorber entgegengesetzt dotierten amorphen Halbleitermaterial, einer intrinsischen Zwischenschicht aus amorphem Halbleitermaterial zwischen Absorber und Emitter, einer Deckschicht auf der lichtzugewandten Seite des Absorbers, einer ein Minoritätsladungsträger reflektierendes Oberflächenfeld ausbildenden Schicht sowie mit einer ohmschen Kontaktierungsstruktur mit einer minimierten Beschattungsfläche auf der lichtzugewandten Seite des Absorbers und einer ohmschen Kontaktierungsstruktur auf der lichtabgewandten des Absorbers.

Stand der Technik

Heterokontaktsolarzellen mit kristallinem und amorphem Silizium gewinnen zunehmend an technischer Bedeutung. Der übliche Aufbau einer Heterokontaktsolarzelle ist beispielsweise aus der **Veröffentlichung I** von K. Brendel et al.: „Interface properties of a-Si:H/c-Si heterostructures" (Annual Report 2003, Hahn-Meitner-Institut, 78/79) bekannt. Auf der lichtzugewandten Seite des zentralen Absorbers aus kristallinem, p-dotierten Silizium (c-Si(p)) und mikrokristallinem Silizium (µc-Si) sind ein Emitter aus amorphem, mit Wasserstoff „legiertem" bzw. angereichertem, n-dotiertem amorphem Silizium (a-Si:H(n+)) und eine transparente leitfähige Oxidschicht (TCO) als Deckschicht unter fingerförmigen Frontkontakten angeordnet. Der Emitter auf der lichtzugewandten Oberseite des Absorbers absorbiert Strahlung, die den Absorber entsprechend nicht mehr erreichen kann. Auf der lichtabgewandten Unterseite

befindet sich zwischen dem Absorber und einem ganzflächigen Rückkontakt eine amorphe, mit Wasserstoff angereicherte p-hochdotierte amorphe Siliziumschicht (a-Si:H(p+)) zur Ausbildung eines Minoritätsladungsträger reflektierenden Oberflächenfeld (Back Surface Field BSF).

Wie bei jedem Solarzellentyp leidet auch die Heterokontaktsolarzelle mit bekannter Schichtstrukturgeometrie mit einer Positionierung des Emitters auf der lichtzugewandten Oberseite des Absorbers an Verlusten bei der Umwandlung der in die Solarzelle eindringenden Lichtenergie in elektrische Energie. Grundsätzlich zeigen amorphe Bereiche aufgrund ihrer ungeordneten Struktur schlechtere Transporteigenschaften für Ladungsträger als kristalline Bereiche. Ein Verlustprozess in der Umwandlungskette besteht darin, dass nicht alle Photonen der einfallenden Strahlung in einem „aktiven" Bereich der Solarzelle zu Elektronen-/Loch-Paaren gewandelt werden. Unter „aktivem Bereich" ist dabei diejenige Zone in der Solarzelle zu verstehen, in der die Elektronen und Löcher aufgrund hinreichend großer Lebensdauer gesammelt werden und nachfolgend über die ohmschen Kontaktierungssysteme abfließen können. Notwendige Voraussetzung für eine effizient arbeitende Solarzelle ist, dass ein möglichst großer Strahlungsanteil im aktiven Bereich absorbiert wird. Bei Heterokontaktsolarzellen ist dieser aktive Bereich der Absorber aus kristallinem Silizium, während der hochdotierte Emitter aus amorphem Silizium, durch den das Licht in den Absorber einfällt, dem entgegen als „inaktiver Bereich" zu bezeichnen ist, weil die in dieser Schicht erzeugten Elektronen und Löcher nur eine vergleichsweise geringe Lebensdauer haben und daher kaum eingesammelt werden können. Durch den hohen Absorptionskoeffizienten des amorphen Emittermaterials wird ein erheblicher Anteil des auftreffenden Sonnenlichts im Emitter absorbiert.

Zur Verringerung der genannten Verlustprozesse bei Heterokontaktsolarzellen mit einer konventionellen Schichtstrukturgeometrie mit einem Emitter auf der lichtzugewandten Oberseite des Absorbers ist es aus der **EP 1 187 223 A2**, von der die Erfindung als nächstliegendem Stand der Technik ausgeht, für die

so genannte „HIT"-Solarzelle (Heterojunction with Intrinsic Thin-layer) der Firma Sanyo bekannt, entweder die Dicke des Emitters aus hochdotiertem amorphem Silizium zu verringern, wobei eine Mindestschichtdicke von 5 nm zur vollständigen Ausbildung des pn-Heterokontaktes eingehalten werden muss, oder die Lichtabsorption im Emitter durch eine Vergrößerung der Bandlücke zu reduzieren. Dazu wird das amorphe Silizium des Emitters mit Kohlenstoff legiert. Die in der **EP 1 187 223 A2** offenbarte gattungsgemäße Heterokontakt-solarzelle weist eine Schichtstruktur mit einem n-typ dotierten kristallinen Siliziumwafer in der Mitte als Absorber auf. Auf beiden Seiten des Absorbers ist ein Heterokontakt zu benachbarten amorphen Siliziumschichten aufgebaut. Auf der lichtzugewandten Seite des Absorbers sind zwei intrinsische Zwischenschichten, der amorphe Emitter und eine transparente leitfähige Elektrode (ITO) als Deckschicht vorgesehen. Auf der lichtabgewandten Seite des Absor-bers sind vor einer sammelnden Rückelektrode zur Ausbildung eines BSF zumindest zwei weitere amorphe Schichten vorgesehen, von denen die eine undotiert und die andere wie der Absorber n-typ, jedoch stark dotiert ist. Auf beiden Seiten weist die Heterokontaktsolarzelle gitterförmige Kontaktierungssysteme auf den Ladungsträger sammelnden ITO-Schichten auf.

Somit weist auch die bekannte HIT-Solarzelle eine transparente Leitschicht (TCO, ITO) auf der lichtzugewandten Oberseite auf, um die im schlechter leitenden, amorphen Emitter gesammelten Ladungen abzuführen. Der **Veröffentlichung II** von A.G. Ulyashin et al.: "The influence of the amorphous silicon deposition temperature on the efficiency of the ITO/a-Si:H/c-Si Heterojunction (HJ) solar cells and properties of interfaces" (Thin Solid Films 403-404 (2002) 259-362) ist zu entnehmen, dass die Abscheidung dieser transparenten Leitschicht auf dem amorphen Emitter im Verdacht steht, die elektronischen Eigenschaften an der Grenzfläche zwischen amorphem und kristallinem Silizium (Emitter/Absorber) zu verschlechtern.

Weiterhin ist aus der **DE 100 45 249 A1** eine kristalline Solarzelle bekannt, bei der der kristalline Emitter auf der lichtabgewandten Seite des Absorbers angeordnet ist. Dort ist er streifenförmig unter Anwendung eines Herstellungsprozesses bei hoher Temperatur ausgebildet und wird mit kristallinen Streifen gegensätzlicher Dotierung verschachtelt, die ein BSF ausbilden. Diese reinkristalline, interdigitale Halbleiterstruktur ist nur in einem sehr komplizierten Herstellungsprozess erzeugbar und dient der ausschließlichen Rückseitenkontaktierung, bei der beide ohmschen Kontaktierungsstrukturen auf der lichtabgewandten Unterseite der Solarzelle angeordnet und ebenfalls ineinander verschachtelt sind. Unterhalb der auf der lichtzugewandten Oberseite des Absorbers vorgesehenen Antireflexschicht, die in eine Verkapselung integriert ist, weist die bekannte Solarzelle noch eine zusätzliche Passivierungsschicht auf, die der Verringerung der Rekombination von lichterzeugten Ladungsträgern auf der Vorderseite der Solarzelle dient, jedoch auch zusätzlich Licht absorbiert. Weitere interdigitale Solarzellen sind auch aus der **US 4.927.770** mit sehr kleinen Emitterbereichen und aus der **US 2004/0200520 A1**, bei der größere Emitterbereiche in Gräben vorgesehen sind, bekannt. Bei beiden bekannten interdigitalen Solarzellen ist auf der lichtzugewandten Oberseite neben einer Passivierungsschicht und einer Antireflexschicht auch eine dotierte Frontschicht zur Ausbildung eines Minoritätsladungsträger reflektierenden Oberflächenfelds (Front Surface Field FSF) vorgesehen. Insbesondere die das Oberflächenfeld ausbildende Schicht wirkt, wenn es sich um eine stark dotierte Si-Schicht handelt, stark absorbierend und verringert damit den Lichteinfall in den aktiven Bereich der Solarzelle und die Ladungsträgerausbeute. Auf der lichtzugewandten Oberseite ist die Ausbildung eines FSF jedoch von besonderer Bedeutung, da hier durch den starken Lichteinfall eine hohe Ladungsträgererzeugung auftritt, deren Rekombination minimiert werden muss.

Aus der **DE 100 42 733 A1** ist eine ebenfalls reinkristalline Dünnschicht-Solarzelle mit einem transparenten Glassuperstrat auf der Lichteinfallsseite bekannt, die einen p-typ dotierten polykristallinen Absorber (p-pc-Si) mit einer Kontaktie-

rungsschicht zwischen dem Absorber und dem Glassuperstrat aus p-hochdotiertem polykristallinen Silizium (p^+-pc-Si), die gleichzeitig als transparente Elektrode und als Schicht zum Aufbau eines FSF dient, aufweist. Die Erzeugung des FSF und die Stromsammlung durch die transparente Elektrode auf der lichtzugewandten Seite werden jedoch auch hier mit Absorptionsverlusten im Eintrittsfenster erkauft. Eine Antireflexschicht auf der lichtzugewandten Seite ist nicht vorgesehen, deren Funktion muss von dem Glassuperstrat übernommen werden. Auf der lichtabgewandten Seite des Absorbers befindet sich direkt auf dem Absorber der Emitter aus n-hochdotiertem mikrokristallinem Silizium (n^+-µc-Si) mit einer rauen abgewandten Oberfläche, auf der eine Aluminiumschicht als rückreflektierender Kontaktschicht und Elektrode angeordnet ist.

Aufgabenstellung

Ausgehend von der gattungsgemäßen Heterokontaktsolarzelle, wie sie im Zusammenhang mit der HIT-Solarzelle oben näher beschrieben ist, besteht die **Aufgabe** für die vorliegende Erfindung darin, eine möglichst einfach herstellbare Schichtstrukturgeometrie für eine Heterokontaktsolarzelle mit geringen optischen Verlusten zu schaffen, die ohne eine transparent leitfähige Elektrode (TCO) auf der lichtzugewandten Seite auskommt und trotzdem eine zu bekannten Heterokontaktsolarzellen mit konventioneller Schichtstrukturgeometrie vergleichbare Umsetzungseffizienz bei der Gewinnung von elektrischem Strom aus Sonnenenergie liefert. Es soll eine möglichst kurze Energierücklaufzeit für die erzeugten Heterokontaktsolarzellen durch einen möglichst geringen Material-, Zeit- und vor allem Energieeinsatz bei einfacher und kostengünstiger Herstellungsweise erreicht werden. Die erfindungsgemäße **Lösung** für diese Aufgabe ist dem Hauptanspruch zu entnehmen. Vorteilhafte Modifikationen der Erfindung werden in den Unteransprüchen aufgezeigt und im Folgenden im Zusammenhang mit der Erfindung näher erläutert.

Die erfindungsgemäße Heterokontaktsolarzelle weist im grundsätzlichen Unterschied zu bekannten Heterokontaktsolarzellen eine invertierte Schichtstrukturgeometrie und damit einen invertierten Heterokontakt auf. Der amorphe Emitter ist auf der lichtabgewandten Unterseite des Absorbers angeordnet. Hinter dem Absorber ist die Intensität des einfallenden Lichts schon so stark verringert, dass in den Emitter kaum noch Strahlung eindringt und dort absorbiert wird, sodass die Absorptionsverluste gering gehalten werden können. Auf der lichtzugewandten Oberseite des Absorbers ist bei der erfindungsgemäßen Heterokontaktsolarzelle lediglich eine einzelne transparente Antireflexschicht mit verbesserten Antireflexeigenschaften als Deckschicht angeordnet, die aufgrund der Materialwahl gleichzeitig als elektrisch wirkende Passivierungsschicht eine Ladungsträgerrekombination durch Ausbildung eines Minoritätsladungsträger rückstreuenden Oberflächenfeldes (FSF) verhindert. Die Antireflexeigenschaften der Antireflex-schicht werden durch die Wahl ihres Materials bedingt, das einen Brechungsindex (n_{ARS}) aufweisen muss, der größer als der Brechungsindex von Luft(n_L), aber kleiner als der Brechungsindex des kristallinen Halbleitermaterials des Absorbers (n_{AB}) ist ($n_L<n_{ARS}<n_{AB}$). Durch die doppelte Funktion der Deckschicht als transparente Antireflexschicht und als Passivierungsschicht entfällt insbesondere eine transparent leitfähige Elektrode (TCO) auf der lichtzugewandten Seite, da deren Funktion der Stromableitung durc ein feines Kontaktgitter als oberes Konatkierungssystem übernommen werden kann. Außerdem entfallen weitere Schichten, insbesondere hochdotierte Si-FSF-Schichten und damit stark absorbierende Passivierungsschichten, und deren Präparation auf der Solarzellenoberseite. Durch den Wegfall zusätzlicher Deckschichten wird der Herstellungsaufwand bezüglich Material-, Zeit- und Energieeinsatz bei der Heterokontaktsolarzelle nach der Erfindung bedeutsam reduziert und vereinfacht.

Im Unterschied zu den bekannten interdigitalen kristallinen Solarzellen, die einen kristallinen, streifenförmigen Emitter auch auf der lichtabgewandten

Absorberseite aufweisen, ist der amorphe Emitter der erfindungsgemäßen Heterokontaktsolarzelle als durchgängige Schicht ausgebildet, sodass er einfacher herstellbar ist, effizient arbeitet und einfach kontaktiert werden kann. Darüber hinaus wird der Emitter bei der Heterokontaktsolarzelle nicht durch Eindiffusion der entsprechenden Dotierspezies bei Temperaturen über 900°C gebildet, sondern beispielsweise durch plasmagestütztes Abscheiden aus der Gasphase (PECVD) bei Substrattemperaturen von unter 250°C erzeugt.

Weiterhin können bei der erfindungsgemäßen Heterokontaktsolarzelle durch die Separation von transparenter Antireflexschicht und Emitter deren Schichtdicken unabhängig voneinander optimiert werden. So kann der Emitter auf der lichtabgewandten Unterseite des Absorbers in größerer Schichtdicke ausgeführt werden als auf dessen lichtzugewandter Oberseite, wodurch eine gute, stabile Raumladungszone erzeugt wird. Die elektronischen Eigenschaften der aktiven Grenzfläche zwischen Emitter und Absorber werden dadurch verbessert. Bei der Erzeugung der transparenten Antireflexschicht wiederum muss keine Rücksicht mehr auf darunter liegende Schichten und einen Einfluss auf deren elektronische Eigenschaften genommen werden.

Die im Absorber generierten Ladungsträger werden am Heterokontakt zwischen kristallinem Absorber und amorphen Emitter in der Raumladungszone getrennt und über die ohmschen Kontaktierungsstrukturen abgeführt. Dabei durchdringt die eine ohmsche Kontaktierungsstruktur auf der lichtzugewandten Oberseite des Absorbers, die mit einer minimierten Beschattungsfläche ausgebildet ist, die transparente Antireflexschicht. Die andere ohmsche Kontaktierungsstruktur ist großflächig auf dem Emitter auf der lichtabgewandten Unterseite des Absorbers ausgebildet. Vorteilhaft können auch unterhalb der die transparente Antireflexschicht durchdringenden Kontaktierungsstruktur im Absorber Ladungsträger reflektierende Zonen ausgebildet sein, sodass zusammen mit dem von der transparenten Antireflexschicht bewirkten Ladungsträger rückstreuenden Oberflächenfeld (FSF) auf der gesamten Oberfläche des Absorbers ein geschlossenes Oberflächenfeld

erzeugt wird. Es wird zur Kontaktierung des Emitters keine transparent leitfähige Oxidschicht (TCO : z.B. ITO) als Elektrode mehr benötigt, deren Abscheidung auf dem amorphen Emitter in Verdacht steht, die elektronischen Eigenschaften am Heteroübergang zu verschlechtern (s.o.). Diese technologische Schwierigkeit wird bei der Erfindung durch eine sanfte Metallisierung des amorphen Emitters, der eine gute großflächige Kontaktierung erlaubt, zur Erzeugung der großflächigen Kontaktierungsstruktur über beispielsweise thermische Verdampfung vermieden. Dabei kann die großflächige Kontaktierungsstruktur die gesamte Unterseite des Emitters überdecken oder durch Anwendung einer Maskentechnik größere Flächenbereiche davon.

Besonders günstig wirken sich die zuvor aufgeführten Vorteile auf die Heterokontaktsolarzelle nach der Erfindung mit invertiertem Heteroübergang aus, wenn der Absorber aus n-typ dotiertem kristallinem Silizium und der Emitter aus p-typ dotiertem amorphem Silizium mit einer intrinsischen, d.h. undotierten, amorphen Zwischenschicht bestehen. Bei einer derartigen Materialwahl kann ein technisch gut beherrschbarer, n-leitender Absorber aus Silizium mit sehr guten Transporteigenschaften und einer hohen Ladungsträgerlebensdauer, das mono-, multi- oder auch mikro-kristallin ausgebildet sein kann. Bei der Wahl eines solchen Materialsystems ist es möglich, die FSF-bildende Passivierungsschicht nicht – wie aus dem Stand der Technik bekannt - aus Siliziumoxid, sondern aus Siliziumnitrit zu erzeugen. Dessen optischer Brechungsindex liegt zwischen dem von Luft und Silizium, sodass die Passivierungsschicht gleichzeitig als gute transparente Antireflexschicht wirksam ist. Eine entsprechend doppeltfunktionelle transparente Antireflexschicht ist auch möglich, wenn der Absorber p-leitend dotiert ist. Der Brechungsindex des gewählten Materials muss wieder zwischen dem von Luft und Absorber liegen und das Material muss passivierend auf den Absorber einwirken. Weiterhin kann der Silizium-Absorber auf seiner lichtabgewandten Unterseite in einfacher Weise in einem Niedertemperaturprozess durch den Emitter aus amorphem Silizium passiviert werden, wodurch eine sehr geringe Grenzflächenrekombination bedingt wird, da offene Bindungen, so genannte

„dangling bonds" sehr effizient chemisch abgesättigt werden. Die Absättigung mit amorphem Silizium, dessen Bandlücke weit oberhalb der des kristallinen Siliziums liegt, ergibt einen sehr guten pn-Heterokontaktübergang. Das amorphe Silizium des Emitters hingegen zeigt starkes Absorptions- und Rekombinationsverhalten. Die Anordnung eines dünnen Emitters hinter dem aktiven Bereich ist somit optimal.

Weiterhin kann die eine ohmsche Kontaktierungsstruktur auf der lichtzugewandten Oberseite des Absorbers als Kontaktfinger oder -gitter aus Silber oder Aluminium und die andere ohmsche Kontaktierungsstruktur auf dem Emitter als dünne, flächige Metallschicht aus Gold oder einem anderen geeigneten Material ausgebildet sein. Beide Edelmetalle sind zwar relativ teuer, werden aber in so geringen Mengen verwendet, dass ihren sehr guten Leit- und Verarbeitungseigenschaften der Vorzug zu geben ist. Zudem ist bei großflächigen Strukturen eine Verdickung der Kontakte mit kostengünstigeren Metallen denkbar. Außerdem kann der Absorber als selbsttragender Wafer, insbesondere Siliziumwafer, in relativ großer Schichtdicke ausgeführt sein. Die Solarzelle nach der Erfindung kann aber auch in Dünnschichttechnik, d.h. mit einzelnen Schichten von Schichtdicken im nm- bis µm-Bereich, ausgeführt sein und durch ein Glassubstrat auf der lichtabgewandten Unterseite des Absorbers die erforderliche Stabilität erhalten. Weitere Anordnungen, Materialsysteme und Herstellungsprozesse können dem nachfolgenden speziellen Beschreibungsteil entnommen werden.

Ausführungsbeispiele

Ausbildungsformen der Heterokontaktsolarzelle mit invertierter Schichtstrukturgeometrie nach der Erfindung werden nachfolgend anhand der schematischen Figuren näher erläutert. Dabei zeigt :

Figur 1 einen Schichtstrukturquerschnitt durch die Heterokontaktsolarzelle,

Figur 2 ein Diagramm mit einer Dunkel- und Hellkennlinie einer hergestellten Heterokontaktsolarzelle und

Figur 3 ein Diagramm zur spektralen Quantenausbeute der Heterokontaktsolarzelle gemäß **Figur 2**.

Die **Figur 1** zeigt eine Heterokontaktsolarzelle **HKS** mit einem Absorber **AB**, in dessen lichtzugewandter Oberseite **LO** Lichtstrahlung (natürlich oder künstlich, sichtbar und/oder unsichtbar) einfällt (Pfeile). Der Absorber **AB** besteht aus einem selbsttragenden Wafer der Schichtdicke d_{AB} aus n-typ dotiertem kristallinem Silizium **n c-Si**. Dabei kann das verwendete Silizium mono-, poly-, multi- oder mikrokristallin ausgebildet und entsprechend hergestellt sein.

Auf der lichtzugewandten Oberseite **LO** des Absorbers **AB** ist als Deckschicht **DS** eine transparente Antireflexschicht **ARS** aus Siliziumnitrit Si_3N_4 angeordnet, die gleichzeitig als Passivierungsschicht **PS** auf dem Absorber **AB** wirkt und ein Ladungsträger rückstreuendes Oberflächenfeld **FSF** (in **Figur 1** gestrichelt dargestellt) ausbildet zur Vermeidung von Ladungsträger-rekombination auf der Lichteinfallsseite. Die Doppelfunktion der Deckschicht **DS** ergibt sich durch deren Materialwahl in Abhängigkeit vom Absorbermaterial. Die Antireflexeigenschaften der transparente Antireflexschicht werden durch die Wahl ihres optischen Brechungsindex n_{ARS} zwischen dem Brechungsindex n_L von Luft und dem Brechungsindex n_{AB} des Absorbermaterials bedingt ($n_L<n_{ARS}<n_{AB}$). Die Passivierungseigenschaften hängen von der elektrischen Wirkung des gewählten Materials auf die Absorberoberfläche ab. Durch die einzige Deckschicht **DS** auf dem Absorber **AB** werden die Photonenverluste durch Absorption gegenüber einem konventionellen Heterokontaktsolarzellenaufbau mit einer Anordnung des Emitters **EM** auf der lichtzugewandten Oberseite **LO** des Absorbers **AB** erheblich reduziert. Außerdem besteht beim Aufbau der transparenten

Antireflexschicht **ARS** keine Gefahr, die darunter liegende Schichten und deren elektronische Eigenschaften zu stören.

Bei der Heterokontaktsolarzelle **HKS** mit invertierter Schichtstrukturgeometrie ist der Emitter **EM** auf der lichtabgewandten Unterseite **LU** des Absorbers **AB** angeordnet. Im gewählten Ausführungsbeispiel besteht der Emitter **EM** aus mit Wasserstoff **H** angereichertem amorphem Silizium mit einer p-typ Dotierung **p a-Si:H**. Aufgrund seiner invertierten Positionierung hinter dem Absorber **AB** kann der Emitter **EM** kein Licht absorbieren und somit in seiner Schichtdicke d_{dot} individuell, insbesondere auch ausreichend dick, bemessen werden. Da die Beweglichkeit der Ladungsträger in amorphem Silizium sehr viel geringer ist als in kristallinen Silizium, darf d_{dot} aber auch nicht zu dick sein. Somit kann d_{dot} im Hinblick auf einen geringen Serienwiderstand der Heterokontaktsolarzelle **HKS** optimiert werden. Eine sehr dünne intrinsische (nicht dotierte) Zwischenschicht **IZS** mit der Schichtstärke d_i zwischen Absorber **AB** und Emitter **EM** ist im gewählten Ausführungsbeispiel aus amorphem Silizium **i a-Si:H** ausgebildet.

Die Heterokontaktsolarzelle **HKS** mit invertierter Schichtstrukturgeometrie weist auf ihrer lichtzugewandten Oberseite eine obere Kontaktierungsstruktur **OKS** auf, die so ausgelegt ist, dass sie den Absorber **AB** mit nur einer minimalen Fläche abschattet, sodass ein maximaler Lichteinfall möglich ist. Dazu kann die Kontaktierungsstruktur **OKS** finger- oder gitterförmig ausgebildet sein. Im gewählten Ausführungsbeispiel wird die obere Kontaktierungsstruktur **OKS** von einem Kontaktgitter **KG** aus Silber **Ag** gebildet. Im Bereich des Kontaktgitters **KG** wird die transparente Antireflexschicht **AR** durchdrungen, sodass direkt unter den Kontaktfingern zunächst kein Minoritätsladungsträger reflektierendes Oberflächenfeld **FSF** ausgebildet ist. Bei der Erzeugung des Kontaktgitters **KG** können aber Maßnahmen (s.u.) ergriffen werden, die zu einer im gewählten Ausführungsbeispiel hoch n-dotierten n^+ Einlagerung unterhalb des Kontaktgitters **KG** im Absorber **AB** führen, sodass auch hier ein Minoritätsladungs-

träger reflektierendes Oberflächenfeld **FSF** (in **Figur 1** strichpunktiert dargestellt) ausgebildet wird. Somit kann die gesamte Oberfläche des Absorbers **AB** passiviert werden.

Auf der Unterseite des Emitters **EM** befindet sich eine untere Kontaktierungsstruktur **UKS**, welche nicht dem Lichteinfall ausgesetzt ist. Folglich muss sie in ihrer Beschattungsfläche auch nicht minimiert sein, sondern kann den schlecht leitenden amorphen Emitter **EM** möglichst großflächig zur Sammlung der getrennten Ladungsträger kontaktieren. Im gewählten Ausführungsbeispiel ist die untere Kontaktierungsstruktur **UKS** als dünne flächige Metallschicht **MS** aus Gold **Au** ausgebildet.

Die in der **Figur 1** dargestellte Heterokontaktsolarzelle **HKS** mit invertierter Schichtstrukturgeometrie kann beispielsweise nach folgendem Ablauf hergestellt werden. Andere Herstellungsverfahren sind jedoch ebenfalls anwendbar.

Auf einen absorbergroßen Abschnitt eines 0,7 bis 1,5 Ωcm n-dotierten Silizium-Wafers zur Bildung des Absorbers **AB** der Schichtdicke d_{AB} werden nach bekannter Standardrezeptur Wasserstoff (**H**)-terminierte Oberflächen nasschemisch präpariert. Auf die präparierte Oberfläche wird anschließend bei 325°C bis 345°C mittels Plasma-CVD eine etwa 70 nm dicke Schicht Siliziumnitrit Si_3N_4 als transparente Antireflexschicht **ARS** abgeschieden. Diese kann anschließend von dem durch Siebdruck einer kommerziell erhältlichen Silberleitpaste mit Phosphorquelle aufgebrachte Kontaktgitter **KG** bei 600°C bis 800°C durchdrungen (Durchfeuern der Kontakte durch die transparente Antireflexschicht **ARS**) werden. Dabei entstehen unterhalb des Kontaktgitters **KG** durch das lokale Eindiffundieren des Phosphors stark n-dotierte Bereiche n^+, die als Minoritätsladungsträger reflektierendes Oberflächenfeld **FSF** die Rekombination der lichtgenerierten Ladungsträger reduzieren und das Minoritätsladungsträger reflektierendes Oberflächenfeld **FSF** von der transparenten

Antireflexschicht **ARS** im Bereich des Kontaktgitters **KG** schließen. Alternativ kann die transparente Antireflexschicht **ARS** beispielsweise mit photolithographischen Schritten partiell geöffnet werden, um das Silizium des Absorbers **AB** auf der lichtzugewandten Oberseite **LO** mit aufgedampftem Aluminium als Kontaktgitter **KG** ohmsch zu kontaktieren.

Auf der lichtabgewandten Unterseite **LU** des Absorbers **AB** wird dann nach einem Ätzreinigungsschritt dieser Oberfläche in verdünnter Flusssäure ebenso mit Plasmadeposition amorphes Silizium als Emitter **EM** der Solarzelle **SZ** abgeschieden. Dies erfolgt in zwei Etappen : Zunächst wird eine wenige nm dünne intrinsische Zwischenschicht **IS** der Schichtdicke d_i undotiertes Silizium (**i a-Si:H**) aufgewachsen und anschließend eine mit etwa 10000 ppm Bor dotierte 20 nm - 40 nm dicke (Schichtdicke d_{dot}) Emitterschicht (**p a-Si:H**) aufgebracht.

Der Emitter **EM** wird auf der lichtabgewandten Unterseite **LU** im nächsten Schritt durch Aufdampfen einer etwa 150 nm dicken Metallschicht **MS** aus Gold **Au** metallisiert und auf diese Weise die untere Kontaktierungsstruktur **UKS** gebildet, wobei deren laterale Ausdehnung durch Verwendung verschieden großer Masken festgelegt werden kann.

Alternativ hierzu kann bei Raumtemperatur eine manuelle Präparation der oberen Kontaktierungsstruktur **OKS** auf der transparenten Antireflexschicht **ARS** durch partielles Fortätzen der transparenten Antireflexschicht **ARS** aus Si_3N_4, durch die Benetzung dieser freigelegten Stellen mit Galliumindium-Eutektikum GaIn und deren anschließendes Verkapseln mit silberhaltigen Leitklebern erfolgen.

Erste nach dem vorbeschrieben Verfahren hergestellte Heterokontaktsolarzellen **HKS** mit invertierter Schichtstrukturgeometrie gemäß **Figur 1** zeigen einen Wirkungsgrad von über 11,05 % auf (**Figur 2**, Diagramm mit einer

Dunkel- und Hellkennlinie, Stromdichte **SD** in A/cm² über dem Potenzial **P** in V) bei einer für kristallines Silizium typischen externen spektralen Quantenausbeute (**Figur 3**, Diagramm spektrale Quantenausbeute für die Solarzelle gemäß **Figur 2**, externe Quantenausbeute **eQA** über der Wellenlänge λ in nm). Der durch den relativ hohen Serienwiderstand begrenzte Wirkungsgrad ist durch eine Optimierung der oberen Kontaktierungsstruktur **OKS** noch deutlich steigerbar.

Bezugszeichenliste

AB	Absorber
ARS	transparente Antireflexschicht
d_{AB}	Schichtdicke Absorber
d_{dot}	Schichtdicke dotierter Emitter
d_i	Schichtstärke intrinsische Zwischenschicht
DS	Deckschicht
EM	Emitter
FSF	Minoritätsladungsträger reflektierendes Oberflächenfeld
HKS	heterogene Heterokontaktsolarzelle
IZS	intrinsische Zwischenschicht
i a-Si:H	intrinsisches amorphes Silizium
KG	Kontaktgitter
LO	lichtzugewandte Oberseite
LU	lichtabgewandte Unterseite
MS	Metallschicht
n_{AB}	optischer Brechungsindex Absorber
n_{ARS}	optischer Brechungsindex Antireflexschicht
n c-Si	n-typ dotiertes kristallines Silizium.
n_L	optischer Brechungsindex Luft
OKS	obere Kontaktierungsstruktur
p a-Si:H	p-typ dotiertes amorphes Silizium
P	Potenzial
PS	Passivierungsschicht
eQA	externe Quantenausbeute
SD	Stromdichte
UKS	untere Kontaktierungsstruktur

Patentansprüche

1. Heterokontaktsolarzelle in Schichtstruktur mit einem Absorber aus p- oder n-typ dotiertem kristallinem Halbleitermaterial, einem Emitter aus einem zum Absorber entgegengesetzt dotierten amorphen Halbleitermaterial, einer intrinsischen Zwischenschicht aus amorphem Halbleitermaterial zwischen Absorber und Emitter, einer Deckschicht auf der lichtzugewandten Seite des Absorbers, einer ein Minoritätsladungsträger reflektierendes Oberflächenfeld ausbildenden Schicht sowie mit einer ohmschen Kontaktierungsstruktur mit einer minimierten Beschattungsfläche auf der lichtzugewandten Seite des Absorbers und einer ohmschen Kontaktierungsstruktur auf der lichtabgewandten des Absorbers,
dadurch gekennzeichnet, dass
in einer invertierten Schichtstrukturgeometrie der Emitter (EM) auf der lichtabgewandten Unterseite (LU) des Absorbers (AB) angeordnet ist, dass die Deckschicht (DS) auf der lichtzugewandten Seite des Absorbers (AB) durch eine Materialwahl in Abhängigkeit vom Absorbermaterial sowohl als transparente Antireflexschicht (ARS) als auch als eine ein Minoritätsladungsträger - reflektierendes Oberflächenfeld (FSF) ausbildende Passivierungsschicht (PS) des Absorbers (AB) ausgebildet ist und dass die ohmsche Kontaktierungsstruktur (OKS) auf der lichtzugewandten Oberseite (LO) des Absorbers (AB) die transparente Antireflexschicht (ARS) durchdringt und die andere ohmsche Kontaktierungsstruktur (UKS) großflächig auf dem Emitter (EM) auf der lichtabgewandten Unterseite (LU) des Absorbers (AB) ausgebildet ist.

2. Solarzelle nach Anspruch 1,
dadurch gekennzeichnet, dass
unterhalb der die transparente Antireflexschicht (ARS) durchdringenden Kontaktierungsstruktur (OKS) im Absorber (AB) Ladungsträger reflektierende Bereiche (n^+) ausgebildet sind.

3. Solarzelle nach Anspruch 1 oder 2,
dadurch gekennzeichnet, dass
der Absorber (AB) aus n-typ dotiertem kristallinem Silizium (n c-Si), der Emitter (EM) aus p-typ dotiertem amorphem Silizium (p a-Si:H) und die intrinsische Zwischenschicht (IZS) aus undotiertem amorphem Silizium (i a-Si:H) bestehen.

4. Solarzelle nach einem der Ansprüche 1 bis 3,
dadurch gekennzeichnet, dass
die transparente Antireflexschicht (ARS) aus Siliziumnitrit (Si_3N_4) besteht.

5. Solarzelle nach einem der Ansprüche 1 bis 4,
dadurch gekennzeichnet, dass
die eine ohmsche Kontaktierungsstruktur (OKS) auf der lichtzugewandten Oberseite (LO) des Absorbers (AB) als Kontaktfinger oder –gitter (KG) aus Silber (Ag) und die andere ohmsche Kontaktierungsstruktur (UKS) als dünne flächige Metallschicht (MS) aus Gold (Au) ausgebildet ist.

6. Solarzelle nach einem der Ansprüche 1 bis 5,
dadurch gekennzeichnet, dass
der Absorber (AB) aus einem selbsttragenden Wafer besteht.

7. Solarzelle nach einem der Ansprüche 1 bis 6,
dadurch gekennzeichnet, dass
ein Dünnschichtaufbau für die Schichten der Solarzelle (SZ) und ein tragendes Glassubstrat auf der lichtabgewandten Unterseite (LU) des Absorbers (AB) vorgesehen sind.

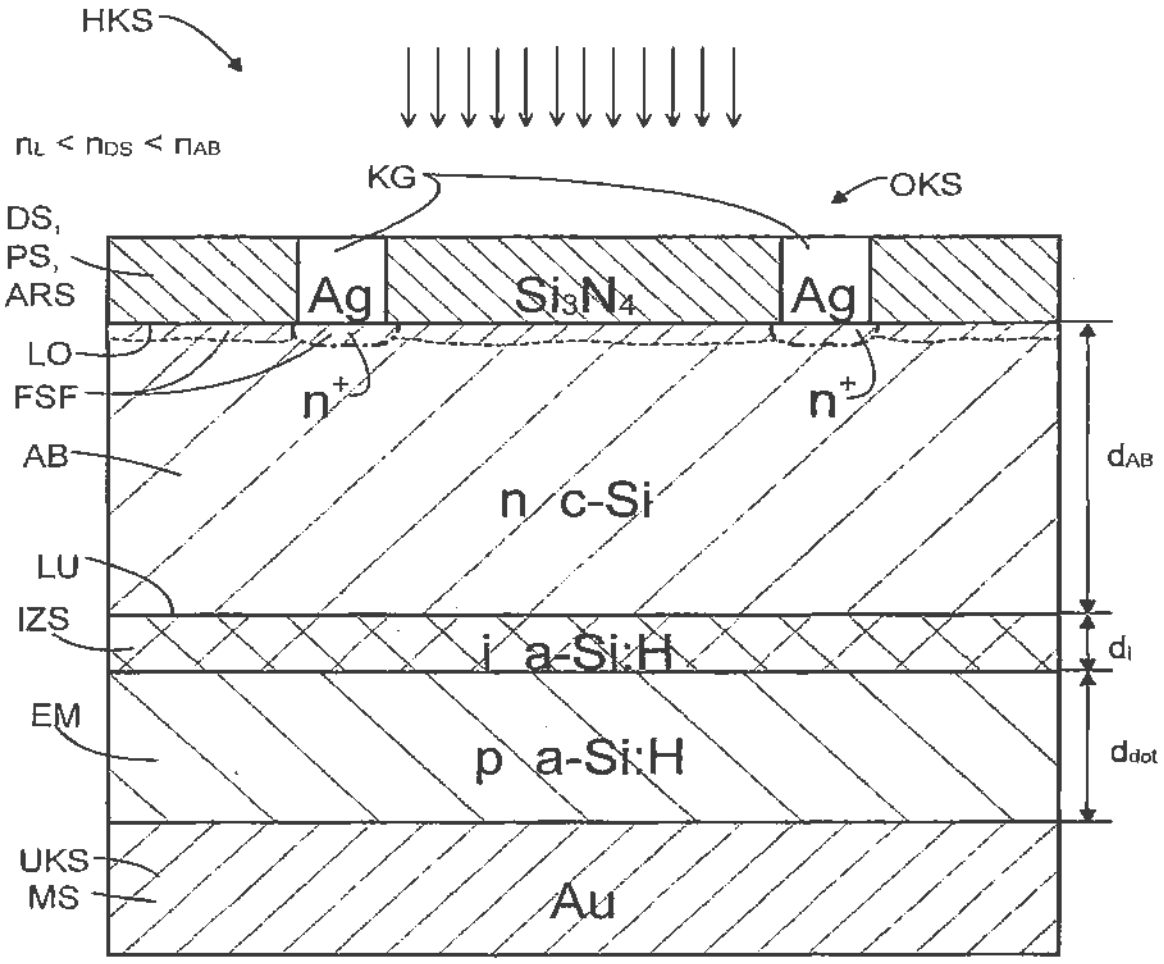

HKS
$n_L < n_{DS} < n_{AB}$
KG
OKS
DS,
PS,
ARS
Ag
Si_3N_4
Ag
LO
FSF
n^+
n^+
AB
n c-Si
LU
IZS
i a-Si:H
EM
p a-Si:H
UKS
MS
Au
d_{AB}
d_I
d_{dot}

Fig.1

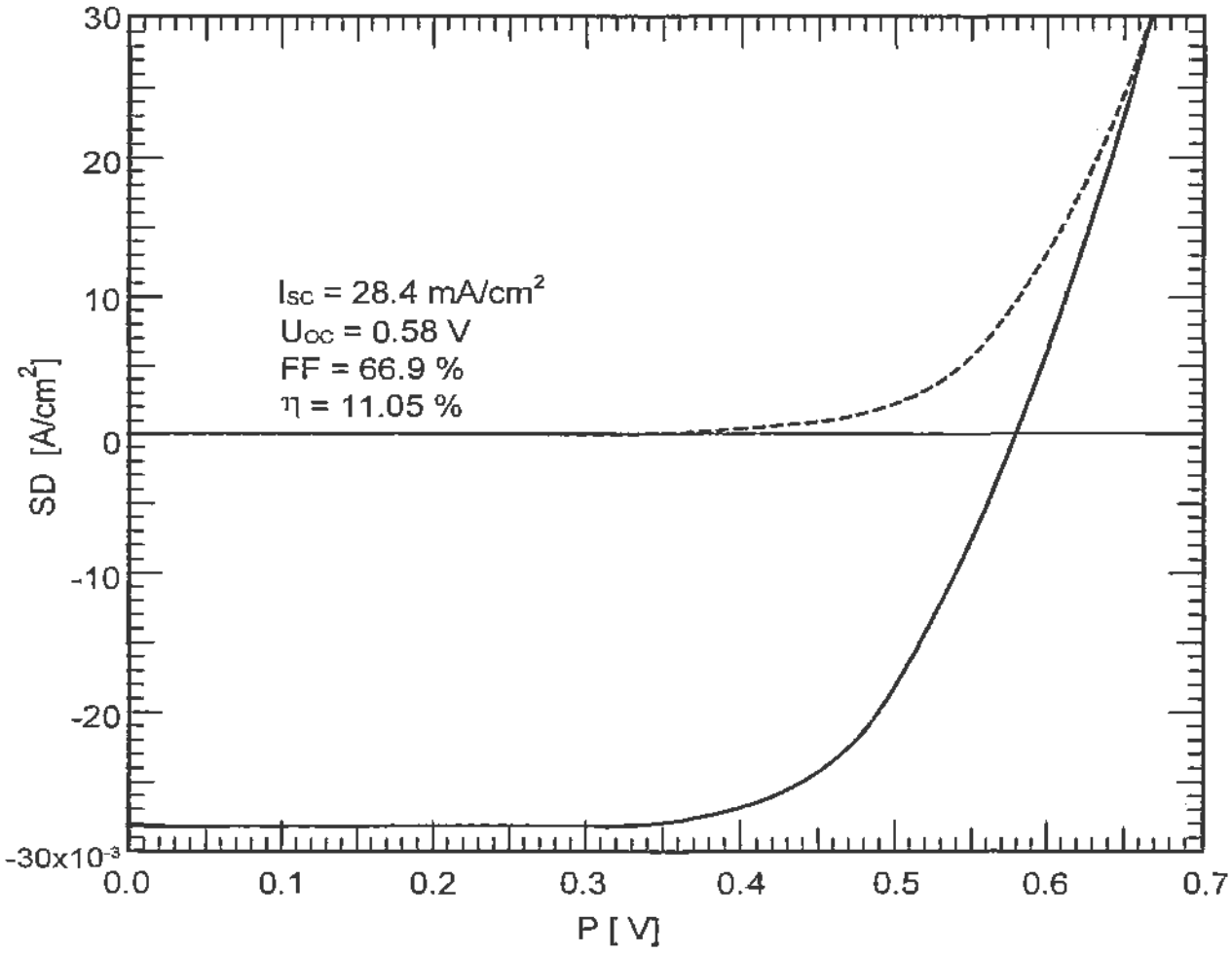

30
20
10
0
-10
-20
-30x10-3
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
SD [A/cm2]
P [V]
Isc = 28.4 mA/cm2
Uoc = 0.58 V
FF = 66.9 %
η = 11.05 %

Fig.2

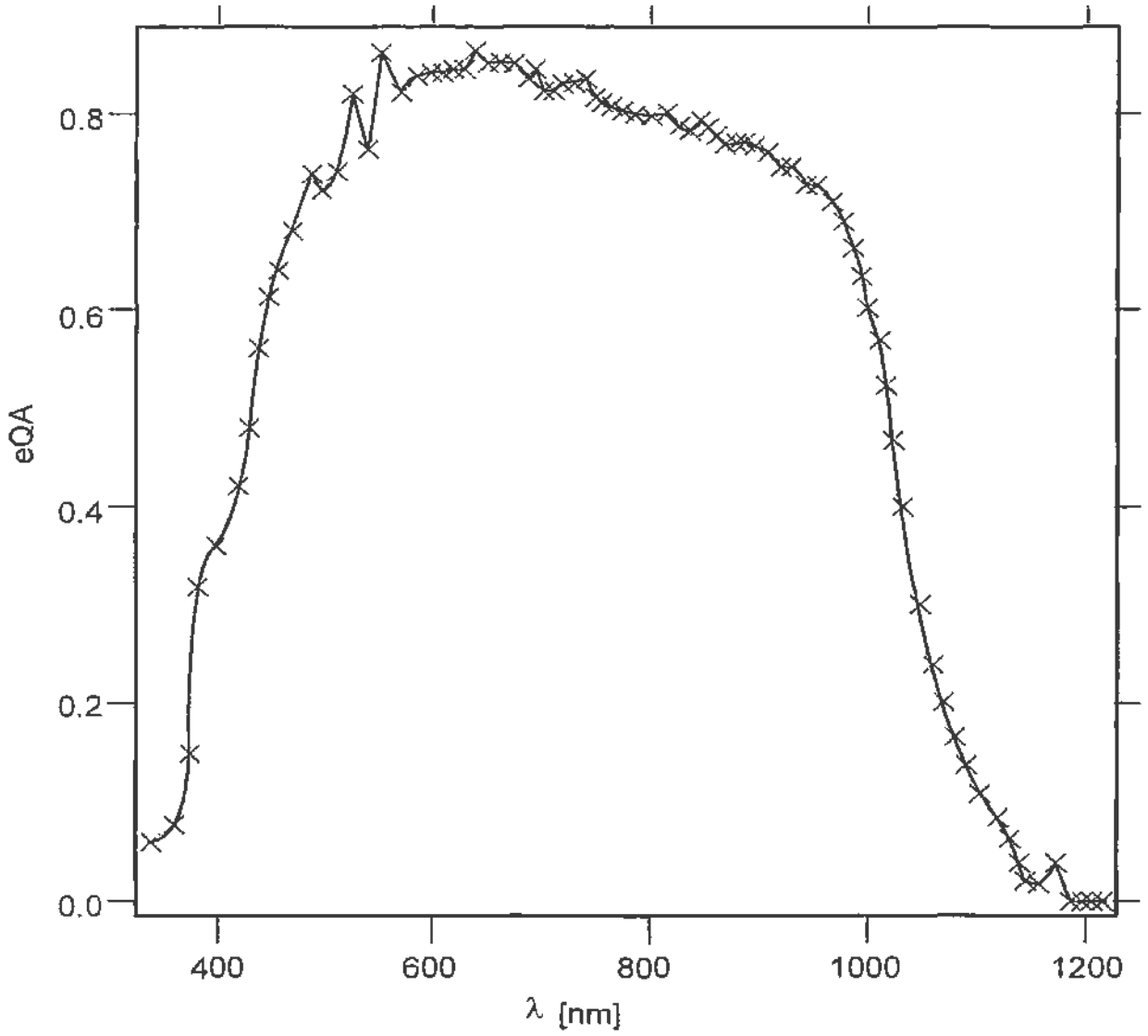


Fig.3

INTERNATIONAL SEARCH REPORT

International application No
PCT/DE2006/000670

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L31/075

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 4 620 058 A (WINTERLING ET AL) 28 October 1986 (1986-10-28) column 1, line 47 - column 2, line 58; figures 3-5 column 3, line 6 - column 5, line 18	1,2,7 3-6
Y	EP 1 519 422 A (SANYO ELECTRIC CO., LTD) 30 March 2005 (2005-03-30) paragraph [0062] - paragraph [0158]; figures 2-13	3-6
A	US 4 498 092 A (YAMAZAKI ET AL) 5 February 1985 (1985-02-05) column 5, line 11 - column 7, line 68; figures 1,3,5,6 column 11, line 35 - column 15, line 7	1-7

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 August 2006	11/08/2006

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Boero, M

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/DE2006/000670

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Information on patent family members

International application No
PCT/DE2006/000670

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EP 1519422	A	30-03-2005	CN	1601759 A	30-03-2005
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US 4498092	A	05-02-1985	AU	537887 B2	19-07-1984
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INTERNATIONALER RECHERCHENBERICHT

Internationales Aktenzeichen
PCT/DE2006/000670

A. KLASSIFIZIERUNG DES ANMELDUNGSGEGENSTANDES
INV. H01L31/075

Nach der Internationalen Patentklassifikation (IPC) oder nach der nationalen Klassifikation und der IPC

B. RECHERCHIERTE GEBIETE

Recherchierter Mindestprüfstoff (Klassifikationssystem und Klassifikationssymbole)
H01L

Recherchierte, aber nicht zum Mindestprüfstoff gehörende Veröffentlichungen, soweit diese unter die recherchierten Gebiete fallen

Während der internationalen Recherche konsultierte elektronische Datenbank (Name der Datenbank und evtl. verwendete Suchbegriffe)
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C. ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie*	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
X Y	US 4 620 058 A (WINTERLING ET AL) 28. Oktober 1986 (1986-10-28) Spalte 1, Zeile 47 - Spalte 2, Zeile 58; Abbildungen 3-5 Spalte 3, Zeile 6 - Spalte 5, Zeile 18	1,2,7 3-6
Y	EP 1 519 422 A (SANYO ELECTRIC CO., LTD) 30. März 2005 (2005-03-30) Absatz [0062] - Absatz [0158]; Abbildungen 2-13	3-6
A	US 4 498 092 A (YAMAZAKI ET AL) 5. Februar 1985 (1985-02-05) Spalte 5, Zeile 11 - Spalte 7, Zeile 68; Abbildungen 1,3,5,6 Spalte 11, Zeile 35 - Spalte 15, Zeile 7	1-7

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[X] Weitere Veröffentlichungen sind der Fortsetzung von Feld C zu entnehmen [X] Siehe Anhang Patentfamilie

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Datum des Abschlusses der internationalen Recherche	Absendedatum des internationalen Recherchenberichts
4. August 2006	11/08/2006

Name und Postanschrift der internationalen Recherchenbehörde	Bevollmächtigter Bediensteter
Europäisches Patentamt, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Boero, M

Formblatt PCT/ISA/210 (Blatt 2) (April 2005)

INTERNATIONALER RECHERCHENBERICHT

Internationales Aktenzeichen
PCT/DE2006/000670

C. (Fortsetzung) ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie*	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
A	EP 0 500 067 A (CANON KABUSHIKI KAISHA) 26. August 1992 (1992-08-26) das ganze Dokument	1-7

INTERNATIONALER RECHERCHENBERICHT

Angaben zu Veröffentlichungen, die zur selben Patentfamilie gehören

Internationales Aktenzeichen
PCT/0E2006/000670

Im Recherchenbericht angeführtes Patentdokument		Datum der Veröffentlichung	Mitglied(er) der Patentfamilie		Datum der Veröffentlichung
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EP 0500067	A	26-08-1992	DE	69211724 D1	01-08-1996
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			JP	4266D66 A	22-09-1992
			US	5279681 A	18-01-1994



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/504,771	10/02/2014	Peter John COUSINS	10031.004211	3342

74254 7590 03/21/2016

Okamoto & Benedicto LLP
P.O. Box 641330
San Jose, CA 95164-1330

EXAMINER
PILLAY, DEVINA

ART UNIT	PAPER NUMBER
1755	

MAIL DATE	DELIVERY MODE
03/21/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/504,771	Applicant(s) COUSINS, PETER JOHN	
	Examiner DEVINA PILLAY	Art Unit 1755	AIA (First Inventor to File) Status No

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1-20*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-20* are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-14, drawn to a solar cell, classified in H01L31/022425.

II. Claims 15-20, drawn to a method of fabricating a solar cell, classified in H01L31/182.

The inventions are distinct, each from the other because of the following reasons:

3. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process. For example, the substrate can be formed on the first tunnel dielectric.

4. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention.**

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after

the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

5. The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be

maintained. Withdrawn process claims that are not commensurate in scope with an allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEVINA PILLAY whose telephone number is (571)270-1180. The examiner can normally be reached on Monday thru Friday 7:30am -5:00pm (EST). Examiner Fax Number is (571)-270-2180.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey T. Barton can be reached on 571-272-1307. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DEVINA PILLAY/
Primary Examiner, Art Unit 1755

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14504771	COUSINS, PETER JOHN
	Examiner	Art Unit
	DEVINA PILLAY	1755

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/17/2016								
	1	÷								
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	3	÷								
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S0123 US2 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.:	14/504,771	Confirm. No. 3342
Applicant:	Peter John Cousins	Art Unit: 1755
Filed:	October 2, 2014	Examiner: Devina Pillay
Docket No.:	10031.004211	Customer No.: 74254

Title: FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

RESPONSE TO MARCH 21, 2016 RESTRICTION REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the March 21, 2016 Restriction Requirement, Applicants respectfully submit the following response.

REMARKS

Claims 1-20 are pending in the present application.

Restriction Requirement

A restriction requirement under 35 U.S.C. 121 was made in the latest Office Action to one of the following two groups of claims:

I. Claims 1-14, drawn to a solar cell, classified in H01L31/022425.

II. Claims 15-20, drawn to a method of fabricating a solar cell, classified in H01L31/182.

In reply to this requirement, Applicants elect Group I, encompassing claims 1-14 for examination. This election is made without traverse.

Conclusion

The Examiner is invited to call the undersigned for any questions. Favorable action is respectfully solicited.

Respectfully submitted,

Dated: MAY 6, 2016

Patrick Benedicto

Patrick D. Benedicto, Reg. No. 40,909
OKAMOTO & BENEDICTO LLP
P.O. Box 641330
San Jose, California 95164
(408) 436-2110

Electronic Acknowledgement Receipt

EFS ID:	25704826
Application Number:	14504771
International Application Number:	
Confirmation Number:	3342
Title of Invention:	FRONT CONTACT SOLAR CELL WITH FORMED EMITTER
First Named Inventor/Applicant Name:	Peter John COUSINS
Customer Number:	74254
Filer:	Patrick D. Benedicto/jina mangaoang
Filer Authorized By:	Patrick D. Benedicto
Attorney Docket Number:	10031.004211
Receipt Date:	06-MAY-2016
Filing Date:	02-OCT-2014
Time Stamp:	12:51:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	S0123US2_RRRmailed21Mar2016.pdf	68366 60d33d1c9a849dad47e3f4eg7e5edd2e0da8891a	no	2

Warnings:	
Information:	

Total Files Size (in bytes):	68366

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/504,771	10/02/2014	Peter John COUSINS	10031.004211	3342

74254 7590 06/29/2016

Okamoto & Benedicto LLP
P.O. Box 641330
San Jose, CA 95164-1330

EXAMINER
PILLAY, DEVINA

ART UNIT	PAPER NUMBER
1755	

MAIL DATE	DELIVERY MODE
06/29/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/504,771	Applicant(s) COUSINS, PETER JOHN	
	Examiner DEVINA PILLAY	Art Unit 1755	AIA (First Inventor to File) Status No

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05/06/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application

5a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-14* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *10/29/2015 06/11/2015*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

2. Claims 15-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected method of fabricating a solar cell, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 05/06/2016.

3. Applicant's election without traverse of claims 1-14, drawn to a solar cell, in the reply filed on 05/06/2016 is acknowledged.

Claim Rejections - 35 USC § 112

4. The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 9-14 rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

6. Claim 9 recites "a back surface" in line 3 and later recites "a back surface" in line 6. It is unclear if these are the same back surfaces or not. Further clarification and appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. This application currently names joint inventors. In considering patentability of the claims under pre-AIA 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of pre-AIA 35 U.S.C. 103(c) and potential pre-AIA 35 U.S.C. 102(e), (f) or (g) prior art under pre-AIA 35 U.S.C. 103(a).

10. Claims 1-14 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Okayasu (JP 07-106611, Machine Translation) in view of Ohmi (US 5,563,092) in further view of Foglietti (US 2002/0142500 A1).

Regarding claims 1-6, Okayasu discloses a solar cell (See Fig. 1), comprising:

a substrate (1);

an emitter (2) disposed over the substrate:

a front electrode (either 4 or 6) disposed over a front surface (top or bottom surface) of the substrate; and a back electrode (6 or 4) disposed over a back surface (bottom or top) of the substrate ([0044]).

However, Okayasu does not discloses a tunneling dielectric oxide between the emitter and the substrate.

Ohmi discloses that that when growing an amorphous silicon layer on a monocrystalline substrate a thin tunneling oxide layer is placed between so that crystalline growth is suppressed (C1/L20-25, C3/L50-55 and C4/L5-65) which is applicable to solar cells (C2/L20-23).

Foglietti discloses that polycrystalline growth directly on crystalline silicon results in partial realignment of the polycrystalline grains and to suppress this effect a thin oxide can be grown similar to that disclosed by Ohmi ([0046]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the solar cell of Okayasu by providing a thin tunneling oxide between the emitter layer (2, formed of polysilicon or amorphous silicon) and the substrate (1 formed of single crystalline silicon) and the BSF layer (5 polysilicon layer or

amorphous layer) and the substrate (1 formed of single crystalline silicon) because as disclosed by Ohmi and Foglietti it suppresses realignment of polysilicon emitter and BSF layers.

Regarding claim 7, modified Okayasu discloses all of the claim limitations as set forth above.

In addition, Okayasu discloses that the back electrode (4) includes silver [0044].

Regarding claim 8, modified Okayasu discloses all of the claim limitations as set forth above.

In addition, Okayasu discloses that there is an anti-reflection layer (3 [0044]) disposed over the front surface (top) of the substrate.

Regarding claims 9-13, Okayasu discloses a solar cell (See Fig. 1), comprising:

a substrate (1);

an emitter (2) disposed over a back surface (top surface) of the substrate;

a front electrode (6) disposed over a front surface (bottom surface) of the substrate;

and a back electrode (4) disposed over the back surface (top) of the substrate ([0044]).

However, Okayasu does not discloses a tunneling dielectric oxide between the emitter and the substrate.

bottom or top) of the substrate ([0044]).

However, Okayasu does not discloses a tunneling dielectric oxide between the emitter and the substrate.

Ohmi discloses that that when growing an amorphous silicon layer on a monocrystalline substrate a thin tunneling oxide layer is placed between so that crystalline growth is suppressed (C1/L20-25, C3/L50-55 and C4/L5-65) which is applicable to solar cells (C2/L20-23).

Foglietti discloses that polycrystalline growth directly on crystalline silicon results in partial realignment of the polycrystalline grains and to suppress this effect a thin oxide can be grown similar to that disclosed by Ohmi ([0046]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the solar cell of Okayasu by providing a thin tunneling oxide between the emitter layer (2, formed of polysilicon or amorphous silicon) and the substrate (1 formed of single crystalline silicon) and the BSF layer (5 polysilicon layer or amorphous layer) and the substrate (1 formed of single crystalline silicon) because as disclosed by Ohmi and Foglietti it suppresses realignment of polysilicon emitter and BSF layers.

Regarding claim 14, modified Okayasu discloses all of the claim limitations as set forth above.

In addition, Okayasu discloses that the back electrode (4) includes silver [0044].

11. Claims 1-14 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Okayasu (JP 07-106611, Machine Translation) in view of Borden (WO 2009/094578 A2, please note provisional filing date).

Regarding claims 1-6, Okayasu discloses a solar cell (See Fig. 1), comprising:

a substrate (1);

an emitter (2) disposed over the substrate:

a front electrode (either 4 or 6) disposed over a front surface (top or bottom surface) of the substrate; and a back electrode (6 or 4) disposed over a back surface (bottom or top) of the substrate ([0044]).

However, Okayasu does not discloses a tunneling dielectric oxide between the emitter and the substrate.

Borden discloses that tunnel oxides can be used in solar cells between doped polysilicon and monocrystalline substrates [0016].

Furthermore, Borden discloses that by providing the tunneling layer it prevents epitaxial growth of the emitter layer and further it protects the surface from plasma damage of the deposited emitter layer [0008].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the interface between polycrystalline layers and monocrystalline substrates of Okayasu by having a tunneling oxide because it prevents epitaxial growth of the emitter layer and further it protects the crystalline surface from plasma damage of the deposited emitter layer.

Regarding claim 7, modified Okayasu discloses all of the claim limitations as set forth above.

In addition, Okayasu discloses that the back electrode (4) includes silver [0044].

Regarding claim 8, modified Okayasu discloses all of the claim limitations as set forth above.

In addition, Okayasu discloses that there is an anti-reflection layer (3 [0044]) disposed over the front surface (top) of the substrate.

Regarding claims 9-13, Okayasu discloses a solar cell (See Fig. 1), comprising:

a substrate (1);

an emitter (2) disposed over a back surface (top surface) of the substrate;

a front electrode (6) disposed over a front surface surface) of the substrate;

and a back electrode (4) disposed over the back surface (bottom or top) of the substrate ([0044]).

However, Okayasu does not discloses a tunneling dielectric oxide between the emitter and the substrate.

Borden discloses that tunnel oxides can be used in solar cells between doped polysilicon and monocrystalline substrates [0016].

Furthermore, Borden discloses that by providing the tunneling layer it prevents epitaxial growth of the emitter layer and further it protects the surface from plasma damage of the deposited emitter layer [0008].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the interface between polycrystalline layers and monocrystalline substrates of Okayasu by having a tunneling oxide because it prevents epitaxial growth of the emitter layer and further it protects the crystalline surface from plasma damage of the deposited emitter layer.

Regarding claim 14, modified Okayasu discloses all of the claim limitations as set forth above.

In addition, Okayasu discloses that the back electrode (4) includes silver [0044].

Double Patenting

12. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg,* 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for

applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/forms/. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

13. Claims 1-14 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-11 of U.S. Patent No. **8,207,444**. Although the claims at issue are not identical, they are not patentably distinct from each other because they discloses a similar solar cell with a backside polysilicon emitter and tunnel oxide at the interfaces between the monocrystalline substrate and the emitter and the monocrystalline substrate and the front side electrode.

14. Claims 1-14 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-12 of U.S. Patent No. **8,222,516**. Although the claims at issue are not identical, they are not patentably distinct from each other because they discloses a similar solar cell with a backside polysilicon emitter and tunnel oxide at the interfaces between the monocrystalline substrate and the emitter and the monocrystalline substrate and the front side electrode.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEVINA PILLAY whose telephone number is (571)270-1180. The examiner can normally be reached on Monday thru Friday 7:30am -5:00pm (EST). Examiner Fax Number is (571)-270-2180.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey T. Barton can be reached on 571-272-1307. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DEVINA PILLAY/
Primary Examiner, Art Unit 1755

Notice of References Cited	Application/Control No. 14/504 771	Applicant(s)/Patent Under Reexamination COUSINS, PETER JOHN	
	Examiner DEVINA PILLAY	Art Unit 1755	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-5,563,092 A	10-1996	Ohmi; Kazuaki	H01L21/02381	118/723E
*	B	US-2002/0142500 A1	10-2002	Foglietti, Pietro	H01L21/02052	438/22
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N	JP 07106611	04-1995	Japan	Okayasu	H01 L 31/04
	O	WO2009/094578 A2	07-2009	United States	Borden	H 01 L 31/0745
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	JP07-106611, Machine Translation, Okayasu
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Receipt date: 10/29/2015 14504771 - GAU: 1755

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14504771
Filing Date	2014-10-02
First Named Inventor	Peter John COUSINS
Art Unit	1757
Examiner Name	
Attorney Docket Number	10031.004211

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5057439		1991-10-15	Swanson, et al.	

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	1	20030183270		2003-10-02	Falk, et al.	

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	1	2006/111138	WO	A1	2006-10-26	HAHN-MEITNER-INSTITUT BERLIN GMBH		☐

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First Named Inventor	Peter John COUSINS
Art Unit	1757
Examiner Name	
Attorney Docket Number	10031.004211

	1	R. KOPECEK, ET AL "Large-Area Screen Printed N-Type Silicon Solar Cells with Rear Aluminum Emitter: Efficiencies Exceeding 16%", May 2006, pages 1044-1047, IEEE 4th World Conference on Photovoltaic Energy Conversion.	☐
	2	JIANHUA ZHAO, ET AL "High Efficiency Rear Emitter Pert Solar Cells on N-Type EZ Single Crystalline Silicon Substrate", June 2005, pages 806-809, Proceedings of the 20th European Photovoltaic Solar Energy Conference.	☐
	3	N. GARRY TARR "A Polysilicon Emitter Solar Cell", December 1985, pages 655-658, IEEE Electron Device Letters, Vol. 6, NO. 12.	☐
	4	J.Y. GAN, ET AL "Polysilicon Emitters for Silicon Concentrator Solar Cells", May 1990, pages 245-250, Proceedings of the 21st IEEE-PVSC.	☐
	5	The extended European Search Report for Application No. EP 09 71 3116, 22-Oct-2015 [22.10.15], 10 sheets.	☐

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OR

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Patrick D. Benedicto/	Date (YYYY-MM-DD)	2015-10-29
Name/Print	PATRICK D. BENEDICTO	Registration Number	40909

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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CONFIRMATION NO. 3342

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/504,771	10/02/2014 RULE	136	1755	10031.004211

APPLICANTS
SunPower Corporation, San Jose, CA;

INVENTORS
Peter John COUSINS, Menlo Park, CA;

**** CONTINUING DATA ***************************
This application is a CON of 13/495,577 06/13/2012 PAT 8878053
which is a DIV of 12/070,742 02/20/2008 PAT 8222516

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
10/07/2014

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /DEVINA PILLAY/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	7	20	3

ADDRESS
Okamoto & Benedicto LLP
P.O. Box 641330
San Jose, CA 95164-1330
UNITED STATES

TITLE
FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14504771	COUSINS, PETER JOHN
	Examiner	Art Unit
	DEVINA PILLAY	1755

CPC- SEARCHED		
Symbol	Date	Examiner
H01L31/0236 H01L31/0745 H01L31/1804	6/8/2016	DP
H01L31/022425 H01L31/068 H01L31/182 H01L31/056	6/8/2016	DP
Y02E10/52 Y02P70/521 Y02E10/547	6/8/2016	DP

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US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor name search in PALM	6/8/2016	DP
EAST Text Search (See Search History)	6/8/2016	DP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14504771	COUSINS, PETER JOHN
	Examiner	**Art Unit**
	DEVINA PILLAY	1755

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/17/2016	06/08/2016							
	1	÷	✓							
	2	÷	✓							
	3	÷	✓							
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	15	÷	N							
	16	÷	N							
	17	÷	N							
	18	÷	N							
	19	÷	N							
	20	÷	N							

Receipt date: 06/11/2015
14504771 – GAU: 1755
Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed
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Art Unit	1757
Examiner Name	
Attorney Docket Number	10031.004211

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8222516		2012-07-17	Cousins	
	2	8878053		2014-11-04	Cousins	

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	1	2002539625	JP		2002-11-19	EBARA SOLAR, INC.		☐
	2	2009535845	JP		2009-10-01	SUNPOWER CORPORATION		☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.P/

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	3	H07106611	JP		1995-04-21	TONEN CORP		☐
	4	WO0055923	WO	A1	2000-09-21	EBARA SOLAR, INC.		☐
	5	WO2007130188	WO	A2	2007-11-15	SUNPOWER CORPORATION		☐

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Name/Print	PATRICK D. BENEDICTO	Registration Number	40909

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	142	"5011565"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 18:47
L2	72	"5057439"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 18:51
L3	6	"7858430"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 18:54
L5	17	(anti?reflect$4) with (stack) with ITO and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 19:15
L9	4439	(aluminum Al) with (silver Ag) with electrode and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 20:20
L10	660	(aluminum Al) with (silver Ag) with electrode and (solar photovoltaic).ab. and BSF	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 20:21
L13	51	("4403392" | "4502206").PN. OR ("5057439").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/08 20:40
L25	212	(polycrystalline polysilicon) near2 emitter and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2016/06/08 20:51

			DERWENT; IBM_TDB			
L26	689	(polycrystalline polysilicon) and BSF and (single near crystal$4 monocrystalline) near5 substrate and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 20:52
L27	699	(polycrystalline polysilicon) and (FSF BSF) and (single near crystal$4 monocrystalline) near5 substrate and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 20:53
L28	507	(polycrystalline polysilicon) and (FSF BSF) and (single near crystal$4 monocrystalline) near5 substrate and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 20:53
L29	63	(polycrystalline polysilicon) and (FSF) and (single near crystal$4 monocrystalline) near5 substrate and (solar photovoltaic).ab	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 20:54
L30	93	(FSF) and (single near crystal$4 monocrystalline) near5 substrate and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 20:55
L31	30	30 not 29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 20:56
L32	186	(FSF front near2 surface near field) and (single near crystal$4 monocrystalline) near5 substrate and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 20:57
L33	265	(FSF front near2 surface near field) and (single near crystal$4 monocrystalline wafer) near5 substrate and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 20:58
L34	172	33 not 30	US-PGPUB; USPAT; USOCR;	OR	ON	2016/06/08 20:58

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L35	71	Veschetti.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 21:02
L36	53	Veschetti.in. and photovoltaic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 21:02
L37	1	2008-D39688.NRAN.	DERWENT	OR	ON	2016/06/08 21:03
L38	7	"2003083955"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 21:04
L39	19	"5134090"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 21:06
L53	2	("20030183270" | "5057439").PN.	US-PGPUB; USPAT	OR	ON	2016/06/08 21:21
L54	2	"20030183270"	US-PGPUB; USPAT	OR	ON	2016/06/08 21:25
L55	2	("8222516" | "8878053").PN.	US-PGPUB; USPAT	OR	ON	2016/06/08 21:29
L56	32	(H01L31/0236 H01L31/0745 H01L31/1804 H01L31/022425 H01L31/068 H01L31/182 H01L31/056).cpc. and (Y02E10/52 Y02P70/521 Y02E10/547).cpc. and (polysilicon polycrystalline) near emitter and tunnel$3 near oxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 21:44
S1	2	"20030134469"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 11:43
S2	4	("2003/0134469").URPN.	USPAT	OR	ON	2009/12/07 11:56
S3	0	"10353261"	USPAT	OR	ON	2009/12/07 11:57
S4	1	"10/353261"	USPAT	OR	ON	2009/12/07

						11:57
S5	19	("2999240" | "4001864" | "4104091" | "4133698" | "4142200" | "4152824" | "4156822" | "4201798" | "4377901" | "4478879" | "5013396" | "5543333" | "6096968" | "6136673" | "6146483" | "6206996" | "6278053").PN. OR ("6825104").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 11:58
S6	39	(back near surface near field) and texture and dielectric	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 11:58
S7	18	(back near surface near field) and texture and dielectric and anti near reflective	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 12:06
S8	18	(back near surface near field) and texture and dielectric and anti near reflective	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 12:06
S9	10	(back near surface near field) and texture and antireflective and emitter	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 12:09
S10	65	texture and antireflective and emitter	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 12:09
S11	66	texture and antireflective and emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 12:10
S12	120	textur$4 and antireflective and emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 12:11
S13	54	S12 not S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 12:11
S14	18	S13 and dielectric	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 12:12
S15	3	"20070082206"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2009/12/07 12:17

			DERWENT; IBM_TDB			
S16	443	dielectric and antireflective and emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 12:17
S17	132	dielectric and antireflective and emitter and ((solar near cell) (photovoltaic))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 12:18
S18	192	(back near surface near field) and dielectric	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 12:18
S19	1	"20030134469"	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 12:28
S20	19	("3413157" | "4012235" | "4239810" | "4313768" | "4604791" | "4624045" | "4633031" | "4781766" | "4836861" | "4910153" | "5879977" | "6111191").PN. OR ("6210991").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 12:51
S21	2	"20060196535"	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 12:55
S22	14	("20030070707" | "4070097" | "4084099" | "4278831" | "4496788" | "5057439" | "5066340" | "5213628" | "5468652" | "5728230" | "6013582" | "6118258" | "6210991" | "6465724").PN. OR ("7554031").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 13:13
S23	346	dielectric and (antireflection or anti near reflection or ARC) and emitter and textur$5	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 13:17
S24	347	dielectric and (antireflection or anti near reflection or ARC) and emitter and textur$5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 13:17
S25	124	S23 and ((solar near cell) (photovoltaic))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 13:17
S26	7	11/263159	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 13:50

S27	29	S24 and optoelectronic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 14:08
S28	479	dielectric and (antireflection or anti near reflection or ARC) and (emitter or collector) and textur$5	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 14:09
S29	133	S28 not S24	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 14:09
S30	32	S29 and ((solar near cell) (photovoltaic))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 14:09
S31	19	("4090213" | "4131486" | "4133698" | "4232245" | "4255211" | "4315097" | "4316049" | "4341918" | "4365262" | "4367368" | "4385198" | "4427839").PN. OR ("4665277").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 14:32
S32	14	("3150999" | "4227942" | "4348254").PN. OR ("4427839").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 14:35
S33	1092	(antireflection or anti near reflection or ARC) and emitter and textur$5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 14:47
S34	233	S33 and (solar near cell)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 14:47
S35	215	S34 not (S17)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 14:47
S36	215	S35 not S29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 14:48
S37	0	2004/0112426	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2009/12/07 15:08

			EPO; JPO; DERWENT; IBM_TDB			
S38	2	"20040112426"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 15:08
S39	10	("20040200520" | "4234352" | "4478879" | "4920639" | "4927770" | "5053083" | "5320684" | "5538564" | "5641362" | "6624737").PN. OR ("7339110").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 15:14
S40	88	(back near surface near field) and antireflective and emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 15:23
S41	175	(back near surface near field) and (antireflective ARC (anti near reflective)) and emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 15:24
S42	87	S41 not S40	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 15:24
S43	138	S41 not S36	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 15:24
S44	26	("2841860" | "2854363" | "3134906" | "4070689" | "4341589" | "4428783" | "4523966" | "4665277" | "4703553" | "5156978").PN. OR ("5928438").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 15:30
S45	19	("4090213" | "4131486" | "4133698" | "4232245" | "4255211" | "4315097" | "4316049" | "4341918" | "4365262" | "4367368" | "4385198" | "4427839").PN. OR ("4665277").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 16:00
S46	11	("3081370" | "3757123" | "3948682" | "3969746").PN. OR ("4131486").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 16:02
S47	15	"5258077"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2009/12/07 17:11

			DERWENT; IBM_TDB			
S48	14	("3895975" | "4056879" | "4106047" | "4131486" | "4226017" | "4916503" | "5538564" | "5641362" | "5951742" | "5973260" | "6071753").PN. OR ("6262359").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 17:13
S49	7	(back near junction) and (passiv$4 with "SiO.sub.2")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 18:25
S50	10	(back with surface with field) and (passiv$4 with "SiO.sub.2")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 18:27
S51	15	(passiv$4 with "SiO.sub.2" with emitter)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 18:28
S52	1984	(passiv$4 with ("SiO.sub.2" or (silicon near dioxide)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 18:31
S53	67	(passiv$4 with ("SiO.sub.2" or (silicon near dioxide))) and solar near cell	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 18:31
S54	3	"20070082206"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 18:37
S55	14	("3895975" | "4056879" | "4106047" | "4131486" | "4226017" | "4916503" | "5538564" | "5641362" | "5951742" | "5973260" | "6071753").PN. OR ("6262359").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 19:00
S56	163	(back near junction) and (solar near cell)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 19:13

S57	141	(back near junction) and (photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 19:29
S58	39	S57 not S56	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 19:29
S59	345	(back near2 junction) and (solar near cell or (photovoltaic))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 19:31
S60	182	S59 not S56	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 19:31
S61	32	S60 and emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 19:31
S62	16	(US-20050268963-$ or US-20020153039-$ or US-20060196535-$ or US-20090101199-$ or US-20040097062-$ or US-20040112426-$ or US-20070186970-$).did. or (US-4379944-$ or US-4665277-$ or US-5320684-$ or US-6210991-$ or US-5792280-$ or US-5899704-$ or US-6262359-$ or US-5258077-$).did. or (US-20090205712-$).did.	US-PGPUB; USPAT; DERWENT	OR	ON	2009/12/07 19:33
S63	0	S62 and (isolation near2 trench)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 19:34
S64	346	dielectric and (antireflection or anti near reflection or ARC) and emitter and textur$5	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 19:34
S65	16	S64 and (isolation near trench)	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 19:34
S66	251	solar near cell and (isolation near trench)	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 19:35

S67	232	(back with surface with field) and (isolation near trench)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 19:36
S68	2	S67 and solar near cell	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 19:36
S69	24	(back with surface with field) and (isolation near2 edge) and (solar near cell)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 19:40
S70	49	("20030134469" | "20040200520" | "20040200520" | "20060130891" | "20070082206" | "3961997" | "3961997" | "4927770" | "4927770" | "5030295" | "5053083" | "5057439" | "5164019" | "5217539" | "5360990" | "5369291" | "5641362" | "5030295" | "5053083" | "5057439" | "5164019" | "5217539" | "5266125" | "5360990" | "5369291" | "5641362" | "6274402" | "6313395" | "6333457" | "6387726" | "6423568" | "6998288" | "6998288" | "6274402" | "6313395" | "6333457" | "6337283" | "6387726" | "6423568" | "6524880" | "6998288" | "7135350" | "7135350").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 19:54
S71	288	oxide with passiv$5 with emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 20:00
S72	32	S71 and ((solar near cell) photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 20:00
S73	29	"4726850"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 20:29
S74	0	(back with surface with field) and (isolat$3 near5 edge with trench) and (solar near cell)	US-PGPUB; USPAT; USOCR;	OR	ON	2009/12/07 20:34

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S75	32	(back with surface with field) and (isolat$3 near5 edge) and (solar near cell)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 20:34
S76	39	(back with surface with field) and (isolation near5 trench with etch)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 20:40
S77	20	(solar near cell) and (isolation near5 trench with etch)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 20:41
S78	304	(solar near cell) and (isolation near5 trench)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 20:42
S79	7	(solar near cell) and (isolation near5 trench with edge)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 20:42
S80	24	(trench with (electric$4 near isolat$4)) and emitter and (solar near cell)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 20:52
S81	41	(silver near5 ("SiO.sub.2" or silicon near dioxide)) and (solar near cell) and emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 21:06
S82	42	(silver near5 ("SiO.sub.2" or silicon near dioxide or passiv$4)) and (solar near cell) and emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 21:07
S83	50	((silver or Ag) near5 ("SiO.sub.2" or	US-PGPUB;	OR	ON	2009/12/07

		silicon near dioxide or passiv$4)) and (solar near cell) and emitter	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			21:07
S84	44	((silver) near5 ("SiO.sub.2" or silicon near dioxide or passiv$4)) and ((solar near cell) or photovoltaic) and emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 21:08
S85	90	((silver) near5 ("SiO.sub.2" or silicon near dioxide or passiv$4)) and ((solar near cell) or photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 21:09
S86	46	S85 not S84	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 21:09
S87	105	((silver) near5 ("SiO.sub.2" or silicon near dioxide or passiv$4)) and ((solar near cell) or photovoltaic or optoelectronic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 21:12
S88	15	S87 not S85	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 21:12
S89	345	((silver) with ("SiO.sub.2" or silicon near dioxide or passiv$4)) and ((solar near cell) or photovoltaic or optoelectronic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 21:13
S90	240	S89 not S87	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/07 21:13
S91	14	("3150999" | "4227942" | "4348254").PN. OR ("4427839").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 21:17
S92	1122	silver with infrared with reflect$4	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 21:38

S93	584	silver near5 infrared with reflect$4	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 21:38
S94	565	silver near5 infrared near5 reflect$4	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 21:38
S95	25	S94 and solar near cell	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 21:38
S96	29	S94 and photovoltaic	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 21:41
S97	18	"5479018"	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/07 21:56
S98	1822	dichroic near coating	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/08 10:20
S99	54	dichroic near coating and (powder)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/08 10:21
S100	296	(fluorescent near powder) and (light near5 film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/08 10:22
S101	1	6262359B1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/10 10:08
S102	1	2000-587576.NRAN.	DERWENT	OR	ON	2009/12/10 10:08
S103	5	"6262359"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/12/10 10:08
S104	14	("3895975" | "4056879" | "4106047" | "4131486" | "4226017" | "4916503" | "5538564" | "5641362" | "5951742" | "5973260" | "6071753").PN. OR ("6262359").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/10 10:09
S105	11	("3081370" | "3757123" | "3948682" | "3969746").PN. OR ("4131486").URPN	US-PGPUB; USPAT;	OR	ON	2009/12/10 10:09

			USOCR			
S106	12	("4090213" | "4131486" | "4133698" | "4232245" | "4255211" | "4315097" | "4316049" | "4341918" | "4365262" | "4367368" | "4385198" | "4427839").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/10 10:11
S107	14	("3150999" | "4227942" | "4348254").PN. OR ("4427839").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/10 10:11
S108	19	("4090213" | "4131486" | "4133698" | "4232245" | "4255211" | "4315097" | "4316049" | "4341918" | "4365262" | "4367368" | "4385198" | "4427839").PN. OR ("4665277").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/10 10:11
S109	9	floating same emitter same solar same cell	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/10 10:33
S110	19	("4090213" | "4131486" | "4133698" | "4232245" | "4255211" | "4315097" | "4316049" | "4341918" | "4365262" | "4367368" | "4385198" | "4427839").PN. OR ("4665277").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/12/10 10:35
S111	7	"6262359"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/05/20 10:23
S112	16	("3895975" | "4056879" | "4106047" | "4131486" | "4226017" | "4916503" | "5538564" | "5641362" | "5951742" | "5973260" | "6071753").PN. OR ("6262359").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/20 10:23
S113	4	S112 and polycrystal$4	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/20 10:23
S114	9	("4377901" | "4478879" | "5082791" | "5665175").PN. OR ("6071753").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/20 10:26
S115	10	("20020011590" | "5103851" | "5437734" | "5738732" | "6071753" | "6130380" | "6166320" | "6548751").PN. OR ("6927417").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/20 10:28
S116	6	("4837607" | "5543333" | "5738732").PN. OR ("6130380").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/20 10:29
S117	414	polycrystalline near5 substrate same emitter	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/20 10:43
S118	45	S117 and ((solar photovoltaic) near (battery device cell))	US-PGPUB; USPAT; USOCR	OR	ON	2010/05/20 10:43
S119	10	"4665277"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2010/05/20 11:39

			IBM_TDB			
S120	1	"12070742"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/05/20 11:44
S121	1	"12070742"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/15 16:12
S122	41	polysilicon near2 emitter and (photovoltaic solar near2 (Cell device battery))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 16:28
S123	18	"4989059"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 16:34
S124	50	(polysilicon polycrystalline) near2 emitter and (photovoltaic solar near2 (Cell device battery))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 16:35
S125	9	S124 not S122	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 16:35
S126	343	(polysilicon polycrystalline) same emitter and (photovoltaic solar near2 (Cell device battery))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 16:37
S127	297	(polysilicon polycrystalline) same emitter and (photovoltaic solar near2 (Cell device battery)) and (dielectric oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 16:37
S128	347591	(polysilicon polycrystalline) wiith emitter and (photovoltaic solar near2 (Cell device battery)) and (dielectric oxide)	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2012/03/15 16:37

			EPO; JPO; DERWENT; IBM_TDB			
S129	128	(polysilicon polycrystalline) with emitter and (photovoltaic solar near2 (Cell device battery)) and (dielectric oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 16:37
S130	86	S129 not S124	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 16:38
S131	2	"20090159111"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 16:43
S132	6	"2008004791"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 16:46
S133	10	"7468485"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 16:47
S134	24	("3961997" | "4927770" | "5030295" | "5053083" | "5057439" | "5164019" | "5360990" | "5369291" | "5641362" | "6274402" | "6313395" | "6333457" | "6337283" | "6387726" | "6423568" | "6998288").PN. OR ("7468485").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/15 16:49
S135	14	"5057439"	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/15 16:55
S136	1	"20090159111"	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/15 16:55
S137	23	("4090213" | "4131486" | "4133698" | "4232245" | "4255211" | "4315097" | "4316049" | "4341918" | "4365262" | "4367368" | "4385198" | "4427839").PN. OR ("4665277").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/15 16:58
S138	0	S129 not S126	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2012/03/15 17:03

			DERWENT; IBM_TDB			
S139	215	S126 not S129	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:03
S140	74	emitter and (photovoltaic solar near2 (Cell device battery)) and tunnel near oxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:04
S141	75	emitter and (photovoltaic solar near2 (Cell device battery)) and tunnel$3 near oxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:10
S142	1	S141 not S140	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:10
S143	222	emitter and (photovoltaic solar near2 (Cell device battery)) and tunnel$3 near5 (oxide barrier)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:11
S144	147	S143 not S141	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:12
S145	188	emitter and (photovoltaic solar near2 (Cell device battery)) and tunnel$3 near2 (oxide barrier)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:22
S146	488	(photovoltaic solar near2 (Cell device battery)) and tunnel$3 near2 (oxide barrier)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:27
S147	413	(photovoltaic solar near2 (Cell device battery)) and tunnel$3 near2 (oxide barrier) and silicon	US-PGPUB; USPAT; USOCR;	OR	OFF	2012/03/15 17:27

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S148	238	S147 not S145	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:28
S149	24	("3961997" | "4927770" | "5030295" | "5053083" | "5057439" | "5164019" | "5360990" | "5369291" | "5641362" | "6274402" | "6313395" | "6333457" | "6337283" | "6387726" | "6423568" | "6998288").PN. OR ("7468485").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/15 17:32
S150	0	Sah.in. and emittter	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/15 17:35
S151	10	Sah.in. and emitter	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/15 17:35
S152	23	("4090213" | "4131486" | "4133698" | "4232245" | "4255211" | "4315097" | "4316049" | "4341918" | "4365262" | "4367368" | "4385198" | "4427839").PN. OR ("4665277").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/15 17:36
S153	4089	(photovoltaic solar near2 (Cell device battery)) and (passivat$4 near2 oxide dielectric) and silicon and (passivat$4 near2 oxide dielectric) with (reflect$4 metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:39
S154	11442	(photovoltaic solar near2 (Cell device battery)) and (passivat$4 near2 oxide dielectric) and silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:39
S155	11442	(photovoltaic solar near2 (Cell device battery)) and ((passivat$4 near2 oxide) dielectric) and silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:40
S156	11276	(photovoltaic solar near (Cell battery)) and ((passivat$4 near2 oxide) dielectric) and silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:40
S157	4063	(photovoltaic solar near (Cell battery)) and ((passivat$4 near2 oxide) dielectric) and silicon and (passivat$4 near2 oxide dielectric) with (reflect$4 metal)	US-PGPUB; USPAT; USOCR; FPRS;			

			EPO; JPO; DERWENT; IBM_TDB			
S158	612	(photovoltaic solar near (Cell battery)) and ((passivat$4 near2 oxide) dielectric) and silicon and (passivat$4 near2 oxide dielectric) with (reflect$4 metal) and tunnel$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:40
S159	612	(photovoltaic solar near (Cell battery)) and ((passivat$4 near2 oxide) dielectric) and silicon and (passivat$4 near2 oxide dielectric) with (reflect$4 metal) and tunnel$3 and silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:40
S160	301	(photovoltaic solar near (Cell battery)) and ((passivat$4 near2 oxide) dielectric) and silicon and (passivat$4 near2 oxide dielectric) with (reflect$4 metal) and tunnel$3 and emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:41
S161	301	S160 not S148	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:41
S162	8	"5956571"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:57
S163	58	"4200472"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:58
S164	2	"20060130891"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 17:59
S165	50	Borden.in. and emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/15 18:00
S166	13	"5057439"	USPAT	OR	OFF	2012/03/16 10:33

S167	0	"20090159111"	USPAT	OR	OFF	2012/03/16 10:36
S168	2	"20090159111"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/16 10:36
S169	2	"20050268963"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/16 10:38
S170	24	("3961997" | "4927770" | "5030295" | "5053083" | "5057439" | "5164019" | "5360990" | "5369291" | "5641362" | "6274402" | "6313395" | "6333457" | "6337283" | "6387726" | "6423568" | "6998288").PN. OR ("7468485").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 10:45
S171	14	("4403392" | "4502206").PN. OR ("5057439").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 10:47
S172	1	"20060096635"	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 10:49
S173	1	"20090159111"	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 10:49
S174	1	"20050268963"	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 10:54
S175	114	polysilicon near emitter and native near oxide	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 11:12
S176	2	polysilicon near emitter and native near oxide and (photovoltaic and solar near2 (battery cell device))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 11:13
S177	367	polysilicon near emitter and "SiO.sub.2"	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 11:14
S178	2	polysilicon near emitter and "SiO.sub.2" and (photovoltaic and solar near2 (battery cell device))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 11:15
S179	6	Borden.in. and polysilicon near emitter	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 11:15
S180	10	polysilicon near emitter and (photovoltaic and solar near2 (battery cell device))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 11:17
S181	17	(polycyrstalline multicrystalline polysilicon) near2 emitter and (photovoltaic and solar near2 (battery cell device))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 11:19
S182	0	"2008004791"	US-PGPUB; USPAT;	OR	OFF	2012/03/16 11:27

			USOCR			
S183	2	"20080004791"	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 11:28
S184	0	"2008004791"	US-PGPUB; USPAT; USOCR	OR	OFF	2012/03/16 11:28
S185	6	"2008004791"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/16 11:28
S186	3869	438/72.ccls. 438/57.ccls. 438/69.ccls. 438/97.ccls. 438/98.ccls. 257/461.ccls. 257/436.ccls.	USPAT	OR	OFF	2012/03/19 11:37
S187	7338	438/72.ccls. 438/57.ccls. 438/69.ccls. 438/97.ccls. 438/98.ccls. 257/461.ccls. 257/436.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/19 11:37
S188	552	S187 and emitter and (photovoltaic solar near (cell device battery))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/19 11:37
S189	426	S188 and oxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/19 11:38
S190	39	S188 and oxide and polysilicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/19 11:38
S191	419	S188 and oxide and silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/19 11:45
S192	237	S188 and oxide and (light near incident front) near5 (contact wir$4 connect$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/03/19 11:46
S193	12	S188 and oxide and (light near incident	US-PGPUB;	OR	OFF	2012/03/19

		front) near5 (contact wir$4 connect$4) and tunnel$3 near5 oxide	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:53
S194	2	"12707042"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/11 13:10
S195	16	"1270742"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/11 13:10
S196	2	"12070742"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/11 13:10
S197	31	("20030134469" | "20040200520" | "20050268963" | "20060130891" | "20060157103" | "20070082206" | "3961997" | "4427839" | "4665277" | "4927770" | "5030295" | "5053083" | "5057439" | "5164019" | "5217539" | "5266125" | "5360990" | "5369291" | "5449626" | "5479018" | "5641362" | "6262359" | "6274402" | "6313395" | "6333457" | "6337283" | "6387726" | "6423568" | "6524880" | "6998288" | "7135350").PN. OR ("8222516").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 13:11
S198	1	"20040055894"	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 13:26
S199	2	"11915984"	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 13:26
S200	2	"20090159111"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 13:32
S201	42	("3961997" | "4927770" | "5030295" | "5053083" | "5057439" | "5164019" | "5360990" | "5369291" | "5641362" | "6274402" | "6313395" | "6333457" | "6337283" | "6387726" | "6423568" | "6998288").PN. OR ("7468485").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 13:35
S202	26	"5057439"	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 13:41

S203	26	("4403392" | "4502206").PN. OR ("5057439").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 13:42
S204	1	"12983846"	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 13:50
S205	33	polysilicon near emitter and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 13:51
S206	3	"7468482"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 13:54
S207	30	"7468485"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 13:54
S208	2	"20090288704"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 14:01
S209	1	2009-P84539.NRAN.	DERWENT	OR	ON	2013/09/11 14:01
S210	3	"20070256728"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 14:03
S211	2074	polysilicon near emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 14:08
S212	55	polysilicon near emitter and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 14:08
S213	72	polysilicon near5 emitter and (solar photovoltaic)	US-PGPUB; USPAT; USOCR;	OR	ON	2013/09/11 14:14

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S214	17	S213 not S212	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 14:14
S215	6	"2008004791"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 14:15
S216	24	(polycyrstalline multicrystalline polysilicon) near2 emitter and (photovoltaic and solar near2 (battery cell device))	US-PGPUB; USPAT; USOCR	OR	OFF	2013/09/11 14:17
S217	4	lindholm.in. and solar near cell	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 14:54
S218	0	lindholm.in. and "136."	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 14:56
S219	3	lindholm.in. and "136".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 14:56
S220	2	polysilicon near solar same emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 14:59
S221	20	("3900943" | "4062038" | "4171997" | "4197141" | "4219368" | "4230508" | "4249957" | "4278473" | "4283589" | "4320168" | "4366338").PN. OR ("4431858").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 15:00
S222	6	("20030183270" | "20090255574" | "20090283138" | "3969163" | "4431858" | "4571448").PN. OR ("8283557").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 15:02
S223	26	("4403392" | "4502206").PN. OR	US-PGPUB;	OR	ON	2013/09/11

		("5057439").URPN.	USPAT; USOCR			16:29
S224	2	"12166266"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 16:43
S225	395	polysilicon near5 emitter same oxide same dopant	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 16:45
S226	377	polysilicon near5 emitter same oxide with dop$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 16:45
S227	26	polysilicon near5 emitter same oxide with dop$3 same phosphorus	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 16:45
S228	6	"11201817"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 16:48
S229	53	Swanson near Richard and solar near cell	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 16:52
S230	158	"5053083"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 16:53
S231	38	("20040200520" | "4234352" | "4478879" | "4920639" | "4927770" | "5053083" | "5320684" | "5538564" | "5641362" | "6624737").PN. OR ("7339110").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 17:03
S232	687	phosphosilicate near glass same (dielectric oxide) with (passivation capping)	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 17:14
S233	41	phosphosilicate near glass same	US-PGPUB;	OR	ON	2013/09/11

		(dielectric oxide) with (passivation capping) same polysilicon	USPAT; USOCR			17:15
S234	0	"2008004791"	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 17:17
S235	2	"20080004791"	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 17:17
S236	59	"5693578"	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 17:17
S237	11	(back near surface near field BSF) same polysilicon	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/11 17:19
S238	14	(back near surface near field BSF) same polysilicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 17:21
S239	3	S238 not S237	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 17:21
S240	81	(back near surface near field BSF) same polycrystalline near silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 17:23
S241	81	S240 not S238	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 17:23
S242	157	(back near surface near field BSF) and polysilicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 17:35
S243	143	S242 not S238	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 17:35
S244	476	(back near surface near field BSF) same passivat$4 and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2013/09/11 17:45

			EPO; JPO; DERWENT; IBM_TDB			
S245	108	(back near surface near field BSF) same passivat$4 and (solar photovoltaic).ab. and heterojunction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 17:45
S246	26	"4315097"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:00
S247	2	"20040205520"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:02
S248	3	"20040200520"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:02
S249	25	(back near surface near field BSF) same passivat$4 and (solar photovoltaic).ab. and polysilicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:09
S250	717	(back near surface near field BSF) same (capping oxide dielectric passivat$4) and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:10
S251	75	(back near surface near field BSF) same (capping oxide dielectric passivat$4) and (solar photovoltaic).ab. and Phosphosilicate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:11
S252	114	(back near surface near field BSF) same (capping oxide dielectric passivat$4) and (solar photovoltaic).ab. and (Phosphosilicate PSG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:16
S253	39	S252 not S251	US-PGPUB; USPAT;	OR	ON	2013/09/11 18:16

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S254	158	(back near surface near field BSF) same (capping oxide dielectric passivat$4) and (Phosphosilicate PSG)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:18
S255	44	S254 not S252	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:18
S256	1163	(back near surface near field BSF) same (capping oxide dielectric passivat$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:20
S257	727	(back near surface near field BSF) same (capping oxide dielectric passivat$4) and (solar photovoltaic photoelectric).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:21
S258	33	(back near surface near field BSF) same (capping oxide dielectric passivat$4) and (solar photovoltaic photoelectric).ab. and polysilicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:21
S259	703	polysilicon with PSG with (dielectric oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:30
S260	81	polysilicon with PSG with (dielectric oxide) and emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:31
S261	225	polysilicon with PSG with (dielectric oxide) same dop$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:33

S262	2	polysilicon with PSG with (dielectric oxide) same dop$3 and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:34
S263	44	polysilicon with PSG with (dielectric oxide) and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:34
S264	161	(phosphosilicate PSG) with (dielectric oxide) same dop$4 and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:35
S265	62	(phosphosilicate PSG) with (dielectric oxide) same dop$4 and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:35
S266	103	(phosphosilicate PSG borosilicate BSG) with (dielectric oxide) same dop$4 and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:42
S267	41	S266 not S265	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:42
S268	2	"20080173347"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:43
S269	3	"20060196535"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:45
S270	179	"4927770"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2013/09/11 18:46

			DERWENT; IBM_TDB			
S271	57	(phosphosilicate PSG borosilicate BSG) with (dielectric oxide cap$4) same dop$4 and (back near surface near field BSF)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:50
S272	145	(phosphosilicate PSG borosilicate BSG) with (dielectric oxide cap$4) and (back near surface near field BSF)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:52
S273	0	S271 not S271	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:52
S274	88	S272 not S271	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:53
S275	190	(phosphosilicate PSG borosilicate BSG) with (dielectric oxide cap$4) with (dop$4) with (burn$4 escap$4 leav$4 diffus$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 10:22
S276	130	(phosphosilicate PSG borosilicate BSG) with (dielectric "SiO.sub.2" silicon near oxide cap$4) with (dop$4) with (burn$4 escap$4 leav$4 diffus$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 10:28
S277	341	(phosphosilicate PSG borosilicate BSG) with (dielectric "SiO.sub.2" silicon near oxide cap$4) and (solar photoelectric photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 10:39
S278	14	(phosphosilicate PSG borosilicate BSG) with (dielectric "SiO.sub.2" silicon near oxide cap$4) with (dop$4) with (burn$4 escap$4 leav$4 diffus$4) and (solar photoelectric photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 10:42
S279	23	(phosphosilicate PSG borosilicate BSG) with (dielectric "SiO.sub.2" silicon near oxide cap$4) with (dop$4) with (burn$4	US-PGPUB; USPAT; USOCR;	OR	ON	2013/09/12 10:44

		escap$4 leav$4 diffus$4) and (solar photoelectric photovoltaic)	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S280	18	(phosphosilicate PSG borosilicate BSG) with (cap$4) with (dop$4) and (solar photoelectric photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 10:46
S281	35	("3895975" | "4056879" | "4106047" | "4131486" | "4226017" | "4916503" | "5538564" | "5641362" | "5951742" | "5973260" | "6071753").PN. OR ("6262359").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/12 12:04
S282	6	(oxide with tunnel) same (pn near junction) and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:08
S283	6	(oxide with tunnel$5) same (pn near junction) and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:10
S284	86	(oxide with tunnel$5) same (junction) and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:10
S285	80	S284 not S283	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:10
S286	3	"20070256728"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:12
S287	52	"4272641"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:14
S288	211	(oxide with tunnel$5) and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR;	OR	ON	2013/09/12 12:15

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S289	88	thin same (oxide with tunnel$5) and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:15
S290	87	S289 not S287	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:15
S291	1100	(oxide with tunnel$5) and (solar photovoltaic photoelectric)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:22
S292	301	(oxide with tunnel$5) same (pn junction p-type n-type) and (solar photovoltaic photoelectric)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:24
S293	243	(S292 not S289)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:24
S294	7	"4495375"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:31
S295	6	("3990097" | "4338482").PN. OR ("4495375").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/12 12:31
S296	24	("3559281" | "4013485" | "4062102" | "4253881" | "4403239" | "4404421" | "4404422" | "4495375" | "4640002" | "4806496" | "4828628").PN. OR ("4891325").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/12 12:32
S297	60	"6998288"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:41

S298	53	("20040200520" | "4927770" | "5053083" | "5164019" | "5217539" | "5360990" | "5369291" | "6274402" | "6313395" | "6333457" | "6337283" | "6387726" | "6423568").PN. OR ("6998288").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/12 12:55
S299	23	Sunpower.as. and oxide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 13:35
S300	5	"12070742"	US-PGPUB; USPAT; USOCR	OR	OFF	2016/06/08 12:05
S301	5181	tunneling near2 oxide	US-PGPUB; USPAT; USOCR	OR	OFF	2016/06/08 12:19
S302	205	tunnel$4 near2 oxide and (solar photovoltaic) and (rear$4 back$4) near2 (electrode contact) and (passivat$4 anti?reflect$4 ARC)	US-PGPUB; USPAT; USOCR	OR	OFF	2016/06/08 12:20
S303	210	tunnel$4 near2 oxide and (solar photovoltaic) and (rear$4 back$4) near2 (electrode contact) and (passivat$4 anti?reflect$4 ARC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 12:29
S304	5	S303 not S302	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 12:29
S305	238	(heterojunction) and (solar photovoltaic) and (rear$4 back$4) near2 (electrode contact) and (passivat$4 anti?reflect$4 ARC) and (polysilicon polycrystalline) same (wafer monocrystalline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 12:31
S306	99	"7468485"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 12:46
S307	66	"6262359"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 12:49
S308	421	(heterojunction) and (solar photovoltaic) and (passivat$4 anti?	US-PGPUB; USPAT;	OR	OFF	2016/06/08 13:20

		reflect$4 ARC) and (polysilicon polycrystalline) same (wafer monocrystalline)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S309	183	S308 not S305	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 13:21
S310	49	"5030295"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 13:23
S311	129	("4602120" | "4675468" | "4703553" | "4726850" | "4781766" | "4824489" | "5030295" | "5053083" | "5346850").PN. OR ("5538564").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/08 13:25
S312	248	tunnel$4 near2 oxide and (solar photovoltaic) and (rear$4 back$4) near2 (electrode contact)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 13:43
S313	199	tunnel$4 near2 oxide and (solar photovoltaic) and (polysilicon polycrystalline) same (wafer monocrystalline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 13:44
S314	105	S313 not S302	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 13:44
S315	516	(solar photovoltaic) and (polysilicon polycrystalline) with emitter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 13:48
S316	115	(solar photovoltaic) and (polysilicon polycrystalline) with emitter and heterojunction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 13:49
S317	635	(solar photovoltaic) and (polysilicon polycrystalline multicrystalline silicon) with emitter and heterojunction	US-PGPUB; USPAT; USOCR;	OR	OFF	2016/06/08 13:59

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S318	442	(solar photovoltaic) and (polysilicon polycrystalline multicrystalline silicon Si) with emitter and heterojunction and (polysilicon polycrystalline multicrystalline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 13:59
S319	327	S318 not S316	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 14:00
S320	51	("4403392" | "4502206").PN. OR ("5057439").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/08 14:09
S321	8	("20030089393" | "20060255340" | "20060263642" | "4703553" | "5011565" | "5057439" | "6403877" | "7858430").PN. OR ("8207443").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/08 14:12
S322	34	"5030295"	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/08 14:16
S323	1803	tunnel$4 and (solar photovoltaic) and heterojunction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 14:20
S324	380	tunnel$4 and (solar photovoltaic) and heterojunction and emitter and heterojunction and (polysilicon polycrystalline multicrystalline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 14:20
S325	275	S324 not S319	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 14:20
S326	3	"20060263642"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 14:22
S327	807	tunnel$4 and (solar photovoltaic) and heterojunction and emitter	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2016/06/08 14:23

			EPO; JPO; DERWENT; IBM_TDB			
S328	427	S327 not S324	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/08 14:23
S329	35	"5563092"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 15:23
S330	516761	polycrystalline and (thin tunnel$3) oxide and crystalline	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 15:25
S331	11587	polycrystalline and (thin tunnel$3) near2 oxide and crystalline	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 15:25
S332	1066	polycrystalline same (thin tunnel$3) near2 oxide same (monocrystalline wafer crystalline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 15:25
S333	147	polycrystalline same (thin tunnel$3) near2 oxide same (monocrystalline wafer crystalline) and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 15:25
S334	282	(polysilicon polycrystalline) same (thin tunnel$3) near2 oxide same (monocrystalline wafer crystalline) and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 15:30
S335	27	(emitter) with (thin tunnel$3) near2 oxide same (monocrystalline wafer crystalline) and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 15:39
S336	28	(emitter) with (thin tunnel$3 interfacial) near2 oxide same (monocrystalline	US-PGPUB; USPAT;	OR	ON	2016/06/08 15:40

		wafer crystalline) and (solar photovoltaic)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S337	1098	(thin tunnel$3) near2 oxide and heterojunction and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 15:42
S339	432	(thin tunnel$3) near2 oxide and heterojunction and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 15:43
S340	405	S339 not S328	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 15:43
S341	176	(interfacial interface tunnel$3) near2 oxide and heterojunction and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 15:46
S342	3	"20070256728"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 15:49
S343	16	emitter with interfacial near oxide and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:02
S344	24	("3919639" | "4296372" | "4431460" | "4464627" | "4467519" | "4483726" | "4598249" | "4609867" | "4695794" | "4709141" | "4859939" | "4956603").PN. OR ("5138256").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/08 16:05
S345	353	(interfacial interface tunnel$3) near2 oxide same (polysilicon polycrystalline) and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:06
S346	356	(interfacial interface tunnel$3) near2 oxide same (polysilicon polycrystalline	US-PGPUB; USPAT;	OR	ON	2016/06/08 16:09

		multicrystalline) and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S347	449	(interfacial interface tunnel$3 silicon) near2 oxide with (interfac$3 tunnel$) same (polysilicon polycrystalline) and (solar photovoltaic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:14
S348	62	tunneling near oxide and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:23
S349	2632	(inversion tunneling near oxide) and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:25
S350	123	(inversion with oxide tunneling near oxide) and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:25
S351	276	(inversion with oxide tunnel$3 near oxide) and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:26
S352	222	(tunnel$3 near oxide) and (solar photovoltaic).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:27
S353	153	S352 not S350	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:27
S354	35	"5563092"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:37

S355	84638	polysilicon with interfac$4 oxide with growth	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:38
S356	17344	polysilicon with interfac$4 oxide with growth with (crystalline single near crystal wafer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:38
S357	0	polysilicon with interfac$4 near3 oxide with growth with (crystalline single near crystal wafer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:38
S358	62	polysilicon with interfac$4 near3 oxide with (crystalline single near crystal wafer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/08 16:38

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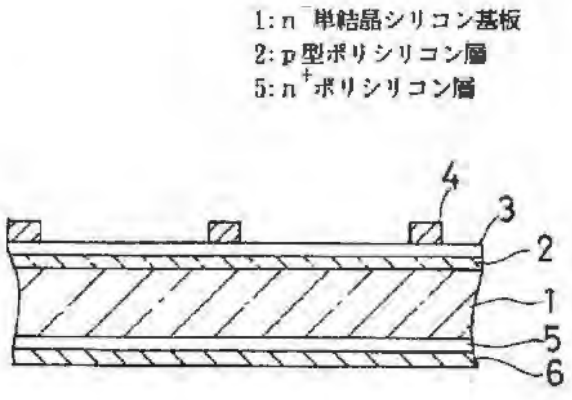
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(54)【発明の名称】　ＢＳＦ型太陽電池の製造方法

(57)【要約】

【目的】　光電変換効率の高いＢＳＦ型太陽電池を安定して製造できる方法を提供すること。

【構成】　ｎ⁻単結晶シリコン（以下、Si）基板１と、この光入射側面に設けられたｐ型のポリSi層２と、反対側面に設けられSi基板との間でＨＬ接合を形成するｎ⁺ポリSi層５を備えるＢＳＦ型太陽電池の製造方法であり、上記ｎ⁺ポリSi層をB_2H_6／SiH_4／SiF_4を原料ガスとする熱ＣＶＤ法により形成することを特徴とする。この方法によれば、ハロゲン原子を放出するSiF_4を適用しているにも拘らず製膜室内における浮遊異物の発生を防止でき、かつ、熱ＣＶＤ法を適用しているにも拘らず基板加熱温度の低減を図ることが可能となるため、ｎ⁺ポリSi層の膜質が改善されて光電変換効率の高いＢＳＦ型太陽電池を安定して製造できる効果を有している。



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【特許請求の範囲】

【請求項1】n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法において、

n型又はp型シリコン基板を配置した製膜室内にシリコン原子が含まれる製膜ガスとSiF_4ガス及びn型又はp型のドーパントガスを供給し、かつ、上記供給ガスを加熱されたシリコン基板近傍で熱分解させると共に、熱分解された製膜ガスのラジカル成分と上記SiF_4ガスとの反応により生じたフッ素系ラジカルをエッチング成分として作用させながらn型又はp型シリコン基板面に上記n⁺又はp⁺シリコン層を形成することを特徴とするBSF型太陽電池の製造方法。

【請求項2】n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法において、

n型又はp型シリコン基板を配置した製膜室内に水素化珪素を主成分とする製膜ガスとSiH_mF_{4-m}（但しmは1～3）で示されるフッ素化シランガス及びn型又はp型のドーパントガスを供給し、かつ、上記供給ガスを加熱されたシリコン基板近傍で熱分解させると共に、フッ素化シランガスの熱分解により生じたフッ素系ラジカル、及び、熱分解された製膜ガスのラジカル成分が上記フッ素化シランガスと反応して生じたフッ素系ラジカルをエッチング成分として作用させながらn型又はp型シリコン基板面に上記n⁺又はp⁺シリコン層を形成することを特徴とするBSF型太陽電池の製造方法。

【請求項3】製膜室内に配置されたn型又はp型シリコン基板近傍の空間部位に上記基板が覆われるように網状の発熱部材を配置したことを特徴とする請求項1又は2記載のBSF型太陽電池の製造方法。

【請求項4】n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法において、

加熱されたシリコン基板面に上記n⁺又はp⁺シリコン層を光CVD法により形成することを特徴とするBSF型太陽電池の製造方法。

【請求項5】n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL

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接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法において、

n型又はp型シリコン基板を配置した製膜室内にSiH_mF_{4-m}（但しmは1～3）で示されるフッ素化シランガス又はSiF_4ガスを供給し、かつ、このフッ素化シランガス又はSiF_4ガスが存在する条件下においてイオンプレーティング法により加熱されたシリコン基板面に上記n⁺又はp⁺シリコン層を形成することを特徴とするBSF型太陽電池の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明はBSF（Back Surface Field）型太陽電池の製造方法に係り、特に、光電変換効率の高いBSF型太陽電池を安定して製造できるBSF型太陽電池の製造方法に関するものである。

【0002】

【従来の技術】この種のBSF型太陽電池としては、例えば、図7～8に示すようにp型単結晶シリコン基板aと、このシリコン基板aの光入射側面に設けられシリコン基板aとの間でpn接合を形成するn⁺シリコン層bと、このn⁺シリコン層b上に一様に成膜されたITO（酸化インジウム錫）の反射防止層cと、この反射防止層c上に設けられた櫛歯状電極dと、上記シリコン基板aの反対側面に設けられシリコン基板aとの間でHL（High-Low）接合を形成するp⁺シリコン層eと、このp⁺シリコン層eの背面側に一様に設けられた裏面電極fとでその主要部が構成され、光入射に伴って発生したエレクトロンとホールが上記電極d、fから電流として取出される構造のものが知られている。

【0003】尚、図9はこのBSF型太陽電池の構造をモデル的に記載した構造概念図であり、また、図10はこの構造を有するBSF型太陽電池のエネルギーバンド図を示している。

【0004】そして、p⁺シリコン層eを具備しない構造の太陽電池と較べてこのBSF型太陽電池においては、HL接合gを形成するシリコン基板aとp⁺シリコン層e間に存在する内蔵電界が少数キャリア（この場合、エレクトロン）の裏面電極fへの拡散の障壁となり見掛け上エレクトロンの拡散長が増加し、かつ上記p⁺シリコン層eがホールに対して低抵抗のオーム性電極になるためシリーズ抵抗が低下し、従って、その光電変換効率を向上できる利点を有するものであるとされていた。

【0005】ところで、開放電圧を上昇させる上記p⁺シリコン層eについては、従来『熱拡散法』により形成されていた。すなわち、B（ボロン）等を含むp型ドーパントガスで満たされた反応室内に上記単結晶シリコン基板aを導入し、このドーパントガスをシリコン基板a内に1000℃前後の高温条件下で熱拡散させて形成したり、単結晶シリコン基板a面にAl（アルミニウム）

等のp型ドーパント層を積層しこれを１０００℃前後の高温条件下で焼成してp⁺シリコン層eを形成していた。

【０００６】しかし、この『熱拡散法』によりp⁺シリコン層eを形成した場合、p⁺シリコン層eの厚み制御が難しくその層厚が数百オングストローム～数μmと大きくなり易く、かつ、熱的条件の僅かなばらつきでB、Al等ドーパントガスの拡散距離が変動し易いためシリコン基板aの特性がばらつき易い欠点があった。

【０００７】更に、上記『熱拡散法』ではドーパントガスの回り込みも起こり易く、シリコン基板との間でpn接合を形成するn⁺シリコン層b内へも上記ドーパントガスが熱拡散してしまうことがあり、また、シリコン基板が１０００℃前後の高温に晒されることから基板の熱劣化を引起こす等の欠点もあった。

【０００８】このような技術的背景の下、本出願人は上記n型又はp型シリコン基板との間でHL接合を形成するn⁺シリコン層又はp⁺シリコン層をプラズマCVD法により形成するBSF型太陽電池の製造方法を既に提案している。すなわち、この製造方法によれば、従来の熱拡散法による場合に較べてn⁺シリコン層又はp⁺シリコン層形成時における熱的条件が緩和されるためシリコン基板の特性劣化が起こり難くなると共に、上記n⁺シリコン層又はp⁺シリコン層の厚さを従来より薄い数十オングストローム～数百オングストローム程度に形成することが可能になるためその光電変換効率の向上が図れる利点を有する方法であった。

【０００９】

【発明が解決しようとする課題】ところで、プラズマCVD法を適用した上記製造方法においてはn⁺シリコン層又はp⁺シリコン層の低温製膜とその薄膜化が図れることから上述した利点を有していたが、その反面、上記n⁺シリコン層又はp⁺シリコン層の製膜工程中において粉状の浮遊異物が製膜室内に多量に発生し易く、この浮遊異物が製膜途上のn⁺シリコン層又はp⁺シリコン層内に混入されてその膜特性を劣化させてしまう欠点があった。

【００１０】すなわち、プラズマCVD法を適用したこの製造方法においては製膜室内のプラズマ形成領域にプラズマ化された原料ガスが一様に分布しかつこのプラズマ化された原料ガスは励起状態にあるため、製膜室内の任意の空間において原料ガスが互いに反応してシリコンの粉状体を生成したり、基板以外の部位すなわち製膜室の内壁面においてプラズマ化された原料ガスが反応してシリコンが析出しこれが粉状体となって剥離する等粉状の浮遊異物が多量に発生し易い状態にある。

【００１１】また、プラズマCVD法においては製膜ガスであるSiH_4ガス等に加えてハロゲンガスを配合する場合があり、このハロゲン原子のエッチング作用により製膜室の内壁面や内部治具表面が腐食され易いためこ

の腐食面が剥離して上記浮遊異物に加わることになる。

【００１２】このため、プラズマCVD法を適用した上記製造方法においては上述した利点を有している反面、良質なn⁺シリコン層又はp⁺シリコン層を形成することが困難なためこれに起因して得られたBSF型太陽電池の光電変換効率も一定の限界を有する問題点があった。

【００１３】本発明はこのような問題点に着目してなされたもので、その課題とするところは、低温製膜条件で良質なn⁺シリコン層又はp⁺シリコン層が形成できる熱CVD法、光CVD法、及び、イオンプレーティング法を選択することにより光電変換効率が更に向上したBSF型太陽電池を安定して製造できる方法を提供することにある。

【００１４】

【課題を解決するための手段】すなわち、請求項１に係る発明は、n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法を前提とし、n型又はp型シリコン基板を配置した製膜室内にシリコン原子が含まれる製膜ガスとSiF_4ガス及びn型又はp型のドーパントガスを供給し、かつ、上記供給ガスを加熱されたシリコン基板近傍で熱分解させると共に、熱分解された製膜ガスのラジカル成分と上記SiF_4ガスとの反応により生じたフッ素系ラジカルをエッチング成分として作用させながらn型又はp型シリコン基板に上記n⁺又はp⁺シリコン層を形成することを特徴とするものであり、また、請求項２に係る発明は、n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法を前提とし、n型又はp型シリコン基板を配置した製膜室内に水素化珪素を主成分とする製膜ガスとSiH_nF_{4-n}（但しmは１～３）で示されるフッ素化シランガス及びn型又はp型のドーパントガスを供給し、かつ、上記供給ガスを加熱されたシリコン基板近傍で熱分解させると共に、フッ素化シランガスの熱分解により生じたフッ素系ラジカル、及び、熱分解された製膜ガスのラジカル成分が上記フッ素化シランガスと反応して生じたフッ素系ラジカルをエッチング成分として作用させながらn型又はp型シリコン基板に上記n⁺又はp⁺シリコン層を形成することを特徴とするものである。

【００１５】そして、請求項１に係る発明においてはハロゲン原子を放出するガスとして熱分解を受け難いSiF_4ガスが適用されており、また、請求項２に係る発明においてはハロゲン原子を放出するガスとして上記製膜

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ガスよりその熱分解温度が高いフッ素化シランガスを適用しているため、製膜室内の基板から離れた温度分布の低い領域においてはSiF_4及びフッ素化シランガスの熱分解が起り難く、その分、この領域のフッ素系ラジカル濃度は低い状態になっている。

【0016】従って、プラズマCVD法を適用した従来の製造方法に較べて、製膜室内の任意の空間において上記製膜ガスがフッ素系ラジカルと反応してシリコン粉状体を生成したり、あるいは、製膜室の内壁面や内部治具表面が上記フッ素系ラジカルの作用を受けて腐食される可能性が低いため、ハロゲン原子を放出するSiF_4又はフッ素化シランガスを適用しているにも拘らず製膜室内における浮遊異物の発生を防止することが可能となる。

【0017】一方、請求項1に係る発明において上記SiF_4ガスは熱分解を受けにくい反面、熱分解されたシラン化合物等製膜ガスのラジカル成分との反応によりその熱分解が促進されるため、上記ラジカル成分の多い領域、すなわちn型又はp型シリコン基板近傍領域において分解を受け易くこの領域に高濃度のフッ素系ラジカルが偏在することになる。また、請求項2に係る発明においも上記SiH_2F_2等フッ素化シランガスはn型又はp型シリコン基板近傍の高温領域において熱分解を受け易いと共に、熱分解された製膜ガスのラジカル成分（SiH_xラジカル、H系ラジカル等）との反応によりその分解が促進されるため、基板近傍領域に高濃度のフッ素系ラジカルが偏在することになる。

【0018】従って、このフッ素系ラジカルの作用によりn型又はp型シリコン基板上若しくは成長中のn^+又はp^+シリコン層に混入された不純物のみが選択的にエッチングを受けて取除かれることになるため、本来、この不純物を取除くための高温加熱処理が必要となる熱CVD法を適用しているにも拘らず請求項1又は2に係る発明においては基板加熱温度の低減が図れる。

【0019】尚、請求項1又は2に係る発明において製膜室内の基板近傍の空間部位に上記基板を加熱する発熱手段を設けると、製膜ガスの熱分解が促進されるため基板加熱温度を更に低減することが可能となる。請求項3に係る発明はこのような技術的理由に基づきなされている。

【0020】すなわち、請求項3に係る発明は、請求項1又は2記載の発明に係るBSF型太陽電池の製造方法を前提とし、製膜室内に配置されたn型又はp型シリコン基板近傍の空間部位に上記基板が覆われるように網状の発熱部材を配置したことを特徴とするものである。

【0021】そして、n型又はp型シリコン基板近傍の空間部位に配置される上記発熱部材とは、基板全面を覆うように配置されてもn^+又はp^+シリコン層の製膜に支障を来さないような形状を備え、かつ水素化珪素等の製膜ガスを基板近傍領域で熱分解させる程度に発熱する材

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料で構成されているもので、具体例としてタングステン、トリウムタングステン等から成る網状の熱フィラメントが挙げられる。

【0022】また、請求項1～3に係る発明の熱CVD法においては、製膜処理中にこの製膜室内の真空度を略一定に維持するためその下流側において継続して排気処理を行っており、エッチング作用に供されたフッ素系ラジカルあるいは余剰のフッ素系ラジカルは上記排気処理により製膜室から外部へ排除されている。

【0023】ここで、請求項1～3に係る発明においてn型又はp型シリコン基板との間でHL接合を形成するn^+シリコン層又はp^+シリコン層としては、n型又はp型ドーパントガスが導入されたアモルファスシリコン層、ポリシリコン層、あるいは、単結晶シリコン層が適用できる。この場合、内部抵抗を下げる観点からポリシリコン層よりはその抵抗値の低い単結晶シリコン層が望ましく、また、アモルファスシリコン層よりはその抵抗値の低いポリシリコン層が望ましい。

【0024】尚、n型のドーパントガスとしては元素周期率表第III族のSb（アンチモン）、As（ひ素）、及び、P（リン）等を含む化合物が適用でき、具体例としては、SbH_3、$SbCl_3$、AsH_3、As_2H_4、及び、PH_3等が挙げられる。また、p型のドーパントガスとしては元素周期率表第V族のGa（ガリウム）、B（ボロン）In（インジウム）、及び、Al（アルミニウム）等を含む化合物が適用でき、具体例としては、B_2H_6、$Ga(CH_3)_3$、$In(CH_3)_3$、及び、$Al(CH_3)_3$等が挙げられる。

【0025】また、請求項1又は3に係る発明においてシリコン原子が含まれる上記製膜ガスとしては、熱分解され易いSiH_4、Si_2H_6、及び、Si_3H_8等の水素化珪素やSiH_mX_{4-m}（但し、mは1～3、好ましくは2～3、XはCl又はF原子、好ましくはF原子である）で示されるハロゲン化シラン等が適用できる。尚、この製膜ガス内に水素ガスを添加してもよい，この水素系ラジカルもSiF_4ガスに作用してその分解を促進させるからである。ここで、製膜ガスとして後者のハロゲン化シランガスを適用した場合、このハロゲン化シランガスの配合割合が高過ぎると製膜室内に上述した浮遊異物が生ずることがある。従って、SiH_mX_{4-m}で示されるハロゲン化シランガスを適用する場合にはその配合割合を上記SiF_4より少なく設定することが望ましい。

【0026】また、請求項2又は3に係る発明において上記製膜ガスの主要部を構成する水素化珪素としては、SiH_4、Si_2H_6、及び、Si_3H_8等が適用できる。また、請求項1又は3に係る発明と同様、上記製膜ガス内に水素ガスを添加してもよい。この水素系ラジカルも上記SiH_2F_2等のフッ素化シランガスと反応しその熱分解を促進させるからである。

【0027】尚、請求項1～3に係る発明において上記

製膜ガス中に希釈ガスとして、ヘリウム、ネオン、アルゴン等の不活性ガスを加えてもよい。

【0028】そして、請求項1～3記載の発明に係るBSF型太陽電池の製造方法においては、製膜開始前における製膜室の真空度をこの製膜室内に不純物が若干残留する程度（10^{-5}Torr程度）に設定し、かつ、配置されたn型又はp型シリコン基板の温度を500℃～700℃程度に設定した後、少なくとも上記製膜ガスとSiF_4ガス及びn型又はp型のドーパントガスを供給するか、あるいは、少なくとも上記製膜ガスとSiH_mF_{4-m}（但しmは1～3）で示されるフッ素化シランガス及びn型又はp型のドーパントガスを供給して上記n型又はp型シリコン基板上にn⁺又はp⁺シリコン層を形成する。このとき、基板加熱温度を500℃～700℃程度の低温条件に設定しても上記フッ素系ラジカルのエッチング作用により不純物は選択的に除去され、また、浮遊異物の発生も殆ど起らずn⁺又はp⁺シリコン層内への混入が起こり難いため上記n⁺又はp⁺シリコン層の膜特性に悪影響を及ぼす可能性がほとんどない。

【0029】従って、光電変換効率が更に向上したBSF型太陽電池を安定して製造できる利点を有している。

【0030】次に、請求項4～5に係る発明は、請求項1～3に係る発明において n⁺又はp⁺シリコン層の製膜に適用された熱CVD法に代えて光CVD法及びイオンプレーティング法を適用したBSF型太陽電池の製造方法に関する。

【0031】まず、請求項4に係る発明は、n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法を前提とし、加熱されたシリコン基板面に上記n⁺又はp⁺シリコン層を光CVD法により形成することを特徴とするものである。

【0032】すなわち、この光CVD装置は、図5に示すように製膜室11と、この製膜室11内に石英窓30を介し配設された紫外線照射ランプ31と、この紫外線照射ランプ31の対向側に設けられヒータ15が組込まれた基板ホルダー13と、製膜室11内へSiH_4等の製膜ガスと、適宜ドーパントガスと、水素ガス等を供給するガス供給源16、17と、調圧弁19を介して接続された減圧ポンプ18とでその主要部が構成されており、上記製膜室11内にn型又はp型シリコン基板14を配置すると共に、このシリコン基板14を500～600℃程度に加熱した後、上記ガス供給源16、17から製膜ガス、ドーパントガス等を供給し、かつ、紫外線を照射して上記n型又はp型シリコン基板14上にn⁺又はp⁺シリコン層を形成する方法である。

【0033】そして、この請求項4記載の発明に係る製造方法によれば、低温製膜条件で膜質良好なn⁺又はp⁺シリコン層をp型シリコン基板14上に形成できるため、請求項1～3に係る発明と同様、光電変換効率が更に向上したBSF型太陽電池を安定して製造できる利点を有している。

【0034】次に、請求項5に係る発明は、n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法を前提とし、n型又はp型シリコン基板を配置した製膜室内にSiH_mF_{4-m}（但しmは1～3）で示されるフッ素化シランガス又はSiF_4ガスを供給し、かつ、このフッ素化シランガス又はSiF_4ガスが存在する条件下においてイオンプレーティング法により加熱されたシリコン基板面に上記n⁺又はp⁺シリコン層を形成することを特徴とするものである。

【0035】すなわち、このイオンプレーティング装置は、図6に示すように製膜室11と、この製膜室11内の下方側に設けられ製膜材料であるドーパント混入のSiターゲットが収容された抵抗加熱蒸発源40と、この抵抗加熱蒸発源40の上方側空間部に設けられたRFコイル41と、上記抵抗加熱蒸発源40からの供給量を調整するシャッター42と、製膜室11内の上方側に設けられシリコン基板14を600～700℃程度に加熱する基板ホルダー43とでその主要部が構成されており、かつ、RFコイル41には高周波電源44が、また、基板ホルダー43には正の高圧電源（図示せず）が接続されている。そして、上記製膜室11内にn型又はp型シリコン基板14を配置し、かつ、この製膜室11内にフッ素化シランガス又はSiF_4ガスを供給すると共に、上記シリコン基板14を600～700℃程度に加熱した後、抵抗加熱蒸発源40からドーパントとシリコンを蒸発させてn型又はp型シリコン基板14上にn⁺又はp⁺シリコン層を形成する方法である。

【0036】この請求項5に係る発明においても、請求項1～3に係る発明と同様、ハロゲン原子を放出するガスとして熱分解を受け難いフッ素化シランガス又はSiF_4ガスが適用されているためn型又はp型シリコン基板近傍領域において高濃度のフッ素系ラジカルが偏在することになる。すなわち、n型又はp型シリコン基板の近傍領域においては熱分解されたシリコン分子のラジカル成分が遍在しているため、このラジカル成分と上記フッ素化シランガス又はSiF_4ガスとの反応により高濃度のフッ素系ラジカルが偏在している。そして、このフッ素系ラジカルの作用によりn型又はp型シリコン基板上若しくは成長中のn⁺又はp⁺シリコン層に混入された不純物のみが選択的にエッチングを受けて取除かれることになるため、低温製膜条件で膜質良好なn⁺又はp⁺シ

リコン層をn型又はp型シリコン基板上に形成することが可能となり、請求項1～4に係る発明と同様、光電変換効率が更に向上したBSF型太陽電池を安定して製造できる利点を有している。

【0037】

【作用】請求項1に係る発明によれば、ハロゲン原子を放出するガスとして熱分解を受け難いSiF_4ガスが適用されており、このガスが熱分解され難い分、製膜室内におけるフッ素系ラジカル濃度は低い状態になっているため、プラズマCVD法を適用した従来の製造方法に較べて製膜室内の任意の空間において製膜ガスがフッ素系ラジカルと反応してシリコン粉状体を生成したり、あるいは、製膜室の内壁面や内部治具表面が上記フッ素系ラジカルの作用を受けて腐食される可能性が極端に低くなり、ハロゲン原子を放出するSiF_4ガスを適用しているにも拘らず製膜室内における浮遊異物の発生を確実に防止することが可能となる。

【0038】一方、上記SiF_4ガスは製膜ガスのラジカル成分（SiH_xラジカル、H系ラジカル等）との反応によりその熱分解が促進されることからこのラジカル成分の多いn型又はp型シリコン基板近傍領域に高濃度のフッ素系ラジカルが偏在し易くなり、このフッ素系ラジカルの作用により上記基板上若しくは成長中のn^+又はp^+シリコン層に混入された不純物のみが選択的にエッチングを受けて取除かれるため、本来、この不純物を取除くための高温加熱処理が必要となる熱CVD法を適用しているにも拘らず基板加熱温度の低減を図ることが可能となる。

【0039】また、請求項2に係る発明によれば、ハロゲン原子を放出するガスとして上記製膜ガスよりその熱分解温度が高いフッ素化シランガスを適用しており、製膜室内の基板から離れた温度分布の低い領域においては上記製膜ガスに較べてこのフッ素化シランガスの熱分解が起り難くフッ素系ラジカル濃度は低い状態になっているため、プラズマCVD法を適用した従来の製造方法に較べて製膜室内の任意の空間において製膜ガスがフッ素系ラジカルと反応してシリコン粉状体を生成したり、あるいは、製膜室の内壁面や内部治具表面が上記フッ素系ラジカルの作用を受けて腐食される可能性が低くなり、ハロゲン原子を放出するフッ素化シランガスを適用しているにも拘らず製膜室内における浮遊異物の発生を防止することが可能となる。

【0040】一方、上記フッ素化シランガスはn型又はp型シリコン基板近傍の高温領域において熱分解を受け易いと共に熱分解された製膜ガスのラジカル成分（SiH_xラジカル、H系ラジカル等）との反応によりその分解が促進されることからn型又はp型シリコン基板近傍領域に高濃度のフッ素系ラジカルが偏在し易くなり、このフッ素系ラジカルの作用により上記基板上若しくは成長中のn^+又はp^+シリコン層に混入された不純物のみが

選択的にエッチングを受けて取除かれるため、請求項1に係る発明と同様、熱CVD法を適用しているにも拘らず基板加熱温度の低減を図ることが可能となる。

【0041】更に、請求項3に係る発明によれば、製膜室内に配置されたn型又はp型シリコン基板近傍の空間部位に上記基板が覆われるように網状の発熱部材を配置していることから、この発熱部材が発する熱エネルギの作用により上記基板近傍領域においては製膜ガスの熱分解が著しく促進されているため、上記フッ素系ラジカルのエッチング作用と相乗して基板加熱温度を更に低減させることが可能となる。

【0042】次に、請求項4に係る発明によれば、加熱されたシリコン基板面にn^+又はp^+シリコン層を光CVD法により製膜しているため、低温製膜条件で膜質良好なn^+又はp^+シリコン層を上記n型又はp型シリコン基板上に形成することが可能となる。

【0043】また、請求項5に係る発明によれば、フッ素化シランガス又はSiF_4ガスが存在する条件下においてイオンプレーティング法により加熱されたシリコン基板面に上記n^+又はp^+シリコン層を製膜しているため、低温製膜条件で膜質良好なn^+又はp^+シリコン層を上記n型又はp型シリコン基板上に形成することが可能となる。

【0044】

【実施例】以下、本発明の実施例について詳細に説明するとこの実施例に係るBSF型太陽電池は、従来同様、図1に示すようにn^-単結晶シリコン基板（100配向、比抵抗1～10Ω・cm）1と、このシリコン基板1の光入射側面に設けられシリコン基板1との間でpn接合を形成するp型アモルファスシリコン又はポリシリコン層2と、このp型アモルファスシリコン又はポリシリコン層2上に一様に成膜されITO（酸化インジウム錫）にて形成された反射防止層3と、この反射防止層3上に設けられ銀ペーストにて形成された櫛歯状電極4と、上記シリコン基板1の反対側面に設けられシリコン基板1との間でHL接合を形成するn^+アモルファスシリコン又はポリシリコン層5と、このn^+アモルファスシリコン又はポリシリコン層5の背面側に一様に設けられアルミニウムにて形成された裏面電極6とでその主要部が構成されているものである。

【0045】そしてこのBSF型太陽電池は以下の工程に従って製造されたものである。

【0046】［実施例1］図3はこの実施例で適用された熱CVD装置の概略構成を示した説明図で、図中11は製膜室、13はヒータ15が組込まれた基板ホルダー、14はこの基板ホルダー13に取付けられたn^-単結晶シリコン基板、16、17は原料ガスの供給源、及び、18は調圧弁19を介し製膜室11に接続された減圧ポンプをそれぞれ示している。

【0047】まず、この製膜室11を排気して1×10

$^{-6}$Torrの真空にし、次いで、この製膜室11内に下記原料ガスを導入すると共に下記の製膜条件に従ってその一面側にp型ポリシリコン層2を、他方の面にn$^+$ポリシリコン層5をそれぞれ製膜した（図2A参照）。

【0048】（p型ポリシリコン層2の製膜条件）

原料ガスの種類と組成：B_2H_6／SiH_4／SiF_4＝0．1／10／500

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：700℃

（n$^+$ポリシリコン層5の製膜条件）

原料ガスの種類と組成：PH_3／SiH_4／SiF_4＝0．1／10／330

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：700℃

次に、図2（B）に示すようにスパッタリング法にてp型ポリシリコン層2上にITOを着膜させて反射防止層3を形成し、かつ、この面上に銀ペーストにより櫛歯状電極4を形成すると共に、n$^+$ポリシリコン層5の背面側にスパッタリング法によりアルミニウムを一様に製膜して裏面電極6を形成し実施例に係るBSF型太陽電池を求めた（図1参照）。

【0049】そして、この電池の特性を調べたところ、n$^+$ポリシリコン層の製膜手段にプラズマCVD法を適用した従来のものの特性が0．57V～0．58V、35mA～37mAであったのに対し、この実施例に係るBSF型太陽電池の特性は0．59V～0．60V、37mA～39mAであった。

【0050】［実施例2］p型ポリシリコン層2とn$^+$ポリシリコン層5に代えてp型アモルファスシリコン層とn$^+$アモルファスシリコン層を適用し、かつ、その製膜条件が下記である点を除き実施例1と略同一である。

【0051】そして、この実施例に係るBSF型太陽電池においてもその特性が0．59V～0．60V、37mA～39mAであり従来例に較べて良好であった。

【0052】（p型アモルファスシリコン層2の製膜条件）

原料ガスの種類と組成：B_2H_6／SiH_4／SiF_4／H_2＝0．1／10／100／400

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：600℃

（n$^+$アモルファスシリコン層5の製膜条件）

原料ガスの種類と組成：PH_3／SiH_4／SiF_4／H_2＝0．1／10／100／400

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mlorr～1lorr

n$^-$単結晶シリコン基板の加熱温度：600℃

［実施例3］p型アモルファスシリコン層2とn$^+$アモルファスシリコン層5の製膜条件が下記である点を除き実施例2と略同一である。

【0053】そして、この実施例に係るBSF型太陽電池においてもその特性が0．58V～0．59V、36mA～38mAであり従来例に較べて良好であった。

【0054】（p型アモルファスシリコン層2の製膜条件）

原料ガスの種類と組成：$In(CH_3)_3$／SiH_4／SiH_2F_2／アルゴン＝0．1／10／100／400

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：650℃

（n$^+$アモルファスシリコン層5の製膜条件）

原料ガスの種類と組成：$SbCl_3$／SiH_4／SiH_2F_2／アルゴン＝0．1／10／100／400

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：650℃

［実施例4］p型アモルファスシリコン層2とn$^+$アモルファスシリコン層5の製膜条件が下記である点を除き実施例2と略同一である。

【0055】そして、この実施例に係るBSF型太陽電池においてもその特性が0．58V～0．59V、36mA～38mAであり従来例に較べて良好であった。

【0056】（p型アモルファスシリコン層2の製膜条件）

原料ガスの種類と組成：$Al(CH_3)_3$／SiH_4／SiH_2F_2／H_2／アルゴン＝0．1／10／100／300／100

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：700℃

（n$^+$アモルファスシリコン層5の製膜条件）

原料ガスの種類と組成：PH_3／SiH_4／SiH_2F_2／H_2／アルゴン＝0．1／10／100／300／100

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：700℃

［実施例5］図3に示された装置に代えて図4に示すように基板近傍の空間部位にタングステンの熱フィラメント20が配置された熱CVD装置を適用すると共に、上記p型ポリシリコン層2とn$^+$ポリシリコン層5の製膜条件が下記である点を除き実施例1と略同一である。

【0057】そして、この実施例に係るBSF型太陽電池においてもその特性が0．59V～0．60V、37mA～39mAであり従来例に較べて良好であった。

【0058】（p型ポリシリコン層2の製膜条件）

原料ガスの種類と組成：$Ga(CH_3)_3$／SiH_4／SiF_4／H_2＝0．1／10／100／400

原料ガスの供給速度：5sccm～100sccm
原料ガスの圧力：50mtorr～1torr
n⁻単結晶シリコン基板の加熱温度：650℃
（n⁺ポリシリコン層5の製膜条件）
原料ガスの種類と組成：AsH_3／SiH_4／SiF_4／H_2＝0．1／10／100／400
原料ガスの供給速度：5sccm～100sccm
原料ガスの圧力：50mtorr～1torr
n⁻単結晶シリコン基板の加熱温度：650℃
［実施例6］図4に示された熱CVD装置を適用した点と、p型ポリシリコン層2とn⁺ポリシリコン層5の製膜条件が下記である点を除き実施例1と略同一である。
【0059】そして、この実施例に係るBSF型太陽電池においてもその特性が0．58V～0．59V、36mA～38mAであり従来例に較べて良好であった。
【0060】（p型ポリシリコン層2の製膜条件）
原料ガスの種類と組成：B_2H_6／SiH_4／SiH_2F_2／H_2／アルゴン＝0．1／10／100／400／100
原料ガスの供給速度：5sccm～100sccm
原料ガスの圧力：50mtorr～1torr
n⁻単結晶シリコン基板の加熱温度：650℃
（n⁺ポリシリコン層5の製膜条件）
原料ガスの種類と組成：PH_3／SiH_4／SiH_2F_2／H_2／アルゴン＝0．1／10／100／400／100
原料ガスの供給速度：5sccm～100sccm
原料ガスの圧力：50mtorr～1torr
n⁻単結晶シリコン基板の加熱温度：650℃
［実施例7］図5に示された光CVD装置を適用した点と、p型アモルファスシリコン層2とn⁺アモルファスシリコン層5の製膜条件が下記である点を除き実施例2と略同一である。
【0061】そして、この実施例に係るBSF型太陽電池においてもその特性が0．59V～0．60V、37mA～39mAであり従来例に較べて良好であった。
【0062】（p型アモルファスシリコン層2の製膜条件）
製膜室内の圧力：1～10mTorr
原料ガスの種類と組成：B_2H_6／SiH_4／H_2＝0．1／10／300
原料ガスの供給速度：5sccm～100sccm
原料ガスの圧力：50mtorr～1torr
紫外光の照射光源：Hgランプ
n⁻単結晶シリコン基板の加熱温度：600℃
（n⁺アモルファスシリコン層5の製膜条件）
製膜室内の圧力：1～10mTorr
原料ガスの種類と組成：PH_3／SiH_4／H_2＝0．1／10／300
原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr
紫外光の照射光源：Hgランプ
n⁻単結晶シリコン基板の加熱温度：600℃
［実施例8］図6に示されたイオンプレーティング装置を適用し、かつ、このイオンプレーティング装置内にSiF_4ガスを供給した点と、p型ポリシリコン層2とn⁺ポリシリコン層5の製膜条件が下記である点を除き実施例1と略同一である。
【0063】そして、この実施例に係るBSF型太陽電池においてもその特性が0．58V～0．59V、36mA～38mAであり従来例に較べて良好であった。
【0064】（p型ポリシリコン層2の製膜条件）
製膜室内の圧力：1～10mTorr
ターゲット：B_2H_6がドープされたSi
RFコイルへの投入電力：50～200W
n⁻単結晶シリコン基板の加熱温度：700℃
（n⁺ポリシリコン層5の製膜条件）
製膜室内の圧力：1～10mTorr
ターゲット：PH_3がドープされたSi
RFコイルへの投入電力：50～200W
n⁻単結晶シリコン基板の加熱温度：700℃
【0065】
【発明の効果】請求項1～2に係る発明によれば、ハロゲン原子を放出するSiF_4ガスあるいはフッ素化シランガスを適用しているにも拘らず製膜室内における浮遊異物の発生を確実に防止でき、かつ熱CVD法を適用しているにも拘らず基板加熱温度の低減を図ることが可能となる。
【0066】また、請求項3に係る発明によれば、製膜室内に配置されたn型又はp型シリコン基板近傍の空間部位に設けられた発熱部材の作用により製膜ガスの熱分解が著しく促進されるため、フッ素系ラジカルのエッチング作用と相乗して基板加熱温度を更に低減させることが可能となる。
【0067】従って、低温製膜条件で膜質良好なn⁺又はp⁺シリコン層をn型又はp型シリコン基板上に形成することが可能になるため、光電変換効率の高いBSF型太陽電池を安定して製造できる効果を有している。
【0068】次に、請求項4に係る発明によれば、加熱されたシリコン基板面に上記n⁺又はp⁺シリコン層を光CVD法により製膜し、また、請求項5に係る発明によれば、フッ素化シランガス又はSiF_4ガスが存在する条件下においてイオンプレーティング法により加熱されたシリコン基板面に上記n⁺又はp⁺シリコン層を製膜しているため、請求項1～3に係る発明と同様、低温製膜条件で膜質良好なn⁺又はp⁺シリコン層をn型又はp型シリコン基板上に形成することが可能となり、光電変換効率の高いBSF型太陽電池を安定して製造できる効果を有している。
【図面の簡単な説明】

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【図1】実施例に係るBSF型太陽電池の断面図。

【図2】図2（A）～（B）はBSF型太陽電池の製造工程図。

【図3】実施例1において適用された熱CVD装置の説明図。

【図4】実施例5において適用された熱CVD装置の説明図。

【図5】実施例7において適用された光CVD装置の説明図。

【図6】実施例8において適用されたイオンプレーティング装置の説明図。

【図7】従来の太陽電池の斜視図。

【図8】従来の太陽電池の断面図。

【図9】従来の太陽電池の構造をモデル的に記載した構造概念図。

【図10】従来の太陽電池のエネルギーバンド図。

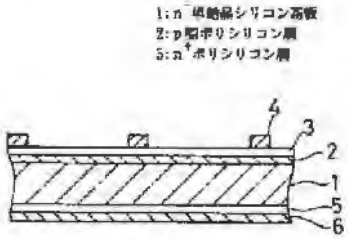
【符号の説明】

1　n⁻ 単結晶シリコン基板

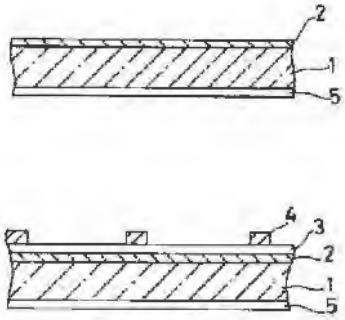
2　p型ポリシリコン層

5　n⁺ ポリシリコン層

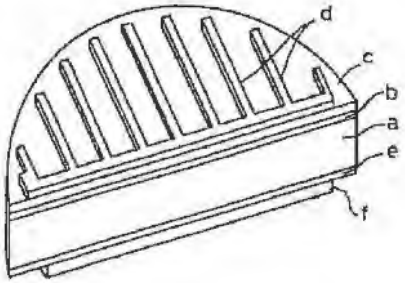
【図1】



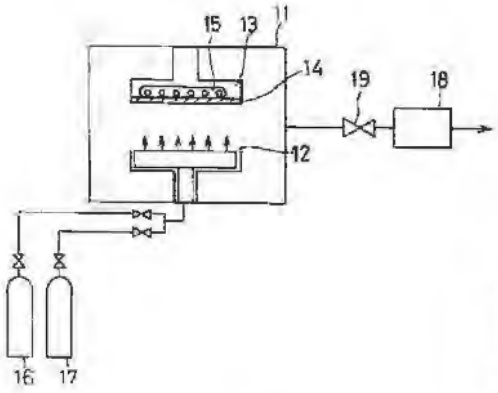
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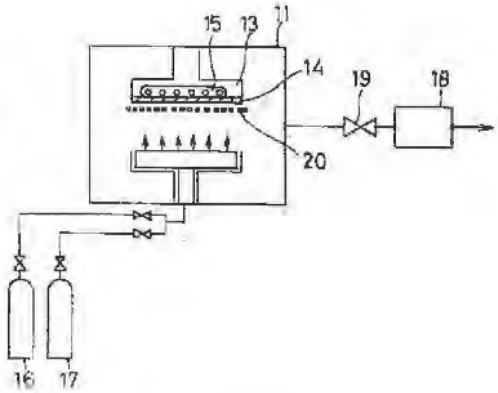
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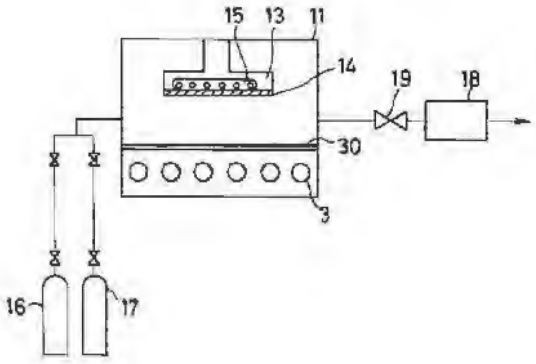
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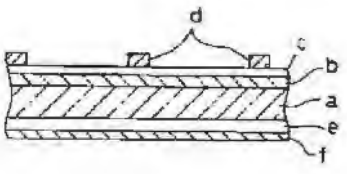
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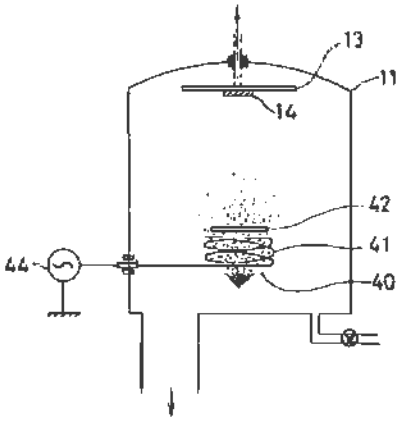
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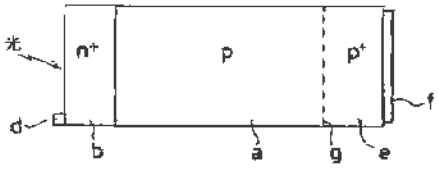
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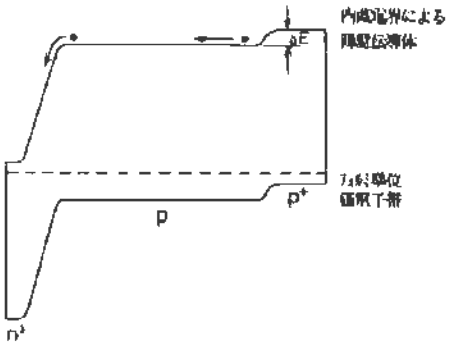
【図6】



【図9】



【図10】



Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	14504771
Filing Date	02-Oct-2014
First Named Inventor	Peter COUSINS
Attorney Docket Number	10031 004211
Title of Invention	FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
SunPower Corporation	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

8222516

8207444

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

- (◉) Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.
- ( ) I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

- ( ) Small Entity
- ( ) Micro Entity
- (◉) Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

- (◉) An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

  Registration Number 40909

- ( ) A sole inventor
- ( ) A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application
- ( ) A joint inventor; all of whom are signing this request

Signature	/Patrick D. Benedicto/
Name	PATRICK D BENEDICTO

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 14504771

Filing Date: 02-Oct-2014

Applicant/Patent under Reexamination: COUSINS et al.

Electronic Terminal Disclaimer filed on September 19, 2016

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Docket No. 10031.004211
Response To Office Action

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:

Peter John COUSINS

Application No.: 14/504,771 Examiner: PILLAY, DEVINA

Filing Date: October 2, 2014 Art Unit: 1755

Title: FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

RESPONSE TO OFFICE ACTION AND AMENDMENT

INTRODUCTORY COMMENTS

This paper is responsive to the office action mailed on June 29, 2016 ("last office action").

Please amend the above-identified application as follows:

AMENDMENTS TO THE SPECIFICATION

A. Please insert the following section on page 1 of the specification, after the "REFERENCE TO RELATED APPLICATIONS" and before the "BACKGROUND OF THE INVENTION".

> STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT
>
> The invention described herein was made with Governmental support under contract number DE-FC36-07GO17043 awarded by the United States Department of Energy. The Government may have certain rights in the invention.

B. Please replace the paragraph beginning on page 1, line 6 with the following paragraph:

> This application is a continuation of U.S. Application No. 13/495,577, filed on June 13, 2012, now U.S. Patent No. 8,878,053, which is a divisional of U.S. Application No. 12/070,742, filed on February 20, 2008, now U.S. Patent No. 8,222,516. The just-mentioned disclosures are incorporated herein by reference in their entirety.

AMENDMENTS TO THE CLAIMS

1 (Currently amended) A solar cell, comprising:

a substrate having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

a first tunnel dielectric disposed over the back surface of the substrate;

an emitter disposed over the first tunnel dielectric, the emitter forming a backside junction with the substrate;

a front electrode disposed over [[a]]the front surface of the substrate; and

a back electrode disposed over [[a]]the back surface of the substrate.

2. (Original) The solar cell of claim 1, wherein the emitter is a polysilicon emitter.

3. (Original) The solar cell of claim 1, wherein the substrate is a monocrystalline silicon substrate.

4. (Original) The solar cell of claim 1, wherein the first tunnel dielectric is a tunnel oxide.

5. (Canceled)

6. (Currently amended) The solar cell of claim 1, further comprising a second tunnel dielectric disposed on ~~an opposite side of~~ the front surface of the substrate ~~than the first tunnel dielectric~~.

7. (Original) The solar cell of claim 1, wherein the back electrode includes silver.

8. (Original) The solar cell of claim 1, further comprising an antireflective layer disposed over the front surface of the substrate.

9. (Currently amended) A solar cell, comprising:

a substrate having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

an emitter over [[a]]the back surface of the substrate, the emitter forming a backside junction with the substrate;

a first dielectric between the emitter and the back surface;

a front electrode disposed on [[a]]the front surface of the substrate ~~solar cell~~; and

a back electrode disposed on [[a]]the back surface of the substrate ~~solar cell~~.

10. (Original) The solar cell of claim 9, wherein the emitter is a polysilicon emitter.

11. (Original) The solar cell of claim 9, wherein the substrate is a monocrystalline silicon substrate.

12. (Original) The solar cell of claim 9, wherein the first dielectric is an oxide.

13. (Currently amended) The solar cell of claim 9, further comprising a second dielectric disposed on ~~an opposite side~~ the front surface of the substrate ~~than the first dielectric~~.

14. (Original) The solar cell of claim 9, wherein the back electrode includes silver.

15-20. (Canceled)

REMARKS

With the above amendments, claims 1-4 and 6-14 remain in the application. Claims 5 and 15-20 are canceled without prejudice.

Claim amendments have been made to expedite prosecution. Applicant expressly reserves the right to pursue the original version of an amended claim in a continuing application.

Terminal Disclaimer

An eTerminal Disclaimer has been submitted to obviate the nonstatutory double patenting rejection that is based on US 8,207,444 and US 8,222,516.

Claim Rejection -- 35 U.S.C. §112

Claim 9 is amended to address the rejection under pre-AIA 35 U.S.C. §112, second paragraph.

Claim Rejection -- 35 U.S.C. § 103

Claims 1-4 and 6-14 are rejected under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Okayasu (JP 07-106611) in view of Ohmni (US 5,516,092) and Foglietti (US 2002/0142500). The rejection is respectfully traversed.

Claim 1 is patentable over the combination of Okayasu, Omnhi, and Foglietti at least for reciting: "an emitter disposed over the first tunnel dielectric, the emitter forming a backside junction with the substrate."

In the embodiment of claim 1, the emitter is disposed over the tunnel dielectric and forms a hackside junction with the substrate. It is respectfully submitted that this feature of claim 1 is not taught or suggested by the combination of Okayasu, Ohmni, and Foglietti.

To the extent the applicant understands the machine translation of the disclosure of Okayasu, Okayasu FIG. 1 shows a solar cell with an N-type substrate 1, a layer 2 on the front side, an N+ BSF layer 5, an electrode 6 on the backside, and an electrode 4 on the front side. It is respectfully submitted that because the layer 5 is a back surface field layer, ***the layer 5 is necessarily on the back surface and has the same polarity as the substrate 1***. Accordingly, the BSF layer 5 cannot form a backside junction with the substrate, and thus cannot correspond to the recited emitter. It is respectfully submitted that Ohmni and Foglietti do not add to Okayasu regarding the recited emitter feature of claim 1.

Therefore, it is respectfully submitted that claim 1 is patentable over the combination of Okayasu, Ohmni, and Foglietti.

Claims 2-4 and 6-8 are patentable over the combination of Okayasu, Ohmni, and Foglietti at least for depending from claim 1.

Claim 9 is patentable over the combination of Okayasu, Ohmni, and Foglietti at least for reciting: "an emitter over the back surface of the substrate, the emitter forming a backside junction with the substrate; a first dielectric between the emitter and the back surface." It is respectfully submitted that the combination of Okayasu, Ohmni, and Foglietti does not teach or suggest a solar cell with an emitter that is over a dielectric that forms a backside junction with the substrate.

Claims 10-14 are patentable over the combination of Okayasu, Ohmni, and Foglietti at least for depending from claim 9.

Claims 1-4 and 6-14 are rejected under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Okayasu in view of Borden (WO 2009/094578). The rejection is respectfully traversed.

Claim 1 is patentable over the combination of Okayasu and Borden at least for reciting: "an emitter disposed over the first tunnel dielectric, the emitter forming a backside junction with the substrate." It is respectfully submitted that Okayasu does not disclose an emitter that is disposed over a tunnel dielectric and forms a backside junction with the substrate. Instead, Okayasu discloses a solar cell with a back surface field layer, which is necessarily a back surface layer that has the same polarity as the substrate. It is

respectfully submitted that Borden does not add to Okayasu regarding the recited emitter feature of claim 1.

Claims 2-4 and 6-8 are patentable over the combination of Okayasu and Borden at least for depending from claim 1.

Claim 9 is patentable over the combination of Okayasu and Borden least for reciting: "an emitter over the back surface of the substrate, the emitter forming a backside junction with the substrate; a first dielectric between the emitter and the back surface." It is respectfully submitted that the combination of Okayasu and Borden does not teach or suggest a solar cell with an emitter that is over a dielectric that forms a backside junction with the substrate.

Claims 10-14 are patentable over the combination of Okayasu and Borden at least for depending from claim 9.

Conclusion

For at least the above reasons, it is believed that the pending claims are in condition for allowance. The Examiner is invited to telephone the undersigned for any questions and to resolve any remaining concerns regarding allowability of the present application.

Respectfully submitted,

Dated: SEPT. 19, 2016

Patrick Benedicto

Patrick D. Benedicto, Reg. No. 40,909
Okamoto & Benedicto LLP
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San Jose, CA 95164
Tel.: (408)436-2112
Fax.: (408)436-2114



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/504,771	10/02/2014	Peter John COUSINS	10031.004211	3342

74254 7590 10/26/2016

Okamoto & Benedicto LLP
P.O. Box 641330
San Jose, CA 95164-1330

EXAMINER
PILLAY, DEVINA

ART UNIT	PAPER NUMBER
1757	

MAIL DATE	DELIVERY MODE
10/26/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/504,771	Applicant(s) COUSINS, PETER JOHN	
	Examiner DEVINA PILLAY	Art Unit 1757	AIA (First Inventor to File) Status No

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/09/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-4 and 6-14* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-4 and 6-14* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Rejections - 35 USC § 103

2. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under pre-AIA 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of pre-AIA 35 U.S.C. 103(c) and potential pre-AIA 35 U.S.C. 102(e), (f) or (g) prior art under pre-AIA 35 U.S.C. 103(a).

5. Claims 1-4 and 6-14 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Meier (US 6,262,359) in view of Okayasu (JP 07-106611, Machine Translation) in view of Ohmi (US 5,563,092) in further view of Foglietti (US 2002/0142500 A1).

Regarding claims 1-4, 6, and 9-13, Meier discloses a solar cell comprising (see Fig. 3D, C5/L38-C6/L55):

a substrate (218 n-type) having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

an emitter (220 p-type) forming a backside junction with the substrate;

a front electrode disposed over the front surface of the substrate (212);

a back electrode disposed over the back surface of the substrate (222).

However, Meier does not disclose that the emitter is a polysilicon emitter and that there is a first tunnel dielectric formed between the emitter and the back surface of the substrate.

Okayasu discloses that instead of forming an emitter or surface field from a portion of a substrate which is doped an emitter can be formed using a doped polysilicon layer ([0005][0009]) and by forming an emitter or surface field this way the thickness can be more accurately controlled and it prevent generation of floating foreign matter.

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the method of forming the emitter and front surface field from a portion of a substrate of Meier and instead forming the emitter and front surface field by using a doped polysilicon layer as disclosed by Okayasu because the thickness can be more accurately controlled and it prevent generation of floating foreign matter.

Foglietti discloses that polycrystalline growth directly on crystalline silicon results in partial realignment of the polycrystalline grains and to suppress this effect a thin oxide can be grown similar to that disclosed by Ohmi ([0046]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the solar cell of modified Meier by providing a thin tunneling oxide between the emitter layer and the substrate and the FSF layer and the substrate because as disclosed by Ohmi and Foglietti it suppresses realignment of polysilicon emitter and BSF layers.

Regarding claims 7 and 14, modified Meier discloses all of the claim limitations as set forth above.

However, Meier does not disclose that the electrode that is in contact with the p-type polysilicon layer is silver.

Okayasu discloses that the back electrode on the polysilicon emitter is formed of a silver electrode [0044].

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the aluminum electrode of Meier with the silver electrode of

Okayasu because one of ordinary skill in the art would have been able to carry out such a substitution, and the results would be reasonably predictable.

Regarding claim 8, modified Meier discloses all of the claim limitations as set forth above.

In addition, Meier discloses an antireflection layer (214) disposed over the top surface of the substrate (C6/L20-25).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEVINA PILLAY whose telephone number is (571)270-

1180. The examiner can normally be reached on Monday thru Friday 7:30am -5:00pm (EST). Examiner Fax Number is (571)-270-2180.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey T. Barton can be reached on 571-272-1307. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DEVINA PILLAY/
Primary Examiner, Art Unit 1757

Notice of References Cited	Application/Control No. 14/504,771	Applicant(s)/Patent Under Reexamination COUSINS, PETER JOHN	
	Examiner DEVINA PILLAY	Art Unit 1757	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-6,262,359 B1	07-2001	Meier; Daniel L.	H01L31/022425	136/255
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14504771	COUSINS, PETER JOHN
	Examiner	Art Unit
	DEVINA PILLAY	1755

CPC- SEARCHED		
Symbol	Date	Examiner
H01L31/0236 H01L31/0745 H01L31/1804	6/8/2016	DP
H01L31/022425 H01L31/068 H01L31/182 H01L31/056	6/8/2016	DP
Y02E10/52 Y02P70/521 Y02E10/547	6/8/2016	DP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor name search in PALM	6/8/2016	DP
EAST Text Search (See Search History)	6/8/2016	DP
Updated Inventor name search in PALM	10/5/2016	DP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14504771	COUSINS, PETER JOHN
	Examiner	**Art Unit**
	DEVINA PILLAY	1755

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/17/2016	06/08/2016	10/05/2016						
	1	÷	✓	✓						
	2	÷	✓	✓						
	3	÷	✓	✓						
	4	÷	✓	✓						
	5	÷	✓	-						
	6	÷	✓	✓						
	7	÷	✓	✓						
	8	÷	✓	✓						
	9	÷	✓	✓						
	10	÷	✓	✓						
	11	÷	✓	✓						
	12	÷	✓	✓						
	13	÷	✓	✓						
	14	÷	✓	✓						
	15	÷	N	-						
	16	÷	N	-						
	17	÷	N	-						
	18	÷	N	-						
	19	÷	N	-						
	20	÷	N	-						

Doc Code: AP.PRE.REQ

PTO/AIA/33 (03-13)
Approved for use through 07/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 10031.004211

I hereby certify that this correspondence is being facsimile transmitted to the USPTO, EFS-Web transmitted to the USPTO, or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on 12/16/2016

Signature /Patrick D. Benedicto/

Typed or printed name PATRICK D. BENEDICTO

Application Number	Filed
14/504,771	10/02/2014

First Named Inventor: Peter John COUSINS

Art Unit	Examiner
1757	PILLAY, DEVINA

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s)
Note: No more than five (5) pages may be provided.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 40,909

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

/Patrick D. Benedicto/
Signature

PATRICK D. BENEDICTO
Typed or printed name

408.436 2110
Telephone number

December 16, 2016
Date

NOTE. This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ARGUMENTS

Claims 1-4 and 6-14 remain in the application and stand rejected. Reconsideration of the rejection is respectfully requested in light of the following reasons.

Claim Rejection -- 35 U.S.C. § 103

Claims 1-4 and 6-14 are rejected under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Meier (US 6,262,359), in view of Okayasu (JP 07-106611), in view of Ohmi (US 5,563,092), and further in view of Foglietti (US 2002/0142500). The rejection is respectfully traversed.

Claim 1 is patentable over the combination of Meier, Okayasu, Ohmi, and Foglietti at least for reciting: "an emitter disposed over the first tunnel dielectric, the emitter forming a backside junction with the substrate."

In the embodiment of claim 1, the emitter is disposed over the tunnel dielectric and forms a backside junction with the substrate. It is respectfully submitted that this feature of claim 1 is not taught or suggested by the combination of Meier, Okayasu, Ohmi, and Foglietti.

The final office action suggests that in the cited combination, Meier discloses the recited backside junction. Meier FIG. 3D is reproduced below for ease of discussion.

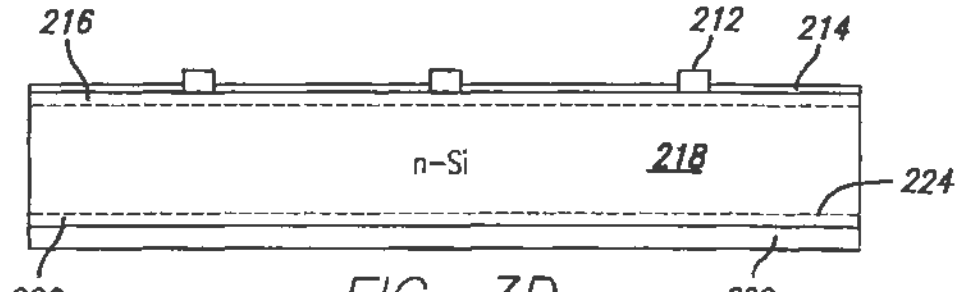


FIG. 3D

Meier discloses a solar cell with an aluminum alloy back junction (Meier, Title). More specifically, Meier discloses forming a p+ layer 220 ("emitter") that forms a backside junction with the n-Si base layer 218 ("substrate") within the base layer 218 by doping using the aluminum contact layer 222 (Meier, col. 6, lines 51-54). That is, the main

teaching of Meier is to form an aluminum alloy back junction by forming the p+ layer 220 within the substrate by diffusion into the substrate using the aluminum alloy electrode, thereby providing a strongly doped p-type emitter (Meier, abstract). Accordingly, Meier does not teach an emitter over a tunnel oxide and that forms a backside junction with the substrate. In Meier, the emitter that forms a backside junction with the substrate is ***within the substrate*** and ***in contact with the electrode***. There can be no intervening layer (such as a tunnel dielectric) between the emitter and the electrode because of the required diffusion of aluminum from the electrode to the emitter.

Okayasu does not cure the deficiencies of Meier. To the extent the appellant understands the machine translation of the disclosure of Okayasu, Okayasu FIG. 1 shows a solar cell with an N-type substrate 1, a layer 2 on the front side, an N+ BSF layer 5, an electrode 6 on the backside, and an electrode 4 on the front side. It is respectfully submitted that because the layer 5 is a back surface field (BSF) layer, the layer 5 is necessarily on the back surface and has the same polarity as the substrate 1. Accordingly, ***the BSF layer 5 cannot form a backside junction with the substrate***, and thus cannot correspond to the recited emitter. As Okayasu further explains, ***in such a BSF structure, the junction is formed on the front side of the solar cell***, not on the backside where the BSF is (Okayasu, paragraph 2; paragraph 14, lines 1-6). It is thus respectfully submitted that Okayasu has no teaching regarding a backside junction, external to the substrate or otherwise.

The final office action suggests that it would have been obvious to use the BSF formation technique of Okayasu to form the backside junction emitter of Meier. As explained, Okayasu has no relevant teaching regarding formation of a backside junction. There is no teaching or suggestion in Meier and Okayasu that the BSF layer of Okayasu may be employed as an emitter. Such a modification would use the BSF layer of Okayasu for a totally different function and structure in Meier, would require a change of polarity relative to the substrate, and would require substantial redesign of the process of Meier and Okayasu, as it is not clear how the internal aluminum alloy junction of Meier can be changed to an external polysilicon junction.

Furthermore, Meier modified with Okayasu does not teach or suggest a tunnel dielectric between the backside junction emitter and the substrate. The final office action suggests that Foglietti and Ohmi disclose the benefits of using a thin oxide with polysilicon. It is respectfully submitted that there is no teaching in Meier, Okayasu, Foglietti, and Ohmi that this thin oxide can be advantageously implemented with a backside junction emitter. Such a teaching is only in the present application, not in the cited combination.

It is to be noted that Meier, Okayasu, Foglietti, and Ohmi disclose very different processes. In Meier, the backside aluminum alloy back junction is achieved by diffusing aluminum of an electrode into the substrate. In Okayasu, the BSF layer is formed by reaction of SiF_4 gas with the silicon substrate (Okayasu, paragraph 14). It is respectfully submitted that the there is no teaching or suggestion in Meier, Okayasu, Foglietti, and Ohmi that the processes of Meier and Okayasu would work with an intervening thin dielectric between the silicon substrate and the emitter.

Therefore, it is respectfully submitted that claim 1 is patentable over the combination of Meier, Okayasu, Ohmi, and Foglietti.

Claims 2-4 and 6-8 are patentable over the combination of Meier, Okayasu, Foglietti, and Ohmi at least for depending from claim 1.

Claim 9 is patentable over the combination of Meier, Okayasu, Ohmi, and Foglietti at least for reciting: "an emitter over the back surface of the substrate, the emitter forming a backside junction with the substrate; a first dielectric between the emitter and the back surface." It is respectfully submitted that the combination of Meier, Okayasu, Ohmi, and Foglietti does not teach or suggest a solar cell with an emitter that is over a dielectric that forms a backside junction with the substrate.

Claims 10-14 are patentable over the combination of Meier, Okayasu, Ohmi, and Foglietti at least for depending from claim 9.

PTO/AIA/31 (03-14)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

NOTICE OF APPEAL FROM THE EXAMINER TO THE PATENT TRIAL AND APPEAL BOARD

Docket Number (Optional): 10031.0004211

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Signature /Patrick D. Benedicto/

Typed or printed name PATRICK D. BENEDICTO

In re Application of: Peter John COUSINS

Application Number	Filed
14/504,771	10/02/2014

For: FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

Art Unit	Examiner
1757	PILLAY, DEVINA

Applicant hereby **appeals** to the Patent Trial and Appeal Board from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) $ 800

☐ Applicant asserts small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by 50%, and the resulting fee is: $ _____

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Therefore, the fee shown above is reduced by 75%, and the resulting fee is: $ _____
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 50-2427.

☑ Payment made via EFS-Web.

☐ A petition for an extension of time under 37 CFR 1.136(a) (PTO/AIA/22 or equivalent) is enclosed.
For extensions of time in reexamination proceedings, see 37 CFR 1.550.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant ☑ attorney or agent of record Registration number 40,909 ☐ attorney or agent acting under 37 CFR 1.34 Registration number _____

Signature /Patrick D. Benedicto/

Typed or printed name PATRICK D. BENEDICTO

Telephone Number 408.436.2110

Date December 16, 2016

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 41.20(b)(1) and 41.31. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/504,771	10/02/2014	Peter John COUSINS	10031.004211	3342

74254 7590 01/25/2017

Okamoto & Benedicto LLP
P.O. Box 641330
San Jose, CA 95164-1330

EXAMINER
PILLAY, DEVINA

ART UNIT	PAPER NUMBER
1757	

MAIL DATE	DELIVERY MODE
01/25/2017	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of Panel Decision from Pre-Appeal Brief Review	Application No. 14/504,771	Applicant(s) COUSINS, PETER JOHN
	Examiner DEVINA PILLAY	Art Unit 1757

This is in response to the Pre-Appeal Brief Request for Review filed 16 December, 2016.

1. ☐ **Improper Request** – The Request is improper and a conference will not be held for the following reason(s):

☐ The Notice of Appeal has not been filed concurrent with the Pre-Appeal Brief Request.
☐ The request does not include reasons why a review is appropriate.
☐ A proposed amendment is included with the Pre-Appeal Brief request
☐ Other: .

The time period for filing a response continues to run from the receipt date of the Notice of Appeal or from the mail date of the last Office communication, if no Notice of Appeal has been received.

2. ☐ **Proceed to Board of Patent Appeals and Interferences** – A Pre-Appeal Brief conference has been held. The application remains under appeal because there is at least one actual issue for appeal. Applicant is required to submit an appeal brief in accordance with 37 CFR 41.37. The time period for filing an appeal brief will be reset to be one month from mailing this decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater. Further, the time period for filing of the appeal brief is extendible under 37 CFR 1.136 based upon the mail date of this decision or the receipt date of the notice of appeal, as applicable.

☐ The panel has determined the status of the claim(s) is as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____
Claim(s) rejected: _____
Claim(s) withdrawn from consideration: _____.

3. ☐ **Allowable application** – A conference has been held. The rejection is withdrawn and a Notice of Allowance will be mailed. Prosecution on the merits remains closed. No further action is required by applicant at this time.

4. ☒ **Reopen Prosecution** – A conference has been held. The rejection is withdrawn and a new Office action will be mailed. No further action is required by applicant at this time.

All participants:

(1) *DEVINA PILLAY*	(3) *Christine Tierney*.
(2) *Jeffrey Barton*.	(4)_____

/DEVINA PILLAY/ Primary Examiner, Art Unit 1757	/Jeffrey Barton/ Supervisory Patent Examiner, Art Unit 1757	/Christine Tierney/ Supervisory Patent Examiner, Art Unit 1700



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/504,771	10/02/2014	Peter John COUSINS	10031.004211	3342

74254 7590 02/17/2017

Okamoto & Benedicto LLP
P.O. Box 641330
San Jose, CA 95164-1330

EXAMINER
PILLAY, DEVINA

ART UNIT	PAPER NUMBER
1757	

MAIL DATE	DELIVERY MODE
02/17/2017	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/504,771	Applicant(s) COUSINS, PETER JOHN	
	Examiner DEVINA PILLAY	Art Unit 1757	AIA (First Inventor to File) Status No

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/19/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-4 and 6-14* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-4 and 6-14* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Rejections - 35 USC § 103

2. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under pre-AIA 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of pre-AIA 35 U.S.C. 103(c) and potential pre-AIA 35 U.S.C. 102(e), (f) or (g) prior art under pre-AIA 35 U.S.C. 103(a).

5. Claims 1-4 and 6-14 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Meier (US 6,262,359) in view of Okayasu (JP07-106611, Machine Translation) in view of Borden (WO 2009/094578 A2).

Regarding claims 1-4, 6, and 9-13, Meier discloses a solar cell comprising (see Fig. 3D, C5/L38-C6/L55):

a substrate (218 n-type) having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

an emitter (220 p-type) forming a backside junction with the substrate;

a front electrode disposed over the front surface of the substrate (212);

a back electrode disposed over the back surface of the substrate (222).

However, Meier does not disclose that the emitter is a polysilicon emitter and that there is a first tunnel dielectric formed between the emitter and the back surface of the substrate.

Okayasu discloses that instead of forming an emitter or surface field from a portion of a substrate which is doped, an emitter or surface field can be formed using a doped polysilicon layer ([0005][0009], Abstract) and by forming an emitter or surface field this way the thickness can be more accurately controlled and it prevents generation of floating foreign matter ([0008] [0009]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the method of forming the emitter and front surface field from a

portion of a substrate of Meier and instead forming the emitter and front surface field by using a doped polysilicon layer as disclosed by Okayasu because the thickness can be more accurately controlled and it prevent generation of floating foreign matter.

However, modified Meier does not discloses a tunneling dielectric oxide between the emitter and the substrate.

Borden discloses that tunnel oxides can be used in solar cells between doped polysilicon and monocrystalline substrates [0016].

Furthermore, Borden discloses that by providing the tunneling layer it prevents epitaxial growth of the emitter layer and further it protects the surface from plasma damage of the deposited emitter layer [0008].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the interface between polycrystalline layers and monocrystalline substrates of modified Meier by having a tunneling oxide because it prevents epitaxial growth of the emitter layer and further it protects the crystalline surface from plasma damage of the deposited emitter layer.

Regarding claims 7 and 14, modified Meier discloses all of the claim limitations as set forth above.

However, Meier does not disclose that the electrode that is in contact with the p-type polysilicon layer is silver.

Okayasu discloses that the back electrode on the polysilicon emitter is formed of a silver electrode [0044].

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the aluminum electrode of Meier with the silver electrode of Okayasu because one of ordinary skill in the art would have been able to carry out such a substitution, and the results would be reasonably predictable.

Regarding claim 8, modified Meier discloses all of the claim limitations as set forth above.

In addition, Meier discloses an antireflection layer (214) disposed over the top surface of the substrate (C6/L20-25).

6. Claims 1-4 and 6-14 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Meier (US 6,262,359) in view of Okayasu (JP07-106611, Machine Translation) in view of Foglietti (US 2002/0142500 A1) in view of Gan (Polysilicon Emitters for Silicon Concentrator Solar Cells).

Regarding claims 1-4, 6, and 9-13, Meier discloses a solar cell comprising (see Fig. 3D, C5/L38-C6/L55):

a substrate (218 n-type) having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

an emitter (220 p-type) forming a backside junction with the substrate;

a front electrode disposed over the front surface of the substrate (212);

a back electrode disposed over the back surface of the substrate (222).

However, Meier does not disclose that the emitter is a polysilicon emitter and that there is a first tunnel dielectric formed between the emitter and the back surface of the substrate.

Okayasu discloses that instead of forming an emitter or surface field from a portion of a substrate which is doped, an emitter or surface field can be formed using a doped polysilicon layer ([0005][0009], Abstract) and by forming an emitter or surface field this way the thickness can be more accurately controlled and it prevent generation of floating foreign matter ([0008] [0009]).

Gan further discloses that solar cell performance can be improved when a doped-emitter is replaced with a polysilicon emitter (see pg. 245 second column).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the method of forming the emitter and front surface field from a portion of a substrate of Meier and instead forming the emitter and front surface field by using a doped polysilicon layer as disclosed by Okayasu because the thickness can be more accurately controlled and it prevent generation of floating foreign matter and furthermore because as disclosed by Gan this results in a solar cell with better performance.

However, modified Meier does not discloses a tunneling dielectric oxide between the emitter and the substrate.

Foglietti discloses that polycrystalline growth directly on crystalline silicon results in partial realignment of the polycrystalline grains and to suppress this effect a thin oxide can be grown ([0046]).

Gan discloses that the presence of a stable thermal oxide between a polysilicon emitter and a CZ wafer (See pg. 248, first column, and Table 1) results in recombination occurring primary at the oxide interface and that the presence of this oxide at the

interface can be useful for silicon solar cells with polysilicon emitters (See Conclusion, pg. 249).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the interface between the doped polysilicon regions and the monocyrstalline substrate by adding an interfacial oxide as disclosed by Fogiletti and Gan because it will allow for optimal grown of the polysilicon region and furthermore will result in recombination primarily occurring at the oxide interface.

Regarding claims 7 and 14, modified Meier discloses all of the claim limitations as set forth above.

However, Meier does not disclose that the electrode that is in contact with the p-type polysilicon layer is silver.

Okayasu discloses that the back electrode on the polysilicon emitter is formed of a silver electrode [0044].

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the aluminum electrode of Meier with the silver electrode of Okayasu because one of ordinary skill in the art would have been able to carry out such a substitution, and the results would be reasonably predictable.

Regarding claim 8, modified Meier discloses all of the claim limitations as set forth above.

In addition, Meier discloses an antireflection layer (214) disposed over the top surface of the substrate (C6/L20-25).

Response to Arguments

7. Applicant argues that Okayasu cannot cure the deficiencies of Meier because the backside junction of Meier is formed integrally with the substrate and therefore there can be no interfacial oxide. Since Okayasu is concerned with a front side emitter and therefore Okayasu is not possible because it would require a total redesign of Meier.

8. Examiner respectfully disagrees. Meier discloses method of forming a junction which consists of an emitter formed on a substrate which comprises using the electrode as a dopant material and driving in those dopants through annealing. Okayasu discloses an alternative method of forming an emitter which comprises depositing a doped polysilicon emitter over a single crystalline substrate. Okayasu also discloses that this method is preferable to that of heating and driving in dopants because it can be performed at lower temperatures which prevents damage to the substrate and furthermore the thickness of the emitter can be more accurately controlled ([0008]). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the emitter of Meier with the emitter of Okayasu because of the above advantages.

9. Applicant further argues that neither Foglietti nor Ohmi disclose that a thin oxide can be used in a backside junction solar cell.

10. As disclosed above Gan, Foglietti and Borden disclose that a thin oxide can be provide advantageous properties between a doped polysilicon emitter and a monocrystalline substrate.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEVINA PILLAY whose telephone number is (571)270-1180. The examiner can normally be reached on Monday thru Friday 7:30am -5:00pm (EST). Examiner Fax Number is (571)-270-2180.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey T. Barton can be reached on 571-272-1307. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DEVINA PILLAY/
Primary Examiner, Art Unit 1757

Notice of References Cited	Application/Control No. 14/504 771	Applicant(s)/Patent Under Reexamination COUSINS, PETER JOHN	
	Examiner DEVINA PILLAY	Art Unit 1757	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
	A	US-				
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N	JP07-106611	04-1995	Japan	Okayasu	H01L31/04
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Gan, Polysilicon emitters for silicon concentrator solar cells, Photovoltaic Specialists Conference. May 1990., Conference Record of the Twenty First IEEE, pgs. 245-250.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14504771	COUSINS, PETER JOHN
	Examiner	**Art Unit**
	DEVINA PILLAY	1755

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/17/2016	06/08/2016	10/05/2016	01/31/2017					
	1	÷	✓	✓	✓					
	2	÷	✓	✓	✓					
	3	÷	✓	✓	✓					
	4	÷	✓	✓	✓					
	5	÷	✓	-	-					
	6	÷	✓	✓	✓					
	7	÷	✓	✓	✓					
	8	÷	✓	✓	✓					
	9	÷	✓	✓	✓					
	10	÷	✓	✓	✓					
	11	÷	✓	✓	✓					
	12	÷	✓	✓	✓					
	13	÷	✓	✓	✓					
	14	÷	✓	✓	✓					
	15	÷	N	-	-					
	16	÷	N	-	-					
	17	÷	N	-	-					
	18	÷	N	-	-					
	19	÷	N	-	-					
	20	÷	N	-	-					

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14504771	COUSINS, PETER JOHN
	Examiner	Art Unit
	DEVINA PILLAY	1755

CPC- SEARCHED		
Symbol	Date	Examiner
H01L31/0236 H01L31/0745 H01L31/1804	6/8/2016	DP
H01L31/022425 H01L31/068 H01L31/182 H01L31/056	6/8/2016	DP
Y02E10/52 Y02P70/521 Y02E10/547	6/8/2016	DP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor name search in PALM	6/8/2016	DP
EAST Text Search (See Search History)	6/8/2016	DP
Updated Inventor name search in PALM	10/5/2016	DP
Updated Inventor name search in PALM	2/1/2017	DP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

DERWENT-ACC-NO: 1995-189164

DERWENT-WEEK: 199525

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TITLE: BSF type solar battery mfr. by forming poly:silicon@ layer on N=type silicon substrate by CVD and using silicon fluoride as etching gas

INVENTOR: OKAYASU Y; SAGAWA Y

PATENT-ASSIGNEE: TONEN CORP[TOFU]

PRIORITY-DATA: 1993JP-243040 (September 29, 1993)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
JP 07106611 A	April 21, 1995	JA

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 07106611A	N/A	1993JP-243040	September 29, 1993

INT-CL-CURRENT:

TYPE	IPC DATE
CIPP	H01 L 31/04 20060101

ABSTRACTED-PUB-NO: JP 07106611 A

BASIC-ABSTRACT:

The method involves forming a P type polysilicon layer (2) on the light incident side of a N type single crystal silicon substrate (1). Thus, a PN junction is formed. A N+ polysilicon layer (5) is set up at the opposite side of the silicon substrate and forms a HL junction. The N+ polysilicon layer is formed by CVD method which applies B2H6 or SiF4 or SiH4 gas onto the heated silicon substrate. When Sif4 is used as an etching agent, a halogen radical emitted near the heated silicon substrate.

ADVANTAGE - The method prevents generation of floating foreign material in a room; reduces substrate temp. of BSF type solar battery; and enables mfr. of BSF type solar battery with high photoelectric conversion efficiency and high stability.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: TYPE SOLAR BATTERY MANUFACTURE FORMING POLY SILICON@ LAYER N=TYPE SILICON SUBSTRATE CVD FLUORIDE ETCH GAS

ADDL-INDEXING-TERMS: BACK SURFACE FIELD

DERWENT-CLASS: L03 U12 X15

CPI-CODES: L03-E05; L04-C02; L04-C10B;

EPI-CODES: U12-A02A3;

SECONDARY-ACC-NO:

CPI Secondary Accession Numbers: 1995-087785

Non-CPI Secondary Accession Numbers: 1995-148457

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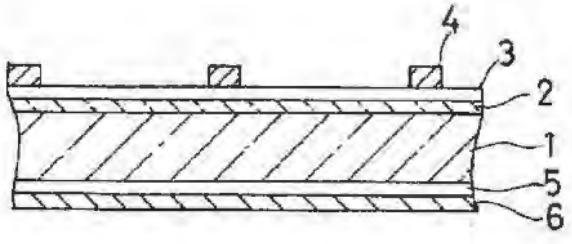
(54)【発明の名称】　ＢＳＦ型太陽電池の製造方法

(57)【要約】

【目的】　光電変換効率の高いＢＳＦ型太陽電池を安定して製造できる方法を提供すること。

【構成】　ｎ⁻単結晶シリコン（以下、Ｓｉ）基板１と、この光入射側面に設けられたｐ型のポリSi層２と、反対側面に設けられSi基板との間でＨＬ接合を形成するｎ⁺ポリSi層５を備えるＢＳＦ型太陽電池の製造方法であり、上記ｎ⁺ポリSi層をB_2H_6／ＳｉＨ₄／ＳｉＦ₄を原料ガスとする熱ＣＶＤ法により形成することを特徴とする。この方法によれば、ハロゲン原子を放出するＳｉＦ₄を適用しているにも拘らず製膜室内における浮遊異物の発生を防止でき、かつ、熱ＣＶＤ法を適用しているにも拘らず基板加熱温度の低減を図ることが可能となるため、ｎ⁺ポリSi層の膜質が改善されて光電変換効率の高いＢＳＦ型太陽電池を安定して製造できる効果を有している。

1：ｎ⁻単結晶シリコン基板
2：ｐ型ポリシリコン層
5：n^+ポリシリコン層



1

【特許請求の範囲】

【請求項1】n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法において、

n型又はp型シリコン基板を配置した製膜室内にシリコン原子が含まれる製膜ガスとSiF_4ガス及びn型又はp型のドーパントガスを供給し、かつ、上記供給ガスを加熱されたシリコン基板近傍で熱分解させると共に、熱分解された製膜ガスのラジカル成分と上記SiF_4ガスとの反応により生じたフッ素系ラジカルをエッチング成分として作用させながらn型又はp型シリコン基板面に上記n⁺又はp⁺シリコン層を形成することを特徴とするBSF型太陽電池の製造方法。

【請求項2】n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法において、

n型又はp型シリコン基板を配置した製膜室内に水素化珪素を主成分とする製膜ガスとSiH_mF_{4-m}（但しmは1～3）で示されるフッ素化シランガス及びn型又はp型のドーパントガスを供給し、かつ、上記供給ガスを加熱されたシリコン基板近傍で熱分解させると共に、フッ素化シランガスの熱分解により生じたフッ素系ラジカル、及び、熱分解された製膜ガスのラジカル成分が上記フッ素化シランガスと反応して生じたフッ素系ラジカルをエッチング成分として作用させながらn型又はp型シリコン基板面に上記n⁺又はp⁺シリコン層を形成することを特徴とするBSF型太陽電池の製造方法。

【請求項3】製膜室内に配置されたn型又はp型シリコン基板近傍の空間部位に上記基板が覆われるように網状の発熱部材を配置したことを特徴とする請求項1又は2記載のBSF型太陽電池の製造方法。

【請求項4】n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法において、

加熱されたシリコン基板面に上記n⁺又はp⁺シリコン層を光CVD法により形成することを特徴とするBSF型太陽電池の製造方法。

【請求項5】n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL

2

接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法において、

n型又はp型シリコン基板を配置した製膜室内にSiH_mF_{4-m}（但しmは1～3）で示されるフッ素化シランガス又はSiF_4ガスを供給し、かつ、このフッ素化シランガス又はSiF_4ガスが存在する条件下においてイオンプレーティング法により加熱されたシリコン基板面に上記n⁺又はp⁺シリコン層を形成することを特徴とするBSF型太陽電池の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明はBSF（Back Surface Field）型太陽電池の製造方法に係り、特に、光電変換効率の高いBSF型太陽電池を安定して製造できるBSF型太陽電池の製造方法に関するものである。

【0002】

【従来の技術】この種のBSF型太陽電池としては、例えば、図7～8に示すようにp型単結晶シリコン基板aと、このシリコン基板aの光入射側面に設けられシリコン基板aとの間でpn接合を形成するn⁺シリコン層bと、このn⁺シリコン層b上に一様に成膜されたITO（酸化インジウム錫）の反射防止層cと、この反射防止層c上に設けられた櫛歯状電極dと、上記シリコン基板aの反対側面に設けられシリコン基板aとの間でHL（High-Low）接合を形成するp⁺シリコン層eと、このp⁺シリコン層eの背面側に一様に設けられた裏面電極fとでその主要部が構成され、光入射に伴って発生したエレクトロンとホールが上記電極d、fから電流として取出される構造のものが知られている。

【0003】尚、図9はこのBSF型太陽電池の構造をモデル的に記載した構造概念図であり、また、図10はこの構造を有するBSF型太陽電池のエネルギーバンド図を示している。

【0004】そして、p⁺シリコン層eを具備しない構造の太陽電池と較べてこのBSF型太陽電池においては、HL接合gを形成するシリコン基板aとp⁺シリコン層e間に存在する内蔵電界が少数キャリア（この場合、エレクトロン）の裏面電極fへの拡散の障壁となり見掛け上エレクトロンの拡散長が増加し、かつ上記p⁺シリコン層eがホールに対して低抵抗のオーム性電極になるためシリーズ抵抗が低下し、従って、その光電変換効率を向上できる利点を有するものであるとされていた。

【0005】ところで、開放電圧を上昇させる上記p⁺シリコン層eについては、従来『熱拡散法』により形成されていた。すなわち、B（ボロン）等を含むp型ドーパントガスで満たされた反応室内に上記単結晶シリコン基板aを導入し、このドーパントガスをシリコン基板a内に1000℃前後の高温条件下で熱拡散させて形成したり、単結晶シリコン基板a面にAl（アルミニウム）

等のp型ドーパント層を積層しこれを１０００℃前後の高温条件下で焼成してp⁺シリコン層eを形成していた。

【０００６】しかし、この『熱拡散法』によりp⁺シリコン層eを形成した場合、p⁺シリコン層eの厚み制御が難しくその層厚が数百オングストローム～数μmと大きくなり易く、かつ、熱的条件の僅かなばらつきでB、Al等ドーパントガスの拡散距離が変動し易いためシリコン基板aの特性がばらつき易い欠点があった。

【０００７】更に、上記『熱拡散法』ではドーパントガスの回り込みも起こり易く、シリコン基板との間でpn接合を形成するn⁺シリコン層b内へも上記ドーパントガスが熱拡散してしまうことがあり、また、シリコン基板が１０００℃前後の高温に晒されることから基板の熱劣化を引起こす等の欠点もあった。

【０００８】このような技術的背景の下、本出願人は上記n型又はp型シリコン基板との間でHL接合を形成するn⁺シリコン層又はp⁺シリコン層をプラズマCVD法により形成するBSF型太陽電池の製造方法を既に提案している。すなわち、この製造方法によれば、従来の熱拡散法による場合に較べてn⁺シリコン層又はp⁺シリコン層形成時における熱的条件が緩和されるためシリコン基板の特性劣化が起こり難くなると共に、上記n⁺シリコン層又はp⁺シリコン層の厚さを従来より薄い数十オングストローム～数百オングストローム程度に形成することが可能になるためその光電変換効率の向上が図れる利点を有する方法であった。

【０００９】

【発明が解決しようとする課題】ところで、プラズマCVD法を適用した上記製造方法においてはn⁺シリコン層又はp⁺シリコン層の低温製膜とその薄膜化が図れることから上述した利点を有していたが、その反面、上記n⁺シリコン層又はp⁺シリコン層の製膜工程中において粉状の浮遊異物が製膜室内に多量に発生し易く、この浮遊異物が製膜途上のn⁺シリコン層又はp⁺シリコン層内に混入されてその膜特性を劣化させてしまう欠点があった。

【００１０】すなわち、プラズマCVD法を適用したこの製造方法においては製膜室内のプラズマ形成領域にプラズマ化された原料ガスが一様に分布しかつこのプラズマ化された原料ガスは励起状態にあるため、製膜室内の任意の空間において原料ガスが互いに反応してシリコンの粉状体を生成したり、基板以外の部位すなわち製膜室の内壁面においてプラズマ化された原料ガスが反応してシリコンが析出しこれが粉状体となって剥離する等粉状の浮遊異物が多量に発生し易い状態にある。

【００１１】また、プラズマCVD法においては製膜ガスであるSiH_4ガス等に加えてハロゲンガスを配合する場合があり、このハロゲン原子のエッチング作用により製膜室の内壁面や内部治具表面が腐食され易いためこ

の腐食面が剥離して上記浮遊異物に加わることになる。

【００１２】このため、プラズマCVD法を適用した上記製造方法においては上述した利点を有している反面、良質なn⁺シリコン層又はp⁺シリコン層を形成することが困難なためこれに起因して得られたBSF型太陽電池の光電変換効率も一定の限界を有する問題点があった。

【００１３】本発明はこのような問題点に着目してなされたもので、その課題とするところは、低温製膜条件で良質なn⁺シリコン層又はp⁺シリコン層が形成できる熱CVD法、光CVD法、及び、イオンプレーティング法を選択することにより光電変換効率が更に向上したBSF型太陽電池を安定して製造できる方法を提供することにある。

【００１４】

【課題を解決するための手段】すなわち、請求項１に係る発明は、n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法を前提とし、n型又はp型シリコン基板を配置した製膜室内にシリコン原子が含まれる製膜ガスとSiF_4ガス及びn型又はp型のドーパントガスを供給し、かつ、上記供給ガスを加熱されたシリコン基板近傍で熱分解させると共に、熱分解された製膜ガスのラジカル成分と上記SiF_4ガスとの反応により生じたフッ素系ラジカルをエッチング成分として作用させながらn型又はp型シリコン基板に上記n⁺又はp⁺シリコン層を形成することを特徴とするものであり、また、請求項２に係る発明は、n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法を前提とし、n型又はp型シリコン基板を配置した製膜室内に水素化珪素を主成分とする製膜ガスとSiH_nF_{4-n}（但しmは１～３）で示されるフッ素化シランガス及びn型又はp型のドーパントガスを供給し、かつ、上記供給ガスを加熱されたシリコン基板近傍で熱分解させると共に、フッ素化シランガスの熱分解により生じたフッ素系ラジカル、及び、熱分解された製膜ガスのラジカル成分が上記フッ素化シランガスと反応して生じたフッ素系ラジカルをエッチング成分として作用させながらn型又はp型シリコン基板に上記n⁺又はp⁺シリコン層を形成することを特徴とするものである。

【００１５】そして、請求項１に係る発明においてはハロゲン原子を放出するガスとして熱分解を受け難いSiF_4ガスが適用されており、また、請求項２に係る発明においてはハロゲン原子を放出するガスとして上記製膜

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ガスよりその熱分解温度が高いフッ素化シランガスを適用しているため、製膜室内の基板から離れた温度分布の低い領域においてはSiF_4及びフッ素化シランガスの熱分解が起り難く、その分、この領域のフッ素系ラジカル濃度は低い状態になっている。

【0016】従って、プラズマCVD法を適用した従来の製造方法に較べて、製膜室内の任意の空間において上記製膜ガスがフッ素系ラジカルと反応してシリコン粉状体を生成したり、あるいは、製膜室の内壁面や内部治具表面が上記フッ素系ラジカルの作用を受けて腐食される可能性が低いため、ハロゲン原子を放出するSiF_4又はフッ素化シランガスを適用しているにも拘らず製膜室内における浮遊異物の発生を防止することが可能となる。

【0017】一方、請求項1に係る発明において上記SiF_4ガスは熱分解を受けにくい反面、熱分解されたシラン化合物等製膜ガスのラジカル成分との反応によりその熱分解が促進されるため、上記ラジカル成分の多い領域、すなわちn型又はp型シリコン基板近傍領域において分解を受け易くこの領域に高濃度のフッ素系ラジカルが偏在することになる。また、請求項2に係る発明においも上記SiH_2F_2等フッ素化シランガスはn型又はp型シリコン基板近傍の高温領域において熱分解を受け易いと共に、熱分解された製膜ガスのラジカル成分（SiH_xラジカル、H系ラジカル等）との反応によりその分解が促進されるため、基板近傍領域に高濃度のフッ素系ラジカルが偏在することになる。

【0018】従って、このフッ素系ラジカルの作用によりn型又はp型シリコン基板上若しくは成長中のn^+又はp^+シリコン層に混入された不純物のみが選択的にエッチングを受けて取除かれることになるため、本来、この不純物を取除くための高温加熱処理が必要となる熱CVD法を適用しているにも拘らず請求項1又は2に係る発明においては基板加熱温度の低減が図れる。

【0019】尚、請求項1又は2に係る発明において製膜室内の基板近傍の空間部位に上記基板を加熱する発熱手段を設けると、製膜ガスの熱分解が促進されるため基板加熱温度を更に低減することが可能となる。請求項3に係る発明はこのような技術的理由に基づきなされている。

【0020】すなわち、請求項3に係る発明は、請求項1又は2記載の発明に係るBSF型太陽電池の製造方法を前提とし、製膜室内に配置されたn型又はp型シリコン基板近傍の空間部位に上記基板が覆われるように網状の発熱部材を配置したことを特徴とするものである。

【0021】そして、n型又はp型シリコン基板近傍の空間部位に配置される上記発熱部材とは、基板全面を覆うように配置されてもn^+又はp^+シリコン層の製膜に支障を来さないような形状を備え、かつ水素化珪素等の製膜ガスを基板近傍領域で熱分解させる程度に発熱する材

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料で構成されているもので、具体例としてタングステン、トリウムタングステン等から成る網状の熱フィラメントが挙げられる。

【0022】また、請求項1～3に係る発明の熱CVD法においては、製膜処理中にこの製膜室内の真空度を略一定に維持するためその下流側において継続して排気処理を行っており、エッチング作用に供されたフッ素系ラジカルあるいは余剰のフッ素系ラジカルは上記排気処理により製膜室から外部へ排除されている。

【0023】ここで、請求項1～3に係る発明においてn型又はp型シリコン基板との間でHL接合を形成するn^+シリコン層又はp^+シリコン層としては、n型又はp型ドーパントガスが導入されたアモルファスシリコン層、ポリシリコン層、あるいは、単結晶シリコン層が適用できる。この場合、内部抵抗を下げる観点からポリシリコン層よりはその抵抗値の低い単結晶シリコン層が望ましく、また、アモルファスシリコン層よりはその抵抗値の低いポリシリコン層が望ましい。

【0024】尚、n型のドーパントガスとしては元素周期率表第III族のSb（アンチモン）、As（ひ素）、及び、P（リン）等を含む化合物が適用でき、具体例としては、SbH_3、$SbCl_3$、AsH_3、As_2H_4、及び、PH_3等が挙げられる。また、p型のドーパントガスとしては元素周期率表第V族のGa（ガリウム）、B（ボロン）In（インジウム）、及び、Al（アルミニウム）等を含む化合物が適用でき、具体例としては、B_2H_6、$Ga(CH_3)_3$、$In(CH_3)_3$、及び、$Al(CH_3)_3$等が挙げられる。

【0025】また、請求項1又は3に係る発明においてシリコン原子が含まれる上記製膜ガスとしては、熱分解され易いSiH_4、Si_2H_6、及び、Si_3H_8等の水素化珪素やSiH_mX_{4-m}（但し、mは1～3、好ましくは2～3、XはCl又はF原子、好ましくはF原子である）で示されるハロゲン化シラン等が適用できる。尚、この製膜ガス内に水素ガスを添加してもよい、この水素系ラジカルもSiF_4ガスに作用してその分解を促進させるからである。ここで、製膜ガスとして後者のハロゲン化シランガスを適用した場合、このハロゲン化シランガスの配合割合が高過ぎると製膜室内に上述した浮遊異物が生ずることがある。従って、SiH_mX_{4-m}で示されるハロゲン化シランガスを適用する場合にはその配合割合を上記SiF_4より少なく設定することが望ましい。

【0026】また、請求項2又は3に係る発明において上記製膜ガスの主要部を構成する水素化珪素としては、SiH_4、Si_2H_6、及び、Si_3H_8等が適用できる。また、請求項1又は3に係る発明と同様、上記製膜ガス内に水素ガスを添加してもよい。この水素系ラジカルも上記SiH_2F_2等のフッ素化シランガスと反応しその熱分解を促進させるからである。

【0027】尚、請求項1～3に係る発明において上記

製膜ガス中に希釈ガスとして、ヘリウム、ネオン、アルゴン等の不活性ガスを加えてもよい。

【0028】そして、請求項1～3記載の発明に係るBSF型太陽電池の製造方法においては、製膜開始前における製膜室の真空度をこの製膜室内に不純物が若干残留する程度（10^{-5}Torr程度）に設定し、かつ、配置されたn型又はp型シリコン基板の温度を500℃～700℃程度に設定した後、少なくとも上記製膜ガスとSiF_4ガス及びn型又はp型のドーパントガスを供給するか、あるいは、少なくとも上記製膜ガスとSiH_mF_{4-m}（但しmは1～3）で示されるフッ素化シランガス及びn型又はp型のドーパントガスを供給して上記n型又はp型シリコン基板上にn⁺又はp⁺シリコン層を形成する。このとき、基板加熱温度を500℃～700℃程度の低温条件に設定しても上記フッ素系ラジカルのエッチング作用により不純物は選択的に除去され、また、浮遊異物の発生も殆ど起らずn⁺又はp⁺シリコン層内への混入が起こり難いため上記n⁺又はp⁺シリコン層の膜特性に悪影響を及ぼす可能性がほとんどない。

【0029】従って、光電変換効率が更に向上したBSF型太陽電池を安定して製造できる利点を有している。

【0030】次に、請求項4～5に係る発明は、請求項1～3に係る発明において n⁺又はp⁺シリコン層の製膜に適用された熱CVD法に代えて光CVD法及びイオンプレーティング法を適用したBSF型太陽電池の製造方法に関する。

【0031】まず、請求項4に係る発明は、n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法を前提とし、加熱されたシリコン基板面に上記n⁺又はp⁺シリコン層を光CVD法により形成することを特徴とするものである。

【0032】すなわち、この光CVD装置は、図5に示すように製膜室11と、この製膜室11内に石英窓30を介し配設された紫外線照射ランプ31と、この紫外線照射ランプ31の対向側に設けられヒータ15が組込まれた基板ホルダー13と、製膜室11内へSiH_4等の製膜ガスと、適宜ドーパントガスと、水素ガス等を供給するガス供給源16、17と、調圧弁19を介して接続された減圧ポンプ18とでその主要部が構成されており、上記製膜室11内にn型又はp型シリコン基板14を配置すると共に、このシリコン基板14を500～600℃程度に加熱した後、上記ガス供給源16、17から製膜ガス、ドーパントガス等を供給し、かつ、紫外線を照射して上記n型又はp型シリコン基板14上にn⁺又はp⁺シリコン層を形成する方法である。

【0033】そして、この請求項4記載の発明に係る製造方法によれば、低温製膜条件で膜質良好なn⁺又はp⁺シリコン層をp型シリコン基板14上に形成できるため、請求項1～3に係る発明と同様、光電変換効率が更に向上したBSF型太陽電池を安定して製造できる利点を有している。

【0034】次に、請求項5に係る発明は、n型又はp型シリコン基板と、このシリコン基板の光入射面側に設けられシリコン基板との間でpn接合を形成するp型又はn型シリコン層と、上記シリコン基板の反対面に設けられシリコン基板との間でHL接合を形成するn⁺又はp⁺シリコン層とを備えるBSF型太陽電池の製造方法を前提とし、n型又はp型シリコン基板を配置した製膜室内にSiH_mF_{4-m}（但しmは1～3）で示されるフッ素化シランガス又はSiF_4ガスを供給し、かつ、このフッ素化シランガス又はSiF_4ガスが存在する条件下においてイオンプレーティング法により加熱されたシリコン基板面に上記n⁺又はp⁺シリコン層を形成することを特徴とするものである。

【0035】すなわち、このイオンプレーティング装置は、図6に示すように製膜室11と、この製膜室11内の下方側に設けられ製膜材料であるドーパント混入のSiターゲットが収容された抵抗加熱蒸発源40と、この抵抗加熱蒸発源40の上方側空間部に設けられたRFコイル41と、上記抵抗加熱蒸発源40からの供給量を調整するシャッター42と、製膜室11内の上方側に設けられシリコン基板14を600～700℃程度に加熱する基板ホルダー43とでその主要部が構成されており、かつ、RFコイル41には高周波電源44が、また、基板ホルダー43には正の高圧電源（図示せず）が接続されている。そして、上記製膜室11内にn型又はp型シリコン基板14を配置し、かつ、この製膜室11内にフッ素化シランガス又はSiF_4ガスを供給すると共に、上記シリコン基板14を600～700℃程度に加熱した後、抵抗加熱蒸発源40からドーパントとシリコンを蒸発させてn型又はp型シリコン基板14上にn⁺又はp⁺シリコン層を形成する方法である。

【0036】この請求項5に係る発明においても、請求項1～3に係る発明と同様、ハロゲン原子を放出するガスとして熱分解を受け難いフッ素化シランガス又はSiF_4ガスが適用されているためn型又はp型シリコン基板近傍領域において高濃度のフッ素系ラジカルが偏在することになる。すなわち、n型又はp型シリコン基板の近傍領域においては熱分解されたシリコン分子のラジカル成分が遍在しているため、このラジカル成分と上記フッ素化シランガス又はSiF_4ガスとの反応により高濃度のフッ素系ラジカルが偏在している。そして、このフッ素系ラジカルの作用によりn型又はp型シリコン基板上若しくは成長中のn⁺又はp⁺シリコン層に混入された不純物のみが選択的にエッチングを受けて取除かれることになるため、低温製膜条件で膜質良好なn⁺又はp⁺シ

リコン層をn型又はp型シリコン基板上に形成することが可能となり、請求項1～4に係る発明と同様、光電変換効率が更に向上したBSF型太陽電池を安定して製造できる利点を有している。

【0037】

【作用】請求項1に係る発明によれば、ハロゲン原子を放出するガスとして熱分解を受け難いSiF_4ガスが適用されており、このガスが熱分解され難い分、製膜室内におけるフッ素系ラジカル濃度は低い状態になっているため、プラズマCVD法を適用した従来の製造方法に較べて製膜室内の任意の空間において製膜ガスがフッ素系ラジカルと反応してシリコン粉状体を生成したり、あるいは、製膜室の内壁面や内部治具表面が上記フッ素系ラジカルの作用を受けて腐食される可能性が極端に低くなり、ハロゲン原子を放出するSiF_4ガスを適用しているにも拘らず製膜室内における浮遊異物の発生を確実に防止することが可能となる。

【0038】一方、上記SiF_4ガスは製膜ガスのラジカル成分（SiH_xラジカル、H系ラジカル等）との反応によりその熱分解が促進されることからこのラジカル成分の多いn型又はp型シリコン基板近傍領域に高濃度のフッ素系ラジカルが偏在し易くなり、このフッ素系ラジカルの作用により上記基板上若しくは成長中のn^+又はp^+シリコン層に混入された不純物のみが選択的にエッチングを受けて取除かれるため、本来、この不純物を取除くための高温加熱処理が必要となる熱CVD法を適用しているにも拘らず基板加熱温度の低減を図ることが可能となる。

【0039】また、請求項2に係る発明によれば、ハロゲン原子を放出するガスとして上記製膜ガスよりその熱分解温度が高いフッ素化シランガスを適用しており、製膜室内の基板から離れた温度分布の低い領域においては上記製膜ガスに較べてこのフッ素化シランガスの熱分解が起り難くフッ素系ラジカル濃度は低い状態になっているため、プラズマCVD法を適用した従来の製造方法に較べて製膜室内の任意の空間において製膜ガスがフッ素系ラジカルと反応してシリコン粉状体を生成したり、あるいは、製膜室の内壁面や内部治具表面が上記フッ素系ラジカルの作用を受けて腐食される可能性が低くなり、ハロゲン原子を放出するフッ素化シランガスを適用しているにも拘らず製膜室内における浮遊異物の発生を防止することが可能となる。

【0040】一方、上記フッ素化シランガスはn型又はp型シリコン基板近傍の高温領域において熱分解を受け易いと共に熱分解された製膜ガスのラジカル成分（SiH_xラジカル、H系ラジカル等）との反応によりその分解が促進されることからn型又はp型シリコン基板近傍領域に高濃度のフッ素系ラジカルが偏在し易くなり、このフッ素系ラジカルの作用により上記基板上若しくは成長中のn^+又はp^+シリコン層に混入された不純物のみが選択的にエッチングを受けて取除かれるため、請求項1に係る発明と同様、熱CVD法を適用しているにも拘らず基板加熱温度の低減を図ることが可能となる。

【0041】更に、請求項3に係る発明によれば、製膜室内に配置されたn型又はp型シリコン基板近傍の空間部位に上記基板が覆われるように網状の発熱部材を配置していることから、この発熱部材が発する熱エネルギの作用により上記基板近傍領域においては製膜ガスの熱分解が著しく促進されているため、上記フッ素系ラジカルのエッチング作用と相乗して基板加熱温度を更に低減させることが可能となる。

【0042】次に、請求項4に係る発明によれば、加熱されたシリコン基板面にn^+又はp^+シリコン層を光CVD法により製膜しているため、低温製膜条件で膜質良好なn^+又はp^+シリコン層を上記n型又はp型シリコン基板上に形成することが可能となる。

【0043】また、請求項5に係る発明によれば、フッ素化シランガス又はSiF_4ガスが存在する条件下においてイオンプレーティング法により加熱されたシリコン基板面に上記n^+又はp^+シリコン層を製膜しているため、低温製膜条件で膜質良好なn^+又はp^+シリコン層を上記n型又はp型シリコン基板上に形成することが可能となる。

【0044】

【実施例】以下、本発明の実施例について詳細に説明するとこの実施例に係るBSF型太陽電池は、従来同様、図1に示すようにn^-単結晶シリコン基板（100配向、比抵抗1～10Ω・cm）1と、このシリコン基板1の光入射側面に設けられシリコン基板1との間でpn接合を形成するp型アモルファスシリコン又はポリシリコン層2と、このp型アモルファスシリコン又はポリシリコン層2上に一様に成膜されITO（酸化インジウム錫）にて形成された反射防止層3と、この反射防止層3上に設けられ銀ペーストにて形成された櫛歯状電極4と、上記シリコン基板1の反対側面に設けられシリコン基板1との間でHL接合を形成するn^+アモルファスシリコン又はポリシリコン層5と、このn^+アモルファスシリコン又はポリシリコン層5の背面側に一様に設けられアルミニウムにて形成された裏面電極6とでその主要部が構成されているものである。

【0045】そしてこのBSF型太陽電池は以下の工程に従って製造されたものである。

【0046】［実施例1］図3はこの実施例で適用された熱CVD装置の概略構成を示した説明図で、図中11は製膜室、13はヒータ15が組込まれた基板ホルダー、14はこの基板ホルダー13に取付けられたn^-単結晶シリコン基板、16、17は原料ガスの供給源、及び、18は調圧弁19を介し製膜室11に接続された減圧ポンプをそれぞれ示している。

【0047】まず、この製膜室11を排気して1×10

$^{-6}$Torrの真空にし、次いで、この製膜室11内に下記原料ガスを導入すると共に下記の製膜条件に従ってその一面側にp型ポリシリコン層2を、他方の面にn$^+$ポリシリコン層5をそれぞれ製膜した（図2A参照）。

【0048】（p型ポリシリコン層2の製膜条件）

原料ガスの種類と組成：B_2H_6／SiH_4／SiF_4＝0．1／10／500

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：700℃

（n$^+$ポリシリコン層5の製膜条件）

原料ガスの種類と組成：PH_3／SiH_4／SiF_4＝0．1／10／330

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：700℃

次に、図2（B）に示すようにスパッタリング法にてp型ポリシリコン層2上にITOを着膜させて反射防止層3を形成し、かつ、この面上に銀ペーストにより櫛歯状電極4を形成すると共に、n$^+$ポリシリコン層5の背面側にスパッタリング法によりアルミニウムを一様に製膜して裏面電極6を形成し実施例に係るBSF型太陽電池を求めた（図1参照）。

【0049】そして、この電池の特性を調べたところ、n$^+$ポリシリコン層の製膜手段にプラズマCVD法を適用した従来のものの特性が0．57V～0．58V、35mA～37mAであったのに対し、この実施例に係るBSF型太陽電池の特性は0．59V～0．60V、37mA～39mAであった。

【0050】［実施例2］p型ポリシリコン層2とn$^+$ポリシリコン層5に代えてp型アモルファスシリコン層とn$^+$アモルファスシリコン層を適用し、かつ、その製膜条件が下記である点を除き実施例1と略同一である。

【0051】そして、この実施例に係るBSF型太陽電池においてもその特性が0．59V～0．60V、37mA～39mAであり従来例に較べて良好であった。

【0052】（p型アモルファスシリコン層2の製膜条件）

原料ガスの種類と組成：B_2H_6／SiH_4／SiF_4／H_2＝0．1／10／100／400

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：600℃

（n$^+$アモルファスシリコン層5の製膜条件）

原料ガスの種類と組成：PH_3／SiH_4／SiF_4／H_2＝0．1／10／100／400

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mlorr～1lorr

n$^-$単結晶シリコン基板の加熱温度：600℃

［実施例3］p型アモルファスシリコン層2とn$^+$アモルファスシリコン層5の製膜条件が下記である点を除き実施例2と略同一である。

【0053】そして、この実施例に係るBSF型太陽電池においてもその特性が0．58V～0．59V、36mA～38mAであり従来例に較べて良好であった。

【0054】（p型アモルファスシリコン層2の製膜条件）

原料ガスの種類と組成：$In(CH_3)_3$／SiH_4／SiH_2F_2／アルゴン＝0．1／10／100／400

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：650℃

（n$^+$アモルファスシリコン層5の製膜条件）

原料ガスの種類と組成：$SbCl_3$／SiH_4／SiH_2F_2／アルゴン＝0．1／10／100／400

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：650℃

［実施例4］p型アモルファスシリコン層2とn$^+$アモルファスシリコン層5の製膜条件が下記である点を除き実施例2と略同一である。

【0055】そして、この実施例に係るBSF型太陽電池においてもその特性が0．58V～0．59V、36mA～38mAであり従来例に較べて良好であった。

【0056】（p型アモルファスシリコン層2の製膜条件）

原料ガスの種類と組成：$Al(CH_3)_3$／SiH_4／SiH_2F_2／H_2／アルゴン＝0．1／10／100／300／100

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：700℃

（n$^+$アモルファスシリコン層5の製膜条件）

原料ガスの種類と組成：PH_3／SiH_4／SiH_2F_2／H_2／アルゴン＝0．1／10／100／300／100

原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr

n$^-$単結晶シリコン基板の加熱温度：700℃

［実施例5］図3に示された装置に代えて図4に示すように基板近傍の空間部位にタングステンの熱フィラメント20が配置された熱CVD装置を適用すると共に、上記p型ポリシリコン層2とn$^+$ポリシリコン層5の製膜条件が下記である点を除き実施例1と略同一である。

【0057】そして、この実施例に係るBSF型太陽電池においてもその特性が0．59V～0．60V、37mA～39mAであり従来例に較べて良好であった。

【0058】（p型ポリシリコン層2の製膜条件）

原料ガスの種類と組成：$Ga(CH_3)_3$／SiH_4／SiF_4／H_2＝0．1／10／100／400

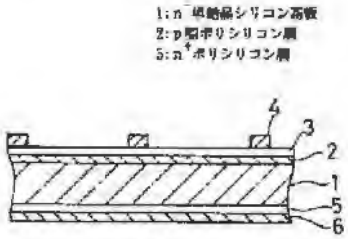
原料ガスの供給速度：5sccm～100sccm
原料ガスの圧力：50mtorr～1torr
n⁻単結晶シリコン基板の加熱温度：650℃
（n⁺ポリシリコン層5の製膜条件）
原料ガスの種類と組成：AsH_3／SiH_4／SiF_4／H_2＝0．1／10／100／400
原料ガスの供給速度：5sccm～100sccm
原料ガスの圧力：50mtorr～1torr
n⁻単結晶シリコン基板の加熱温度：650℃
［実施例6］図4に示された熱CVD装置を適用した点と、p型ポリシリコン層2とn⁺ポリシリコン層5の製膜条件が下記である点を除き実施例1と略同一である。
【0059】そして、この実施例に係るBSF型太陽電池においてもその特性が0．58V～0．59V、36mA～38mAであり従来例に較べて良好であった。
【0060】（p型ポリシリコン層2の製膜条件）
原料ガスの種類と組成：B_2H_6／SiH_4／SiH_2F_2／H_2／アルゴン＝0．1／10／100／400／100
原料ガスの供給速度：5sccm～100sccm
原料ガスの圧力：50mtorr～1torr
n⁻単結晶シリコン基板の加熱温度：650℃
（n⁺ポリシリコン層5の製膜条件）
原料ガスの種類と組成：PH_3／SiH_4／SiH_2F_2／H_2／アルゴン＝0．1／10／100／400／100
原料ガスの供給速度：5sccm～100sccm
原料ガスの圧力：50mtorr～1torr
n⁻単結晶シリコン基板の加熱温度：650℃
［実施例7］図5に示された光CVD装置を適用した点と、p型アモルファスシリコン層2とn⁺アモルファスシリコン層5の製膜条件が下記である点を除き実施例2と略同一である。
【0061】そして、この実施例に係るBSF型太陽電池においてもその特性が0．59V～0．60V、37mA～39mAであり従来例に較べて良好であった。
【0062】（p型アモルファスシリコン層2の製膜条件）
製膜室内の圧力：1～10mTorr
原料ガスの種類と組成：B_2H_6／SiH_4／H_2＝0．1／10／300
原料ガスの供給速度：5sccm～100sccm
原料ガスの圧力：50mtorr～1torr
紫外光の照射光源：Hgランプ
n⁻単結晶シリコン基板の加熱温度：600℃
（n⁺アモルファスシリコン層5の製膜条件）
製膜室内の圧力：1～10mTorr
原料ガスの種類と組成：PH_3／SiH_4／H_2＝0．1／10／300
原料ガスの供給速度：5sccm～100sccm

原料ガスの圧力：50mtorr～1torr
紫外光の照射光源：Hgランプ
n⁻単結晶シリコン基板の加熱温度：600℃
［実施例8］図6に示されたイオンプレーティング装置を適用し、かつ、このイオンプレーティング装置内にSiF_4ガスを供給した点と、p型ポリシリコン層2とn⁺ポリシリコン層5の製膜条件が下記である点を除き実施例1と略同一である。
【0063】そして、この実施例に係るBSF型太陽電池においてもその特性が0．58V～0．59V、36mA～38mAであり従来例に較べて良好であった。
【0064】（p型ポリシリコン層2の製膜条件）
製膜室内の圧力：1～10mTorr
ターゲット：B_2H_6がドープされたSi
RFコイルへの投入電力：50～200W
n⁻単結晶シリコン基板の加熱温度：700℃
（n⁺ポリシリコン層5の製膜条件）
製膜室内の圧力：1～10mTorr
ターゲット：PH_3がドープされたSi
RFコイルへの投入電力：50～200W
n⁻単結晶シリコン基板の加熱温度：700℃
【0065】
【発明の効果】請求項1～2に係る発明によれば、ハロゲン原子を放出するSiF_4ガスあるいはフッ素化シランガスを適用しているにも拘らず製膜室内における浮遊異物の発生を確実に防止でき、かつ熱CVD法を適用しているにも拘らず基板加熱温度の低減を図ることが可能となる。
【0066】また、請求項3に係る発明によれば、製膜室内に配置されたn型又はp型シリコン基板近傍の空間部位に設けられた発熱部材の作用により製膜ガスの熱分解が著しく促進されるため、フッ素系ラジカルのエッチング作用と相乗して基板加熱温度を更に低減させることが可能となる。
【0067】従って、低温製膜条件で膜質良好なn⁺又はp⁺シリコン層をn型又はp型シリコン基板上に形成することが可能になるため、光電変換効率の高いBSF型太陽電池を安定して製造できる効果を有している。
【0068】次に、請求項4に係る発明によれば、加熱されたシリコン基板面に上記n⁺又はp⁺シリコン層を光CVD法により製膜し、また、請求項5に係る発明によれば、フッ素化シランガス又はSiF_4ガスが存在する条件下においてイオンプレーティング法により加熱されたシリコン基板面に上記n⁺又はp⁺シリコン層を製膜しているため、請求項1～3に係る発明と同様、低温製膜条件で膜質良好なn⁺又はp⁺シリコン層をn型又はp型シリコン基板上に形成することが可能となり、光電変換効率の高いBSF型太陽電池を安定して製造できる効果を有している。
【図面の簡単な説明】

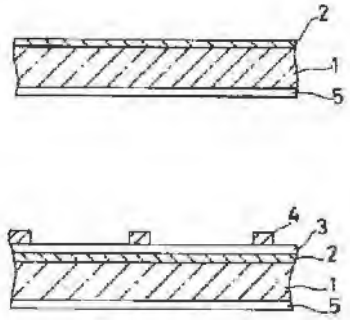
15　　16

【図1】実施例に係るBSF型太陽電池の断面図。
【図2】図2（A）～（B）はBSF型太陽電池の製造工程図。
【図3】実施例1において適用された熱CVD装置の説明図。
【図4】実施例5において適用された熱CVD装置の説明図。
【図5】実施例7において適用された光CVD装置の説明図。
【図6】実施例8において適用されたイオンプレーティング装置の説明図。
【図7】従来の太陽電池の斜視図。
【図8】従来の太陽電池の断面図。
【図9】従来の太陽電池の構造をモデル的に記載した構造概念図。
【図10】従来の太陽電池のエネルギーバンド図。
【符号の説明】
1　n⁻ 単結晶シリコン基板
2　p型ポリシリコン層
5　n⁺ ポリシリコン層

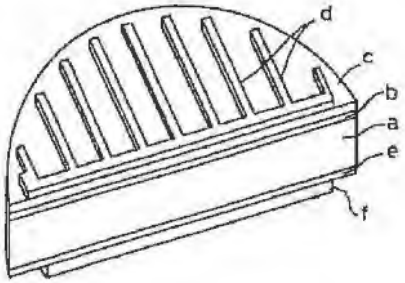
【図1】



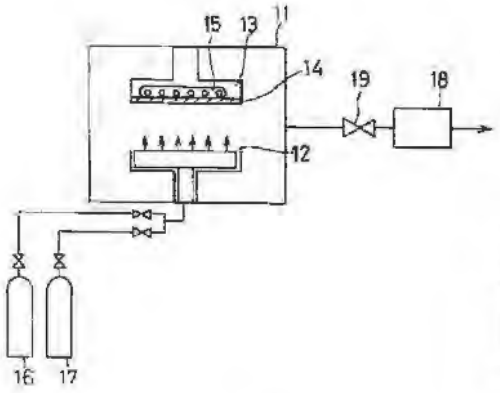
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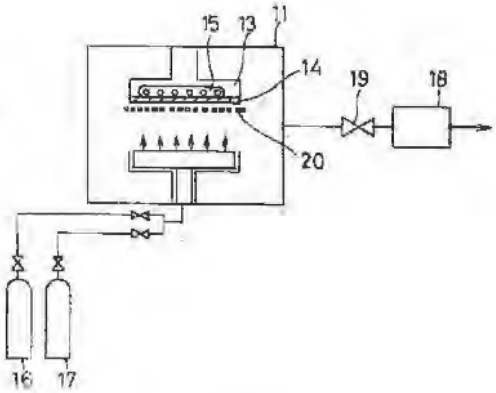
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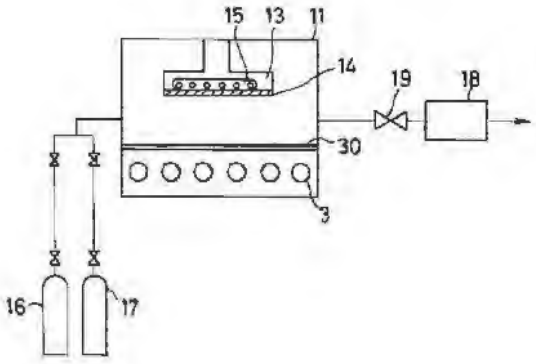
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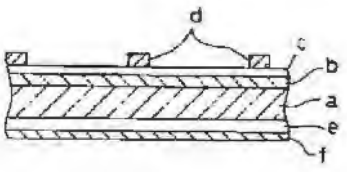
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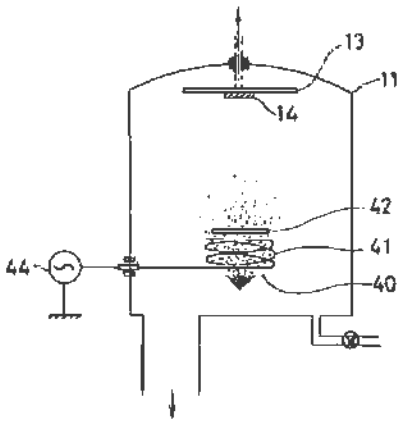
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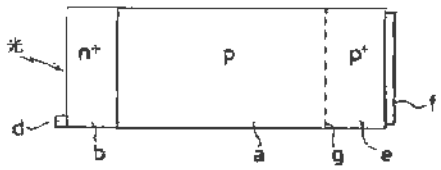
【図8】



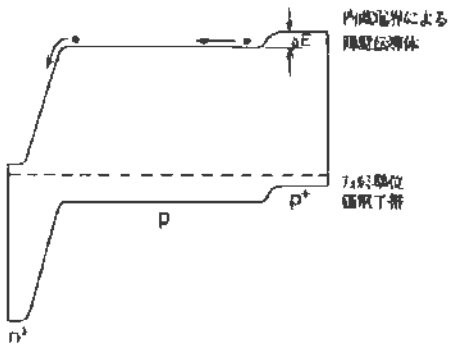
【図6】



【図9】



【図10】



Doc Code: AP.PRE.REQ

PTO/AIA/33 (03-13)
Approved for use through 07/31/2013. OMB 0651-0031
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 10031.004211

I hereby certify that this correspondence is being facsimile transmitted to the USPTO, EFS-Web transmitted to the USPTO, or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]
on 03/28/2016

Signature /Patrick D. Benedicto/

Typed or printed name PATRICK D. BENEDICTO

Application Number	Filed
14/504,771	10/02/2014

First Named Inventor: Peter John COUSINS

Art Unit	Examiner
1757	PILLAY, DEVINA

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 40,909

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

/Patrick D. Benedicto/
Signature

PATRICK D. BENEDICTO
Typed or printed name

408.436.2110
Telephone number

March 28, 2017
Date

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

ARGUMENTS

Claim Rejection -- 35 U.S.C. § 103 (Meier/Okayasu/Borden)

Claims 1-4 and 6-14 are rejected under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Meier (US 6,262,359), in view of Okayasu (JP 07-106611), and in view of Borden (US WO 2009/094578 A2). The rejection is respectfully traversed.

1. External emitter that forms a backside junction with the substrate

Claim 1 is patentable over the combination of Meier, Okayasu, Ohmi, and Foglietti at least for reciting: "an emitter disposed over the first tunnel dielectric, the emitter forming a backside junction with the substrate."

Claim 1 recites a structure of a solar cell. In the embodiment of claim 1, the solar cell has an emitter that is disposed over a tunnel dielectric and forms a backside junction with the substrate. It is respectfully submitted that this feature of claim 1 is not taught or suggested by the combination of Meier, Okayasu, and Borden.

The final office action suggests that in the cited combination, Meier discloses the recited backside junction. Meier FIG. 3D is reproduced below for ease of discussion.

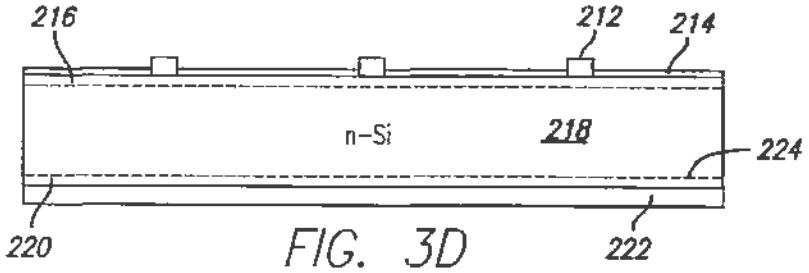
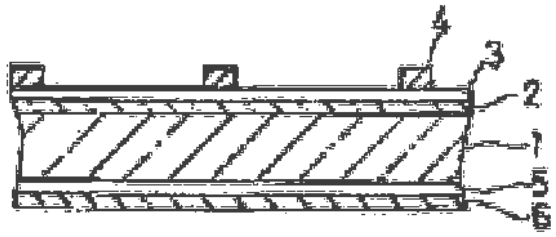


FIG. 3D

Meier discloses a solar cell with an aluminum alloy back junction (Meier, Title). More specifically, Meier discloses forming a p+ layer 220 ("emitter") that forms a backside junction with the n-Si base layer 218 ("substrate") within the base layer 218 by doping using the aluminum contact layer 222 (Meier, col. 6, lines 51-54). That is, the primary teaching of Meier is to form an aluminum alloy back junction by forming the p+ layer 220 within the substrate by diffusion into the substrate using the aluminum alloy electrode, thereby providing a strongly doped p-type emitter (Meier, abstract).

Meier discloses a solar cell structure where the emitter that forms a backside junction with the substrate is within the substrate and in contact with the electrode. In the solar cell structure of Meier there is no intervening layer (such as a tunnel dielectric) between the emitter and the electrode because of the required diffusion of aluminum from the electrode to the emitter. Accordingly, Meier does not disclose a solar cell structure where an external emitter forms a backside junction with the substrate.

Okayasu does not disclose a solar cell structure that cures the deficiencies of Meier. Okayasu FIG. 1 is reproduced below.



The purpose of Okayasu is "to realize a ***BSF type solar cell*** having high photoelectric conversion efficiency by forming an n+ poly-Si layer by thermal CVD using B2H6/SiH4/SiF4 as a material gas thereby improving the quality of n+ poly-Si layer" (Okayashu abstract) (emphasis added). More particularly, to the extent the appellant understands the machine translation of the disclosure of Okayasu, Okayasu FIG. 1 shows a solar cell with an N-type substrate 1, a layer 2 on the front side, an N+ BSF layer 5, an electrode 6 on the backside, and an electrode 4 on the front side. Because the layer 5 is a back surface field (BSF) layer, the layer 5 is necessarily on the back surface and has the same polarity as the substrate 1. Accordingly, the BSF layer 5 cannot form a backside junction with the substrate.

Therefore, like Meier, Okayasu does not disclose a solar cell structure where an external emitter forms a backside junction with the substrate. In the solar cell of Okayasu, the backside is a BSF layer in accordance with the purpose of Okayasu and, in such a BSF structure, the junction is formed on the front side of the solar cell, not on the backside where the BSF layer is (Okayasu, paragraph 2; paragraph 14, lines 1-6).

The final office action suggests that it would have been obvious to use the BSF formation technique of Okayasu to form the backside junction emitter of Meier. The appellant respectfully disagrees.

First, Meier's solar cell is not a BSF type solar cell. Okayasu does not teach or suggest that its method is applicable to non-BSF type solar cells -- Okayasu has no relevant teaching regarding formation of a backside junction. The suggestion to use the BSF method of Okayasu to form the emitter of Meier would use the BSF method of Okayasu for a totally different function and structure in Meier.

Second, Okayasu discloses a method of forming the high-low junction (HL) on the front side of a BSF solar cell structure (Okayasu, paragraphs 1 and 2) . Instead of using thermal diffusion (Okayasu, paragraphs 5-7) or plasma CVD (Okayasu, paragraphs 8-12), Okayasu suggests forming the HL junction by thermal CVD (Okayasu, paragraph 14) to minimize foreign matter or to control deposition thickness. It is respectfully submitted that this suggested method of Okayasu pertains to manufacture of the HL junction of a BSF type solar cell, i.e., structures on the front side of a BSF solar cell. The ***method*** of Okayasu is for the ***structure*** taught by Okayasu, which is a BSF solar cell. In other words, Okayasu does not teach or suggest solar cell structure where an external emitter forms a backside junction with the substrate.

2. Backside junction with tunnel dielectric

It is respectfully submitted that Meier modified with Okayasu does not teach or suggest a tunnel dielectric between the backside junction emitter and the substrate. The final office action suggests that Borden (paragraphs 8 and 16) discloses use of a tunnel oxide between polysilicon and substrate.

First, it is respectfully submitted that the final office action has not established that Borden is prior art to the present application. Borden has an international filing date of January 23, 2009, whereas the present application has a priority date of February 20, 2008 by claiming priority to US 8,878,053 and US 8,222,516. It is acknowledged that Borden claims priority from a provisional application 61/023,342. However, the final office action cites to the international publication of Borden (which on its face is not prior art to the present application as explained), not to the provisional application.

Furthermore, the provisional application of Borden does not appear to be publicly accessible.

Second. Borden does not disclose that the polysilicon/tunnel oxide/substrate is for forming a backside junction. There is no teaching or suggestion in Borden that such tunnel oxide structure may be applied to the teachings of Meier and Okayasu to read on the solar cell of claim 1.

Claims 2-4 and 6-8 are patentable over the combination of Meier, Okayasu, and Borden at least for depending from claim 1.

Claim 9 is patentable over the combination of Meier, Okayasu, and Borden at least for reciting: "an emitter over the back surface of the substrate, the emitter forming a backside junction with the substrate; a first dielectric between the emitter and the back surface." It is respectfully submitted that the combination of Meier, Okayasu, and Borden does not teach or suggest a solar cell with an emitter that is over a dielectric that forms a backside junction with the substrate.

Claims 10-14 are patentable over the combination of Meier, Okayasu, and Borden at least for depending from claim 9.

Claim Rejection -- 35 U.S.C. § 103 (Meier/Okayasu/Foglietti/Gan)

Claims 1-4 and 6-14 are rejected under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Meier (US 6,262,359), in view of Okayasu (JP 07-106611), in view of Foglietti (US 2002/0142500), and further in view of Gan (*Polysilicon Emitters for Silicon Concentrator Solar Cells*). The rejection is respectfully traversed.

1. External emitter that forms a backside junction with the substrate

Claim 1 is patentable over the combination of Meier, Okayasu, Foglietti, and Gan at least for reciting: "an emitter disposed over the first tunnel dielectric, the emitter forming a backside junction with the substrate."

Claim 1 recites a structure of a solar cell. In the embodiment of claim 1, the solar cell has an emitter that is disposed over the tunnel dielectric and forms a backside

junction with the substrate. It is respectfully submitted that this feature of claim 1 is not taught or suggested by the combination of Meier, Okayasu, Foglietti, and Gan.

The final office action suggests that in the cited combination, Meier modified with the teachings of Okayasu discloses the above-recited features of claim 1. As explained, the combination of Meier and Okayasu does not teach or suggest a solar cell structure where an external emitter forms a backside junction with the substrate.

2. Backside junction with tunnel dielectric

It is respectfully submitted that Meier modified with Okayasu does not teach or suggest a tunnel dielectric between the backside junction emitter and the substrate. The final office action suggests that Gan discloses that doped emitter can be replaced with a polysilicon emitter and that Foglietti discloses using a thin oxide. It is respectfully submitted that Gan and Foglietti does not disclose structures where polysilicon emitters and tunnel oxides are employed in backside junctions. There is no teaching or suggestion in Gan and Foglietti to apply their teachings to arrive at a structure where an external polysilicon emitter separated from the substrate by a tunnel oxide forms a backside junction with the substrate.

Therefore, it is respectfully submitted that claim 1 is patentable over the combination of Meier, Okayasu, Foglietti, and Gan. Claims 2-4 and 6-8 are patentable over the combination of Meier, Okayasu, Foglietti, and Gan at least for depending from claim 1.

Claim 9 is patentable over the combination of Meier, Okayasu, Foglietti, and Gan at least for reciting: "an emitter over the back surface of the substrate, the emitter forming a backside junction with the substrate; a first dielectric between the emitter and the back surface." It is respectfully submitted that the combination of Meier, Okayasu, Foglietti, and Gan does not teach or suggest a solar cell with an emitter that is over a dielectric that forms a backside junction with the substrate.

Claims 10-14 are patentable over the combination of Meier, Okayasu, Foglietti, and Gan at least for depending from claim 9.

Docket No. 10031.004211
Notice of Appeal
March 28, 2017

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Peter John COUSINS

Application No.: 14/504,771 Examiner: PILLAY, DEVINA

Filing Date: October 2, 2014 Art Unit: 1757

Title: FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

NOTICE OF APPEAL

Submitted herewith is a notice of appeal. This is the second notice of appeal filed on this application. The first notice of appeal was filed by Applicants on December 16, 2016. The Patent Trial and Appeal Board did not render a decision on the case from the first notice of appeal.

Applicants believe that they are entitled to credit for the notice of appeal fee paid on December 16, 2016 because the Board did not render a decision from the first notice of appeal. Therefore, Applicants believe that there is no fee due for this filing. If for any reasons additional fees are required, the Commissioner is hereby authorized to charge the insufficiency to Deposit Account No. 50-2427.

Respectfully submitted,

Dated: March 28, 2017

/Patrick D. Benedicto/
Patrick D. Benedicto, Reg. No. 40,909
Attorney or Record
Okamoto & Benedicto LLP
(408) 436-2110

PTO/AIA/31 (03-14)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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NOTICE OF APPEAL FROM THE EXAMINER TO THE PATENT TRIAL AND APPEAL BOARD

Docket Number (Optional): 10031.0004211

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Signature /Patrick D. Benedicto/

Typed or printed name PATRICK D. BENEDICTO

In re Application of: Peter John COUSINS

Application Number	Filed
14/504,771	10/02/2014

For: FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

Art Unit	Examiner
1757	PILLAY, DEVINA

Applicant hereby **appeals** to the Patent Trial and Appeal Board from the last decision of the examiner.

The fee for this Notice of Appeal is [37 CFR 41.20(b)(1)) $ 0.00

☐ Applicant asserts small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by 50%, and the resulting fee is: $ _____

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Therefore, the fee shown above is reduced by 75%, and the resulting fee is: $ _____
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

Payment by credit card. Form PTO-2038 is attached.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 50-2427.

☐ Payment made via EFS-Web.

☐ A petition for an extension of time under 37 CFR 1.136(a) (PTO/AIA/22 or equivalent) is enclosed.
For extensions of time in reexamination proceedings, see 37 CFR 1.550.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant

☑ attorney or agent of record
Registration number 40,909

☐ attorney or agent acting under 37 CFR 1.34
Registration number _____

Signature /Patrick D. Benedicto/

Typed or printed name PATRICK D. BENEDICTO

Telephone Number 408.436.2110

Date March 28, 2017

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 41.20(b)(1) and 41.31. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/504,771	10/02/2014	Peter John COUSINS	10031.0042US1	3342

74254 7590 04/28/2017

Okamoto & Benedicto LLP
P.O. Box 641330
San Jose, CA 95164-1330

EXAMINER
PILLAY, DEVINA

ART UNIT	PAPER NUMBER
1757	

MAIL DATE	DELIVERY MODE
04/28/2017	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of Panel Decision from Pre-Appeal Brief Review	**Application No.** 14/504,771	**Applicant(s)** COUSINS, PETER JOHN
	Examiner DEVINA PILLAY	**Art Unit** 1757

This is in response to the Pre-Appeal Brief Request for Review filed .

1. ☐ **Improper Request** – The Request is improper and a conference will not be held for the following reason(s):

☐ The Notice of Appeal has not been filed concurrent with the Pre-Appeal Brief Request.
☐ The request does not include reasons why a review is appropriate.
☐ A proposed amendment is included with the Pre-Appeal Brief request.
☐ Other .

The time period for filing a response continues to run from the receipt date of the Notice of Appeal or from the mail date of the last Office communication, if no Notice of Appeal has been received.

2. ☒ **Proceed to Board of Patent Appeals and Interferences** – A Pre-Appeal Brief conference has been held. The application remains under appeal because there is at least one actual issue for appeal. Applicant is required to submit an appeal brief in accordance with 37 CFR 41.37. The time period for filing an appeal brief will be reset to be one month from mailing this decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater. Further, the time period for filing of the appeal brief is extendible under 37 CFR 1.136 based upon the mail date of this decision or the receipt date of the notice of appeal, as applicable.

☒ The panel has determined the status of the claim(s) is as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: *1-4 and 6-14*.
Claim(s) withdrawn from consideration: _____.

3. ☐ **Allowable application** – A conference has been held. The rejection is withdrawn and a Notice of Allowance will be mailed. Prosecution on the merits remains closed. No further action is required by applicant at this time.

4. ☐ **Reopen Prosecution** – A conference has been held. The rejection is withdrawn and a new Office action will be mailed. No further action is required by applicant at this time.

All participants:

(1) *DEVINA PILLAY*	(3) *Jennifer McNeil*.
(2) *Jeffrey Barton*.	(4)_____.

/DEVINA PILLAY/ Primary Examiner, Art Unit 1757	/Jeffrey T Barton/ Supervisory Patent Examiner, Art Unit 1757	/Jennifer McNeil/ Primary Examiner, TC 1700

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-14)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	14504771	Filing Date	2014-10-02	Docket Number (if applicable)	10031.004211	Art Unit	1757
First Named Inventor	Peter John COUSINS			Examiner Name	PILLAY, DEVINA		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, to any international application that does not comply with the requirements of 35 U.S.C. 371, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV.

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 502427

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

Doc code: RCEX
Doc description Request for Continued Examination (RCE)

PTO/SB/30EFS (07-14)
Approved for use through 07/31/2016. OMB 0651-0031
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Signature of Registered U.S. Patent Practitioner			
Signature	/Patrick D Benedicto/	Date (YYYY-MM-DD)	2017-05-05
Name	PATRICK D. BENEDICTO	Registration Number	40909

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Docket No. 10031.004211

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:

Peter John COUSINS

Application No.: 14/504,771 Examiner: PILLAY, DEVINA

Filing Date: October 2, 2014 Art Unit: 1757

Title: FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

REQUEST FOR CONTINUED EXAMINATION AND AMENDMENT

INTRODUCTORY COMMENTS

This paper is responsive to Notice of Panel Decision From Pre-Appeal Brief Review mailed on April 28, 2017.

Please amend the above-identified application as follows:

AMENDMENTS TO THE CLAIMS

1. (Currently amended) A solar cell, comprising:

a substrate having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

a first doped region and a second doped region in the substrate on the front surface of the substrate, the first doped region having a sheet resistance that is higher than a sheet resistance of the second doped region;

a ~~first~~ tunnel dielectric disposed over the back surface of the substrate;

an emitter disposed over the ~~first~~ tunnel dielectric, the emitter forming a backside junction with the substrate;

a front electrode ~~disposed over~~ that is coupled to the second doped region on the front surface of the substrate; and

a back electrode disposed over the back surface of the substrate.

2. (Original) The solar cell of claim 1, wherein the emitter is a polysilicon emitter.

3. (Original) The solar cell of claim 1, wherein the substrate is a monocrystalline silicon substrate.

4. (Currently) The solar cell of claim 1, wherein the ~~first~~ tunnel dielectric is a tunnel oxide.

5. (Canceled)

6. (Canceled)

7. (Original) The solar cell of claim 1, wherein the back electrode includes silver.

8. (Original) The solar cell of claim 1, further comprising an antireflective layer disposed over the front surface of the substrate.

9. (Currently amended) A solar cell, comprising:

a substrate having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

a first doped region and a second doped region in the substrate on the front surface of the substrate, the first doped region having a sheet resistance that is higher than a sheet resistance of the second doped region;

an emitter over the back surface of the substrate, the emitter forming a backside junction with the substrate;

a first dielectric between the emitter and the back surface;

a front electrode disposed on the front surface of the substrate and is coupled to the second doped region;

a second dielectric on the front surface of the substrate; and

a back electrode disposed on the back surface of the substrate.

10. (Original) The solar cell of claim 9, wherein the emitter is a polysilicon emitter.

11. (Original) The solar cell of claim 9, wherein the substrate is a monocrystalline silicon substrate.

12. (Original) The solar cell of claim 9, wherein the first dielectric is an oxide.

13. (Canceled)

14. (Original) The solar cell of claim 9, wherein the back electrode includes silver.

15-20. (Canceled)

21. (New) The solar cell of claim 1, wherein the first and second doped regions are N-type, and the emitter is P-type.

22. (New) The solar cell of claim 1, wherein the sheet resistance of the first doped region is 100 to 500 Ω/sq, and the sheet resistance of the second doped region is 10 to 50 Ω/sq.

REMARKS

With the above amendments, claims 1-4, 7-12, 14, 21, and 22 remain in the application.

Claim amendments have been made to expedite prosecution. Applicant expressly reserves the right to pursue the original version of an amended claim in a continuing application.

Claim Amendments

The applicant maintains the arguments presented in the Pre-Appeal Brief Request for Review submitted by the applicant on March 28, 2017.

In the interest of compact prosecution, claim 1 has been amended to recite "a first doped region and a second doped region in the substrate on the front surface of the substrate, the first doped region having a sheet resistance that is higher than a sheet resistance of the second doped region." Support for this feature of claim 1 may be found at least on FIG. 1 of the specification, showing an N-type doped region 105 and an N-type doped region 106 in the substrate 101 on the front surface of the substrate 101. As explained in the specification, the N-type doped region 105 may have a sheet resistance of 100 to 500 Ω/sq, and the N-type doped region 106 may have a sheet resistance of 10 to 50 Ω/sq (specificatiou, page 4, lines11-13).

It is respectfully submitted that the above-noted feature of claim 1 are not taught or suggested by the references of record. More particularly, Meier (US 6,262,359), Okayasu (JP07-106611), Borden (WO 2009/094578), Foglietti (US 2002/0142500), and Gan (*Polysilicon Emitters for Silicon Concentrator Solar Cells*) individually or in combination do not disclose a solar cell with the recited first and second doped regions on the front side of the substrate.

Conclusion

For at least the above reasons, it is believed that the pending claims are in condition for allowance. The Examiner is invited to telephone the undersigned for any questions and to resolve any remaining concerns regarding allowability of the present application.

Respectfully submitted,

Dated: MAY 5, 2017

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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/504,771	Filing Date 10/02/2014	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT	05/05/2017	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 13	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1

SLIE
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This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/504,771	10/02/2014	Peter John COUSINS	10031.004211	3342

74254 7590 05/15/2017

Okamoto & Benedicto LLP
P.O. Box 641330
San Jose, CA 95164-1330

EXAMINER
PILLAY, DEVINA

ART UNIT	PAPER NUMBER
1757	

MAIL DATE	DELIVERY MODE
05/15/2017	PAPER

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
14/504,771	02 October, 2014	COUSINS, PETER JOHN	10031.004211

	EXAMINER	
Okamoto & Benedicto LLP P.O. Box 641330 San Jose, CA 95164-1330	DEVINA PILLAY	
	ART UNIT	PAPER
	1757	20170417-A

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

To Whom It May Concern,

Examiner is providing Applicant a copy of the provisonal application 61/023,342 which Borden (WO 2009/094578 A2) claims priority to. The provisional application has a filing date of 01/24/2008 which supports all of the relevant sections mapped to in Borden and therefore the 102 (e) date of Borden is 01/24/2008. Examiner notes that paragraphs [0013]-[0015] in 61/023,342 recite the information that is relied upon in Borden. In addition, Examiner has attached a human translation for Okayasu (JP07-106611) relied upon in the final rejection mailed 02/17/2017.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEVINA PILLAY whose telephone number is (571)270-1180. The examiner can normally be reached on Monday thru Friday 7:30am -5:00pm (EST). Examiner Fax Number is (571)-270-2180.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey T. Barton can be reached on 571-272-1307. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sincerely,

Devina Pillay

/DEVINA PILLAY/
Primary Examiner, Art Unit 1757

Notice of References Cited	Application/Control No. 14/504 771	Applicant(s)/Patent Under Reexamination COUSINS, PETER JOHN	
	Examiner DEVINA PILLAY	Art Unit 1757	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
	A	US-				
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Provisional 61/023,342 filed 01/24/2008, provided on 04/17/2017
	V	JP07_106611. Human Translation. 04/21/1995. Okayasu
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/504,771	10/02/2014	Peter John COUSINS	10031.004211	3342

74254 7590 06/30/2017

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EXAMINER
PILLAY, DEVINA

ART UNIT	PAPER NUMBER
1757	

MAIL DATE	DELIVERY MODE
06/30/2017	PAPER

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The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/504,771	Applicant(s) COUSINS, PETER JOHN	
	Examiner DEVINA PILLAY	Art Unit 1757	AIA (First Inventor to File) Status No

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05/15/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-4,7-12,14,21 and 22* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-4,7-12,14,21 and 22* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid. the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/15/2017 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. **Claims 1-4, 7-12, 14 and 21 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Meier (US 6,262,359) in view of Okayasu (JP07-106611, Human Translation) in view of Borden (WO 2009/094578 A2) and in further view of Wenham (6,429,037 B1).**

Regarding claims 1-4 and 9-12, Meier discloses a solar cell comprising (see Fig. 3D. C5/L38-C6/L55):

a substrate (218 n-type) having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

an emitter (220 p-type) forming a backside junction with the substrate;

a front electrode disposed over the front surface of the substrate (212);

a back electrode disposed over the back surface of the substrate (222).

However, Meier does not disclose that the emitter is a polysilicon emitter and that there is a first tunnel dielectric formed between the emitter and the back surface of the substrate.

Okayasu discloses that instead of forming an emitter ***or*** surface field from a portion of a substrate which is doped, an emitter or surface field can be formed using a doped polysilicon layer ([0005][0009], Abstract) and by forming an emitter or surface field this way the thickness can be more accurately controlled and it prevents generation of floating foreign matter ([0008] [0009]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the method of forming the emitter from a portion of a substrate of Meier and instead forming the emitter and front surface field by using a doped polysilicon layer as disclosed by Okayasu because the thickness can be more accurately controlled and it prevent generation of floating foreign matter.

However, modified Meier does not discloses a tunneling dielectric oxide between the emitter and the substrate.

Borden discloses that tunnel oxides can be used in solar cells between doped polysilicon and monocrystalline substrates [0016].

Furthermore, Borden discloses that by providing the tunneling layer it prevents epitaxial growth of the emitter layer and further it protects the surface from plasma damage of the deposited emitter layer [0008].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the interface between polycrystalline layers and monocrystalline substrates of modified Meier by having a tunneling oxide because it prevents epitaxial growth of the emitter layer and further it protects the crystalline surface from plasma damage of the deposited emitter layer.

However, modified Meier does not disclose that there is a first doped region and a second doped region in the substrate on the front surface of the substrate, the first doped region having a sheet resistance that is higher than a sheet resistance of a second doped region.

Wenham discloses a solar cell wherein the area beneath point contacts includes areas of high doping which is important for reducing contact resistance (see Fig. 5, portions 18 and 23) (C1/L25-41).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the front surface field formed in the substrate of modified Meier by adding in highly doped regions under the metallic contacts as disclosed by Wenham because doing so reduces the contact resistance and will improve the efficiency of the solar cell.

Regarding claim 9, please note that the anti-reflective layer disposed over the front surface (214 of Meier (C6/L20-25)) of the substrate is also a dielectric (Si_3N_4 or TiO_2 is a dielectric, see Wenham for further evidence C6/L50-55).

Regarding claims 7 and 14, modified Meier discloses all of the claim limitations as set forth above.

However, Meier does not disclose that the electrode that is in contact with the p-type polysilicon layer is silver.

Okayasu discloses that the back electrode on the polysilicon emitter is formed of a silver electrode [0044].

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the aluminum electrode of Meier with the silver electrode of Okayasu because one of ordinary skill in the art would have been able to carry out such a substitution, and the results would be reasonably predictable.

Regarding claim 8, modified Meier discloses all of the claim limitations as set forth above.

In addition, Meier discloses an antireflection layer (214) disposed over the top surface of the substrate (C6/L20-25).

Regarding claim 21, modified Meier discloses all of the claim limitations as set forth above.

In addition, Meier discloses that the first and second doped regions are n-type (since the n-type contacts make direct contact to FSF region, the higher doped regions are also n-type and the emitter region (220 is p-type, C5/L38-C5/L55).

6. **Claim 22 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Meier (US 6,262,359) in view of Okayasu (JP07-106611, Human Translation) in view of Borden (WO 2009/094578 A2) and in further view of Wenham (6,429,037 B1) as applied to claims 1-4, 7-12, 14 and 21 above and in further view of Fath (WO 2007/082760 A1) with English Translation provided by Fath (US 2009/0017606 A1).**

Regarding claim 22, modified Meier discloses all of the claim limitations as set forth above.

Meier discloses that the a highly doped region in the n-type substrate can have a sheet resistance between 10Ω/□ -200Ω/□.

However, Meier does not disclose the sheet resistance of the first doped region is 100 to 500 Ω/□ and that the sheet resistance of the second doped region is 10 to 50 Ω/□.

Fath discloses a higher doped region formed under metallic contacts and a lower doped region which is between contacts and further discloses that typical sheet resistance values of these areas relative to one another which include the lower sheet resistance are being 10 to 30 Ω/□ and the higher sheet resistance area being 80 to 140 Ω/□ ([0042]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the sheet resistance of the first and second doped regions of modified Meier so that they are within the overlapping portions of the ranges of Fath and the instant claim because selection of overlapping portion of ranges has been held to be a prima facie case of obviousness. *In re Malagari*, 182 USPQ 549.

7. **Claims 1-4, 7-12, 14 and 21 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Meier (US 6,262,359) in view of Okayasu (JP07-106611, Machine Translation) in view of Foglietti (US 2002/0142500 A1) in view of Gan (Polysilicon Emitters for Silicon Concentrator Solar Cells) and in further view of Wenham (6,429,037 B1).**

Regarding claims 1-4 and 9-12, Meier discloses a solar cell comprising (see Fig. 3D, C5/L38-C6/L55):

a substrate (218 n-type) having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

an emitter (220 p-type) forming a backside junction with the substrate;

a front electrode disposed over the front surface of the substrate (212);

a back electrode disposed over the back surface of the substrate (222).

However, Meier does not disclose that the emitter is a polysilicon emitter and that there is a first tunnel dielectric formed between the emitter and the back surface of the substrate.

Okayasu discloses that instead of forming an emitter **or** surface field from a portion of a substrate which is doped, an emitter or surface field can be formed using a doped polysilicon layer ([0005][0009], Abstract) and by forming an emitter or surface field this way the thickness can be more accurately controlled and it prevent generation of floating foreign matter ([0008] [0009]).

Gan further discloses that solar cell performance can be improved when a doped-emitter is replaced with a polysilicon emitter (see pg. 245 second column).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the method of forming the emitter from a portion of a substrate of Meier and instead forming the emitter by using a doped polysilicon layer as disclosed by Okayasu because the thickness can be more accurately controlled and it prevent generation of floating foreign matter and furthermore because as disclosed by Gan this results in a solar cell with better performance.

However, modified Meier does not discloses a tunneling dielectric oxide between the emitter and the substrate.

Foglietti discloses that polycrystalline growth directly on crystalline silicon results in partial realignment of the polycrystalline grains and to suppress this effect a thin oxide can be grown ([0046]).

Gan discloses that the presence of a stable thermal oxide between a polysilicon emitter and a CZ wafer (See pg. 248, first column, and Table 1) results in recombination occurring primary at the oxide interface and that the presence of this oxide at the interface can be useful for silicon solar cells with polysilicon emitters (See Conclusion, pg. 249).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the interface between the doped polysilicon regions and the monocyrstalline substrate by adding an interfacial oxide as disclosed by Fogiletti and Gan because it will allow for optimal grown of the polysilicon region and furthermore will result in recombination primarily occurring at the oxide interface.

Regarding claim 9, please note that the anti-reflective layer disposed over the front surface (214 of Meier (C6/L20-25)) of the substrate is also a dielectric (Si_3N_4 or TiO_2 is a dielectric, see Wenham for further evidence C6/L50-55).

Regarding claims 7 and 14, modified Meier discloses all of the claim limitations as set forth above.

However, Meier does not disclose that the electrode that is in contact with the p-type polysilicon layer is silver.

Okayasu discloses that the back electrode on the polysilicon emitter is formed of a silver electrode [0044].

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the aluminum electrode of Meier with the silver electrode of

Okayasu because one of ordinary skill in the art would have been able to carry out such a substitution, and the results would be reasonably predictable.

Regarding claim 8, modified Meier discloses all of the claim limitations as set forth above.

In addition, Meier discloses an antireflection layer (214) disposed over the top surface of the substrate (C6/L20-25).

Regarding claim 21, modified Meier discloses all of the claim limitations as set forth above.

In addition, Meier discloses that the first and second doped regions are n-type (since the n-type contacts make direct contact to FSF region, the higher doped regions are also n-type and the emitter region (220 is p-type, C5/L38-C5/L55).

8. **Claim 22 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Meier (US 6,262,359) in view of Okayasu (JP07-106611, Machine Translation) in view of Foglietti (US 2002/0142500 A1) in view of Gan (Polysilicon Emitters for Silicon Concentrator Solar Cells) and in further view of Wenham (6,429,037 B1) as applied to claims 1-4, 7-12, 14 and 21 above and in further view of Fath (WO 2007/082760 A1) with English Translation provided by Fath (US 2009/0017606 A1).**

Regarding claim 22, modified Meier discloses all of the claim limitations as set forth above.

Meier discloses that the highly doped region in the n-type substrate can have a sheet resistance between 10Ω/□ -200Ω/□.

However, Meier does not disclose the sheet resistance of the first doped region is 100 to 500 Ω/□ and that the sheet resistance of the second doped region is 10 to 50 Ω/□.

Fath discloses a higher doped region formed under metallic contacts and a lower doped region which is between contacts and further discloses that typical sheet resistance values of these areas relative to one another which include the lower sheet resistance are being 10 to 30 Ω/□ and the higher sheet resistance area being 80 to 140 Ω/□ ([0042]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the sheet resistance of the first and second doped regions of modified Meier so that they are within the overlapping portions of the ranges of Fath and the instant claim because selection of overlapping portion of ranges has been held to be a prima facie case of obviousness. *In re Malagari*, 182 USPQ 549.

Response to Arguments

9. Applicant's arguments with respect to claims 1-4, 7-12, 14, 21 and 28 have been considered but are moot because the arguments do not apply to the current rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEVINA PILLAY whose telephone number is (571)270-1180. The examiner can normally be reached on Monday thru Friday 7:30am -5:00pm (EST). Examiner Fax Number is (571)-270-2180.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey T. Barton can be reached on 571-272-1307. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DEVINA PILLAY/
Primary Examiner, Art Unit 1757

Notice of References Cited	Application/Control No. 14/504,771	Applicant(s)/Patent Under Reexamination COUSINS, PETER JOHN	
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*	B	US-2009/0017606 A1	01-2009	Fath; Peter	H01L21/2255	438/558
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	D	US-				
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	G	US-				
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	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

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	V	
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

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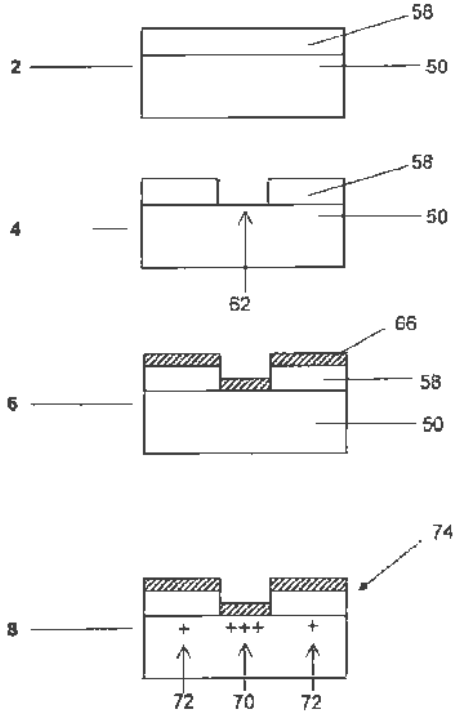
(81) Bestimmungsstaaten (*soweit nicht anders angegeben, für jede verfügbare nationale Schutzrechtsart*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS,

[Fortsetzung auf der nächsten Seite]

WO 2007/082760 A1

(54) Title: METHOD FOR FABRICATING A SEMICONDUCTOR COMPONENT HAVING REGIONS WITH DIFFERENT LEVELS OF DOPING

(54) Bezeichnung: VERFAHREN ZUR HERSTELLUNG EINES HALBLEITERBAUELEMENTS MIT UNTERSCHIEDLICH STARK DOTIERTEN BEREICHEN



(57) Abstract: Method for fabricating a semiconductor component (74; 140), particularly a solar cell (140), having regions (70, 72; 120, 122) with different levels of doping, comprising the method steps of forming (2; 14) a layer (58; 108) which inhibits diffusion of a dopant and which can be penetrated by a dopant on at least one portion (56; 106) of the surface of a semiconductor component material (50; 100), of at least partial removal (4;16a, 16b) of the diffusion-inhibiting layer (58; 108) in at least one highly doped region (62; 112a, 112b), of formation (6; 18) of a dopant source (66; 116) on the diffusion-inhibiting layer (58; 108) and in the at least one highly doped region (62; 112a, 112b), and of diffusion (8; 20) of the dopant from the dopant source (66; 116) into the semiconductor component material (50; 100) and also the use thereof in integrated circuits, electronic circuits, solar cell modules and to produce solar cells (140) with a selective emitter structure.

(57) Zusammenfassung: Verfahren zur Herstellung eines Halbleiterbauelements (74; 140), insbesondere einer Solarzelle (140), mit unterschiedlich stark dotierten Bereichen (70, 72; 120, 122) aufweisend die Verfahrensschritte des Ausbildens (2; 14) einer die Diffusion eines Dotierstoffes hemmenden und für einen Dotierstoff durchdringbaren Schicht (58; 108) auf zumindest einem Teil (56, 106) der Oberfläche eines Halbleiterbauelementmaterials (50; 100), des wenigstens teilweises Entfernens (4;16a, 16b) der diffusionhemmenden Schicht (58; 108) in wenigstens einem Hochdotierungsbereich (62, 112a, 112b), des Ausbildens (6; 18) einer Dotierstoff quelle (66; 116) auf der diffusionhemmenden Schicht (58; 108) und in dem wenigstens einen Hochdotierungsbereich (62, 112a, 112b)

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RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Bestimmungsstaaten** *(soweit nicht anders angegeben, für jede verfügbare regionale Schutzrechtsart)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), eurasisches (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), europäisches (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Veröffentlicht:

— *mit internationalem Recherchenbericht*

Zur Erklärung der Zweibuchstaben-Codes und der anderen Abkürzungen wird auf die Erklärungen ("Guidance Notes on Codes and Abbreviations") am Anfang jeder regulären Ausgabe der PCT-Gazette verwiesen.

und der Diffusion (8: 20) des Dotierstoffes aus der Dotierstoff quelle (66: 116) in das Halbleiterbauelementmaterial (50: 100) sowie dessen Ver wendung in integrierten Schaltungen, elektronischen Schaltungen, Solarzellenmodulen und zur Herstellung von Solarzellen (140) mit selektiver Emitterstruktur.

Beschreibung

Verfahren zur Herstellung eines Halbleiterbauelements mit unterschiedlich stark dotierten Bereichen

Die Erfindung betrifft ein Verfahren zur Herstellung eines Halbleiterbauelements, insbesondere einer Solarzelle, mit unterschiedlich stark dotierten Bereichen sowie dessen Verwendung in integrierten Schaltungen, elektronischen Schaltungen, Solarzellenmodulen sowie zur Herstellung von Solarzellen mit selektiver Emitterstruktur.

Bei der Herstellung vieler Halbleiterbauelemente ist es erforderlich, Bereiche mit unterschiedlich starker Dotierung vorzusehen, wobei unter Halbleiterbauelementen im Sinne dieser Patentanmeldung nicht nur kommerziell eingesetzte elektronische Bauelemente verstanden werden, sondern auch Halbfabrikate und dotierte Halbleiterstrukturen. Im Extremfall also auch ein Halbleiter, der lediglich unterschiedlich dotierte Bereiche aufweist.

Beispielsweise werden bei der Herstellung von Solarzellen Bereiche unterschiedlich starker Dotierung vorgesehen, um auf diese Weise eine Emitterstruktur auszubilden, welche in gewissen Bereichen auf einer starken Dotierung, in den übrigen Bereichen auf einer schwachen Dotierung beruht. Mit dieser so genannten selektiven Emitterstruktur, bei welcher üblicherweise auf den hoch dotierten Bereichen Metallkontakte ausgebildet werden, lässt sich bekanntermaßen eine effiziente Stromabfuhr bei gleichzeitig geringer Ladungsträgerrekombination in den übrigen schwach dotierten Bereichen realisieren.

BESTÄTIGUNGSKOPIE

Der vorliegenden Erfindung liegt daher das Problem zu Grunde, ein einfaches und aufwandsgünstiges Verfahren zur Herstellung eines Halbleiterbauelements mit unterschiedlich stark dotierten Bereichen zur Verfügung zu stellen.

Dieses Problem wird erfindungsgemäß gelöst durch ein Verfahren mit den Verfahrensschritten des unabhängigen Anspruchs 1.

Vorteilhafte Weiterbildungen sind Gegenstand abhängiger Unteransprüche.

Der Grundgedanke der Erfindung besteht darin, auf zumindest einem Teil der Oberfläche eines Halbleiterbauelementmaterials eine die Diffusion eines Dotierstoffes hemmende und für einen Dotierstoff durchdringbare Schicht auszubilden. Diese wird anschließend in wenigstens einem Hochdotierungsbereich zumindest teilweise entfernt. Im Weiteren wird eine Dotierstoffquelle auf der diffusionhemmenden Schicht und in dem wenigstens einen Hochdotierungsbereich ausgebildet. Aus dieser Dotierstoffquelle wird schließlich Dotierstoff in das Halbleiterbauelementmaterial eindiffundiert.

Bei dieser Diffusion gelangt Dotierstoff aus der in dem wenigstens einen Hochdotierungsbereich ausgebildeten Teil der Dotierstoffquelle vergleichsweise ungehindert in das Halbleiterbauelementmaterial hinein, da hier die diffusionhemmende Schicht wenigstens teilweise entfernt wurde. Nach einer gewissen Diffusionsdauer ist an diesen Stellen relativ viel Dotierstoff in das Halbleiterbauelementmaterial gelangt. In den Hochdotierungsbereichen liegt somit die erwünschte hohe Dotierung vor.

In denjenigen Bereichen hingegen, in welchen der Teil der Oberfläche des Halbleiterbauelementmaterials unter der diffusionhemmenden Schicht liegt, gelangt nur wenig Dotierstoff in das Halbleiterbauelementmaterial. In Folge wird dieses in diesen Bereichen schwach dotiert.

Auf diese Weise können einfach und aufwandsgünstig Halbleiterbauelemente mit unterschiedlich stark dotierten Bereichen hergestellt werden, insbesondere ohne dass hierfür Maskierungsschritte notwendig wären, in welchen Teile der diffundierten Bereiche des Halbleiterbauelementmaterials vor einem Abätzen mittels eines gegenüber dem Ätzmedium inerten Material geschützt werden, und ohne dass mehrere Diffusionen durchzuführen währen.

Ein derartig gefertigtes Halbleiterbauelement kann erfindungsgemäß in integrierten Schaltkreisen oder elektronischen Schaltungen verwendet werden.

Darüber hinaus ist es Bestandteil der Erfindung, das erfindungsgemäße Verfahren zur Herstellung von Halbleiterbauelemente darstellenden Solarzellen mit selektiver Emitterstruktur zu verwenden.

Überdies sieht die Erfindung vor, wenigstens eine nach dem erfindungsgemäßen Verfahren hergestellte Solarzelle zur Herstellung von Solarzellenmodulen zu verwenden.

Als Halbleiterbauelementmaterial kann grundsätzlich jedes Halbleitermaterial Verwendung finden, insbesondere Silizium oder Gallium oder deren Verbindungen. Auch die Verwendung von Verbindungshalbleitern ist selbstverständlich denkbar.

In den meisten Anwendungsfällen weist das Halbleiterbauelementmaterial eine Grunddotierung auf. So kann bspw. p-dotiertes oder n-dotiertes Silizium Verwendung finden. Hierfür können bekannte Dotierstoffe wie Phosphor oder Bor eingesetzt werden. Die einzubringenden Dotierstoffe und die diesbezüglichen Dotierstoffquellen sind unter Berücksichtigung der Funktionsweise des Halbleiterbauelements auf die im Halbleiterbauelementmaterial vorherrschende Grunddotierung abzustimmen. So ist beispielsweise bei der Herstellung einer Solarzelle mit selektiver Emitterstruktur bei einem p-dotierten Solarzellenmaterial ein n-Dotierstoff wie z.B. Phosphor zu wählen.

Eine Weiterbildung des erfindungsgemäßen Verfahrens sieht vor, dass die diffusionhemmende Schicht durch Aufspinnen und anschließende Trocknung, eine chemische Abscheidung aus der Dampfphase (CVD-Abscheidung) oder ein thermisches Aufwachsen in Ofenprozessen erfolgt. Solch ein thermisches Aufwachsen in einem Ofenprozess kann dabei beispielsweise in einem Ofen nach der Art eines aus der Halbleitertechnik bekannten Diffusionsofens erfolgen. Hierbei wird ein Stoff oder ein Stoffgemenge, gegebenenfalls unter Zuhilfenahme eines Trägergases durch ein Rohr des beheizten Ofens geleitet, wobei es mit in dem Rohr angeordneten Halbleiterbauelementmaterial derart in Wechselwirkung tritt, dass eine Anlagerung oder Abscheidung oder dergleichen der diffusionhemmenden Schicht auf dem Halbleiterbauelementmaterial eintritt.

Eine andere Ausgestaltungsvariante der Erfindung sieht vor, dass die diffusionhemmende Schicht in dem wenigstens einen Hochdotierungsbereich vollständig entfernt wird. Auf diese Weise kann an dieser Stelle ein besonders starker Dotierstoffeintrag erfolgen. Je nach Halbleiterbauelement und den zu des-

sen Herstellung weiter erforderlichen Schritten kann eine vollständige Entfernung der diffusionhemmenden Schicht jedoch auch nachteilig sein. So können beispielsweise bei mechanischem Abtrag oder bei Abtrag mittels eines Lasers, dem so genannten Ablationslaser, Schädigungen der Kristalloberfläche entstehen, welche eine erhöhte Ladungsträgerrekombination an diesen Stellen zur Folge haben. Diese wiederum kann die Funktion von Halbleiterbauelementen, beispielsweise Solarzellen, beeinträchtigen. Vor diesem Hintergrund kann es zweckmäßig erscheinen, die diffusionhemmende Schicht in dem wenigstens einen Hochdotierungsbereich nur teilweise zu entfernen und einen Rest stehen zu lassen. Dieser Rest vermag zwar die Diffusion zu behindern, doch fällt diese, bei entsprechender Auslegung der Schichtdicken und Diffusionszeiten, in den Hochdotierungsbereichen dennoch deutlich stärker aus als in den übrigen, von einer diffusionhemmenden Schicht vollständiger Dicke bedeckten Bereichen.

Durch geeignete Technologien, beispielsweise einen Ablationslaser mit ausreichend hohem Energieeintrag, kann das Entfernen der diffusionhemmenden Schicht in Hochdotierungsbereichen gegebenenfalls auch ohne Schädigung der Kristalloberfläche erfolgen. In diesen Fällen kann auf das Verbleiben einer restlichen, dünnen diffusionhemmenden Schicht in den Hochdotierungsbereichen verzichtet werden.

Ein Ausführungsbeispiel der Erfindung sieht vor, dass das Halbleiterbauelement als Solarzelle ausgeführt wird, wobei zumindest ein Teil von Metallkontakten in den Hochdotierungsbereichen angeordnet wird, vorzugsweise Fingerkontakte. Dabei sind unter Fingerkontakten feingliedrige Kontakte zu verstehen, die der Einsammlung des generierten Stromes bei gleich-

zeitig geringstmöglicher Abschattung der aktiven Solarzellenfläche dienen.

Im Folgenden wird die Erfindung anhand von Figuren näher erläutert. Es zeigen:

Figur 1: Schematische Darstellung eines ersten Ausführungsbeispiels des erfindungsgemäßen Verfahrens

Figur 2a: Schematische Darstellung eines Verfahrens zur Herstellung einer Solarzelle mit selektiver Emitterstruktur als zweites Ausführungsbeispiel des erfindungsgemäßen Verfahrens (Fortsetzung in Figur 2b)

Figur 2b: Fortsetzung des Verfahrens aus Figur 2a

Figur 1 zeigt schematisch ein erstes Ausführungsbeispiel des Verfahrens gemäß der Erfindung. Hierin wird zunächst auf einer oberseitigen Oberfläche 56 eines Halbleiterbauelementmaterials 50 eine diffusionhemmende und für einen Dotierstoff durchdringbare Schicht 58 ausgebildet 2. Im Weiteren wird die diffusionhemmende Schicht 58 in wenigstens einem Hochdotierungsbereich 62 vollständig entfernt 4.

Es folgt das Ausbilden 6 einer Dotierstoffquelle 66, aus welcher unter bestimmten Bedingungen ein Dotierstoff heraus diffundiert. Die Dotierstoffquelle 66 wird dabei auf der diffusionhemmenden Schicht 58 wie auch in dem Hochdotierungsbereich 62 aufgebracht. Im letzteren Fall kommt sie aufgrund der vollständigen Entfernung der diffusionhemmenden Schicht 58 in diesem Bereich direkt auf der oberseitigen Oberfläche 56 des Halbleiterbauelementmaterials 50 zu liegen. Bei der Dotierstoffquelle 66 kann es sich beispielsweise um ein Phosphorglas

handeln. Daneben ist jedoch prinzipiell jede andere Dotierstoffquelle denkbar.

Aus der Dotierstoffquelle 66 wird im Folgenden Dotierstoff aus- und in die oberseitige Oberfläche 56 des Halbleiterbauelementmaterials 50 eindiffundiert 8. Dies erfolgt in den meisten Fällen durch thermische Energiezufuhr. Im Falle der von der diffusionhemmenden Schicht 58 bedeckten Bereichen der oberseitigen Oberfläche 56 des Halbleiterbauelementmaterials 50 bewegt sich hierbei Dotierstoff durch die diffusionhemmende Schicht, wodurch nur ein gewisser Anteil des in der Dotierstoffquelle 66 freigesetzten Dotierstoffes in das Halbleiterbauelementmaterial gelangen kann.

Im Hochdotierungsbereich 62 hingegen gelangt der Dotierstoff ungehindert in die oberseitige Oberfläche 56 des Halberbauelementmaterials. Infolgedessen stellt sich in der Umgebung der Hochdotierungsbereichs 62 in der oberseitigen Oberfläche 56 des Halbleiterbauelementmaterials eine starke Dotierung 70 ein, wogegen in den unter der diffusionhemmenden Schicht 58 gelegenen Bereichen der oberseitigen Oberfläche 56 eine schwache Dotierung 72 resultiert.

Somit ergibt sich auf einfache Weise ein Halbleiterbauelement mit unterschiedlich stark dotierten Bereichen.

Die Figuren 2a und 2b zeigen ein Verfahren zur Herstellung einer Solarzelle mit selektiver Emitterstruktur als weiteres Ausführungsbeispiel des erfindungsgemäßen Verfahrens. Den Ausgangspunkt des Verfahrens bildet das Bereitstellen 10 des Ausgangssolarzellenmaterials, was im vorliegenden Ausführungsbeispiel durch p-dotiertes Solarzellenmaterial, insbesondere Silizium, gebildet wird. In analoger Weise könnte auch n-

dotiertes Solarzellenmaterial den Ausgangspunkt bilden. Die verwendeten Dotierstoffe und Dotierstoffquelle wären sodann entsprechend angepasst zu wählen.

Im schematisch dargestellten Fall der Figur 2a weist das Solarzellenmaterial 100 einen Sägeschaden 102 auf, wie er üblicherweise bei Halbleiterscheiben vorkommt, die von einem gegossenen Block bzw. einem gezogenen ingot durch Sägen abgetrennt wurden. Dieser Sägeschaden wird zunächst entfernt 12, was üblicherweise durch Überätzen der Siliziumscheibe bzw. des Solarzellenmaterials 100 geschieht, und eine Textur 104 in die oberseitige Oberfläche 106 des Solarzellenmaterials 100 eingebracht 12. Die Textur 104 kann dabei unter Ausnutzung bekannter Verfahren wie chemische oder mechanische Texturierung realisiert werden.

Im Folgenden wird die diffusionhemmende Schicht in Form einer porösen Schicht 108 aus Solarzellenmaterial 100 ausgebildet 14. Im Falle von Silizium als Solarzellenmaterial kann dies beispielsweise mittels einer Ätzlösung erfolgen, welche Flusssäure (HF), Salpetersäure (HNO_3) und Wasser (H_2O) enthält, vorzugsweise in einem Mischungsverhältnis von HF : HNO_3 : H_2O im Bereich von 100 : 1 bis 2 : 5 bis 10. Dabei wird die poröse Schicht 108 in einer Dicke von weniger als 200 nm ausgebildet, bevorzugt in einer Dicke im Bereich von 80 bis 120 nm.

Hernach wird Ablationslaserlicht 110 in Hochdotierungsbereichen 112a, 112b appliziert 16a. Unter diesem Energieeintrag verdampft in den Hochdotierungsbereichen die poröse Schicht 108, wobei diese jedoch im vorliegenden Ausführungsbeispiel jedoch nur teilweise entfernt wird 16b, so dass ein Rest 114a, 114b der porösen Schicht 108 bestehen bleibt. Auf diese Weise wird ausgeschlossen, dass die Oberfläche des Solarzellenmate-

rials 100, geschädigt wird und in den Hochdotierungsbereichen 112a, 112b eine Erhöhung der Ladungsträgerrekombination erfolgt.

Im Weiteren wird eine Dotierstoffquelle ausgebildet. Da es sich bei dem Solarzellenmaterial um p-dotiertes Material handelt, wird vorliegend Phosphor als gängigster n-Dotierstoff verwendet. Es können aber auch andere Dotierstoffe verwendet werden. Die Dotierstoffquelle wird in diesem Ausführungsbeispiel als Phosphorglas 116 ausgebildet. Dies kann beispielsweise in einem Ofenprozess erfolgen, in welchem das Solarzellenmaterial einem $POCl_3$-Strom, gegebenenfalls ergänzt um ein Trägergas, ausgesetzt wird. Daneben Phosphor auch in anderer Weise in einer Dotierstoffquelle zur Verfügung gestellt werden, beispielsweise durch Aufspinnen und anschließendes Trocknen einer phosphorhaltigen Paste oder Lösung oder durch chemische oder physikalische Abscheidung von phosphorhaltigen Verbindungen.

Sodann erfolgt die Diffusion 20 des Phosphors aus dem Phosphorglas, oder gegebenenfalls anderen Dotierstoffquellen, in das Solarzellenmaterial. Dabei ist die Diffusion aus dem Phosphorglas 116 in die oberseitige Oberfläche 106 des Solarzellenmaterials 100 durch die poröse Schicht aus Solarzellenmaterial 108 gehemmt. Da in diesem Ausführungsbeispiel auch in den Hochdotierungsbereichen 112a, 112b noch poröses Siliziummaterial vorliegt, ist auch hier die Diffusion gehemmt. Allerdings deutlich geringer als in denjenigen Bereichen, in denen die poröse Schicht 108 nach wie vor in ihrer gesamten Dicke vorliegt. Da in den Hochdotierungsbereichen 112a, 112b nur ein geringer Rest 114a, 114b der porösen Schicht 108 vorliegt, kann somit in diesen Bereichen in gleicher Zeit deutlich mehr Dotierstoff in die oberseitige Oberfläche 106 des Solarzellen-

materials gelangen. Infolgedessen werden hier niederohmige Emitterbereiche 120 ausgebildet. Im Übrigen werden hochohmige Emitterbereiche 122 ausgebildet. In der Summe ergibt sich eine Emitterstruktur 118 mit hochohmigen 122 und niederohmigen 120 Bereichen, die üblicherweise als selektiver Emitter bezeichnet wird.

Nach der Diffusion 20 haben die poröse Schicht 108 wie auch das als Dotierstoffquelle wirkende Phosphorglas 116 ihren Zweck erfüllt und werden gemeinsam entfernt 22. Dies erfolgt bevorzugt in einem gemeinsamen Ätzschritt.

Im Weiteren wird eine Antireflexionsbeschichtung 124 aufgebracht 24. Danach folgt das Ausbilden 26 von Metallkontakten 126,128, 130 auf der Vorderseite der Solarzelle 140 sowie auf deren Rückseite. Im vorliegenden Ausführungsbeispiel werden dabei die Metallkontakte 126 der Vorderseite auf den niederohmigen Bereichen 120 der Emitterstruktur 118 angeordnet. Auf diese Weise kann ein geringer Kontaktwiderstand zwischen der Emitterstruktur 118 und den Metallkontakten 126 gewährleistet werden, wogegen in den übrigen Bereichen ein geringe Ladungsträgerrekombination aufgrund der hochohmigen Emitterbereiche 122 vorliegt. Typische Schichtwiderstandswerte für niederohmige Emitterbereiche 120 liegen bei etwa 10 bis 30 Ω/square, für hochohmige Emitterbereiche 122 bei etwa 80 bis 140 Ω/square.

Auf der Rückseite wird zur Verbesserung der Konversionseffizienz ein an sich bekanntes back-surface-field aufgebracht, welches vorliegend aus einer flächigen Rückseitenmetallisierung aus Aluminium besteht. Dieses wird durchsetzt von wenigstens einem lokalen rückseitigen Metallkontakt 130, welcher die

Kontaktierung des p-dotierten Solarzellenmaterials 100 bewerkstelligt.

Das erfindungsgemäße Verfahren lässt sich offensichtlich auch auf andere Solarzellenkonzepte als das in Verbindung mit den Figuren 2a und 2b beschriebene übertragen. Insbesondere kann es bei Bifacialzellen, bei welchen sowohl die Vorder- als auch die Rückseite der Solarzelle für die Stromgeneration genutzt werden, wie auch bei vollständig rückseitig kontaktierten Solarzellen Verwendung finden.

Bezugszeichenliste

2 Ausbilden diffusionhemmende Schicht
4 vollständiges Entfernen der diffusionhemmenden Schicht in Hochdotierungsbereich
6 Ausbilden Dotierstoffquelle
8 Diffundieren des Dotierstoffes aus Dotierstoffquelle in Halbleiterbauelementmaterial

10 Bereitstellen des Ausgangssolarzellenmaterials
12 Entfernen des Sägeschadens und Texturierung der Oberfläche des Solarzellenmaterials
14 Ausbilden einer porösen Schicht aus Solarzellenmaterial
16a Applizieren von Ablationslaserlicht
16b teilweises Entfernen der porösen Schicht in Hochdotierungsbereichen
18 Ausbilden von Phosphorglas als Dotierstoffquelle
20 Diffundieren des Phosphors aus dem Phosphorglas in das Solarzellenmaterial
22 Gemeinsames Entfernen des Phosphorglases und der porösen Schicht
24 Aufbringen einer Antireflexionsbeschichtung
26 Ausbilden von Metallkontakten auf der Vorder- und Rückseite

50 Halbleiterbauelementmaterial
56 oberseitige Oberfläche des Halbleiterbauelementmaterials
58 diffusionhemmende Schicht
62 Hochdotierungsbereich
66 Dotierstoffquelle
70 stark dotierter Bereich
72 schwach dotierter Bereich

74 Halbleiterbauelement

100 p-dotiertes Solarzellenmaterial
102 Sägeschaden
104 Textur
106 oberseitige Oberfläche des Solarzellenmaterials
108 poröse Schicht aus Solarzellenmaterial
110 Ablationslaserlicht
112a Hochdotierungsbereich
112b Hochdotierungsbereich
114a Rest der porösen Schicht
114b Rest der porösen Schicht
116 Phosphorglas
118 Selektive Emitterstruktur
120 niederohmiger Emitterbereich
122 hochohmiger Emitterbereich
124 Antireflexionsbeschichtung
126 Metallkontakte auf der Vorderseite
128 flächige Rückseitenmetallisierung
130 lokaler Metallkontakt auf der Rückseite
140 Solarzelle

Patentansprüche

1. Verfahren zur Herstellung eines Halbleiterbauelem ...
(74;140) mit unterschiedlich stark dotierten Bereichen (70,72) aufweisend die Verfahrensschritte
- des Ausbildens (2; 14) einer die Diffusion eines Dotierstoffes hemmenden und für einen Dotierstoff durchdringbaren Schicht (58; 108) auf zumindest einem Teil (56; 106) der Oberfläche eines Halbleiterbauelementmaterials (50; 100);
- des wenigstens teilweises Entfernens (4; 16a, 16b) der diffusionhemmenden Schicht (58; 108) in wenigstens einem Hochdotierungsbereich (62; 112a, 112b);
- des Ausbildens (6; 18) einer Dotierstoffquelle (66; 116) auf der diffusionhemmenden Schicht (58; 108) und in dem wenigstens einen Hochdotierungsbereich (62; 112a, 112b);
- der Diffusion (8; 20) des Dotierstoffes aus der Dotierstoffquelle (66; 116) in das Halbleiterbauelementmaterial (50; 100).

2. Verfahren nach Anspruch 1,
d a d u r c h g e k e n n z e i c h n e t, dass
die Ausbildung (2; 14) der diffusionhemmenden Schicht (58; 108) durch Aufbringen einer Siliziumnitrid-, einer Siliziumoxid-, einer Titanoxid-, einer Tantaloxidschicht oder einer Schicht aus Oxiden anderer Übergangsmetalle erfolgt, wobei im Falle der Übergangsmetalloxidschichten vorzugsweise solche Übergangsmetalle verwendet werden, welche eine vergleichsweise kleine Diffusionskonstante im Halbleiterbauelementmaterial (50; 100) aufweisen.

3. Verfahren nach einem der Ansprüche 1 bis 2,
d a d u r c h g e k e n n z e i c h n e t, dass
die diffusionhemmende Schicht (58; 108) in einer Dicke von wenigen Nanometern bis zu wenigen Mikrometern ausgebildet wird, vorzugsweise im Dickenbereich von 20 nm bis 300 nm.

4. Verfahren nach einem der Ansprüche 1 bis 3,
d a d u r c h g e k e n n z e i c h n e t, dass
das Ausbilden (2; 14) der diffusionhemmenden Schicht (58; 108) durch Aufspinnen und anschließende Trocknung, eine chemische Abscheidung aus der Dampfphase (CVD-Abscheidung) oder thermisches Aufwachsen in Ofenprozessen erfolgt.

5. Verfahren nach Anspruch 1,
d a d u r c h g e k e n n z e i c h n e t, dass
als diffusionhemmende Schicht (108) eine poröse Schicht (108) ausgebildet wird.

6. Verfahren nach Anspruch 5,
d a d u r c h g e k e n n z e i c h n e t, dass die poröse Schicht (108) aus Halbleiterbauelementmaterial (100) ausgebildet wird.

7. Verfahren nach einem der Ansprüche 5 bis 6,
d a d u r c h g e k e n n z e i c h n e t, dass
die poröse Schicht (108) in einer Dicke von weniger als 200 nm ausgebildet wird, vorzugsweise in einer Dicke im Bereich von 80 bis 120 nm.

8. Verfahren nach einem der Ansprüche 6 bis 7,
d a d u r c h g e k e n n z e i c h n e t, dass

zur Ausbildung der porösen Schicht (108) aus Halbleiterbauelementmaterial (100) wenigstens der Teil (106) der Oberfläche des Halbleiterbauelements einer Ätzlösung ausgesetzt wird.

9. Verfahren nach Anspruch 8,
dadurch gekennzeichnet, dass
die Ätzlösung Flusssäure (HF), Salpetersäure (HNO_3) und Wasser (H_2O) enthält, vorzugsweise in einem Mischungsverhältnis von HF : HNO_3 : H_2O im Bereich von 100 : 1 bis 2 : 5 bis 10.

10. Verfahren nach einem der Ansprüche 6 bis 7,
dadurch gekennzeichnet, dass
zur Ausbildung der porösen Schicht (108) aus Halbleiterbauelementmaterial (100) wenigstens der Teil (106) der Oberfläche des Halbleiterbauelements einem ätzenden Plasma ausgesetzt wird.

11. Verfahren nach einem der Ansprüche 1 bis 10,
dadurch gekennzeichnet, dass
das wenigstens teilweise Entfernen (4; 16a, 16b) der diffusionhemmenden Schicht (58; 108) in dem wenigstens einen Hochdotierungsbereich (62; 112a, 112b) mittels Ablationslaserlicht (110) erfolgt, vorzugsweise mittels Licht eines frequenzverdoppelten oder frequenzverdreifachten Ablationslasers.

12. Verfahren nach einem der Ansprüche 1 bis 10,
dadurch gekennzeichnet, dass
das wenigstens teilweise Entfernen (4; 16b) der diffusionhemmenden Schicht (58; 108) in dem wenigstens einen Hochdotierungsbereich (62; 112a, 112b) mittels einer ät-

zenden Paste, vorzugsweise einer Flusssäure enthaltenden Paste erfolgt.

13. Verfahren nach Anspruch 12, dadurch gekennzeichnet, dass die ätzende Paste mittels einer Druck- oder Spritztechnik auf den wenigstens einen Hochdotierungsbereich (62; 112a, 112b) aufgebracht wird, vorzugsweise mittels einer Siebdruck-, Stempeldruck-, Spritzendruck- oder Rollendrucktechnik.

14. Verfahren nach einem der Ansprüche 1 bis 13, dadurch gekennzeichnet, dass die diffusionhemmende Schicht (58) in dem wenigstens einen Hochdotierungsbereich (62) vollständig entfernt wird (4).

15. Verfahren nach einem der Ansprüche 1 bis 14, dadurch gekennzeichnet, dass der Schichtwiderstand in unter der nicht entfernten diffusionhemmenden Schicht (58; 108) gelegenen Bereichen (72; 122) des Teils (56; 106) der Oberfläche des Halbleiterbauelementmaterials (50; 100) durch die Dicke der diffusionhemmenden Schicht (58; 108) bestimmt wird.

16. Verfahren nach einem der Ansprüche 1 bis 15, dadurch gekennzeichnet, dass als Halbleiterbauelementmaterial (50; 100) Silizium verwendet wird, vorzugsweise p-dotiertes (100) oder n-dotiertes Silizium.

17. Verfahren nach einem der Ansprüche 1 bis 16, dadurch gekennzeichnet, dass

nach der Diffusion (8; 20) des Dotierstoffes aus der Dotierstoffquelle (66; 116) in den Teil (56; 106) der Oberfläche des Halbleiterbauelementmaterials (50; 100) die Dotierstoffquelle (66; 116) zusammen mit der diffusionhemmenden Schicht (58; 108) entfernt wird.

18. Verfahren nach einem der Ansprüche 1 bis 17, dadurch gekennzeichnet, dass das Halbleiterbauelement als Solarzelle (140) ausgeführt wird, wobei zumindest ein Teil von Metallkontakten (126), vorzugsweise Fingerkontakte, in Hochdotierungsbereichen (112a, 112b) angeordnet wird.

19. Verfahren nach Anspruch 18, dadurch gekennzeichnet, dass sowohl auf der Vorderseite der Solarzelle wie auch auf deren Rückseite Hochdotierungsbereiche (112a, 112b) vorgesehen werden.

20. Verfahren nach einem der Ansprüche 18 bis 19, dadurch gekennzeichnet, dass die Solarzelle als vorder- wie rückseitig lichtempfindliche Bifacialzelle ausgeführt wird.

21. Verfahren nach einem der Ansprüche 18 bis 20, dadurch gekennzeichnet, dass die Dotierstoffquelle (66; 116) aus Phosphorglas (116) gebildet wird, als diffusionhemmende Schicht (58; 108) poröses Solarzellenmaterial (108) verwendet wird und das Phosphorglas (116) zusammen mit der Schicht porösen Solarzellenmaterials (108) durch Ätzen in einer Ätzlösung oder einem Plasma entfernt wird.

22. Verfahren nach einem der Ansprüche 18 bis 21, dadurch gekennzeichnet, dass die Hochdotierungsbereiche (62; 112a, 112b) breiter ausgeführt werden als die später in diesen Bereichen aufgebrachte Metallisierung (126).

23. Verwendung eines nach einem der Ansprüche 1 bis 17 gefertigten Halbleiterbauelements (74) in integrierten Schaltkreisen.

24. Verwendung eines nach einem der Ansprüche 1 bis 17 gefertigten Halbleiterbauelements (74) in elektronischen Schaltungen.

25. Verwendung wenigstens einer nach einem der Ansprüche 18 bis 22 gefertigten Solarzelle (140) zur Herstellung eines Solarzellenmoduls.

26. Verwendung eines Verfahrens nach einem der Ansprüche 18 bis 22 zur Herstellung einer Solarzelle (140) mit selektiver Emitterstruktur (118).

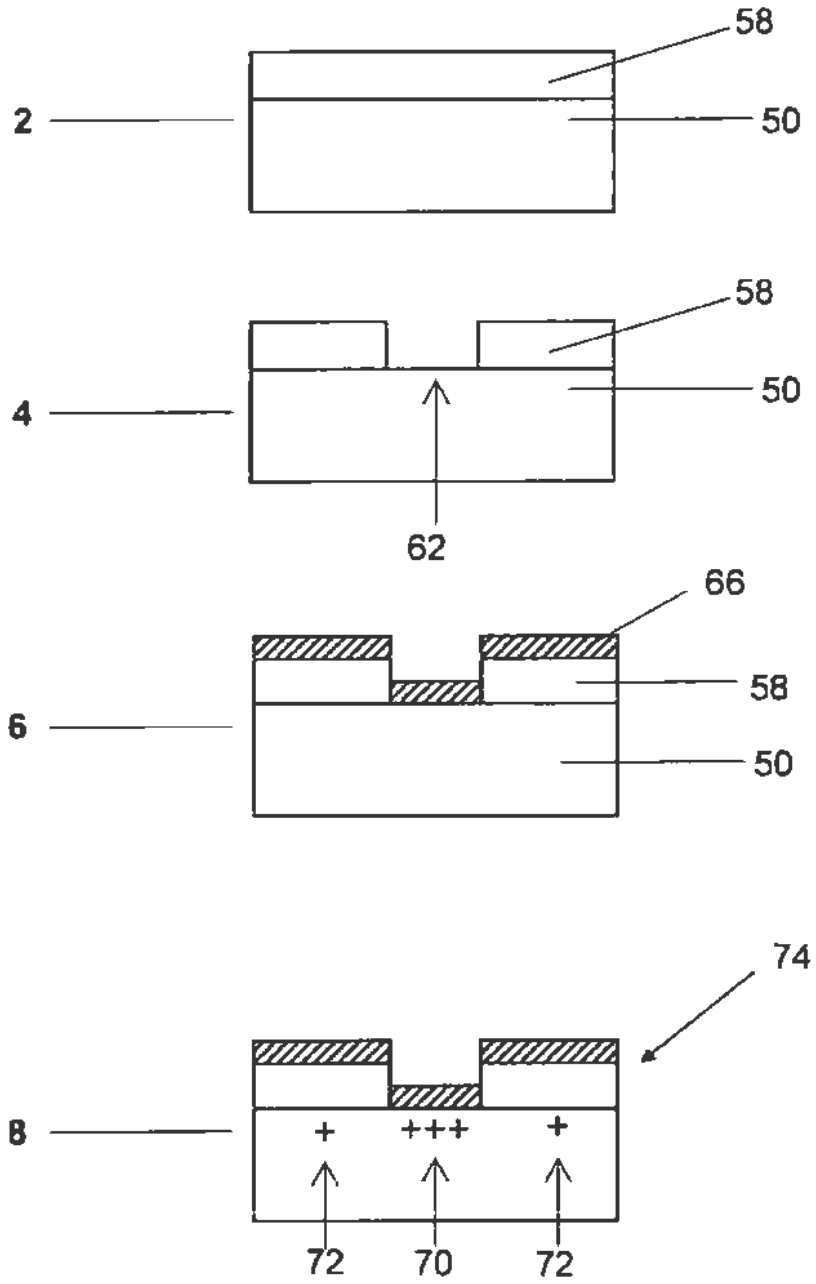


Fig. 1

2/3

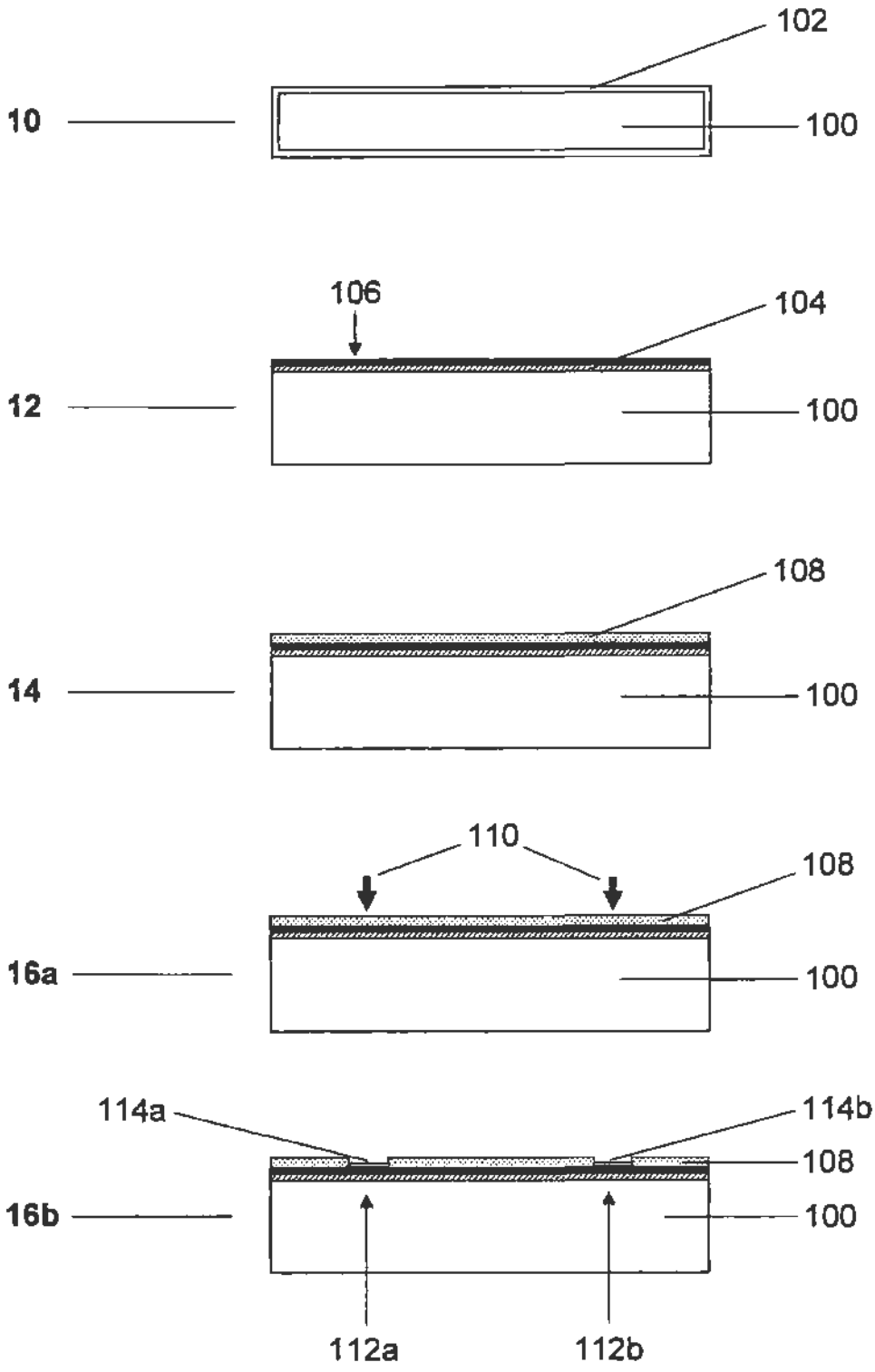

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106
104
12
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110
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114a
114b
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16b
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112a
112b

Fig. 2a

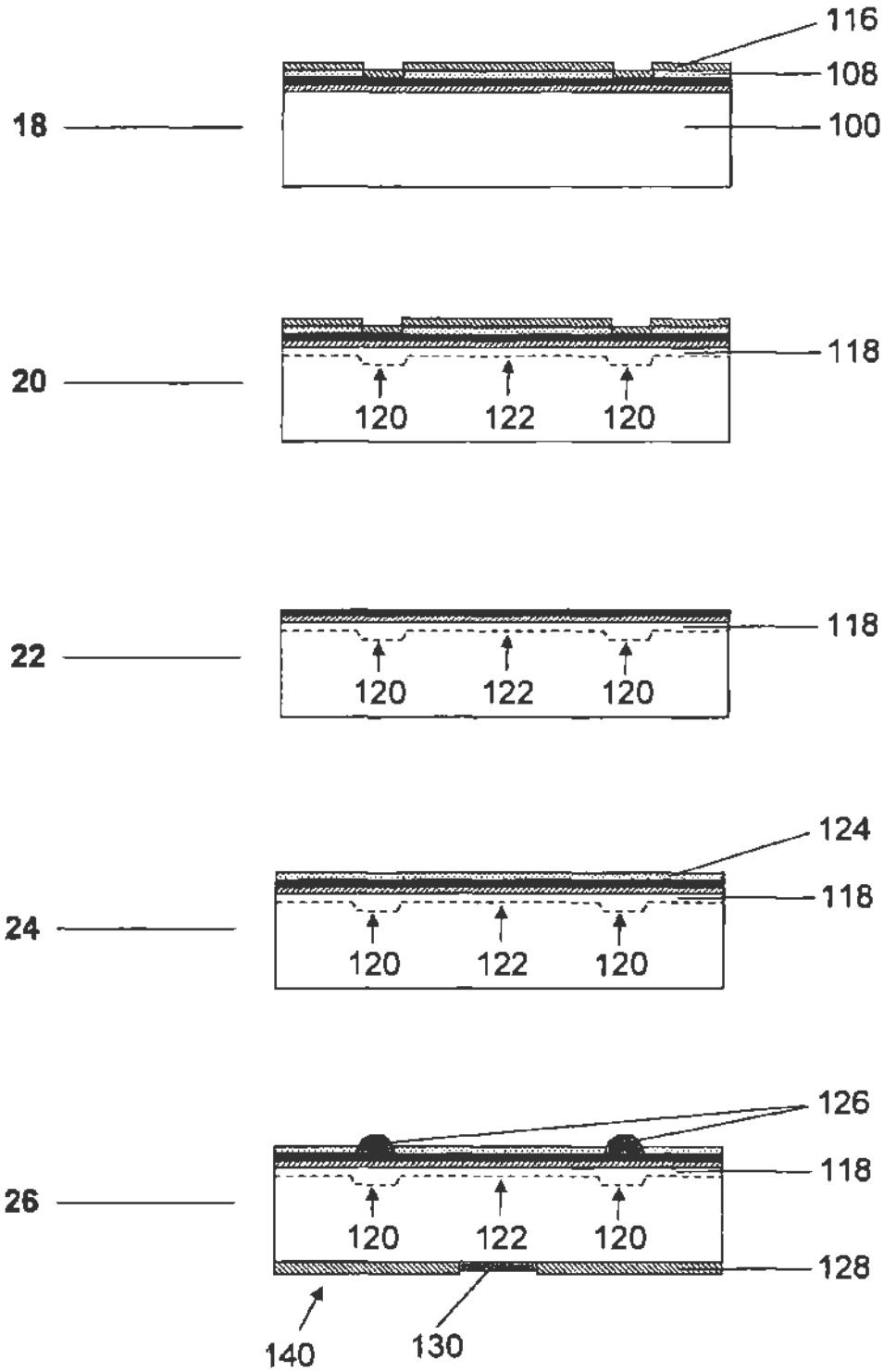

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Fig. 2b

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2007/000463

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/225 H01L27/142 H01L31/0224

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 4 152 824 A (GONSIORAWSKI RONALD) 8 May 1979 (1979-05-08) sequence ZUSAMMENFASSUNG column 3, lines 30-51 column 3, line 68 - column 4, line 1 column 4, lines 35-40,60-63 column 5, lines 38-63 column 6, lines 18-20,28-42 column 7, lines 60-63 figures 1,2,7 ——— -/--	1,2,4, 12-19, 22,25,26 3,5-11, 20,21, 23,24

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
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"P" document published prior to the international filing date but later than the priority date claimed

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 April 2007	27/04/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl Fax: (+31-70) 340-3016	Markmann, Markus

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2007/000463

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	YEROKHOV V YU ET AL: "Photoconversion in solar cell structures with porous silicon" PROCEEDINGS OF THE SPIE - THE INTERNATIONAL SOCIETY FOR OPTICAL ENGINEERING SPIE-INT. SOC. OPT. ENG USA, vol. 3580, 1998, pages 168-177, XP002428596 ISSN: 0277-786X sequences 2.1, 2.2 SEITE 169, ABSATZ 1	3,5-10, 21
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Information on patent family members

International application No
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INTERNATIONALER RECHERCHENBERICHT

Internationales Aktenzeichen
PCT/EP2007/000463

A. KLASSIFIZIERUNG DES ANMELDUNGSGEGENSTANDES
INV. H01L21/225 H01L27/142 H01L31/0224

Nach der Internationalen Patentklassifikation (IPC) oder nach der nationalen Klassifikation und der IPC

B. RECHERCHIERTE GEBIETE

Recherchierter Mindestprüfstoff (Klassifikationssystem und Klassifikationssymbole)
H01L

Recherchierte, aber nicht zum Mindestprüfstoff gehörende Veröffentlichungen, soweit diese unter die recherchierten Gebiete fallen

Während der internationalen Recherche konsultierte elektronische Datenbank (Name der Datenbank und evtl. verwendete Suchbegriffe)
EPO-Internal, WPI Data, INSPEC

C. ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie*	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
X	US 4 152 824 A (GONSIORAWSKI RONALD) 8. Mai 1979 (1979-05-08)	1,2,4, 12-19, 22,25,26
Y	Sequenz ZUSAMMENFASSUNG Spalte 3, Zeilen 30-51 Spalte 3, Zeile 68 - Spalte 4, Zeile 1 Spalte 4, Zeilen 35-40,60-63 Spalte 5, Zeilen 38-63 Spalte 6, Zeilen 18-20,28-42 Spalte 7, Zeilen 60-63 Abbildungen 1,2.7	3,5-11, 20,21, 23,24

-/--

[X] Weitere Veröffentlichungen sind der Fortsetzung von Feld C zu entnehmen [X] Siehe Anhang Patentfamilie

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Datum des Abschlusses der internationalen Recherche	Absendedatum des internationalen Recherchenberichts
10. April 2007	27/04/2007

Name und Postanschrift der Internationalen Recherchenbehörde	Bevollmächtigter Bediensteter
Europäisches Patentamt, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Markmann, Markus

Formblatt PCT/ISA/210 (Blatt 2) (April 2005)

INTERNATIONALER RECHERCHENBERICHT

Internationales Aktenzeichen
PCT/EP2007/000463

C. (Fortsetzung) ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie*	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
Y	YEROKHOV V YU ET AL: "Photoconversion in solar cell structures with porous silicon" PROCEEDINGS OF THE SPIE - THE INTERNATIONAL SOCIETY FOR OPTICAL ENGINEERING SPIE-INT. SOC. OPT. ENG USA, Bd. 3580, 1998, Seiten 168-177, XP002428596 ISSN: 0277-786X Sequenzen 2.1, 2.2 SEITE 169, ABSATZ 1	3,5-10, 21
Y	RALPH KUHN ET AL: "Characterization of Novel Mono- and Bifacially Active Semi-Transparent Crystalline Silicon Solar Cells" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ, US, Bd. 46, Nr. 10, Oktober 1999 (1999-10), XP011017052 ISSN: 0018-9383 Zusammenfassung	20
Y	US 2005/172996 A1 (HACKE PETER [US] ET AL) 11. August 2005 (2005-08-11) Absätze [0045], [0053]	11
X Y	GB 1 172 491 A (HITACHI LTD [JP]) 3. Dezember 1969 (1969-12-03) Seite 1, Zeilen 9-15 Seite 2, Zeile 106 - Seite 3, Zeile 6 Seite 3, Zeilen 60-65 Abbildung 2b	1-4,12, 14-16 23,24
X	US 3 541 678 A (MCDONALD BRUCE A) 24. November 1970 (1970-11-24) Sequenz ZUSAMMENFASSUNG Spalte 2, Zeile 71 - Spalte 3, Zeile 44 Abbildungen 2,3	1-4,12, 15,16, 23,24
X	WO 01/24279 A (STICHTING ENERGIE [NL]; BULTMAN JAN HENDRIK [NL]) 5. April 2001 (2001-04-05) Sequenz ZUSAMMENFASSUNG Seite 2, Zeilen 28-33 Seite 4, Zeilen 1-11,24-30	1,2,4, 14-17, 25,26
A	YEROKHOV V Y ET AL: "Porous silicon in solar cell structures: a review of achievements and modern directions of further use" RENEWABLE AND SUSTAINABLE ENERGY REVIEWS, ELSEVIERS SCIENCE, NEW YORK, NY, US, Bd. 3, Nr. 4, Dezember 1999 (1999-12), Seiten 291-322, XP004268410 ISSN: 1364-0321 Sequenz 4.2	3,5-9,21

Formblatt PCT/ISA/210 (Fortsetzung von Blatt 2) (April 2005)

INTERNATIONALER RECHERCHENBERICHT

Angaben zu Veröffentlichungen, die zur selben Patentfamilie gehören

Internationales Aktenzeichen
PCT/EP2007/000463

Im Recherchenbericht angeführtes Patentdokument		Datum der Veröffentlichung	Mitglied(er) der Patentfamilie		Datum der Veröffentlichung
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WO 0124279	A	05-04-2001	AU	7457600 A	30-04-2001
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			JP	2003510852 T	18-03-2003
			NL	1012961 C2	05-03-2001
			US	6756290 B1	29-06-2004

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14504771	COUSINS, PETER JOHN
	Examiner	Art Unit
	DEVINA PILLAY	1755

CPC- SEARCHED		
Symbol	Date	Examiner
H01L31/0236 H01L31/0745 H01L31/1804	6/8/2016	DP
H01L31/022425 H01L31/068 H01L31/182 H01L31/056	6/8/2016	DP
Y02E10/52 Y02P70/521 Y02E10/547	6/8/2016	DP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor name search in PALM	6/8/2016	DP
EAST Text Search (See Search History)	6/8/2016	DP
Updated Inventor name search in PALM	10/5/2016	DP
Updated Inventor name search in PALM	2/1/2017	DP
Updated EAST Text Search (See Search History)	6/26/2017	DP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14504771	COUSINS, PETER JOHN
	Examiner	**Art Unit**
	DEVINA PILLAY	1755

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/17/2016	06/08/2016	10/05/2016	01/31/2017	06/26/2017				
	1	÷	✓	✓	✓	✓				
	2	÷	✓	✓	✓	✓				
	3	÷	✓	✓	✓	✓				
	4	÷	✓	✓	✓	✓				
	5	÷	✓	-	-	-				
	6	÷	✓	✓	✓	-				
	7	÷	✓	✓	✓	✓				
	8	÷	✓	✓	✓	✓				
	9	÷	✓	✓	✓	✓				
	10	÷	✓	✓	✓	✓				
	11	÷	✓	✓	✓	✓				
	12	÷	✓	✓	✓	✓				
	13	÷	✓	✓	✓	-				
	14	÷	✓	✓	✓	✓				
	15	÷	N	-	-	-				
	16	÷	N	-	-	-				
	17	÷	N	-	-	-				
	18	÷	N	-	-	-				
	19	÷	N	-	-	-				
	20	÷	N	-	-	-				
	21					✓				
	22					✓				

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S400	1	"14504771"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 12:27
S401	73	"6262359"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 12:30
S402	76	(US-20050268963-$ or US-20020153039-$ or US-20060196535-$ or US-20090101199-$ or US-20040097062-$ or US-20040112426-$ or US-20070186970-$ or US-20050272175-$ or US-20040063326-$ or US-20100224238-$ or US-20100000597-$ or US-20070256728-$ or US-20060060238-$ or US-20080092944-$ or US-20110162706-$ or US-20070151598-$ or US-20080092951-$ or US-20110104618-$ or US-20080223446-$ or US-20070151599-$ or US-20090205712-$ or US-20100186803-$ or US-20090142880-$ or US-20060255340-$ or US-20050017257-$ or US-20100186802-$).did. or (US-20020142500-$ or US-20040003836-$ or US-20100087031-$).did. or (US-4379944-$ or US-4665277-$ or US-5320684-$ or US-6210991-$ or US-5792280-$ or US-5899704-$ or US-6262359-$ or US-5258077-$ or US-6071753-$ or US-7468485-$ or US-7838400-$ or US-5641362-$ or US-8222516-$ or US-3961997-$ or US-5057439-$ or US-8207443-$ or US-5138256-$ or US-7633006-$ or US-6130380-$ or US-5738731-$ or US-4927770-$ or US-6624049-$ or US-4152824-$ or US-6214743-$ or US-7029943-$ or US-6998288-$) did. or (US-8878053-$ or US-8207444-$ or US-5538564-$ or US-7566974-$ or US-5030295-$ or US-6407012-$ or US-5563092-$ or US-7858430-$ or US-7554031-$).did or (WO-2009094578-$	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/06/26 12:33

		or WO-2009094578-$).did. or (WO-2009094578-$).did. or (US-20090205712-$ or US-20080121279-$ or WO-2007130188-$ or US-7468485-$ or JP-07106611-$ or US-20040200520-$ or JP-2004247364-$ or US-5030295-$ or WO-03083955-$).did.				
S403	25	S402 and (contact near2 (resistance resistivi$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 12:34
S404	787	(solar photovoltaic).ab. and (contact near2 (resistance resistivi$3)) near7 (dop$3 diffus$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 12:39
S405	678	(solar photovoltaic).ab and (contact near2 (resistance resistivi$3)) near7 (dop$3 diffus$4) and (crystal$4 wafer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 12:43
S406	230	(solar photovoltaic) ab and (contact near2 (resistance resistivi$3)) near7 (dop$3 diffus$4) and (crystal$4 wafer) and ohms	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 12:46
S409	196	(solar photovoltaic).ab. and (contact near2 (resistance resistivi$3)) near7 (dop$3 diffus$4) and (crystal$4 wafer) and omega	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 12:51
S408	1	S400 and omega	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 12:51
S410	14	("3620829" | "4078945" | "4227942" | "4640001" | "4675466").PN. OR ("5759292").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/26 13:16
S411	66	(solar photovoltaic).ab. and (contact near2 (resistance resistivi$3)) near7 (dop$3 diffus$4) same omega	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 13:20
S413	153	S412 not S411	US-PGPUB; USPAT;	OR	ON	2017/06/26 13:22

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S412	219	(solar photovoltaic).ab. and (contact near2 (resistance resistivi$3)) same omega	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 13:22
S415	1	2007-797066.NRAN.	DERWENT	OR	ON	2017/06/26 13:26
S414	9	"20090017606"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 13:26
S416	1	2007-797066.NRAN.	DERWENT	OR	ON	2017/06/26 13:28
S417	120	"4152824"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 13:29
S419	107	S418 not S412	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 14:07
S418	209	(solar photovoltaic).ab. and (contact near2 (resistance resistivi$3)) near7 (dop$3 diffus$4) and omega	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 14:07
S420	131	(solar photovoltaic).ab. and (contact near2 (resistance resistivi$3)) near7 (dop$3 diffus$4) and (back rear) near2 (junction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 14:18
S421	3	"20100197126"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 14:23
S422	210	"6429037"	US-PGPUB; USPAT;	OR	ON	2017/06/26 14:25

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L3	34	2 and polysilicon	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/06/26 15:56
L2	82	(US-20050268963-$ or US-20020153039-$ or US-20060196535-$ or US-20090101199-$ or US-20040097062-$ or US-20040112426-$ or US-20070186970-$ or US-20050272175-$ or US-20040063326-$ or US-20100224238-$ or US-20100000597-$ or US-20070256728-$ or US-20060060238-$ or US-20080092944-$ or US-20110162706-$ or US-20070151598-$ or US-20080092951-$ or US-20110104618-$ or US-20080223446-$ or US-20070151599-$ or US-20090205712-$ or US-20100186803-$ or US-20090142880-$ or US-20060255340-$ or US-20050017257-$ or US-20100186802-$).did. or (US-20020142500-$ or US-20040003836-$ or US-20100087031-$ or US-20090017606-$ or US-20090183768-$ or US-20110139231-$).did. or (US-4379944-$ or US-4665277-$ or US-5320684-$ or US-6210991-$ or US-5792280-$ or US-5899704-$ or US-6262359-$ or US-5258077-$ or US-6071753-$ or US-7468485-$ or US-7838400-$ or US-5641362-$ or US-8222516-$ or US-3961997-$ or US-5057439-$ or US-8207443-$ or US-5138256-$ or US-7633006-$ or US-6130380-$ or US-5738731-$ or US-4927770-$ or US-6624049-$ or US-4152824-$ or US-6214743-$ or US-7029943-$ or US-6998288-$).did. or (US-8878053-$ or US-8207444-$ or US-5538564-$ or US-7566974-$ or US-5030295-$ or US-6407012-$ or US-5563092-$ or US-7858430-$ or US-7554031-$ or US-5759292-$ or US-6429037-$).did. or (WO-2009094578-$ or WO-2009094578-$).did. or (WO-2009094578-$).did. or (US-20090205712-$ or US-20080121279-$ or WO-2007130188-$ or US-7468485-$ or JP-07106611-$ or US-20040200520-$ or JP-2004247364-$ or US-5030295-$ or WO-03083955-$ or WO-2007082760-$).did.	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/06/26 15:56
L6	1235	(silicon near nitride "Si.sub.3N.sub.4") near5 dielectric and (solar photovoltaic).ab.	US-PGPUB; USPAT; FPRS; EPO;	OR	ON	2017/06/26 16:59

			DERWENT			
L5	1931	(silicon near nitride "Si.sub.3N.sub.4") with dielectric and (solar photovoltaic).ab.	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/06/26 16:59
L4	105792	(silicon near nitride "Si.sub.3N.sub.4") with dielectric	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/06/26 16:59
L8	373	(silicon near nitride "Si.sub.3N.sub.4") near8 (titanium dioxide "TiO.sub.2") with dielectric and (solar photovoltaic).ab. and H01L31$.cpc.	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/06/26 17:00
L7	785	(silicon near nitride "Si.sub.3N.sub.4") near5 dielectric and (solar photovoltaic).ab. and H01L31$.cpc.	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/06/26 17:00
L9	91	(silicon near nitride "Si.sub.3N.sub.4") near8 (titanium near dioxide "TiO.sub.2") with dielectric and (solar photovoltaic).ab. and H01L31$.cpc.	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/06/26 17:01
L12	17	11 and omega	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/06/26 17:59
L11	82	(US-20050268963-$ or US-20020153039-$ or US-20060196535-$ or US-20090101199-$ or US-20040097062-$ or US-20040112426-$ or US-20070186970-$ or US-20050272175-$ or US-20040063326-$ or US-20100224238-$ or US-20100000597-$ or US-20070256728-$ or US-20060060238-$ or US-20080092944-$ or US-20110162706-$ or US-20070151598-$ or US-20080092951-$ or US-20110104618-$ or US-20080223446-$ or US-20070151599-$ or US-20090205712-$ or US-20100186803-$ or US-20090142880-$ or US-20060255340-$ or US-20050017257-$ or US-20100186802-$).did. or (US-20020142500-$ or US-20040003836-$ or US-20100087031-$ or US-20090017606-$ or US-20090183768-$ or US-20110139231-$).did. or (US-4379944-$ or US-4665277-$ or US-5320684-$ or US-6210991-$ or US-5792280-$ or US-5899704-$ or US-6262359-$ or US-5258077-$ or US-6071753-$ or US-7468485-$ or US-7838400-$ or US-5641362-$ or US-8222516-$ or US-3961997-$ or US-5057439-$ or US-8207443-$ or US-5138256-$ or US-7633006-$ or US-	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/06/26 17:59

		6130380-$ or US-5738731-$ or US-4927770-$ or US-6624049-$ or US-4152824-$ or US-6214743-$ or US-7029943-$ or US-6998288-$).did. or (US-8878053-$ or US-8207444-$ or US-5538564-$ or US-7566974-$ or US-5030295-$ or US-6407012-$ or US-5563092-$ or US-7858430-$ or US-7554031-$ or US-5759292-$ or US-6429037-$).did. or (WO-2009094578-$ or WO-2009094578-$).did. or (WO-2009094578-$).did. or (US-20090205712-$ or US-20080121279-$ or WO-2007130188-$ or US-7468485-$ or JP-07106611-$ or US-20040200520-$ or JP-2004247364-$ or US-5030295-$ or WO-03083955-$ or WO-2007082760-$).did.				
L13	1	2007-797066.NRAN.	DERWENT	OR	ON	2017/06/26 18:03
L15	1	2007-797066.NRAN.	DERWENT	OR	ON	2017/06/26 18:09
L16	21	"8222516"	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/06/26 18:27
L17	27	"8207444"	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/06/26 18:28

EAST Search History (Interference)

<This search history is empty>

6/26/2017 7:00:57 PM
C:\Users\dpillay\Documents\EAST\Workspaces\14504771.wsp

Docket No. 10031.004211

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:

Peter John COUSINS

Application No.: 14/504,771 Examiner: PILLAY. DEVINA

Filing Date: October 2, 2014 Art Unit: 1757

Title: FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

RESPONSE TO OFFICE ACTION AND AMENDMENT

INTRODUCTORY COMMENTS

This paper is responsive to the office action mailed on June 30, 2017.

Please amend the above-identified application as follows:

AMENDMENTS TO THE SPECIFICATION

A. Please replace the paragraph beginning on page 1, line 6 with the following paragraph:

> This application is a continuation of U.S. Application No. 13/495,577, filed on June 13, 2012, now U.S. Patent No. 8,878,053, which is a divisional of U.S. Application No. 12/070,742, filed on February 20, 2008, now U.S. Patent No. 8,222,516. The just-mentioned disclosures are incorporated herein by reference in their entirety.

AMENDMENTS TO THE CLAIMS

1. (Currently amended) A solar cell, comprising:

a substrate having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

~~a first doped region and a second doped region in the substrate~~ an oxide layer disposed on the front surface of the substrate~~, the first doped region having a sheet resistance that is higher than a sheet resistance of the second doped region~~;

an anti-reflective coating on the oxide layer;

a tunnel dielectric disposed over the back surface of the substrate;

an emitter disposed over the tunnel dielectric, the emitter forming a backside junction with the substrate;

a doped diffusion region in the substrate;

a front electrode that is coupled to the ~~second~~ doped diffusion region on the front surface of the substrate; and

a back electrode that is coupled to the emitter on ~~disposed over~~ the back surface of the substrate.

2. (Original) The solar cell of claim 1, wherein the emitter is a polysilicon emitter.

3. (Original) The solar cell of claim 1, wherein the substrate is a monocrystalline silicon substrate.

4. (Currently) The solar cell of claim 1, wherein the ~~first~~ tunnel dielectric is a tunnel oxide.

5. (Canceled)

6. (Canceled)

7. (Original) The solar cell of claim 1, wherein the back electrode includes silver.

8. (Canceled)

9. (Currently amended) A solar cell, comprising:

a substrate having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

~~a first doped region and a second doped region in the substrate on the front surface of the substrate, the first doped region having a sheet resistance that is higher than a sheet resistance of the second doped region~~;

a doped diffusion region in the substrate on the front surface of the substrate;

an emitter over the back surface of the substrate, the emitter forming a backside junction with the substrate;

a first dielectric between the emitter and the back surface;

a front electrode disposed on the front surface of the substrate and is coupled to the ~~second~~ doped diffusion region;

a second dielectric on the front surface of the substrate;

an anti-reflective coating on the second dielectric; and

a back electrode disposed on the back surface of the substrate.

10. (Original) The solar cell of claim 9, wherein the emitter is a polysilicon emitter.

11. (Original) The solar cell of claim 9, wherein the substrate is a monocrystalline silicon substrate.

12. (Original) The solar cell of claim 9, wherein the first dielectric is an oxide.

13. (Canceled)

14. (Original) The solar cell of claim 9, wherein the back electrode includes silver.

15-22. (Canceled)

REMARKS

Claims 1-4, 7, 9-12, and 14 remain in the application and stand rejected. Reconsideration of the rejection is respectfully requested in light of the following reasons.

Claim amendments have been made to expedite prosecution. Applicant expressly reserves the right to pursue the original version of an amended claim in a continuing application.

Claim Amendments

Applicant maintains the arguments presented in the Pre-Appeal Brief Request for Review submitted by the applicant on March 28, 2017 for purposes of appeal.

As previously explained, the cited references do not disclose the recited external emitter that forms a backside junction in a front contact solar cell. Meier (US 6,262,359) does not disclose an externally formed emitter on the backside because Meier discloses forming a backside junction by diffusion from the backside electrode. Accordingly, any intervening material, such as tunnel oxide/polysilicon would prevent the diffusion, rendering Meier's process unworkable. Okayasu (JP07-106611) discloses an external emitter for a high-low junction, i.e., an emitter with the same polarity as the substrate, which is the opposite of a backside junction for a front contact cell. Like Okayasu, Gan (*Polysilicon Emitters for Silicon Concentrator Solar Cells*) does not disclose an external emitter for a backside junction of a front contact cell. Gan discloses poly emitters without further guidance on application to specific structures. For example, Gan's poly emitter could very well be for a high-low junction as in Okayasu. It is respectfully submitted that without using the present application as a blueprint, there is no guidance in the prior art to form a front contact solar cell with a formed backside junction emitter.

In the interest of compact prosecution, claims 1 and 9 have been amended to recite an oxide layer on the front surface of the substrate and an anti-reflective coating on the oxide layer. Support for this feature may be found at least on FIG. 1 of the specification, showing an oxide 124 and an anti-reflective coating 103 on the front side of the solar cell (specification, page 4, lines 14-18).

It is respectfully submitted that the above-noted feature of claims 1 and 9 are not taught or suggested by the references of record. More particularly, Meier (US 6,262,359), Okayasu (JP07-106611), Borden (WO 2009/094578), Foglietti (US 2002/0142500), Gan (*Polysilicon Emitters for Silicon Concentrator Solar Cells*), and Wenham (US 6,429,037) individually or in combination do not disclose a front contact solar cell with the recited external backside junction on the backside and the recited oxide/anti-reflective coating structure on the front side.

The dependent claims are patentable at least for depending from patentable base claims.

Conclusion

For at least the above reasons, it is believed that the pending claims are in condition for allowance. The Examiner is invited to telephone the undersigned for any questions and to resolve any remaining concerns regarding allowability of the present application.

Respectfully submitted,

Dated: Sept. 21, 2017

Patrick Benedicto

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/504,771	COUSINS, Peter John
	Examiner	Art Unit
	DEVINA PILLAY	1757

CPC - Searched*		
Symbol	Date	Examiner
H01L31/0236 H01L31/0745 H01L31/1804	6/8/2016	DP
H01L31/022425 H01L31/068 H01L31/182 H01L31/056	6/8/2016	DP
Y02E10/52 Y02P70/521 Y02E10/547	6/8/2016	DP

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor name search in PALM	6/8/2016	DP
EAST Text Search (See Search History)	6/8/2016	DP
Updated Inventor name search in PALM	10/5/2016	DP
Updated Inventor name search in PALM	2/1/2017	DP
Updated EAST Text Search (See Search History)	6/26/2017	DP
Updated Inventor name search in PALM	09/28/2017	DP

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/504,771	COUSINS, Peter John
	Examiner	Art Unit
	DEVINA PILLAY	1757



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/504,771	10/02/2014	Peter John COUSINS	10031.004211	3342

74254 7590 10/02/2017

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EXAMINER	
PILLAY, DEVINA	

ART UNIT	PAPER NUMBER
1757	

MAIL DATE	DELIVERY MODE
10/02/2017	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/504,771	Applicant(s) COUSINS, Peter John	
	Examiner DEVINA PILLAY	Art Unit 1757	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 09/21/2017 .

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____ .

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☑ Claim(s) 1-4, 7, 9-12, 14 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☑ Claim(s) 1-4, 7, 9-12, 14 is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____ .

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____ .

4) ☐ Other: _____ .

DETAILED CORRESPONDENCE

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 103

2. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-4, 7, 9-12 and 14 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Meier (US 6,262,359) in view of Okayasu (JP07-106611, Human Translation) in view of Borden (WO 2009/094578 A2) and in further view of Wenham (6,429,037 B1).

Regarding claims 1-4 and 9-12, Meier discloses a solar cell comprising (see Fig. 3D, C5/L38-C6/L55):

a substrate (218 n-type) having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

an emitter (220 p-type) forming a backside junction with the substrate;

a front surface field (216), high doped concentration area (n+), on the front surface of the substrate;

an anti-reflection (214) coating on the top most surface of the solar cell;

a front electrode disposed over the front surface of the substrate (212);

a back electrode disposed over the back surface of the substrate (222).

However, Meier does not disclose that the emitter is a polysilicon emitter or that the front surface field is formed of polysilicon and that there is a tunnel dielectric formed between the emitter and the back surface of the substrate or that there is a tunnel dielectric formed between the front surface field and the substrate.

Okayasu discloses that instead of forming an emitter ***or*** surface field from a portion of a substrate which is doped, an emitter or surface field can be formed using a doped polysilicon layer ([0005] [0009], Abstract) and by forming an emitter or surface field this way the thickness can be more accurately controlled and it prevents generation of floating foreign matter ([0008] [0009]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the method of forming the emitter/front surface field from a portion of a substrate of Meier and instead forming the emitter and front surface field by using a

doped polysilicon layer as disclosed by Okayasu because the thickness can be more accurately controlled and it prevent generation of floating foreign matter.

However, modified Meier does not discloses a tunneling dielectric oxide between the emitter/front surface field and the substrate.

Borden discloses that tunnel oxides can be used in solar cells between doped polysilicon and monocrystalline substrates [0016] and can be formed on both the front and back surfaces of a monocrystalline substrate.

Furthermore, Borden discloses that by providing the tunneling layer it prevents epitaxial growth of the emitter layer and further it protects the surface from plasma damage of the deposited emitter layer [0015].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the interface between polycrystalline layers and monocrystalline substrate back and front surfaces of modified Meier by having a tunneling oxide at the interfaces because it prevents epitaxial growth of the emitter layer and further it protects the crystalline surface from plasma damage of the deposited emitter layer.

Modified Meier discloses a first tunnel dielectric between the emitter and back surface and a second tunnel dielectric at the front surface of the substrate.

However, modified Meier does not disclose that doped region in the substrate.

Wenham discloses a solar cell wherein the area beneath point contacts includes areas of high doping which is important for reducing contact resistance (see Fig. 5, portions 18 and 23) (C1/L25-41).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the front surface field formed in the substrate of modified Meier by

adding in highly doped regions under the metallic contacts as disclosed by Wenham because doing so reduces the contact resistance and will improve the efficiency of the solar cell.

Regarding claims 7 and 14, modified Meier discloses all of the claim limitations as set forth above.

However, Meier does not disclose that the electrode that is in contact with the p-type polysilicon layer is silver.

Okayasu discloses that the back electrode on the polysilicon emitter is formed of a silver electrode [0044].

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the aluminum electrode of Meier with the silver electrode of Okayasu because one of ordinary skill in the art would have been able to carry out such a substitution, and the results would be reasonably predictable.

5. Claims 1-4, 7, 9-12 and 14 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Meier (US 6,262,359) in view of Okayasu (JP07-106611, Machine Translation) in view of Foglietti (US 2002/0142500 A1) in view of Gan (Polysilicon Emitters for Silicon Concentrator Solar Cells) and in further view of Wenham (6,429,037 B1).

Regarding claims 1-4 and 9-12, Meier discloses a solar cell comprising (see Fig. 3D, C5/L38-C6/L55):

a substrate (218 n-type) having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

an emitter (220 p-type) forming a backside junction with the substrate;

a front surface field (216), high doped concentration area (n+), on the front surface of the substrate;

an anti-reflection (214) coating on the top most surface of the solar cell;

a front electrode disposed over the front surface of the substrate (212);

a back electrode disposed over the back surface of the substrate (222).

However, Meier does not disclose that the emitter is a polysilicon emitter or that the front surface field is formed of polysilicon and that there is a tunnel dielectric formed between the emitter and the back surface of the substrate or that there is a tunnel dielectric formed between the front surface field and the substrate.

Okayasu discloses that instead of forming an emitter ***or*** surface field from a portion of a substrate which is doped, an emitter or surface field can be formed using a doped polysilicon layer ([0005][0009], Abstract) and by forming an emitter or surface field this way the thickness can be more accurately controlled and it prevents generation of floating foreign matter ([0008] [0009]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the method of forming the emitter/front surface field from a portion of a substrate of Meier and instead forming the emitter and front surface field by using a doped polysilicon layer as disclosed by Okayasu because the thickness can be more accurately controlled and it prevent generation of floating foreign matter.

However, modified Meier does not discloses a tunneling dielectric oxide at the interfaces between the emitter and the substrate and the front surface field and the substrate.

Foglietti discloses that polycrystalline growth directly on crystalline silicon results in partial realignment of the polycrystalline grains and to suppress this effect a thin oxide can be grown ([0046]).

Gan discloses that the presence of a stable thermal oxide between a polysilicon emitter and a CZ wafer (See pg. 248, first column, and Table 1) results in recombination occurring primary at the oxide interface and that the presence of this oxide at the interface can be useful for silicon solar cells with polysilicon emitters (See Conclusion, pg. 249).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the interface between the doped polysilicon regions and the monocrystalline substrate by adding an interfacial oxide as disclosed by Fogiletti and Gan because it will allow for optimal grown of the polysilicon region and furthermore will result in recombination primarily occurring at the oxide interface.

Modified Meier discloses a first tunnel dielectric between the emitter and back surface and a second tunnel dielectric at the front surface of the substrate.

However, modified Meier does not disclose that doped region in the substrate.

Wenham discloses a solar cell wherein the area beneath point contacts includes areas of high doping which is important for reducing contact resistance (see Fig. 5, portions 18 and 23) (C1/L25-41).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the front surface field formed in the substrate of modified Meier by adding in highly doped regions under the metallic contacts as disclosed by Wenham

because doing so reduces the contact resistance and will improve the efficiency of the solar cell.

Regarding claims 7 and 14, modified Meier discloses all of the claim limitations as set forth above.

However, Meier does not disclose that the electrode that is in contact with the p-type polysilicon layer is silver.

Okayasu discloses that the back electrode on the polysilicon emitter is formed of a silver electrode [0044].

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the aluminum electrode of Meier with the silver electrode of Okayasu because one of ordinary skill in the art would have been able to carry out such a substitution, and the results would be reasonably predictable.

Response to Arguments

6. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

7. Applicant argues that Okayasu cannot cure the deficiencies of Meier because the backside junction of Meier is formed integrally with the substrate and therefore there

can be no interfacial oxide. An interfacial oxide coupled with a polysilicon emitter and surface field would render the device of Meier unworkable. Applicant further argues that since Okayasu is concerned with a front side emitter and therefore Okayasu is not possible because it would require a total redesign of Meier.

8. Examiner respectfully disagrees. Meier discloses method of forming a junction which consists of an emitter formed on a substrate which comprises using the electrode as a dopant material and driving in those dopants through annealing and also forming a front surface field through driving of dopants into substrate. Okayasu discloses an alternative method of forming an emitter and surface field which comprises depositing a doped polysilicon doped layers over back and front surfaces of a single crystalline substrate. Okayasu also discloses that this method is preferable to that of heating and driving in dopants because it can be performed at lower temperatures which prevents damage to the substrate and furthermore the thickness of the emitter can be more accurately controlled ([0008]). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the emitter of Meier with the emitter of Okayasu because of the above advantages.

9. Applicant further argues that neither Foglietti nor Borden nor Gan disclose that a thin oxide can be used in a backside junction solar cell.

10. As disclosed above Gan, Foglietti and Borden disclose that a thin oxide can be provide advantageous properties between a doped polysilicon emitter and a monocrystalline substrate.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEVINA PILLAY whose telephone number is (571)270-1180. The examiner can normally be reached on Monday-Friday 9:30-6:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey T Barton can be reached on 517-272-1307. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DEVINA PILLAY/
Primary Examiner, Art Unit 1757

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14/504,771	COUSINS, Peter John
	Examiner	Art Unit
	DEVINA PILLAY	1757

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/16/2016	2016-06-08	2016-10-05	2017-01-31	2017-06-26	09/28/2017			
	1	÷	✓	✓	✓	✓	✓			
	2	÷	✓	✓	✓	✓	✓			
	3	÷	✓	✓	✓	✓	✓			
	4	÷	✓	✓	✓	✓	✓			
	5	÷	✓	-	-	-	-			
	6	÷	✓	✓	✓	-	-			
	7	÷	✓	✓	✓	✓	✓			
	8	÷	✓	✓	✓	✓	-			
	9	÷	✓	✓	✓	✓	✓			
	10	÷	✓	✓	✓	✓	✓			
	11	÷	✓	✓	✓	✓	✓			
	12	÷	✓	✓	✓	✓	✓			
	13	÷	✓	✓	✓	-	-			
	14	÷	✓	✓	✓	✓	✓			
	15	÷	N	-	-	-	-			
	16	÷	N	-	-	-	-			
	17	÷	N	-	-	-	-			
	18	÷	N	-	-	-	-			
	19	÷	N	-	-	-	-			
	20	÷	N	-	-	-	-			
	21					✓	-			
	22					✓	-			

Docket No. 10031.004211
Appeal Brief

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:

Peter John COUSINS

Application No.: 14/504,771 Examiner: PILLAY, DEVINA

Filing Date: October 2, 2014 Art Unit: 1757

Assignee: SunPower Corporation

Title: FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

APPEAL BRIEF FILED UNDER 37 C.F.R. § 41.37

This Appeal Brief is submitted with a Notice of Appeal.

I. REAL PARTY IN INTEREST

The real party in interest is the SunPower Corporation, which is the assignee of the present application.

II. RELATED APPEALS AND INTERFERENCES

On information and belief, there are no appeals, interferences, or judicial proceedings known to the appellant, the appellant's legal representative, or assignee which may be related to, directly affect or be directly affected by or have a bearing on the Patent Trial and Appeal Board decision in the pending appeal.

III. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 recites a solar cell that includes: (a) a substrate having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface (specification, page 4, lines 3-14; FIG. 1, 101); (b) an oxide layer disposed on the front surface of the substrate (specification, page 5, lines 1-3; FIG. 1, 124); (c) an anti-reflective coating on the oxide layer (specification, page 4, lines 22 and 23; FIG. 1, 103); (d) a tunnel dielectric disposed over the back surface of the substrate (specification, page 5, lines 4 and 5; FIG. 1, 107); (e) an emitter disposed over the tunnel dielectric, the emitter forming a backside junction with the substrate (specification, page 4, lines 7-9; page 5, lines 4-8; FIG. 1, 108); (f) a doped diffusion region in the substrate (specification, page 4, lines 12-21; FIG. 1, 106); (g) a front electrode that is coupled to the doped diffusion region on the front surface of the substrate (specification, page 5, lines 19-22; FIG. 1, 102); and (h) a back electrode that is coupled to the emitter on the back surface of the substrate (specification, page 5, lines 10-14; FIG. 1, 110).

Claim 9 recites a solar cell that includes: (a) a substrate having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface (specification, page 4, lines 3-14; FIG. 1, 101); (b) a doped diffusion region in the substrate on the front surface of the substrate (specification, page 4, lines 12-21; FIG. 1, 106); (c) an emitter over the back surface of the substrate, the emitter forming a backside junction with the substrate (specification, page 4, lines 7-9; page 5, lines 4-8; FIG. 1, 108); (d) a first dielectric between the emitter and the back surface (specification, page 5, lines 4 and 5; FIG. 1, 107); (e) a front electrode disposed on the front surface of the substrate and is coupled to the doped diffusion region (specification, page 5, lines 19-22; FIG. 1, 102); (f) a second dielectric on the front surface of the substrate (specification, page 5, lines 1-3; FIG. 1, 124); (g) an anti-reflective coating on the second dielectric (specification, page 4, lines 22 and 23; FIG. 1, 103); and (h) a back electrode disposed on the back surface of the substrate (specification, page 5, lines 10-14; FIG. 1, 110).

IV. ARGUMENT

The appellant traverses the rejections in the Final Office Action mailed on October 2, 2017 ("final office action") for the following reasons.

A. CLAIMS 1-4 and 7

Claims 1-4, 7, 9-12, and 14 are rejected under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Meier (US 6,262,359), in view of Okayasu (JP 07-106611), in view of Borden (US WO 2009/094578 A2) and further in view of Wenham (US 6,429,037). The rejection is respectfully traversed.

1. Backside junction emitter with tunnel dielectric

Claim 1 is patentable over the combination of Meier, Okayasu, Borden and Wenham at least for reciting: "a tunnel dielectric disposed over the back surface of the substrate; an emitter disposed over the tunnel dielectric, the emitter forming a backside junction with the substrate."

Claim 1 recites a structure of a solar cell. In the embodiment of claim 1, the solar cell has an emitter that is disposed over a tunnel dielectric and forms a backside junction with the substrate. It is respectfully submitted that this feature of claim 1 is not taught or suggested by the combination of Meier, Okayasu, Borden, and Wenham.

The final office action suggests that in the cited combination, Meier discloses the recited backside junction. Meier FIG. 3D is reproduced below for ease of discussion.

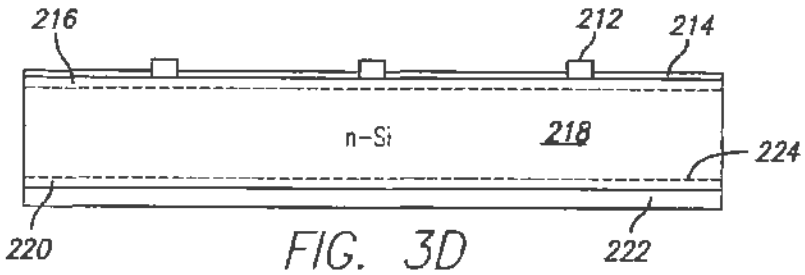


FIG. 3D

Meier discloses a solar cell with an aluminum alloy back junction (Meier, Title). More specifically, Meier discloses forming a p+ layer 220 that forms a backside junction with the n-Si base layer 218, within the base layer 218, by doping using the aluminum contact layer 222 (Meier, col. 6, lines 51-54). That is, the primary teaching of Meier is to form an aluminum alloy back junction by forming the p+ layer 220 by diffusion into the

substrate using the aluminum alloy electrode, thereby providing a strongly doped p-type emitter (Meier, abstract).

More particularly, the final office action suggests that the emitter 220 corresponds to the recited emitter that forms a backside junction with the substrate. It is respectfully submitted that in the embodiment of claim 1, the emitter is disposed over the tunnel dielectric, which is disposed over the substrate. That is, in the embodiment of claim 1, there is an intervening tunnel dielectric between the emitter and the substrate. It is respectfully submitted that this emitter structure with tunnel dielectric is not possible in Meier because of the required diffusion from the contact layer 222 to form the emitter 220 within the substrate 218. ***A tunnel dielectric would block diffusion from the contact layer 222, which is contrary to the teaching of Meier.*** Accordingly, any modification to form a tunnel dielectric between the aluminum contact layer 222 and the substrate 218 will render Meier unsuitable for its intended purpose, and would involve a major redesign of Meier's process.

It is respectfully submitted that Okayasu does not cure the deficiencies of Meier.

Okayasu discloses a manufacturing method for a Back Surface Field (BSF) type solar cell (Okayasu, paragraph [0001]). The final office action suggests that it would have been obvious to use the BSF formation technique of Okayasu to form the backside junction emitter of Meier. The appellant respectfully disagrees.

Okayasu discloses a manufacturing method for a BSF type solar cell. As is well known, a BSF layer is a backside layer that has the same polarity as the substrate. That is, an n-type substrate would have an n-type BSF layer, and a p-type substrate would have a p-type BSF layer (Okayasu, paragraph [0008]). More particularly, a BSF layer cannot form a backside junction with the substrate because it has the same polarity as the substrate.

Therefore, it is respectfully submitted that the proposed modification would use the BSF manufacturing method of Okayasu (to form a BSF layer on the backside) for a totally different function and structure in Meier (to form a backside junction with the substrate).

Okayasu paragraph [0005], cited in the final office action, provides an overview of a thermal diffusion method, which involves diffusion from a dopant gas introduced in the chamber. Okayasu paragraph [0006] discloses that it is difficult to control the emitter thickness with the thermal diffusion method. ***It is to be noted that the gas diffusion method referred to in Okayasu is not the same as contact diffusion of Meier.*** Like Okayasu, Meier discloses that the conventional method of forming the layer makes it difficult to control the depth, i.e., thickness, of the emitter (Meier, col. 2, lines13-25).

Okayasu paragraph [0008], cited in the final office action, discloses that the thermal gas diffusion method to form the BSF layer can be replaced with plasma chemical vapor deposition (CVD). It is important to reiterate that the diffusion method referred to in Okayasu (gas diffusion) is not the same as the diffusion method of Meier (contact diffusion). More particularly, Okayasu is not advocating replacement of Meier's fabrication process. In fact, Meier is solving the same problem as Okayasu.

Okayasu paragraph [0009], cited in the final office action, discloses that although the plasma CVD method has its advantages, the plasma CVD method introduces particulates that deteriorate the BSF layer. It is respectfully submitted that given the problem of particulate contamination caused by plasma CVD, one of ordinary skill in the art would not be motivated to replace the contact diffusion method of Meier with the BSF manufacturing method of Okayasu.

Furthermore, it is respectfully submitted that the plasma CVD method of Meier would form the BSF layer on the ***silicon*** substrate (Okayasu, FIG. 1, BSF layer 5 to substrate 1). Meier does not teach or suggest that a film from its CVD method would adhere to a tunnel dielectric.

Borden, on paragraphs 15 and 16, discloses that a tunnel oxide may be employed between polysilicon and substrate. It is respectfully submitted that Borden does not disclose any particular structure or solar cell configuration where a polysilicon and tunnel oxide may be employed. For example, Borden does not disclose using polysilicon/tunnel oxide/substrate to form a backside junction. There is no disclosure in Borden to apply its teaching to arrive at a structure where an emitter separated from the substrate by a tunnel

oxide forms a backside junction with the substrate. Such teaching is only in the present disclosure, not in any of the references of record.

As explained above, it is respectfully submitted that Meier modified with Okayasu does not teach or suggest a tunnel dielectric between the backside junction emitter and the substrate. A tunnel dielectric, as disclosed by Borden, would block diffusion from the contact layer as taught by Meier. Like Meier, Okayasu does not disclose a tunnel dielectric between its BSF layer and the substrate. It is respectfully submitted that Okayasu has no disclosure regarding applicability of its BSF manufacturing method to form the BSF layer on a tunnel dielectric as taught by Borden.

It is respectfully submitted that Wenham does not add to the teachings of Meier, Okayasu, and Borden with regards to a backside junction emitter with tunnel dielectric.

2. Anti-reflective Coating On An Oxide Layer

Claim 1 is patentable over the combination of Meier, Okayasu, Borden, and Wenham at least for reciting: "an oxide layer disposed on the front surface of the substrate; an anti-reflective coating on the oxide layer."

In the embodiment of claim 1, an oxide layer is disposed on the front surface of the substrate, and an anti-reflective coating is on the oxide layer.

Meier discloses an anti-reflective coating 214 (Meier FIG. 3D). It is respectfully submitted that Meier does not disclose that the anti-reflective coating 214 is on an oxide layer. Instead, in Meier, the anti-reflective coating 214 is formed on the surface of the substrate.

Borden, paragraph 16, discloses that a tunnel oxide may be employed between polysilicon and substrate. It is respectfully submitted that Borden does not disclose an anti-reflective coating formed on an oxide layer on the front surface of the substrate. Borden discloses a polysilicon emitter, not an anti-reflective coating.

It is respectfully submitted that Okayasu and Wenham do not add to Meier and Borden with regards to an anti-reflective coating on an oxide layer.

Therefore, it is respectfully submitted that claim 1 is patentable over the combination of Meier, Okayasu, Borden, and Wenham.

Claims 2-4 are patentable over the combination of Meier, Okayasu, Borden, and Wenham at least for depending from claim 1.

Claim 9 is patentable over the combination of Meier, Okayasu, Borden, and Wenham at least for reciting: "an emitter over the back surface of the substrate, the emitter forming a backside junction with the substrate; a first dielectric between the emitter and the back surface."

As explained, it is respectfully submitted that the combination of Meier, Okayasu, Borden, and Wenham does not teach or suggest a backside junction emitter and a first dielectric between the backside junction emitter and the back surface of the substrate.

Claim 9 is further patentable over the combination of Meier, Okayasu, Borden, and Wenham at least for reciting: "a second dielectric on the front surface of the substrate; an anti-reflective coating on the second dielectric."

As explained, it is respectfully submitted that the combination of Meier, Okayasu, Borden, and Wenham does not teach or suggest an anti-reflective coating that is formed on a dielectric on the front surface of the substrate.

Claims 10-12 are patentable over the combination of Meier, Okayasu, Borden, and Wenham at least for depending from claim 9.

B. CLAIMS 1-4, 7, 9-12, and 14

Claims 1-4, 7, 9-12, and 14 are rejected under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Meier (US 6,262,359), in view of Okayasu (JP 07-106611), in view of Foglietti (US 2002/0142500), in view of Gan (*Polysilicon Emitters for Silicon Concentrator Solar Cells*), and further in view of Wenham (US 6,429,037). The rejection is respectfully traversed.

1. Backside junction emitter with tunnel dielectric

Claim 1 is patentable over the combination of Meier, Okayasu, Foglietti, Gan, and Wenham at least for reciting: "a tunnel dielectric disposed over the back surface of the substrate; an emitter disposed over the tunnel dielectric, the emitter forming a backside junction with the substrate."

Claim 1 recites a structure of a solar cell. In the embodiment of claim 1, the solar cell has an emitter that is disposed over a tunnel dielectric and forms a backside junction with the substrate. It is respectfully submitted that this feature of claim 1 is not taught or suggested by the combination of Meier, Okayasu, Foglietti, Gan, and Wenham.

The final office action suggests that in the cited combination, Meier discloses the recited backside junction. Meier FIG. 3D is reproduced below for ease of discussion.

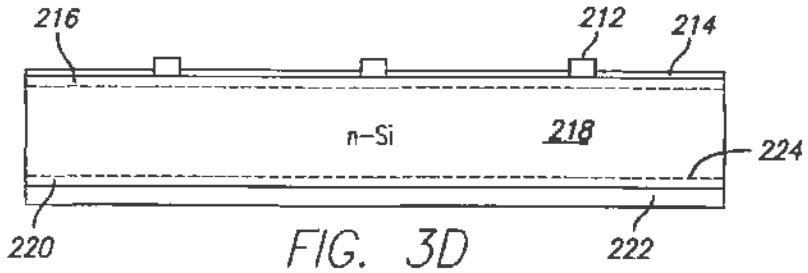


FIG. 3D

Meier discloses a solar cell with an aluminum alloy back junction (Meier, Title). More specifically, Meier discloses forming a p+ layer 220 that forms a backside junction with the n-Si base layer 218, within the base layer 218, by doping using the aluminum contact layer 222 (Meier, col. 6, lines 51-54). That is, the primary teaching of Meier is to form an aluminum alloy back junction by forming the p+ layer 220 by diffusion into the substrate using the aluminum alloy electrode, thereby providing a strongly doped p-type emitter (Meier, abstract).

More particularly, the final office action suggests that the emitter 220 corresponds to the recited emitter that forms a backside junction with the substrate. It is respectfully submitted that in the embodiment of claim 1, the emitter is disposed over the tunnel dielectric, which is disposed over the substrate. That is, in the embodiment of claim 1, there is an intervening tunnel dielectric between the emitter and the substrate. It is respectfully submitted that this emitter structure with tunnel dielectric is not possible in Meier because of the required diffusion from the contact layer 222 to form the emitter 220 within the substrate 218. A tunnel dielectric would block diffusion from the contact layer 222, which is contrary to the teaching of Meier. Accordingly, any modification to form a tunnel dielectric between the aluminum contact layer 222 and the substrate 218

will render Meier unsuitable for its intended purpose, and would involve a major redesign of Meier's process.

It is respectfully submitted that Okayasu does not cure the deficiencies of Meier.

Okayasu discloses a manufacturing method for a Back Surface Field (BSF) type solar cell (Okayasu, paragraph [0001]). The final office action suggests that it would have been obvious to use the BSF formation technique of Okayasu to form the backside junction emitter of Meier. The appellant respectfully disagrees.

Okayasu discloses a manufacturing method for a BSF type solar cell. As is well known, a BSF layer is a backside layer that has the same polarity as the substrate. That is, an n-type substrate would have an n-type BSF layer, and a p-type substrate would have a p-type BSF layer (Okayasu, paragraph [0008]). More particularly, a BSF layer cannot form a backside junction with the substrate because it has the same polarity as the substrate.

Therefore, it is respectfully submitted that the proposed modification would use the BSF manufacturing method of Okayasu (to form a BSF layer on the backside) for a totally different function and structure in Meier (to form a backside junction with the substrate).

Okayasu paragraph [0005], cited in the final office action, provides an overview of a thermal diffusion method, which involves diffusion from a dopant gas introduced in the chamber. Okayasu paragraph [0006] discloses that it is difficult to control the emitter thickness with the thermal diffusion method. It is to be noted that the gas diffusion method referred to in Okayasu is not the same as contact diffusion of Meier. Like Okayasu, Meier discloses that the conventional method of forming the layer makes it difficult to control the depth, i.e., thickness, of the emitter (Meier, col. 2, lines13-25)

Okayasu paragraph [0008], cited in the final office action, discloses that the thermal gas diffusion method to form the BSF layer can be replaced with plasma chemical vapor deposition (CVD). It is important to reiterate that the diffusion method referred to in Okayasu (gas diffusion) is not the same as the diffusion method of Meier

(contact diffusion). More particularly, Okayasu is not advocating replacement of Meier's fabrication process. In fact, Meier is solving the same problem as Okayasu.

Okayasu paragraph [0009], cited in the final office action, discloses that although the plasma CVD method has its advantages, the plasma CVD method introduces particulates that deteriorate the BSF layer. It is respectfully submitted that given the problem of particulate contamination caused by plasma CVD, one of ordinary skill in the art would not be motivated to replace the contact diffusion method of Meier with the BSF manufacturing method of Okayasu.

Furthermore, it is respectfully submitted that the plasma CVD method of Meier would form the BSF layer on the silicon substrate (Okayasu, FIG. 1, BSF layer 5 to substrate 1). Meier does not teach or suggest that a film from its CVD method would adhere to a tunnel dielectric.

The final office action suggests that Gan and Foglietti disclose using a thin oxide with polysilicon. It is respectfully submitted that Gan and Foglietti do not disclose structures where polysilicon emitters and tunnel oxides are employed in backside junctions. There is no disclosure in Gan and Foglietti to apply their teachings to arrive at a structure where a polysilicon emitter separated from the substrate by a dielectric forms a backside junction with the substrate. Such teaching is only in the present application, not in the references of record.

As explained above, it is respectfully submitted that Meier modified with Okayasu does not teach or suggest a tunnel dielectric between the backside junction emitter and the substrate. A dielectric, as disclosed by Gan and Foglietti, would block diffusion from the contact layer as taught by Meier. Like Meier, Okayasu does not disclose a tunnel dielectric between its BSF layer and the substrate. It is respectfully submitted that Okayasu has no disclosure regarding applicability of its BSF manufacturing method to form the BSF layer on a dielectric as taught by Gan and Foglietti.

It is respectfully submitted that Wenham does not add to the teachings of Meier, Okayasu, Gan, and Foglietti with regards to a backside junction emitter formed on a dielectric.

2. Anti-reflective Coating On An Oxide Layer

Claim 1 is patentable over the combination of Meier, Okayasu, Gan, Foglietti, and Wenham at least for reciting: "an oxide layer disposed on the front surface of the substrate; an anti-reflective coating on the oxide layer."

In the embodiment of claim 1, an oxide layer is disposed on the front surface of the substrate, and an anti-reflective coating is on the oxide layer.

Meier discloses an anti-reflective coating 214 (Meier FIG. 3D). It is respectfully submitted that Meier does not disclose that the anti-reflective coating 214 is on an oxide layer. Instead, in Meier, the anti-reflective coating 214 is formed on the surface of the substrate.

Gan and Foglietti disclose that a tunnel oxide may be employed between polysilicon and substrate. It is respectfully submitted that Gan and Foglietti do not disclose an anti-reflective coating formed on an oxide layer on the front surface of the substrate.

It is respectfully submitted that Okayasu and Wenham do not add to Meier, Gan, and Foglietti with regards to an anti-reflective coating on an oxide layer.

Therefore, it is respectfully submitted that claim 1 is patentable over the combination of Meier, Okayasu, Gan, Foglietti and Wenham.

Claims 2-4 and 7 are patentable over the combination of Meier, Okayasu, Gan, Foglietti, and Wenham at least for depending from claim 1.

Claim 9 is patentable over the combination of Meier, Okayasu, Gan, Foglietti and Wenham at least for reciting: "an emitter over the back surface of the substrate, the emitter forming a backside junction with the substrate; a first dielectric between the emitter and the back surface."

As explained, it is respectfully submitted that the combination of Meier, Okayasu, Gan, Foglietti and Wenham does not teach or suggest a backside junction emitter and a first dielectric between the backside junction emitter and the back surface of the substrate.

Claim 9 is further patentable over the combination of Meier, Okayasu, Gan, Foglietti and Wenham at least for reciting: "a second dielectric on the front surface of the substrate; an anti-reflective coating on the second dielectric."

As explained, it is respectfully submitted that the combination of Meier, Okayasu, Gan, Foglietti and Wenham does not teach or suggest an anti-reflective coating that is formed on a dielectric on the front surface of the substrate.

Claims 10-12 and 14 are patentable over the combination of Meier, Okayasu, Gan, Foglietti and Wenham at least for depending from claim 9.

V. CONCLUSION

For at least the above reasons, allowance of the pending claims is respectfully requested.

Respectfully submitted,

Dated: November 8, 2017

/Patrick D. Benedicto/

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CLAIMS APPENDIX

CLAIMS INVOLVED IN THE APPEAL

1. A solar cell, comprising:

a substrate having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

an oxide layer disposed on the front surface of the substrate;

an anti-reflective coating on the oxide layer;

a tunnel dielectric disposed over the back surface of the substrate;

an emitter disposed over the tunnel dielectric, the emitter forming a backside junction with the substrate;

a doped diffusion region in the substrate;

a front electrode that is coupled to the doped diffusion region on the front surface of the substrate; and

a back electrode that is coupled to the emitter on the back surface of the substrate.

2. The solar cell of claim 1, wherein the emitter is a polysilicon emitter.

3. The solar cell of claim 1, wherein the substrate is a monocrystalline silicon substrate.

4. The solar cell of claim 1, wherein the tunnel dielectric is a tunnel oxide.

7. The solar cell of claim 1, wherein the back electrode includes silver.

9. A solar cell, comprising:

a substrate having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

a doped diffusion region in the substrate on the front surface of the substrate;

an emitter over the back surface of the substrate, the emitter forming a backside junction with the substrate;

a first dielectric between the emitter and the back surface;

a front electrode disposed on the front surface of the substrate and is coupled to the doped diffusion region;

a second dielectric on the front surface of the substrate;

an anti-reflective coating on the second dielectric; and

a back electrode disposed on the back surface of the substrate.

10. The solar cell of claim 9, wherein the emitter is a polysilicon emitter.

11. The solar cell of claim 9, wherein the substrate is a monocrystalline silicon substrate.

12. The solar cell of claim 9, wherein the first dielectric is an oxide.

14 The solar cell of claim 9, wherein the back electrode includes silver.

PTO/AIA/31 (03-14)
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NOTICE OF APPEAL FROM THE EXAMINER TO THE PATENT TRIAL AND APPEAL BOARD

Docket Number (Optional): 10031.0004211

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Signature /Patrick D. Benedicto/

Typed or printed name PATRICK D. BENEDICTO

In re Application of: Peter John COUSINS

Application Number	Filed
14/504,771	10/02/2014

For: FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

Art Unit	Examiner
1757	PILLAY, DEVINA

Applicant hereby **appeals** to the Patent Trial and Appeal Board from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) $ 800.00

☐ Applicant asserts small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by 50%, and the resulting fee is: $ _____

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Therefore, the fee shown above is reduced by 75%, and the resulting fee is: $ _____
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 50-2427.

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☐ A petition for an extension of time under 37 CFR 1.136(a) (PTO/AIA/22 or equivalent) is enclosed.
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☑ attorney or agent of record. Registration number 40,909

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____

Signature /Patrick D. Benedicto/

Typed or printed name PATRICK D. BENEDICTO

Telephone Number 408.436.2110

Date November 8, 2017

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 41.20(b)(1) and 41.31. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO.
14/504,771	10/02/2014	Peter John COUSINS	10031.0042US1	3342

74254 7590 03/19/2018

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EXAMINER	
PILLAY, DEVINA	

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Application Number: 14/504,771
Filing Date: 2 Oct 2014
Appellant(s): COUSINS, Peter, John

Patrick D. Benedicto
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/08/2017.

(1) Grounds of Rejection to be Reviewed on Appeal

Every ground of rejection set forth in the Office action dated 10/02/2017 from which the appeal is taken is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

The following ground(s) of rejection are applicable to the appealed claims.

Claim Rejections - 35 USC § 103

Claims 1-4, 7, 9-12 and 14 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Meier (US 6,262,359) in view of Okayasu (JP07-106611, Human Translation) in view of Borden (WO 2009/094578 A2) and in further view of Wenham (6,429,037 B1).

Regarding claims 1-4 and 9-12, Meier discloses a solar cell comprising (see Fig. 3D, C5/L38-C6/L55):

a substrate (218 n-type) having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

an emitter (220 p-type) forming a backside junction with the substrate;

a front surface field (216), high doped concentration area (n+), on the front surface of the substrate;

an anti-reflection (214) coating on the top most surface of the solar cell;

a front electrode disposed over the front surface of the substrate (212);

a back electrode disposed over the back surface of the substrate (222).

However, Meier does not disclose that the emitter is a polysilicon emitter or that the front surface field is formed of polysilicon and that there is a tunnel dielectric formed between the emitter and the back surface of the substrate or that there is a tunnel dielectric formed between the front surface field and the substrate.

Okayasu discloses that instead of forming an emitter ***or*** surface field from a portion of a substrate which is doped, an emitter or surface field can be formed using a doped polysilicon layer ([0005] [0009], Abstract) and by forming an emitter or surface field this way the thickness can be more accurately controlled and it prevents generation of floating foreign matter ([0008] [0009]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the method of forming the emitter/front surface field from a portion of a substrate of Meier and instead forming the emitter and front surface field by using a doped polysilicon layer as disclosed by Okayasu because the thickness can be more accurately controlled and it prevent generation of floating foreign matter.

However, modified Meier does not discloses a tunneling dielectric oxide between the emitter/front surface field and the substrate.

Borden discloses that tunnel oxides can be used in solar cells between doped polysilicon and monocrystalline substrates [0016] and can be formed on both the front and back surfaces of a monocrystalline substrate.

Furthermore, Borden discloses that by providing the tunneling layer it prevents epitaxial growth of the emitter layer and further it protects the surface from plasma damage of the deposited emitter layer [0015].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the interface between polycrystalline layers and monocrystalline substrate back and front surfaces of modified Meier by having a tunneling oxide at the interfaces because it prevents epitaxial growth of the emitter layer and further it protects the crystalline surface from plasma damage of the deposited emitter layer.

Modified Meier discloses a first tunnel dielectric between the emitter and back surface and a second tunnel dielectric at the front surface of the substrate.

However, modified Meier does not disclose that doped region in the substrate.

Wenham discloses a solar cell wherein the area beneath point contacts includes areas of high doping which is important for reducing contact resistance (see Fig. 5, portions 18 and 23) (C1/L25-41).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the front surface field formed in the substrate of modified Meier by adding in highly doped regions under the metallic contacts as disclosed by Wenham because doing so reduces the contact resistance and will improve the efficiency of the solar cell.

Regarding claims 7 and 14, modified Meier discloses all of the claim limitations as set forth above.

However, Meier does not disclose that the electrode that is in contact with the p-type polysilicon layer is silver.

Okayasu discloses that the back electrode on the polysilicon emitter is formed of a silver electrode [0044].

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the aluminum electrode of Meier with the silver electrode of Okayasu because one of ordinary skill in the art would have been able to carry out such a substitution, and the results would be reasonably predictable.

Claims 1-4, 7, 9-12 and 14 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Meier (US 6,262,359) in view of Okayasu (JP07-106611, Machine Translation) in view of Foglietti (US 2002/0142500 A1) in view of Gan (Polysilicon Emitters for Silicon Concentrator Solar Cells) and in further view of Wenham (6,429,037 B1).

Regarding claims 1-4 and 9-12, Meier discloses a solar cell comprising (see Fig. 3D, C5/L38-C6/L55):

a substrate (218 n-type) having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

an emitter (220 p-type) forming a backside junction with the substrate;

a front surface field (216), high doped concentration area (n+), on the front surface of the substrate;

an anti-reflection (214) coating on the top most surface of the solar cell;

a front electrode disposed over the front surface of the substrate (212);

a back electrode disposed over the back surface of the substrate (222).

However, Meier does not disclose that the emitter is a polysilicon emitter or that the front surface field is formed of polysilicon and that there is a tunnel dielectric formed between the emitter and the back surface of the substrate or that there is a tunnel dielectric formed between the front surface field and the substrate.

Okayasu discloses that instead of forming an emitter ***or*** surface field from a portion of a substrate which is doped, an emitter or surface field can be formed using a doped polysilicon layer ([0005][0009], Abstract) and by forming an emitter or surface field this way the thickness can be more accurately controlled and it prevents generation of floating foreign matter ([0008] [0009]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the method of forming the emitter/front surface field from a portion of a substrate of Meier and instead forming the emitter and front surface field by using a doped polysilicon layer as disclosed by Okayasu because the thickness can be more accurately controlled and it prevent generation of floating foreign matter.

However, modified Meier does not discloses a tunneling dielectric oxide at the interfaces between the emitter and the substrate and the front surface field and the substrate.

Foglietti discloses that polycrystalline growth directly on crystalline silicon results in partial realignment of the polycrystalline grains and to suppress this effect a thin oxide can be grown ([0046]).

Gan discloses that the presence of a stable thermal oxide between a polysilicon emitter and a CZ wafer (See pg. 248, first column, and Table 1) results in recombination occurring primary at the oxide interface and that the presence of this oxide at the interface can be useful for silicon solar cells with polysilicon emitters (See Conclusion, pg. 249).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the interface between the doped polysilicon regions and the

monocrystalline substrate by adding an interfacial oxide as disclosed by Fogiletti and Gan because it will allow for optimal grown of the polysilicon region and furthermore will result in recombination primarily occurring at the oxide interface.

Modified Meier discloses a first tunnel dielectric between the emitter and back surface and a second tunnel dielectric at the front surface of the substrate.

However, modified Meier does not disclose that doped region in the substrate.

Wenham discloses a solar cell wherein the area beneath point contacts includes areas of high doping which is important for reducing contact resistance (see Fig. 5, portions 18 and 23) (C1/L25-41).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the front surface field formed in the substrate of modified Meier by adding in highly doped regions under the metallic contacts as disclosed by Wenham because doing so reduces the contact resistance and will improve the efficiency of the solar cell.

Regarding claims 7 and 14, modified Meier discloses all of the claim limitations as set forth above.

However, Meier does not disclose that the electrode that is in contact with the p-type polysilicon layer is silver.

Okayasu discloses that the back electrode on the polysilicon emitter is formed of a silver electrode [0044].

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the aluminum electrode of Meier with the silver electrode of

Okayasu because one of ordinary skill in the art would have been able to carry out such a substitution, and the results would be reasonably predictable.

(2) Response to Argument

A. Arguments with respect to claims 1-4, 7, 9-12, and 14 under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Meier (US 6,262,359), in view of Okayasu (JP 07-106611), in view of Borden (US WO 2009/094578 A2) and further in view of Wenham (US 6,429,037).

1. Backside junction emitter with tunnel dielectric

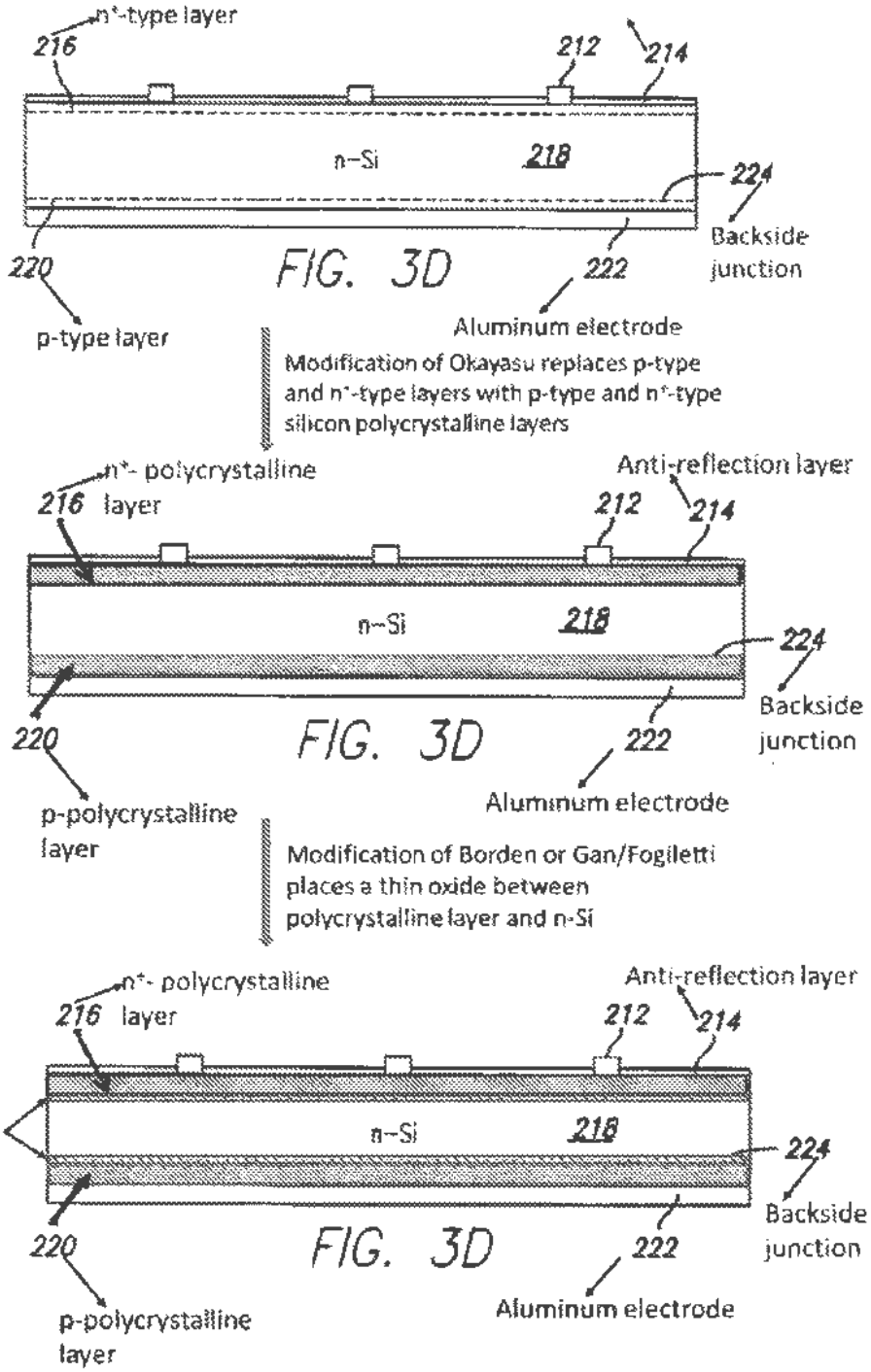
Appellant argues with respect to claim 1 that while Meier discloses a backside junction formed between the emitter (220) and base (228) Meier does not disclose the tunnel oxide between the base and emitter. Furthermore, if there were a tunnel oxide present in Meier the formation of the emitter would not be possible since it is formed from diffusion with the contact layer (222).

Appellant further argues that Okayasu discloses a BSF solar cell and that a BSF layer cannot form a backside junction with the substrate and therefore the combination of Meier and Okayasu is not possible.

Appellant further argues that Okayasu discloses that thermal diffusion method which involves diffusion of dopant gas and that it is not the same as contact diffusion and while Okayasu discloses that thermal gas diffusion can be replaced with plasma CVD to form the BSF one would not have done the replacement for contact diffusion. Furthermore, Appellant argues that plasma CVD also has disadvantages which include particulate contamination so one of ordinary skill would have not been motivated to use the plasma CVD of Okayasu.

Appellant further argues that Borden does not disclose any particular structure of a polysilicon/tunnel oxide/substrate which forms a backside junction.

Examiner respectfully disagrees and points to Figure below for discussion of modifications made to Meier.



Meier discloses method of forming a junction which consists of a p-type emitter (220) formed on an n-type substrate (218) which comprises using the aluminum electrode (222) as a p-type dopant material and driving in those dopants through annealing (C6/L35-50). Meier discloses the presence of the junction (224) on the backside of the solar cell.

In addition, Meier discloses the presence of a front surface field (216-n+-type layer) which comprises the same type of dopant as the n-type substrate and that the front surface field is formed through thermal diffusion (C5/L43-49)

Okayasu discloses an alternative method of forming a doped emitter or a surface field on a doped substrate. Okayasu discloses depositing a doped polysilicon emitter and a doped surface field on a doped single crystalline substrate ([0014] [0043]).

Okayasu also discloses that the method of depositing doped polysilicon layers is preferable to that of thermal diffusion which involves heating and driving in dopants because it can be performed at lower temperatures which prevents damage to the substrate and furthermore the thickness of the emitter can be more accurately controlled ([0008]).

Okayasu discloses that in thermal diffusion the dopant source can be provided in one of two ways (see [0005] of Okayasu) either dopant gas (as in the case of the front surface field formed by Meier, see Meier C5/L43-49) or a p-type Al layer (as in the emitter formed by Meier, see Meier C6/L35-50) is laminated on the single crystal substrate (see [0005] of Okayasu). Okayasu further discloses that after the dopant is provided the substrate is heated to 1000°C ([0005]) and it is difficult to control the

thickness of the doped layers provided this way and degradation of the substrate is known to occur at high temperatures ([0006]-[0008]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the emitter and surface field of Meier with the p-type polysilicon layer and n-type polysilicon of Okayasu, respectively, because of the above advantages.

Examiner notes that Borden was used to provide motivation for providing a tunnel oxide between the polysilicon emitter/surface field and the monocrystalline substrate not to teach the presence of a backside junction.

Borden discloses that tunnel oxides can be used in solar cells between doped polysilicon and monocrystalline substrates [0016]. Furthermore, Borden discloses that by providing the tunneling layer it prevents epitaxial growth of the emitter layer and further it protects the surface from plasma damage of the deposited emitter layer [0008].

Thus it would have been obvious to modify the interfaces between polysilicon layers of the emitter and front surface field and monocrystalline substrates of modified Meier by having a tunneling oxide because it prevents epitaxial growth of the emitter layer and further it protects the crystalline surface from plasma damage of the deposited emitter layer.

2. Anti-reflective Coating On An Oxide Layer

Appellant further argues that anti-reflective layer of Meier (see Fig. 3D, 214) does not disclose that the anti-reflective layer is formed on an oxide layer and is instead formed on the surface of substrate.

Appellant further argues that Borden does not alleviate this deficiency since Borden discloses that there is a polysilicon on an oxide coating on the front surface not an anti-reflective coating on an oxide coating.

Examiner finds that modified Meier discloses between the polysilicon front surface field and the base substrate there is an oxide layer on the front surface of the substrate (see Figure above, tunnel oxide on front and back surfaces). Therefore the anti-reflection layer (214) of Meier is on the tunnel oxide layer which is provided on the front surface of the substrate on the polysilicon layer (see Figure provided above).

B. Arguments with respect to claims 1-4, 7, 9-12, and 14 under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Meier (US 6,262,359) in view of Okayasu (JP07-106611, Machine Translation) in view of Foglietti (US 2002/0142500 A1) in view of Gan (Polysilicon Emitters for Silicon Concentrator Solar Cells) and in further view of Wenham (6,429,037 B1).

1. Backside junction emitter with tunnel dielectric

Appellant argues with respect to claim 1 that while Meier discloses a backside junction formed between the emitter (220) and base (228) Meier does not disclose the tunnel oxide between the base and emitter. Furthermore, if there were a tunnel oxide present in Meier the formation of the emitter would not be possible since it is formed from diffusion with the contact layer (222).

Appellant further argues that Okayasu discloses a BSF solar cell and that a BSF layer cannot form a backside junction with the substrate and therefore the combination of Meier and Okayasu is not possible.

Appellant further argues that Okayasu discloses that thermal diffusion method which involves diffusion of dopant gas and that it is not the same as contact diffusion and while Okayasu discloses that thermal gas diffusion can be replaced with plasma CVD to form the BSF one would not have done the replacement for contact diffusion. Furthermore, Appellant argues that plasma CVD also has disadvantages which include particulate contamination so one of ordinary skill would have not been motivated to use the plasma CVD of Okayasu.

Appellant further argues that neither Gan or Fogiletti disclose any particular structure of a polysilicon/tunnel oxide/substrate which form a backside junction.

Examiner respectfully disagrees and points to Figure above for discussion of modifications made to Meier.

Meier discloses method of forming a junction which consists of a p-type emitter (220) formed on an n-type substrate (218) which comprises using the electrode (222) as a p-type dopant material and driving in those dopants through annealing (C6/L35-50). Meier discloses the presence of the junction on the backside of the solar cell.

In addition, Meier discloses the presence of a front surface field (216-n+-type layer) which comprises the same type of dopant as the n-type substrate and that the front surface field is formed through thermal diffusion (C5/L43-49)

Okayasu discloses an alternative method of forming a doped emitter or a surface field on a doped substrate. Okayasu discloses depositing a doped polysilicon emitter and a doped surface field on a doped single crystalline substrate ([0014] [0043]).

Okayasu also discloses that the method of depositing doped polysilicon layers is preferable to that of thermal diffusion which involves heating and driving in dopants

because it can be performed at lower temperatures which prevents damage to the substrate and furthermore the thickness of the emitter can be more accurately controlled ([0008]).

Okayasu discloses that in thermal diffusion the dopant source can be provided in one of two ways either dopant gas (as in the case of the front surface field formed by Meier, see Meier C5/L43-49) or a p-type Al layer (as in the emitter formed by Meier, see Meier C6/L35-50) is laminated on the single crystal substrate (see [0005] of Okayasu). Okayasu further discloses that after the dopant is provided the substrate is heated to 1000°C ([0005]) and it is difficult to control the thickness of the doped layers provided this way and degradation of the substrate is known to occur at high temperatures ([0006]-[0008]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the emitter and surface field of Meier with the p-type polysilicon layer and n-type polysilicon of Okayasu, respectively, because of the above advantages.

Examiner notes that Gan and Fogiletti was used to provide motivation for providing a tunnel oxide between the polysilicon emitter and the monocrystalline substrate not to teach the presence of a backside junction.

Foglietti discloses that polycrystalline growth directly on crystalline silicon results in partial realignment of the polycrystalline grains and to suppress this effect a thin oxide can be grown ([0046]).

Gan discloses that the presence of a stable thermal oxide between a polysilicon emitter and a CZ wafer (See pg. 248, first column, and Table 1) results in recombination

occurring primary at the oxide interface and that the presence of this oxide at the interface can be useful for silicon solar cells with polysilicon emitters (See Conclusion, pg. 249).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the interface between the doped polysilicon regions and the monocrystalline substrate by adding an interfacial oxide as disclosed by Fogiletti and Gan because it will allow for optimal grown of the polysilicon region and furthermore will result in recombination primarily occurring at the oxide interface.

2. Anti-reflective Coating On An Oxide Layer

Appellant further argues that anti-reflective layer of Meier (see Fig. 3D, 214) does not disclose that the anti-reflective layer is formed on an oxide layer and is instead formed on the surface of substrate.

Appellant further argues that Gan and Fogiletti do not alleviate this deficiency since neither discloses that there is a polysilicon on a oxide coating on the front surface not an anti-reflective coating on an oxide coating.

Examiner finds that modified Meier discloses between the polysilicon front surface field and the base substrate there is an oxide layer on the front surface of the substrate (See Figure above). Therefore the anti-reflection layer (214) of Meier is on the tunnel oxide layer which is provided on the front surface of the substrate (See Fig. Above).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/DEVINA PILLAY/
Primary Examiner, Art Unit 1757

Conferees:
/JEFFREY T BARTON/
Supervisory Patent Examiner, Art Unit 1757

/Jennifer McNeil/
Primary Examiner, TC 1700

Requirement to pay appeal forwarding fee. In order to avoid dismissal of the instant appeal in any application or ex parte reexamination proceeding, 37 CFR 41.45 requires payment of an appeal forwarding fee within the time permitted by 37 CFR 41.45(a), unless appellant had timely paid the fee for filing a brief required by 37 CFR 41.20(b) in effect on March 18, 2013.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:

Peter John COUSINS

Application No.: 14/504,771 Examiner: PILLAY, DEVINA

Filing Date: October 2, 2014 Art Unit: 1757

Title: FRONT CONTACT SOLAR CELL WITH FORMED EMITTER

REPLY BRIEF FILED UNDER 37 C.F.R. § 41.41

This Reply Brief is responsive to the Examiner's Answer mailed March 19, 2018, and follows the Appeal Brief submitted by the appellant on November 8, 2017.

REMARKS

This Reply Brief responds to the contentions in the Examiner's Answer. Detailed explanations why the pending claims are patentable over the references of record are provided in the Appeal Brief, and not repeated here in the interest of clarity and brevity.

A. CLAIMS 1-4, 7, 9-12, and 14

Claims 1-4, 7, 9-12, and 14 are rejected under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Meier (US 6,262,359), in view of Okayasu (JP 07-106611), in view of Borden (US WO 2009/094578 A2) and further in view of Wenham (US 6,429,037). The rejection is respectfully traversed.

1. Backside junction emitter with tunnel dielectric

Claim 1 is patentable over the combination of Meier, Okayasu, Borden and Wenham at least for reciting: "a tunnel dielectric disposed over the back surface of the substrate; an emitter disposed over the tunnel dielectric, the emitter forming a backside junction with the substrate." Claim 1 recites a structure of a solar cell. In the embodiment of elaim 1, the solar cell has an emitter that is disposed over a tunnel dielectric and forms a ***backside*** (i.e., the side opposite the light incident side) junction with the substrate.

The drawing on page 10 of the Examiner's Answer shows the extent of the proposed modification to Meier. Comparing Meir's original structure,

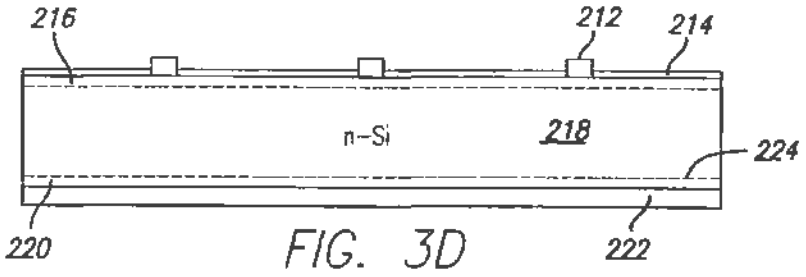


FIG. 3D

to the modified structure,

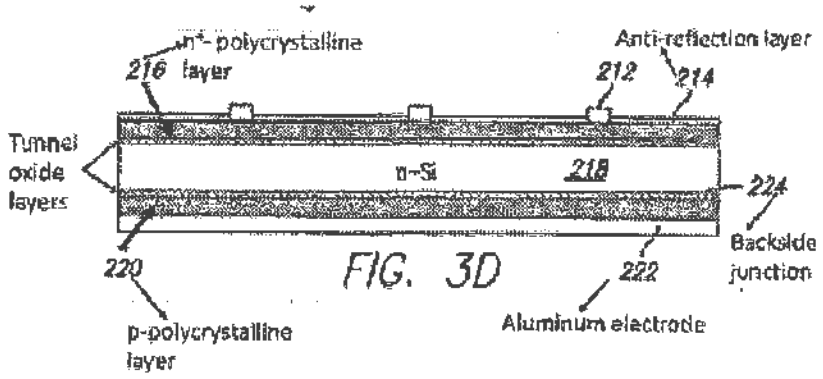


FIG. 3D

one can see immediate major differences.

First, in the original structure, the backside junction 224 is formed by an N-type base layer 218 and a P-type layer 220, both of which are within an N-type single crystal silicon substrate (Meier, column 5, lines 43-49). There is no intervening material, such as the tunnel oxide layer and the P-type polycrystalline layer in the modified structure, between the P-type layer 220 and the N-type base layer 218 because it would block contact of the aluminum contact layer 222 to the substrate to form the P-type layer 220 therein as taught by Meier (Meier, column 6, lines 46-66).

Second, the original structure has a P-type layer 220 within the silicon substrate, whereas the P-type layer 220 is external to the substrate in the modified structure. With regards to solar cell backside structures, Okayasu discloses an alternative way of forming a back surface field (BSF) layer (Okayasu, paragraph 1). A BSF layer forms a high-low (HL) junction, i.e., the highly doped and lightly doped layers of the BSF have the ***same polarity*** on the ***backside*** of the solar cell (Okayasu, paragraph 14) This is opposite to a backside junction, whose layers have ***opposite polarity*** on the ***backside*** of the solar cell. In other words, the proposed modification uses Okayasu's teaching of forming a BSF layer on the backside of the solar cell for a totally different function (i.e., to form a backside junction) in Meier.

Third, the original structure has no tunnel dielectric, whereas the modified structure has a tunnel dielectric. The Examiner's Answer indicates that Borden (or Foglietti and Gan in the other set of rejections) was used to provide motivation for providing a tunnel oxide between a polysilicon layer and a monocrystalline substrate. It is respectfully submitted that just because a tunnel oxide can be used between a

polysilicon layer and a monocrystalline substrate does not mean that one of ordinary skill in the art would do so for a particular structure as claimed. Here, Okayasu itself, the source of the polysilicon layer in the modified structure, does not teach a tunnel oxide between polysilicon and the substrate.

It is thus respectfully submitted that, comparing the original structure to the modified structure, the rejection is based on extensive modifications that could not have been made without guidance from the present application.

2. Anti-reflective Coating On An Oxide Layer

Claim 1 is patentable over the combination of Meier, Okayasu, Borden, and Wenham at least for reciting: "an oxide layer disposed on the front surface of the substrate; an anti-reflective coating on the oxide layer."

In the embodiment of claim 1, an oxide layer is disposed on the front surface of the substrate, and an anti-reflective coating is on the oxide layer.

As explained in the appeal brief, Meier and Borden do not disclose an anti-reflective coating on an oxide layer.

The Examiner's Answer indicates that "Examiner finds that modified Meier discloses between the polysilicon front surface field and the base substrate there is an oxide layer on the front surface of the substrate (see Figure above, tunnel oxide on front and back surfaces)" (Examiner's Answer, page 13). It is respectfully submitted that the Examiner's Answer does not provide articulated reasoning on how a tunnel oxide ends up on the front side of the modified structure.

The modified structure has an N-type polycrystalline layer and a tunnel oxide on the front or light incident side of the substrate. It is respectfully submitted that there is no support for this modification. In the modified structure, a polycrystalline layer is on both sides of the substrate, with a tunnel oxide on both sides of the substrate. It is respectfully submitted that there is no teaching or suggestion in the prior art that a polycrystalline layer with a tunnel oxide can be used on both sides of the substrate, or whether such as solar cell structure would even work or would have practical efficiency given that the

polycrystalline layer and the tunnel oxide would have to receive and allow light to pass through on the front side (i.e., light incident side).

Therefore, it is respectfully submitted that claim 1 is patentable over the combination of Meier, Okayasu, Borden, and Wenham.

Claims 2-4 are patentable over the combination of Meier, Okayasu, Borden, and Wenham at least for depending from claim 1.

Claim 9 is patentable over the combination of Meier, Okayasu, Borden, and Wenham at least for reciting: "an emitter over the back surface of the substrate, the emitter forming a backside junction with the substrate; a first dielectric between the emitter and the back surface."

As explained, it is respectfully submitted that the combination of Meier, Okayasu, Borden, and Wenham does not teach or suggest a backside junction emitter and a first dielectric between the backside junction emitter and the back surface of the substrate.

Claim 9 is further patentable over the combination of Meier, Okayasu, Borden, and Wenham at least for reciting: "a second dielectric on the front surface of the substrate; an anti-reflective coating on the second dielectric."

As explained, it is respectfully submitted that the combination of Meier, Okayasu, Borden, and Wenham does not teach or suggest an anti-reflective coating that is formed on a dielectric on the front surface of the substrate.

Claims 10-12 are patentable over the combination of Meier, Okayasu, Borden, and Wenham at least for depending from claim 9.

B. CLAIMS 1-4, 7, 9-12, and 14

Claims 1-4, 7, 9-12, and 14 are rejected under pre-AIA 35 U.S.C. §103(a) as being unpatentable over Meier (US 6,262,359), in view of Okayasu (JP 07-106611), in view of Foglietti (US 2002/0142500), in view of Gan (*Polysilicon Emitters for Silicon Concentrator Solar Cells*), and further in view of Wenham (US 6,429,037). The rejection is respectfully traversed.

The Examiner's Answer provides substantially the same reasoning for this set of rejection. Appellant accordingly replies as provided above.

C. CONCLUSION

For at least the above reasons, allowance of the pending claims is respectfully requested.

Respectfully submitted,

Dated: MAY 7, 2018

Patrick Benedicto

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Electronic Patent Application Fee Transmittal

Application Number:	14504771
Filing Date:	02-Oct-2014
Title of Invention:	FRONT CONTACT SOLAR CELL WITH FORMED EMITTER
First Named Inventor/Applicant Name:	Peter John COUSINS
Filer:	Patrick D. Benedicto/jina mangaoang
Attorney Docket Number:	10031.004211

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
APPEAL FORWARDING FEE	1413	1	2240	2240
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2240**



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/504,771	10/02/2014	Peter John COUSINS	10031.0042.11	3342

74254 7590 05/15/2018

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EXAMINER	
PILLAY, DEVINA	

ART UNIT	PAPER NUMBER
1726	

MAIL DATE	DELIVERY MODE
05/15/2018	PAPER

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The time period for reply, if any, is set in the attached communication.

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OKAMOTO & BENEDICTO LLP
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Appeal No: 2018-005662
Application: 14/504,771
Appellant: Peter John COUSINS et al.

Patent Trial and Appeal Board Docketing Notice

Application 14/504,771 was received from the Technology Center at the Board on May 14, 2018 and has been assigned Appeal No: 2018-005662.

In all future communications regarding this appeal, please include both the application number and the appeal number.

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Telephone inquiries can be made by calling 571-272-9797 and referencing the appeal number listed above.

By order of the Patent Trial and Appeal Board.

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14/504,771	10/02/2014	Peter John COUSINS	10031.004211	3342

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EXAMINER
PILLAY, DEVINA

ART UNIT	PAPER NUMBER
1726	

MAIL DATE	DELIVERY MODE
05/09/2019	PAPER

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The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte PETER JOHN COUSINS

Appeal 2018-005662
Application 14/504,771
Technology Center 1700

Before KAREN M. HASTINGS, JEFFREY R. SNAY, and DEBRA L. DENNETT, *Administrative Patent Judges*.

DENNETT, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

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[1] In our Decision, we refer to Application 14/504,771 filed October 2, 2012 as the "'771 Specification" ("Spec."); the Final Office Action dated October 2, 2017 ("Final Act."); the Appeal Brief filed November 8, 2017 ("App. Br."); the Examiner's Answer dated March 19, 2018 ("Ans."); and the Reply Brief filed May 8, 2018 ("Reply Br.").

STATEMENT OF THE CASE

Appellant[2] appeals under 35 U.S.C. § 134(a) from a rejection of claims 1–4, 7, 9–12, and 14. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

The subject matter on appeal relates to bipolar solar cells that include a backside junction formed by an N-type silicon substrate and a P-type polysilicon emitter formed on the backside of the solar cell, and an anti-reflection layer formed on a textured front surface of the silicon substrate. Spec. 2, ll. 14–16. The Specification describes a negative polarity metal contact on the front side of the solar cell making electrical connection to the substrate, and a positive polarity metal contact on the backside of the solar cell making electrical connection to the polysilicon emitter. Spec. 2, ll. 17–19. The '771 Specification explains that front contact solar cells with electrical connection to a diffusion region on the front side of the solar cell are less aesthetic, and thus less preferred, for residential applications. Spec. 2, ll. 3–8. Where aesthetics are not a major requirement, such as in power plants and other applications where power generation is the main concern, front contact solar cells such as the disclosed structures are said to provide a relatively efficient and cost-effective device. Spec. 2, ll. 6–11.

Figure 1 of the '771 Application, reproduced below, shows a schematic cross-section of solar cell **100**[3] in accordance with an embodiment of the invention. Spec. 4, ll. 3–4.

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[2] Appellant identifies SunPower Corporation as the real party in interest. App. Br. 1.

[3] Labels to elements are presented in bold font thru out this Decision, regardless of their presentation in the original document.

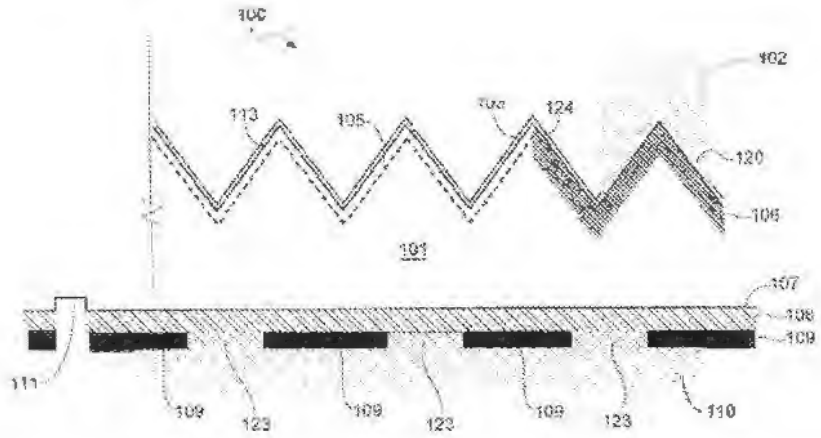


FIG. 1

Solar cell **100** has a front side where metal contact **102** is located and a backside on a same side as metal contact **110**. Spec. 4, ll. 4–5. The front side faces the sun during normal operation to collect solar radiation. Spec. 4, l. 5. Solar cell **100** includes a backside junction formed by a P-type doped polysilicon emitter **108** serving as a P-type diffusion region and an N-type silicon substrate **101** serving as an N-type diffusion region. Spec. 4, ll. 7–9. The front side surface of the substrate **101** is randomly textured (labeled as **113**) and includes N-type doped regions **105** and **106** formed in the substrate. Spec. 4, ll. 12–14. N-type doped region **105** provides low front surface recombination and region **106** provides low contact resistance and minimizes contact recombination. Spec. 4, ll. 14–17. Anti-reflective coating of silicon nitride layer **103** is formed on the textured front side surface of the substrate **101**. Spec. 4, ll. 22–23. Passivating oxide **124** may comprise silicon dioxide thermally grown on the front side surface of the substrate **101**. Spec. 5, ll. 1–2. Polysilicon emitter **108** may be formed on tunnel oxide layer **107**. Spec. 5, ll. 4–5. Metal contact **110** electrically connects to polysilicon emitter **108** and provides a positive polarity terminal to allow an external electrical circuit to be coupled to and be powered by

solar cell **100**. Spec. 5, ll. 10–14. On the front side of solar cell **100**, metal contact **102** electrically connects to region **106** through contact holes through the silicon nitride layer **103** and provides a negative polarity terminal to allow an external electrical circuit to be coupled to and be powered by solar cell **100**. Spec. 5, ll. 19–22.

Claim 1, reproduced below, illustrates the claimed subject matter:

1. A solar cell, comprising:

a substrate having a front surface that faces the sun to collect solar radiation during normal operation and a back surface opposite the front surface;

an oxide layer disposed on the front surface of the substrate;

an anti-reflective coating on the oxide layer;

a tunnel dielectric disposed over the back surface of the substrate;

an emitter disposed over the tunnel dielectric, the emitter forming a backside junction with the substrate;

a doped diffusion region in the substrate;

a front electrode that is coupled to the doped diffusion region on the front surface of the substrate; and

a back electrode that is coupled to the emitter on the back surface of the substrate.

App. Br. 13 (Claims App.).

REFERENCES

The Examiner relies on the following prior art in rejecting the claims on appeal:

Meier et al. ("Meier")	US 6,262,359 B1	July 17, 2001
Wenham et al. ("Wenham")	US 6,429,037 B1	Aug. 6, 2002
Foglietti et al. ("Foglietti")	US 20002/0142500 A1	Oct. 3, 2002
Okayasu et al. ("Okayasu")[4]	JP 07106611	Apr. 21, 1995
Borden	WO 2009/094578 A2	July 30, 2009

Gan and Swanson, *POLYSILICON EMITTERS FOR SILICON CONCENTRATOR SOLAR CELLS*, Stanford Electronics Laboratories. Electric Power Research Institute, 1 Conf. Record of IEEE Photovoltaic Specialists Conf., 245–250 (1990)

REJECTIONS

The Examiner maintains the following rejections under 35 U.S.C. § 103(a)[5]: (1) claims 1–4, 7, 9–12, and 14 over Meier in view of Okayasu, Borden, and Wenham; and (2) claims 1–4, 7, 9–12, and 14 over Meier in view of Okayasu, Foglietti, Gan, and Wenham. Final Act. 2–8.

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[4] The Examiner refers to a human translation of Okayasu (*see* Final Act. 2) to which Appellant does not object.

[5] Because this application was filed before the March 16, 2013, effective date of the America Invents Act, we refer to the pre-AIA version of the statute.

OPINION

Rejection 1 over Meier in view of Okayasu, Borden, and Wenham

Appellant argues for patentability of claim 1 and its dependent claims 2–4 and 7 as a group, and for claim 9 and its dependent claims 10–12 as a group. App. Br. 3–7. However, Appellant's arguments regarding claim 9 do not differ substantively from those made in support of patentability of claim 1. *Compare* App. Br. 3–6 *with* App. Br. 7. We, therefore, select claim 1 as representative of the group. 37 C.F.R. § 41.37(c)(1)(iv).

With respect to claim 1, the Examiner finds that Meier teaches the majority of the limitations. Final Act. 3. The Examiner finds that Meier teaches a method of forming a junction consisting of a p-type emitter on an n-type substrate which comprises using an aluminum electrode as a p-type dopant material and driving the dopant in through annealing. Ans. 11 (citing Meier col. 6, ll. 35–50). The Examiner further finds that Meier discloses the presence of a front surface field formed through thermal diffusion and comprised of the same type of dopant as the n-type substrate. *Id.* (citing Meier col. 5, ll. 43–49).

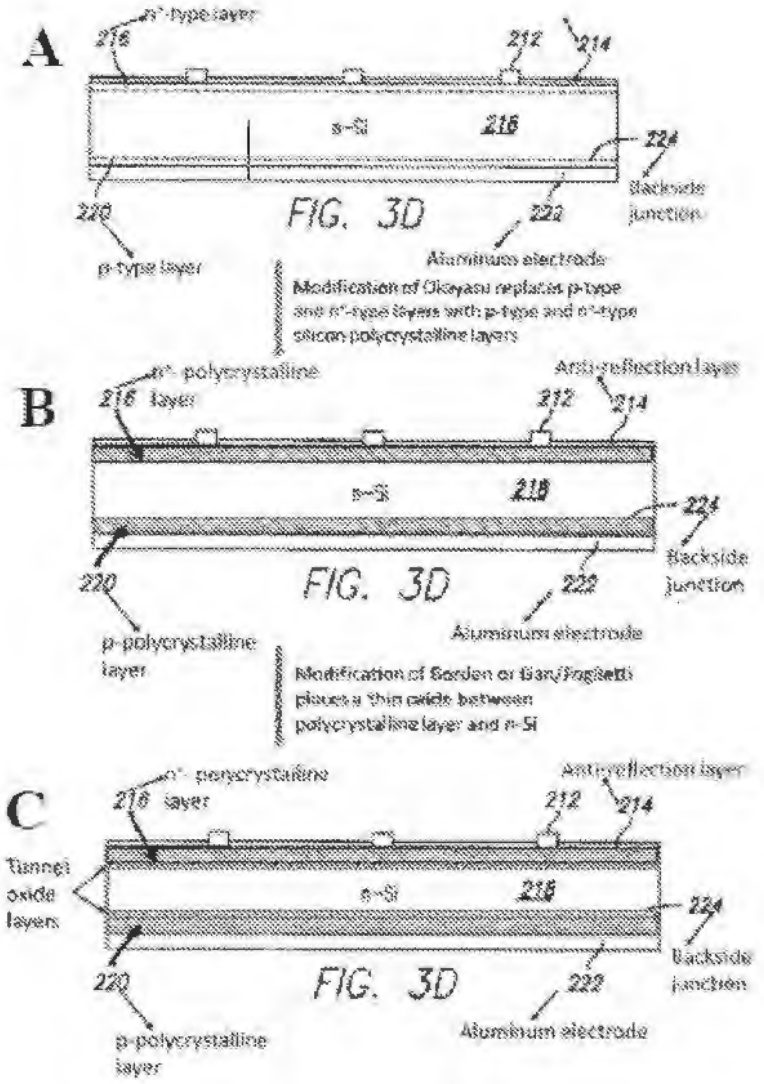
The Examiner finds that Okayasu discloses an alternative method for forming a doped emitter or a surface field on a dope substrate. *Id.* The Examiner finds that Okayasu teaches depositing a doped polysilicon emitter and dope surface field on a doped single crystalline substrate. *Id.* (citing Okayasu ¶¶ 14, 43). The Examiner finds that Okayasu teaches that its method of depositing doped polysilicon layers is preferable to that of thermal diffusion (as taught in Meier) because it can be performed at lower temperatures, preventing damage to the substrate, and allows more accurate control of the emitter thickness. *Id.* (citing Okayasu ¶ 8).

The Examiner concludes that one of ordinary skill in the art at the time of the invention would have found it obvious to employ Okayasu's method of forming an emitter or surface field in Meier's back junction solar cell for the advantages articulated by Okayasu. *Id.* at 12.

The Examiner finds that Meier as modified by Okayasu does not disclose a tunneling dielectric oxide between the emitter/front surface field and the substrate. Final Act. 4. However, the Examiner finds that Borden discloses that tunnel oxides can be used in solar cells between doped polysilicon and monocrystalline substrates on both front and back surfaces of the monocrystalline substrate. *Id.* The Examiner finds that Borden teaches that the tunnel oxide prevent epitaxial growth of amorphous silicon and provides a layer to protect the surface from plasma damage of the deposited emitter layer. *Id.*[6] The Examiner concludes that it would have been obvious to the skilled artisan to modify the interface between polycrystalline layers and a monocrystalline substrate front and back surface by having a tunneling oxide at the interfaces for the benefits expressed by Borden. *Id.*

The Examiner provides annotated figures, reproduced on the next page, in support of the rejection:

[6] The Examiner cites to paragraph 15 of Borden in support of the finding, however, the disclosure is found at paragraph 8.



Ans. 10.

Figure A is a reproduction of Meier Figure 3D annotated by the Examiner to identify a junction consisting of p-type emitter **220** formed on n-type substrate **218** which comprises using aluminum electrode **222** as a p-type dopant material. *Id.* at 11 (citing Meier col. 6, ll. 35–50). The dopants are driven into the substrate through annealing. *Id.* Junction **224** is shown on the backside of the solar cell. *Id.* Front surface field **216** (n+-type emitter) comprises the same type of dopant as the n-type substrate and is formed through thermal diffusion. *Id.* (citing Meier col. 5, ll. 43–49).

Figure B illustrates the Examiner's modification of Meier by Okayasu. Figure B shows the result of modifying Meier such that the emitter and surface field produced by Meier's process are replaced with a p-type polysilicon layer and a n-type polysilicon layer taught by Okayasu. *See* Ans. 12.

Figure C shows modification of the *combination* of Meier and Okayasu (Figure B) with tunnel oxide layers taught by Borden. In Figure C a tunnel oxide layer is shown between the n+-polycrystalline layer and the substrate and between the p-polycrystalline layer and the substrate.

Appellant argues that the combined references fail to teach a backside junction emitter with a tunnel dielectric. App. Br. 3–5; *see also* Reply Br. 2–4. Appellant contends that the *original* structure has the backside junction **224** formed by n-type base layer **218** and p-type layer **220**, both of which are within the n-type single crystal silicon substrate. Reply Br. 3. Appellant argues that an intervening layer (tunnel oxide layer) would block contact of Meier's aluminum layer contact layer **222** to substrate **218** to form p-type layer **220**.

We do not find Appellant's arguments persuasive to show reversible error. The rejection is based on combining Borden with the *modified* structure that would result from altering Meier's method with that of Okayasu, not on applying Borden's tunnel oxide layers to Meier's structure. *See* Ans. 11–12. The *modified* Meier solar cell does not require contact of the aluminum layer with the substrate in order to form the p-type layer. Rather, the p-type layer of the modified structure is formed by depositing a doped polysilicon emitter on a doped single crystalline substrate. *See* Okayasu ¶¶ 14, 43. Appellant's argument against combining Meier directly

with Borden thus fails to identify reversible error. *In re Jung*, 637 F.3d 1356, 1365 (Fed. Cir. 2011) (explaining that even if the examiner had failed to make a prima facie case, the Board would not have erred in framing the issue as one of reversible error because it has long been the Board's practice to require an appellant to identify the alleged error in the examiner's rejections). Each reference cited by the Examiner must be read, not in isolation, but for what it fairly teaches in combination with the prior art as a whole. *See In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). Appellant's avoidance of Okayasu's disclosures fails to consider the combination of the entirety of the art cited by the Examiner.

Appellant argues that Okayasu teaches forming a back surface field (BSF) layer that forms a high-low junction with a highly doped and lightly doped layer having the same polarity on the backside of the solar cell. Reply Br. 4. Appellant contends that the proposed modification uses Okayasu's teaching of forming a BSF layer on the solar cell backside for a totally different function (forming a backside junction) in Meier. App. Br. 4; *see also* Reply Br. 3. Appellant argues that Meier and Okayasu solve the same problem: that of the conventional method of forming doped layers. App. Br. 5. According to Appellant, one of skill in the art would not have been motivated to replace Meier's contact diffusion method with the BSF manufacturing method of Okayasu because Okayasu discloses the plasma CVD method has advantages, but introduces particulates that deteriorate the BSF layer. App. Br. 5.

Appellant again fails to persuade us of reversible error. The Examiner employs Okayasu for its teaching of depositing a doped polysilicon layer on a doped substrate. *See* Ans. 11. The rejection is not based on a finding that

the BSF layer (as opposed to the doped polysilicon layer) can be substituted for Meier's p-type emitter. Okayasu discloses that the *prior art* plasma CVD method has advantages, but introduces floating foreign substances that are mixed in the n+ silicon layer of p+ silicon layer. Okayasu ¶ 9. However, Okayasu addresses preventing generation of floating foreign substances in the inventive process. *Id.* ¶ 16. "The prior art must be considered *as a whole* for what it teaches." *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1164 (Fed. Cir. 2006). Okayasu would have given the skilled artisan adequate motivation to combine its teaching with that of Meier in disclosing the problems associated with the thermal diffusion method. *Id.* ¶¶6–8.

In disputing the rejection Appellant also argues that Meier's original structure has p-type layer **220** within the silicon substrate, whereas the modified structure has the p-type layer external to the substrate. Reply Br. 3. However, other than a statement of that difference, Appellant does not explain its importance.

Appellant contends that Meier's original structure has no tunnel dielectric, but the modified structure does. *Id.* Appellant argues that merely because a tunnel oxide can be used between a polysilicon layer and a monocrystalline substrate does not mean that one of ordinary skill would do so. *Id.* at 4. Appellant urges that there is no teaching or suggestion in the prior art that a polycrystalline layer with a tunnel oxide can be used on both sides of the substrate, or whether such a solar cell structure would work or have practical efficiency. *Id.*

Borden's invention concerns polysilicon emitter solar cells and includes forming a masking oxide layer on the *front and back* of the cell.

Borden Abstract. The Examiner's explanation of the reasons one of ordinary skill in the art would have had to combine Borden's tunnel oxide with the modified Meier structure (preventing epitaxial growth of amorphous silicon and providing a layer to protect the surface from plasma damage of the deposited emitter layer) is sufficient when an allowance is made for "the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

Appellant argues that claim 1 recites an oxide layer disposed on the front surface of the substrate and an anti-reflective coating on the oxide layer. App. Br. 6. Appellant contends that Meier discloses an anti-reflective coating formed on the surface of the substrate (not on an oxide layer) and Borden does not disclose an anti-reflective coating. Reply Br. 6.

The argument fails to show reversible error. Appellant attacks Meier and Borden individually, ignoring that the rejection is based on the combined references. "Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

We sustain the rejection of claim 1 for the reasons given above. For these same reasons, we sustain the rejection of claims 2–4, 7, 9–12, and 14.

Rejection 2 over Meier in view of Okayasu, Foglietti, Gan, and Wenham

The Examiner's findings and Appellant's arguments in Rejection 2 regarding the combination of Meier and Okayasu are identical to those in our discussion of Rejection 1 *supra*. We do not repeat them here.

The Examiner finds that Foglietti discloses that polycrystalline growth directly on crystalline silicon results in partial realignment of the polycrystalline grains and this effect can be suppressed by growth of a thin oxide. Final Act. 7 (citing Foglietti ¶ 46). The Examiner finds that Gan teaches that he presence of a stable thermal oxide between a polysilicon emitter and a CZ layer. *Id.* The Examiner concludes that it would have been obvious to one of ordinary skill in the art to modify the interface between the doped polysilicon regions and the monocrystalline substrate by adding an interfacial oxide as disclosed by Foglietti and Gan to allow for optimal growth of the polysilicon region and result in recombination occurring primarily at the oxide interface. *Id.*

Appellant's arguments against combining Foglietti or Gan with the modified Meier is substantially the same as that made in opposing Rejection 1. *Compare* App. Br. 10–11 *with* App. Br. 6–7.

For the reasons provided *supra* relating to Rejection 1, we do not find Appellant's arguments persuasive to show reversible error, and sustain Rejection 2.

DECISION

For the above reasons, the Examiner's rejection of claims 1–4, 7, 9–12, and 14 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED



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14/504,771	10/02/2014	Peter John COUSINS	10031.0042US1	3342

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EXAMINER	
PILLAY, DEVINA	

ART UNIT	PAPER NUMBER
1726	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of Abandonment	Application No.	Applicant(s)
	14/504,771	COUSINS, Peter John
	Examiner	Art Unit
	DEVINA PILLAY	1726

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

This application is abandoned in view of:

1. ☐ Applicant's failure to timely file a proper reply to the Office letter mailed on _____.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☐ A proposed reply was received on _____, but it does not constitute a proper reply under 37 CFR 1.113 to the final rejection. (A proper reply under 37 CFR 1.113 to a final rejection consists only of:(1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) if this is utility or plant application, a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. Note that RCEs are not permitted in design applications.)
   (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a bona fide attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 7 below).
   (d) ☐ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
   (b) ☐ The submitted fee of $ _____ is insufficient. A balance of $ _____ is due
   The issue fee required by 37CFR 1.18 is $ _____ . The publication fee, if required by 37 CFR 1.18(d), is $ _____
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file corrected drawings as required by and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ No corrected drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record or other party authorized under 37 CFR 1.33 (b). See 37 CFR 1.138(b).

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34) upon the filing of a continuing application

6. ☑ The decision by the Board of Patent Appeals and Interference rendered on 09 May 2019 and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☐ The reason(s) below:

_____

/DEVINA PILLAY/
Primary Examiner, Art Unit 1726

Petitions to revive under 37 CFR 1.137, or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.