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SOLAR CELLS

Operating Principles,
Technology and
System Applications

MARTIN A. GREEN

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Chapter

7

IMPROVED SILICON CELL TECHNOLOGY

7.1 INTRODUCTION

In Chapter 6, the standard technology used in the past to produce silicon solar cells was described. In converting quartzite, the source material, to encapsulated cells, several steps were seen to be costly and energy-intensive.

Activity worldwide is being directed at reducing these costs. The present chapter describes some of the most promising new silicon technology for each of the processing steps outlined in Chapter 6. Most of this technology is at an advanced stage of development. Some aspects are being evaluated at the pilot production stage, whereas others have already been incorporated into commercial products.

7.2 SOLAR-GRADE SILICON

It was seen in Chapter 6 that solar cells presently use the ultrapure silicon produced for the semiconductor industry. However, in tran-

sistors and integrated circuits, the emphasis is on silicon quality, and material costs are relatively unimportant. For solar cells, it is worthwhile considering a trade-off between performance and cost.

As mentioned in Section 3.4.4, impurities in solar cells generally introduce allowed levels into the forbidden gap and thereby act as recombination centers. It was seen in Section 5.4.2 that an increased density of such centers will decrease the cell efficiency. Figure 7.1 shows the experimental results for a range of different metallic impurities, when each is the only impurity present apart from the dopant (Ref. 7.1). Although some metallic impurities (Ta, Mo, Nb, Zr, W, Ti, and V) can reduce cell performance when present in extremely small concentrations, others can be present in concentrations in excess of $10^{15}/\text{cm}^3$ before becoming a problem. This is about 100 times higher than impurity levels in semiconductor-grade silicon (SeG-Si). It makes it likely that an alternative, less expensive process might produce a less pure *solar-grade* silicon (SoG-Si) which still gives cells of adequate performance. Several alternative processes appear capable of producing silicon of quality not appreciably lower than Se-G but at a fraction of the cost of conventional technology.

One of the more promising is that developed by the Union Carbide Corporation. It involves the preparation of silane (SiH_4) from

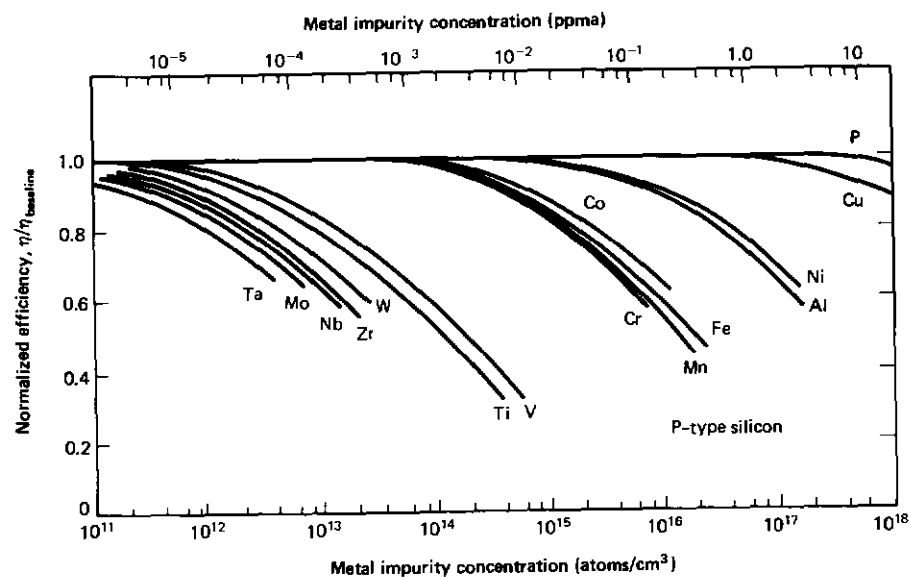


Figure 7.1. Effect of different secondary impurities on the performance of silicon solar cells (After Ref. 7.1, ©1978 IEEE.)

metallurgical-grade silicon and the subsequent deposition of silicon from silane (Ref. 7.2). Analysis of this process indicates that it is capable of producing silicon at one-fifth the cost of the present commercial process using only one-sixth of the processing energy. An alternative process at an advanced stage of development is that developed by Batelle Columbus Laboratories. It is based on the zinc reduction of silicon tetrachloride (Ref. 7.3). It is probable that improved processes such as these will replace the conventional Siemens process for producing silicon not only for the solar cell industry but also for the semiconductor electronics industry in general.

7.3 SILICON SHEET

7.3.1 Sheet Requirements

Having produced purified silicon, it is then necessary to convert it into the form of thin sheets of good crystallographic quality for use as solar cells. To obtain the full photovoltaic output from the material, it only has to be $100\ \mu\text{m}$ or so thick. In the past, the approach used has been to form a large single-crystal ingot using the Czochralski (CZ) process and then slice thin wafers from this ingot. This approach is very inefficient in converting bulk silicon into large areas of solar cells. Not only is over half the silicon lost in sawing it into wafers, but cutting limitations result in thicker wafers than essential. Also, the wafers are circular, which means that they cannot be packed very densely when encapsulated into solar modules unless trimmed to a square or hexagonal shape.

7.3.2 Ingot Technologies

The Czochralski approach is an example of an *ingot technology*. The fundamental limitation of such a technology is that the ingots produced have to be sliced up into wafers with the disadvantages already mentioned.

The standard Czochralski process can be modified to operate on a semicontinuous basis with resultant cost savings (Ref. 7.4). The fact that the process produces cylindrical ingots¹ is also a disadvantage in solar cell applications.

A simpler approach to producing ingots, particularly those of square cross section, is to use a process similar to casting. This will

¹With modifications, ingots with an approximately square cross section can be prepared by the Czochralski process (Ref. 7.5).

generally result in a polycrystalline ingot which is not ideal for solar cell applications. However, with careful control over the conditions under which molten silicon solidifies, silicon of large grain size can be formed. With a suitable "mold" material, such large-grained material can produce solar cells of good performance (Ref. 7.6).

With a suitable seed and a method of controlling the rate of solidification as in the heat-exchanger method (Ref. 7.7), it is possible to produce essentially single-crystal ingots of quite massive proportions with a "casting" approach. The performance of cells fabricated from such material has been comparable to that of cells made of good-quality Czochralski material. Studies indicate that this approach has a marked economic advantage over even the advanced Czochralski techniques (Ref. 7.8).

7.3.3 Ribbon Silicon

The limitations of the ingot approach can be avoided if the silicon can be formed directly into sheets or ribbons. Several techniques have been developed for achieving this.

The first to be developed to the stage of producing commercial cells is the *edge-defined film-fed growth* (EFG) method, as illustrated in Fig. 7.2. This technique bears some relationship to the Czochralski process except that the shape of the crystal pulled is defined by a graphite "die." As a consequence, it is possible to obtain crystals in the form of thin ribbons directly from the melt (Ref. 7.9). Very high production rates of silicon can be obtained by pulling several ribbons simultaneously from the same melt (Ref. 7.10).

The major problem with this technique relates to the quality of the material produced. The process produces material of relatively poor crystallographic quality compared to the Czochralski process. Owing to the nature of the growth process, impurities introduced into the molten silicon from the die, crucible, and surrounding regions of the growth furnace are incorporated into the growing ribbon. (In other crystal growth processes, most of these are preferentially rejected from the growing crystal to the molten silicon.) In addition, the molten silicon tends to react with the graphite die. This can result in silicon carbide precipitates in the ribbon which can disrupt its growth and degrade the properties of subsequently fabricated cells.

The dendritic web method illustrated in Fig. 7.3 overcomes some of these disadvantages. By controlling temperature gradients, it is possible to encourage the growth of parallel dendrites into the molten material. As these are pulled out of the melt, a film of molten silicon is trapped between them (Ref. 7.11). This subsequently solid-

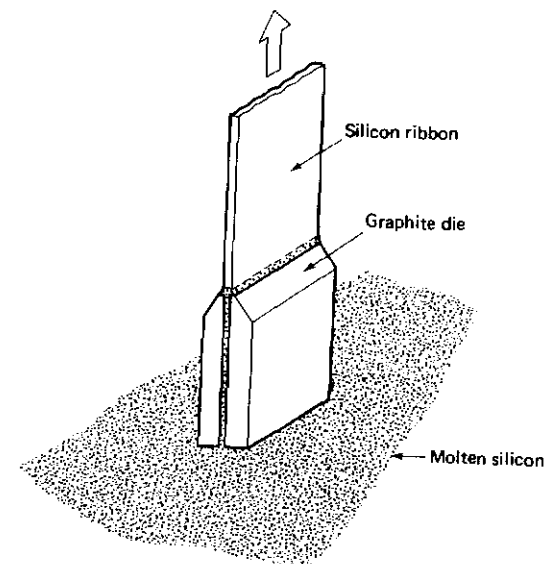


Figure 7.2. Essential features of the edge-defined film-fed growth method for producing ribbon crystals of silicon. The molten silicon moves up the interior of the graphite die by capillary action. The ribbon shape is defined by the shape of the top of the die.

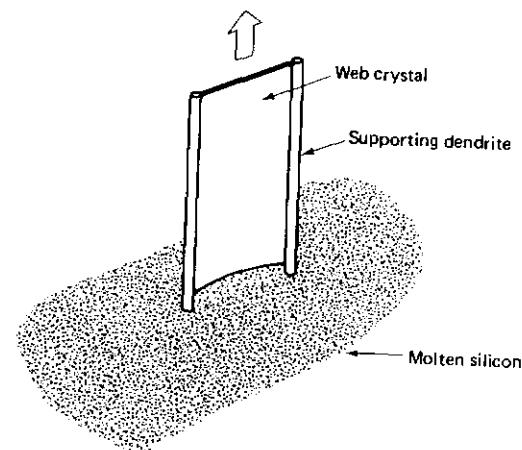


Figure 7.3. Dendritic web approach to producing silicon ribbon. No die is required. The shape of the ribbon is controlled by thermal gradients in the molten silicon. The dendrites down the edge of the ribbon solidify first. As these are drawn out of the melt, a thin layer of initially molten silicon is trapped between them.

ifies to give a thin ribbon of silicon bounded by the thicker dendrites. These can be removed and recycled after cell fabrication on the ribbon section. No die is required and material properties are nearly as good as these obtained from the Czochralski process. The relatively low production rate of silicon crystal material by this process has been its major disadvantage.

Relatively small samples of silicon ribbon produced by both the EFG and dendritic web processes are compared in Fig. 7.4. Note the corrugated surface finish typical of material produced by the EFG process and the mirror finish characteristic of dendritic web material.

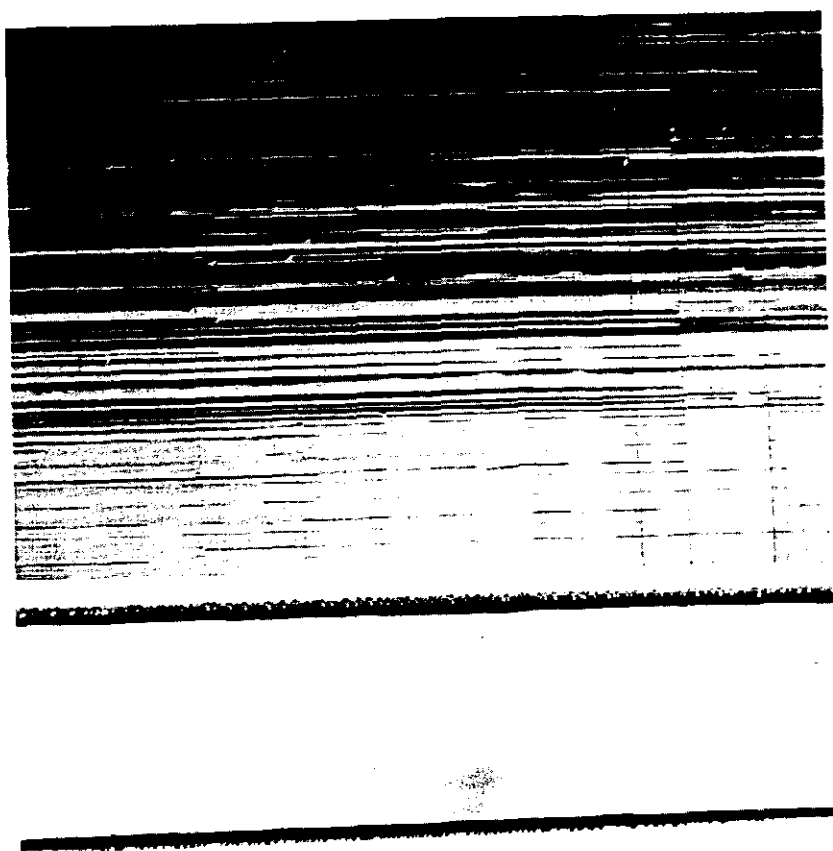


Figure 7.4. Comparison of the physical appearance of EFG and dendritic web silicon ribbon crystals. The dendrites are removed from the latter after cell processing. (Ribbon courtesy of Japan Solar Energy Corporation and Westinghouse Research Laboratories.)

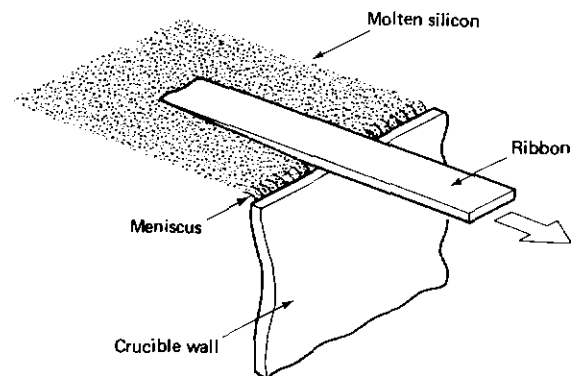


Figure 7.5. Horizontal or low-angle growth method for producing silicon ribbon. Ribbons can be produced at very high rates, but dimensional control has been a problem in the past.

Several other ribbon growth processes are at a less advanced stage of development. One distinguished by very high rates of ribbon production is the *horizontal or low-angle growth method* of Fig. 7.5. The major developmental problems with this technique have related to control of the ribbon dimensions (Ref. 7.12). Casting of silicon directly into sheet or ribbon form has also been explored (Refs. 7.6 and 7.13).

7.4 CELL FABRICATION AND INTERCONNECTION

The disadvantage of the standard technique for fabricating cells on silicon wafers as described in Chapter 6 is that it is a "batch"-oriented technique. As such, it is capable of only relatively low throughput and also is extravagant in the use of materials, particularly metal for forming the cell contacts. Several approaches are now being used in commercial devices which overcome these limitations and, as a bonus, result in cells of higher performance.

One major development has been the use of silicon wafers with *textured surfaces*. Using selective etching, it is possible to form small pyramids on the surface of silicon wafers (Ref. 7.14). The appearance of these pyramids greatly magnified under the scanning electron microscope is shown in Fig. 7.6. Light reflected from the side of one of these pyramids is reflected downward, getting a second chance of being coupled into the cell. With the use of an antireflection coating, reflection losses can be reduced to less than a few percent. As shown

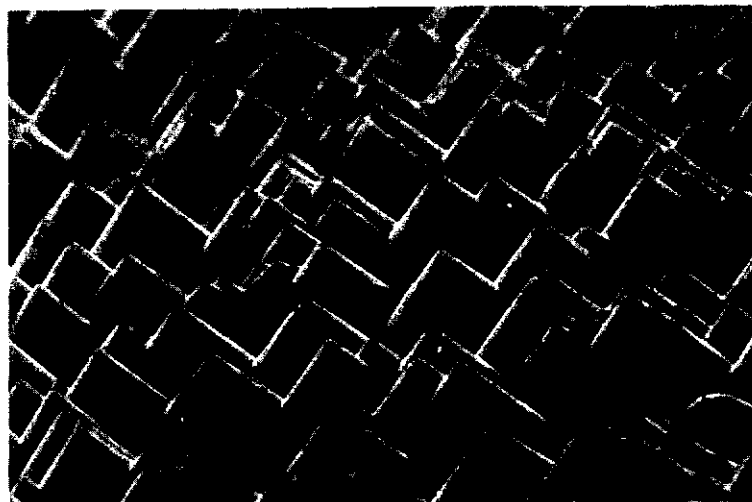


Figure 7.6. Appearance of a textured silicon surface under a scanning electron microscope. The peaks are typically 10 μm high and are the tops of square-based pyramids. The sides of these pyramids are intersecting (111) planes within the crystal structure of the silicon.

in Chapter 8, this technique can give acceptable performance even without antireflection coatings.

In the previous standard process, the p - n junction was formed by diffusing impurities on a batch basis. A more cost-effective approach is to spray layers containing the required dopant onto the wafer surface and to diffuse the impurity in using a continuous-belt process (Ref. 7.15). An alternative approach is to use a technique known as *ion implantation* (Ref. 7.16). Ions of the dopant are accelerated to high velocities and directed at the wafer surface. These are embedded in the silicon wafer near the surface they impact. A subsequent annealing step removes the damage inflicted on the silicon lattice by this process and also "activates" the dopants in an electronic sense. Pulsing by an electron beam or laser is an energy-efficient annealing approach. A very tidy process for the high-volume production of solar cells based on ion implantation is indicated in Fig. 7.7.

Further improvement in solar cell performance has been obtained by paying attention to obtaining a low-surface-recombination-velocity contact to the rear of the cell. As indicated in Chapter 5, this improves the open-circuit voltage of the cell and it also marginally increases the current output. The use of what is somewhat

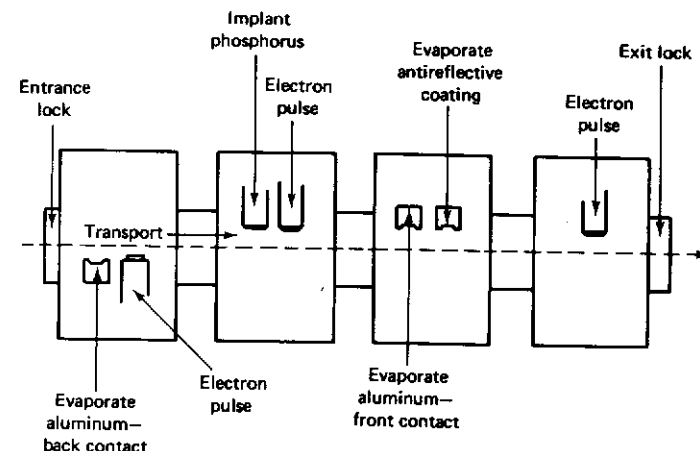


Figure 7.7. Schematic diagram of a continuous vacuum process for producing solar cells based on ion-implanted junctions, evaporated metal contacts, and pulsed electron beam annealing. (After Ref. 7.16, © 1976 IEEE.)

inappropriately called a *back surface field* (BSF) is one technique for achieving low effective recombination velocities at the rear of the cell. As indicated in Fig. 7.8, a heavily doped region is included right at the back contact to the cell. From theoretical considerations, the interface between this region and the more lightly doped bulk regions can be shown to act as a low-recombination-velocity surface. Not only does this technique improve voltage and current output as mentioned, but it also makes it easier to make a low-resistance contact to the silicon at the rear of the cell. In practice, the most effective technique for producing this "back surface field" has been to screen print an alu-

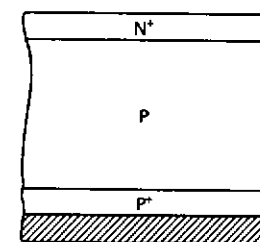


Figure 7.8. Sketch of the N^+PP^+ solar cell. The heavily doped P^+ region at the rear of the cell blocks minority carrier flows, making the PP^+ junction plane an effective low-recombination-velocity surface.

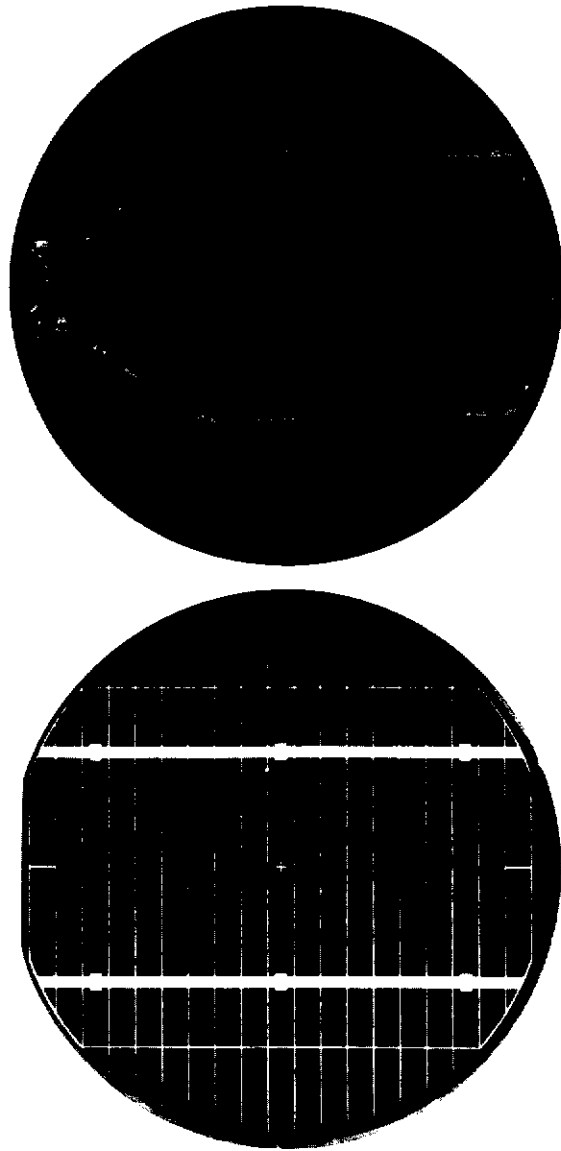


Figure 7.9. Solar cells of 10 cm in diameter with solder-dipped (upper) and screen-printed (lower) top-layer metallization.

minum-based paste onto the rear of the cell and alloy the aluminum into the silicon in a subsequent firing step (Ref. 7.15).

Metallization was one of the weak links in the standard solar cell processing sequence of Chapter 6. Two lower-cost processes used in commercial cells are screen printing and electroplating. Both of these prevent wastage of metal and eliminate the requirement for expensive vacuum equipment. In the former, a paste containing the metal is printed onto the silicon wafer through a mask and subsequently fired to remove "binders" in the paste and to lower the metal resistivity. Silver pastes were the first to be used commercially although nickel, aluminum, and copper pastes may be lower-cost alternatives. In the plating approach, a pattern is etched through an insulating layer on the cell surface and the desired metal layer is plated through this. More than one type of metal layer generally is plated sequentially, since few metals by themselves possess the properties of good adherence to silicon, corrosion resistance, low resistivity, and low cost. A final step in this approach may be "solder dipping" to cover the plated metal by a layer of solder for corrosion protection and lower series resistance. Figure 7.9 compares the physical appearance of cells with solder-dipped and screen-printed top-layer metallization.

Spraying appears to be the most cost-effective method for applying the antireflection coating, although with textured surfaces this layer may not be required. Automated machinery has been developed for connecting the cells together and for their encapsulation into solar modules (Ref. 7.17).

7.5 ANALYSIS OF CANDIDATE FACTORIES

Several alternative approaches to producing silicon cells have been outlined in previous sections. To provide common ground for the comparison of economic aspects of these approaches, a costing technique known as SAMICS (Solar Array Manufacturing Industry Costing Standards) has been developed (Ref. 7.18). Using a computer program based on this technique, some of the best documented and validated costing has been done of the processing sequences involved in fabricating solar modules.

Large-capacity factories have been designed based on different combinations of the technologies described in this chapter and the cost of the resulting solar modules compared using the SAMICS methodology. The results have been that several combinations of these technologies appear capable of producing solar modules at costs which

would make them competitive energy generators in some of the large-scale applications described in Chapter 14. The EFG and dendritic web ribbon approaches as well as HEM (heat-exchanger method) with subsequent wafer slicing all appear viable silicon sheet technologies, with the advanced Czochralski approaches lagging somewhat behind (Ref. 7.8).

As an example of an automated factory capable of producing low-cost silicon modules, the characteristics of one of the first to be analyzed by the SAMICS approach will be described (Ref. 7.19). The product resulting from this factory is a 1.2×1.2 m module made up of 192 cells fabricated on EFG ribbon silicon cut to a size of 10×7.5 cm as shown in Fig. 7.10. The module efficiency is 11.4%.

The processing sequence used to produce the module is shown in Fig. 7.11. The Union Carbide process is used to refine metallurgical-grade silicon. Silicon sheet is prepared from this material by the EFG process and cut to size. The major stages in fabricating cells on this material are the application of a back surface field, texture etching, ion implantation of the junction followed by pulse annealing, and the screen printing of contacts. The cells are then encapsulated and tested.

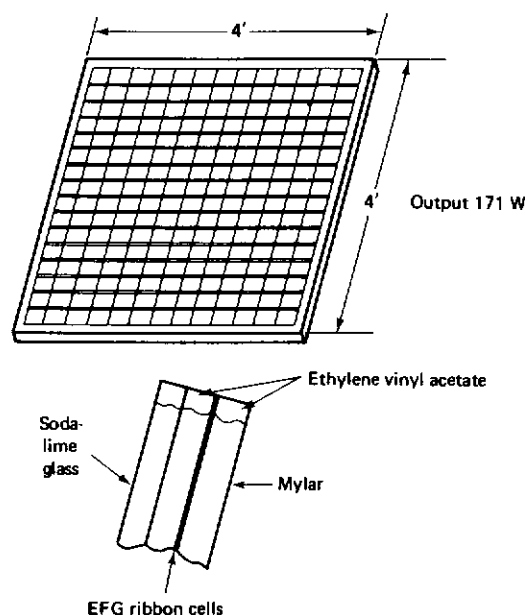


Figure 7.10. Solar cell module produced by the candidate factory described in the text. (After Ref. 7.19.)

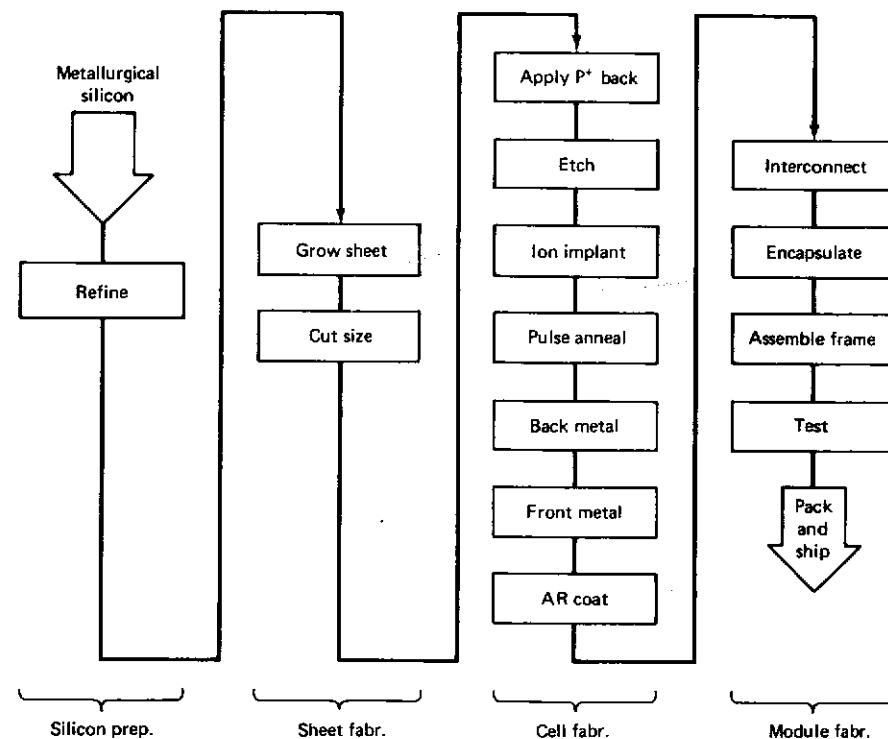
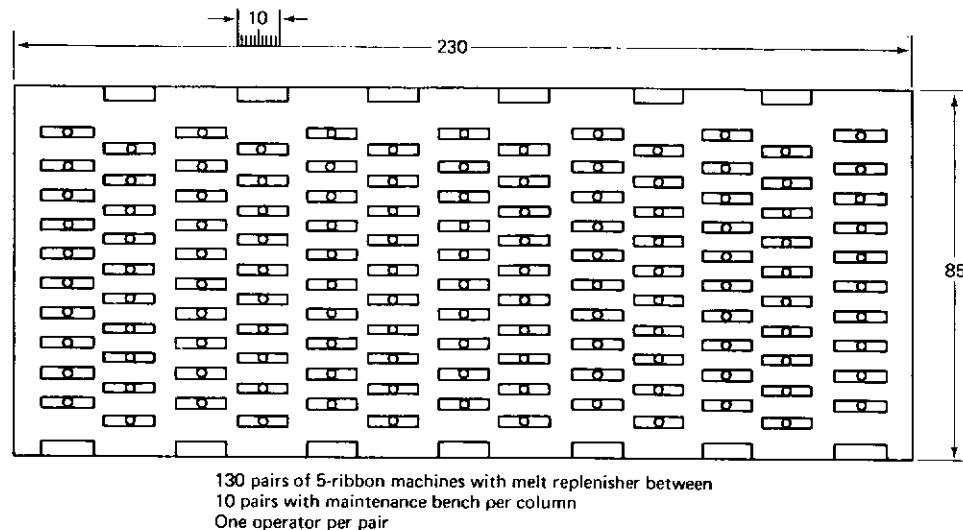


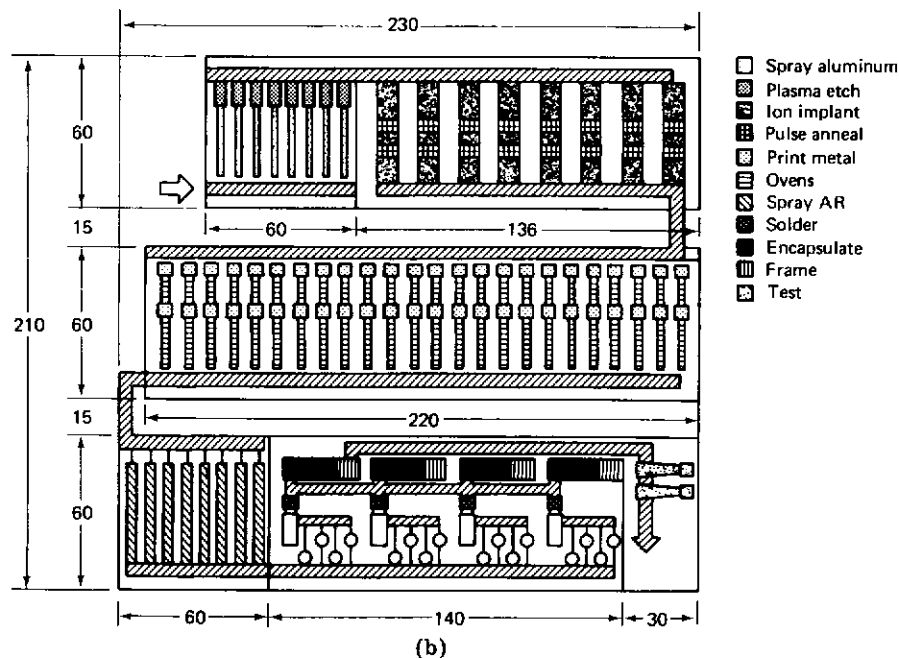
Figure 7.11. Processing sequence used to produce the module of Figure 7.10. (After Ref. 7.19.)

ADM	Silicon refinement 40,800 ft ²	Production rate (W/yr)	250,000,000
		Labor force (all shifts)	1,152 direct 529 indirect
Sheet, cell, and module fabrication 91,630 ft ²		Factory area (ft ²)	
		Silicon refinement	40,800
		Sheet growth	19,550
		Cell fabrication	31,200
		Module fabrication	10,200
		Warehouse	9,779
		Misc. (aisles, shops, cafeteria, etc.)	20,901
		Capital equipment (\$)	
		Silicon refinement	19,400,000 *
		Sheet growth	14,820,000
		Cell and module fabrication	8,219,000
		*Union Carbide	
		Energy payback time sheet, cell, and module	0.179 year

Figure 7.12. Calculated space, labor, and capital requirements (1975 \$US) to produce cells in a volume of 250 MW_p/yr. The calculated selling price of the module (F.O.B. factory) was \$0.46 per W_p in the same monetary units. (After Ref. 7.19.)



(a)



(b)

Figure 7.13. (a) Physical layout of the ribbon crystal pullers for the candidate factory. Each puller produces five ribbons simultaneously using the EFG approach (dimensions are in feet). (b) Physical layout of cell processing, encapsulation, and testing sections of the plant. (After Ref. 7.19.)

To achieve the low costs mentioned, production volume has to be an estimated $250 \text{ MW}_p/\text{yr}$. The labor requirements and area requirements for different steps in the module fabrication are shown in Fig. 7.12. The operating time of the modules to pay back the processing energy invested in them for this processing sequence is a very low 65 days.

To give an idea of the size and physical layout of different sections of the candidate $250 \text{ MW}_p/\text{yr}$ factory, Fig. 7.13(a) shows a possible layout for the sheet-preparation section of the factory. Figure 7.13(b) shows the sections dealing with cell fabrication, encapsulation, and testing.

7.6 SUMMARY

Several advanced technologies have been developed for producing low-cost silicon solar cell modules. These eliminate the deficiencies in the standard processing sequence described in Chapter 6.

Direct growth of silicon ribbons eliminates wafer slicing, which is the weak link in any ingot technology. The main requirements on techniques for fabricating cells on silicon wafers are that they be capable of a high degree of automation and that they do not consume excessive materials. Several processing sequences satisfy these criteria. Economic analysis of candidate factories based on advanced processing sequences show that it should be possible to produce silicon solar cell modules at prices that would make them competitive with conventional sources of electricity, at least in some large-scale applications. A "thin-film" technology as described in Chapter 9 places less severe demands on the quantity of photovoltaic material required. For this reason, approaches other than those based on crystalline silicon, as described in this chapter, will prove even less expensive in the long term.

EXERCISES

- 7.1. The volume density of silicon atoms in a silicon crystal is about $5 \times 10^{28} \text{ m}^{-3}$. According to Fig. 7.1, how many parts per billion of the following impurities can be tolerated in standard solar cells without degrading performance by more than 10%? (a) Mo; (b) Ti; (c) Cu.
- 7.2. (a) The best performance in the near term expected to be able to be maintained in a production setting with advanced silicon ingot slicing techniques is to produce wafers $250 \mu\text{m}$ thick with a cutting or kerf loss

of 150 μm . With such a technology, what is the maximum area of silicon that can be obtained from each kilogram of silicon starting material, assuming that the material lost in cutting is not reclaimed?

- (b) What is the corresponding figure for a ribbon technology that produces ribbons 100 μm thick?
 - (c) If the material produced as above results in cells of 16% and 12% energy-conversion efficiency, respectively, under bright sunlight (1 kW/m^2), find a value for the maximum power-generating capacity of each of the foregoing technologies expressed as peak watts/kilograms.
 - (d) If pure silicon were to be produced at the present volume of metallurgical-grade silicon (~ 1000 million kilograms annually), what would be the maximum possible generating capacity from one year's production for solar cells made by each of the foregoing approaches?
- 7.3. Calculate the maximum packing density (cell area to module area) that can be obtained for circular cells packed into rectangular modules.

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Chapter 8

DESIGN OF SILICON SOLAR CELLS

8.1 INTRODUCTION

In previous chapters, standard and improved technologies for producing silicon solar cells have been described. In the present chapter, considerations relevant to the detailed design of silicon cells will be discussed. Answers will be found to questions such as: What is the optimum level of dopants on either side of the junction? Where is the best location for the junction? What is the best shape for the top contact to the cell? How can optical losses from the cell be minimized?

Although answers to these questions will be provided specifically for silicon cells, parallel considerations will apply to cells made from other materials discussed in Chapter 10.

8.2 MAJOR CONSIDERATIONS

8.2.1 Collection Probability of Generated Carriers

A spatially dependent parameter, the *collection probability*, can be defined as the *probability a light-generated minority carrier*

has of contributing to the short-circuit current of a solar cell. This is a function of the position the carrier is generated within the cell. This parameter will be seen to be critical in determining the physical design of solar cells.

To find the collection probability, the artificial situation shown in Fig. 8.1(a) will be analyzed. Generation of electron-hole pairs by light will be assumed to occur only at points lying on a single plane throughout the cell. For the case where symmetry allows a "one-dimensional" analysis, the generation rate as a function of distance through the cell will be an impulse function, as indicated in Fig. 8.1(b).

The aim of the analysis will be to find the proportion of electrons generated at the point x_1 which contribute to the corresponding current flowing in the cell under short-circuit. During the analysis, it will be seen that no nonlinearities are involved and, by the superposition principle, the results can be applied to cases where the form of the generation rate corresponds more closely to practical situations. The analysis closely parallels that of Section 4.6.

In region 1 of Fig. 8.1(b), the generation rate is zero everywhere except at the single point x_1 right at the edge of the region. The differential equation that the excess minority carriers, Δn , must satisfy is therefore similar to Eq. (4.25):

$$\frac{d^2 \Delta n}{dx^2} = \frac{\Delta n}{L_e^2} \quad (8.1)$$

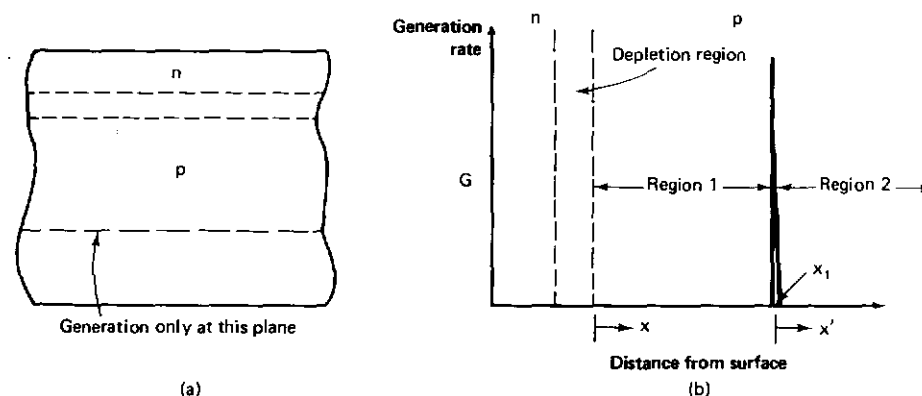


Figure 8.1. Idealized carrier-generation conditions used to calculate collection probabilities. An expression for the fraction of carriers generated at point x_1 which contribute to the cell short-circuit current is found in the text.

where L_e is the diffusion length. The general solution is, as before,

$$\Delta n = Ae^{x/L_e} + Be^{-x/L_e} \quad (8.2)$$

Boundary conditions are applied to assign values to the constants A and B . Under short-circuit conditions, the excess electron concentration at $x = 0$ is zero, since its value is determined by the voltage across the junction. Hence, $A = -B$ and

$$\Delta n = A(e^{x/L_e} - e^{-x/L_e}) = 2A \sinh\left(\frac{x}{L_e}\right) \quad (8.3)$$

Similarly, in region 2 of Fig. 8.1(b),

$$\Delta n = Ce^{x'/L_e} + De^{-x'/L_e}$$

where the origin of the x' direction is at the point x_1 . In this case, the excess concentration must be finite as x' becomes large. Hence, $C = 0$ and

$$\Delta n = De^{-x'/L_e} \quad (8.4)$$

At the position x_1 , the two solutions given by Eqs. (8.3) and (8.4) must match up since the electron concentration is continuous. Hence,

$$D = 2A \sinh\left(\frac{x_1}{L_e}\right) \quad (8.5)$$

On the n -type side of the device, the generation rate is zero throughout since the only generation occurs at x_1 . Also, the excess hole concentration Δp is zero at the edge of the depletion region when the cell is short-circuited. It follows that Δp is zero throughout this region. The resulting distributions of electrons and holes are shown in Fig. 8.2(a). Since minority carriers in uniformly doped quasi-neutral regions flow predominantly by diffusion (Section 4.5), minority-carrier current flows can be readily calculated by differentiating the foregoing distributions. The results are illustrated in Fig. 8.2(b).

The discontinuity in the electron current density at the point x_1 arises from the generation of carriers at this point. The size of the discontinuity is just the electronic charge multiplied by the rate of generation at this point. Assuming little change in currents across

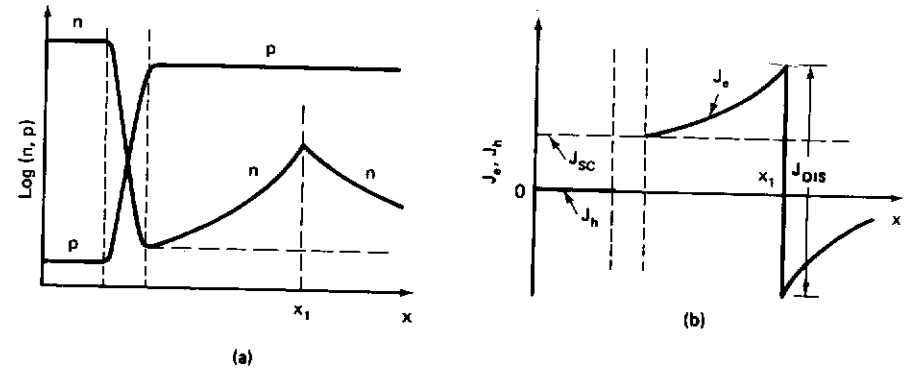


Figure 8.2. (a) Carrier distributions through the solar cell for the generation conditions of Fig. 8.1. (b) Corresponding minority carrier current distributions.

the depletion region (as previously discussed in Sections 4.6.2 and 5.4.3), the total current density in the device is equal to the electron current density at $x = 0$. The probability of collection (f_c) is just the ratio of the rate of flow of carriers in the external circuit to the rate of generation. Hence,

$$f_c = \frac{J_{sc}}{J_{dis}} \quad (8.6)$$

However, in the p -type region,

$$J_e = qD_e \frac{dn}{dx} \quad (8.7)$$

Hence, in region 1,

$$J_e = \frac{2qD_e A}{L_e} \cosh\left(\frac{x}{L_e}\right) \quad (8.8)$$

which gives, at $x = 0$,

$$J_{sc} = \frac{2qD_e A}{L_e} \quad (8.9)$$

J_{dis} can be found by evaluating the two expressions for current flow on either side of the discontinuity (J_{e-} and J_{e+}):

$$J_{e-} = \frac{2qD_eA}{L_e} \cosh\left(\frac{x_1}{L_e}\right) \quad (8.10)$$

$$J_{e+} = \frac{-qD_eD}{L_e} = \frac{-2qD_eA}{L_e} \sinh\left(\frac{x_1}{L_e}\right) \quad (8.11)$$

The latter equation follows from Eqs. (8.5) and (8.7). Hence,

$$\begin{aligned} J_{DIS} &= J_{e-} - J_{e+} \\ &= \frac{2qD_eA}{L_e} e^{x_1/L_e} \end{aligned} \quad (8.12)$$

It follows that

$$f_c = e^{-x_1/L_e} \quad (8.13)$$

The collection probability decreases exponentially with increasing distance of the point of generation away from the edge of the junction-depletion region. The characteristic decay length is just the minority carrier diffusion length. Since the foregoing analysis is linear, this conclusion is valid regardless of the distribution of the generation rate of carriers throughout the device.

A sketch of the probability of collection as a function of distance through a solar cell is shown in Fig. 8.3. As postulated earlier (Section 4.7), the depletion region and the region of the cell lying

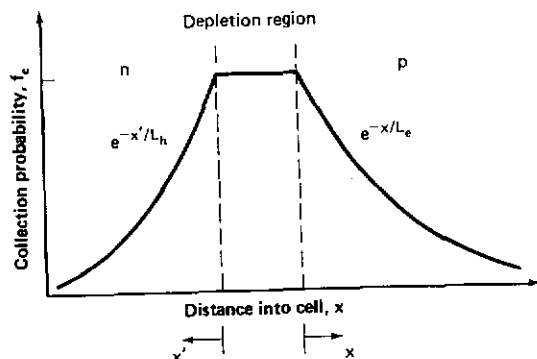


Figure 8.3. Calculated collection probability of generated minority carriers as a function of the point of generation in the solar cell.

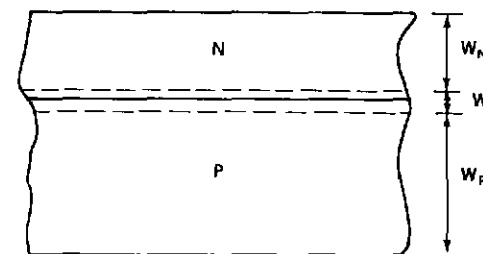


Figure 8.4. Critical dimensions in a cell of finite extent.

within a minority-carrier diffusion length of it are the regions where generated carriers have the highest chance of contributing to current flows (i.e., of being collected). A minority carrier generated outside these regions has an excellent chance of recombining before reaching the junction and subsequently the device terminals.

The foregoing analysis has assumed implicitly that both the *n*- and *p*-type regions extend much further than a diffusion length from the junction. For actual cells of finite extent as shown in Fig. 8.4, the collection probability will be modified. For example, if the surface on the *p*-type side of the device has a high recombination velocity, the expression corresponding to Eq. (8.13) is

$$f_c = \frac{\sinh[(W_P - x)/L_e]}{\sinh(W_P/L_e)} \quad (8.14)$$

If it has a low surface-recombination velocity, then

$$f_c = \frac{\cosh[(W_P - x)/L_e]}{\cosh(W_P/L_e)} \quad (8.15)$$

Both these approach the expression of Eq. (8.13) for $W_P \gg L_e$.

8.2.2 Junction Depth

Exposed surfaces such as between grid lines at the top of the solar cell are generally high-recombination-velocity surfaces. Interfaces between ohmic metal contacts and semiconductor are also generally regions of high recombination velocity. It has already been shown in Section 7.4 that one way of creating an effective low-recombination-velocity interface was by using a back surface field (i.e., by forming a junction between highly doped and lightly doped material of the same dopant type).

In view of the above and Eqs. (8.14) and (8.15), the collection probability of generated carriers as a function of distance from the surface of a p - n junction solar cell has the form shown in Fig. 8.5(a). Two features are important. A back surface field improves the probability of collection of carriers generated near the back contact and hence improves the short-circuit current of the cell. The probability of collection of carriers generated near the top surface of the solar cell is generally low.

Considering the actual generation rate of carriers in a semiconductor when illuminated by sunlight, the highest rate of generation will occur right at the semiconductor surface. For monochromatic light, the generation rate is given by

$$G = (1 - R) \alpha N e^{-\alpha x} \quad (8.16)$$

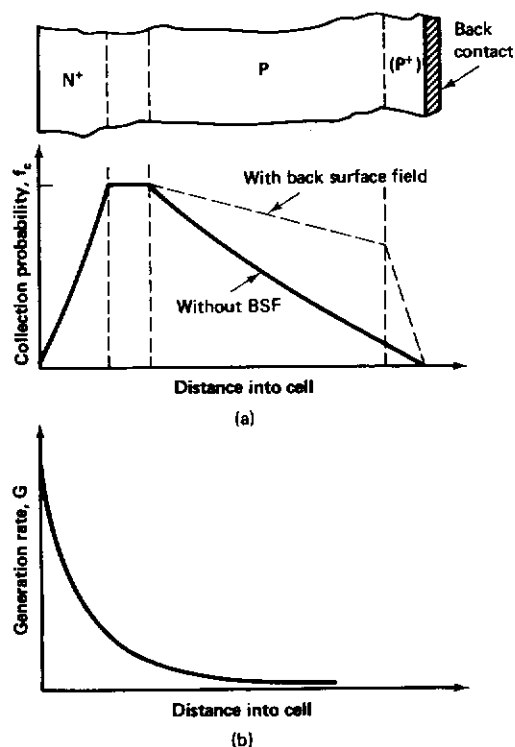


Figure 8.5. (a) Collection probability for a cell of finite extent with and without a back surface field. (b) Schematic diagram showing the generation rate of electron-hole pairs as a function of distance into the cell when illuminated by sunlight.

where x is the distance below the surface, α the absorption coefficient, N the incident photon flux, and R the fraction reflected. Under sunlight, the generation rate becomes

$$G(x) = \int_0^{\lambda_{\max}} [1 - R(\lambda)] \alpha(\lambda) N'(\lambda) e^{-\alpha(\lambda)x} d\lambda \quad (8.17)$$

where $N'(\lambda)$ is the incident flux per unit wavelength. The approximate form of this weighted exponential is shown in Fig. 8.5(b). The generation rate has a very strong peak near the surface precisely where the probability of collection is low. This deficiency obviously is minimized if the junction is as close to the surface as possible.

8.2.3 Lateral Resistance of Top Layer

Current flows in the bulk of the device are generally perpendicular to the surface of the cell as indicated in Fig. 8.6(a). To extract current via a contact that partially covers the top of the cell, current must flow laterally through the top layer of cell material. For a uniformly doped n -type layer, the resistivity of this layer is given by (Section 2.14)

$$\rho = \frac{1}{q\mu_e N_D} \quad (8.18)$$

A quantity more appropriate for describing the lateral resistance of this layer is the "sheet resistivity" (ρ_s), which is the resistivity divided by the layer thickness, t :

$$\rho_s = \frac{1}{q\mu_e N_D t} \quad (8.19)$$

For nonuniformly doped layers, the product $\mu_e N_D t$ is replaced by the integral $\int_0^t \mu_e(x) N_D(x) dx$. Sheet resistivities have the dimensions of ohms but are normally expressed as ohms/square ($\Omega/\square$).

The sheet resistivity determines the minimum spacing required between the grid lines of the top contact. Referring to Fig. 8.6(b), the resistive power loss due to lateral current flow is readily calculable. The incremental power loss in the section dy is given by

$$dP = I^2 dR \quad (8.20)$$

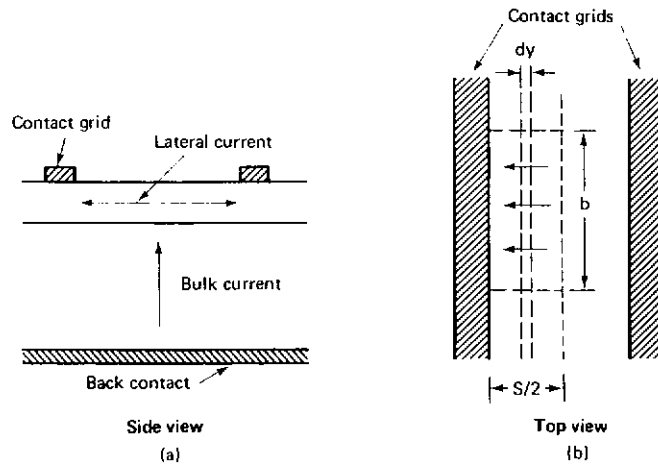


Figure 8.6. (a) Direction of current flow in different regions of a p - n junction solar cell. (b) Calculating power loss due to the lateral resistance of the top layer.

where dR is just $\rho_s dy/b$, and I , the lateral current flow, is zero at the midpoint between grating lines and increases linearly to its maximum at the grating line under uniform illumination. Hence,

$$I = Jby \quad (8.21)$$

where J is the current density in the device. The total power loss is the integral of the incremental losses:

$$P_{\text{loss}} = \int I^2 dR = \int_0^{S/2} \frac{J^2 b^2 y^2 \rho_s dy}{b} = \frac{J^2 b \rho_s S^3}{24} \quad (8.22)$$

At the maximum power point, the generated power from the region under consideration is $V_{\text{mp}} J_{\text{mp}} bS/2$. Hence, the fractional power loss at this point is

$$p = \frac{P_{\text{loss}}}{P_{\text{mp}}} = \frac{\rho_s S^2 J_{\text{mp}}}{12 V_{\text{mp}}} \quad (8.23)$$

This allows the minimum spacing S to be found for a given set of cell parameters. For example, for a typical commercial silicon cell, $\rho_s = 40 \Omega/\square$, $J_{\text{mp}} = 30 \text{ mA/cm}^2$, and $V_{\text{mp}} = 450 \text{ mV}$. For less

than 4% power loss due to lateral resistance effects,

$$S^2 < \frac{12 p V_{\text{mp}}}{\rho_s J_{\text{mp}}}$$

That is,

$$S < \left(\frac{12 \times 0.04 \times 0.45}{40 \times 0.03} \right)^{1/2} \text{ cm} < 4 \text{ mm} \quad (8.24)$$

This agrees with the grid spacings found on commercial silicon cells. Those with any larger spacing have a smaller sheet resistivity, and those with smaller spacing have a larger sheet resistivity. In practice, the major factor determining the sheet resistivity is the depth of the junction in Eq. (8.19). In fact, the resolution limits of the technology used to produce the grid pattern effectively sets the lower limit to the depth of the junction beneath the cell surface. To achieve minimum sheet resistivity of this layer, it is doped as high as practical.

8.3 DOPING OF THE SUBSTRATE

The substrate is uniformly doped during its preparation from molten material. The level of doping used is determined by the criteria which will now be discussed.

To get maximum I_{sc} once the junction depth is specified, the key parameter is the diffusion length in the substrate material. This is determined primarily by the minority-carrier lifetime in this region ($L_e = \sqrt{D_e \tau_e}$). In Section 3.4, three different recombination mechanisms were identified which determine the value of this quantity. For all of these, the general trend is a decrease in lifetime with increasing doping level. This is indicated in Fig. 8.7, which shows this dependency and the relative values of the lifetimes as caused by the different processes. For recombination by traps, the ideal expression for the variation of lifetime with doping follows from Eq. (3.22). It has the form

$$\tau_{nT} = \tau_{n0} \left(1 + \frac{m_1}{N_A} \right) \quad (8.25)$$

where m_1 is approximately equal to the larger of the parameters p_1 and $\tau_{p0} n_1 / \tau_{n0}$. Its value is determined by the energy and perhaps the

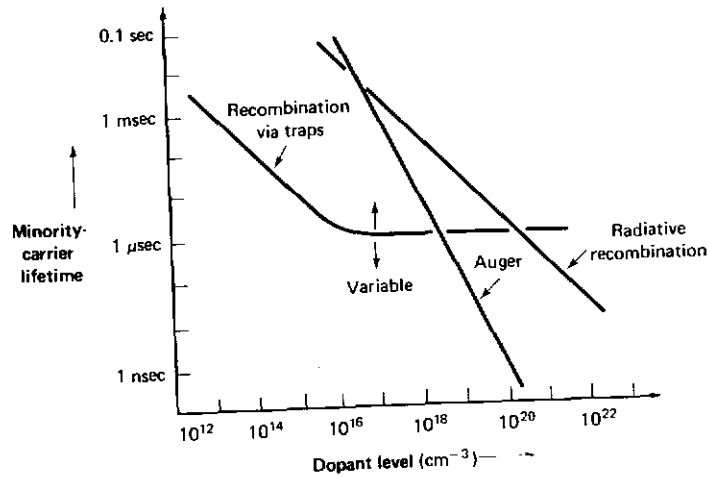


Figure 8.7. Relative magnitudes and dependence upon dopant density of minority-carrier lifetimes as determined by three competing processes for silicon.

capture cross sections of the dominant trap. For Auger recombination, the approximate expression at high doping levels is (Section 3.4.3)

$$\tau_{nA} = \frac{1}{DN_A^2} \quad (8.26)$$

while for radiative recombination (Section 3.4.2),

$$\tau_{nR} = \frac{1}{2BN_A} \quad (8.27)$$

The net recombination rate is given by

$$\frac{1}{\tau_n} = \frac{1}{\tau_{nT}} + \frac{1}{\tau_{nA}} + \frac{1}{\tau_{nR}} \quad (8.28)$$

As a consequence of the discussion above, it is concluded that increasing N_A will tend to decrease I_{sc} . Regarding the open-circuit voltage, the simple form of the expression for the saturation current density of a diode is given by Eq. (4.37)

$$I_0 = qA \left(\frac{D_e n_i^2}{L_e N_A} + \frac{D_h n_i^2}{L_h N_D} \right) \quad (8.29)$$

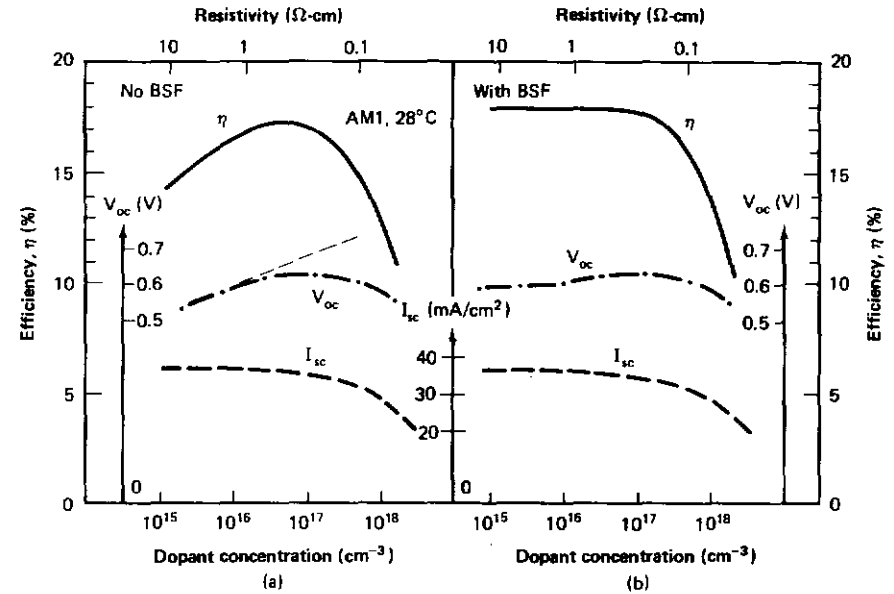


Figure 8.8. Dependence of key solar cell parameters upon the density of p -type dopants as obtained by high-performance experimental devices:

- (a) Without a back surface field.
- (b) With a back surface field.

The smaller I_0 , the larger V_{oc} . Hence, it would appear appropriate to make N_A and N_D as large as possible to obtain maximum V_{oc} . For a p -type substrate, the doping in the n -type diffused region (N_D) is made as large as possible to reduce the sheet resistivity. Hence, the second component in Eq. (8.29) is reasonably small, as discussed further in Section 8.6. It is concluded that V_{oc} will tend to increase with increasing N_A .

Because of the opposite dependencies of I_{sc} and V_{oc} upon N_A , it follows that there will be an optimum substrate doping level for maximum energy-conversion efficiency. This is in agreement with experimental results as indicated in Fig. 8.8(a). The results shown are indicative of experimental devices of good performance on substrates of different doping levels.

8.4 BACK SURFACE FIELDS

It has been mentioned that a highly doped region near the back contact will increase the short-circuit current and the open-circuit volt-

age. It improves the former by virtue of improved collection efficiency in the vicinity of the back contact, as indicated in Fig. 8.5. It improves the latter by virtue of a reduced saturation current (Section 4.9). The contribution to the saturation current from a p -type substrate with such a BSF takes the form

$$I_{0p} = \frac{qD_e n_i^2}{L_e N_A} \tanh\left(\frac{W_p}{L_e}\right) \quad (8.30)$$

Once the thickness of the p -type region is much less than a diffusion length ($W_p \ll L_e$), this equation reduces to

$$I_{0p} = \frac{qn_i^2 W_p}{\tau_e N_A} \quad (8.31)$$

With the increase of τ_e with decreasing N_A indicated in Fig. 8.7, this means that V_{oc} will not be dependent on resistivity for the higher resistivities. This differs from the case without a back surface field. Maximum efficiencies will occur at lower doping densities, provided that the series resistance of the substrate is not a problem.¹ This is indicated in Fig. 8.8(b), which shows results corresponding to Fig. 8.8(a) when a back surface field is present.

8.5 TOP-LAYER LIMITATIONS

8.5.1 Dead Layers

In Section 8.3, it was shown that high effective recombination velocities at the top surface of the cell lead to an optimal design where the top diffused layer of the cell is made as thin as possible consistent with obtaining reasonable sheet resistivities. In cells developed in the 1960s for space use, junction depths beneath the surface were typically about 0.5 μm . As much phosphorus dopant as

¹ For high resistivities, minority carrier concentrations are likely to be comparable to majority carrier concentrations during cell operation. This not only complicates the calculation of series resistance but invalidates the analysis on which the expressions of this section are based. An expression for the dark current in this case of comparable simplicity to that implied by Eq. (8.31) is (Ref. 8.1):

$$I = \frac{qn_i W_p}{(\tau_e + \tau_h)} (e^{qV/2kT} - 1)$$

possible was diffused into this thickness to keep the sheet resistivity low. This created undesirable side effects.

From simple theoretical considerations (Ref. 8.2), a Gaussian or similar distribution of phosphorus is expected within the silicon after the high-temperature diffusion step from what is essentially an infinite source of phosphorus. Figure 8.9(a) is a sketch of the distribution of electrically active phosphorus, as typically measured after different diffusion times at fixed diffusion temperature. It clearly shows an upper limit to the amount of electrically active phosphorus. This limit equals the solid solubility of phosphorus in silicon at the diffusion temperature. Phosphorus in excess of this would be expected to be incorporated into phosphorus-rich precipitates. In regions of such excess phosphorus, minority-carrier lifetimes are dramatically reduced.

In a solar cell, regions of excess phosphorus would lie near the surface of the cell. This can produce a "dead layer" near the surface where light-generated carriers have very little chance of being collected because of the very low minority-carrier lifetimes. The collection probability corresponding to this situation is shown in Fig. 8.9(b). When this problem was clearly identified (Ref. 8.3), substantial modifications in the cell design were made to produce a high efficiency cell known as the "violet" cell. Much shallower junctions were used ($\sim 0.2 \mu\text{m}$) and the surface concentration of phosphorus was kept below the solid solubility limit, eliminating dead layers. This also reduced the sheet resistivity of the diffused layer, making it essential to use much closer spacing of the grid lines of the top contact.

8.5.2 High-Doping Effects

In the heavily doped top region of the cell, minority-carrier lifetimes would be expected to be low on several accounts. From Fig. 8.7, Auger recombination would result in low maximum values for lifetimes in this region. Additionally, the possibility of precipitates and defects in the crystal structure created by the high-temperature diffusion process would increase the number of centers for recombination via trapping levels. This would decrease lifetimes below the Auger limit.

Another effect of importance in heavily doped regions is the effective narrowing of the forbidden band gap of the semiconductor (Ref. 8.4). This will have a major influence on the effective value of the intrinsic concentration, n_i .

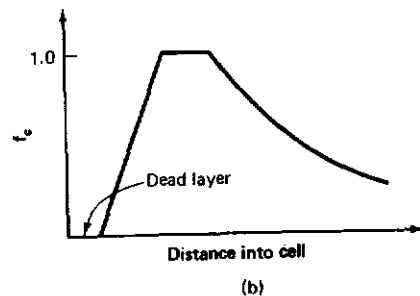
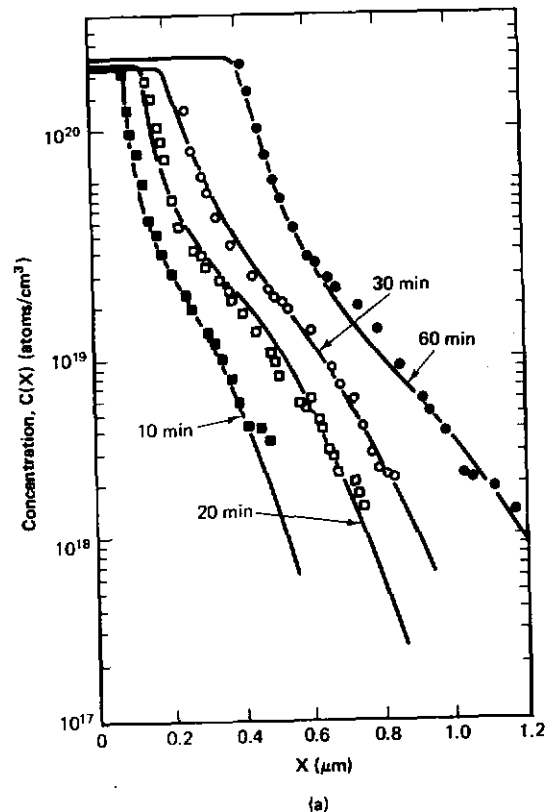


Figure 8.9. (a) Profile of electrically active phosphorus introduced into silicon for different diffusion times at fixed diffusion temperature. [After J. C. Tsai, *Proceedings of the IEEE* 57 (1969), p. 1499, © 1969 IEEE.] (b) Collection probability as a function of distance into the cell for a diffused cell with a dead layer.

8.5.3 Contribution to Saturation Current Density

In Sections 8.3 and 8.4, contributions to the saturation current density, I_0 , of the solar cell arising from the properties of the bulk region were discussed. The heavily doped top layer can also contribute significantly to this parameter.

Some general comments about the desirable properties of the top layer to minimize this contribution can be made. For example, recombination in this region and its associated surface has to be kept to a minimum. However, because of the multiplicity of effects that have to be taken into account in heavily doped regions, it is not straightforward to calculate how this is best accomplished from theoretical considerations. Experimentally, for diffused silicon cells, the minimum contribution to the saturation current density from this layer lies in the range of 1 to 3×10^{-12} A/cm². Ion-implanted top layers appear to be capable of giving slightly lower values (Ref. 8.5).

Regardless of how the substrate properties are chosen to minimize the substrate contribution to the saturation current density, the top-layer contribution will provide an upper limit to the maximum open-circuit voltage that a silicon cell of the type described can attain. This limit is in the range 600 to 630 mV at standard test conditions. The effect of this limit can be seen by referring to Fig. 8.8(a) and (b). It does not allow the full photovoltaic potential of the substrate material to be utilized. Alternative cell designs are described in Chapter 9 which overcome this limitation.

8.6 TOP-CONTACT DESIGN

One important area of cell design is the design of the top metal contact grid. This area becomes increasingly important as the size of individual cells increases. Figure 8.10 shows some of the diverse approaches to top contact design which have been used in terrestrial cells.

There are several power-loss mechanisms associated with the top contact. The loss due to lateral current flow in the top diffused layer of the cell has already been described. Additionally, there are losses due to the series resistance of the metal lines and the contact resistance between these lines and the semiconductor. Finally, there are the losses due to the shadowing of the cell by these lines.

In this section, the design of contacts for square or rectangular cells will be considered. Parallel techniques can be used for cells

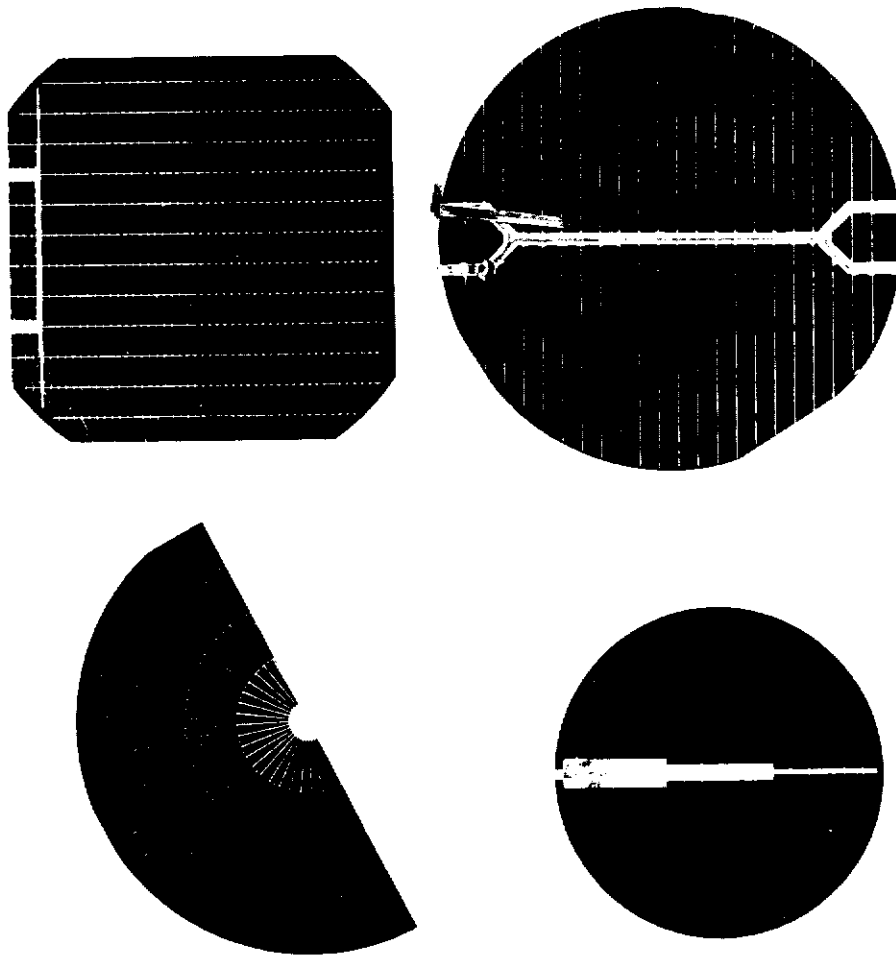


Figure 8.10. Collection of production silicon solar cells, showing diverse approaches to the design of the top contact to the cell.

of more general shape. For common contact designs, two types of metallic elements can be identified as indicated in Fig. 8.11(a). *Bus-bars* are relatively heavy areas of metallization directly connected to the external leads to the cell; *fingers* are finer elements which collect current for delivery to a busbar. As shown in Fig. 8.10, there can be more than one level of fingers in some cell designs. Fingers and bus-bars are usually either of constant width, linearly tapered, or have step changes in width.

A symmetrical contacting scheme such as in Fig. 8.11(a) can be broken down into unit cells as in Fig. 8.11(b). The maximum power output of this unit cell can be seen to be given by $ABJ_{mp}V_{mp}$, where AB is the area of the unit cell. J_{mp} and V_{mp} are the current density and voltage, respectively, at the maximum power point. The resistive losses in the fingers and busbars can be calculated using the integral approach as used to calculate the power loss in the top layer of the cell in Section 8.2.3. Normalized to the maximum output of the unit cell, the results are (Ref. 8.6)

$$p_{rf} = \frac{1}{m} B^2 \rho_{smf} \frac{J_{mp}}{V_{mp}} \frac{S}{W_F} \quad (8.32)$$

$$p_{rb} = \frac{1}{m} A^2 B \rho_{smb} \frac{J_{mp}}{V_{mp}} \frac{1}{W_B} \quad (8.33)$$

for the fractional resistive power loss in the fingers and busbars, respectively. ρ_{smf} and ρ_{smb} are the sheet resistivities of the contact metal layers for the fingers and busbars. In some cases these will be identical, whereas in others such as solder-dipped cells, where a thicker layer builds up over the wider busbar, ρ_{smb} will be smaller. The value of m is 4 if the respective element is linearly tapered and 3 if of uniform width. W_F and W_B are the average width of the fingers or busbar lying within the unit cell, and S is the pitch of the fingers as indicated in Fig. 8.11(b).

The fractional power losses due to shadowing by the fingers and busbar are

$$p_{sf} = \frac{W_F}{S} \quad (8.34)$$

$$p_{sb} = \frac{W_B}{B} \quad (8.35)$$

Neglecting current flows directly from the semiconductor to the busbar, the contact resistance loss is due solely to the fingers. The fractional power loss due to this effect is, as a general approximation

$$p_{cf} = \rho_c \frac{J_{mp}}{V_{mp}} \frac{S}{W_F} \quad (8.36)$$

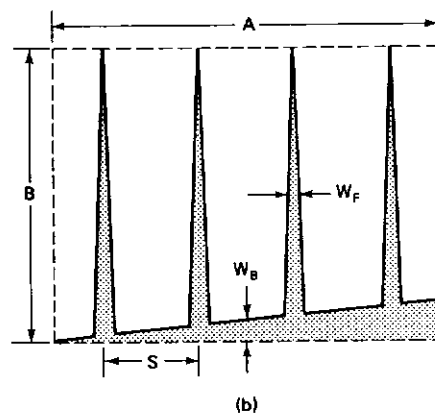
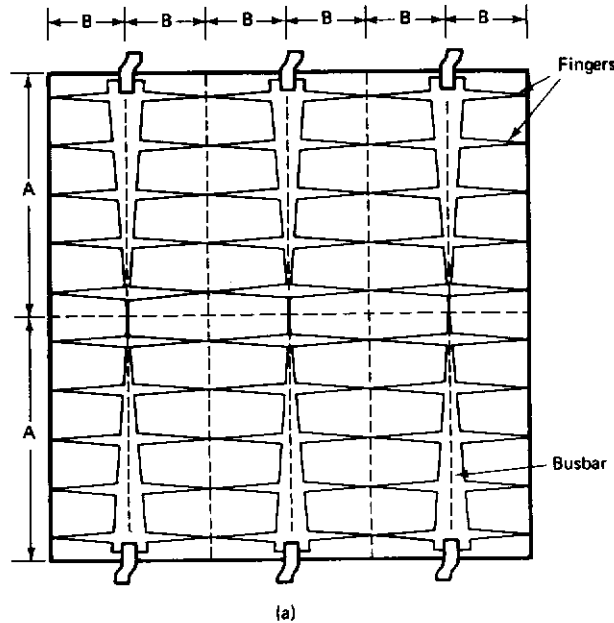


Figure 8.11. (a) Schematic of a top contact design showing busbars and fingers. Also shown is the symmetry in this particular design whereby the contact can be broken down into 12 identical unit cells. (b) Important dimensions of a typical unit cell.

where ρ_c is the specific contact resistance. Contact resistance losses are not generally an important consideration for silicon cells under one sun operation. The remaining loss is that due to the lateral current flow in the top layer of the cell. In normalized form, this is given by Eq. (8.23)

$$p_{tl} = \frac{\rho_s}{12} \frac{J_{mp}}{V_{mp}} S^2 \quad (8.37)$$

where ρ_s is the sheet resistivity of this layer.

The optimum dimensions of the busbar can be found by summing Eqs. (8.33) and (8.35) and differentiation with respect to W_B to find its optimum value (Ref. 8.6). The result is that the optimum occurs when W_B is such that the resistive loss in the busbar equals its shadowing loss. This occurs when

$$W_B = AB \sqrt{\frac{\rho_{smb}}{m} \frac{J_{mp}}{V_{mp}}} \quad (8.38)$$

with the minimum value of fractional power loss given by

$$(p_{rb} + p_{sb})_{min} = 2A \sqrt{\frac{\rho_{smb}}{m} \frac{J_{mp}}{V_{mp}}} \quad (8.39)$$

This indicates that power losses are about 13% lower when a tapered busbar ($m = 4$) is used rather than a busbar of constant width ($m = 3$).

The design of the lowest level² of finger metallization is more complex, because this also determines the lateral loss in the top region of the cell and the contact resistance losses in the cell. Mathematically, the optimum occurs when the spacing between the fingers becomes very small to make the lateral loss negligible. The optimum is then given by the conditions

$$S \rightarrow 0 \quad (8.40)$$

$$\frac{W_F}{S} = B \sqrt{\frac{\rho_{smf} + \rho_c m / B^2}{m} \frac{J_{mp}}{V_{mp}}} \quad (8.41)$$

²If there is more than one level of finger metallization, the optimum dimensions of the higher levels can be found by regarding them as the busbars for the next lowest level. Note that in this case there will be a different unit cell for each level of metallization.

$$(p_{rf} + p_{cf} + p_{sf} + p_{tl})_{\min} = 2B \sqrt{\frac{\rho_{smf} + \rho_c m/B^2}{m}} \frac{J_{mp}}{V_{mp}} \quad (8.42)$$

In practice, it will not be possible to obtain this optimum performance. Each of the technologies for forming the top contacts previously discussed will place its own limit on how small W_F and hence S can be while still maintaining acceptable yields in a production environment.

In this case the optimum finger design can be realized by a simple iterative process. Regarding the finger width W_F as fixed at some minimum value by technological limitations, the optimum value of S corresponding to this can be found by successive approximations. At some trial value of S' , the corresponding fractional power losses p_{rf} , p_{cf} , p_{sf} , and p_{tl} are calculated. A better approximation to the optimum value can then be calculated as³

$$S'' = \frac{S'(3p_{sf} - p_{rf} - p_{cf})}{2(p_{sf} + p_{tl})} \quad (8.43)$$

This process will quickly converge to a constant value corresponding to the optimum. A starting trial value for the optimum can be found by noting that the value of S calculated from Eq. (8.41) will be an overestimate. A value equal to half this should result in a stable iteration sequence.

The approach, as described above, will allow selection of the optimum dimensions of busbar and fingers once the gross features of a particular contact design have been specified. These gross features might be dictated by considerations other than optimized top-contact design such as the ease with which cells can be automatically interconnected. As a rule of thumb, the smaller the unit cell, the smaller the top-contact loss. Redundant contacts not only improve module reliability but also reduce top-contact losses by reducing the size of unit cells. If the sheet resistivity of the busbar is less than that of the fingers, it is best to use a design with long busbars and short fingers, as in the figure immediately preceding the Preface at the front of this book, provided that contact-resistance effects are small. In the case shown, the current-carrying section of the busbars

³This equation can be derived by differentiating the expression for the power loss ($p_{rf} + p_{cf} + p_{sf} + p_{tl}$) with respect to S . This derivative must equal zero for the optimum value of S . This optimum S is then found using the Newton iteration scheme (Ref. 8.7) for finding the roots of a nonlinear equation.

are the metal interconnect ribbons which extend the whole length of the cell. Even for rectangular cells, it may be worthwhile considering contact schemes other than the rectilinear ones discussed. For example, radial contact schemes such as illustrated in Fig. 8.12 can also give very low overall losses for rectangular cells.

It should be noted in passing that the equations described in this section are based on certain approximations (Ref. 8.8) regarding the size of the normalized power losses, the magnitude of resistive voltage drops, and the direction of current flow, particularly near intersections of fingers and busbars. Also, linear tapers may not be the optimum shape for busbars or fingers for differently shaped cells (Ref. 8.9). The effect of these second-order effects may be well worth checking for situations, such as in concentrating cells, where contact design is critical.

Problem: Design the top contact for a 10×10 cm silicon solar cell. This cell gives its maximum power output at a voltage of 450 mV and a current density of about 30 mA/cm². The sheet resistivity of the diffused layer in this cell is 40 $\Omega/\square$.

Two interconnections per cell are specified. The metallization is to be applied by plating and subsequent solder dipping. The finger width is specified as 150 μm . The sheet resistivity of the metallization is determined primarily by the solder layer, whose bulk resistivity is 15 $\mu\Omega\text{-cm}$. The solder builds up to an average thickness of 42 μm over the fingers and 80 μm over the wider busbars. The specific contact resistance between the fingers and the semiconductor is 370 $\mu\Omega\text{-cm}^2$.

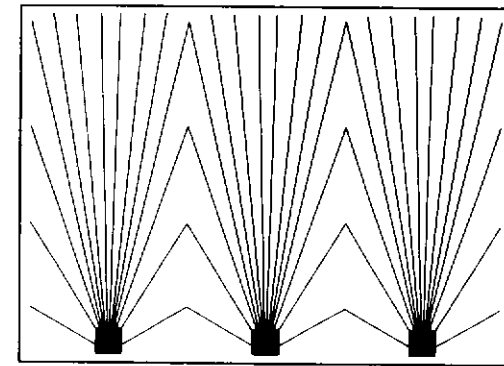


Figure 8.12. Radial contact metallization scheme for a rectangular cell.

Solution: In the terminology of this section,

$$J_{mp} = 0.03 \text{ A/cm}^2 \quad V_{mp} = 0.45 \text{ V}$$

$$\rho_s = 40 \Omega/\square \quad \rho_c = 370 \mu\Omega\text{-cm}^2$$

$$\text{Sheet resistivity of solder layers} = \frac{\text{bulk resistivity}}{\text{layer thickness}}$$

Therefore,

$$\rho_{smf} = 0.00357 \Omega/\square \quad \rho_{smb} = 0.00188 \Omega/\square$$

Since $\rho_{smb} < \rho_{smf}$, a contact design with long busbars and short fingers is preferable. One suitable for two interconnections per cell is shown in Fig. 8.13. This breaks down into four unit cells, each with $A = 10 \text{ cm}$, $B = 2.5 \text{ cm}$.

The optimized dimensions of the busbar can be calculated from Eq. (8.38). Using a tapered busbar ($m = 4$), its optimum width per unit cell is

$$W_B = 10 \times 2.5 \left(\frac{0.00188 \times 0.03}{4 \times 0.45} \right) \text{ cm} = 0.14 \text{ cm}$$

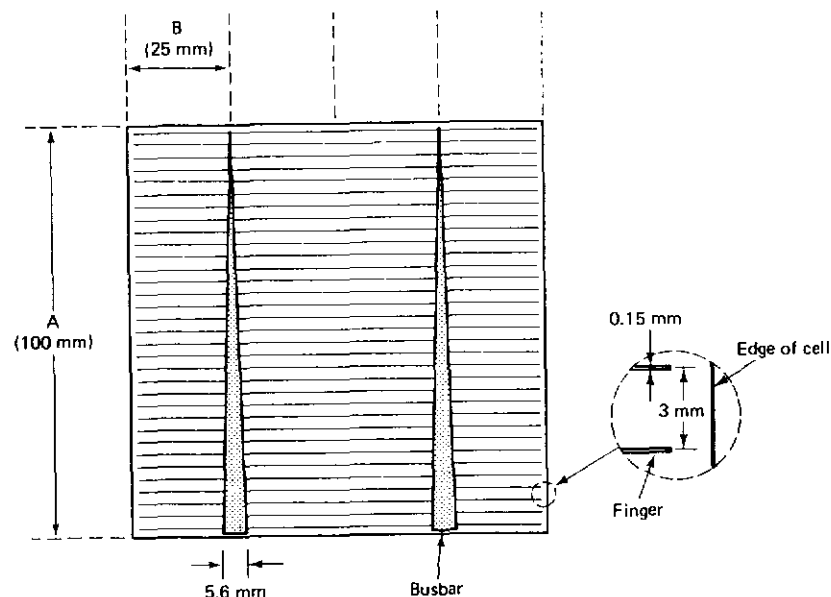


Figure 8.13. Contact scheme chosen for the design example. The shadowing loss is 10.6% and resistive losses in the contact and the diffused layer of the cell total 8.6%.

Since the actual busbar lies in two unit cells, the average busbar width is twice this. Hence, the busbar tapers from the thinnest value possible to a maximum width of 0.56 cm. The corresponding fractional power loss is, from Eq. (8.39),

$$p_{rb} + p_{sb} = 0.112$$

The finger width is specified as $150 \mu\text{m}$ ($W_F = 0.015 \text{ cm}$). Assume that this is a result of technical limitations and the finger cannot be made any finer. With this constraint, a constant width ($m = 3$) finger will not be far below optimum. The optimum finger spacing S has to be found iteratively. A starting trial value is found by dividing the value given by Eq. (8.41) by 2. This gives

$$S = 0.3286 \text{ cm} \quad p_{rf} = 0.0109 \quad p_{cf} = 0.0005$$

$$p_{sf} = 0.0456 \quad p_{tl} = 0.0240$$

Substituting these values into Eq. (8.43) gives the improved trial solution:

$$S = 0.2962 \text{ cm} \quad p_{rf} = 0.0098 \quad p_{cf} = 0.0005$$

$$p_{sf} = 0.0506 \quad p_{tl} = 0.0195$$

Continuing this for another iteration gives

$$S = 0.2991 \text{ cm} \quad p_{rf} = 0.0099 \quad p_{cf} = 0.0005$$

$$p_{sf} = 0.0502 \quad p_{tl} = 0.0199$$

Further iteration does not change the value of S , indicating that an optimum has been reached. The total fractional power loss due to the fingers and the top layer resistance is 0.080. The combined losses in the cell for this contact design is then 19.2% of the intrinsic output. The complete contact design is specified in Fig. 8.13.

8.7 OPTICAL DESIGN

8.7.1 Antireflection Coating

The principle of a quarter-wavelength antireflection coating is illustrated in Fig. 8.14. Light reflected from the second interface arrives back at the first interface 180° out of phase with that reflected from the first interface, canceling it out to some extent.

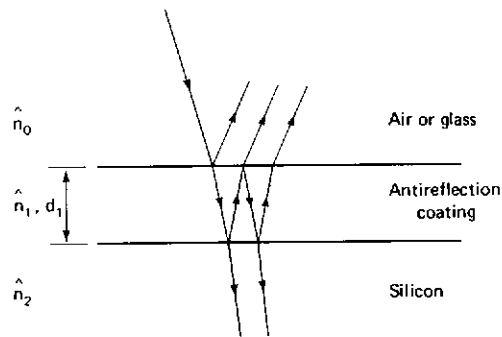


Figure 8.14. Interference effects created by a quarter-wavelength antireflection coating.

The expression for the fraction of the energy in a normally incident beam of light reflected from the surface of a material covered by a transparent layer of thickness d_1 is (Ref. 8.10)

$$R = \frac{r_1^2 + r_2^2 + 2r_1r_2 \cos 2\theta}{1 + r_1^2r_2^2 + 2r_1r_2 \cos 2\theta} \quad (8.44)$$

where r_1 and r_2 are given by

$$r_1 = \frac{n_0 - n_1}{n_0 + n_1} \quad r_2 = \frac{n_1 - n_2}{n_1 + n_2} \quad (8.45)$$

where the n_i represent the refractive indices of the different layers. θ is given by

$$\theta = \frac{2\pi n_1 d_1}{\lambda} \quad (8.46)$$

When $n_1 d_1 = \lambda_0/4$, the reflectance has its minimum value:

$$R_{\min} = \left(\frac{n_1^2 - n_0 n_2}{n_1^2 + n_0 n_2} \right)^2 \quad (8.47)$$

This is zero if the refractive index of the antireflection (AR) coating is the geometric mean of those of the materials on either side ($n_1^2 = n_0 n_2$). For a silicon cell in air ($n_{si} \approx 3.8$), the optimum refractive index is the square root of that of silicon (i.e., $n_{opt} \approx 1.9$). Figure 8.15

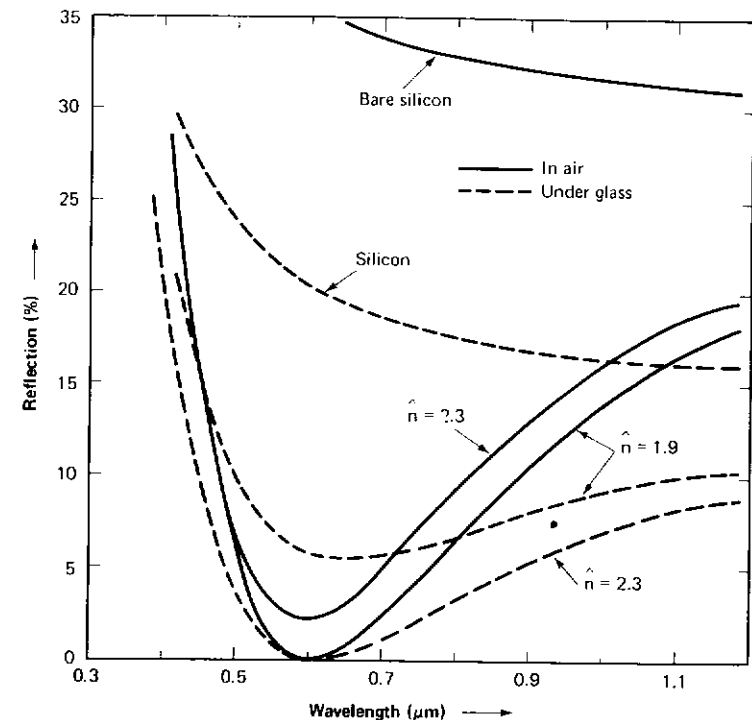


Figure 8.15. Percentage of normally incident light reflected from bare silicon and silicon with antireflection coatings of refractive indices of 1.9 and 2.3 as a function of wavelength. The thicknesses of the latter coatings are chosen to produce minimum reflection at 600 nm. The dashed lines show the effect of encapsulating the silicon under glass or material of a similar refractive index.

includes a curve showing the percentage of incident light reflected from silicon as a function of wavelength for an antireflection coating of this refractive index designed to produce minimum reflection at 600 nm. The weighted average of usable sunlight reflected from silicon can be kept to 10% as opposed to over 30% for bare silicon.

Cells are normally encapsulated under glass or embedded in a material of a similar refractive index to glass ($n_0 \sim 1.5$). This increases the optimum value of the index of the AR coating to about 2.3. Reflection from a cell with an AR coating of this refractive index is also shown in Fig. 8.15, both before and after encapsulation. The refractive index of a range of materials used in commercial solar cells is listed in Table 8.1. Apart from having the correct refractive index, the AR material must be transparent. It is usually deposited

Table 8.1. REFRACTIVE INDICES OF MATERIALS
USED IN SINGLE- OR MULTIPLE-LAYER
ANTIREFLECTION COATINGS

Material	Refractive index
MgF ₂	1.3-1.4
SiO ₂	1.4-1.5
Al ₂ O ₃	1.8-1.9
SiO	1.8-1.9
Si ₃ N ₄	~1.9
TiO ₂	~2.3
Ta ₂ O ₅	2.1-2.3
ZnS	2.3-2.4

as a noncrystalline or amorphous layer which prevents problems with light scattering at grain boundaries. Layers formed by vacuum evaporation generally tend to be absorbing at UV wavelengths. However, layers formed by such techniques as oxidizing or anodizing a deposited metal layer or layers deposited chemically tend to have a "vitreous" structure (amorphous with short-range order) which reduces this UV absorption (Ref. 8.11).

The use of multiple layers of AR coating materials can improve performance. The design of such coatings is more complex, but it is possible to reduce reflection over a broader band (Ref. 8.11). At least one manufacturer uses a two-layer coating in high efficiency cells to reduce the reflection of usable sunlight to 4%.

8.7.2 Textured Surfaces

Another approach previously mentioned to reduce reflection is to use textured surfaces. These are produced by etching the silicon surface with an etch that etches silicon much more rapidly in one direction through the crystal structure than another. This exposes certain planes within the crystal. The pyramids apparent in Fig. 7.6 are formed by the intersection of these crystal planes. In terms of Miller indices (Section 2.2), the silicon surface for textured cells is normally aligned parallel to a (100) plane and the pyramids are formed by the intersection of (111) planes. Dilute caustic soda (NaOH) solutions are a commonly used selective etch.

The angles of the pyramids are defined by the orientations of the crystal planes. These are such that incident light has at least two chances of being coupled into the cell. If 33% is reflected at each point of incidence, as is the case for normal incidence on bare silicon,

the total reflected overall is 0.33×0.33 , about 11%. If an antireflection coating is used, reflection of sunlight can be kept well below 3%. Even without an antireflection coating, the reflection when embedded in a material of refractive index similar to glass is only about 4%. Another desirable feature is that light is coupled into the silicon at an angle which ensures that it will be absorbed closer to the surface of the cell. This will increase the probability of its collection, particularly for the more weakly absorbed long wavelengths.

There are some disadvantages associated with the use of textured surfaces. One is that more care is required in handling (Ref. 8.12). A second is that such surfaces are much more effective in coupling light of all wavelengths into the cell, including unwanted infrared radiation of insufficient photon energy to create electron-hole pairs. This tends to make the cells "run hotter." Finally, top contact metallization has to run up and down the sides of the pyramids. If the height of the metal layer is less than or comparable to that of the pyramids ($\sim 10 \mu\text{m}$), it follows that two to three times the metal must be used to maintain the same resistive loss as on a flat surface.

8.8 SPECTRAL RESPONSE

The spectral response of a cell was mentioned in Section 5.5. It is the output current under short-circuit per unit incident power in monochromatic light as a function of wavelength. Measurement of the spectral response can provide detailed information about the design parameters of any particular solar cell.

Monochromatic light causes electron-hole pairs to be generated in the semiconductor with a spatial distribution given by

$$G = (1 - R) \alpha N e^{-\alpha x} \quad (8.48)$$

where N is the incident photon flux, R the fraction reflected, and α the absorption coefficient. For short wavelengths (UV light), α is large and light is absorbed quickly upon entering the semiconductor, as indicated in Fig. 8.16(a). Normal solar cells are not very effective at collecting light generated near the surface. If a quantum collection efficiency η_Q is defined as the number of electrons flowing in the external short-circuiting lead per incident photon in the monochromatic light, it will be very low for such UV light, as shown in Fig. 8.16(b). At intermediate wavelengths, α is smaller in value and a large proportion of the generated carriers are generated in regions where the collection probability is high. η_Q therefore increases.

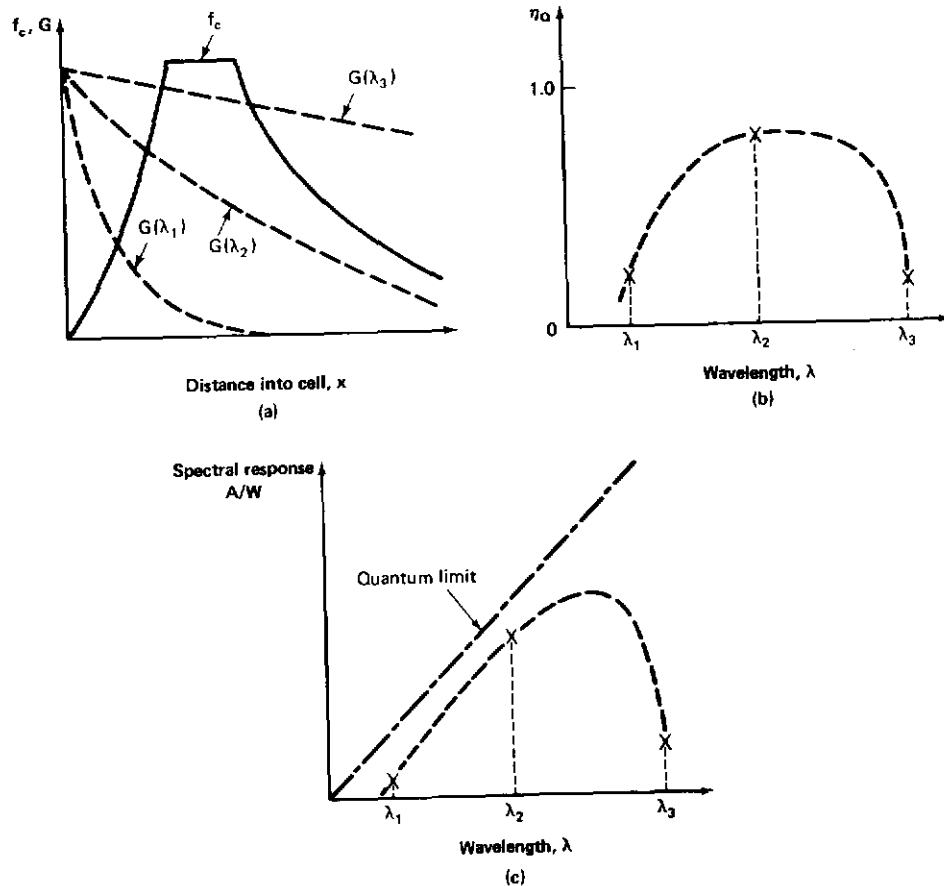


Figure 8.16. (a) Collection probability for a representative solar cell and, shown by the dashed lines, the carrier generation profiles for three different wavelengths of light. (b) Corresponding quantum collection efficiency, η_Q , as a function of wavelength. (c) Corresponding spectral sensitivity (A/W), also as a function of wavelength.

Long-wavelength light is absorbed very weakly and only a small proportion is absorbed in the active region of the cell. η_Q therefore decreases, dropping to zero once the photons have insufficient energy to create electron-hole pairs.

Another way of showing the spectral response apart from the quantum yield curve of Fig. 8.16(b) is to plot the sensitivity in A/W as a function of wavelength, as shown in Fig. 8.16(c). The quantum

limit is also indicated. At short wavelengths, the cells cannot utilize all the energy in the photons, so the sensitivity is low, even if operating ideally.

For "conventional" cells (referring to the type of cell developed for use in space), the response at short wavelengths is poor due to the deep junction employed augmented by the absorption in the AR coating. At long wavelengths, the spectral response is determined by the diffusion length in the cell material. The violet cell was a shallow junction cell developed in the early 1970s. The design emphasis was on achieving good collection at UV wavelengths by using the shallower junction and an improved, less absorbing AR coating. Textured cells demonstrate improved sensitivity to light at all wavelengths due to reduced reflection.

A back surface field (BSF) increases the collection probability for carriers generated near the back contact and hence boosts the long-wavelength sensitivity. The back contact to the cell can be designed to be reflective to give the longer wavelengths a second chance at being absorbed. Such back surface reflectors (BSR) can give quite a boost to the performance of thin cells, as well as helping to maintain low operating temperatures.

8.9 SUMMARY

The design of silicon junction solar cells has evolved from the following considerations. The p - n junction has to lie close to the surface of the cell to give maximum current output. This can lead to problems due to the lateral resistance of this layer unless it is doped as high as practical. Excessive doping of this layer introduces effects that cause its electronic properties to be less than optimal.

The optimum substrate resistivity for a solar cell depends on whether a back surface field is present. If absent, the optimum resistivity is quite clearly defined at dopant levels in the range 10^{16} to 10^{17} cm^{-3} . If present, the optimum becomes less dependent on resistivity and is displaced to lower dopant levels.

In the design of the top contact to the cell, the critical parameters determining the associated power loss are the contact layout, the sheet resistivities of the contact metal layer and the diffused top layer of the cell, and the minimum width line permissible with the technology used to define the contact geometry. A quarter-wavelength antireflection coating can increase the output current of a solar cell by 35 to 45%. Texturing the cell surface can produce even better performance, although there are some associated disadvantages.

EXERCISES

- 8.1. A particular silicon solar cell consists of a very thin, uniformly doped n -type layer on a p -type substrate. The surface recombination velocity along the surface of the n -type layer is very large. Assuming that minority-carrier diffusion lengths in the n -type layer are very large compared to the thickness of this layer, derive an expression for the probability of collection of minority carriers as a function of distance generated away from the surface in the n -type layer. (Note: Since the diffusion length is very large compared to the thickness of the n -type region, recombination in bulk of this region will be small and can be neglected compared to the rate of surface recombination.)
- 8.2. Calculate the sheet resistivity of the n -type layer in Exercise 8.1 given that the dopant concentration is 10^{18} cm^{-3} and the thickness of the layer is $0.5 \mu\text{m}$.
- 8.3. Silicon solar cells of conventional structure are fabricated on p -type wafers $150 \mu\text{m}$ thick. Cells with a high recombination back contact give a short-circuit current of 2.1 A and an open-circuit voltage of 560 mV . Similar cells with a back surface field give a short-circuit current of 2.2 A . Given that the minority carrier diffusion length in the p -type region after processing in all cases is $500 \mu\text{m}$, what would be the ideal value of the open-circuit voltage for the cells with a back surface field?
- 8.4. Design the top contact for a rectangular silicon solar cell $7.5 \times 10 \text{ cm}$ in size and calculate the total power loss of your design. The sheet resistivity of the diffused layer in this cell is nominally $60 \Omega/\square$. The cell gives its maximum power at a voltage of 430 mV and a current density of 28 mA/cm^2 under bright sunshine. Three interconnections per cell are specified, all lying along the same side of the cell.
The metallization is to be applied by vacuum evaporation through a metal shadow mask. The minimum line width is specified as $180 \mu\text{m}$. The metallization consists of a layer of titanium ($0.12 \mu\text{m}$) adjacent to the silicon separated by a thin layer of palladium ($0.02 \mu\text{m}$) from a $4\text{-}\mu\text{m}$ -thick layer of silver. The specific contact resistance to the silicon is $200 \mu\Omega\text{-cm}^2$. The bulk resistivities of these metals are 48, 11, and $1.6 \mu\Omega\text{-cm}$, respectively.
- 8.5. Consider a cell of given top contact geometry with metallization and cell parameters fixed. Show that the relative power loss attributable to this top contact increases as the cell dimensions increase.

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