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Polysilicon emitters for silicon concentrator solar cells

Gan, Jon-Yiew, Ph.D.

Stanford University, 1990

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POLYSILICON EMITTERS FOR SILICON CONCENTRATOR SOLAR CELLS

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING
AND THE COMMITTEE ON GRADUATE STUDIES
OF STANFORD UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

By
Jon-Yiew Gan
July 1990

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Abstract

Recently, a single-crystal silicon point-contact solar cell has been shown to have energy conversion efficiency of 28% at 100 suns. Such a cell has been fully analyzed; and it appears that the cell efficiency can be increased more than one absolute percentage by eliminating the emitter recombination. In order to do this, the emitter saturation current density (J_o), which characterizes the dopant-diffused region recombination, of both n- and p- type emitters has to be kept around 2×10^{-14} A/cm^2. Unfortunately, such low J_o cannot be obtained by the diffused emitters formed in the single-crystal silicon. Polysilicon emitters, n-type in particular, have been reported to have very low J_o ($\sim 1 \times 10^{-14}$ A/cm^2); therefore, they can be a very useful substitute for the diffused emitters for high efficiency solar cells. Nevertheless, some problems in the polysilicon emitter itself have to be resolved before they can be used in silicon concentrator solar cells. One is the high contact resistance. For the polysilicon emitter to have low J_o, a thin interfacial oxide has to be placed in between the polysilicon and the substrate. However, such an interfacial oxide also causes high contact resistance ($\rho_c \geq 1 \times 10^{-4}$ Ω-cm^2). Another is the high J_o of the p-type polysilicon emitter. Prior to this work, the lowest J_o of the p-type polysilicon emitter reported was $\sim 3 \times 10^{-13}$ A/cm^2 which is high for a solar cell application. The other is the complexity of the oxide breakup during a high temperature anneal, which appears to increase the J_o of the polysilicon emitter. In this work, both the minority and the majority carrier transport of the polysilicon emitter are closely examined. Theoretically, a model was proposed to make the polysilicon emitter with both low J_o ($\sim 3 \times 10^{-14}$ A/cm^2) and low contact resistance ($\rho_c \leq 1 \times 10^{-5}$ Ω-cm^2). Experimentally, such polysilicon emitters for both types were successfully demonstrated.

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I am sincerely grateful for the help, support, and encouragement of many people around me throughout this work.

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It is a great pleasure to have been in this group. Since the day I joined, all of my group members have been unfailingly helpful. Wendell Eades was the first to teach me "ultraclean" processing and properties of the Si/SiO_2 interface, both which have been very useful for this work. Then, Young Kwark taught me the processing technique for bipolar devices, which laid the foundation for this work. And, Stan Swirhun's perfect mask-design for contact devices has made the measurement a lot easier. Special thanks to Ron Sinton, who helped me on everything: device modeling, experiments, and jobs. Frequent discussions with Dave Kane are also very helpful for understanding the device physics as well as the details of measurements. Richard King's "couldn't-be-better" program for photoconductivity decay measurement has been appreciated by everyone, and was vastly used in this work. The collaboration with Peter Gruenbaum on the polysilicon passivation was surely a wonderful experience although it is not included in this thesis. The work with Andrés Cuevas on ammonium-hydroxide anisotropic etching is also an interesting issue. Dick Crane has been very helpful to me. He measured the solar cell characteristics for me at his most inconvenient time. Valuable advice from Sharleen Beckwith on wafer-processing will never fade from my memory.

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Chapter 1

Introduction

1.1 Motivation

Recently, silicon concentrator solar cells have been demonstrated to have energy conversion efficiency as high as 28% [1]. The structure of such a cell is shown in Figure 1.1, along with the cell efficiency versus the incident power density. Several features of this cell are distinctive from the "conventional" cell. First of all, both types of contacts are made on the backside. By making all contacts on the backside, the trade-off between the shadowing effect and the series resistance caused by narrow grid lines is essentially eliminated. This enables the cell to operate at higher concentrations of light so that the cell can be more cost-effective. In addition, the front surface of the cell is texturized such that the light absorption is dramatically enhanced. Typically, such a texturized cell has responsivity of 0.415 A/watt compared with 0.35 A/watt of an untexturized cell [1]. Finally, the contacts cover only a small areal fraction of the backside surface. The main reason of making small contacts is to reduce the recombination in the diffusion regions even though such a design sacrifices the current-collection capability.

The dopant diffusions in the cell are used to separate the carriers via the diffusion potential formed at the junction; they collect majority carriers (electrons for n-type) and repel minority carriers (holes for n-type). Such a function is similar to that of the emitter in a bipolar transistor; therefore, the diffusion region is usually

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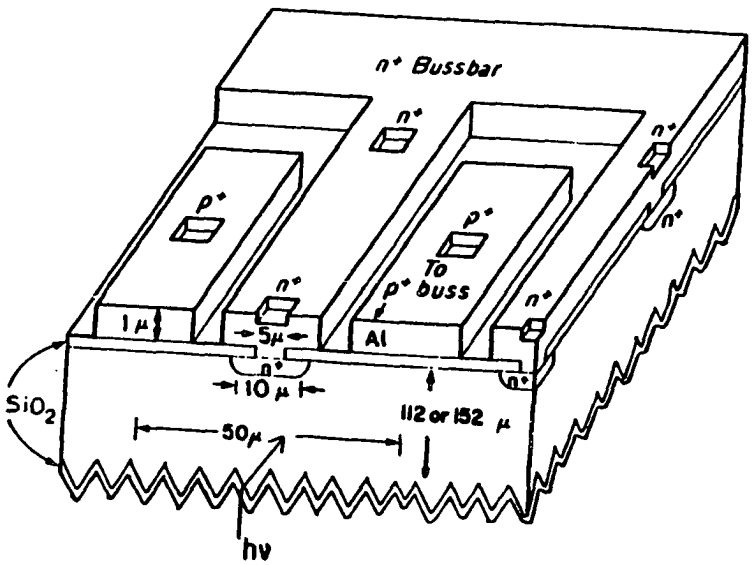

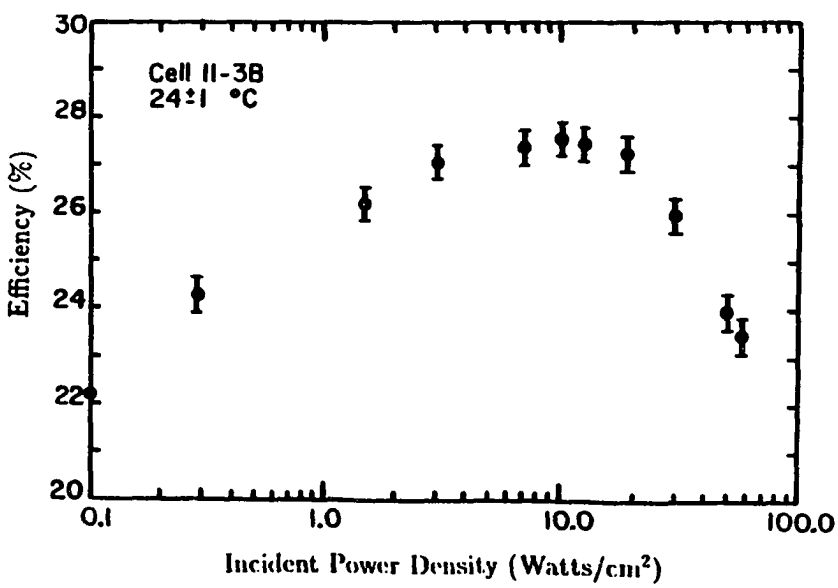

Figure 1.1: The structure and performance of a backside point-contact solar cell; (a)a cross section of a region in the solar cell near one of the Al busbars, (b)the efficiency versus incident power density.

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referred to as the emitter, and the rest of bulk as the base region. When the cell is under illumination, increased recombination in the emitter takes place because the increase of the excess charge carriers in the base region effectively lowers the junction potential. Similarly to the base current of a bipolar transistor, this recombination can be characterized by the emitter saturation current density, J_o. In the point contact solar cell, the diffused region, as its name implies, is formed by introducing a high density of dopants under the contacts (see Figure 1.1). The J_o of both p^+ and n^+ diffused regions is around 4.5×10^{-13} A/cm^2 which is so high that it can degrade the cell performance significantly if these diffusion regions cover the whole backside of the cell. This can be seen from the plot of the cell efficiency versus the total emitter saturation current density which is given in Figure 1.2 for an interdigitated backside contact cell. In the figure, the cell efficiency is plotted at two different incident power densities; at 36 watts/cm^2, which is the design point for this backside contact cell, and at 10 watts/cm^2, which gives the highest efficiency (28%) measured from a backside point-contact solar cell. The parameters used in the simulation are the same as those used to simulate the 28% backside point contact cell [2]. The cell efficiency, as shown in the figure, is hardly affected by the emitter recombination when J_o is below 1×10^{-14} A/cm^2; however, it falls off rapidly as the J_o increases over 1×10^{-14} A/cm^2. If we allow the emitters to cover the entire backside surface, then the total J_o is 4.5×10^{-13} A/cm^2, and the cell efficiency will be limited to about 27% at the incident power density of 10 watts/cm^2. In contrast, the efficiency of the point contact cell is increased to 28% by scaling the emitter areal-coverage fraction to 20% such that the total J_o of the cell is effectively reduced to about 1×10^{-13} A/cm^2.

Nevertheless, the cell efficiency loss due to the emitter recombination is still significant in the point-contact cell. One indicator of this evidence is that there is one absolute percentage difference of cell efficiency when the current result is compared with the simulation results (29.3% in Figure 1.2 for 10 watts/cm^2). To show this is the case, the internal quantum efficiency loss due to various recombination mechanisms of the cell is plotted as a function of the incident-power-density in Figure 1.3 [2]. Typically, there are four main recombination mechanisms in the cell as shown

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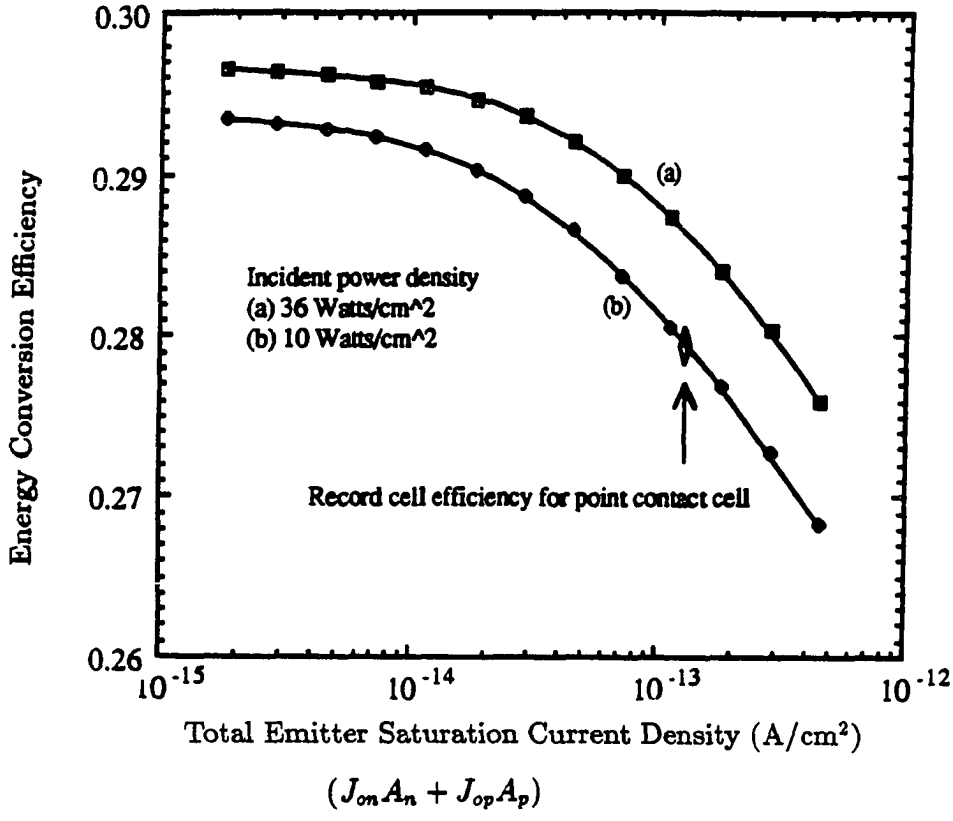

Figure 1.2: The cell efficiency versus the total emitter saturation current density of an inter-digited backside contact cell.

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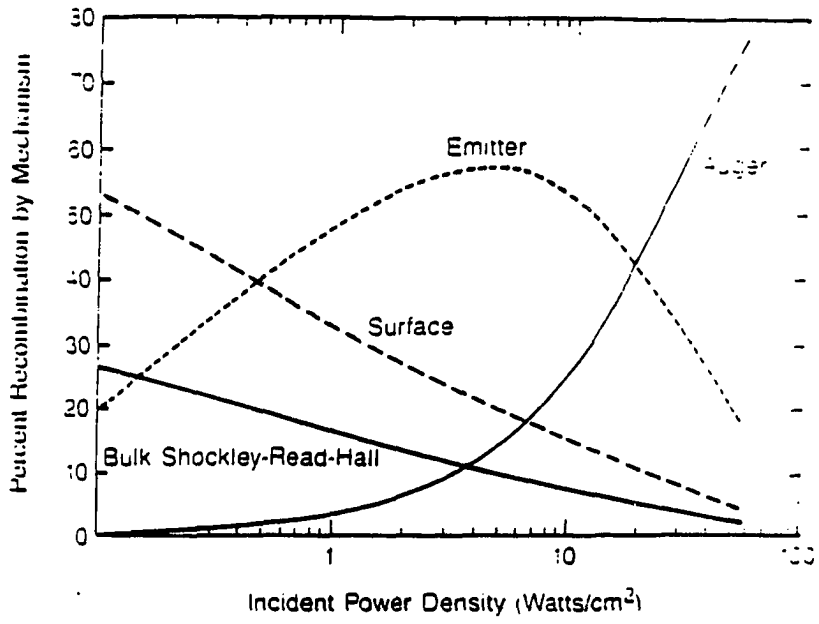

Figure 1.3: The percentage of recombination by mechanism at the maximum power point for a solar cell as a function of the incident power density.

in the figure. Because each recombination mechanism has a different dependence on the carrier density, which in turn is a function of the incident power density, the dominant recombination mechanisms vary with the incident power density. For the incident power density in the span from 0.6 to 20 watts/cm^2, the efficiency loss is primarily due to the emitter recombination. Such an incident power-density range spans the geometric concentration from 6 to 200 suns for AM1.5 sunlight in which most silicon concentrator solar cells are designed to operate. Note that the emitter recombination has been effectively reduced by a factor of 5 in the figure; yet, it prevails over the other sources of recombination.

At first sight, it is tempting to think that the emitter recombination loss can be further reduced with even smaller emitter areal coverage fraction. In doing so, however, we are running into another problem—high internal series resistance. By reducing the emitter areal coverage fraction, we are sacrificing the capability of the emitter to collect the majority carrier flow. Evidently, the power loss caused by the high series resistance will overwhelm the gain from reducing the emitter

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recombination when the emitter areal coverage fraction is smaller than the optimum value. In fact, the emitter areal coverage fraction of a high-performance point-contact cell has been fairly close to the optimum value. Any further improvement via this method is limited [2]. This points out that the only way to resolve the emitter recombination completely is to use a substitute material, which has very low J_o when it contacts to the silicon, to replace the diffused emitters.

An ideal emitter for silicon should have a wide band gap such that an additional potential barrier will appear in the minority band when it is doped. To illustrate this point, a simplified band diagram of a p^+-i-n^+ diode is given in Figure 1.4 [3]. At the junction, the band is bent in such a way that majority carriers are facing a downhill potential and free to flow into the emitter; however, minority carriers are excluded from the emitter by an extra potential barrier due to the band discontinuity. Although the minority carriers are blocked by the additional potential barrier, they still can recombine at the interface; therefore, for an ideal emitter, it also requires the recombination at the interface between the silicon and the emitter to be negligible. Unfortunately, there is no such material known to be ideal for silicon. Most of them are subject to high recombination at the interface; therefore, J_o appears even higher than that of a diffused emitter [4]. There are only two materials which were reported to have very low J_o; one is the semi-insulating polysilicon emitter (SIPOS) [5]-[7], the other is the polysilicon-contacted emitter [7]-[11]. SIPOS is formed by introducing oxygen during the silicon deposition, and is a mixture of silicon and silicon oxide microstructurally [7],[12]-[16]. The mechanism for polysilicon and SIPOS to have low J_o is likely the same since their J_o depend critically on the interfacial structure [3,7].

1.2 Approach and Outline

The reason that the n-type polysilicon emitter can have very low J_o is primarily due to a very thin oxide sandwiched between the polysilicon and the substrate. It has been known that there is always a very thin oxide formed on the silicon surface prior to the silicon deposition [3,7,10,11], [17]-[22]. Depending on the predeposition

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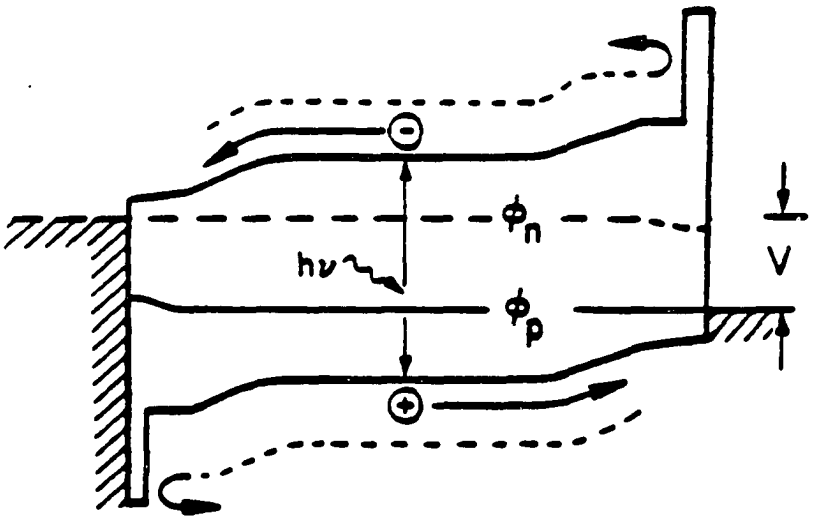

Figure 1.4: The band diagram for a p^+-i-n^+ diode with selective emitter contacts.

cleaning process, the oxide thickness varies from 8 to 15 Å which is enough to create a potential barrier to impede the carrier transport. In particular, it has been reported by several authors [7,10] that the J_o for an n-type polysilicon emitter with an interfacial oxide of 15 Å thick can be as low as 1×10^{-14} A/cm^2.

One important characteristic of such a thin oxide is that it tends to break up during a high temperature anneal. In the broken regions, there is no oxide and polysilicon tends to realign with the monosilicon underneath [10,19,20]. When the oxide loses its integrity, J_o increases accordingly because more minority carriers can enter the polysilicon and recombine there [7,10,21,22]. To distinguish these two cases, we refer to the one with an intact interfacial oxide as polysilicon SIS emitter and the other as "pure" polysilicon emitter for which J_o is dominated by the recombination inside the polysilicon. It is clear that we are interested only in the polysilicon SIS emitter because it is the one that can offer lower J_o.

Although the J_o of the n-type polysilicon SIS emitter can be made very low, it is still not useful for concentrator solar cells unless the following two problems can be resolved. One is the high contact resistance imposed by the interfacial oxide. Because of the wide band gap of the oxide, it is likely that the majority carrier

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transport will be hampered by a similar potential barrier to that for the minority carrier. The same situation also occurs in the MIS solar cell which, because of high contact resistance [23,24], can be operated only at very low incident power density. Unless the contact resistance can be lowered effectively, such an emitter would be useless for concentrator solar cells.

The other problem is that the J_o of the p-type polysilicon SIS emitter has never been made as low as that of n-type. To date, the lowest J_o of p-type polysilicon SIS emitter is around 3×10^{-13} A/cm^2 [7] which is about one order of magnitude higher than that of n-type. In solar cell applications, p-type emitters are as important as n-type in terms of the recombination loss. Since the hole mobility is about three times smaller than that of n-type, any scaling on p-type coverage fraction will induce a rapid increase of series resistance and the advantage of using polysilicon SIS emitter diminishes.

The fact that the interfacial oxide will break during high temperature anneals has been utilized in making very low-contact-resistance polysilicon emitters which in turn are the essential part of the high speed silicon bipolar transistor [22]. Because low emitter resistance is very much needed for a high speed bipolar device, the process is usually designed to break the interfacial oxide as much as possible. Nevertheless, it is interesting to see how much the interfacial oxide has to be broken in order to have low enough contact resistance. Contact resistance is usually expressed in terms of the specific contact resistivity, ρ_c, which is independent of the contact area and has units of Ω-cm^2. Consider that a thin conducting layer with known resistivity and thickness is placed between two electrodes, then the additional potential drop caused by the current flow through the conducting layer is

$$\Delta V = I \times \frac{\rho t}{A} = J \times (t\,\rho) = J \times \rho_c;$$

Where I and J are the the current and current density flowing through the conducting layer, t is the thickness of the conducting layer, A is the contact area, and ρ is the resistivity of the conducting layer. Note that the ρ_c can be derived if the resistivity and thickness of the conducting film are known. A similar approach can be used to estimate the ρ_c of a broken interfacial oxide.

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Assuming that the interfacial oxide is broken uniformly across the entire emitter contact, and the resistivity across the interfacial oxide at each broken spot is the same as that of the bulk. Under such a condition, we can estimate the specific contact resistivity by assuming that the current only flows through those broken spots. Suppose that the total broken area fraction is 1%, and the resistivity of a polysilicon emitter is 5 mΩ-cm, so the specific contact resistivity is

$$\begin{aligned}\rho_c &= \frac{\text{resistivity} \times \text{oxide thickness}}{\text{the broken areal fraction}} \\ &= (5 \times 10^{-3} \times 15 \times 10^{-8})/(0.01) \\ &= 7.5 \times 10^{-8}\ (\Omega\text{-cm}^2);\end{aligned}$$

where 15 Å oxide thickness is assumed. The broken areal fraction accounts for the increase of the current density at the broken spots. The result indicates that by breaking 1% the interfacial oxide, the ρ_c is already too low to be noticeable in most device applications. For silicon concentrator solar cells, the current density at the emitter front is typically less than 100 A/cm^2; therefore, the potential drop across the interfacial oxide would be negligible with such a low specific contact resistivity. An addition "spreading resistance" will occur as the current converge into the broken regions. this will be discussed further in Sec. 4.3.

Such a small fraction of broken oxide can also be a great advantage in preserving the low emitter saturation current density. For example, with 1% of broken areal fraction, the J_o will be effectively reduced by a factor of 100 from that of the pure polysilicon emitter if the recombination in the other areas is assumed to be negligible. Normally, the J_o of an n-type pure polysilicon emitter is 1×10^{-12} A/cm^2 [21], so the effective J_o will be 1×10^{-14} A/cm^2, ideal for solar cells (see Figure 1.2). In addition, it also offers a way to improve the p-type polysilicon emitter. The high J_o of the p-type polysilicon emitter has to do with the interfacial oxide. One of the possibilities is that the interfacial oxide may break more rapidly with the presence of boron in the high temperature anneal so that it becomes a "pure" polysilicon emitter which has high J_o. The other possibility is that boron degrades the oxide interface such that high recombination at the oxide interface leads to high J_o like the other heterojunction systems to the silicon. In either case, low J_o seems possible

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if the interaction between the interfacial oxide and boron can be suppressed to a minimum level. Above all, obtaining small broken areal fraction of the interfacial oxide seems to be a very promising method for making polysilicon emitters of both types useful for concentrator solar cells, and is the approach of this work.

To carry out the task, the cell modeling is given in the next chapter. This serves two purposes in this work. First, it gives an idea how the cell performance is related to the emitter and its design. Second, The requirements for a good emitter substitute can also be sought from the simulation. Chapter 3 starts a thorough review of the work done on the polysilicon emitter. In particular, the review will point out all the problems of the polysilicon emitter for use in silicon concentrator solar cells. Chapter 4 is dedicated to the derivations of carrier transport mechanisms for the polysilicon SIS emitters. In particular, it shows that, under certain conditions, a polysilicon SIS emitter with low J_o and ρ_c can be obtained by breaking a very small fraction of interfacial oxide. Chapter 5 is the demonstration of the experimental results. The results shown in this chapter are very much like what are predicted in Chapter 4. In practice, there are some technical problems in controlling the oxide breakup process. They are discussed in Chapter 6 for the polysilicon emitter with low J_o and ρ_c. In the final chapter, a summary of contributions of this study and suggestions for future work are given.

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Chapter 2

Solar Cell Modeling

2.1 Introduction

The cell modeling serves two purposes in this work. First, it gives an idea how the cell performance is related to the emitter and its design. Second, the requirements for a good emitter substitute can also be sought from the simulation.

Theoretically, the ultimate cell efficiency is limited by the laws of thermodynamics [25,26]. However, the cell performance of a silicon solar cell, before reaching such a limit, suffers from non-ideal light absorption and all sorts of recombination taking place inside the cell. Since the absorption coefficient of silicon for most of the solar spectrum is not sufficiently large, a significant amount of incident light may escape before the actual absorption takes place. This is demonstrated by the the difference of the photo-responsivity between a texturized and a non-texturized cell, which has been mentioned in the beginning of the previous chapter. More detailed discussions of the light trapping can also be found in Ref. [27,28].

The other main limitation of a practical cell is the recombination of the photo-generated electron-hole pairs before they are collected separately. As will be shown, the output voltage and current of the solar cell are related. Consequently, high recombination hurts the cell performance in two ways; reducing the output voltage and current simultaneously. Typically, the loss of the photo-current density, J_{rec},

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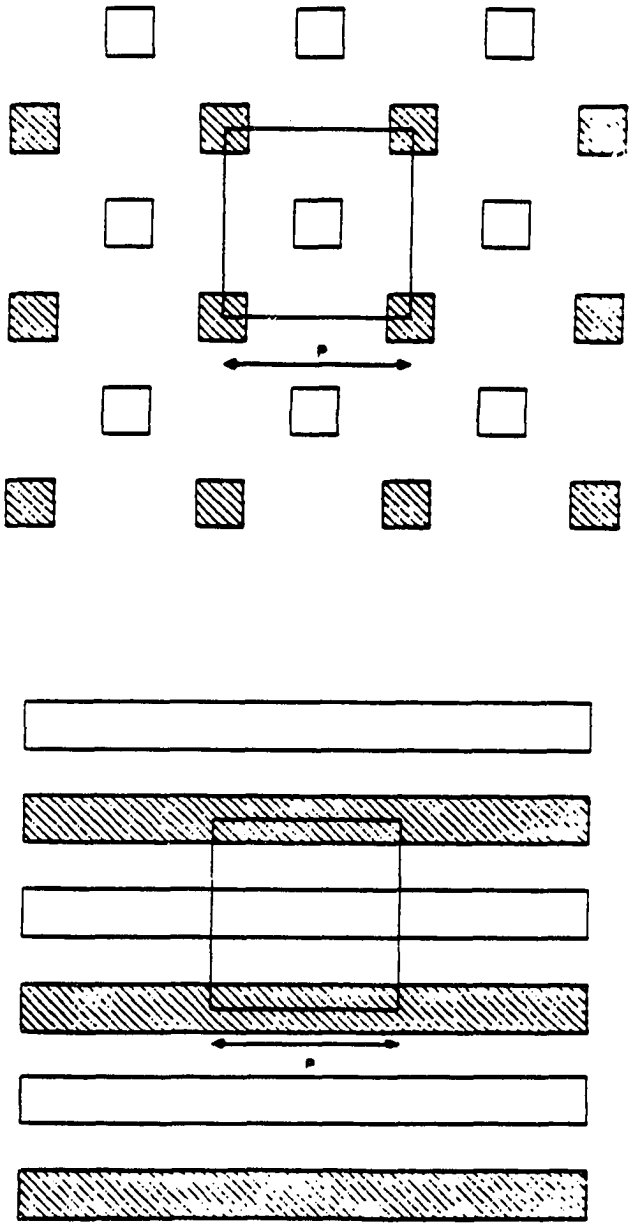

Figure 2.1: The emitter configuration of (a) a BPC cell, and (b) an IBC cell. In both (a) and (b), the square enclosed by dot lines is the unit cell used in the simulation.

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can be expressed as the following equation, assuming the base is in the high-level-injection regime,

$$J_{rec} = \frac{q}{\tau}\int n(x)dx + qS\int ndA + J_{op}A_p\left(\frac{n_{op}}{n_i}\right)^2 + J_{on}A_n\left(\frac{n_{on}}{n_i}\right)^2 + qC_a\int n^3(x)dx. \tag{2.1}$$

The first term in the equation represents the bulk Shockley-Read-Hall recombination, and τ is the lifetime that characterizes the recombination rate via this mechanism. The second term is the recombination at the passivated surface which is typically assumed to be linearly proportional to the carrier density at the surface through the constant S, the surface recombination velocity. The third and the fourth term are the emitter recombination of p- and n- type emitters respectively. They are characterized by the emitter areal coverage fraction A_p and A_n, and the emitter saturation current density J_{op} and J_{on}. Assume that the carrier density in front of the emitter is equal ($n_{op} = n_{on}$), the total emitter saturation current density mentioned in the previous chapter (also in Figure 1.2) is the sum of the A_pJ_{op} and the A_nJ_{on}. The last term is the Auger recombination.

Because of the higher order dependence of the carrier density, the last three terms are conceivably dominant under high concentrated light. The Auger recombination of a high quality silicon wafer has been demonstrated by Sinton [29] to be intrinsic and can be suppressed only by reducing the cell thickness, which in turn has to be compromised with the light absorption. As pointed out in the first chapter, it is the emitter recombination that most concerns this work. Consequently, the modeling presented in this chapter assumes the best results of the other terms and concentrates on the effect of the emitter on the cell performance.

For a back-side contact cell, two emitter geometries are investigated. One is the back-side point-contact (BPC) cell of which the contact is a square dot; the other is the inter-digited back-side contact (IBC) cell of which the contact is a line. The configurations of emitters of both cells are shown in Figure 2.1 (p. 12). Since the emitter pattern is a periodic array in both cells, the actual computation is done on one unit cell as shown in Figure 2.1, and is expected to be the same as that using the entire cell.

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Because the emitter recombination is the main concern for a cell with conventional diffused emitters, the design rule is to seek the smallest possible emitter areal coverage fraction while the resulting internal series resistance is negligible. As a result, this usually leads to the choice of the BPC cell structure over the IBC cell structure because of the better current-collection capability of the BPC cell. However, as the emitter recombination becomes negligible, the optimized emitter areal coverage fraction is expected to increase in order to reduce the internal series resistance further. Under such condition, the IBC cell is more appropriate than the BPC cell because a larger emitter areal coverage fraction can be obtained from an IBC cell.

The modeling of both cell structures is outlined in the next section. The simulation results are then discussed in Section 2.3. In Section 2.4, we conclude our discussion and post the requirements for the emitter to be used in the silicon concentrator solar cell.

2.2 The Outline of the Cell Modeling

The cell modeling on a BPC cell has been reported by Swanson and Sinton [2,26,30]. Since the difference between a BPC and an IBC cell is only the emitter geometry, the modeling for a IBC cell can follow its counterpart's procedures with only a few modifications. In this section we outline their approaches for a BPC cell, and present modified equations for an IBC cell occasionally. In addition, it should be noted that the modeling applies only for cells for which the base is in the high-level-injection regime. However, this should not be a problem for most solar cells made from a high resistivity ($\geq$ 100 Ω-cm) silicon wafer. The assumption of high-level-injection is appropriate even when such cell is operated under one sun.

The goal of the modeling is to find the cell output characteristics, the terminal voltage and current density, in terms of the incident power density and the known properties of silicon. The terminal voltage and current density can be expressed as

$$V = \frac{kT}{q} \ln \left(\frac{n_{on} n_{op}}{n_i^2} \right) - V_{res}, \tag{2.2}$$

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and

$$J = J_{ph} - J_{rec}. \tag{2.3}$$

In the equations, J_{rec} has been expressed explicitly in Eqn. (2.1); n_{on} and n_{op} also have the same meaning as those in that equation. V_{res} is the potential drop across the p- and n- type contact caused by the internal series resistance. It turns out that, when the cell is operated in the high-level-injection regime, every term in Eqn. (2.2) and (2.3) is a function of the carrier distribution inside the cell. Consequently, finding the carrier distribution is equivalent to having the problem solved.

One shortcut is used in finding the carrier distribution inside the cell. A back-side contact cell, according to the dominant carrier transport mechanism, can be roughly divided into three regions, as shown in Figure 2.2; the diffusion, the stagnant, and the collection region. Those regions are divided by the demarcation labeled r_1, the collection radius. From the top to r_1 is the diffusion region where electrons and holes are assumed to travel in the same direction—to the backside of the cell. Because of charge neutrality, both types of carriers diffuse at the same speed, and the electric current flowing in this region can be ignored. In the collection region, which is defined by the semi-circle (or hemi-sphere) around the emitter, carriers are collected selectively; electrons are mainly collected by the n-type contact, and holes by the p-type contact. As a result, this region is dominated by the majority carrier transport, and accounts for V_{res} in Eqn. (2.2). In the stagnant region, the carrier density is assumed to be constant. This implies that the potential drop in this region is negligible. This is a good approximation because the spacing between n- and p- type contact is relatively narrow, and a high conductivity results from high carrier density in this region.

The shortcut of this process is that an analytic form of the demarcation (r_1 shown in Figure 2.2) among those regions can be found [26]. The form is presented in the following equation

$$r_1 = \frac{P \times D_A}{\sqrt{8\pi}} \sqrt{\frac{1}{D_p^2} + \frac{1}{D_n^2}} \tag{2.4}$$

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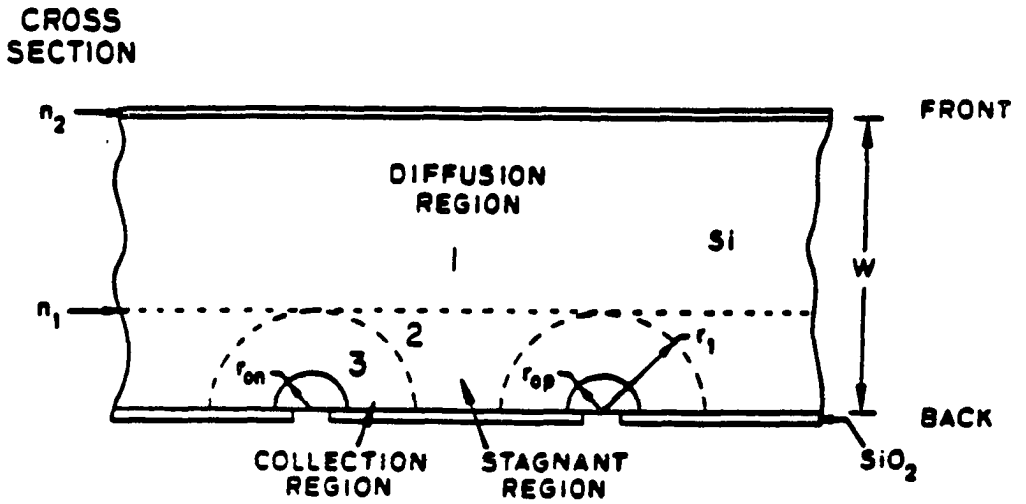

Figure 2.2: A cross section of a BPC (and IBC) cell showing the regions considered in modeling.

for a BPC cell, and

$$r_1 = \frac{P \times D_A^2}{4\pi}\left(\frac{1}{D_p^2} + \frac{1}{D_n^2}\right) \tag{2.5}$$

for an IBC cell; where P is the width of the unit cell shown in Figure 2.1, D_A is the ambipolar diffusivity, and D_p and D_n is the diffusivity of electrons and holes respectively. Note that both expressions are independent of the contact size. With the r_1 determined, the carrier density n_1 at r_1 can be related to the carrier density at the front n_2. In addition, n_{op} can also be related to n_1 through the following expressions

$$n_{op} = n_1 - \frac{J(r_1) \times P^2}{2\pi q D_p}\left(\frac{1}{r_{op}} - \frac{1}{r_1}\right) \tag{2.6}$$

for a BPC cell, and

$$n_{op} = n_1 - \frac{J(r_1) \times P}{2\pi q D_p}\left(\ln(\frac{r_1}{r_{op}})\right) \tag{2.7}$$

for an IBC cell; where $J(r_1)$ is the current density at r_1 which is the photo-generated current density less all the recombination loss in the diffusion and the stagnant region. The expression for n_{on} can be found by replacing the subscript p with n. With some derivations, the terminal voltage and current density can then be expressed as [2,26]

$$V = \frac{2kT}{q}\ln\left(\frac{n_{op}n_{on}}{n_1 n_i}\right), \tag{2.8}$$

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and,

$$J = J(r_1) - \left[J^p_{o,e} A_p \left(\frac{n_{op}}{n_i} \right)^2 + J^n_{o,e} A_n \left(\frac{n_{on}}{n_i} \right)^2 \right] \tag{2.9}$$

if the other recombination in the collection region is ignored.

The actual computation use the procedures above, and calculates the carrier density $(n_2, n_1, n_{op}, n_{on})$ self-consistently for a given photo-current density or an incident power density with known photo-response function.

2.3 Results and Discussion

Although the three-region approach mentioned in the previous section greatly reduces the actual computation time, it is not a real two-dimensional simulation. Therefore, it is interesting to see how close it is to a real two-dimensional device simulator—PISCES [31]. Figure 2.3 shows the carrier density contours for two IBC unit cells with different contact size; 5 and 15 μm. Both unit cells are 50 μm wide and 100 μm thick. The carrier density contours of both electrons and holes are generated under the applied voltage 0.8 volt across the p- and the n- type contact. The highest carrier density is about 1×10^{17} cm^{-3} at the contact and decreases toward the front surface. The spacing between two contours is 1×10^{15} cm^{-3}.

First, note that there is a substantial region, from the top surface downward to the back side, where the contours are essentially flat. This verifies the concept of the diffusion region. Second, the location where the contour starts to bend is about the same for both cells indicates that Eqn. (2.5) truthfully depicts the contact-size independence. Finally, in Figure 2.3a, the highest density of contours occurs at the p-type contact because of the lower diffusivity of holes. This indicates that majority carrier transport dominates in the collection region, which is one of the postulates in our modeling. In addition, the density of contours per unit length represents the gradient, and it also shows that most of potential drop occurs in the collection region, which verifies another point—the V_{res} can be calculated from the collection region only. Another minor point, which is obvious, is that the gradient of carrier density around the contact in Figure 2.3b is less than that in Figure 2.3a, indicates

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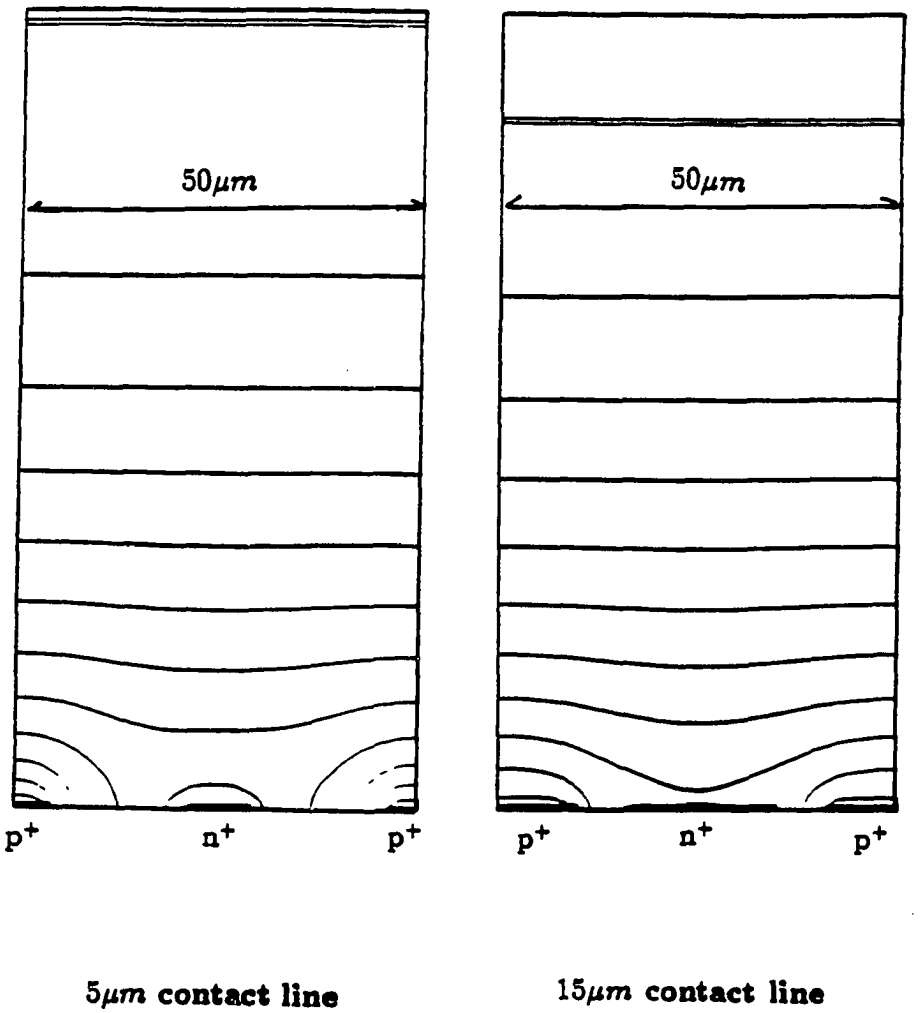

Figure 2.3: The carrier density contours of IBC cells; (a) with 5 μm, and (b) with 15 μ contact lines.

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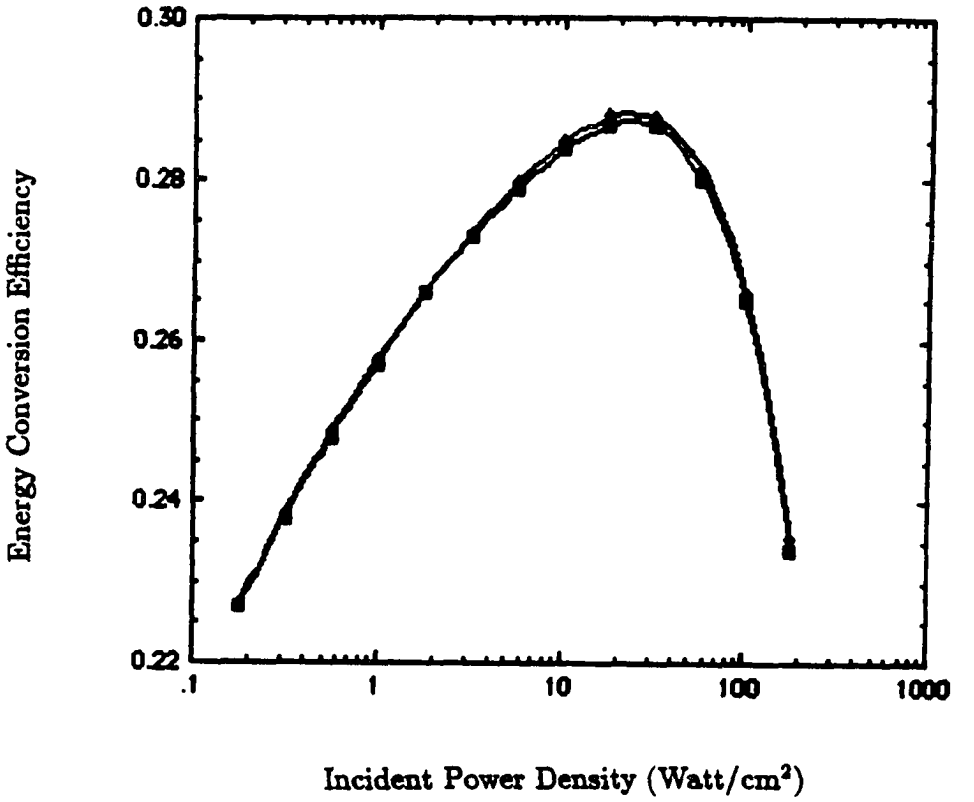

Figure 2.4: The cell efficiency vs the incident power density for a BPC and an IBC cell.

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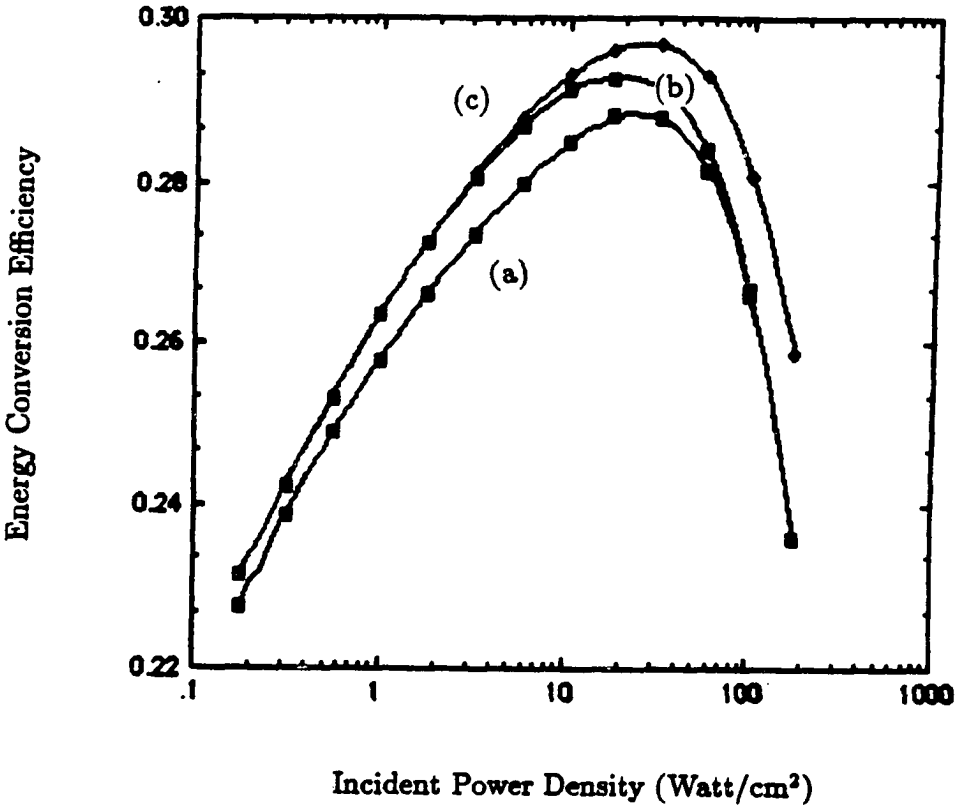

Figure 2.5: The cell efficiency vs the incident power density for three IBC cells; cell (a) 5 μm contact line and $J_{o,e} = 4.5 \times 10^{-13}$ A/cm^2, cell (b) 5 μm contact line and $J_{o,e} = 1 \times 10^{-14}$ A/cm^2, and cell (c) 15 μm contact line and $J_{o,e} = 1 \times 10^{-14}$ A/cm^2. The center-to-center distance between n$^+$ and p$^+$ line is 50 μm.

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Table 2.1: Modeling parameters

Cell thickness	100 μm
P	The dimension of the unit cell; 50 μm
R	The photo-responsivity; 0.415 A/watt
τ	The SRH bulk lifetime; 3 milliseconds
S	The effective surface recombination velocity; 7.5 cm/sec
C_a	Ambipolar Auger coefficient; 1.66×10^{-30} cm^6/sec
D_A	Ambipolar diffusivity; 18 cm^2/sec [32]
D_n/D_p	Majority carrier mobility data [33]
n_i	$3.563 \times 10^{16}(T^{1.5})\exp(-6980/T)$ [28]
$J^n_{o,e}$, $J^p_{o,e}$	4.5×10^{-13} or 1×10^{-14} A/cm^2

that V_{res} will be less for the larger contact.

Above all, we have shown that the modeling proposed in the previous section is almost the same as for a real two-dimensional device simulator. This provides a good frame of reference. Therefore, the question left is how to choose the parameters used in the computation. These are provided by Sinton who used the same modeling to simulate a BPC cell that fitted the experimental results well [2,29]. His data are included in Table 2.1 which lists all parameters that will be used in our simulation.

In Figure 2.4, the calculated cell efficiency is plotted against the incident power density for both a BPC and an IBC cell. Both cells have identical emitter coverage fraction ($\sim$ 10%), and the J_o of 4.5×10^{-13} A/cm^2 for both n- and p- type emitters. As shown in the figure, both cells have almost the same performance. A similar comparison between a BPC and an IBC cell were also reported by Sinton and Parrott respectively [2,34]; however, both showed that the BPC cell outperforms the IBC. This is attributed to that a larger unit cell size was used for the IBC cell in both reports. As shown in Eqn. (2.4) and (2.5), this leads to larger r_1 and higher potential drop in the collection region of the IBC cell; therefore, the IBC is

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worse. In our case, we use the same size of unit cell (50 μm), and both cells show no difference in terms of the performance at all. Nevertheless, there is another limitation, in practice, to make such IBC cells with diffused emitters. To have J_o of 4.5×10^{-13} A/cm^2, the emitter-base junction is about 4 μm deep, which means that the actual contact opening has to be less than one μm for a 50 μm wide unit cell. This may be a limit for most lithography technologies.

As we reduce the J_o down to 1×10^{-14} A/cm^2, and enlarge the emitter contact area, the cell performance is improved globally. This is shown in Figure 2.5 where the cell efficiency of three IBC cells are plotted against the incident power density. In the figure, cell (a) has 5 μm line contact and J_o of 4.5×10^{-13} A/cm^2, cell (b) has the same contact size as cell (a) but J_o is 1×10^{-14} A/cm^2, and cell (c) has the same J_o as cell (b) but with wider contact lines—15 μm. The curve for the cell (b) is less clear, it is first merged with that for cell (c) at low incident power density and change to that for cell (a) at high incident power density. By comparing cell (a) with (b), the better performance of cell (b) results from the lower J_o which is consistent with the results shown in Figure 1.3. However, the advantage of low J_o diminishes as the incident power density increases over 50 watts/cm^2.

The comparison between cell (b) and (c) is even more interesting. First, the cell efficiency of both cells stays the same at low incident power density, which indicates that the emitter recombination will be negligible as the J_o is below 1×10^{-14} A/cm^2. Secondly, note that the cell (c) starts to outperform the cell (b) at 10 watts/cm^2. This implies that the low internal series resistance is important even at the incident power density as low as 10 watts/cm^2, and becomes more obvious in the regime of high incident power density where the better current-collection capability of the large-contact cell lessens the power loss through the Auger recombination.

It now becomes obvious to see what an emitter should be for the concentrator solar cells. Low J_o is of course the primary requirement. As shown in Figure 1.2, the total emitter saturation current density below 1×10^{-14} A/cm^2 shows negligible effect. Take this value and assume the emitter areal coverage fraction is 30% for each type, this means that the J_o of each type of emitters should be around 2×10^{-14} A/cm^2. As far as the specific contact resistivity is concerned, the upper limit

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of ρ_c can be estimated by the potential drop across the contact interface at the short-circuit condition. Assume that the cell is operated at the design point (36 watts/cm^2) and the photo-responsivity is 0.415 A/watt, a current density about 50 A/cm^2 (short-circuit current) will flow through each type of contact of 30% coverage fraction. If we deliberately set the maximum potential drop, due to the contact resistance, to be 5 mV on each contact, this leads to the conclusion that ρ_c for each type has to be less than 1×10^{-4} Ω-cm^2. Note that, with the same structure and incident power density, a 15 mV potential drop will be seen due to the internal series resistance.

2.4 Summary

To summarize, we have modeled both BPC and IBC cells simultaneously in this chapter. The model adopted was shown to be very similar to a real two-dimensional device simulator. Based on our simulation results, we showed that the cell performance is insensitive to the emitter geometry if the same unit cell is used. Further simulations also indicated that the benefit for the cell of having low J_o emitters comes from two facts. One is the low emitter recombination, and the other is the low series resistance accompanied with the use of large contacts. The requirements for the emitter to be used in the concentrator solar cells were determined. It is certain that a noticeable improvement of the cell performance will be seen if an emitter fulfills the requirements. The requirements are 2×10^{-14} A/cm^2 for J_o, and less than 1×10^{-4} Ω-cm^2 for ρ_c for both types.

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Chapter 3

Polysilicon-Contacted Emitters

This chapter reviews the polysilicon-contacted emitter with emphasis on the problems associated with an interfacial oxide. The necessity of an interfacial oxide for a polysilicon-contacted emitter to have low J_o is explained in the first three sections. However, there are some problems with the interfacial oxide. First, the p-type polysilicon emitter with an interfacial oxide does not appear to have as low J_o as the n-type. There are several possibilities for this high J_o. One of the explanations is that the recombination at the oxide interface on the substrate side is inherently higher when it is doped with boron. This is examined in Section 2.4. Another problem is the high emitter resistance associated with the polysilicon SIS emitter. In Section 2.5, it is shown that the emitter resistance for a polysilicon SIS emitter, which has very low J_o, is too high for concentrator solar cells. In the final section, the integrity of the interfacial oxide is discussed. The interfacial oxide tends to break up during a high temperature anneal. As the oxide breaks up, both J_o and ρ_c are affected. The oxide breakup process appears to depend on the oxide thickness as well as the dopant levels, which make it difficult to control in the processing.

3.1 The Polysilicon-Contacted Emitter

The polysilicon-contacted emitter is now widely used in the silicon bipolar technology. The demand for polysilicon-contacted emitters stems from the down-scaling

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of bipolar transistors. As the lateral dimension of devices decreases, the width of the base region has to be made narrower in order to reduce the base transit time which is now appreciable to the delay of the device in operation [35,36]. This calls for a shallow emitter junction, because a precise control of thin base width, which is crucial for the device performance, is difficult to make with a deep emitter junction. The use of polysilicon contacts, on one hand, fulfills this requirement because of the high dopant diffusivity compared with that in the substrate. On the other hand, it also retains low base current since it can act as the extension of the shallow emitter to prevent minority carriers from reaching the metal contact where a high surface recombination velocity is generally conceived. This is shown in Figure 3.1 [8] in which the maximum current gain is plotted against the inverse of the base Gummel number for devices contacted with either polysilicon or metal. As shown in the figure, the current gain of a polysilicon-contacted transistor is almost an order of magnitude higher than that of the metal-contacted counterpart. With the same base Gummel number, the collector current should be roughly the same in both devices; therefore, the improvement can be attributed to the reduction of the base current. One advantage of low base current is that it can be used to tailor the base resistivity which is a dominant parameter of the device delay time in the modern high-speed bipolar design.

The results shown in Figure 3.1, which was first reported by Graul *et al.* [8], have more profound implications. Since the base current is primarily due to the recombination in the emitter region, the reduction of base current also indicates that the polysilicon-contacted device has lower J_o. This is shown by the emitter Gummel number, $(Q_e/D_p)_{eff}$, of these two devices. Graul *et al.* reported that their polysilicon-contacted device has an emitter Gummel number of 2×10^{14} cm^{-4}, thus the equivalent J_o is

$$J_{o,e} = \frac{(qn_i^2)}{\left(\frac{Q_e}{D_p}\right)_{eff}} = 1.7 \times 10^{-13}\ (\mathrm{A/cm^2}).$$

This implies that the contribution from the polysilicon to the J_o has to be less than 1.7×10^{-13} A/cm^2. However, the simulation result [3] indicates that the J_o of the monosilicon emitter with the same doping configuration is about an order of

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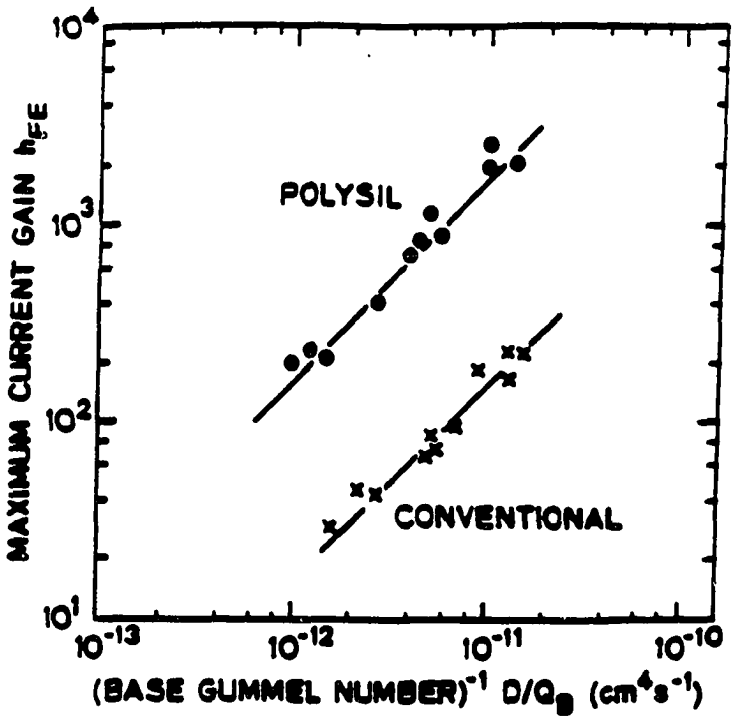

Figure 3.1: Maximum current gain versus inverse Gummel number D_n/Q_B for double-implanted conventional transistors and transistors with As-polysil emitter.

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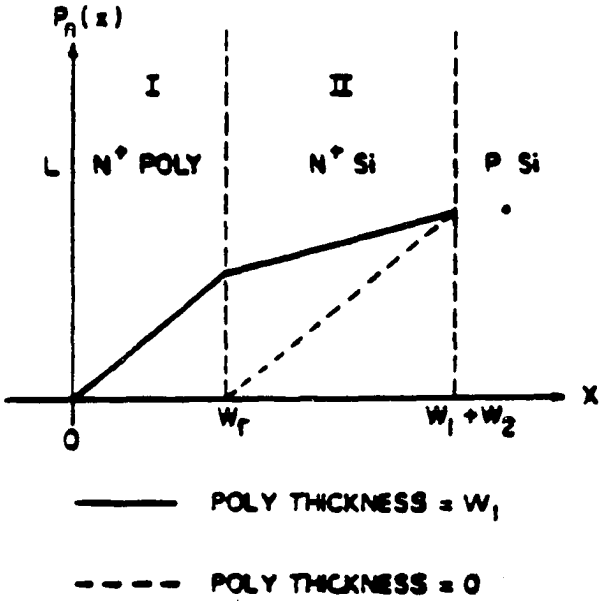

Figure 3.2: Schematic illustrating the two-region model for shallow emitters with n^+ polysilicon contact.

magnitude higher. In another words, polysilicon must be different from monosilicon in terms of the minority carrier transport.

It appears that the base current of a polysilicon-contacted bipolar transistor depends critically on the detail structure of the bulk of the polysilicon as well as its interface to the substrate. Correspondingly, two theories have been proposed to explain the result observed by Graul *et al.*.

3.2 The "Pure" Polysilicon Emitter

Ning and Isaac [18] proposed that the increase of the current gain observed on the polysilicon-contacted emitter can be explained by the two-region model. This is illustrated in Figure 3.2 which shows the hole distribution in the n-type emitter region. From left to right along the horizontal axis, it denotes the metal contact at $x = 0$, the contact between the polysilicon and the substrate at $x = w_1$, and the

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emitter-base junction at $x = w_1 + w_2$. Note that the metal-contacted device is represented in the figure by assuming that $w_1 = 0$ or simply moving the metal contact to w_1. In addition, the relative magnitude of the base current for different devices can be compared by evaluating the slope of the hole distribution at $x = w_1 + w_2$ ($\propto (\frac{dp_n}{dx})_{x=w_1+w_2}$). For a shallow junction in which the width of the monosilicon region (w_2) is less than the minority carrier diffusion length (L_{p2}), the hole distribution is presented in the figure for both the polysilicon-contacted device (the solid line) and the metal-contacted device (the dashed line). The steeper gradient of the metal-contacted device, indicating higher base current, results from the high recombination velocity at the metal contact ($x = w_1 = 0$) which forces p_n to be zero at $x = w_1 = 0$. In contrast, less recombination in the polysilicon reduces the hole gradient of the polysilicon-contacted device. Consequently, the current gain is higher for the polysilicon-contacted device.

Although the two-region model explains the higher current gain observed in the polysilicon-contacted device, it does not guarantee that the recombination in the polysilicon will be less than that in the monosilicon as we pointed out previously. Nevertheless, Ning and Isaac suggested a possibility that the recombination in the polysilicon will be less than that in the monosilicon. They argued that the minority carrier mobility in the polysilicon should be smaller because of the grain boundary scattering. Moreover, since the emitter is heavily doped, the minority carrier lifetime is likely dominated by the Auger recombination and appears the same for both the polysilicon and the monosilicon. Consequently, the lower transport velocity of minority carriers, due to smaller mobility, will reduce the recombination in the polysilicon.

In the experiments, they made npn bipolar transistors with either polysilicon-contacted or metal-contacted emitters. The current gain of the polysilicon-contacted device was found to be about six times higher than that of the metal-contacted device. In addition, they also observed a weak dependence of base current on the polysilicon thickness, confirming that the minority diffusion length is very short. A similar weak dependence was also observed by Patton *et al.* [37], which also indicated the blocking capability of the structure defect (the regrown polysilicon-monosilicon

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interface in their experiments) can be enhanced by the dopant segregation. This seemed in agreement with what was observed by Neugrochel [38] that the base current reduction was observed only on the device with dopant segregation at the polysilicon-substrate interface. In a way, this seems to support their view that hole mobility, due to the grain-boundary scattering, is smaller in the polysilicon.

Since this mechanism concerns only the bulk properties of the polysilicon, we refer to this kind of emitter as the "pure" polysilicon emitter in order to distinguish it from the otehr based on different mechanism.

Although Ning and Isaac's results do show that the current gain of the polysilicon-contacted device is six times higher than that of the metal-contacted counterpart, it is still smaller than what was observed by Graul *et al.*. Moreover, the current gain is sensitive to the device design and it is difficult to verify, based on their results, that the low minority carrier mobility does reduce the recombination in the polysilicon.

More systematic experiments were carried out by Patton *et al.* [21,37]. In their study, the J_o contribution from the recombination in the polysilicon alone was extracted out by the device modeling. Their results are shown in Figure 3.3 where the J_o contribution from the polysilicon bulk, J_{os}, is plotted against the doping concentration of the polysilicon. Three distinct regions are observed from the figure. In region I, J_{os} starts high at low doping concentration then decreases as the concentration increases. This is attributed to the high recombination at the grain boundary. As the doping concentration increases, more defects at the grain boundaries are passivated by the dopant segregation; thereby, the J_{os} decreases as the doping concentrations increases. In region II, J_{os} is relatively insensitive to the doping level. This is because the grain boundary is almost saturated with dopants. Although the grain-boundary recombination will not change much as the doping concentration goes beyond this region, any increase of doping will shorten the minority carrier lifetime in the grain because of the heavy doping effect. Consequently, the recombination inside the grain gradually prevails over the grain-boundary recombination, which explains the increase of J_{os} in region III.

The results shown in Figure 3.3 are significant because they include all the effects of the recombination in the polysilicon. The effect of the detailed structure of the

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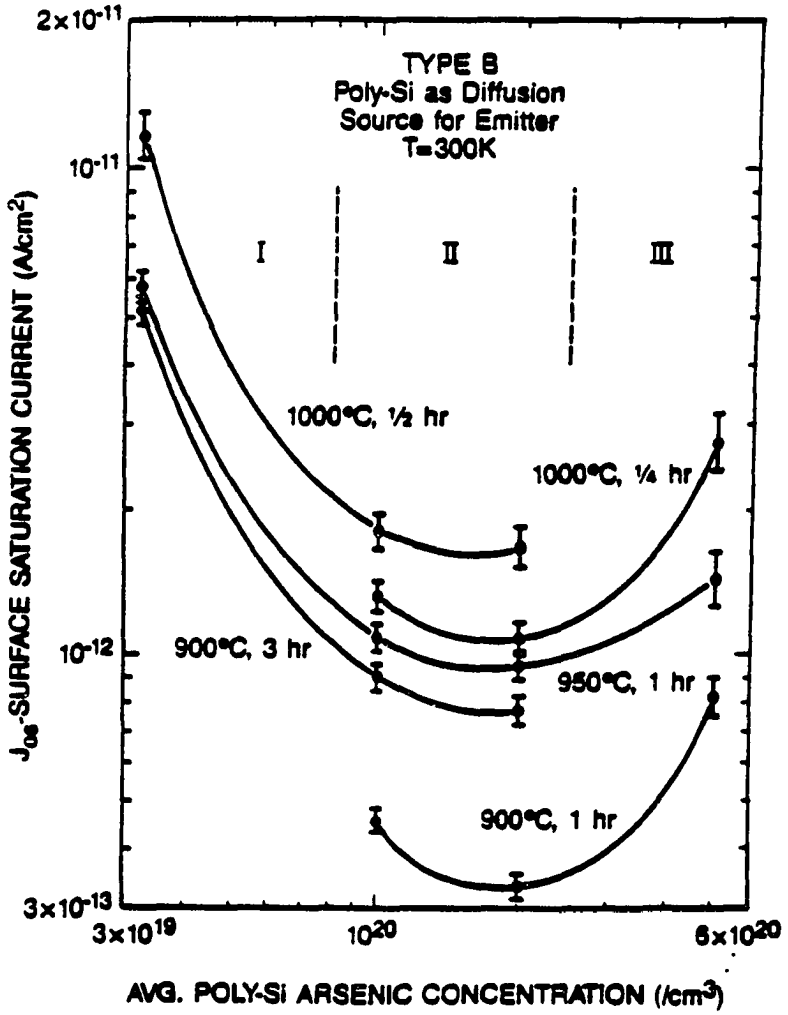

Figure 3.3: Dependence of J_{os}, the surface of contact saturation current density, on the average chemical concentration of As in the polysilicon.

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polysilicon can be seen from the difference in J_{os} of various curves which are labeled with the drive-in temperature. At the same doping concentration, the variation of J_{os} can be attributed to the grain size difference of the polysilicon under various drive-in schedules. However, as we can see from the figure, the structure variation of the polysilicon does not make too much difference in J_{os}. More importantly, except for the one labeled 900 °C-1 hour, the J_{os} is about 1×10^{-12} A/cm^2 at the optimum doping level (region II). This is about one order of magnitude higher than what was reported by Graul *et al.*. Clearly, the improvement due to the low minority carrier mobility in the polysilicon, suggested by Ning and Isaac, is not likely to be the only mechanism responsible for low J_o.

In fact, the Auger recombination under most conditions is not, as suggested by Ning and Isaac, the dominant mechanism for the minority carrier lifetime. As the results shown in the figure, the Auger Recombination is important only when the doping level in the polysilicon is extremely high. This implies that the minority carrier lifetime, due to additional grain-boundary recombination, will be shorter in the polysilicon compared to that in the single-crystal silicon. Since the low mobility and the short lifetime of minority carriers have the opposite effect on J_o, they cancel each other out so that the J_{os} is not too much different from the J_o observed in the single-crystal counterpart.

To conclude, it is not likely that a polysilicon emitter with low J_o can be explained with the bulk-structure difference between the polysilicon and the single-crystal counterpart. Consequently, another mechanism that attribute the low J_o to the interfacial structure was proposed.

3.3 The Polysilicon SIS Emitter

The other proposed mechanism attributes the improvement of base current to the existence of a very thin oxide (interfacial oxide) sandwiched between the polysilicon and the substrate. This was first suggested by de Graaff and de Groot [9], and their reasoning is straightforward. Most minority carriers injected into the emitter will be blocked by the interfacial oxide so that the recombination in the polysilicon region

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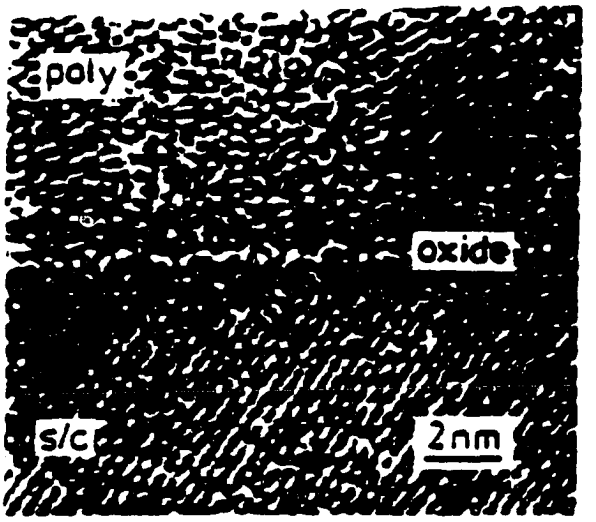

Figure 3.4: HREM micrograph of an as-deposited specimen given an HF treatment.

can be very small. If the recombination in the rest of emitter is also negligible, very low J_o will then be obtainable. The same concept has been used in the metal-insulator-semiconductor (MIS) devices [23,24]. For clarity, we refer this type of polysilicon-contacted emitter as the polysilicon SIS emitter.

The existence of an interfacial oxide has been observed by several authors with the transmission electron microscope (TEM) [10,19,20,22,39]. Such an oxide is primarily formed in the polysilicon predeposition cleaning process. Even with a HF dip prior to the silicon deposition, there is still a native oxide of 5-8 Å at the silicon surface as in the picture shown in Figure 3.4 [10]. On the other hand, the oxide thickness can be doubled [3,10,19,20] if the final cleaning step involves chemicals such as $HCl:H_2O_2:H_2O$ or $NH_4OH:H_2O_2:H_2O$ which is typical in wafer cleaning processes.

The interfacial oxide appears quite intact and can be broken only under a high temperature anneal. If the carrier transmission probability across the interfacial oxide is low enough, the situation would be close to what de Graaff and de Groot proposed. In general, the transmission probability across a thin oxide is dominated by the tunneling process which is sensitive to the oxide thickness. Consequently,

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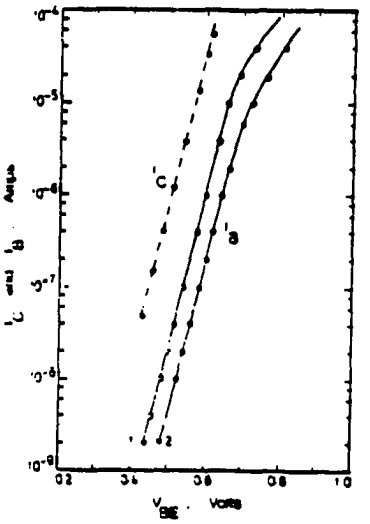

Figure 3.5: Collector and base current as a function of base/emitter voltage for a device given an HF etch (device 1), and a comparable device given an RCA clean (device 2).

it is possible to see a significant difference of J_o for devices with different oxide thickness. This is demonstrated in Figure 3.5 [11] where the Gummel plots are given for two different devices; the HF-device and RCA-device. Both devices had identical processing, except for the cleaning step prior to the polysilicon deposition. The HF device was given an etch in buffered hydrofluoric acid before the polysilicon deposition, while the RCA device had a chemical oxide ($\leq$15 Å) grown in the predeposition cleaning process. As shown in Figure 3.5, the current gain of the RCA device is improved by a factor of 5 compared with that of HF device. Since the characteristics for both devices are ideal, the reduction in emitter recombination due to the existence of an interfacial oxide is evident.

Note that the comparison made above is based on the current gain improvement and cannot be used as an evidence that the J_o of a polysilicon SIS emitter is reduced. However, the very low J_o of the polysilicon SIS emitter has been demonstrated by other authors [7,10]. Figure 3.6 is the J_o of polysilicon SIS emitter reported by Kwark [7]. Note that J_o of 1×10^{-14} A/cm^2 was observed on the device annealed at 850 °C. The rapid increase of J_o upon the anneal temperature is due to the

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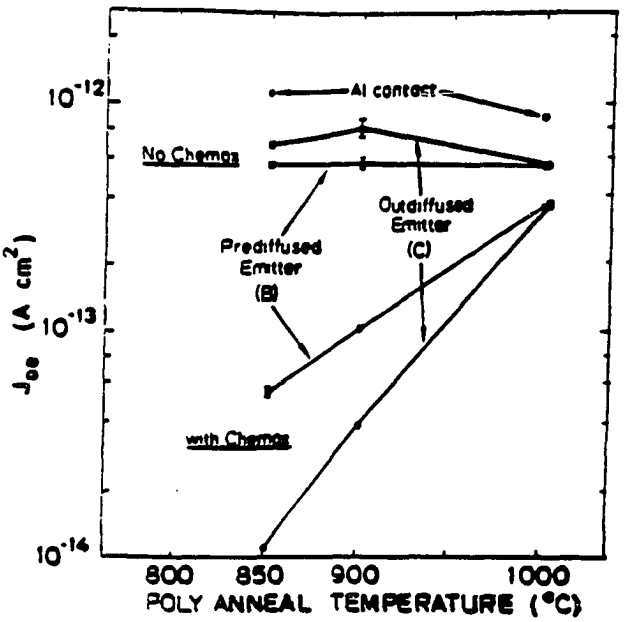

Figure 3.6: $J_{o,e}$ for n-type polysilicon emitters with and without a chemically grown interfacial oxide.

breakup of the interfacial oxide which will be discussed later. A relatively intact interfacial oxide also explains a much lower J_{os} observed on the 900 °C-1 hour curve in Figure 3.3.

3.4 The p-type Polysilicon SIS Emitters

As pointed out in Chapter 1, the p-type polysilicon SIS emitter is as important as the n-type polysilicon SIS emitter for solar cell applications. Because of fewer applications in integrated circuits, very little data for J_o were reported for the p-type polysilicon emitter. Even worse, the reported J_o on the p-type polysilicon SIS emitter is much higher than that of the n-type with similar processing. Table 3.1 [7] lists both J_o and ρ_c of the p-type polysilicon emitter with or without chemically grown oxide ($\leq$15 Å). For devices with a chemical oxide and the least anneal, the J_o is already as high as 3×10^{-13} A/cm^2, which is more than ten times higher than that of the n-type counterpart [7].

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J_o and ρ_c for P^+ POLY				
without ChemOx				
T_{anneal}	900	975	1000	1050
J_o (10^{-13} A/cm^2)	9		17	
ρ_c($\mu\Omega$-cm^2)		3.8		5.4
with chemox				
J_o (10^{-13} A/cm^2)	3		9.5	
ρ_c($\mu\Omega$-cm^2)		4.23		6.1

Table 3.1: J_o and ρ_c for P^+ polysilicon contacts.

There are two possible explanations for higher J_o observed on the p-type polysilicon SIS emitter. One possibility is that the interfacial oxide is no longer intact such that electrons are free to enter the polysilicon region. This could happen if the interaction between boron and the interfacial oxide enhances the oxide break-up [22]. The other possibility is that the recombination at the oxide interface to the substrate is much higher in the p-type polysilicon SIS emitter.

In the following paragraphs, we show some evidence which indicates that the quality of the oxide interface is indeed inferior when the substrate is doped with boron [40]. Although the results presented below are mainly from experiments done on the thick oxide, it is expected that the behavior for a thin oxide should be similar, if not worse.

Typically, the J_o contribution from the recombination at the interfacial oxide, J_{ox}, can be expressed as

$$J_{ox} = q\, n_o\, S; \tag{3.1}$$

where n_o is the equilibrium minority carrier density, and S is the effective surface recombination velocity. Clearly, in order to keep the J_{ox} low enough, we would like to have both n_o and S as low as possible. To make n_o low, the doping in the vicinity

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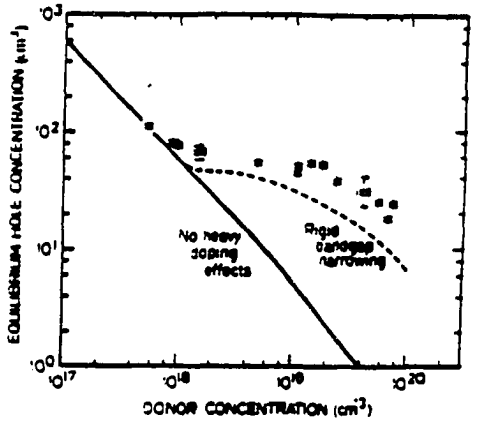
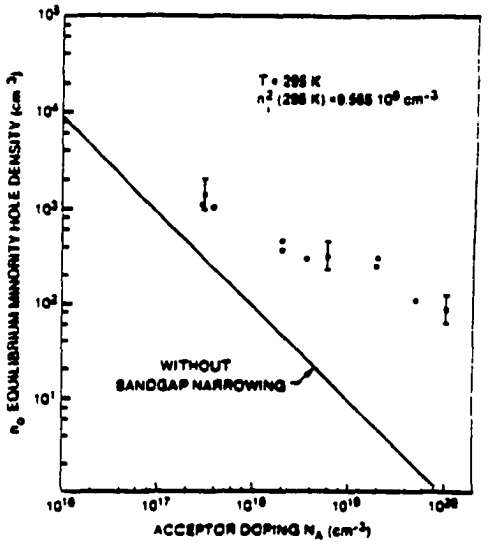


(a)



(b)

Figure 3.7: Extracted equilibrium minority carrier density of heavily-doped silicon; (a) n^+-Si, and (b) p^+-Si.

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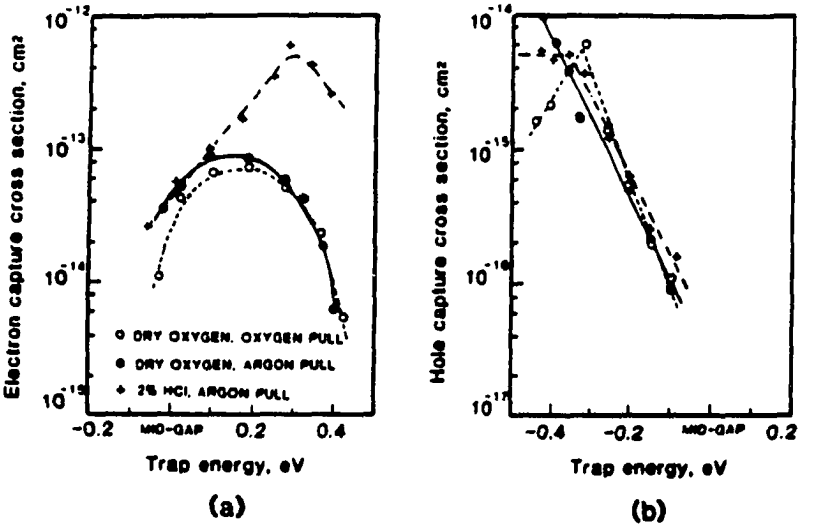

Figure 3.8: The electron and hole capture cross section vs the trap energy.

of the interfacial oxide has to be high which is generally the case for most emitters; however, high doping degrades the S as well. In addition, n_o does not decrease linearly as the doping concentration increases because of the heavy doping effect. This is shown in Figure 3.7a and b where n_o is plotted as function of the doping concentration for each type [41,42]. Note that n_o decreases with a lower rate once the doping concentration is higher than 1×10^{17} cm^{-3} for both types, and the n_o in the p-type is generally higher than that in the n-type.

S can be expressed as the product of the interface defect state density, D_{it}, the minority carrier capture cross section, σ, and the carrier mean velocity, v_{th}; thus

$$S = D_{it}\ \sigma\ v_{th}; \tag{3.2}$$

Although D_{it} depends critically on the oxide growth and post-anneal conditions [43], it should be noted that D_{it} is also a function of the doping level. Snel [44] reported that D_{it} is virtually independent of the doping levels until these levels reach 1×10^{16}~1×10^{17} cm^{-3}. Above this doping level, D_{it} increases with doping concentration sublinearly and faster for the p-type sample, which indicates that boron degrades the oxide interface more rapidly than phosphorus. The carrier capture cross section is a function of the location of the defect states in the silicon

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band gap and can be very different for electrons and holes. Figure 3.8a and b is the electron and the hole capture cross section measured with deep-level-transient-spectroscopy (DLTS) for oxides processed under various conditions [45]. The data presented in the figures are derived under the assumption that the carrier mean velocity is the same for both electrons and holes (1×10^7 cm/sec); therefore, the difference of σ in both figures accounts for the collective effects resulted from the last two terms in the equation above. Since the recombination at the interface is, in most case, dominated by the Shockley-Read-Hall (SRH) mechanism, it is the capture cross section at the mid-gap that is of concern. From the figures, σ of both type carriers at the mid-gap is about the same for various processing conditions. However, the electron capture cross section is generally about 100 times higher than the hole capture cross section at the mid-gap. This means that the S of the p-type emitter will be much higher than that of the n-type.

As shown in the above, every parameter involved in the expression of J_{ox} appears larger for p-type; therefore, J_{ox} of the p-type polysilicon SIS emitter will be higher even with the same interfacial oxide quality. In another words, it is far more important to improve the interfacial oxide, instead of increasing the oxide thickness, for the p-type polysilicon SIS emitter to have a low J_o.

3.5 The Specific Contact Resistivity of a Polysilicon SIS Emitters

One of the major problems of the polysilicon SIS emitter is that the emitter resistance is much higher compared with that of the "pure" polysilicon emitter. This is due to the insertion of the interfacial oxide. Because of the wide band gap of the oxide, it is likely that the majority carrier may face a similar energy barrier to that for the minority carrier. In order to maintain the same current level in the polysilicon SIS emitter, an additional potential drop develops across the interfacial oxide which in turn is seen as an increase in the emitter resistance. The series

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resistance caused by the interfacial oxide is usually expressed in terms of the specific contact resistivity, ρ_c, with the unit of Ω-cm^2. The high ρ_c of the polysilicon SIS emitter is demonstrated in Figure 3.9 which was observed by Crabbé [22]. In Figure 3.9, the ρ_c of the device with either a native oxide (HF) or a chemical oxide (ChemOx) was plotted against the doping concentrations under various anneal conditions. Depending on the type of the interfacial oxide, the results can be divided into two distinct groups. With the same doping concentration and anneal schedule, the ρ_c of the ChemOx device is about ten times higher than that of the HF device. Since the only difference between these two devices is the oxide thickness, it clearly indicates that the carrier transport across the interfacial oxide is very sensitive to the oxide thickness, which usually implies that tunneling is the dominant process. As mentioned previously, a very low J_o can be obtained (see Figure 3.6) for the n-type polysilicon SIS emitter with a chemically grown interfacial oxide. However, the corresponding ρ_c of such device can be as high as 4×10^{-4} Ω-cm^2 at the doping concentration of 1×10^{20} cm^{-3}, which is the typical doping concentration of the emitter. This is four times higher than the value mentioned in the previous chapter as our goal, and the potential drop across the polysilicon SIS emitter would be intolerable.

3.6 The Integrity of the Interfacial Oxide

Another complication in the polysilicon SIS emitter is that the interfacial oxide is not thermally stable; therefore, both J_o and ρ_c are sensitive to the processing conditions as well as the structure of the interfacial oxide. In this section, we summarize the results which show the effect of the oxide integrity to the J_o and ρ_c respectively.

3.6.1 The Breakup of the Interfacial Oxide

During a high temperature anneal, the breakup of the interfacial oxide has been reported by several authors [10,19,20,22,39]. For a chemically grown interfacial

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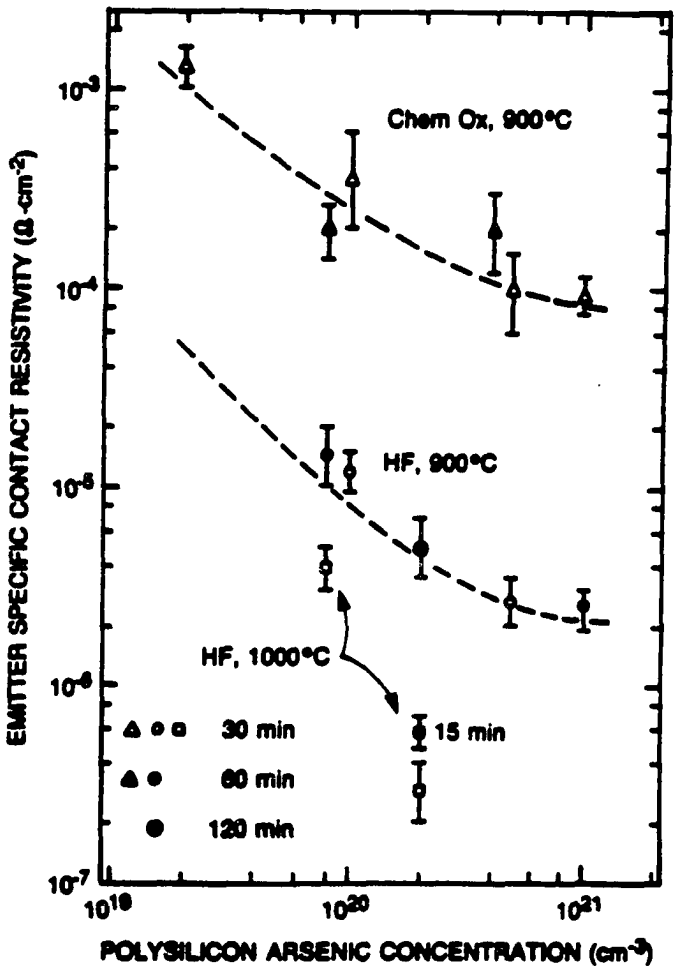

Figure 3.9: Emitter resistance as a function of processing conditions.

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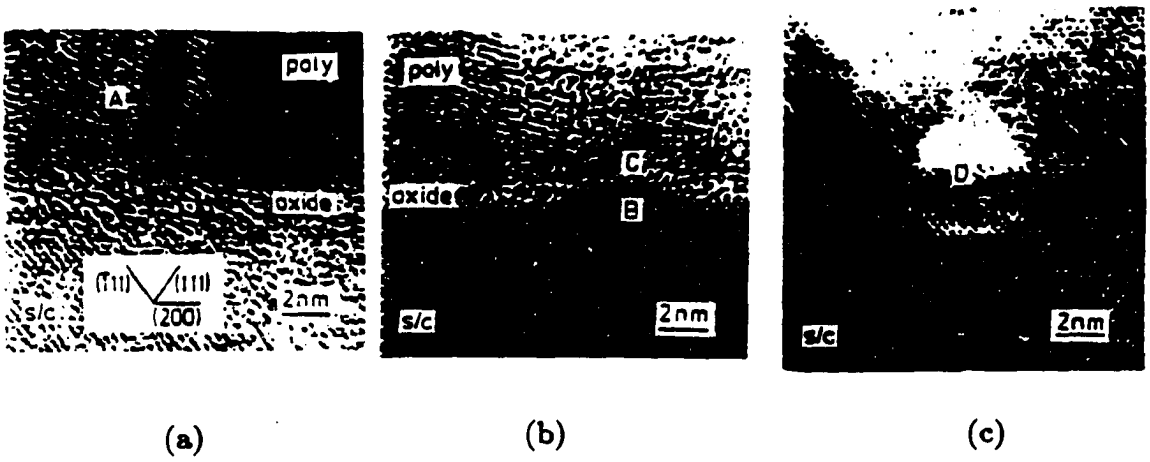

Figure 3.10: The integrity of a chemically grown interfacial oxide for (a) as-deposited sample, (b) 950 °C-preanneal sample, and (c) 1100 °C-preanneal sample.

oxide, the breakup process was studied by Wolstenholme [10] in detail.

In the experiment, they prepared two sets of samples with identical processing; one with bipolar devices for the electrical measurement, the other for the TEM examination. Prior to the polysilicon deposition, the samples were either dipped into HF (HF-devices) or immersed into hot NH_4OH:H_2O_2:H_2O as 1:1:5 for 10 min (RCA-devices). The treatments gave a very thin oxide on the silicon surface. Typically, the thickness was $\sim$ 8 and $\sim$ 15 Å on HF- and RCA- devices respectively. The samples, after the polysilicon deposition, were given a 10 min anneal at various temperatures between 950 to 1100 °C before the second anneal at 900 °C for 30 min which served to drive arsenic into the polysilicon. Because the final drive-in temperature is lower than that for the pre-anneal treatment, the temperature dependence of the oxide integrity can be correlated to the preanneal temperature.

Figure 3.10a is the picture for the sample with a chemically grown oxide. The interfacial oxide layer is seen as a thin bright band separating the lattice fringes of the polysilicon from that of the silicon and is about 15 Å wide. A similar configuration was also reported by Bravman *et al.* [19]. The interfacial oxide remains continuous and uniform after a 900 °C-30 min preanneal; however, it begins to undulate as the preanneal temperature was increased to 950 °C. In some regions, the oxide actually

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has been broken up so that the polysilicon is epitaxially realigned with the substrate as shown in Figure 3.10b. The oxide breakup and the thickness-undulation become more pronounced for the sample with 1000 °C preanneal. In some regions, the oxide has increased in thickness to 22 Å in contrast to the original thickness of 15 Å, and more breakup regions were observed. For a 1100 °C-10 min anneal, the oxide, in fact, balls up to numerous tiny inclusions embedded in the epitaxial regrown matrix as Figure 3.10c shows.

For HF-devices, the high temperature anneal effect appears similar, except that the oxide breakup takes place at lower temperature. Even in the sample without any preanneal and full processing (900 °C-30 min), the interfacial oxide is no longer continuous. With a 1000 °C-10 min anneal, the interfacial oxide balls up just like the RCA-device sample with 1100 °C preanneal (see Figure 3.10c).

The cause for the oxide break-up has been attributed to the reduction of the total energy related to the SiO_2/Si interface [10]. The consequence of reducing such energy is to reduce the area-to-volume ratio. Wolstenholme *et al.* found that the total volume of the oxide does not change for the oxide going from a continuous layer to a balled-up state; instead, the interfacial area decreases by typically ~ 5 to ~ 10 times. Although the global trend is to reduce the area-to-volume ratio, the driving force for the thin oxide to break up may come from two different sources; the high initial area-to-volume ratio of a thin and continuous oxide film, and the high energy state caused by unsaturated Si-O bondings of the interfacial oxide. Current results appear not sufficient enough to distinguish these two sources since both are oxide-thickness dependent. For example, the native oxide formed on the HF devices is known to break up more rapidly than the chemically grown oxide, which seems to support the first case. However, it was also reported that the oxygen content in the native oxide is much less than the stoichiometric ratio of SiO_2 [17]. As a result, the fast-breakup of the native oxide can be attributed to the highly unsaturated Si-O bondings as well. In addition, the oxide breakup is found to be enhanced with high doping concentration [10,19,20]. This is understandable because most dopants are glass formers which tends to compete with silicon atoms to bond with oxygen [46]. As the dopant concentration increases, more oxygen atoms either bond with the

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dopant to form low melting temperature doped-glass, or are released and rebond at more stable locations. In both cases, the oxide breakup process is enhanced.

3.6.2 The Oxide-Integrity Dependence of J_o and ρ_c

In the same report, Wolstenholme *et al.* also measured the corresponding base current for each preanneal sample. This is shown in Figure 3.11 which is the Gummel plot for devices annealed under conditions described above. Since the interfacial oxide does not change for the sample annealed under 900 °C, the base current of the 900 °C-sample is, as expected, very close to that of the control sample. As the oxide starts to break up at 950 °C, the base current increases accordingly because of the increase of the recombination in the polysilicon region. Note that the J_o of 1100 °C-sample is about 2.4×10^{-12} A/cm^2 which is close to that of a pure polysilicon emitter. This is what is expected since the interfacial oxide has balled up completely.

The other consequence of the oxide breakup is the significant reduction of the ρ_c. In the region in which the oxide is broken, the polysilicon has a tendency to realign with the substrate underneath (see Figure 3.11). Such realignment offers a highly conductive channel through the interfacial oxide; consequently, the contact resistance can be drastically reduced. For the carrier tunneling through the interfacial oxide, the equivalent resistivity is evaluated in Section 4.3 (p. 56). Assume that the interfacial oxide thickness is 15 Å, the equivalent resistivity is $\sim$ 800 Ω-cm, If the resistivity in the broken region is the same as that of the bulk resistivity of the emitter ($\sim$ 5 mΩ-cm), then the resistivity in the broken region is about five orders of magnitude lower than that of the unbroken region. A rough estimate of such an effect on ρ_c has been demonstrated in Chapter 1. Experimentally, the low ρ_c resulting from a broken interfacial oxide was also reported by several authors [22,47,39].

In addition, we have pointed out earlier that J_o for the p-type polysilicon SIS emitter will be higher because of the inferior oxide interface quality. However, another possibility is that the oxide breakup may proceed more rapidly in the the

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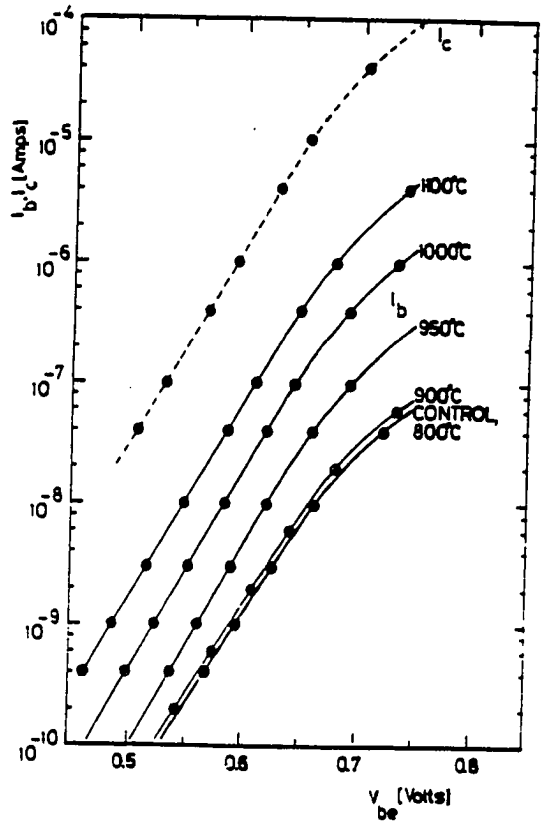

Figure 3.11: Gummel plots of devices given an RCA treatment and preanneal in the range 800-1100 °C.

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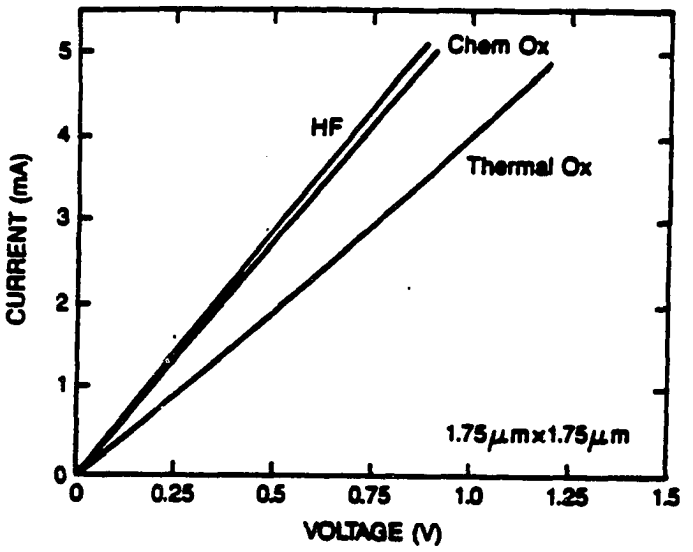

ρ_c $\Omega.cm^2$	HF	ChemOx	ThermalOx
	2.5×10^{-7}	3.5×10^{-7}	5.5×10^{-7}

Figure 3.12: Specific Contact Resistivities of p^+ Contacts

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presence of boron. If this is the case, the corresponding ρ_c for p-type polysilicon emitters will be lower too. This was also found by Crabbé [22] and is presented in Figure 3.12. The results were obtained from the samples with various interfacial oxide but all annealed at 950 °C for 30 min. For comparison, the ρ_c for the n-type sample, which had a chemical oxide and was annealed at 1000 °C for one hour is 8×10^{-7} Ω-cm^2, while the p-type one with the same interfacial oxide, as shown in the figure, is more than two times lower.

Since both J_o and ρ_c relate to the integrity of the oxide, it is clear that a simple correlation would appear if ρ_c is mapped as a function of J_o. This was first demonstrated by Crabbé [22] and is presented in Figure 3.13 for n-type polysilicon contacts. In the figure, the data run from upper-left corner to the lower-right corner which, as expected, shows the effect of the oxide breakup on the J_o is the opposite to that on the ρ_c. In addition, the data cover a great range of variations in terms of the type of the interfacial oxide as well as the anneal conditions; yet a very simple relationship is shown. This may indicate that the oxide integrity is the primary parameter for both the J_o and ρ_c once the oxide is broken.

3.7 Summary

In this chapter, we have discussed many aspects of the polysilicon-contacted emitter. It is clear that an intact interfacial oxide is essential for a polysilicon-contacted emitter to have low J_o because of the high recombination inside the polysilicon. Even so, the J_o of experimentally demonstrated p-type polysilicon SIS emitters are still too high for concentrator solar cells. Another major problem of the polysilicon SIS emitter is the high emitter resistance imposed by the interfacial oxide. This is due to the low transmission probability of majority carriers across the interfacial oxide, which is the same mechanism used to suppress the J_o. Consequently, a polysilicon SIS emitter with low J_o always suffers high emitter resistance. The interfacial oxide integrity also poses some difficulties in the processing. During a high temperature anneal, the interfacial oxide tends to break up. As a result, both J_o and ρ_c are affected. This is shown in Figure 3.13 which manifests many

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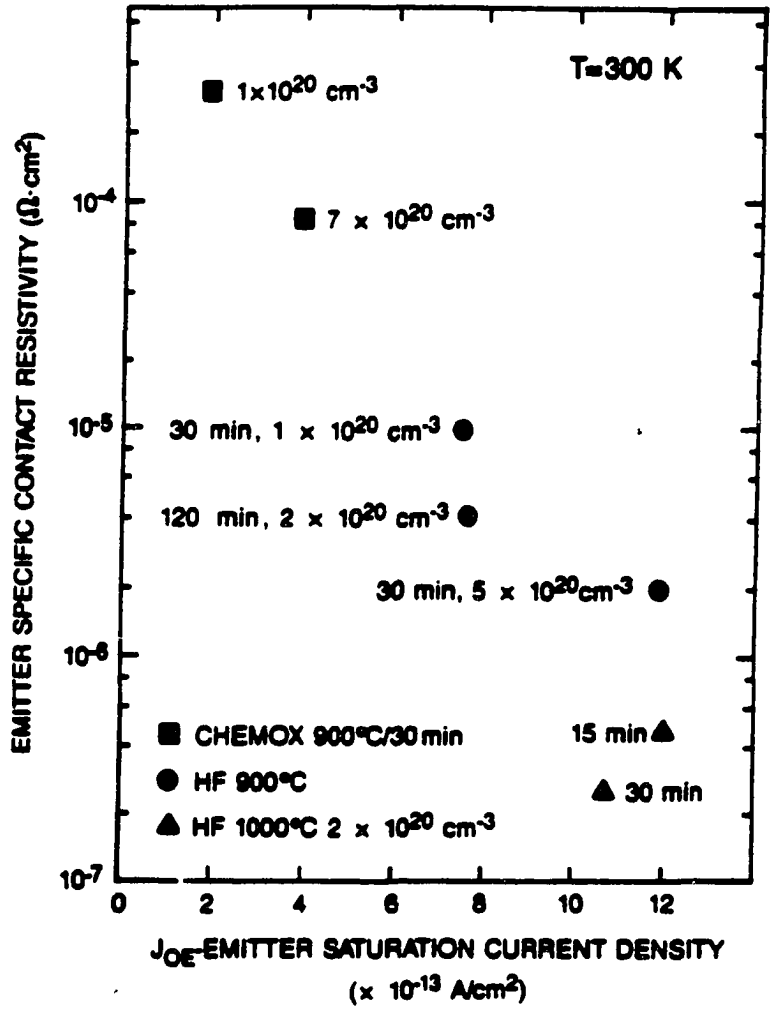

Figure 3.13: ρ_c-J_o trade-off

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aspects of problems of a polysilicon SIS emitter. At the upper-left corner, the polysilicon SIS emitter suffers a high contact resistance which makes it useless for device applications. At the lower-right corner, the polysilicon SIS emitter is just the same as a pure polysilicon emitter for which the J_o is too high for concentrator solar cells.

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Chapter 4

The Carrier Transport through the Interfacial Oxide

4.1 Introduction

In the previous chapter, we examined the problems hampering applications of polysilicon SIS emitters in Si concentrator solar cells. It then comes to a question. Can the polysilicon-contacted emitter be improved to the level that both low J_o and ρ_c can be obtained simultaneously? To answer such a question, we need a more quantitative analysis of the carrier transport across the interfacial oxide.

When the interfacial oxide is intact, the carriers can pass through the interfacial oxide only by tunneling or thermionic emission. In either case the carrier transport is uniform across the whole contact, and can be characterized by the carrier transmission probability across the interfacial oxide. Under such a condition, the specific contact resistivity can be expressed as a function of the majority carrier transmission probability, and the emitter saturation current density in terms of the minority carrier transmission probability. These are derived in Section 4.2.

To complete the analysis of carrier transport across an intact oxide, the transmission probability of both electrons and holes is also needed. However, because the detailed structure of a very thin oxide is not clearly understood, a rigorous derivation of the transmission probability is impossible. Consequently, the carrier

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transmission probability can be obtained only from experiments. Very few experiments have reported on the carrier transmission, and significant discrepancies among the results are found. In addition, some other concerns are also discussed.

When the interfacial oxide is broken, the carrier transport shows a completely different characteristic [48]. This is attributed to the epitaxial realignment of the polysilicon to the substrate in the broken region. For majority carrier transport, the broken region represents a highly conductive channel through the interfacial oxide. Naturally, most current tends to flow through the channel, and the resistance along the channel determines the specific contact resistivity. Similarly, because minority carriers are free to enter the polysilicon region through the channel, the recombination via this process cannot be ignored. Section 4.3 is dedicated to a more detailed analysis of these effects.

4.2 Carrier Transport through an Intact Interfacial Oxide

4.2.1 Derivations of J_o and ρ_c

To see the effect of the interfacial oxide on the minority carrier transport, we can evaluate the difference in the minority carrier flux into the polysilicon emitter before and after the insertion of the interfacial oxide. For simplicity, an n-type polysilicon SIS emitter is used in the following analysis. The same results, however, apply to the p-type polysilicon SIS emitter by replacing the appropriate parameters. Consider an n-type polysilicon SIS emitter shown in Figure 4.1 where the interfacial oxide imposes an energy barrier in the valence band. Assuming that recombinations in the monosilicon emitter region and at the monosilicon interface are negligible. Then the hole current density flowing into the emitter is determined by how fast the recombination takes place in the polysilicon region. This can be expressed as the product of the hole transport velocity in the polysilicon, S_h, and the hole density

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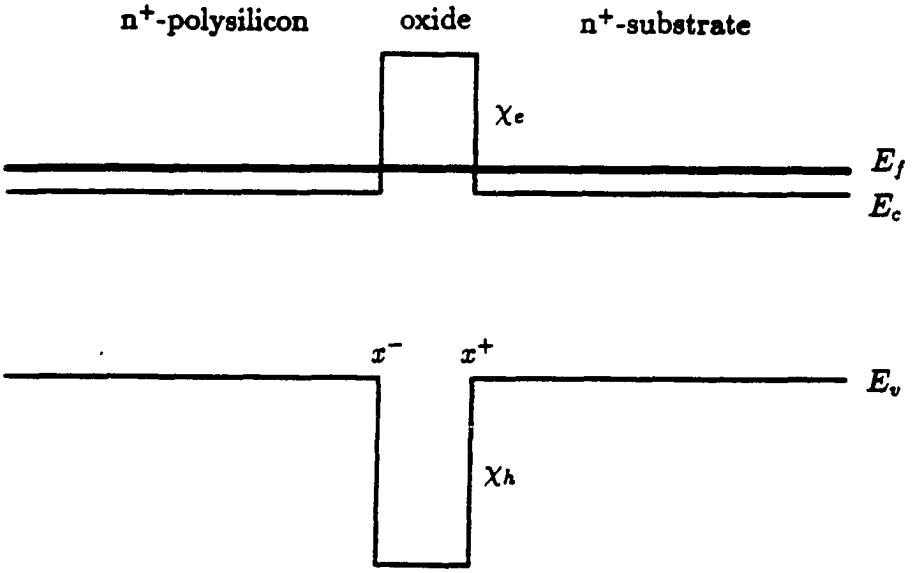

Figure 4.1: A simplified band diagram for an n-type polysilicon SIS emitter.

at the interface, p_{x^-},

$$J_h = J_{os}\left(\exp[\frac{q\phi_p(x^-)}{kT}] - 1\right) = q\ S_h\ (p_{x^-} - p_{no}) \sim q\ S_h\ p_{x^-}; \tag{4.1}$$

where J_{os} is the saturation current density of a "pure" polysilicon emitter (J_{os} in Figure 3.3), p_{no} is the equilibrium hole density, and $\phi_p(x^-)$ is the hole quasi-Fermi level at x^-.

When there is no interfacial oxide, p_{x^-} is the same as p_{x^+} so that J_h can be written as

$$J_h = J_{os}\left(\exp[\frac{q\phi_p(x^+)}{kT}] - 1\right); \tag{4.2}$$

On the other hand, when the interfacial oxide exists, the relationship between p_{x^-} and p_{x^+} can be derived by applying the continuity condition at x^-. Assuming that T_h is the hole transmission probability across the interfacial oxide and v_h is the hole mean velocity in both the polysilicon and the monosilicon, then the net hole current density injected into the polysilicon is

$$J_h(x^-) = \frac{1}{4} q\ v_h\ T_h\ (p_{x^+} - p_{x^-}). \tag{4.3}$$

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For the continuity condition to hold at x^-, $J_h(x^-)$ has to be equal to the recombination in the polysilicon region,

$$J_h(x^-) = q\ S_h\ p_{x^-}, \tag{4.4}$$

$$\frac{1}{4} q\ v_h\ T_h\ (p_{x^+} - p_{x^-}) = q\ S_h\ p_{x^-}; \tag{4.5}$$

thus,

$$p_{x^-} = \frac{p_{x^+}}{1 + \frac{4\ S_h}{T_h\ v_h}}. \tag{4.6}$$

Substituting this into Eqn. (4.1), the saturation current density of the polysilicon SIS emitter, caused by tunneling, is

$$J_{o,tun} = \frac{J_{os}}{1 + \frac{4\ S_h}{T_h\ v_h}}. \tag{4.7}$$

In the derivations above, it should be noted that we ignored recombination in the monosilicon region and at the oxide interface on the substrate side. While the first can always be made negligible by limiting the dopant outdiffusion, the recombination at the oxide interface may be appreciable. Since the recombination at the oxide interface is independent of that by the tunneling process [3], the J_o of a polysilicon SIS emitter is simply the sum of these two terms.

$$J_o = J_{ox} + J_{o,tun} = J_{ox} + \frac{J_{os}}{1 + \frac{4\ S_h}{T_h\ v_h}}; \tag{4.8}$$

where J_{ox} denotes the contribution from the interface recombination.

For the majority carrier transport, the relation between the ρ_c and the majority carrier transmission probability can be derived based on the definition of the ρ_c. This has been done by Kwark [7]. ρ_c can be defined as the derivative of the potential drop across an interfacial oxide with respect to the current density which is kept close to zero, thus

$$\rho_c = \left(\frac{\Delta V}{\Delta J}\right)_{J \to 0}; \tag{4.9}$$

where ΔV is the potential drop across the interfacial oxide, and ΔJ is the net current density that flows through the interfacial oxide. With the potential drop ΔV across

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the interfacial oxide, the net current density can also be expressed as

$$\begin{aligned} \Delta J &= qN\frac{v_e}{4}T_e\left[\exp(\frac{q\Delta V}{kT}-1\right] \\ &\sim qN\frac{v_e}{4}T_e\left(\frac{q\Delta V}{kT}\right), \text{ for } \Delta V < \frac{kT}{q} \end{aligned} \tag{4.10}$$

where v_e is the mean electron velocity, and N is the majority carrier density. Combine Eqn. (4.9) and (4.11),

$$\rho_c = \frac{kT}{qN}\frac{4}{v_e}\frac{1}{T_e}. \tag{4.11}$$

4.2.2 Discussions: Can a polysilicon SIS emitter with Intact Interfacial Oxide Be Useful?

Theoretically, it is possible to make a polysilicon SIS emitter with an intact interfacial oxide having low J_o and "acceptable" ρ_c simultaneously. This can be seen from Eqns. (4.8) and (4.11). The maximum T_h allowed for an emitter with given J_o can be estimated by assuming that J_{ox} is negligible. Under such a condition, T_h has to be less than 4×10^{-4} in order for the polysilicon SIS emitter to have J_o about 1×10^{-14} A/cm^2. Assuming that J_{os} is 1×10^{-12} A/cm^2 [21], S_h is 1×10^5 cm/sec [41], and v_h is 1×10^7 cm/sec [7]. To calculate T_e, we assume that the carrier density is 1×10^{20} cm^{-3}, and v_e is 1×10^7 cm/sec. Substituting these into Eqn. (4.11), it shows that T_e has to be higher than 6×10^{-6} in order to have ρ_c less than 1×10^{-4} Ω-cm^2. Thus, an n-type polysilicon SIS emitter can be useful if it falls between $T_e \geq 6 \times 10^{-6}$ and $T_h \leq 4 \times 10^{-4}$. Conversely, if the transport of holes is more or less the same as that of electrons, similar window may exist for a p-type polysilicon SIS emitter too. As a result, the whole problem comes down to the question—whether or not such a window exists.

There are two ways that carriers can pass an energy barrier; one is by thermionic emission, and the other is by tunneling. For a given barrier height χ, and width t, the transmission probability is

$$T_t = \exp\left(-\frac{\chi}{kT}\right), \tag{4.12}$$

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if the thermionic process dominates, or

$$T_t = \exp(-\sqrt{\chi}\, t), \tag{4.13}$$

if the tunneling process dominates. To have the right magnitude, χ is in units of eV and t in Å. Although both equations are approximate, they are the ones used in extracting the χ or the transmission probability in practice. Any corrections of equations are absorbed in the unknown parameter, χ. In general, χ can be roughly thought of as the band discontinuity between the silicon and the oxide.

When the oxide is very thin, the carrier transport is likely dominated by tunneling. Under such a condition, different combinations of J_o and ρ_c can be obtained by varing the oxide thickness. Thus, a polysilicon SIS emitter is useful for solar cells relies on whether there is a range of oxide thickness (oxide-thickness window) that results in both low J_o and ρ_c. However, to find the right oxide-thickness window, we also need to know the magnitude of χ. It has been known that, χ for a very thin oxide is lower than that for a thick oxide and varies with the oxide thickness. Such anomalous phenomena are not clearly understood, and usually are attributed to the non-stoichiometric composition of the thin oxide [17,49]. A similar non-stoichiometric transition layer at the Si-SiO_2 interface was also reported for thick oxide [50,51,52], which seems to support the concept. In particular, Lewicki and Maserijian [52] reported that the oxide conduction band edge is not abrupt at the Si-SiO_2 interface; instead, it gradually increases with the oxide thickness and does not attain the value of a thick oxide until the the oxide is more than 65 Å thick.

For the oxide thinner than 20 Å, the carrier transmission probability has been studied by Kasprzak *et al.* [49] in great detail. To determine χ, they measured the I-V characteristics of a metal-oxide-silicon (MIS) structure of which silicon is heavily doped to either n or p type. Assuming that the tunneling process is dominant, there will be a sudden slope change in tunneling I-V at the applied voltage equals the barrier height χ. The abrupt change in the slope is attributed to the fact that the potential barrier changes from a trapezoid to a triangle. For the applied voltage $V \leq \chi$, the barrier width is constant, and the applied voltage dependence of the transmission probability comes from the barrier-height-lowering effect alone.

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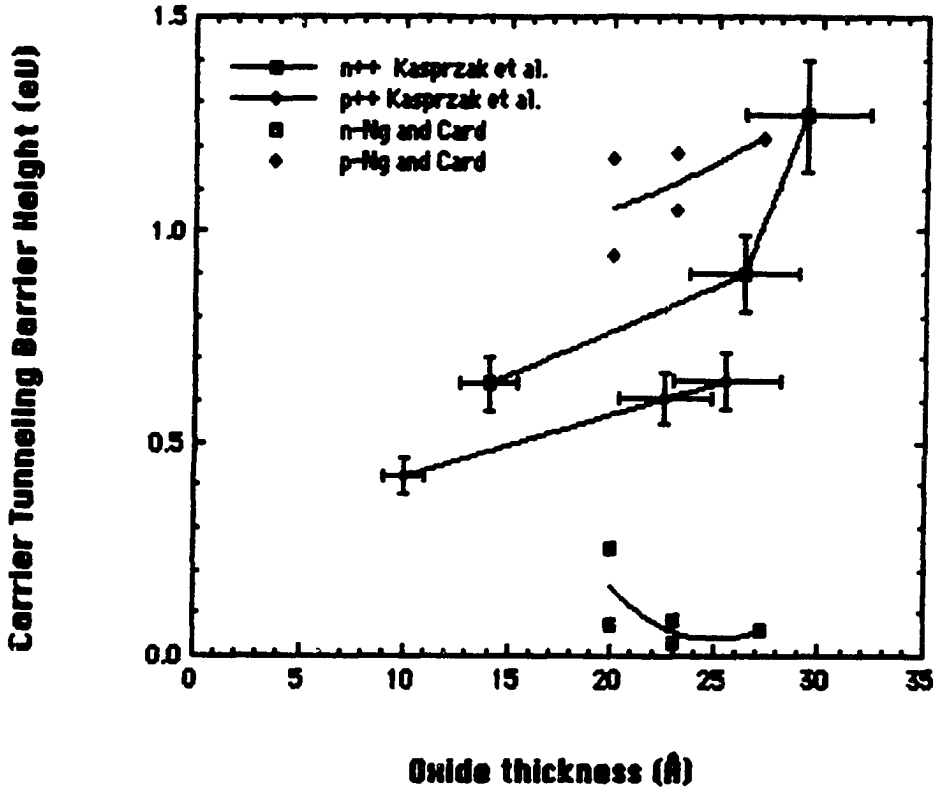

Figure 4.2: The tunneling barrier height versus the oxide thickness.

Conversely, both barrier height and width are affected by the applied voltage when the applied voltage $V \geq \chi$. The barrier height determined with this method is summarized in Figure 4.2.

In the same range of oxide thickness, the χ was also reported by Ng and Card [53] on the similar structure except that, in their devices, the silicon is lightly doped. They determined the carrier transmission probability with an n-type Schottky-barrier diode, on which a very thin oxide is grown before the metal deposition. The electron transmission probability was determined from the diode I-V characteristics. In contrast, the hole transmission probability was determined by the suppression of the photocurrent. Their results are also shown in Figure 4.2. For the electron barrier height, their results are considerably lower than those of Kasprzak's. On the other hand, the hole tunnel barrier height, as shown in Figure 4.2, is much higher than that of Kasprzak's. With such a wide discrepancy in the tunnel barrier height, it is impossible to find out the oxide-thickness window.

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For the n-type, it seems that Ng's results are too small to be correct. This can be seen from the ρ_c predicted with their tunnel barrier height in comparison with the ρ_c measured by Crabbé. Ng's results fail in predicting the right magnitude of ρ_c. However, the ρ_c calculated with Kasprzak's n-type results appears very close to that reported by Crabbé. From the figure, T_e is derived to be 6×10^{-6} for a 15 Å oxide, which is about the thickness of a chemically-grown thin oxide. Substituting it into Eqn (4.11) and assuming that the majority carrier density is 1×10^{20} cm^{-3}, v_e is 1×10^7 cm/sec, then ρ_c is $\sim 1.2 \times 10^{-4}$ Ω-cm^2, which is quite close to what was measured ($\sim 2 \times 10^{-4}$ Ω-cm^2). Unfortunately, the significant discrepancy of the p-type cannot be justified because no available data exists like that of the n-type case.

In practice, there is another difficulty we may have to face if the tunnel barrier height is around the range shown in Figure 4.3. Figure 4.3 is the transmission probability of both electrons and holes plotted with the tunneling barrier height reported by Kasprzak *et al.*. As shown in the figure, for the T_h and T_e specified in the beginning of this section, it corresponds to an oxide-thickness window 15±2 Å. With a window so narrow, it is not possible to have good control over the characteristics of a polysilicon SIS emitter.

4.3 The ρ_c and J_o for a Broken Interfacial Oxide

4.3.1 Derivations

As the interfacial oxide breaks up, the polysilicon has a tendency to realign epitaxially with the substrate underneath (see Figure 3.11). The realignment offers a highly conductive channel through the interfacial oxide; consequently, the contact resistance can be drastically reduced. More specifically, this can be seen from the following analysis. The equivalent resistivity in the unbroken region can be estimated by dividing the ρ_c by the oxide thickness. For a 15 Å thick oxide, the ρ_c has been calculated to be 1.2×10^{-4} Ω-cm^2; thus, the corresponding resistivity is 800 Ω-cm. If the resistivity in the broken region is the same as that of the bulk

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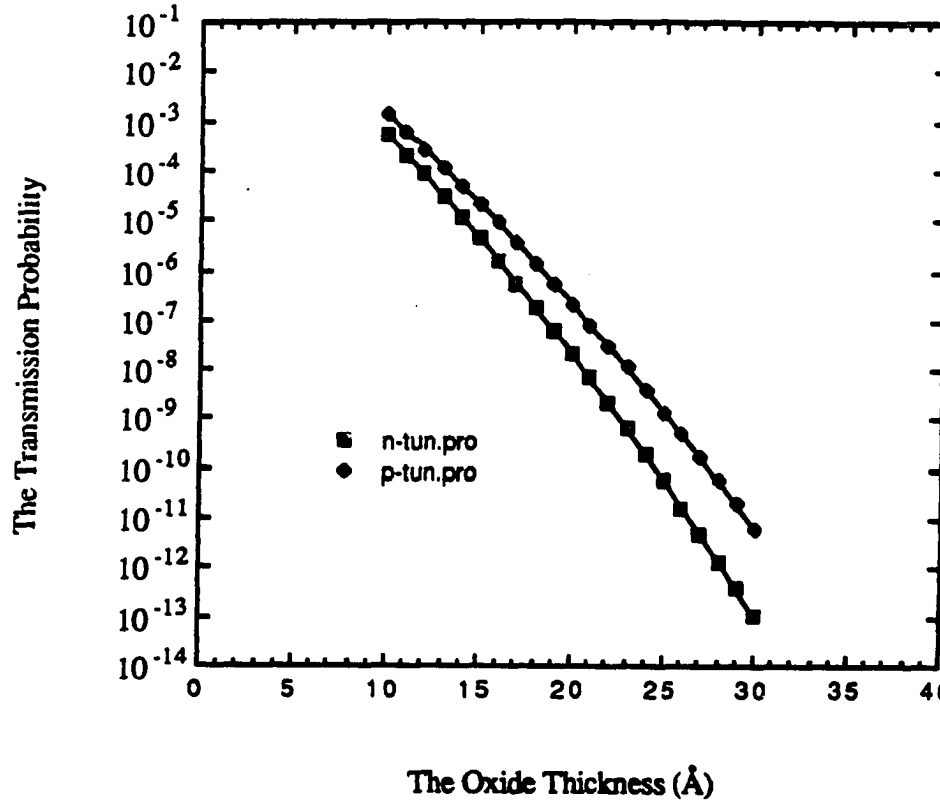

Figure 4.3: The transmission probability of electrons and holes.

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resistivity of the emitter ($\sim$ 5 mΩ-cm), then the resistivity in the broken region is about five orders of magnitude lower than that of the unbroken region. With such a huge difference in resistivity, current tends to flow through the channel instead of tunneling through the unbroken region. When most current is flowing through the broken regions, it is the resistance along the channel that determines the specific contact resistivity ρ_c.

With a few assumptions, the ρ_c can be expressed explicitly in terms of the oxide broken areal fraction and the other related parameters. First, we assume that the current flows only through the broken region because of the huge difference in the resistivity mentioned above. Under such a condition, the emitter contact behaves like a multi-spot contact which has been discussed by Holm [54]. The specific contact resistivity of the multi-spot contact consists of two terms. One is the spreading resistance caused by the gradual increase of the current density as the current flows toward the broken region. The other is the resistance imposed by the channel through the interfacial oxide (the broken region) which has been used to demonstrate the low ρ_c of a broken interfacial oxide in Chapter 1.

The first term can be derived following Holm [48]. Figure 4.4a is the top-view of the interfacial oxide of an circular emitter contact. The shaded circles represent the broken spots where polysilicon forms contact with the substrate intimately. The spreading resistance at each spot i, on polysilicon side, can then be expressed as [54],

$$R_i = \frac{\rho_{poly}}{\pi d_i} \tan^{-1}\left[\frac{\sqrt{l_i^2 - d_i^2}}{d_i}\right]. \tag{4.14}$$

As shown in Figure 4.4b, ρ_{poly} is the resistivity of the polysilicon, l_i is the diameter of the equal-potential surface projected at the interfacial oxide plane, d_i is the diameter of the broken region, and $\sqrt{l_i^2 - d_i^2}$ is the height of the equal-potential surface. A similar expression for the spreading resistance on the substrate side can be obtained by replacing the polysilicon resistivity with that of the substrate.

As long as the spacing between any two neighboring spots is much larger than the diameter of the spot, they can be treated as two parallel resistors. Thus, the

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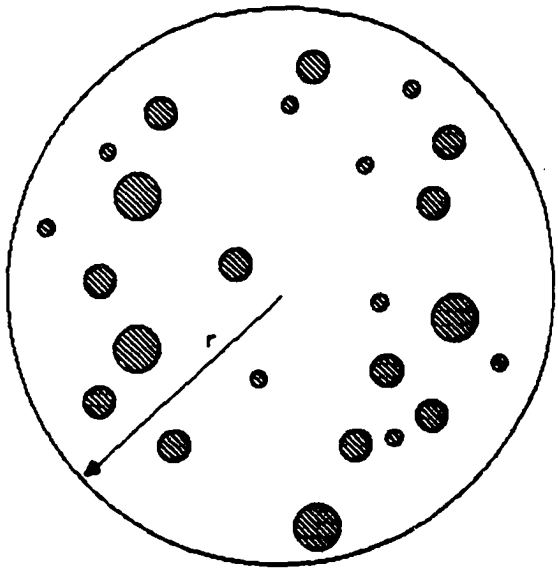
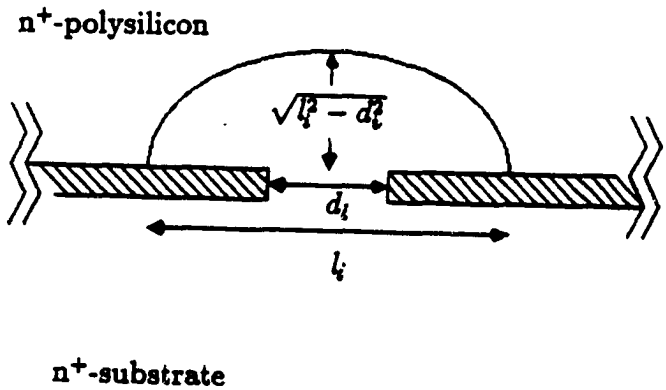


(a)



(b)

Figure 4.4: (a) the top-view of a broken interfacial oxide, (b) the equal-potential surface in the vicinity of a circular broken spot.

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total spreading resistance for a multi-spot contact is

$$R = \left(\sum_i \frac{1}{R_i}\right)^{-1} = \frac{\rho_{poly}}{\pi}\left(\sum_i \frac{d_i}{\tan^{-1}\left(\frac{\sqrt{l_i^2-d_i^2}}{d_i}\right)}\right)^{-1}; \tag{4.15}$$

Assuming that the spacing between two broken spots, l, is of equal distance, and the diameter of each spot, d, is identical, the equation can be further simplified to

$$R = \frac{(\rho_{poly}+\rho_{sub})\,l^2}{4\,A_r\,d}\tan^{-1}\left(\frac{\sqrt{l^2-d^2}}{d}\right); \tag{4.16}$$

where A_r is the total area of the emitter contact. Note that Eqn. (4.16) has accounted for the spreading resistance from both the polysilicon and the substrate side. In addition, the spreading resistance expressed in Eqn. (4.16) does not completely result from the existence of the interfacial oxide. It also includes the bulk resistance which exists even there is no interfacial oxide. Subtracting this out, the excess resistance caused by the small contact areal fraction is

$$R' = \frac{(\rho_{poly}+\rho_{sub})}{4\,A_r}\left[\frac{l^2}{d}\tan^{-1}\left(\frac{\sqrt{l^2-d^2}}{d}\right) - K\sqrt{l^2-d^2}\right]; \tag{4.17}$$

where K is a constant (~ 1) that makes R' approach 0 as $d \to l$. Take $K = 1$ and multiply both sides with the total contact area A_r, the equation becomes

$$\rho_{c,spread} = (R')A_r \sim \frac{(\rho_{poly}+\rho_{sub})}{4}\left[\frac{l^2}{d}\tan^{-1}\left(\frac{\sqrt{l^2-d^2}}{d}\right) - \sqrt{l^2-d^2}\right]. \tag{4.18}$$

$\rho_{c,spread}$ denotes the component of the specific contact resistivity caused by the spreading resistance. In reality, an additional error may arise because the current is not uniform across the entire emitter contact; *i.e.*, more current flows through the broken spots that are closer to the rim of the emitter contact. However, this effect only causes an error of up to 20% when the broken spots are very close to each other [54]. Under the assumption that the interfacial oxide is broken uniformly, $(\frac{d}{l})^2$ also represents the total broken areal fraction x_b. Thus, the equation above can also be expressed as

$$\rho_{c,spread} = \frac{(\rho_{poly}+\rho_{sub})\,d}{4}\left[\frac{\tan^{-1}\left(\sqrt{\frac{1-x_b}{x_b}}\right)}{x_b} - \sqrt{\frac{1-x_b}{x_b}}\right]. \tag{4.19}$$

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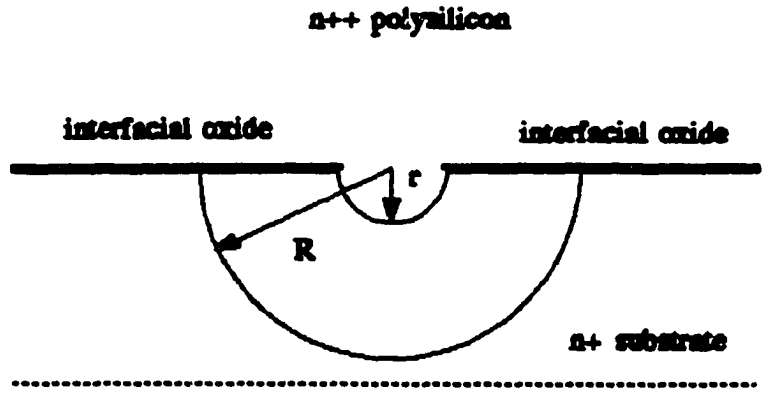

Figure 4.5: The emitter region around a broken spot.

Similarly, the channel resistance contribution to the ρ_c is

$$\rho_{c,channel} = w\,\frac{(\rho_{poly}+\rho_{sub})}{2}\left[(\frac{1}{T_{ref}})\frac{1}{x_b}-1\right]; \tag{4.20}$$

where w is the channel length which can be approximated with the oxide thickness, and the resistivity in the channel is assumed to be the average of the polysilicon and the substrate around the broken region. The constant T_{ref} (≤ 1) in the equation accounts for the possible carrier reflection at the junction between the channel and the rest of the bulk. The carrier reflection may occur due to the dopant segregation or the quantum effect of a very narrow channel. The ρ_c is then the sum of Eqn. (4.19) and (4.20),

$$\begin{aligned}\rho_c &= \rho_{c,spread}+\rho_{c,channel}\\ &= \frac{(\rho_{poly}+\rho_{sub})}{4}\\ &\quad\left\{d\left[\frac{\tan^{-1}\left(\sqrt{\frac{1-x_b}{x_b}}\right)}{x_b}-\sqrt{\frac{1-x_b}{x_b}}\right]+2w\left[(\frac{1}{T_{ref}})\frac{1}{x_b}-1\right]\right\}\end{aligned} \tag{4.21}$$

When the interfacial oxide is broken, the calculation for J_o appears to be simple. Figure 4.5 shows the emitter around a broken spot. The hole current flown into the polysilicon can be expressed as

$$I_p = 2\pi r^2\, q\, S_h\, n_r; \tag{4.22}$$

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where n_r is the hole density at the radius r, and S_h is the hole transport velocity in the polysilicon. The equation in fact overestimates the hole current by assuming larger collection area ($2\pi r^2$ instead πr^2). Assuming that the recombination, except in the broken region, is negligible for the entire emitter, then the minority carrier density outside the hemisphere of R can be treated as a constant. Inside, a gradient of the hole density develops in order to support the hole current flowing into the polysilicon. The hole current density at R is

$$J_p = \frac{I_p}{2\pi(R)^2} = qD_p\left(\frac{dp}{dx}\right)_R \sim qD_p\left(\frac{n-n_r}{R-r}\right); \tag{4.23}$$

where D_p is hole diffusivity in the n^+-emitter region. With Eqns (4.22) and (4.23), n_r can be expressed in terms of n.

$$n_r = \frac{n}{1+(\frac{r}{R})^2\frac{S_h}{D_p/(R-r)}}. \tag{4.24}$$

Thus,

$$I_p = 2\pi r^2\, q\, S_h \frac{n}{1+(\frac{r}{R})^2\frac{S_h}{D_p/(R-r)}}. \tag{4.25}$$

If we take R as half of the spacing between two broken spots, and r as half of d, then the equivalent J_o of the emitter is

$$\begin{aligned} J_o &= x_b\, q\, S_h\, n_o \frac{1}{1+\frac{2x_bS_h}{D_p/(l-d)}} \\ &= \frac{x_b\, J_{os}}{1+\frac{2x_bS_h}{D_p/(l-d)}}; \end{aligned} \tag{4.26}$$

Similar equation can be found for the p-type emitter by replacing the subscript h (p) with e (n). The denominator of the equation represents the crowding effect, or in another words, the reduction of the minority carrier density in front of the channel. For small x_b, we can add the term J_{ox} into above equation and neglect the crowding effect,

$$J_o \sim J_{ox}(1-x_b) + J_{os}\, x_b. \tag{4.27}$$

From the Gummel plots shown in Figure 3.11, the J_o of the 950 °C-sample is 1×10^{-13} A/cm^2. The corresponding broken areal fraction estimated in the same report is 10%. The J_o measured is very close to what expected from the equation if we assume $J_{os} = 1\times10^{-12}$ A/cm^2 as shown in Figure 3.3.

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4.3.2 Discussion

Before showing the result of Eqn. (4.21), it is important to see how much error can result from the uncertainty of T_{ref}. As mentioned earlier, T_{ref} accounts for the the possible carrier reflection at the junction between the channel and the rest of the bulk. This may occur due to the dopant segregation or the quantum effect of a very narrow channel. Since the resistivity of a heavily doped polysilicon is at most a factor of two higher than that of a monosilicon, it is likely that the effect caused by the dopant segregation is negligible. The quantum reflection occurs if the electronic states in the channel are distorted as the channel becomes narrower. Because of the mismatch between the states inside and the states outside the channel, carriers cannot propagate the way they do in the bulk. In that case, the carrier transport across the channel can be thought as a tunneling process, with the energy barrier set by the energy spacing between two adjacent states along the transverse direction ($\Delta E_{\perp}$). Assuming a free-electron model, and a channel width (the diameter of the broken region) and a channel length (the oxide thickness) of 50 and 15 Å respectively, then the energy spacing $\Delta E_{\perp}$ is

$$\Delta E_{\perp} = \frac{\pi^2 \hbar^2}{2 m_e d^2} \sim 15 \text{ meV};$$

and,

$$T_{ref} \sim \exp\left[-\sqrt{\Delta E_{\perp}}\, w\right] \sim 0.16$$

which shows that $\rho_{c,channel}$ may increases by a factor about 5 because of the quantum reflection. Apparently, the quantum effect will be significantly less when the broken size is larger than 100 Å. Nevertheless, such a quantum effect is incorporated in the results presented below. Strictly speaking, if the tunneling process is the transport mechanism for carriers to propagate through the channel, it is more appropriate to use Eqn. (4.11) to estimate $\rho_{c,channel}$. Nevertheless, we keep the form of Eqn. (4.21) because the quantum effect may not be significant in most cases.

Figure 4.6 is the ρ_c versus x_b generated with Eqn. (4.21). The parameters used in the equation are: d = 100 Å, ρ_{poly} = 5 mΩ-cm, w = 15 Å, and ρ_{sub} = 5 or 50 mΩ-cm. As shown in the figure, ρ_c deceases more rapidly at small x_b ($\leq$5%).

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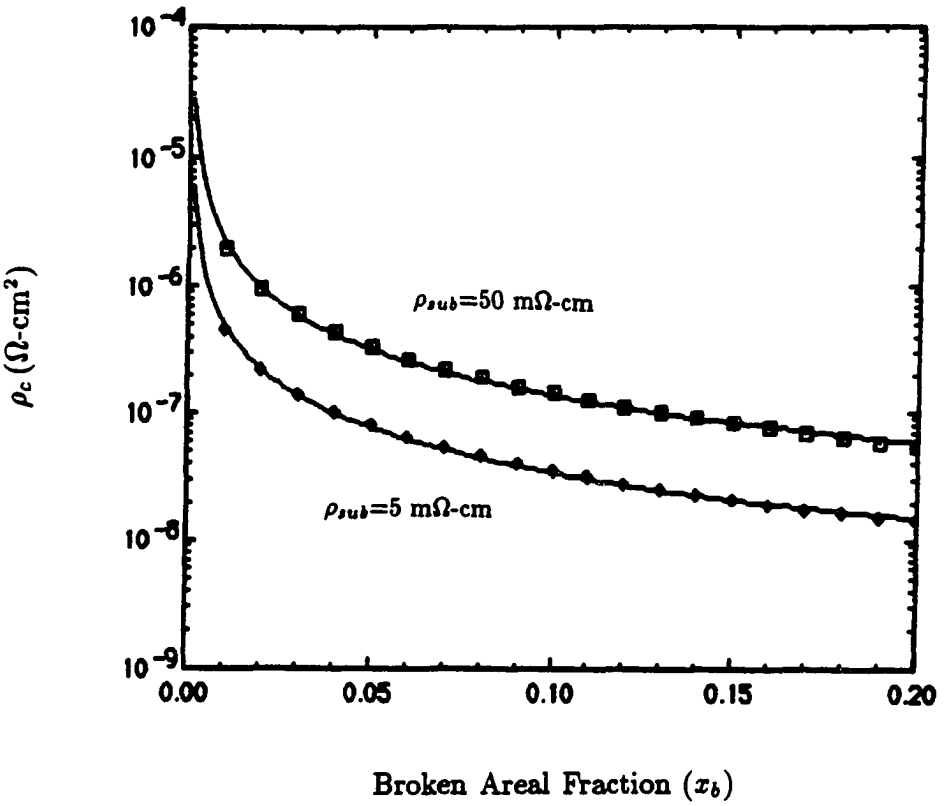

Figure 4.6: ρ_c versus x_b. Two curves are shown with ρ_{sub} of 5 and 50 mΩ-cm respectively. The rest of parameters are: $d = 100$ Å, $\rho_{poly} = 5$ mΩ-cm, $w = 15$ Å.

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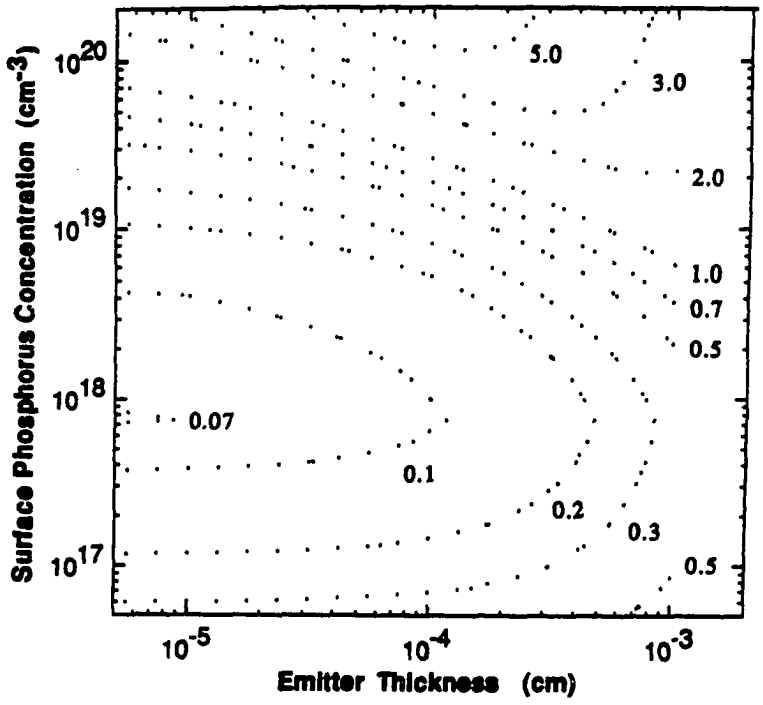

Figure 4.7: Contours of constant J_o for oxide-passivated emitters. The contours are labeled with the value of J_o in units of 10^{-13} A/cm^2.

As mentioned earlier, such a steep drop signifies a drastic change of the resistance across the oxide once the oxide is broken. The two curves show the effect of surface dopant concentration of the substrate. Although high surface concentration offers lower ρ_c it raises the surface recombination velocity, which in turn increases the J_o as well [55]. Figure 4.7 shows the J_o plotted as the function of surface phosphorus concentration and emitter thickness for oxide-passivated emitters. Note that there is significant dependence of J_o on the surface concentration for concentrations higher than 1×10^{18} cm^{-3}. Since both cases, with very small x_b, are capable of having low enough ρ_c for concentrator solar cells, it is beneficial to keep a low surface concentration in order to minimize the surface recombination velocity. For ρ_{sub} = 5 mΩ-cm, ρ_c has dropped to less than 1×10^{-7} Ω-cm^2 before x_b reaches 5%. However, it is still higher than the preliminary estimation given in Chapter 1. This is because we did not include the contribution of the other term in the estimation.

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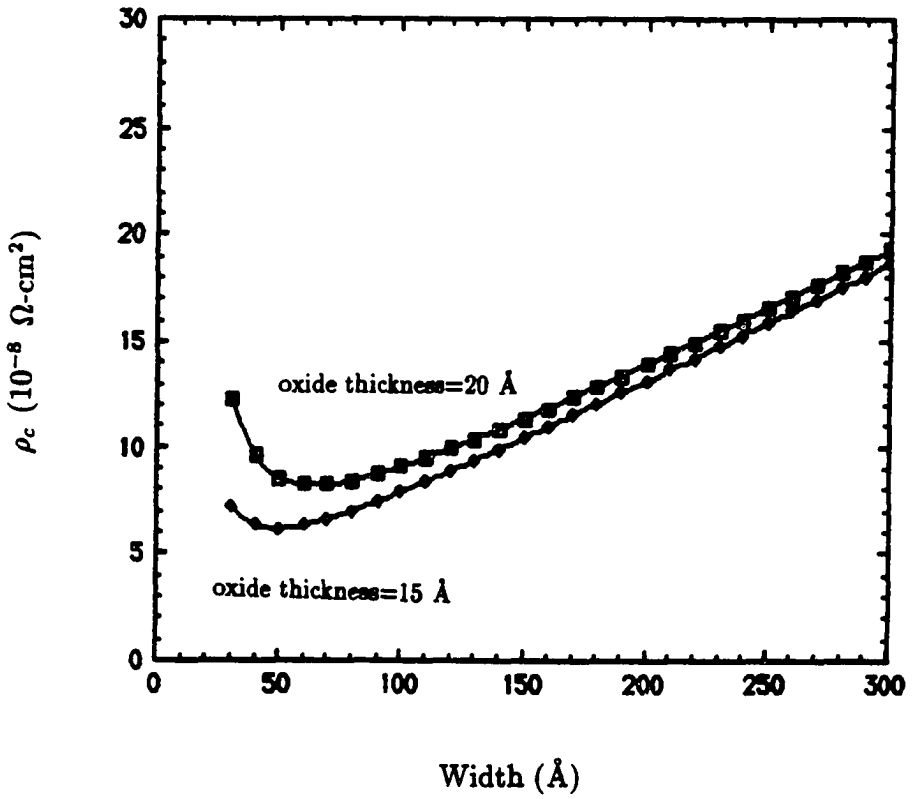

Figure 4.8: ρ_c versus x_b. Two curves are shown with oxide thickness of 15 and 20 Å respectively. The rest of parameters are: $x_b = 5\%$, $\rho_{poly} = \rho_{sub} = 5$ mΩ-cm.

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Eqn. (4.21) for ρ_c consists of two terms; one is from the spreading resistance, the other is from the channel resistance. Because only the first term depends on the broken size, it is expected that a minimum in ρ_c will be seen when the ρ_c is plotted as a function of the broken size, d. This is shown in Figure 4.8. The parameters used to generate those two curves are: $x_b = 5\%$, $\rho_{poly} = \rho_{sub} = 5$ mΩ-cm, and $w = 15$ or 20 Å. The left-hand side of both curves is dominated by the term from the channel resistance; therefore, it increases as d decreases, partly due to the incorporation of the quantum effect. In contrast, it is the term from the spreading resistance that dominates the right-hand side of the curves. By the time that $d = 100$ Å, ρ_c has reached 1×10^{-7} Ω-cm^2, which explains the higher-than-expected ρ_c shown in the previous figure. In this regime, the effect of the oxide thickness is negligible too. This is drastically different from the case of the intact oxide, in which both ρ_c and J_o are plagued by a sensitive dependence on the oxide thickness. Consequently, the immediate benefit of the oxide breakup is clearly seen in this case.

Instead of expressing ρ_c as a function of x_b, let us see what happens when ρ_c is plotted against J_o. This is shown in Figure 4.9, in which both ρ_c and J_o are regulated by x_b [48]. The parameters used in Eqns. (4.21) and (4.27) are $J_{os} = 1 \times 10^{-12}$ A/cm^2, $\rho_{poly} = \rho_{sub} = 5$ mΩ-cm, $d = 100$ Å. Two curves are shown in the figure: one with J_{ox}=2×10^{-14} A/cm^2, the other with J_{ox}=5×10^{-14} A/cm^2. As shown in the figure, two distinct regimes are observed on both curves. On the left-hand side, ρ_c drops dramatically while J_o is almost constant. Compared with Figure 4.6, the steep drop of ρ_c is intensified. This can be attributed to the fact that, when x_b is very small, J_{ox} dominates J_o as shown in Eqn. (4.27). Apparently, J_o will be "linearly" proportional to J_{ox} in this regime because of the J_{ox} dominance. Such a proportionality is shown by the shift of the curve with J_{ox} =5×10^{-14} A/cm^2 away from the curve with J_{ox} =2×10^{-14} A/cm^2. As shown in Figure 4.7, such a change can be induced simply by the fluctuation of the surface concentration from 1 to 3×10^{19} cm^{-3} (for the n-type emitter), which also points out the importance of the dopant drive-in process. That J_o is relatively insensitive to the change of ρ_c is remarkable because it marks a region in which ρ_c is independent of J_o. Compared with the case that the intact oxide is kept intact, this is another advantage.

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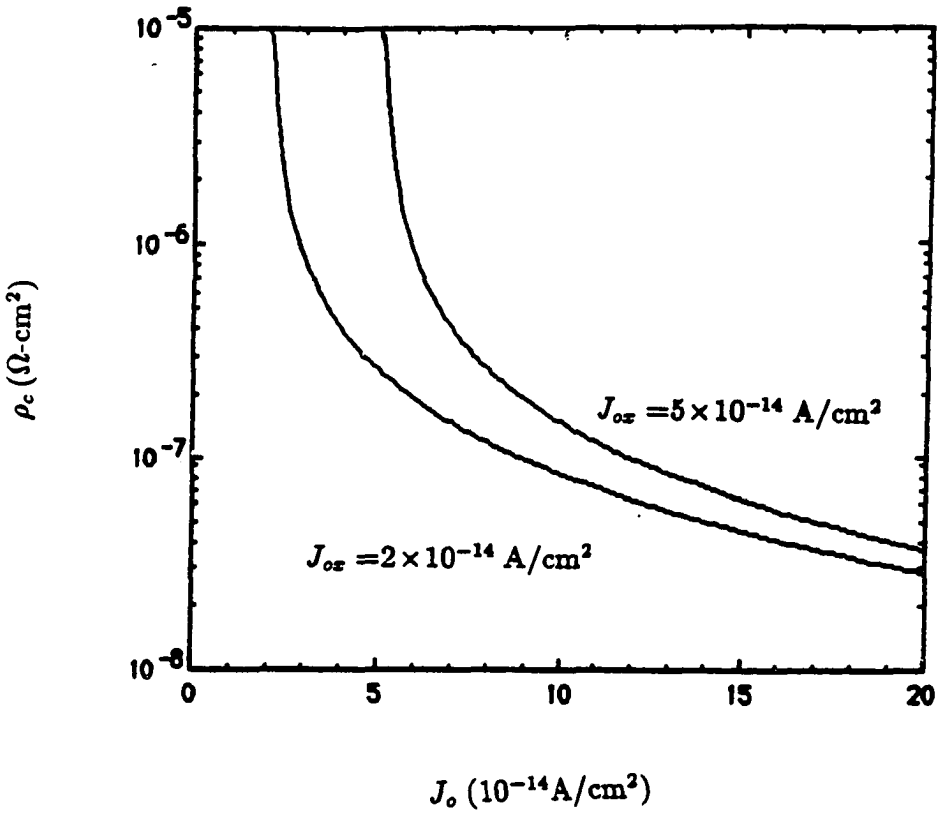

Figure 4.9: Simulated ρ_c versus J_o. Two curves are shown with J_{ox} of 2×10^{-14} and 5×10^{-14} A/cm^2 respectively. The rest of parameters are: $J_{os} = 1 \times 10^{-12}$ A/cm^2, $\rho_{poly} = \rho_{sub} = 5$ mΩ-cm, $d = 100$ Å.

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4.4 Conclusions

In this chapter, we have derived the carrier transport mechanisms through an interfacial oxide for both minority and majority carriers. When the interfacial oxide is intact, the carrier transport is determined by tunneling. Despite the great uncertainty of the transmission probability, it appears that a useful polysilicon SIS emitter with intact interfacial oxide is difficult to make. When the interfacial oxide is broken, the majority carrier transport mechanism is dominated by the series resistance imposed by the broken region. With a few percentages of the interfacial oxide being broken, the ρ_c will be negligible for the application in concentrator solar cells. Under such a condition, there is a regime in which the J_o will not be affected by the oxide breakup because it is dominated by the recombination at the oxide interface. Thus, it is possible for polysilicon SIS emitter to have both low J_o and ρ_c.

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Chapter 5

Experimental

5.1 Introduction

From the discussion in the previous chapter, there is a great chance to make a polysilicon SIS emitter with both low J_o and ρ_c by breaking a very small fraction of the interfacial oxide. In this chapter, we shall show, experimentally, that this is indeed the case.

In the next section, we first introduce the photoconductivity decay measurement which was used in most of our experiments to derive the J_o of a polysilicon SIS emitter. One of the advantages of this method is that the sample preparation is much simpler than making a bipolar transistor. In addition, the measurement of J_o is freed from the possible interference of high contact resistance. Such high emitter contact resistance usually makes both the collector and the base current of the bipolar transistor nonideal. As a result, it is more difficult to obtain J_o from such a device.

In Section 5.3, we examined the polysilicon SIS emitter with a chemically grown oxide in the attempt to understand the recombination at the oxide interface [56]. It is important because it is the one being reported that can be broken during a high temperature anneal. If the interface quality is shown to be good enough, the task of finding a suitable processing technique of making polysilicon SIS emitters of both types with low J_o and ρ_c will be simplified. Unfortunately, the results show that

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the interface quality of the chemical oxide is not good enough to make the p-type polysilicon SIS emitter with low J_o.

Section 5.4 reports the results of the polysilicon SIS emitter with a thermally grown interfacial oxide. It appears that the quality of the interfacial quality is much better than that of the chemical oxide. A low J_o ($\sim 1 \times 10^{-14}$ A/cm^2) has been observed on polysilicon SIS emitters of both types.

With this interfacial oxide of good quality found, the task is then reduced to seeing if the oxide can be broken controllably. To break the oxide without causing too much dopant outdiffusion, we use two steps of high temperature anneal. The first anneal, which is intended to break the interfacial oxide, is performed at higher temperature. The dopant is then introduced in the second anneal, for which the temperature is lower. Such a two-step anneal technique was first used to make p-i-n diodes. The results, which are shown in Section 5.5, strongly suggest that the two-step anneal technique worked. Thereafter, more systematic experiments were carried out, and the results are shown in Section 5.6. When the experimental results are compared with those obtained from simulation, it shows that only a very small fraction of the interfacial oxide of polysilicon SIS emitters made in these experiments is being broken.

5.2 The Photoconductivity Decay Measurement

In the following experiments, the J_o of a polysilicon SIS emitter was measured with the photoconductivity decay method. The principles and the apparatus of such a measurement is described briefly in this section.

When a high resistivity silicon wafer is flashed with a light pulse, the wafer conductivity is modulated by the sudden increase and the subsequent decay of the excess carrier density caused by the recombination. Because of the simple relationship between the photoconductivity and the photo-excited carrier density, the recombination rate of the excess carriers can be obtained by monitoring the decay of the photoconductivity. In our experiments, the photoconductivity decay is measured by the set-up shown in Figure 5.1 schematically. The coupling between

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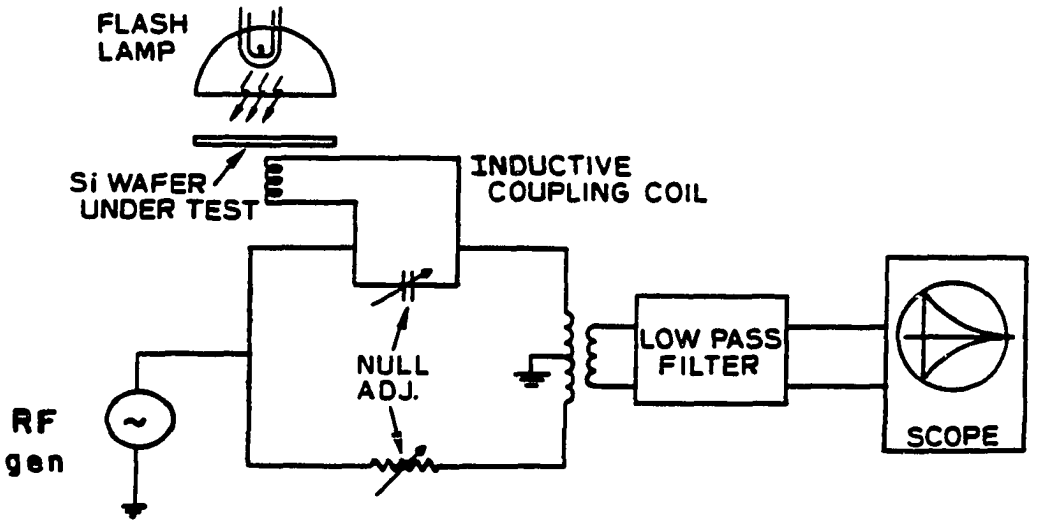

Figure 5.1: Apparatus used to determine J_o from photoconductivity decay measurement.

the silicon wafer and the coil, shown in the figure, changes as the conductivity of the silicon wafer varies. Such a change is reflected in the magnitude of the RF signal from the coil and can be recorded on an oscilloscope, where the data are then transferred to the computer for further analysis. In the actual measurement, the circuit is adjusted such that the subsequent change of the signal is a monotonic function of the wafer conductivity.

A typical decay curve is shown in Figure 5.2, in which the curve is the upper envelope of the signal recorded as a function of time. With a proper calibration, such a decay curve can be converted into the decay of the excess carrier density versus time, which is then used to find the recombination rate and the responsible recombination mechanisms as well. More detailed discussions of this method and its limitations can be found in Ref. [3,57].

The greatest advantage of this method is the simplicity of the sample preparation. The sample is a blank wafer deposited with polysilicon which is doped either n- or p- type. Typically, FZ wafers of long bulk lifetime are preferred. The recombination in such a sample consists of three terms; one is the emitter recombination at both surfaces, another is the bulk SRH recombination, and the other

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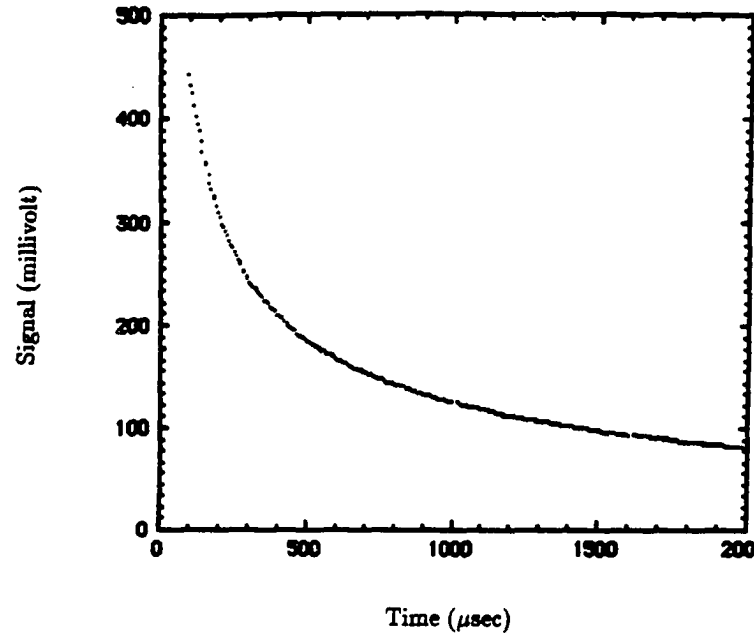

Figure 5.2: The typical photoconductivity decay curve recorded on the oscilloscope.

is the bulk Auger recombination. Assuming that the excess carrier density is uniformly distributed and is much higher than the doping concentration of the wafer (high-level-injection), the total recombination rate can then be expressed as

$$w\frac{d\bar{n}}{dt} = w\frac{\bar{n}}{\tau} + 2\frac{J_o}{q}\left(\frac{\bar{n}}{n_i}\right)^2 + wC_a\bar{n}^3; \tag{5.1}$$

where w is the thickness of the wafer, $\bar{n}$ is the bulk carrier density, and the rest of parameters have their usual meaning. Another expression of the equation is to divide $\bar{n}$ and w on both sides of the equation,

$$\frac{1}{\tau_{eff}(t)} = \frac{1}{\bar{n}}\frac{d\bar{n}}{dt} = \frac{1}{\tau} + \frac{J_{o,e}\,\bar{n}}{q\,n_i^2\frac{w}{2}} + C_a\bar{n}^2. \tag{5.2}$$

Both τ_{eff} and $\bar{n}$ can be derived from the photoconductivity decay curve. Because of different functional dependences of $\bar{n}$ for each recombination mechanism, the J_o can be obtained from the $1/\tau_{eff}$-versus-$\bar{n}$ plot. For example, Figure 5.3 is the plot obtained from the previous figure. Two curves are shown in the figure; one includes the Auger recombination term and is fitted with a parabolic function; the other is derived from the former curve by subtracting the contribution of the Auger recombination, assuming C_a =1.66 $\times 10^{-30}$ cm^6/sec [29]. In fact, the prefactor of the

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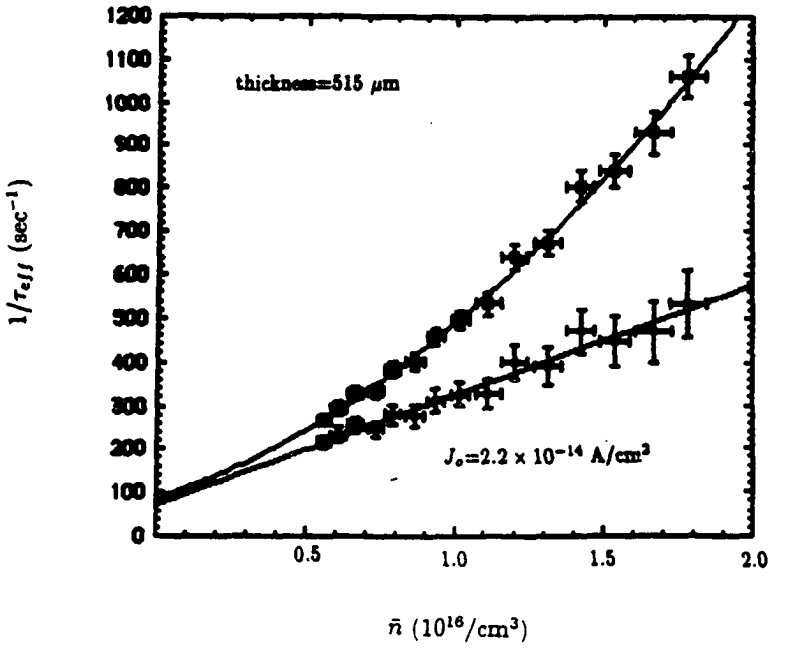

Figure 5.3: The $1/\tau_{eff}$ versus $\bar{n}$ derived from the photoconductivity decay curve of the previous figure. The lower curve has the recombination attributed to Auger subtracted out.

quadratic term in the parabolic fit is 1.77×10^{-30} cm^6/sec, which agrees with the value cited above very well. As indicated in the figure, the J_o is usually extracted from the slope of the second curve (or line), and is 2.2×10^{-14} A/cm^2 in this case.

5.3 The Polysilicon Emitter with Chemically Grown Interfacial Oxide

In the first attempt, we investigated the recombination of a polysilicon emitter with a chemically grown interfacial oxide. On such wafers, the interfacial oxide was grown in an NH_4OH:H_2O_2:H_2O (1:1:5) solution at 70 °C for 10 minutes. After the growth of the interfacial oxide, in-situ doped polysilicon was then deposited on both sides of the wafers. BCl_3 was used as p-type dopant gas, and PH_3 for the n-type dopant gas. The detailed deposition and the polysilicon film characterization has been reported elsewhere [58,59]. Typically, the as-deposited film is polycrystalline and the resistivity is below 5 mΩ-cm for the deposition temperature at 570 °C. The

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Table 5.1: $J_{o,e}$ (A/cm^2) of in-situ doped polysilicon contacts.

Anneal Schedule	as-deposited	800 °C-30 min	800 °C-1 hour	900 °C-30 min
n-type	$\gg 1 \times 10^{-12}$	1×10^{-13}	4.5×10^{-14}	2.5×10^{-13}
p-type	$\gg 1 \times 10^{-12}$	2.6×10^{-13}	2.1×10^{-13}	9.3×10^{-13}

corresponding carrier density, deduced from Hall measurements, is between 2×10^{20} and 1×10^{20} cm^{-3}. After the polysilicon deposition, some of the wafers were then annealed at various conditions. The J_o of these samples were measured with the photoconductivity decay method and summarized in Table 5.1.

In addition, the doping profiles for both n- and p- type polysilicon film were measured with SIMS (secondary ion mass spectrometry). In Figure 5.4, the phosphorus concentration profiles of both as-deposited and post-annealed samples are given. For the post-annealed sample, a phosphorus peak is generally found at the interface between the polysilicon and the substrate. A similar result has also been reported by Burk [60] and was attributed to phosphorus segregation. Since no phosphorus peak is found in the as-deposited sample, it indicates that the dopant outdiffusion through the interfacial oxide is negligible during the polysilicon deposition. Figure 5.5 was the doping profile for a p-type post-annealed sample. Although the boron distribution is not as uniform as that for phosphorus, no significant segregation of boron at the interface is found.

To our surprise, the recombination of the as-deposited samples is so high that the J_o cannot be extracted accurately with the photoconductivity decay method. Only when the samples were annealed under various conditions did the J_o becomes measurable. As pointed out earlier, the photo-generated carriers can recombine with three different mechanisms (Eqn. (5.2)). When the recombination rate is high, the effect of the Auger recombination can be ignored because the carrier density is usually very low in such samples. Consequently, this leaves only two possible

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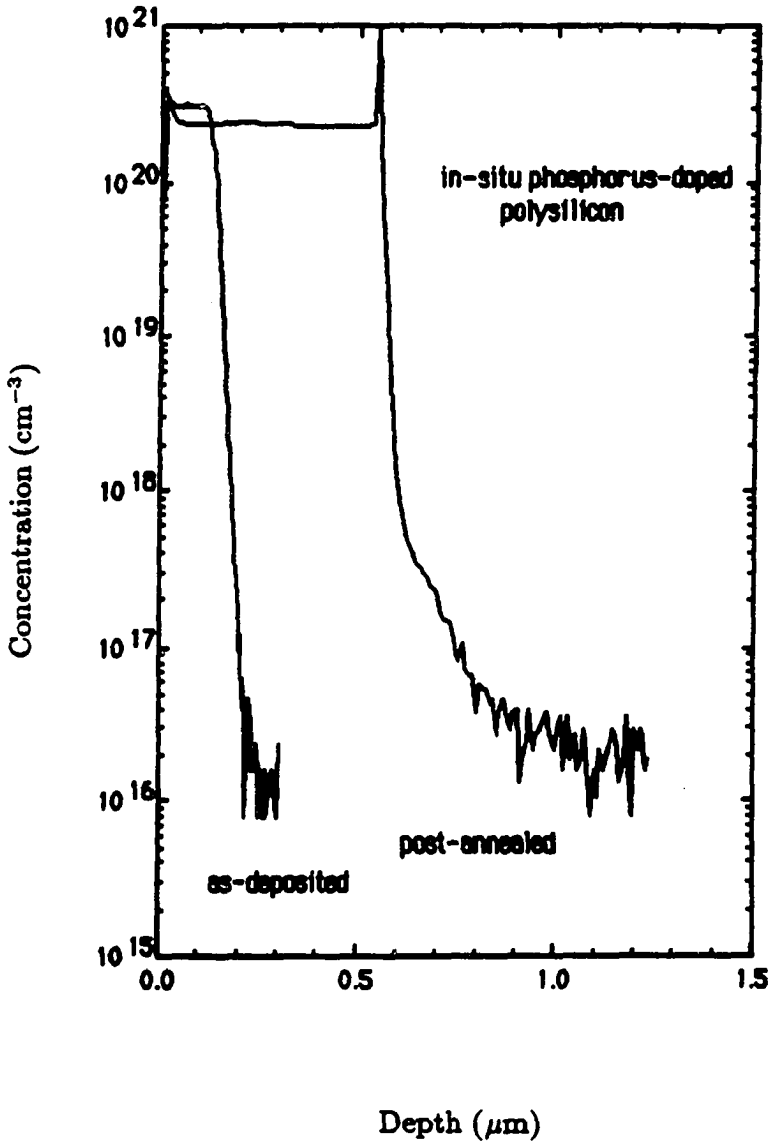

Figure 5.4: Phosphorus distribution in the in-situ doped polysilicon for the as-deposited and post-annealed samples.

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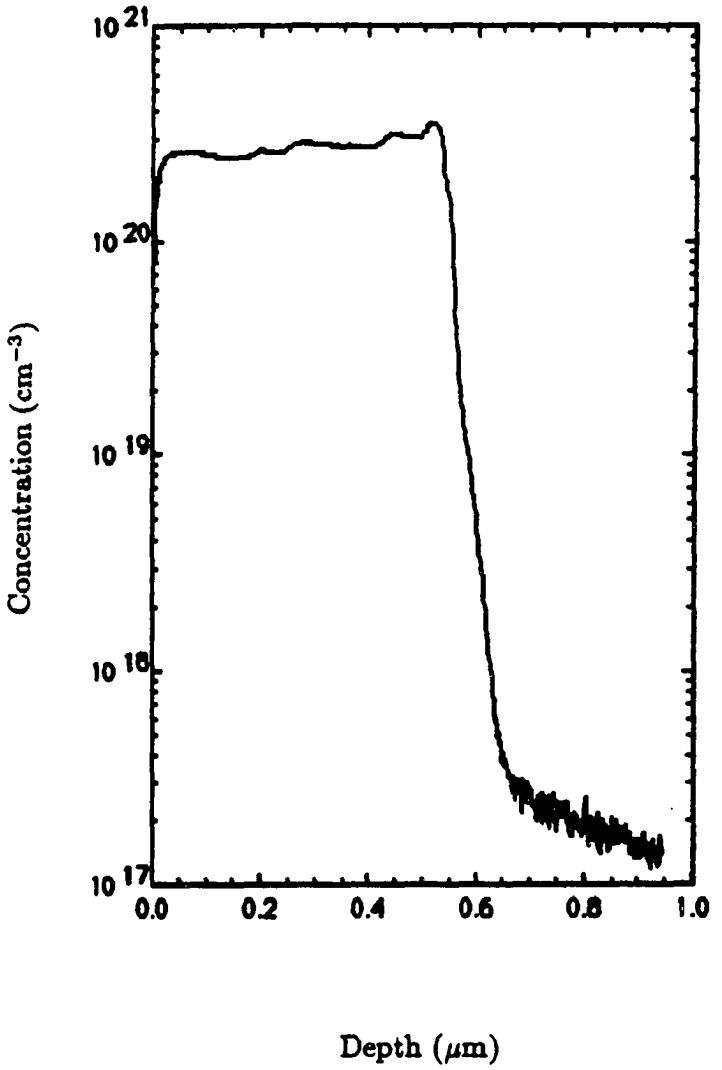

Figure 5.5: Boron distribution in an in-situ boron-doped polysilicon film that was annealed at 800 °C for one hour.

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explanations for such high recombination observed on as-deposited samples: very short bulk lifetime, and very high J_o. Samples of very short lifetime are usually caused by contamination during the processing. However, this cannot explain the much lower recombination rate of the post-annealed samples which were processed along with the as-deposited samples. It is apparent that the high recombination of the as-deposited samples results from the high emitter recombination, or high J_o.

As a matter of fact, the high emitter recombination of as-deposited samples can be entirely attributed to the high interface defect state density of such a thin chemical oxide. For a polysilicon SIS emitter, the emitter recombination can take place either inside the polysilicon, at the oxide interface on the substrate side, or in the outdiffusion region in the substrate. Since these samples received either no or only a short anneal at low temperature (800-900 °C), the outdiffusion region is expected to be very shallow; therefore, the recombination in this region is negligible. This can also be seen from Figure 5.4 and 5.5. In addition, the recombination inside the polysilicon is not likely responsible for the high J_o of the as-deposited samples either, since this would imply that the interfacial oxide has lost its integrity, and the drastic reduction of J_o due to the post-anneal should not be observed.

As shown in the table, the J_o of the p-type polysilicon SIS emitter, with the same post-anneal, is higher than that of n-type counterpart by a factor between 4 and 10. This appears consistent with what observed by Kwark [7]. From the doping profiles shown in Figure 5.4 and 5.5, the difference in J_o between the n- and the p-type polysilicon SIS emitter may result from the dopant segregation at the interface as reported by Neugrochel *et al.* [38].

5.4 Polysilicon SIS emitters with a Thin Thermally Grown Oxide

In the previous section, we have demonstrated that the oxide interface state density of a chemical oxide is so high that it eventually prevents us from making a p-type polysilicon SIS emitter with J_o comparable to that of the n-type counterpart. Thus,

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it is essential to find an interfacial oxide of better quality in order to reduce the J_o of the p-type polysilicon SIS emitter. With this in mind, a very thin thermally grown oxide was used in the hope that it would have a lower interface defect state density. The procedure of sample preparation is shown as followings.

1. $H_2SO_4 + H_2O_2$ (4:1) clean 10 minutes at 90 °C.
2. DI water rinse 10 minutes.
3. $HCl + H_2O_2 + H_2O$ (1:1:5) clean 10 minutes at 70 °C.
4. DI water rinse 10 minutes.
5. 50:1 HF dip until wafer is hydrophobic.
6. DI water rinse 10 minutes.
7. Thermal oxidation 10 minutes at 800 °C.
8. LPCVD Undoped polysilicon deposition at 600 °C for 6000 Å.
9. Doped-glass deposition
   - Boron-doped glass for p-type.
   - Phosphorus-doped glass for n-type.
10. Drive-in at 900 °C for 4 hours.
11. Forming gas anneal (FGA) 30 minutes at 400 °C.

For the thin thermal oxide growth, the furnace ambient was 5 (slm) argon and 200 (sccm) oxygen. Note that undoped polysilicon was used in this experiment. This is because we found that, in the previous experiment, a post-anneal is still needed for in-situ doped samples. Consequently, it does not make any difference when the dopant is introduced. The final step, the forming gas anneal (FGA), was added to see if the thin oxide behaves as the thick oxide. It has been known that, with an FGA the oxide interface defect states can be passivated effectively for thick oxide ($\geq$ 1000 Å) [43,61]. In addition, Fishbein *et al.* [62] reported that the D_{it} of the polysilicon-gate MOS capacitor is reduced after such a device was annealed in the forming gas at the temperature between 400 and 500 °C. Consequently, if the thin oxide behaves the same as the thick oxide, the FGA will be a good vehicle to see if the recombination at the oxide interface is important for the minority carrier transport.

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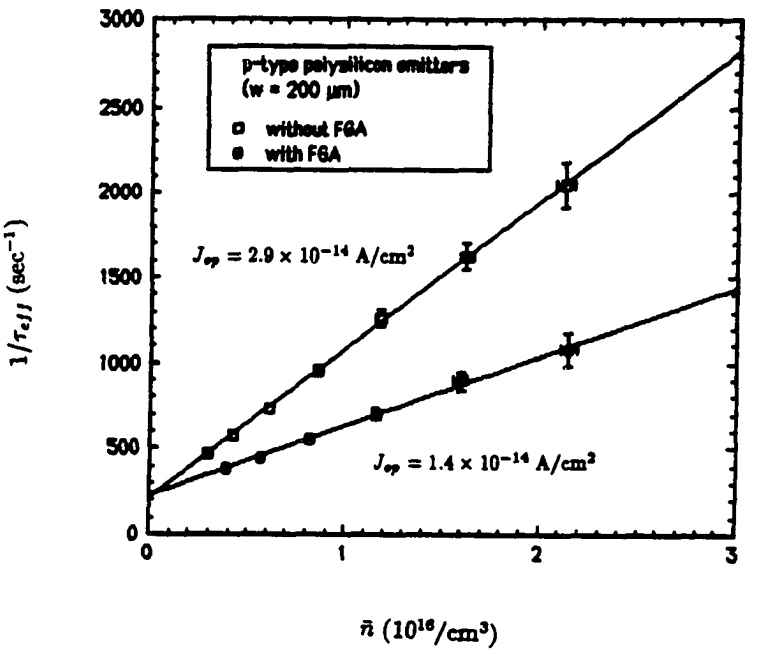

Figure 5.6: $1/\tau_{eff}$ versus $\bar{n}$ for the p-type polysilicon SIS emitter with a thermally grown interfacial oxide; the sample was either with or without a FGA.

Figure 5.6 is the plot of the $1/\tau_{eff}$ versus $\bar{n}$ for p-type polysilicon-emitter samples either with or without an FGA. Note that the J_o of both samples is significantly lower than that in the previous section. Moreover, the J_o is effectively reduced from 2.9×10^{-14} to 1.4×10^{-14} A/cm^2 by the forming gas anneal. This shows that the recombination at the oxide interface is, at least, one of the dominant process for the emitter recombination. Lower J_o was also observed on the n-type polysilicon-emitter sample. This is shown in Figure 5.7 where the J_o of the n-type sample is 1.27×10^{-14} A/cm^2, which is about the same as the lowest J_o reported previously [7].

In fact, the samples in the measurement above were all annealed at 1000 °C for two hours after the polysilicon deposition and before the dopant drive-in. As will be shown later, such an anneal has a significant effect on the J_o measured.

By using a thin thermal oxide as the interfacial layer, we have demonstrated that a very low J_o for both n- and p- type polysilicon emitters can be obtained. In addition, the improvement in J_o by an FGA seems to indicate that the recombination at the oxide interface is the dominant process in the emitter recombination. With

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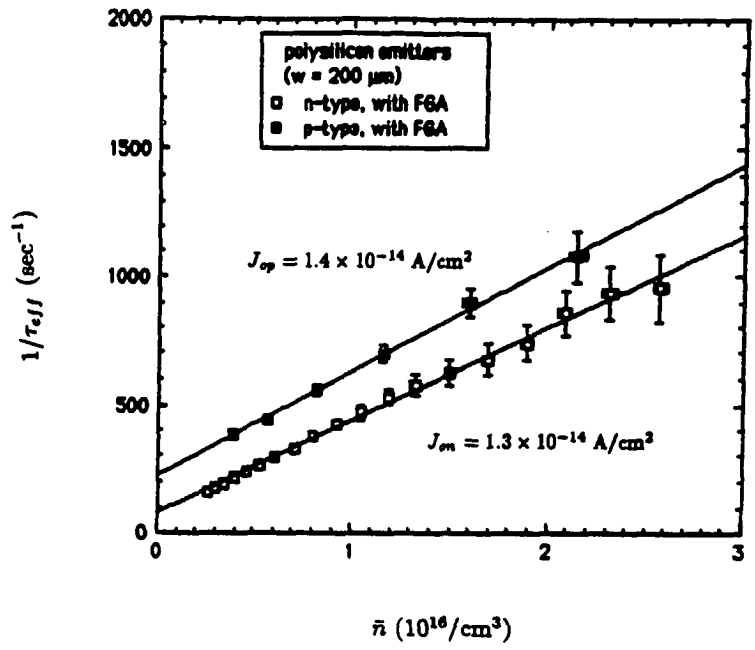

Figure 5.7: $1/\tau_{eff}$ versus $\bar{n}$ for both the n- and the p- type polysilicon-emitter samples; both had been annealed in the forming gas.

the J_o of the magnitude shown above, it is believed that the recombination in the outdiffusion region (in the substrate) should be negligible. Moreover, the dopant surface concentration, as shown in Figure 4.7, should be "relatively" low. This is shown in Figure 5.8. In the figure, the boron and the phosphorus SIMS profile are plotted together. As shown in the figure, the phosphorus outdiffusion is obscured by the sharp segregation peak at the interface and not too much information can be gained from the profile. For the boron profile, however, a small tail of boron is seen in front of the interface. Assuming that the boron concentration at the interface of the substrate is 3×10^{18} cm^{-3}, the concentration at the kink, the effective surface recombination velocity derived from simulation is 115 cm/sec, and only 4% of carrier recombination takes place in the tail region [40]. Thus, the J_o reported above is about the minimum can be obtained for the interfacial oxide quality prepared in this experiment. As a matter of fact, the J_o shown here is the lowest ever measured in this work. Typically, it is around 2×10^{-14} A/cm^2 for both types.

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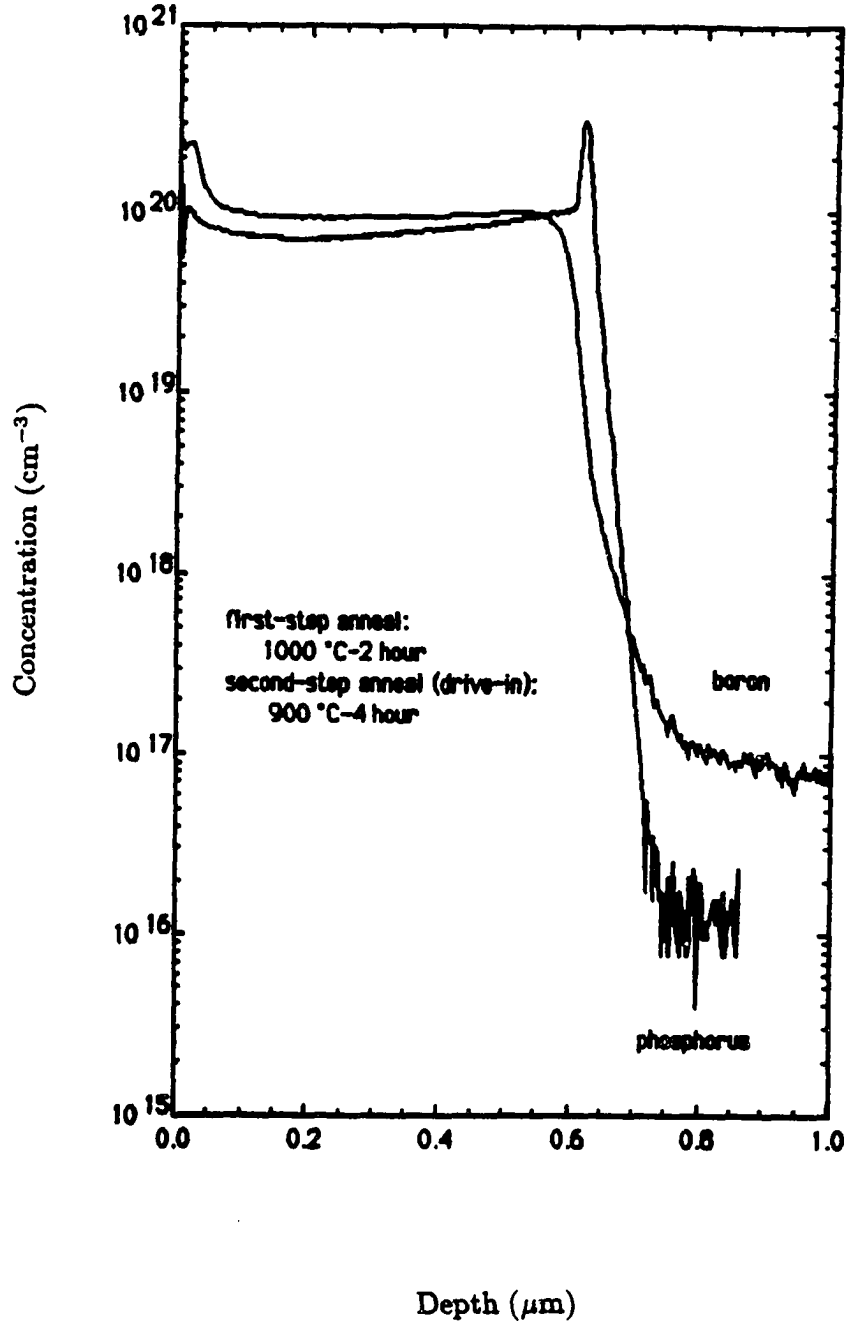

Figure 5.8: The SIMS profiles for phosphorus and boron.

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5.5 P-I-N Diodes with Polysilicon Emitters

In the last section, we discussed the experimental demonstration of very low J_o emitters. Undoubtedly, such a polysilicon SIS emitter may have very high ρ_c too. In order to reduce the high ρ_c, the interfacial oxide has to be broken. As pointed out in the previous chapter, it is likely that only a small fraction of the interfacial oxide needs to break up to give low ρ_c. One way to break it is to do a high temperature anneal. However, in order to limit the dopant outdiffusion, such a process should be performed before the normal dopant drive-in step. For convenience, we refer the high-temperature-anneal for breaking the interfacial oxide as the first-step anneal, and the subsequent dopant drive-in step as the second-step anneal.

Such a two-step-anneal technique was used to make p-i-n diodes, from which both emitter resistance and recombination can be measured simultaneously [64]. The p-i-n diodes were made on high-lifetime FZ wafers such as were used in the photoconductivity decay measurement. The interfacial oxide growth and the polysilicon deposition were the same as those mentioned in the previous section. The first-step anneal conditions were 1000 °C-2 hour, 1000 °C-4 hour, and 1050 °C-1 hour. After the first-step anneal, boron-doped glass was deposited on one side and phosphorus-doped glass on the other side to form a p-i-n diode. The intrinsic region thickness which is the substrate thickness, is 200 μm. The size of the diode is 1.25×1.25 cm^2, and the emitter coverage fraction is 3% of the diode area on each side. The structure of the diode, which in fact is a two-sided cell, is shown in Figure 5.9 schematically.

The total series resistance and the emitter recombination of the diode was measured with the open-circuit-voltage-decay method (OCVD) [28,63]. In the measurement, the diode was clamped between two thick copper chucks which were used as the electrodes for the applied current pulse as well as the voltage probes. The typical decay curve is shown in Figure 5.10. In the figure, the diode total series resistance is obtained by dividing ΔV with the total current applied. ΔV is the sudden drop of the voltage as a result of the current being terminated. When the current is off, the following voltage decay represents the recombination of the excess

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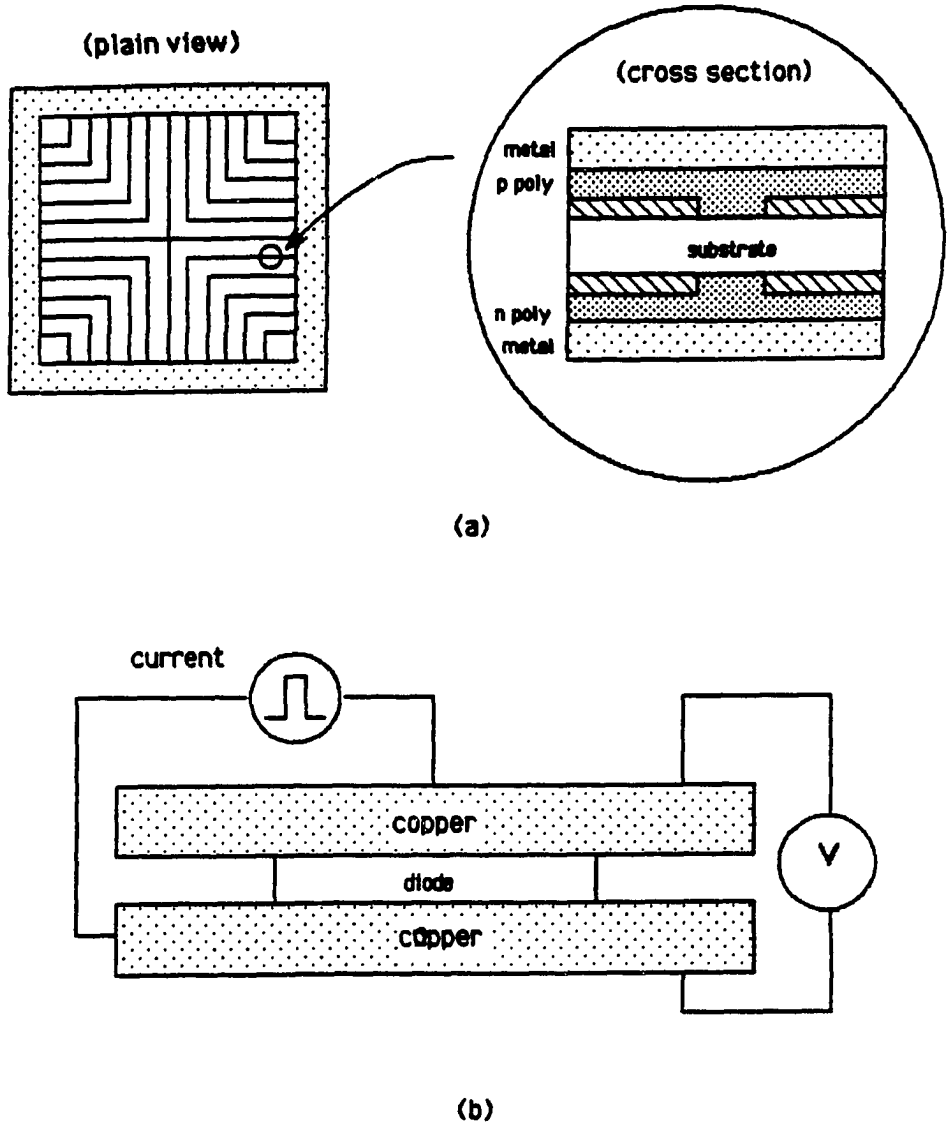

Figure 5.9: The structure of the p-i-n diode and the measurement set-up.

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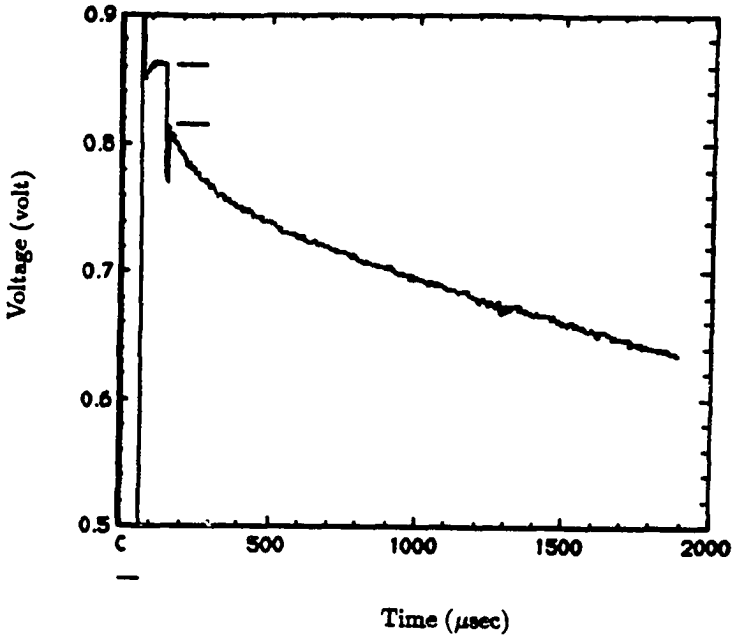

Figure 5.10: The OCVD curve for the diode, of which the first-step anneal is 1050 °C-1 hour.

carriers remained in the diode. Their relationship can be expressed as the following equation [28],

$$\frac{dV}{dt} = \frac{2kT}{qw}\left[(\frac{w}{\tau} + 2S) + \frac{(J_{on}A_n + J_{op}A_p)}{qn_i^2}\bar{n} + C_a w\bar{n}^2\right]; \tag{5.3}$$

where A_n and A_p are the emitter coverage fraction, w is the diode (wafer) thickness, and the rest has its usual definition. $\bar{n}$ can be related to the voltage. In the high-level-injection regime, it is

$$\bar{n} = n_i \exp\left[\frac{qV}{2kT}\right]. \tag{5.4}$$

Taking the time derivative of Eqn. (5.4), and substituting it into Eqn. (5.3), the equation can be expressed in the form similar to Eqn. (5.2),

$$\frac{1}{\tau_{eff}} = \left[(\frac{1}{\tau} + \frac{2S}{w}) + \frac{(J_{on}A_n + J_{op}A_n)}{qwn_i^2}\bar{n} + C_a\bar{n}^2\right]. \tag{5.5}$$

In fact, the difference between Eqn. (5.5) and (5.2) is due to the emitter coverage fraction. Because of the small emitter coverage fraction of the p-i-n diode, the term S is added and approximated with the condition of complete passivated surface.

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Table 5.2: The characteristics of p-i-n diodes measured with OCVD method**.

First-step anneal	1000 °C-2hour	1000 °C-4 hour	1050 °C-1 hour
$I(t = 0^+)$ (Ampere)	17.1	18.83	19.6
$V(t = 0^-)$ (Volt)	0.826	0.823	0.82
ΔV (mV)	56	43	41
Total resistance (mΩ)	(3.3 ± 0.4)	(2.3 ± 0.3)	(2.1 ± 0.2)
Emitter resistance (mΩ)†	~ 1.9	~ 0.96	~ 0.82
$(\rho_{cn} + \rho_{cp})$ ($\times 10^{-4}$ Ω-cm^2)‡	0.92	0.45	0.36
$(J_{on}A_n + J_{op}A_p)$ ($\times 10^{-14}$ A/cm^2)	0.73	0.34	0.56
$(J_{on} + J_{op})$ ($\times 10^{-14}$ A/cm^2)	24	11.3	18.9
$2S + 1/\tau$ (1/sec)	1122	1171	580

* The diode area is 1.5625 cm^2 and the emitter coverage fraction is $A_n = A_p = 3\%$.
† This is the value after the correction explained in the text.
‡ The value is derived from (emitter resistance × area)/(emitter coverage fraction).

This is appropriate for our diodes since the emitter coverage fraction is only 3% on each side.

Table 5.2 gives the results measured from the p-i-n diodes. They are labeled with their first-step anneal conditions. In the table, the total series resistance derived from $(\Delta V/I)$ is listed in the fourth row (total resistance). Note that the total emitter resistance listed in the next row is less than than that of the total resistance. The reason for the difference between these two will be explained later (p. 87). The total specific contact resistivity $(\rho_{cn} + \rho_{cp})$ is obtained from the product of the total emitter area and the emitter resistance. Both the total emitter recombination $(J_{on}A_n + J_{op}A_p)$ and $(\frac{1}{\tau} + \frac{2S}{w})$ were derived from the decay curve by assuming $C_a = 1.66 \times 10^{-30}$ cm^6/sec. As shown in the table, $(J_{on} + J_{op})$ is typically below 2×10^{-13} A/cm^2. In addition, $(\rho_{cn} + \rho_{cp})$ is about at the margin of the limit we mentioned in Chapter 2 ($\leq 1 \times 10^{-4}$ Ω-cm^2). This is excellent because it shows that the two-step anneal worked.

Nevertheless, the results seem confusing. For one thing, the trend of $(J_{on}A_n + J_{op}A_p)$ is not consistent with the change of $(\rho_{cn} + \rho_{cp})$. If we ¡assume that the change of $(\rho_{cn} + \rho_{cp})$ upon the first-step anneal is due to the oxide breakup, we would expect

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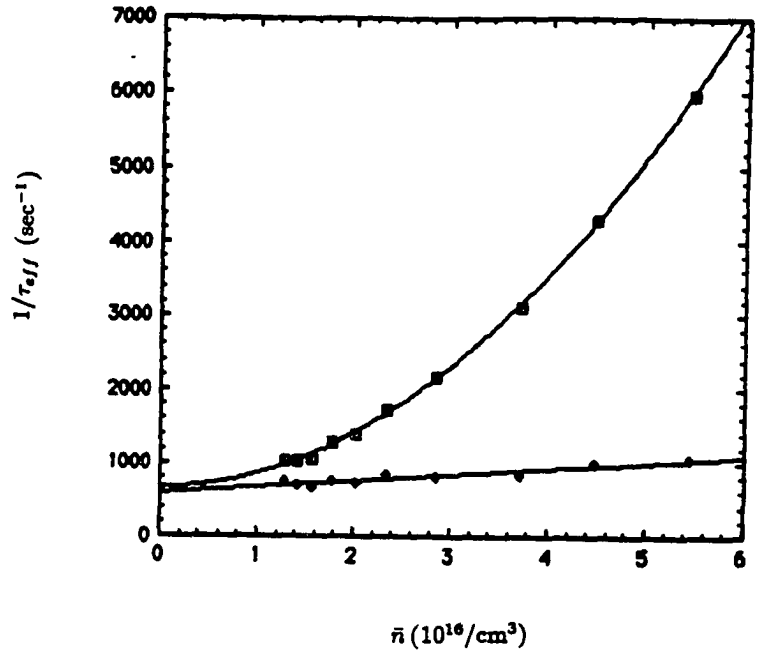

Figure 5.11: The $1/\tau_{eff}$ versus $\bar{n}$ extracted from the OCVD curve shown in the previous figure.

that $(J_{on}A_n + J_{op}A_p)$ would vary in the opposite way. However, this is not shown in the table. One possible explanation is that the emitter recombination derived from the decay curve is about at the limit that the diode can reach. This is shown in the following figure. Figure 5.11 is the $1/\tau_{eff}$-plot for the diode with a first-step anneal at 1050 °C for one hour. For the carrier density in the range shown in the figure, the linear-fit for the data less the Auger recombination is poor. This is because the emitter recombination in this range is only a fraction of the recombination from the term $(\frac{1}{\tau} + \frac{2S}{w})$. Consequently, a little noise in the measurement would distort the value of $(J_{on}A_n + J_{op}A_p)$.

In fact, the series resistance measurement does not reveal the emitter resistance faithfully either. The emitter resistance listed in the table has been corrected with the difference between the measured and the calculated $V(t = 0^+)$. The $V(t = 0^+)$ listed in the table needs to be corrected. This can be seen from the following argument. When the diode is in on-state, the current applied has to be equal to the total recombination current in the diode. To calculate the recombination current, we need to know the carrier density and the dominant recombination mechanism when the diode is at on-state. From Table 5.2 and Eqn. (5.4), the average carrier

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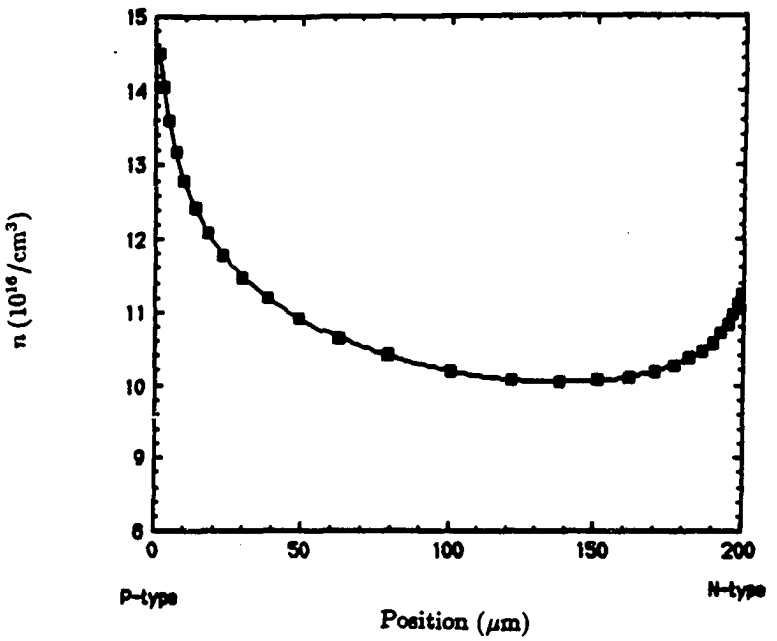

Figure 5.12: The carrier distribution in p-i-n diode from PISCES simulation.

density is $\sim 1 \times 10^{17}$ cm^{-3}. In addition, the huge difference between the data with and without Auger recombination shown in Figure 5.11 suggests that the dominant mechanism in on-state is the Auger recombination. Assume $C_a = 1.66 \times 10^{-30}$ cm^6/sec as usual, then the recombination current is

$$\begin{aligned} I_{rec} &= \text{diode area} \times (q\, w\, C_a\, \bar{n}^3) \\ &= (1.5625)(1.6 \times 10^{-19})(0.02)(1.66 \times 10^{-30})(10^{17})^3 = 8.3 \text{ (Amp)}. \end{aligned}$$

Compared with the current listed in the table (1050 °C-1 hour), the current derived above is about two times less. This implies that the actual carrier density has to be higher than 1×10^{17} cm^{-3}; in another words, the $V(t = 0^-)$ measured is less than the actual value. It is easy to estimate the real $V(t = 0^-)$ by using the applied current as I_{rec} and reversing the calculation. With a simple calculation, the real $V(t = 0^-)$ is 0.83 volt which is 10 mV higher than the value listed in the table.

Such an error is due to the resolution of the system. Strictly speaking, the carrier distribution in the diode is not uniform when the current is flowing. Upon the current being turned off, the carriers redistribute themselves so fast that the measured $V(t = 0^-)$ is the value after the redistribution and is lower too. To see

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Table 5.3: Parameters used in the PISCES simulation.

Diode thickness	200 μm
Dimension of the unit cell	120 μm
Emitter line-contact width	4 μm for each type
Substrate doping	1×10^{13} cm^{-3}
Auger Coefficient	1.66×10^{-30} cm^6/sec
J_{on}, J_{op}	0 A/cm^2
S	20 cm/sec
τ	3 msec
Electron mobility	745 cm^2/volt-sec†
Hole mobility	338 cm^2/volt-sec†

† The value is for carrier density at 1×10^{17} cm^{-3} from Ref. [33].

this is the case, a PISCES simulation [31] on the diode has been carried out. The parameters used in the simulation are listed in Table 5.3. Note that J_{on} and J_{op} are deliberately set to zero for the convenience of simulation. However, such an act is well justified because the emitter recombination in our diode is negligible compared with the Auger recombination. From simulation, the diode in fact has to be forward biased to 0.845 volt in order to keep up with the same amount of current applied on the real diode. This is even 15 mV higher than we estimated earlier. However, this is not surprising since the carrier distribution is not uniform due to the limited carrier mobility given in the table.

Figure 5.12 shows the simulated carrier distribution across the diode from the p-type to the n-type emitter. The steep gradient shown on the p-type end is caused by the smaller hole mobility. Such a distribution is not detected by the system. The main culprit for this failure is the oscillation caused by the sudden termination of current. This is shown in Figure 5.13 which is a close-look at the instant of the switching. Apparently, the information within the first four microseconds is lost

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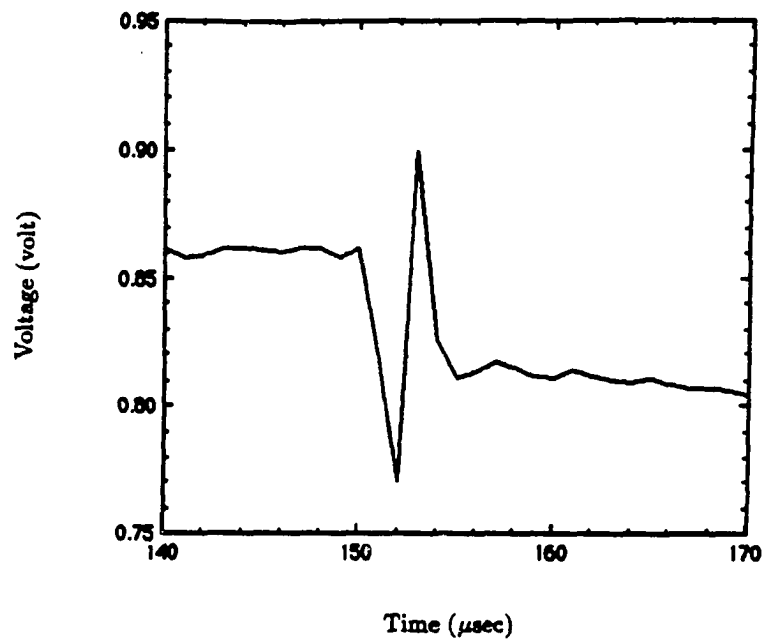

Figure 5.13: The close-look of the OCVD curve at the instant of the switching.

if it can not be recovered from linear extrapolation. Thus, the question remaining is whether such a distribution can disappear within the first four microseconds. The answer is yes. One hint is to calculate the average carrier density and the corresponding $V(t = 0^-)$ after the redistribution. These have been calculated; the average carrier density is 1.17×10^{17} cm^{-3} and the corresponding $V(t = 0^-)$ is 0.823 volt which, within the error range, is the same as the measured value. To see how fast the carriers can redistribute, we can assume that the carriers are initially accumulated at the p-type end and spread out with the form of a Gaussian distribution. Assuming that the ambipolar diffusivity (since both electrons and holes diffuse together) D_a is 18 cm^2/sec [32], the carrier density at ~78 μm away from the p-type end will reach 1.17×10^{17} cm^{-3} at the end of the first four microseconds. With the actual carrier distribution like the one shown in Figure 5.12, it is reasonable to expect that the distribution will level more rapidly.

Since the difference between the real and the measured $V(t = 0^-)$ is included in the ΔV, it should be subtracted off from ΔV in the calculation of the emitter resistance. The emitter resistance listed in the table was calculated based on the corrected ΔV. After the correction, the $\rho_{cn} + \rho_{cp}$ is less than 1×10^{-4} Ω-cm^2, and

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quite useful for concentrator solar cells. More importantly, from the change of J_o and ρ_c, it strongly suggests that the thin thermal oxide can be broken with high temperature anneals.

5.6 The Two-Step Anneal

One drawback of the previous experiment is that the individual contribution of each type emitter cannot be identified. Consequently, there remains the question of whether each type of emitter contributes equally to the emitter recombination and the emitter resistance. In addition, because of the very low emitter recombination of those diodes, it is difficult to determine the exact value of the emitter recombination.

Despite this, the results indicate that, as predicted in Chapter 4, it is possible to make a polysilicon SIS emitter with low J_o and low ρ_c simultaneously. Such a success can be attributed to the use of thermally grown interfacial oxide along with the two-step anneal. Undoubtedly, it is possible that, by varying the first-step anneal condition, the polysilicon SIS emitter with a thermally grown interfacial oxide may bring in more solid evidence for the model we proposed in the previous chapter. It is also important, from the device-application point of view, to have a thorough investigation on the effect of the two-step anneal on such a polysilicon SIS emitter.

In the following experiment, the J_o and ρ_c were measured independently for each type emitter. J_o was measured with the photoconductivity decay method, and ρ_c was measured from devices made on separate wafers. Except for the pattern-definition steps which were not required for J_o-measurement samples, they were processed together. These include thin interfacial oxide growth, polysilicon deposition, first-step anneal, doped glass deposition, and the second-step anneal (dopant drive-in).

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5.6.1 The Specific Contact Resistivity Measurement

The specific contact resistivity, ρ_c, of a polysilicon-substrate contact, is derived from the measurement on the device which is shown in Figure 5.14. Such devices were made on the wafers of resistivity 0.28 and 0.5 Ω-cm for the p- and the n- type respectively. The use of such high resistivity wafers is to avoid the possible interaction of the dopant and the interfacial oxide. The device fabrication procedures are shown as followings.

1. Field oxidation (2000 Å)*.
2. Polysilicon-substrate contact opening*.
3. Thin thermal oxide growth*. (10-minute oxygen flow)
4. Polysilicon deposition (6000 Å) and first-step anneal (1050 °C)*.
5. Polysilicon finger definition.
6. Undoped glass deposition (2000 Å).
7. Metal-polysilicon and metal-substrate contact opening.
8. Doped glass deposition on both sides of the wafer*.
9. Drive-in; 900-1000 °C*.
10. Doped glass stripping and Al-1% Si alloy deposition.
11. Metal finger definition.

Note that the steps marked with "*" are the steps for J_o-measurement samples. In step 2, a series of square contacts of size between 1 and 64 μm are opened for polysilicon-substrate contacts. The metal-substrate contact shown in the figure is made in step 7 and is about 100 μm away from the polysilicon-substrate contact.

As shown in the figure, the voltage difference, V_{ab}, between probe A and B is caused by several components of the series resistance along the current loop. They are the resistance imposed by the bulk of the polysilicon and the wafer, the metal-polysilicon contact resistance, and the polysilicon-substrate contact resistance. The potential drop across the polysilicon film is negligible because the film is heavily doped and very thin. The metal-polysilicon contact resistance is actually measured on the similar device (four-terminal resistor [65]) next to the device shown in the figure. Typically, the ρ_c of the metal-polysilicon contact is less than 1×10^{-6} Ω-cm^2.

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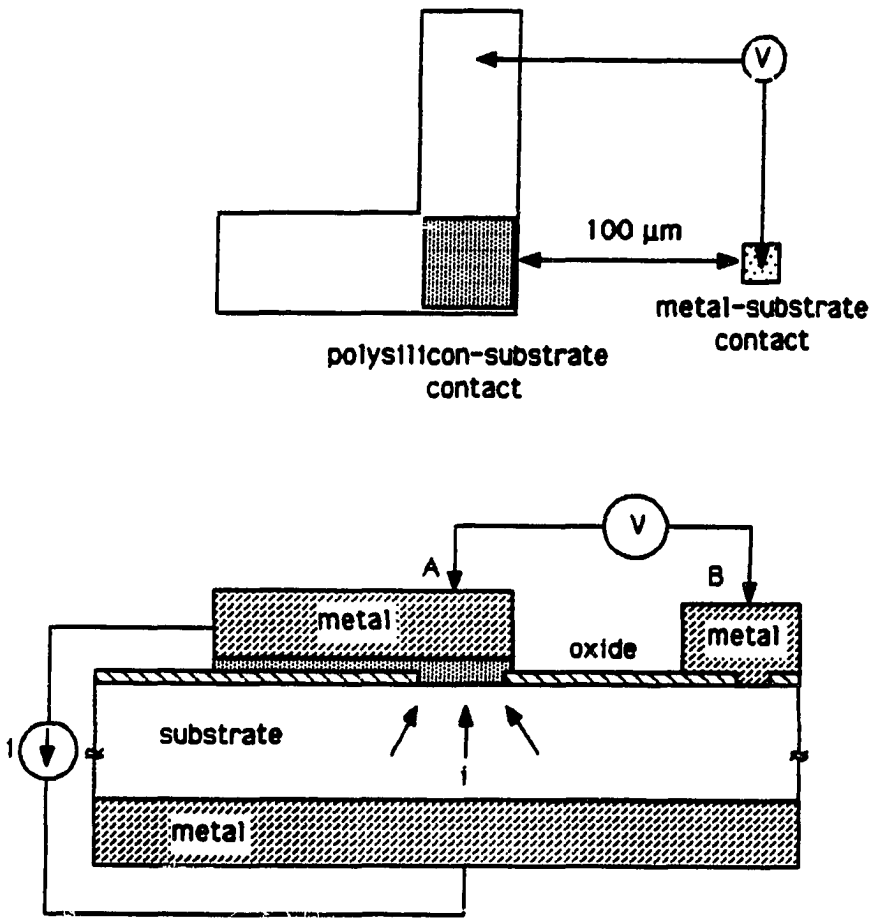

Figure 5.14: The device structure for the specific contact resistivity measurement.

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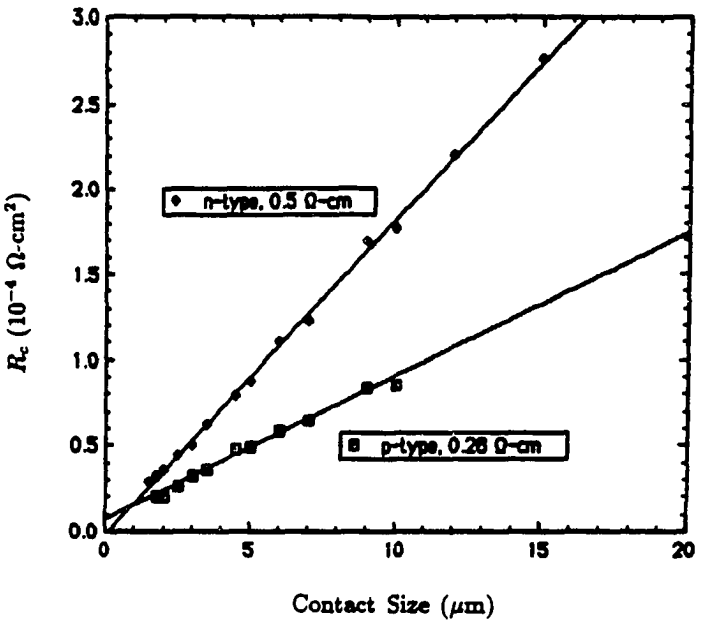

Figure 5.15: The R_c versus the contact size for both n- and p- type polysilicon contacts.

With such a low ρ_c and large contact area between the metal and the polysilicon, the potential drop across the metal-polysilicon contact can be ignored too. As a result, the series resistance derived from V_{ab}/I is essentially determined by two terms; the bulk resistance of the silicon substrate and the polysilicon-substrate contact resistance. Such a series resistance can be expressed as a function of the size of the polysilicon-substrate square contact.

$$R = C\frac{\rho}{d} + \frac{\rho_c}{d^2}, \tag{5.6}$$

or

$$R_c = R \times d^2 = \rho_c + C\rho d; \tag{5.7}$$

where C is a constant that accounts for the contact geometry factor, ρ is the substrate resistivity, d is the width of the square contact, and ρ_c is the specific contact resistivity of the polysilicon-substrate contact. The contact size dependence of the last term in Eqn. (5.7) results from the crowding effect as the current flows toward the polysilicon-substrate contact. It is obvious that, from Eqn. (5.7), the ρ_c can be derived from the plot of R_c versus d which is obtained by measuring the series resistance of contacts of different sizes.

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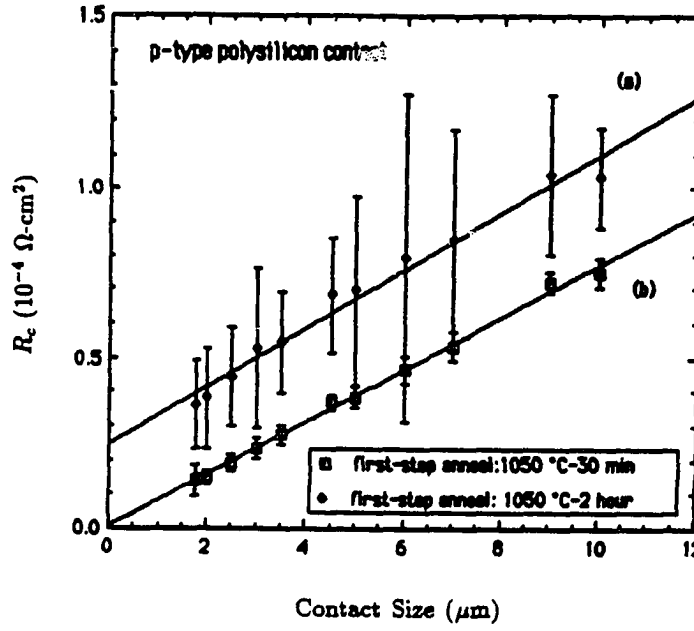

Figure 5.16: The R_c versus the contact size for p-type polysilicon contacts of different first-step anneals.

Figure 5.15 is a plot of R_c versus d for the n- and the p- type polysilicon contact respectively. In the figure, each point is the average value measured from 16 devices. Note that both sets of data can be fitted with linear functions precisely. This indicates that the possible contribution to the series resistance from the other terms, which would be proportional to d^2, is negligible. In Eqn. (5.7), C is the only unknown parameter, and is assumed to be a constant. Such an assumption is verified by comparing the ratio of the bulk resistivities (1.7) with the ratio of the slopes (1.6) shown in the figure. Nevertheless, the figure also shows one of the disadvantages of this method; that is, the resolution of this method depends critically on the substrate resistivity and the magnitude of ρ_c. With the use of wafers of high bulk resistivity like the n-type wafers in this experiment, a slight misfit of the data will cause significant error of ρ_c, especially, when the real ρ_c is very low.

Figure 5.16 shows two R_c-plots for the p-type polysilicon contacts. One has the first-step anneal at 1050 °C for 30 minutes, the other has 1050 °C for 2 hours. The error bars in the figure are drawn with 4 standard deviations. Since devices were made on the wafers of about the same resistivity, the slopes of the linear-fit lines are again almost identical. The effect of the first-step anneal is clearly shown on

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the different intercepts at the R_c-axis, which is the ρ_c. The devices that received a 30-minute first-step anneal has a higher intercept than those that received a 2-hour first-step anneal. Apparently, this has to do with the extent of the oxide breakup which in turn is determined by the anneal schedule. For a shorter anneal, we would expect less breakup of the interfacial oxide, so the ρ_c is higher.

Another characteristic of the interfacial oxide breakup can also be seen from the spread in the data (the length of the error bar). The magnitude of the error bar is irrelevant to the measurement; instead, it results from the random distribution of the oxide breakup. When there is only a very small fraction of the interfacial oxide broken, it is possible that the interfacial oxide on each contact may not be broken equally. Consequently, this gives rise to the fluctuation of the resistance measured. On the other hand, the fluctuation will be reduced when more oxide is broken. This explains the different appearance of error bars observed between these two sets of data. With such a wide fluctuation of data, it would be misleading to use the intercept shown in the figure as the ρ_c of the polysilicon-substrate contact of the devices with 30-minute anneal. Instead, we tend to use the highest possible intercept allowed in the error range as the ρ_c of these devices.

5.6.2 The Effect of the First-Step Anneal

To see how the J_o and the ρ_c is affected by the first-step anneal, one set of samples (and device wafers) were first annealed at 1050 °C for various lengths of time (first-step anneal). After the doped-glass deposition, they were all annealed at 900 °C for 4 hours. The ρ_c measured from the device and the J_o measured from the photoconductivity decay are presented in the following figures.

In Figure 5.17, ρ_c is plotted against the time of the first-step anneal for both types. Note that the ρ_c decreases as the anneal time increases. In addition, ρ_c measured from both n- and p- type devices are more or less the same, except those annealed with 120 minutes. The higher ρ_c of the n-type contact with 120-minute anneal is the victim of the high resistivity of the n-type wafer. Because of the steeper line in the R_c plot, ρ_c below 1×10^{-5} Ω-cm^2 cannot be extracted

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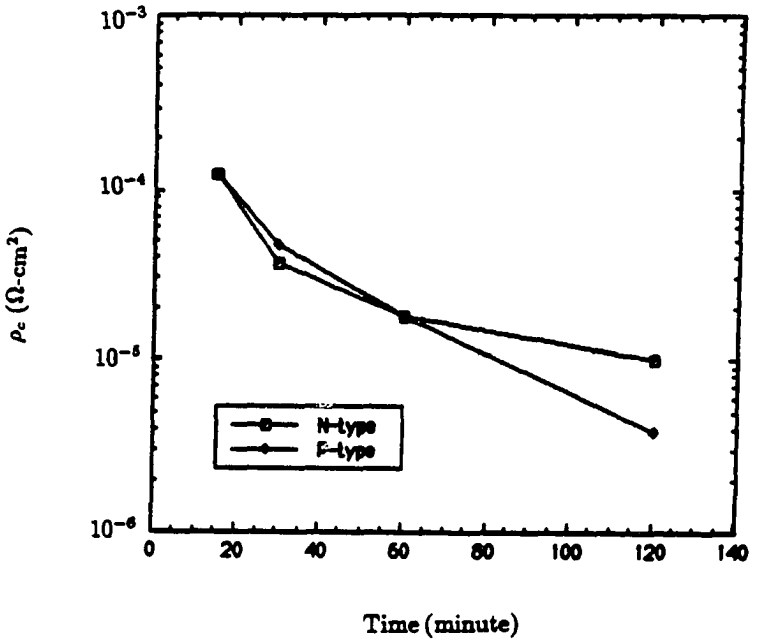

Figure 5.17: ρ_c of both n- and p- type polysilicon-substrate contacts is shown as a function of the time of the first-step anneal.

accurately. The gradual decrease in ρ_c with the anneal time is what is expected when the oxide breaks more and more in the first-step anneal. Moreover, the similarity of ρ_c between the n- and the p- type contact also indicates that the interaction between the dopant and the interfacial oxide is negligible; since such an interaction would cause the resistance of the p-type to be lower [22]. The results obtained in this experiment are believed to be very close to those obtained from the previous experiment. This can be seen from the result of the device with 1050 °C-1 hour anneal, which is present in both experiments. In the p-i-n diode experiment, the $\rho_{on} + \rho_{op}$ (Table 5.2) is $\sim 3.6 \times 10^{-5}$ Ω-cm^2 which is almost the same as the sum of ρ_c of both types shown in the figure.

The effect of the first-step anneal on J_o is presented in Figure 5.18 and 5.19 for the n-type and the p-type polysilicon SIS emitters respectively. In each figure, two sets of data are shown: the one with an FGA, and the one without. One interesting thing in these figures is that the J_o of the sample that received a 15-minute anneal is higher than the J_o for the sample that received a 30-minute anneal. Such a behavior occurs in both the n- and the p- type samples. One possible explanation is that the

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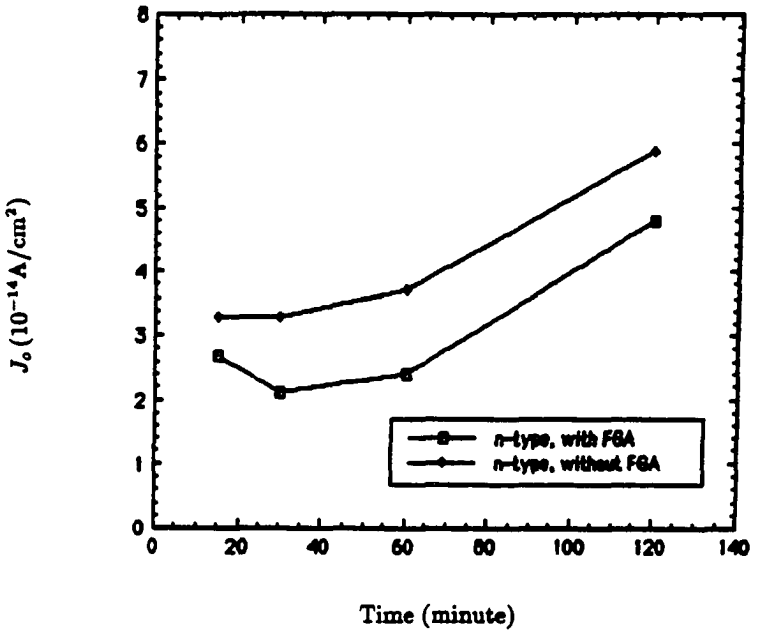

Figure 5.18: The $J_{o,e}$ versus the first-step anneal time for n-type polysilicon SIS emitters.

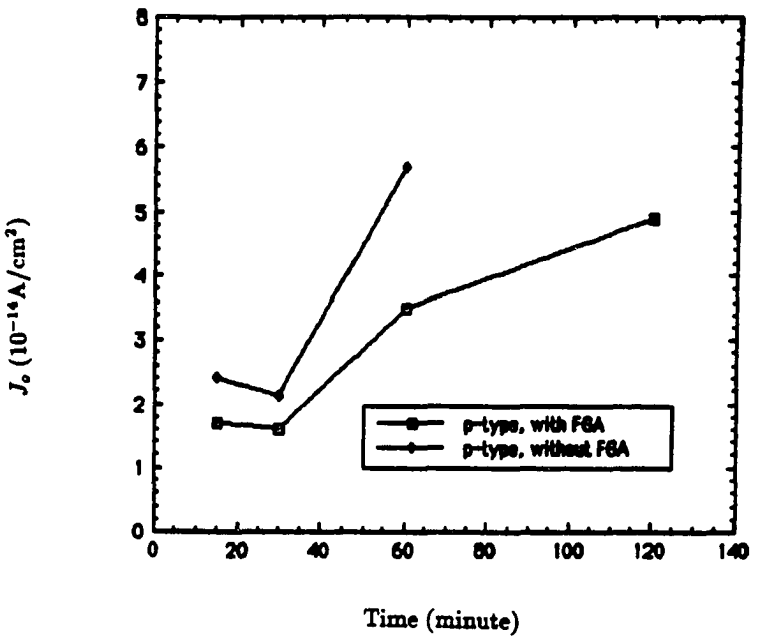

Figure 5.19: The $J_{o,e}$ versus the first-step anneal time for p-type polysilicon SIS emitters.

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interfacial oxide quality is improved by the high temperature anneal. This is not too surprising because the oxide was grown around 800 °C, in which higher D_{it} is expected [43]. As a result, the decrease of J_o for a 30-minute anneal may be due to the reduction of D_{it} caused by the high-temperature anneal [66]. Other than that, the J_o of both types appears to increase slowly with the anneal time. This is consistent with the decrease of ρ_c since J_o depends on the oxide integrity in the opposite way. In addition, the extent of the breakup of the interfacial oxide should be small since the J_o of all samples was effectively reduced after the forming gas anneal.

From the figures, the sum of J_o of both types for the samples with 1050 °C-1 hour anneal is 6×10^{-14} A/cm^2 which is about one third of the value shown in Table 5.2. Although it is very low, such J_o can be obtained equally well from the same set of data in Figure 5.11. This confirms, more or less, our speculation that the inconsistency between the emitter resistance and the emitter recombination might result from the emitter recombination not being accurately measured. As pointed out previously, it is because both the emitter coverage fraction and the emitter recombination are so low that, after the Auger recombination is removed, the recombination is still dominated by $(\frac{1}{\tau} + \frac{2S}{w})$. In the photoconductivity decay measurement, the sample is completely covered with the polysilicon contact such that not only the weight of the emitter recombination is increased but also the recombination at the passivated surface is eliminated. As a result, the resolution of J_o is much improved in the photoconductivity decay measurement. The typical error of the measurement is less than 10% of the J_o measured. Such high accuracy can readily be seen from Figure 5.6. Although the J_o of those two samples is different only by a factor of two, the two sets of data are clearly discernible.

5.6.3 The Effect of the Second-Step Anneal

The effect of the second-step anneal (dopant drive-in) on both the J_o and the ρ_c were also investigated. All samples (and devices) received a first-step anneal at 1050 °C for one hour, followed with various treatments in the second-step anneal. The

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Table 5.4: The effect of the second-step anneal on $J_{o,e}$ and ρ_c.

	N-type		P-type	
	$J_{o,e}$ ($\times 10^{-14}$ A/cm^2)	ρ_c ($\mu\Omega$-cm^2)	$J_{o,e}$ ($\times 10^{-14}$ A/cm^2)	ρ_c ($\mu\Omega$-cm^2)
900 °C-4 hour	2.4	18	3.5	18
1000 °C-30 min	4.5	~ 6	8.2	3.8
1000 °C-60 min	7.9		10.5	

results are summarized in Table 5.4. The label on the right most column represents the second-step anneal condition of that sample. As shown in the table, the J_o increase with the temperature and time for the second-step anneal.

Figure 5.20 is the phosphorus SIMS profiles for samples that received either a 900°C-4 hour or a 1000 °C-1 hour anneal. In the figure, the sample with the 1000 °C-anneal appears to have higher phosphorus concentration in the polysilicon and a much deeper junction in the substrate. The higher doping level observed on the polysilicon film may have to do with the temperature dependence of the phosphorus incorporation rate from the doped glass into the polysilicon. In addition to that, because of the much higher diffusivity of the dopant in the polysilicon, the rate-limiting process is the dopant diffusion in the substrate. Due to the rapid supply of phosphorus from the polysilicon, the surface concentration should attain the thermodynamic equilibrium value; *i.e.*, it should depend only on the drive-in temperature. Consequently, the surface concentration should be lower for the sample annealed at 900 °C compared with that annealed at 1000 °C. Recalling the critical dependence of J_o on the surface dopant concentration in Figure 4.7, the J_o difference between the sample with a 900 °C-4 hour and the sample with a 1000 °C-30 min drive-in can be attributed to the difference of the surface concentration.

The doping profile for the 1000 °C-1 hour drive-in sample has been used in the simulation to calculate the recombination in the outdiffusion region [40]. The result indicated that the recombination in the outdiffusion is in fact the dominant

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one. And not too surprisingly, the J_o difference between the samples with different drive-in time at 1000 °C is due to the extent of the outdiffusion in the substrate.

Similarly, the same argument applies to the p-type samples because the boron diffusion constant is about the same as that of phosphorus [46].

It appears that the argument above also explains the ρ_c listed in the table. Recall Eqn. (4.21),

$$\begin{aligned}\rho_c &= \rho_{c,spread} + \rho_{c,channel} \\ &= \frac{(\rho_{poly} + \rho_{sub})}{4} \\ &\quad \left\{ d \left[\frac{\tan^{-1}\left(\sqrt{\frac{1-x_b}{x_b}}\right)}{x_b} - \sqrt{\frac{1-x_b}{x_b}} \right] + 2w \left[(\frac{1}{T_{ref}})\frac{1}{x_b} - 1 \right] \right\}\end{aligned}$$

where ρ_c also depends on the resistivity of the substrate around the broken spot. As shown in Figure 5.20, the phosphorus distribution around the broken spot for the sample annealed at 900 °C could be quite different from that annealed at 1000 °C. Consequently, that the ρ_c is lower for the devices annealed at 1000 °C may be just because of the lower substrate resistivity around the broken spot.

It is obvious that, by extending the second-step anneal, the polysilicon SIS emitter can be made with much lower ρ_c with the price of higher J_o. For concentrator solar cells, it is not necessary to make such a compromise because the ρ_c is apparently low enough with a 900 °C-anneal. However, since the J_o can increase only slowly due to the outdiffusion, it is still useful for some device applications which do not have to have very low J_o, but need lower ρ_c.

5.6.4 The Relationship between J_o and ρ_c

Probably the best way to summarize our results presented so far is to map ρ_c-J_o as Crabbé did in Figure 3.13. This is shown in the following two figures. Figure 5.21 shows all the results obtained in this experiment. The inset indicates the anneal conditions for each point. It specifies the type of polysilicon SIS emitter, the first-step anneal (temperature/minute), and the second-step anneal (temperature/minute). The data run from the upper-left corner to the lower-right corner

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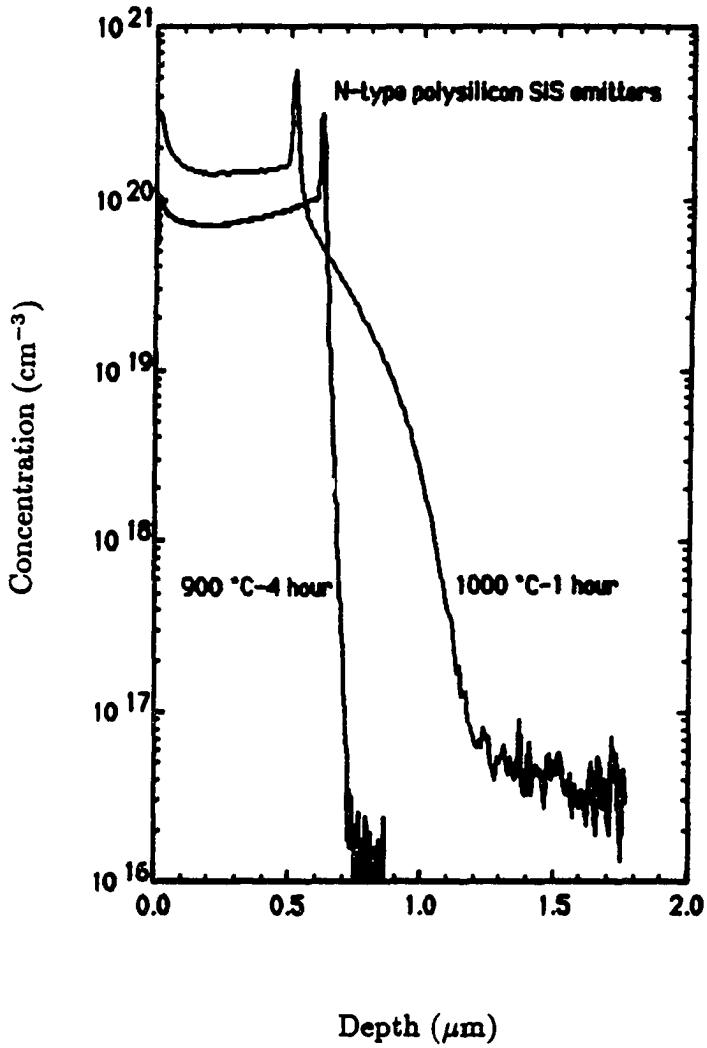

Figure 5.20: Phosphorus SIMS profiles for the sample received either a 900 °C-4 hour or a 1000 °C-1 hour second-step anneal. The first-step anneal for both samples is 1050 °C-1 hour.

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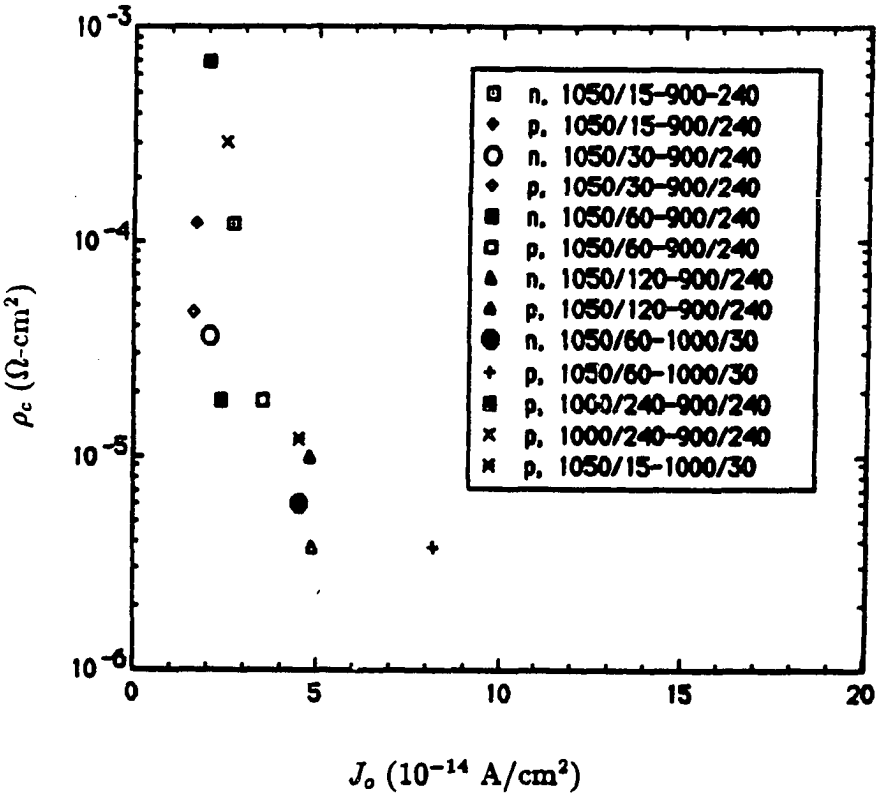

Figure 5.21: ρ_c-J_o of this work.

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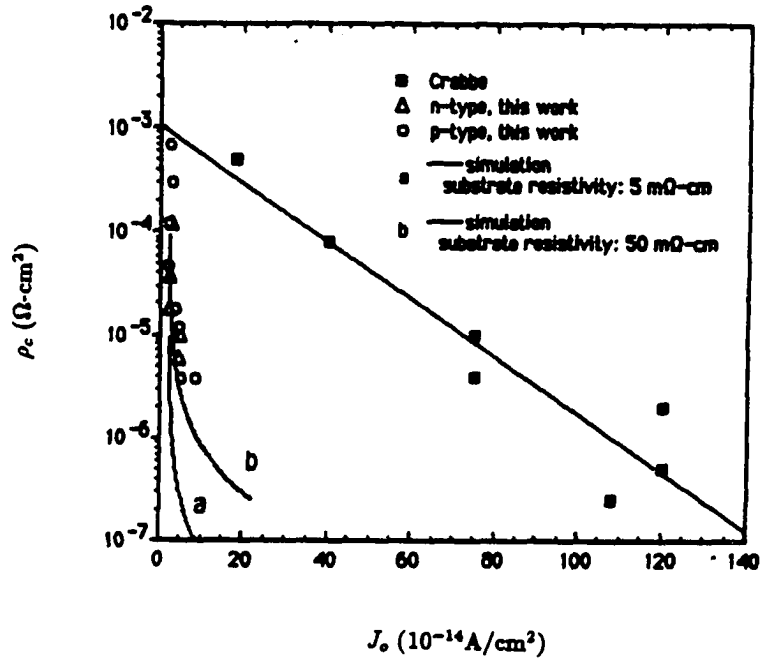

Figure 5.22: ρ_c-J_o of Crabbé's data, the experimental and the simulation results of this work.

which is similar to that reported by Crabbé. In Chapter 2 we have specified the requirements for an emitter to be used in the high efficiency silicon solar cell; that is, the ρ_c has to be lower than 1×10^{-4} Ω-cm^2 with a J_o around 2×10^{-14} A/cm^2. Regarding the ρ_c-requirement, most of the devices prepared in this experiment are qualified. Although only a few of them have J_o as low as we specified, most of them have J_o only two times larger. With appropriate emitter areal coverage fraction, they are probably equally useful for concentrator solar cells [28].

To see how much we have improved the quality of a polysilicon emitter, we plot Crabbé's results, our results shown in Figure 5.21, and the simulation results together in Figure 5.22. A line is drawn through Crabbé's data to outline the trend of his data. Our experimental results are presented with circles and triangles for the n- and p- type emitter respectively. Compared with Crabbé's, the J_o of our results has been dramatically reduced. For the points with higher ρ_c, the improvement can be attributed to the better interfacial oxide quality of our polysilicon emitters. For the points with lower ρ_c, the improvement comes from the combination of better interfacial quality and much smaller broken areal fraction of the interfacial oxide.

A very small broken area fraction, in fact, has been noted in the experiment

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because of the significant improvement of J_o by a FGA. Nevertheless, it is astonishing to see how close this is predicted by our modeling. Curve (a) in the figure is the same curve with J_o=2 × 10^{-14} A/cm^2 that is shown in Figure 4.9 (p. 68). The difference between these two curves results from the different substrate resistivities assumed. For the curve (a), the substrate resistivity is 5 mΩ-cm, while it is 50 mΩ-cm for the curve (b). Basically, our results fall on the same side with the simulation curves; which confirms that, indeed, the interfacial oxide needs to be broken by only a small fraction to have low ρ_c. Moreover, that all points are at the steep portion of the simulation curve further indicates that the broken areal fraction for all devices is extremely small. Thus, it is not surprising that a significant improvement of J_o by a FGA was observed in our experiment.

As we can see, the curve b fits our experimental results almost exactly. Considering that many parameters are simply assumed from other experiments, it is impossible to have such a remarkable match, unless the ρ_c is so critically dependent on whether the oxide is broken. This more or less provides another evidence that very low ρ_c can be made out with the polysilicon emitter with relatively intact interfacial oxide. Although the substrate resistivity has been deliberately set at 50 mΩ-cm in order to fit the data, it is by no means a random choice. Recalling the phosphorus doping profile shown in Figure 5.20, the phosphorus outdiffusion for the 900 °C-4 hour drive-in, which were used in most devices, is essentially negligible. Consequently, it would be misleading to assume the substrate resistivity near the broken region to have average resistivity of 5 mΩ-cm as that measured from the polysilicon film. In addition, the T_{ref} used in Eqn. (4.21) is not clearly understood, and may turn out higher than what we predicted.

5.7 Conclusion

In this chapter, polysilicon emitters with low J_o and ρ_c were demonstrated experimentally. To make low ρ_c, the interfacial oxide needs to be broken by only a very small fraction. Under such a condition, J_o is still dominated by the recombination at the oxide interface so that, with an interfacial oxide of good quality, the J_o can

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be kept very low. In this work, this was carried out on the polysilicon emitter with a thermally grown interfacial oxide, and the results appears to be in consistent with what are predicted in the previous chapter.

The use of a thermally grown interfacial oxide is important in that it not only has a good quality interface to the substrate, but also is robust during high temperature anneals. This allows us to see the subtle relationship between the oxide breakup and the ρ_c and J_o. Depending on the extent of the oxide breakup, various combinations of ρ_c and J_o have been obtained. Typically, the $J_o \leq 5 \times 10^{-14}$ A/cm^2 and $\rho_c \leq 1 \times 10^{-5}$ Ω-cm^2 for both n- and p- type polysilicon emitters have been obtained. As shown in the cell modeling, such polysilicon emitters can be quite useful for silicon concentrator solar cells. Because the ρ_c is low enough, they are also equally useful in other bipolar power devices which are operated at higher current density ($\geq$100 A/cm^2) and suffer high emitter recombination [67].

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Chapter 6

The Effect of the Oxide Thickness

6.1 Introduction

As has been shown in the last two chapters, the polysilicon emitter with low J_o and ρ_c can be made with a very small fraction of the interfacial oxide breakup. The main reason for that can be attributed to the fact that the thermally grown interfacial oxide is more robust compared to the chemically grown one. In Wolstenholme *et al.*'s experiment mentioned in Section 3.6 (p. 39), the substantial breakup of a chemically grown interfacial oxide was clearly shown when the sample was annealed above 1000 °C. In contrast, the thermally grown oxide is broken only very little even with the sample was annealed at 1050 °C as our results indicated.

Although a thermally grown interfacial oxide seems essential for a polysilicon emitter to have both low J_o and ρ_c, the breakup process is still difficult to control. On several occasions, we have encountered reproducibility problems. For example, we find that the ρ_c is quite different between two separate experiments with identical processing conditions. Even worse, solar cells that were made in this study all suffered high contact resistance.

The problem is primarily due to insufficient oxide breakup, and is caused by the fluctuation of the thickness of the interfacial oxide. In the next section, we first show some odd results that have been observed in the experiment. This is followed with a detailed calibration of our process which leads to the discovery of the fluctuation

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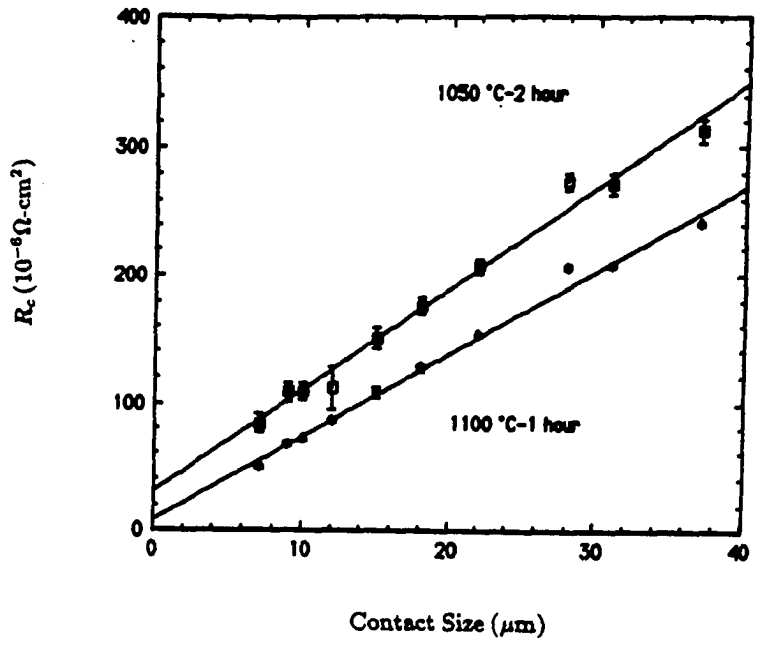

Figure 6.1: The R_c versus the contact size for p-type polysilicon contacts of different first-step anneals the results of the first run of the contact-resistance-device fabrication.

of the oxide thickness. Experimentally, the oxide thickness dependence of the oxide is shown. Such a dependence is also explained based on the breakup mechanism.

6.2 Some Odd Results

In the course of this study, two separate contact-resistance-device runs were carried out. The results of the second run are those presented in the previous section. The first run was made with the purpose of seeing if we can break the interfacial oxide. Figure 6.1 shows the R_c-plots for two different first-step anneal conditions; one was annealed at 1050 °C for two hours, the other was annealed at 1100 °C for one hour. The ρ_c extracted from both cases confirms that the interfacial oxide has been broken. However, the results shown in the figure are much higher than that presented in the previous section; to be exact, ρ_c is about ten times higher for the devices annealed at 1050 °C for two hours. Although this could be the first sign that the oxide-growth recipe is not reliable, it was ignored because the results are still good enough for the emitters to be used in the concentrator solar cells.

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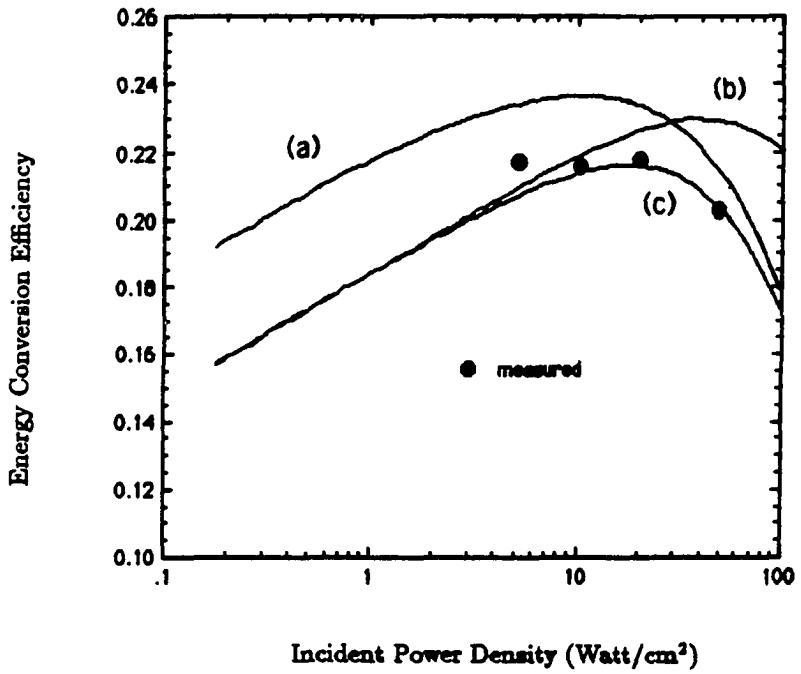

Curve	$J_{on} + J_{op}$ ($\times 10^{-14}$ A/cm^2)	Responsivity (Amp/Watt)	S (cm/sec)	$\rho_{cn} + \rho_{cp}$ Ω-cm^2
(a)	8	0.35	8	1×10^{-3}
(b)	8	0.35	58	0
(c)	8	0.35	58	1×10^{-3}
The cell thickness 115 μm				
The dimension of the unit cell 50 μm				
The width of contact line 15 μm				

Figure 6.2: The cell efficiency versus the incident power density for an untexturized IBC cell. The dot is the measured efficiency, and curve (a), (b), and (c) are the simulation results with parameters shown above.

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Later, in the real solar cell runs, the situation got even worse. The solar cells made in the experiment are the 15-μm-contact-line IBC which have been shown and simulated in Chapter 2. We found that, with the OCVD measurement, the total specific contact resistivity ($\rho_n + \rho_p$) was higher than 1×10^{-3} Ω-cm^2. Although the ($J_{on} + J_{op}$) measured from those cells are between 8×10^{-14} and 4×10^{-14} A/cm^2, the cell efficiency is greatly degraded by such a high emitter resistance. Figure 6.2 is the cell efficiency plotted against the incident power density for one of the "better" cells. The cell had a first-step anneal at 1050 °C for two hours. The measurement technique and apparatus were reported by Sinton [28] in detail. Note that the efficiency is generally lower than that presented in Chapter 2. This is because the cell is not texturized, so that the responsivity is lower accordingly. In the figure, the dots are the measured cell efficiency. In addition, three curves from simulation, and the parameters used to generate those curves are also included. The rest of parameters not shown in the figure are assumed to have the same value as that shown in Table 2.1. The parameters used for the curve (c) are obtained from the real cell. The S is separated from ($\frac{1}{\tau} + \frac{S}{w}$) by measuring cells of various thickness (115, 225, and 500 μm).

As shown in the figure, the cell is in fact plagued by two things: the high surface recombination velocity (S = 58 cm/sec), and high emitter resistance ($\rho_{cn} + \rho_{cp} = 1 \times 10^{-3}$ Ω-cm^2). The effect of high emitter resistance is shown by the difference of the cell efficiency between the curve (b) and the curve (c), while the difference between the curve (a) and the curve (c) shows the projected effect of the high surface recombination velocity. Without the high surface recombination velocity and the emitter resistance, the cell performance would be the curve formed by the maximum efficiency between the curve (a) and the curve (b) which is the ultimate performance we can have for the cell with polysilicon emitters.

From the low emitter recombination and high emitter resistance, it is clear that the interfacial oxide did not break as we expected.

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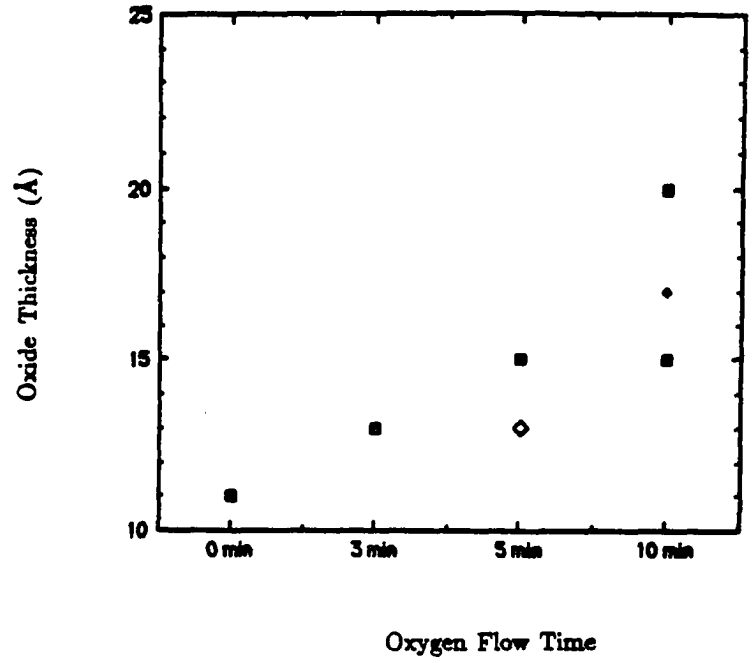

Figure 6.3: The oxide thickness grown with oxygen flown at various length of time.

6.3 The J_o Dependence on the Interfacial Oxide Thickness

Although these results can be attributed to many other reasons, the following experiment shows that the effect of the oxide thickness cannot be ignored. This, combined with the non-reliable oxide-growth recipe gives rise to the mishap of our solar-cell runs.

The calibration of our oxide-growth recipe was carried out in several different periods of time, and various lengths of time of oxygen flow. In addition, every step which may cause the deviation of the oxide thickness was also checked. The wafer cleaning process was kept the same as that shown in Section 5.4. The oxide thickness was measured with an ellipsometer. Typically, the oxide thickness measured prior to the thermal oxidation (step 6) is 7 Å, and stays the same when the wafer is left in the air for more than one hour. In the oxide-growth step, the furnace ambient is pure argon (5 slm); and the oxidation is controlled by introducing an additional oxygen flow (200 sccm) for various lengths of time.

The oxide thickness grown with this scheme is summarized in Figure 6.3. The

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case $t = 0$ means that the furnace was filled with pure argon flow; nevertheless, the oxide thickness has increased to 11 Å. This may have to do with the oxygen residue in the furnace, and is the minimum thickness of oxide that can be obtained from our oxidation recipe. As the time of the oxygen flow increases, the oxide thickness increases accordingly. However, the oxide growth was also found to depend on the furnace condition. This is shown for the oxidation with 5 and 10 minutes of oxygen flow. For a 10-minute flow of oxygen, a difference of 5 Å has been found between the runs done at different times. One possible explanation for such variations is that it may result from the fact that the oxidation proceeded when the furnace was still at the ramp-up stage. Consequently, the oxide growth depends on the final temperature of the furnace, which in turn is determined by how long the boat has been pulled out from the furnace before the wafer loading.

The other place that the oxide thickness can go wrong is at the polysilicon deposition step. In the polysilicon deposition step, the system is set at 600 °C; however, the actual deposition does not take place until the system temperature is stabilized. It is possible that further oxidation may occur in this stand-by period. This was checked out by measuring the oxide thickness of the wafers which have been loaded into the polysilicon LPCVD tube for the same amount of time as the stand-by period in the actual deposition. No further oxidation has been observed for the wafer with oxide thickness shown in Figure 6.3.

From the above, it appears that the variation of the oxide thickness results mainly from the oxide-growth step. If this is the case, it is possible that the thin-oxide growth can be improved by performing the oxidation at lower temperature such that the oxidation rate can be controlled more precisely.

To see how the oxide thickness affects the breakup process, we checked the change of the J_o of the p-type polysilicon SIS emitter upon the first-step anneal. Those emitters were made with the interfacial oxide thickness in the range shown in Figure 6.3. In addition, a much thinner polysilicon (1600 Å) was used in this experiment; therefore, the second-step anneal was performed at 900 °C for only one hour. Figure 6.4 shows the J_o measured on these samples plotted against the thickness of the interfacial oxide. Four data sets are shown in the figure; they are

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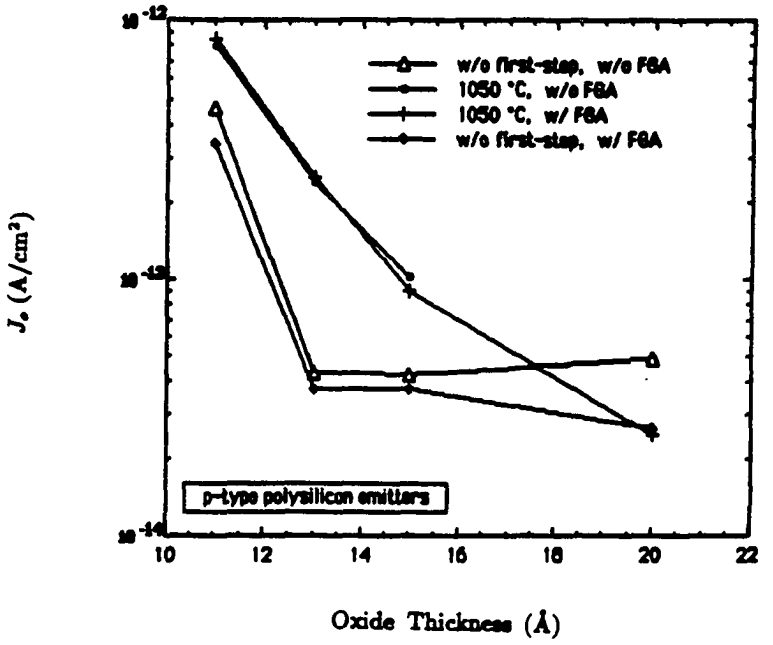

Figure 6.4: The J_o of p-type polysilicon emitters versus the thickness of the thermally grown interfacial oxide.

the various combinations of with/without a first-step anneal and with/without an FGA. The first-step anneal was performed at 1050 °C for two hours, except for the sample with 11 Å interfacial oxide which was only annealed for one hour at the same temperature.

For the samples without a first-step anneal, the J_o is in general lower than those with a first-step anneal. Moreover, the FGA effect on these samples is appreciable too. This indicates that the oxide interface recombination for the oxide thickness in this range is significant. Note that the J_o appears much higher for 11 Å oxide. However, it is difficult to say what mechanism is responsible without knowing the integrity of the interfacial oxide exactly. As the oxide thickness increases beyond 13 Å, J_o only slightly depends on the oxide thickness. When the first-step anneal was added, a dramatic increase of J_o has been observed in most cases. More importantly, the increase of J_o is a function of the interfacial oxide thickness. If we take the ratio of J_o between the one with and the one without the first-step anneal, it appears that the ratio decreases as the thickness of the interfacial oxide increases. With the same anneal time, the ratio decreases about from 5 to 1 as the interfacial oxide thickness increases from 13 to 20 Å. As a matter of fact, the first-step anneal hardly

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changes the J_o of the sample with 20 Å interfacial oxide.

6.4 The Oxide Breakup Mechanisms

It becomes clear that the wide fluctuation of our results is mainly due to the poor control over the oxide thickness. From Eqn. (4.21) (p. 61), ρ_c does not depend on the oxide thickness once the oxide breaks up. Consequently, the oxide-thickness dependence of ρ_c must result from the oxide breakup process. To see how the oxide breakup depends on the oxide thickness, it is necessary to examine the process microscopically. Kinematically, the oxide breakup process consists of two steps: the initiation of the broken spots and the subsequent growth of the broken spots. This is similar to one of the phase transition phenomena which involves the nucleation and grain growth.

Whether a broken spot can be formed may depend critically on the oxide thickness. Figure 6.5a&b show a simplified two-dimensional atomic structure around the interfacial oxide. In Figure 6.5a, a continuous interfacial oxide film is shown which corresponds to the initial state where no breakup has yet occurred. In Figure 6.5b, a silicon cluster (enclosed by a dotted square) is shown in the center of the figure. The reason for the silicon cluster nucleation is due to the high energy associated with the Si-oxide interface which is qualitatively shown by the unsaturated silicon bonding along the interface. At high temperature, the exchange between silicon and oxygen atoms becomes more frequent; as a result, a more stable configuration of oxide can be obtained by reducing the area-to- volume ratio of the interfacial oxide. Morphologically, such a process is manifested by the silicon cluster formation. Whether the silicon cluster is stable depends on how much the total energy has been reduced in the process. For simplicity, let us assume that the interface energy is linearly proportional to the interface area. Therefore, whether the cluster is stable can be judged by the interface area difference caused by the cluster formation. In Figure 6.5b, additional interfaces on each side have been created, along with the elimination of both the top and bottom interfaces, during the cluster formation. As shown in the figure, the newly created interface is proportional to the thickness of

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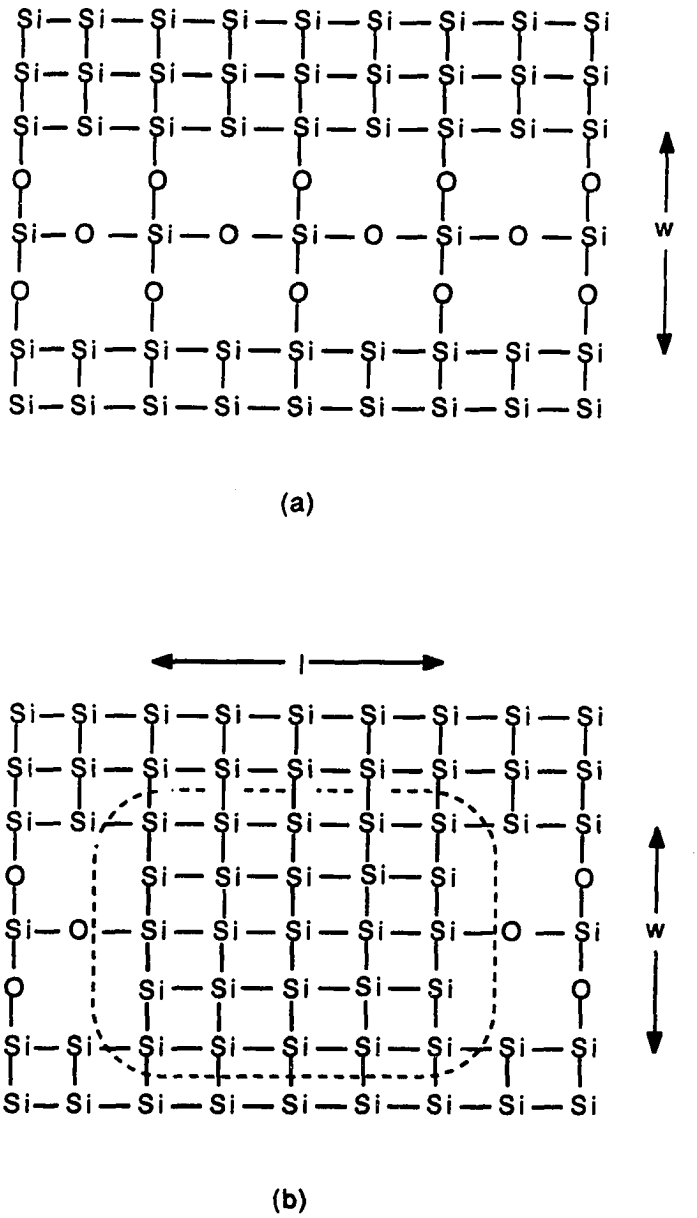

Figure 6.5: A simplied two-dimensional atomic arrangement around the interfacial oxide; (a) a continuous interfacial oxide, (b) a silicon cluster is formed in the interfacial oxide (oxide breakup).

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the interfacial oxide, and the eliminated interface is determined by the width of the cluster. Consequently, a stable cluster must have a size greater than the thickness of the interfacial oxide. When the oxide thickness increases, the required size for a stable cluster increases accordingly.

The oxide-thickness effect comes into play because the stable silicon cluster can be formed only by a multi-exchange process; *i.e.*, all atom exchanges have to occur simultaneously. With the same anneal condition, it is apparent that a thick oxide will be more difficult to break up. This qualitatively explains the oxide-thickness dependence of the oxide breakup process.

It is also interesting to see how this "silicon cluster nucleation" explains the difference in the oxide breakup between the chemically grown and the thermally grown oxide. In Wolstenholme *et al.*'s experiment (p. 39), the substantial breakup of a chemically grown interfacial oxide was clearly shown when the sample was annealed above 1000 °C. In contrast, the thermally grown oxide is broken only very little even when the sample was annealed at 1050 °C as our results indicated. This can be explained by the difference of the extent of the non- stoichiometric oxide. Chemical oxide has been found to be highly oversaturated with silicon [17,61]. Consequently, less effort is needed to create a stable silicon cluster for the same oxide thickness.

Since the silicon cluster nucleation involves bond-breaking processes, any imperfect bonding structure in the interfacial oxide may assist the oxide breakup process. Consequently, it is possible that our inconsistent results may have to do with the initial surface condition of the wafer. If this is the case, it may show up in the J_o results as well. However, no anomalous results in J_o have been observed in our experiments for the thermally grown interfacial oxide, which indicates the effect of the initial surface condition is not the primary cause.

6.5 Conclusion

In this chapter, we found that a consistent result of ρ_c is difficult to reproduce for the polysilicon emitter with a thermally grown interfacial oxide. This is mainly

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attributed to the fact that our thin-oxide growth recipe is not reliable. With the same oxidation schedule, a wide variation of oxide thicknesses have been found for different times. Experimentally, the interfacial oxide breakup was also found to depend on the oxide thickness critically. Such an oxide-thickness dependence of the breakup process can be explained by a "silicon cluster nucleation" process. In order to have reproducible results, it appears that a precise control of the oxide thickness is necessary.

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Chapter 7

Conclusions

7.1 Results

The important contribution of this work is to show that polysilicon emitters with both low J_o and ρ_c can be obtained. This was theoretically predicted first, then experimentally demonstrated. To make low ρ_c, the interfacial oxide needs to be broken by only a very small fraction. Under such a condition, J_o is still dominated by the recombination at the oxide interface so that, with an interfacial oxide of good quality, the J_o can be kept very low. In this work, this was carried out on the polysilicon emitter with an thermally grown interfacial oxide.

The use of a thermally grown interfacial oxide is important not only because it has a good quality interface to the substrate, but also because it is robust during high temperature anneals. This allows us to see the subtle relationship between the oxide breakup and the ρ_c and J_o. Depending on the extent of the oxide breakup, various combinations of ρ_c and J_o have been obtained. Typically, $J_o \leq 5 \times 10^{-14}$ A/cm^2 and $\rho_c \leq 1 \times 10^{-5}$ Ω-cm^2 for both n- and p- type polysilicon emitters have been obtained. As shown in the cell modeling, such polysilicon emitters can be quite useful for silicon concentrator solar cells. Because the ρ_c is low enough, they are also equally useful in other bipolar power devices which are operated at higher current density ($\geq$100 A/cm^2) and suffer high emitter recombination [67].

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7.2 Suggestions for Future Study

It appears that the oxide breakup depends critically on the interfacial oxide thickness. The thin-oxide growth recipe used in this work was not reliable; the oxide thicknesses between 15 to 20 Å have been found with the same growth condition. As a result, this contributes to the fluctuation of the ρ_c results. It is then clear that a more reliable way of growing the thin oxide is needed.

Another topic that has not been addressed is the degradation of the interfacial oxide. It has been reported that the oxide interface degrades when it is exposed to high current and electric field [69]-[71]. Since the current density in the interfacial oxide is considerably higher when only a very small fraction of the interfacial oxide is broken, similar degradation may occur such that the J_o cannot be maintained at the constant low level. Although several reports have indicated that the degradation can be significantly reduced when the oxide is thinner [72]-[74], the possible degradation of the polysilicon emitters is worthwhile to be examined in detail.

One of the interesting things in this work is that the simulated and experimental data agree with each other very well. Since the simulated results were derived under several assumptions: uniform distribution and equal size of the broken spots, the corresponding situation in the real polysilicon emitter should be close to what is predicted. However, this was not verified in this work. Continuing investigations on the microscopic structure of the broken interfacial oxide will reveal more about how much the model corresponds to the real situation.

From the discussion of the oxide breakup mechanisms, it seems that the rate-limiting process is the silicon cluster nucleation in the interfacial oxide. The two-step anneal used in this work is just one of many possible techniques and other techniques may be more controllable. One possible alternative is an ion-mixing technique. Ion-mixing has several advantages over the two-step anneal. One is that it make the oxide breakup more uniform since the breakup primarily takes place at the location which is bombarded with the ions, and can be controlled during the ion-implantation. The other is that the breakup process is greatly enhanced by local damage caused by ion-bombardment. This lowers the required processing

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temperature which is important for integrated-circuit device fabrication.

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