

Exhibit 2027

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HANWHA SOLUTIONS CORPORATION,
Petitioner

v.

MAXEON SOLAR PTE. LTD.,
Patent Owner

Case IPR2024-01199
U.S. Patent No. 8,878,053

**DECLARATION OF DOUGLAS RUBY, PH.D. IN SUPPORT OF
PATENT OWNER'S RESPONSE**

IPR2024-01199
Maxeon Exhibit 2027

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I, Douglas Ruby, Ph.D., declare as follows:

I. INTRODUCTION

1. I have been asked by counsel for Patent Owner Maxeon Solar Pte. Ltd. to provide my opinions on certain matters raised in the Petition for Inter Partes Review, Paper 3, filed by Petitioner Hanwha Solutions Corporation with respect to U.S. Patent No. 8,878,053 (Ex. 1001) (“the ’053 patent”) and the declaration of Dr. Zachary Holman in support of the Petition, Ex. 1003. This declaration sets forth the opinions that I have reached to date regarding these matters.

2. My independent expert consulting services are being billed at the rate of \$450/hour (plus reasonable expenses) for consulting, review, preparation, and \$475/hour (plus reasonable expenses) for depositions. My compensation is not contingent on the outcome of my review and analysis. I have no financial interest in Patent Owner.

II. QUALIFICATIONS

3. Exhibit 2028 is a true and correct copy of my *curriculum vitae* (CV).
4. As set forth in my CV, I have over 30 years of experience leading teams, managing R&D projects, and advancing solar energy technologies.
5. The following is a summary of my relevant qualifications and professional experience.

6. In 1978, I received my Bachelor of Science degree in Physics from the Massachusetts Institute of Technology (MIT). My Bachelor's Thesis, titled *A Study of Linewidths in Rydberg States of Atomic Sodium*, discussed light emissions from highly excited states of sodium atoms. In 1980, I received my Master's degree in Semiconductor Physics from the University of Illinois. And in 1985, I received my Ph.D. in Semiconductor Physics from the University of Illinois. My Ph.D. Thesis, titled *A Study of Electron Traps in VPE GaAs Grown With Added Oxygen*, discussed impurities and defects in semiconductors.

7. I am currently a consultant to the photovoltaics ("PV") industry, specializing in PV cell and system design and performance modeling, PV cell and module test procedures, measurement protocols and performance analysis, and PV cell module fabrication process development. My work typically includes but is not limited to (1) working with PV cell manufacturers to improve the performance and reduce the cost of their cell designs and fabrication processes, (2) providing due diligence and technical expertise on technology selection, conceptual layouts, specification development, and energy production estimates for PV power plant proposals, (3) using numerical modeling to pinpoint sources of loss mechanisms and to determine technical requirements necessary for cost-effective PV cell and module performance, (4) providing expert witness services for legal proceedings requiring photovoltaic technology expertise, (5) writing and presenting short

courses on Silicon PV Manufacturing and Technology to PV manufacturers worldwide, and (6) providing PV module, array and system performance measurements and comparison with energy-production model predictions.

8. From 1985 to 2008, I was a principal member of the technical staff at the Sandia National Laboratories in Albuquerque, NM. The work I performed there include but is not limited to (1) acting as Team Leader of PV Cell Development Team and the \$2M/year semiconductor fabrication facility, where I directed 7 team members, authored annual operating plan, directed all PV cell research projects, and was responsible for tasks and milestones of Si cell research and maintaining quality control, (2) acting as director of Crystalline Silicon Research Cooperative, a government/industry consortium for mutually beneficial research consisting of representatives from the entire US Si-PV manufacturing and research communities, (3) acting as contract monitor and advisor for several R&D contracts in the DOE Concentrator Initiative Program from 1990 to 1993, where I was closely involved and providing technical feedback for manufacturers developing Concentrator Photovoltaics systems, (4) acting as a charter member of the PV Manufacturing Technology Program Implementation Committee, a DOE/National Lab group directing \$11M/year in industry-contracted DOE research, (5) successfully led two 3-year competitively awarded projects as Principal Investigator in silicon solar cell processing, submitting original proposals, building

successful interdisciplinary teams, authoring review presentations, and meeting all milestones. (6) initiated and directed a graduate student research program at the University of New Mexico with Professor Charles Fleddermann, resulting in several graduate student thesis projects in solar cell fabrication processing to improve solar cell performance, (7) authored competitively evaluated proposal to DOE Hydrogen Program to lead a multidisciplinary team in a project to improve efficiency and cost-effectiveness of PV-powered water-electrolysis for hydrogen production, (8) served as subarea chairman of 2000 IEEE PV Specialists Conference in Silicon Cell Processing, (9) served as Session Chairman of PV session at 1999 ASME Renewable Energy Conference, (10) directed graduate student research program contract at Georgia Institute of Technology with Professor Ajeet Rohatgi, and managed a \$2.8M solar cell research and development contract, and (11) initiated and successfully conducted several direct industry joint experiments with most major US Si solar cell manufacturers, resulting in numerous publications and several process improvements adopted by industry into manufacturing production lines.

9. Beyond my academic experience, I have significant professional experience in the field of PV technology. In 1993, I designed and fabricated the world's first 20% efficient Si concentrator solar cell on low-cost Si. In 1999, I received the Best Paper Award at the ASME Renewable Energy Conference.

10. My work has been published in over 60 publications since 1981, including over 50 publications on my work with solar cell technologies. A complete list of my publications and publication metrics are listed on pages 12-18 of my CV.

11. I am an inventor on 5 issued U.S. patents related to solar cell technologies. A complete list of my patents can be found on pages 6-7 of my CV.

III. DOCUMENTS CONSIDERED

12. In formulating my opinions, I have considered the documents cited in this declaration and the following:

- Petition for *Inter Partes* Review of U.S. Patent No. 8,878,053 (Paper 3)
- U.S. Patent No. 8,878,053 (Ex. 1001)
- File History of U.S. Patent No. 8,878,053 (Ex. 1002)
- Declaration of Dr. Zachary Holman in Support of Petition for *Inter Partes* Review of U.S. Patent No. 8,878,053 (Ex. 1003)
- EP17322142A1 to Armin Froitzheim (“Froitzheim”) (Ex. 1004)
- Gan and Swanson, *Polysilicon Emitters for Silicon Concentrator Solar Cells*, IEEE Conference on Photovoltaic Specialists, Vol. 1, Pages 245-240 (1990) (“Gan”) (Ex. 1005)
- WO 2009/094575 A2 (“Borden-575”) (Ex. 1006)
- U.S. Patent No. 6,998,288 to Smith (“Smith”) (Ex. 1005)
- CN 1949545A to Li (Translation) (“Li”) (Ex. 1008)
- Zachary C. Holman, *Electron Transport in Amorphous Silicon* (May 2005) (Thesis Presented to The Division of Mathematics and Natural Sciences, Reed College) (“Holman-Thesis”) (Ex. 1010)
- U.S. Patent No. 7,468,485 to Swanson (“Swanson”) (Ex. 1015)
- R. J. Komp, *Practical Photovoltaics Electricity From Solar Cells*, 3rd Ed. (2002) (“Komp”) (Ex. 1016)

- BP Solar Global Marketing, BP-MSX-120, 120-Watt Multicrystalline Photovoltaic Module (“BP-MSX-120”) (Ex. 1017)
- J. Nelson, *The Physics of Solar Cells*, Imperial College Press (2003) (“Nelson”) (Ex. 1018)
- T. Krygowski, A. Rohatgi, D. Ruby, *Simultaneous P and B Diffusion, In-Situ Surface Passivation, Impurity Filtering and Gettering for High-Frequency Silicon Solar Cells*, SAND-97-2620C; CONF-970953- (“Krygowski”) (Ex. 1019)
- A. Luque, S. Hegedus, *Handbook of Photovoltaic Science and Engineering*, Wiley (2003) (“Luque”) (Ex. 1020)
- J. Gordon, *Solar Energy the State of the Art*, ISES (2001) (“Gordon”) (Ex. 1021)
- U.S. Patent No. 6,262,359 to Meier (“Meier”) (Ex. 1022)
- U.S. Patent No. 4,525,593 to Yablonovitch (“Yablonovitch”) (Ex. 1023)
- WO 2009/094578 A2 (“Borden-578”) (Ex. 1024)
- U.S. Patent No. 4,665,277 to Sah (“Sah”) (Ex. 1025)
- D. Chapin et al., *A New Silicon P-N Junction Photocell for Converting Solar Radiation into Electrical Power*, J. Appl. Phys. 25, 676 (1954) (“Chapin”) (Ex. 1026)
- W. Shockley, H. J. Queisser, *Detailed Balance Limit of Efficiency of pn Junction Solar Cells*, J. Appl. Phys. 32, 510 (1961) (“Shockley”) (Ex. 1027)
- A. Metz, R. Meyer, B. Kuhlmann, M. Grauvogl, R. Hezel, *18.5% Efficient First-Generation MIS Inversion-Layer Silicon Solar Cells*, 26th PVSC (1997) (“Metz”) (Ex. 1029)
- D. De Ceuster, P. Cousins, D. Rose, D. Vicente, P. Tipones, W. Mulligan, *Low Cost, High Volume Production of >22% efficiency silicon solar cells*, 22nd European Photovoltaic Solar Energy Conference, 3-7 September 2007, Milan, Italy, pp. 816-819 (“De-Ceuster”) (Ex. 1029)
- J. Benick, J. Rentsch, Ch. Schetter, C. Voyer, D. Biro, R. Preu, *PECVD PSG as a Dopant Source for Industrial Solar Cells*, Presented at the 21st European Photovoltaic Solar Energy Conference, September 4-8, 2006, Dresden (2CV.4.26) (“Benick”) (Ex. 1030)
- Translation Declaration for JP07-106611 to Okayasu (Ex. 1032)
- Robert F. Pierret, *Semiconductor Device Fundamentals*, Addison Wesley Longman (Part I) (1996) (“Pierret”) (Ex. 1033)

- A. I. A. Rahim, C. D. Marsh, P. Ashburn, G. R. Booker, *Impact of Ex-Situ and In-Situ Cleans on the Performance of Bipolar Transistors With Low Thermal Budget In-Situ Phosphorus-Doped Polysilicon Emitter Contacts*, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 48, NO. 11 (November 2001) (“Rahim”) (Ex. 1034)
- N. S. Parekh, R. V. Taylor, D. O. Massetti, *A Simple Method to Control Bipolar Polysilicon Emitter Interfacial Oxide*, J. Electrochem. Soc., Vol. 141, No. 11, pp. 3167-3172 (1994) (“Parekh”) (Ex. 1035)
- E. Yablonovitch, T. Gmitter, R. M. Swanson, Y. H. Kwark, *A 720 mV open circuit voltage SiO_x:c-Si:SiO₂ double heterostructure solar cell*, Appl. Phys. Lett. 47, 1211–1213 (1985) (“Yablonovitch-1985”) (Ex. 1036)
- File History of U.S. Patent App. No. 14/504,771 (“771FH”) (Ex. 1039)
- U.S. Patent No. 8,222,516 B2 (“the ’516 patent”) (Ex. 1040)
- U.S. Patent Appl. Pub. No. 2002/0142500 A1 (“Foglietti”) (Ex. 1042)
- Mark John Kerr, *Surface, Emitter and Bulk Recombination in Silicon and Development of Silicon Nitride Passivated Solar Cells* (2002) (Ph.D. Thesis, The Australian National University) (“Kerr”) (Ex. 1043)
- M. Green, *Silicon Solar Cells Advanced Principles & Practice*, Centre for Photovoltaic Devices and Systems (1995) (“Green-1995”) (Ex. 1045)
- Y. H. Kwark, R. M. Swanson, *N-Type Sipos and Poly-Silicon Emitters*, Solid-State Electronics Vol. 30, No. 11, pp. 1121-25 (1987) (“Kwark”) (Ex. 1046)
- G. R. Wolstenholme, N. Jorgensen, P. Ashburn, G. R. Booker, *An investigation of the thermal stability of the interfacial oxide in polycrystalline silicon emitter bipolar transistors by comparing device results with high-resolution electron microscopy observations*, J. Appl. Phys. 61, 225-33 (1987) (“Wolstenholme”) (Ex. 1047)
- M. Green, *Solar Cells Operating Principles Technology and System Applications* (1986) (“Green-1986”) (Ex. 1049)
- N. G. Tarr, *A polysilicon emitter solar cell*, IEEE Electron Device Letters, vol. 6, no. 12, pp. 655-658, Dec. 1985 (“Tarr”) (Ex. 1050)
- R. M. Swanson, *Point Contact Solar Cells: Modeling and Experiment*, Solar Cells, 17, pp. 85-118 (1986) (“Swanson-1986”) (Ex. 1051)
- U.S. Patent No. 4,158,591 to Avery (“Avery”) (Ex. 1052)

- U.S. Patent No. 5,899,804 to Schlosser (“Schlosser”) (Ex. 1053)
- U.S. Patent No. 7,144,751 to Gee (“Gee”) (Ex. 1054)
- WO 2006/097303 A1 (“Agostinelli”) (Ex. 1056)
- P.V. Meyers, R. Kee, C. Wolden, L. Raja, V. Kaydanov, T. Ohno, R. Collins, M. Aire, J. Kestner, A. Fahrenbruch, *Atmospheric Pressure Chemical Vapor Deposition of CdTe for High Efficiency Thin Film PV Devices*, NREL Annual Report 26 January 1998 – 25 January 1999 (Sept. 1999) (“NREL-1999”) (Ex. 1057)
- R. M. Swanson, R. A. Sinton, *High-Efficiency Silicon Solar Cells, Advances in Solar Energy: An Annual Review of Research and Development*, vol. 6. Chapter 4 (1990) (“Swanson-1990”) (Ex. 1058)
- G. Lubberts, B. C. Burkey, F. Moser, E. A. Trabka, *Optical properties of phosphorus-doped polycrystalline silicon layers*, J. Appl. Phys. 52(11), (Nov. 1981) (“Lubberts”) (Ex. 1059)
- U.S. Patent No. 6,352,876 to Bordogna (“Bordogna”)
- E. Centurioni, D. Iencinella, R. Rizzoli, F. Zignani, *Silicon Heterojunction Solar Cell: A New Buffer Layer Concept With Low-Temperature Epitaxial Silicon*, IEEE Transactions on Electron Devices, Vol. 51, No. 11 (November 2004) (“Centurioni”) (Ex. 1061)
- M. Farrokh-Baroughi, H. El-Gohary, S. Sivoththaman, *Optical, Electrical, and Structural Properties of PECVD Quasi Epitaxial Phosphorous Doped Silicon Films on Crystalline Silicon Substrate*, Canadian Solar Buildings Conference (August 20-24, 2004) (“Farrokh-Baroughi”) (Ex. 1062)
- Gan, Jon-Yiew, Polysilicon emitters for silicon concentrator solar cells, Stanford University (July 1990) (“Gan Thesis”) (Ex. 2003)
- Feldmann, et al., “A Passivated Rear Contact for High-Efficiency n-Type Silicon Solar Cells Enabling High VocS and FF > 82%” (28th European PV Solar Energy Conference & Exhibition, Paris, Sept. 30 – Oct. 4, 2013) (Ex. 2010)
- Declaration of Mary K. Bolin, Ph.D. (Ex. 2026)
- Transcript of Deposition of Dr. Zachary Holman, taken May 8, 2025 (Ex. 2029)

IV. ASSUMPTIONS

A. Date of Invention

13. Patent Owner's counsel asked me to assume that the date of the inventions of the claims of the '053 patent was February 20, 2008.

B. Person of Ordinary Skill in the Art

14. Petitioner asserts the following qualifications for a POSITA:

A POSITA at the priority date of the '053 patent (February 20, 2008) would have had (i) an advanced degree in electrical engineering, mechanical engineering, applied physics, chemistry, materials science, or a related discipline and (ii) at least one year of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. Alternatively, a POSITA would have had (i) a bachelor's degree in the aforementioned disciplines and (ii) at least two years of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. Less work experience may be compensated by a higher level of education, and vice versa.

Paper 3, 16 (citing Ex. 1003, ¶¶36-41).

15. For this declaration, Patent Owner's counsel asked me to apply Petitioner's qualifications for a POSITA.

16. At the time of the inventions of the claims of the '053 patent, I was aware of the understandings and capabilities of a person having the skill level described above. This awareness was informed by my experience in academia

where I worked with many persons that possessed such a level of skill at and around the time of the invention.

V. RELEVANT PATENT LAW STANDARDS

A. Claim Construction

17. I understand that patent claim terms are generally given their ordinary and customary meaning as understood by a POSITA in the art when read in the context of the specification and prosecution history. Two exceptions are when (1) the patentee acts as their own lexicographer, or (2) the patentee disavows the full scope of the claim term.

18. I also understand that, in construing the claims, the analysis should focus on the words of the claims. However, patent claims are not read in a vacuum and should instead be read in view of the specification and prosecution history, i.e., the back-and-forth correspondence between the patent applicant and the U.S. Patent and Trademark Office. I further understand that the patent specification is the single best guide to the meaning of a claim term. Thus, a construction that is not supported by the specification should be rejected, even if that construction is plausible, if divorced from the specification. However, it is improper to read limitations from the specification into a claim absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited. At bottom, the interpretation to be given a claim term can be determined and confirmed only

with a full understanding of what the inventors actually invented and intended to envelop with the claim.

B. Obviousness

19. I understand that a determination that a claim is “obvious” is based on underlying factual issues including the content of the prior art and the level of skill in the art. I understand that for a single prior art reference or a combination of prior art references to render a claim obvious, and thus unpatentable, a POSITA in the art must have been able to arrive at the claim by altering or combining the references. I have been informed that all elements of a claim must be considered in an obviousness analysis.

20. I further understand that when considering the obviousness of a patent claim, one should consider whether a teaching, suggestion, or motivation to combine the references exists so as to avoid impermissibly applying hindsight when combining or modifying the prior art. I understand that this test should not be applied rigidly, but that the test can be important to avoid such hindsight.

21. I have been informed that, for a claim to have been obvious, a POSITA must have had a reasonable expectation of success in combining or modifying prior art references to arrive at the claim. I understand that absolute predictability is not required. I further understand that the test is reasonable probability of success not some degree of unpredictability.

C. Standard of Proof

22. I understand that the standard to prove unpatentability is by a preponderance of the evidence, which means more likely than not.

VI. BACKGROUND OF THE '053 PATENT AND RELATED TECHNOLOGY

23. The '053 patent “relates generally to solar cells.” Ex. 1001, 1:21. According to the '053 patent, “[s]olar cells are well known devices for converting solar radiation to electrical energy.” Ex. 1001, 1:25-26. This field is also known as photovoltaics.

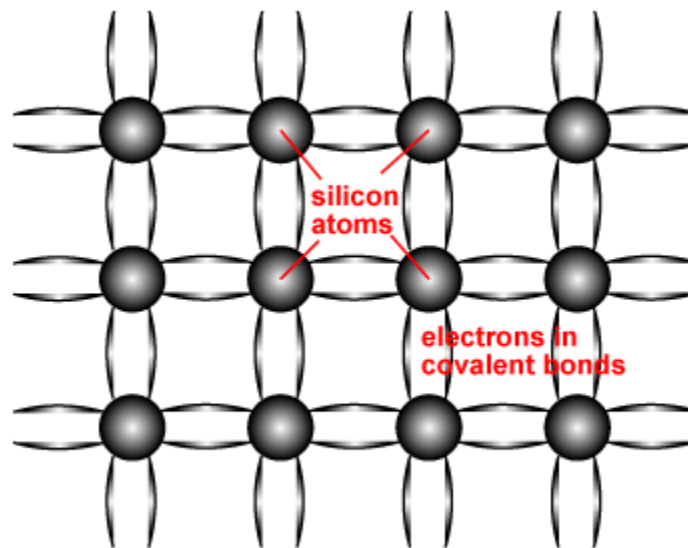
A. Theory of Converting Solar Energy into Electricity

24. Sunlight is composed of a flux of individual particles called photons. A photon is characterized by its wavelength, λ , or its energy, E . The total radiant power emitted from the sun is composed not of a single wavelength, but of many wavelengths and, therefore, does not appear as individual colors to the human eye.

25. According to the '053 patent, solar cells “may be fabricated on a semiconductor wafer.” Ex. 1001, 1:26-27. One type of semiconductor uses a silicon (Si) substrate which is made up of individual Si atoms bonded together in a regular, periodic structure to form an arrangement whereby each atom is surrounded by eight electrons. Each silicon atom has four valence electrons which

are individually shared with those of four neighboring Si atoms, forming four covalent bonds with the four surrounding Si atoms.

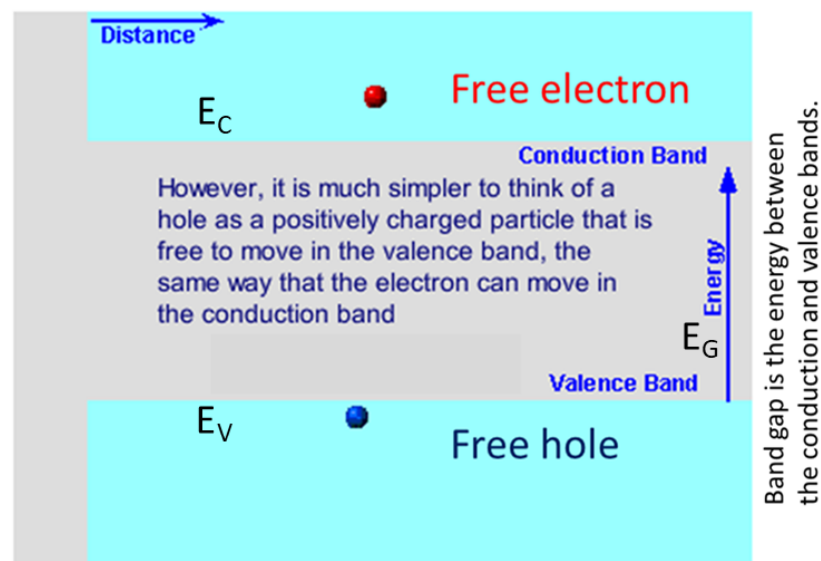
26. Below is a schematic representation of covalent bonds in a silicon crystal lattice. Each line connecting the atoms represents an electron being shared between two atoms. Two electrons being shared are what form the covalent bond.



27. The lowest energy position for an electron to be in is its bound state. If the electron has enough thermal energy to break free of its bond, then it becomes free and available for electric conduction (in the conduction band). The electron cannot attain energy values intermediate to these two levels; it is either at a low energy position in the valence band (valence electron) or it has gained enough energy to break free and contribute to conduction (jumps to conduction band). The

minimum energy required is the difference between conduction and valence band energies and is called the “band gap” of a semiconductor.

28. The vacancy left behind by an electron that has been promoted to the conduction band allows the empty covalent bond to move freely from one atom to another, acting like a positive charge moving through the crystal lattice, much like a bubble moving through a liquid. This empty bond is commonly called a “hole” and acts like a positive charge with unique properties such as mass and mobility, and also contributes to conduction. The lower energy level is E_V and the energy level at which an electron can be considered free is E_C . The band gap (E_G) is the distance between the conduction band and valence band.



B. Doping

29. It is possible to shift the balance of electrons and holes in a silicon crystal lattice by “doping” it with other atoms. Donor atoms with one more valence

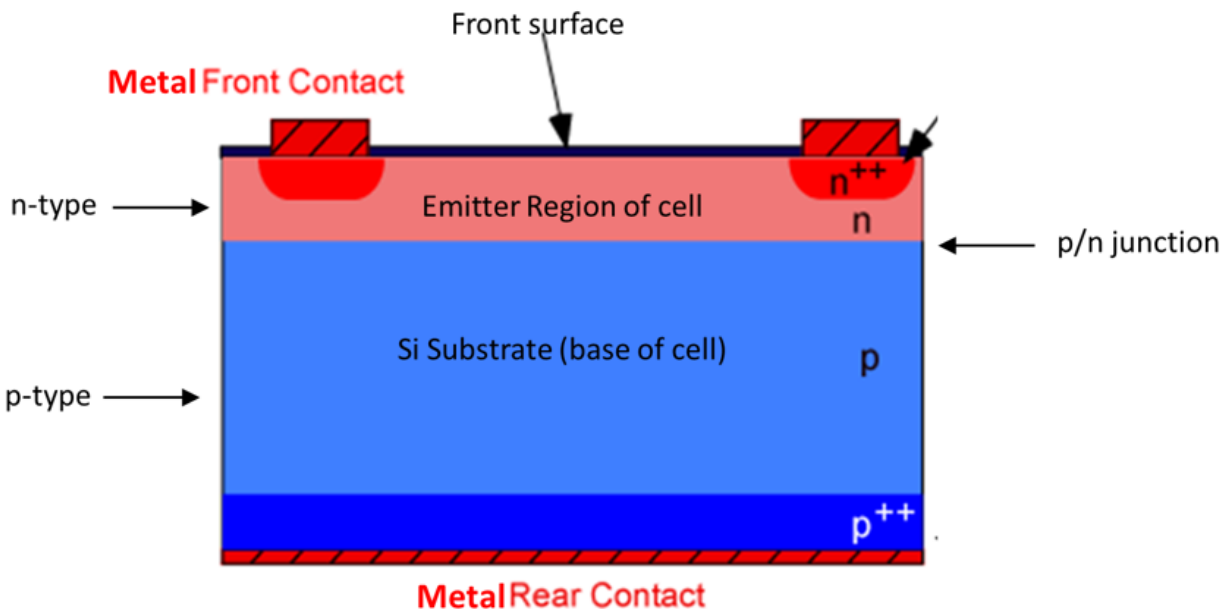
electron than silicon are used to produce “N-type” semiconductor material, which adds electrons to the conduction band and hence increases the number of free electrons (negatively charged carriers). Acceptor atoms with one fewer valence electron result in “P-type” material. In P-type material, the number of electrons missing from covalent bonds is higher, thus effectively increasing the number of free holes (positively charged carriers). In doped material, there is always more of one type of carrier than the other and the type of carrier with the higher concentration is called a “majority carrier,” while the carrier with lower concentration is called a “minority carrier.”

C. Annealing

30. Annealing is a general term for a process during which the atoms of a material are given enough time and thermal energy to find and relax into their lowest energy state.

D. Solar Cell Structure

31. According to the '053 patent, a solar cell has a “front side” that “faces the sun during normal operation to collect solar radiation.” Ex. 1001, 1:39-41. Opposite the front side is the backside. *Id.* at 1:40. This is illustrated in the following diagram of a generic solar cell.



1. *Junctions*

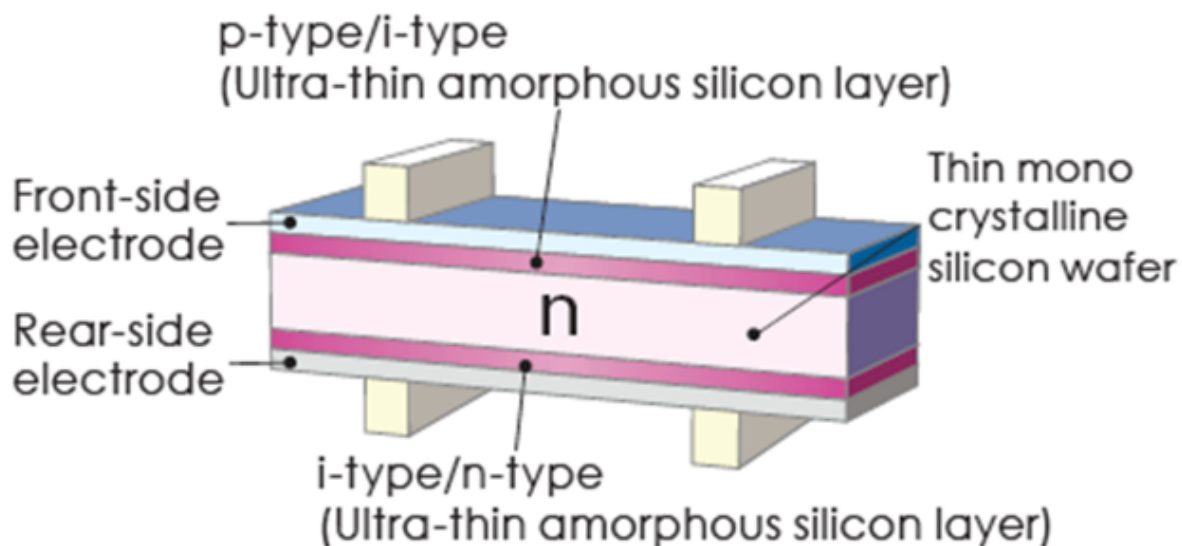
32. A junction is a general term for a region of a semiconductor device where the properties of the material on one side are dissimilar in some way from those on the other side. These can include homojunctions where the two regions are each made of the same material but have different electrical properties, or heterojunctions where the two regions are actually made of different materials with differences in crystal structure, chemical composition, bandgap, or other molecular properties. Claims 9 and 16 in '053 patent recite forming a poly-Si layer on a Si substrate. This material discontinuity constitutes a heterojunction.

a. Heterojunction

33. As noted, a heterojunction is formed by joining of dissimilar materials in contact with a semiconductor substrate. This can be a poly-Si layer, as in the

'053 patent, or an amorphous Si (a-Si) layer as shown below in the famous heterojunction cell invented by Sanyo Corporation. It is the abrupt change in material properties between the c-Si and the a-Si which lead to the excellent performance of this type of solar cell, which held the world record for energy conversion efficiency for many years.

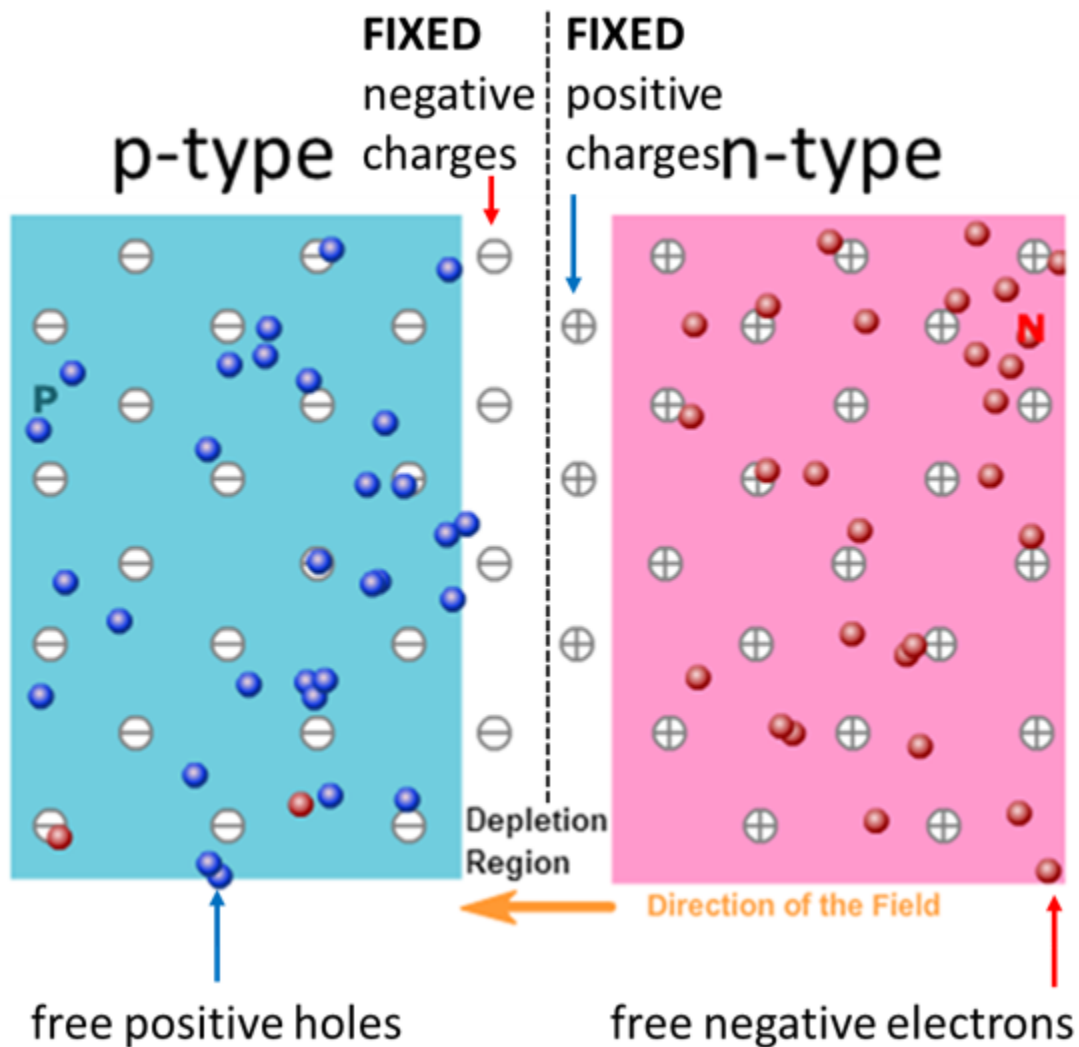
SANYO HIT[®] Solar Cell Structure



b. P-N Junction

34. An example of a P-N junction is that region of a solar cell where a P-type Si base adjoins directly with an N-type emitter region. This can be created by heavily doping a P-type Si substrate with N-type dopant atoms until a shallow layer of N-type Si is formed near the surface of the substrate. Since the N-type region has a high electron concentration and the P-type a high hole concentration,

electrons diffuse from the N-type side to the P-type side and holes flow by diffusion from the P-type side to the N-type side. Diffusion in semiconductors is the motion of charge carriers due to their concentration gradient.



35. After the electrons and holes move to the other side of the P-N junction, they leave behind exposed charges on dopant atom sites, which are fixed in the crystal lattice and are unable to move. On the N-type side, positive ion cores

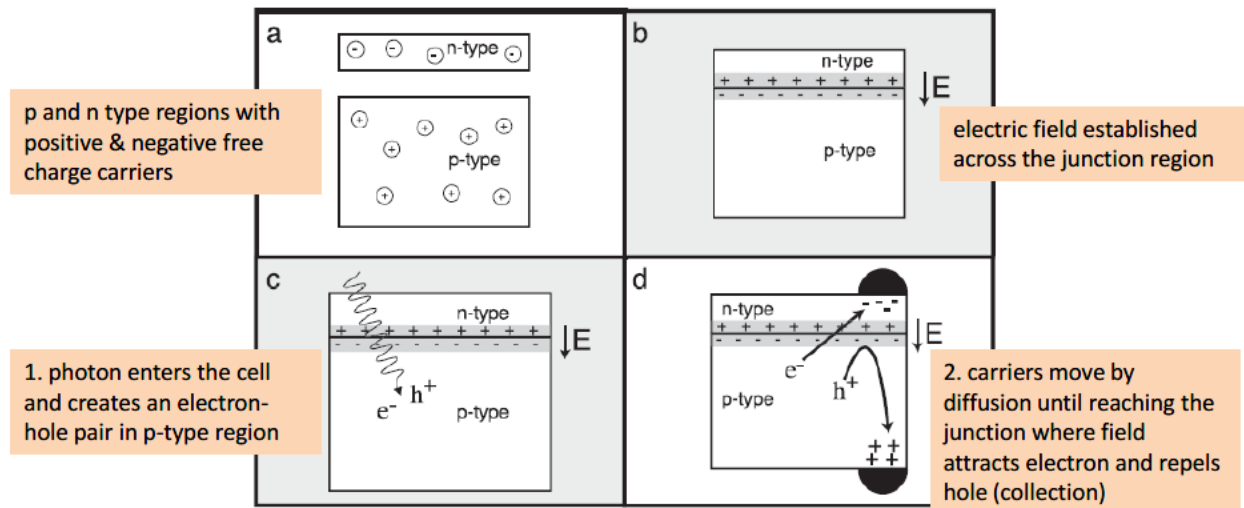
are exposed with donor charge density N_D . On the P-type side, negative ion cores are exposed with acceptor charge density N_A .

36. A built-in electric field $\hat{E}$ forms between the positive ion cores in the N-type material and negative ion cores in the P-type material. This region is called the "depletion region" since the electric field there quickly sweeps any free carriers across, hence the region is depleted of free carriers. This region extends further into the more lightly doped side to expose an equal number of fixed ion cores as on the more heavily doped side.

37. A solar cell absorbs light to generate electric power. This is a three-step process: First, it absorbs as much sunlight as possible through the front side of the solar cell to photogenerate electrons and holes. In a doped region, the increase in photogenerated majority carriers is just a tiny fraction of the majority carriers already present, so these have little effect.

38. Second, since the photogenerated minority carriers represent a large increase in the number of minority carriers present, the process of diffusion of these minority carriers towards the depletion region at the P-N junction naturally takes place. These minority carriers diffuse a distance of what is called the minority carrier diffusion length, which is the average distance they can diffuse before recombining during the average minority carrier lifetime.

39. Third, the electric field present at the junction then sweeps the minority carriers across, at which point they are collected and simply need to pass through contacts into the external circuit.



40. As shown above, in box (a), the basic structure of a solar cell may include an N-type region with negative free charge carriers on the front side, and P-type region with positive free charge carriers on the backside.

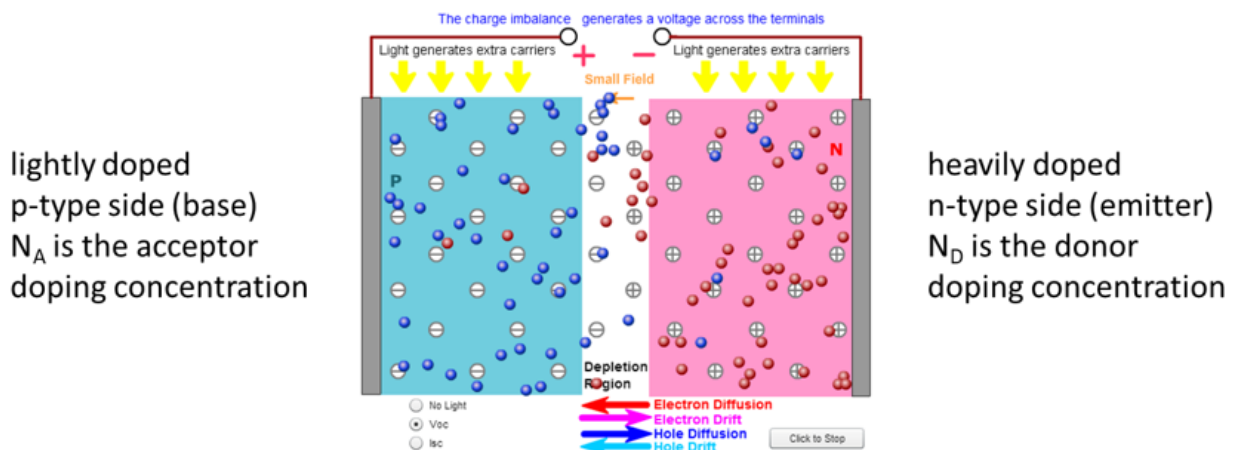
41. In box (b), a built-in electric field is shown to be established across the P-N junction region.

42. In box (c), upon absorbing sunlight, a photon enters the solar cell. If the photon has an energy greater than that of the band gap, an electron-hole pair can be photogenerated, in this instance, in the p-type region.

43. In box (d), the minority carrier electrons move by diffusion until reaching the P-N junction region where they are swept across by the built-in

electric field there. Specifically in the case shown here, the electron is swept across the junction and becomes a majority carrier in the N-region where it can then no longer recombine since there are so few holes present there. The photogenerated hole is repelled by the junction electric field and increases the majority carrier hole concentration slightly in the P-region. This buildup of charged majority carriers creates a voltage across the P-N junction. If an external circuit is present, these excess majority carriers can be pushed through low-resistance metal contacts, thereby generating a negative photocurrent in the circuit and delivering electric power.

44. To generate power, a voltage must be generated as well as a current. If light-generated carriers are prevented from leaving the solar cell (such as in the case of an open-circuit shown below), the number of electrons on the N-side and holes on the P-side increase. This creates an electric field at the P-N junction opposite to the built-in field.



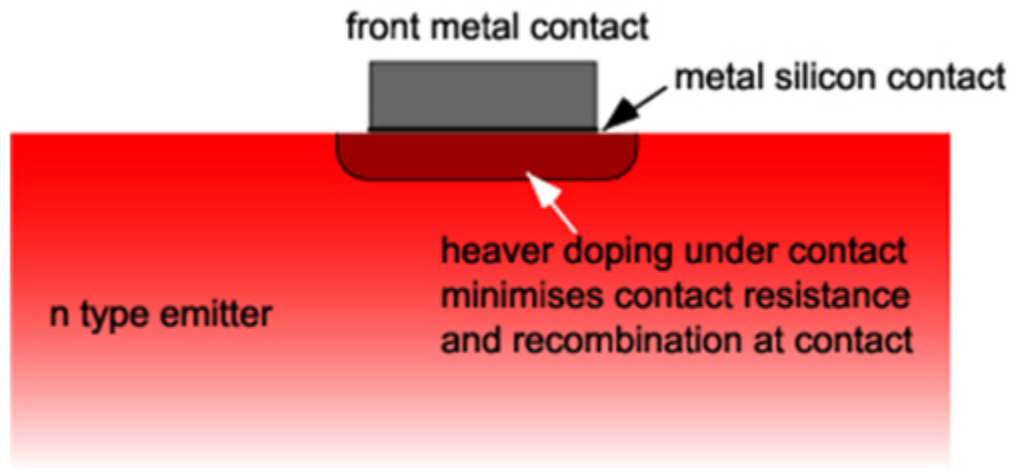
45. This forward voltage across the junction creates a forward bias current, which exactly balances the negative photogenerated current, so the net current is zero at open circuit. The voltage to cause these two currents to exactly balance is called the “open-circuit voltage.” In actual operation, the voltage across the cell is maintained at a slightly lower value so that current can be delivered to an external circuit at the maximum power point. These operating parameters are known as the max power voltage and max power current.

46. The above discussion assumes a P-type substrate doped with N-type dopants to form the emitter. A P-N junction can also be formed with an N-type substrate doped with P-type dopants to form a P-type emitter. Non-asserted claim 1 of the ‘053 patent is directed to such a junction structure. Moreover, as recited in claims 9 and 16 providing a poly-Si layer on the back side of a crystalline silicon substrate also forms a junction, *i.e.*, a heterojunction.

2. *Emitter*

47. In a semiconductor device, the emitter of the device is usually defined as the region which is doped to have the opposite majority carrier polarity compared to the substrate. However, as in claim 9 of the ‘053 patent, the emitter can be a polysilicon layer on the back side of the substrate. Ex. 1001, 6:57-59.

3. *Contacts*



48. The contacts of a solar cell are metal regions deposited on the cell surface intended to conduct the photogenerated current from the semiconductor to an external circuit.

E. Types of Solar Cells: One Sun and Concentrator Solar Cells

49. Solar cells designed for use on earth rather than in outer space are called terrestrial cells as opposed to space cells. Terrestrial cells can be further divided into cells designed to use normal sunlight (one-sun cells) and those designed to use concentrated sunlight (concentrator cells).

50. The distinguishing characteristic of concentrator cells is that they generate many times more free carriers than one sun solar cells do, requiring concentrator solar cells to have a much lower series resistance from the substrate through the emitter, contacts, and gridlines than in a one sun solar cell.

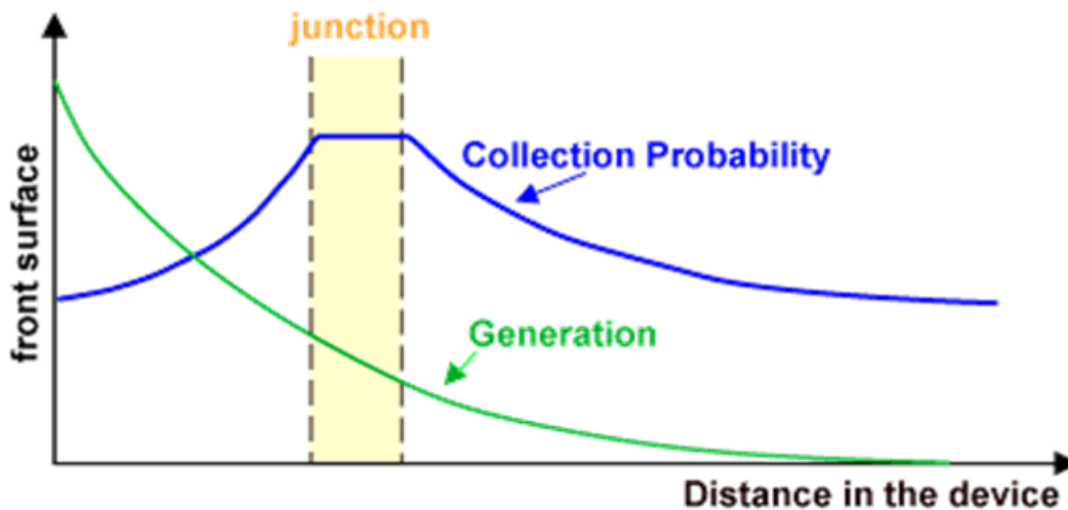
51. In particular, the contact resistances must be much lower than those of one-sun cells, and the metal gridlines are usually much thicker to reduce gridline resistance.

F. Solar Cell Efficiency

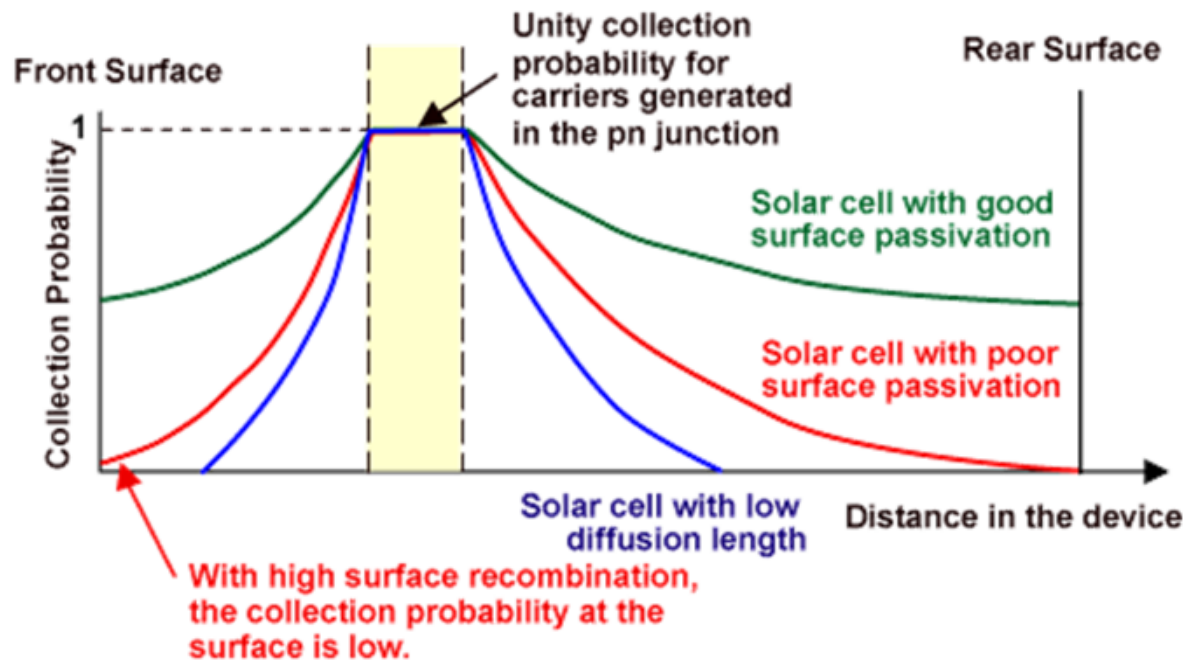
52. The overarching goal of the solar cell industry is to increase the efficiency of the solar cell, which is the ratio of electrical power output at the max power point to the photo power incident in the incoming sunlight. This is achieved by maximizing light absorption, reducing photocarrier recombination to increase current and voltage, and maintaining low electrical resistance within the cell.

1. Recombination and Passivation

53. The free electrons photogenerated by absorbed sunlight can recombine with any free holes present by falling back into the covalent bond vacancies, in which case neither free carrier can contribute to conduction any longer. Most photogeneration takes place close to the front surface of the cell where the light is mainly absorbed. The probability that photocarriers will be collected by the junction decreases with distance from the junction.

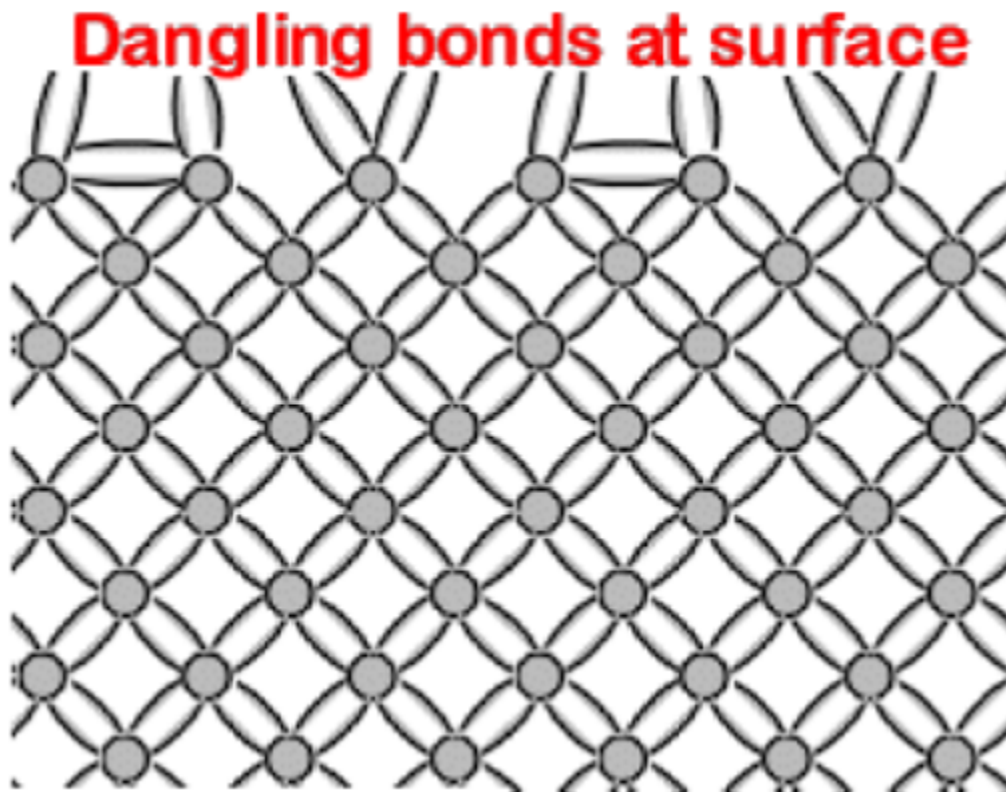


54. The mean time that free carriers exist before recombination is called the minority carrier lifetime. The distance they can diffuse during this time is called the minority carrier diffusion length. This is sometimes measured as a saturation current density called J_0 . The goal of effective solar cell design is to minimize this recombination by maximizing carrier lifetimes and diffusion lengths, thereby keeping J_0 low.



55. Defects at either surface of the semiconductor wafer or impurities within it increase the level of recombination occurring in each of these areas, thereby decreasing the concentration of photogenerated carriers available to generate current and voltage. Each of these regions can be characterized by its own J_0 value, which all add together to determine overall cell efficiency. Effective solar cell design implements the invention and inclusion of critical features to reduce the amount of recombination occurring at surfaces, which is known as surface passivation.

56. The surface of a solar cell represents a severe disruption of the periodic crystal lattice, and these surfaces of the solar cell are a site of particularly high recombination unless they are effectively passivated.



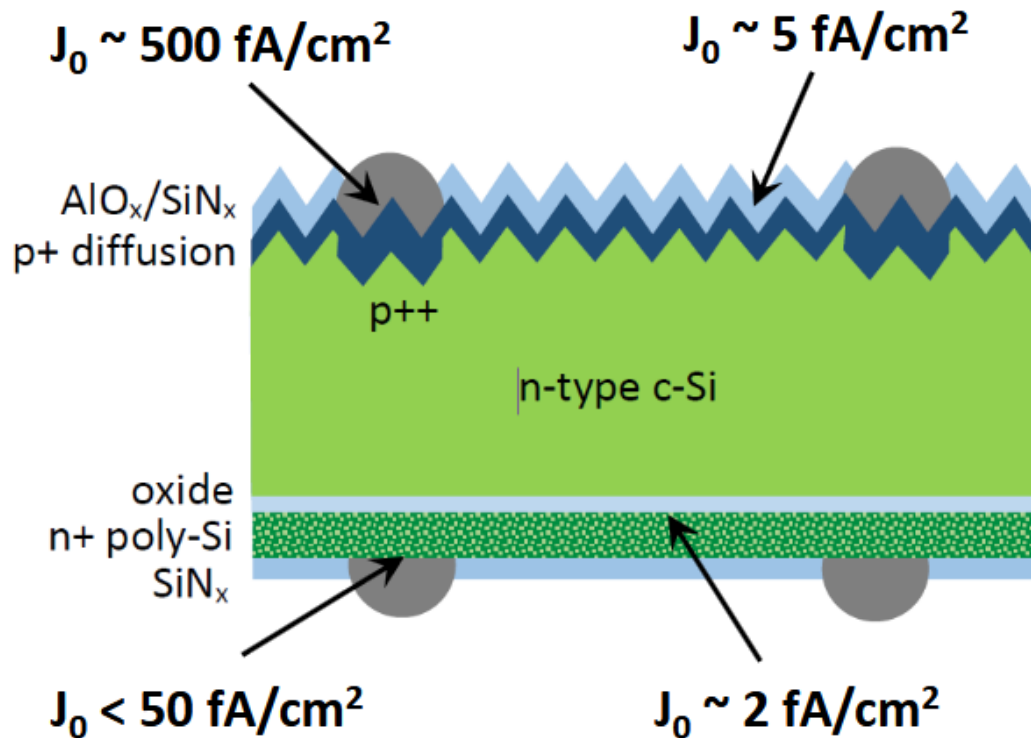
57. The defects at a semiconductor surface are caused by the interruption to the periodicity of the crystal lattice, which causes dangling bonds to form at the semiconductor surface where high levels of recombination can occur. The high recombination rate in the vicinity of a surface reduces the concentration of minority carriers in this region.

58. The reduction of the number of dangling bonds, and hence surface recombination, is often achieved by carefully growing a matching layer on top of the semiconductor surface, whose chemical structure is perfect for tying up some of these dangling bonds. This reduction of dangling bonds is known as surface

passivation. Thermally grown silicon dioxide (SiO_2) is an excellent match for passivating Si surfaces. This oxide is carefully grown at high temperatures in a clean environment containing only oxygen and possibly some inert gas. This thermal oxide needs to be differentiated from the many other types of oxides that can be found on Si surfaces, such as chemical oxides produced at room temperature.

59. The amount of recombination can be quantified by measuring J_0 , which represents recombination in a region of the cell, and is related to the voltage a cell can deliver. Specifically, it is related to the mean lifetime of minority carriers before they recombine. A low J_0 indicates less recombination. This means that more carriers migrate outside the cell and deliver useable power, thereby increasing cell conversion efficiency.

60. A good TOPCon one sun cell, shown in the literature in 2023, such as the one shown by MacDonald in Figure 1 below has rear surface J_0 of $2 \text{ fA/cm}^2 = 2 \times 10^{-15} \text{ A/cm}^2$. This is about 5-30 times lower than that of the concentrator cell, which is the subject of Kwark's experiments (discussed below), and 10-25 times lower than the results of Gan's experiments. Gan is also directed to a concentrator cell.

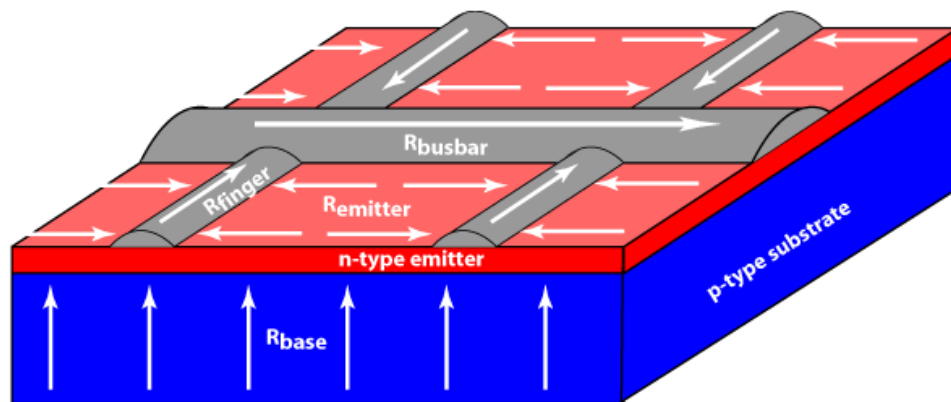


D. MacDonald, Achieving 26% silicon solar cells in mass production with passivating contacts – TOPCon or heterojunctions? Australian National University, UNSW School of Photovoltaic & Renewable Energy Engineering (Sept. 2023) (<https://www2.pv.unsw.edu.au/videos/Daniel-Macdonald-7September2023/slides/UNSW-SPREE-seminar-Sept-2023-DanM.pdf>).

2. Resistance

61. Series resistance in solar cells reduces their efficiency by dissipating power in the cell that would otherwise be delivered to an external circuit. The most common parasitic resistances are series resistance and shunt resistance.

62. Series resistance in a solar cell has three causes: (1) the movement of current through the emitter and base of the solar cell; (2) the contact resistance between the metal contacts and the substrate; and (3) the resistance of the top and rear metal contacts. The diagram below illustrates the components of series resistance:



63. The metallic top contacts are necessary to collect the current generated by a solar cell. “Busbars” are connected directly to the external metal ribbons in a solar panel, while “gridline-fingers” are fine areas of metallization which collect current for delivery to the busbars. A tradeoff is made by having sufficient metal coverage to reduce series resistance without shading too much of the cell, which reduces the capture of sunlight and, therefore, reduces current.

64. Series resistance due to contacts can be quantified as ρ_c , which represents the contact resistivity of any contact of a given area and is due to forcing the current from the Si to the metal of the contact. It is measured by sending

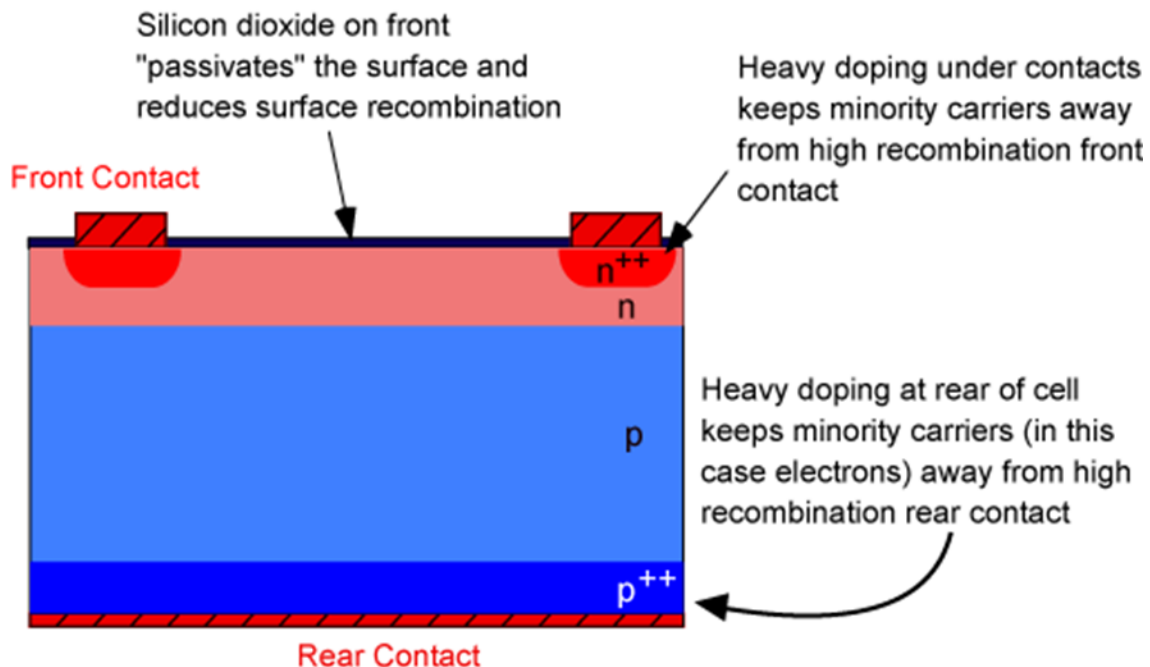
current through the contact, and measuring the voltage across the contact for various values of the current, or measuring the resistance of contacts of different areas, using Ohms Law, *i.e.*, $R=V/I$.

65. A high ρ_c results in excessive loss of power and lower efficiency. Total series resistance for one-sun cells such as described in the '053 patent typically needs to be less than 1 ohm-cm². Back contact resistance typically makes up about 1% of this, so it should be less than 1×10^{-2} ohm-cm². This is only one component of total series resistance, and all need to be optimized simultaneously along with allowing maximum light collection at the front surface to maximize cell efficiency. This involves several tradeoffs and careful optimization.

66. Series resistance is particularly problematic for concentrator solar cells. Concentrator solar cells use external optics to concentrate high intensity sunlight on a cell front surface resulting in much higher current generation. Due to Ohm's law, higher currents make it necessary to significantly reduce series resistance to keep voltage losses low. Simply put, the high level of current generated in concentrator cells increases the losses due to series resistance proportional to the ratio of the concentration intensity. For so-called concentrator cells, the series resistance needs to be made lower by the same ratio as the solar concentration ratio. For this reason, concentrator cells have a very different metal gridline structure than that of the one-sun cell shown above. Using the example of

acceptable contact resistivity for one-sun cells mentioned above, back contact resistivity for a concentrator cell operating at 100 suns concentration should be less than 1×10^{-4} ohm-cm².

67. A commonly used method to reduce contact resistivity is to selectively provide especially heavy doping concentration in emitter regions of the cell that are in direct contact with the metal contacts. This not only reduces contact resistivity, but also produces a slight electric field between the heavily doped region and the more lightly doped regions of the cell, which repels some of the minority carriers away from the metal contacts where they would otherwise certainly recombine.



68. This method of surface and contact passivation is known as field effect passivation because the weak electric field between the heavily and lightly doped regions does introduce a small barrier to minority carriers. The minority carrier concentration is then maintained at higher levels in the base region.

G. Solar Cell Design Principles

69. For one sun silicon solar cells, the design constraints caused by surface reflection, carrier collection, recombination, and resistance result in a maximum device efficiency of about 26%. To optimize solar cell performance, each objective must be pursued concurrently.

- Maximize the absorption of light and the generation of free carriers;
- Optimize collection of the photocarriers to deliver a current;
- Minimize recombination to generate a larger voltage; and
- Minimize dissipation of power in parasitic resistances.

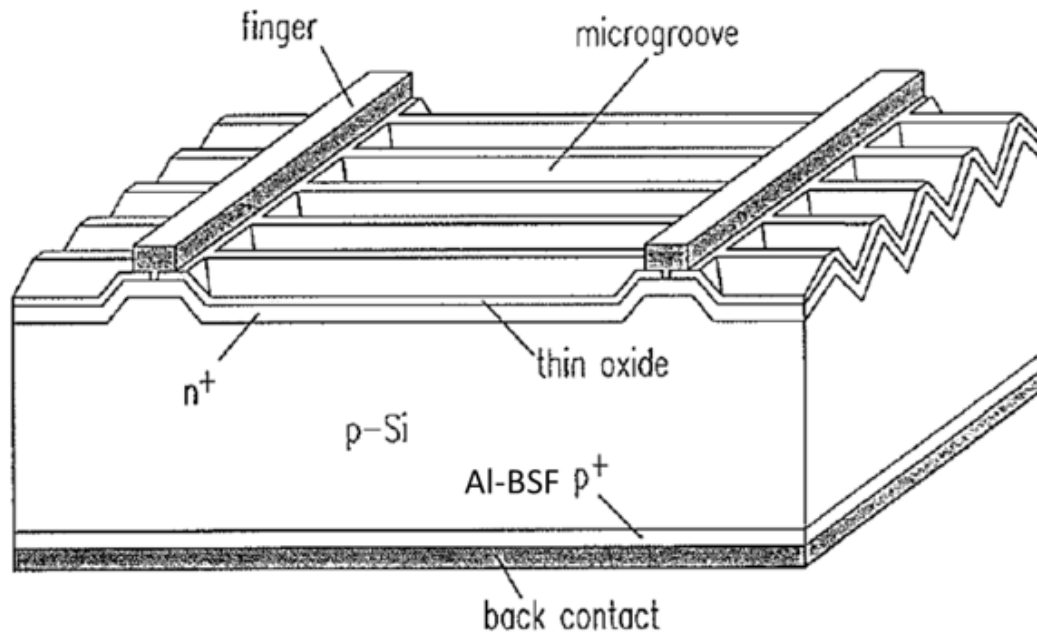
70. The '053 patent includes method claims that recite steps for making a solar cell that addresses improvements pertaining to the last two of these points, reducing recombination and parasitic resistance by reconfiguring the back surface of the cell to substantially reduce recombination there while still allowing the current to pass to the metal contacts with acceptably low resistance. This is done using a new method for back surface design by introducing two elements on the

back surface and forming a heterojunction comprised of a tunnel oxide layer and a heavily doped polysilicon (poly-Si) layer.

1. Passivated Emitter Solar Cells

71. Prior to the introduction of TOPCon solar cells, the most prevalent type of Si cells commercially produced were of the PESC, PERC or PERT type. The PESC (Passivated Emitter Solar Cell) was primarily focused on passivating the front emitter of the cell where most of the photogeneration takes place. A simple rear heavily diffused region using alloyed Al formed the back contact with a Back Surface Field (BSF).

The Passivated Emitter Solar Cell (PESC)



PESC

PERC

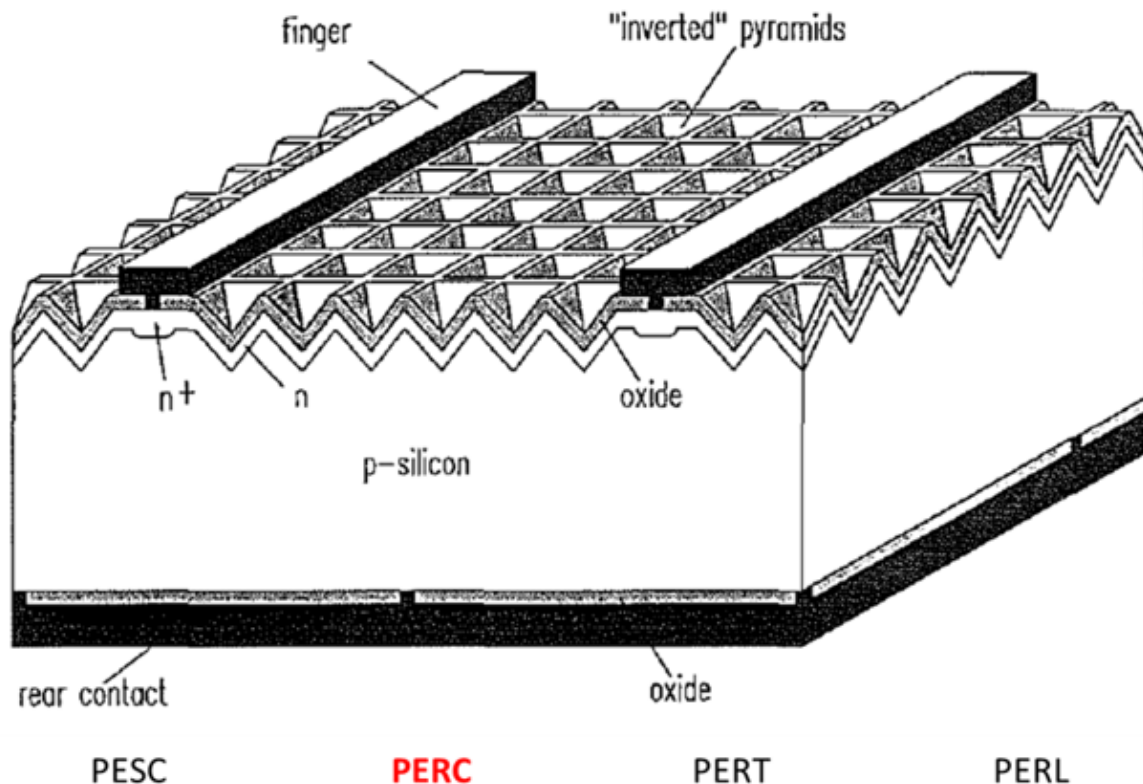
PERT

PERL

From Ph.D. Thesis of Aihua Wang, UNSW, 1992

72. The PERC (Passivated Emitter and Rear Cell) was the next historical improvement in solar cell technology. This cell used a high-quality thermal oxidation on the rear of the cell to passivate most of its surface far more effectively than a simple Al-alloyed BSF was able to achieve. However, small holes had to be formed in this passivating oxide layer in order to make low-resistance contact to the metal beneath.

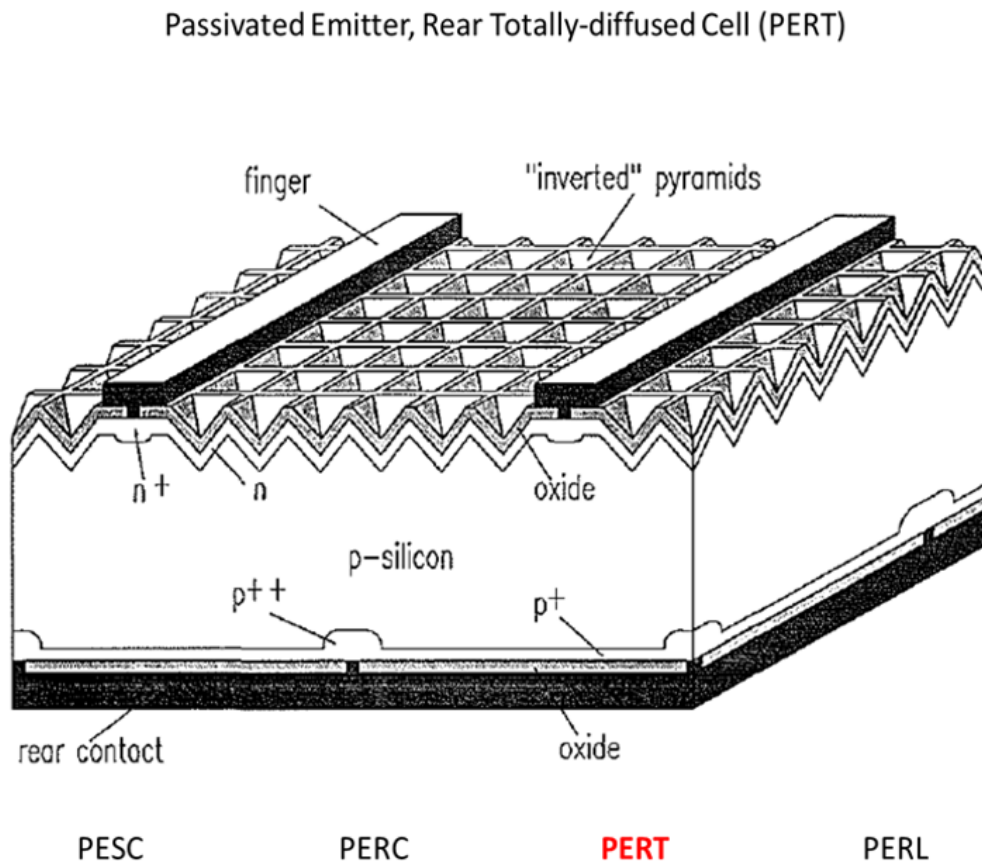
The Passivated Emitter and Rear Cell (PERC)



From Ph.D. Thesis of Aihua Wang, UNSW, 1992

73. Eventually, cell producers were able to get even better results by using an additional doping diffusion on the back surface specifically to get better BSF passivation there. The PERT (Passivated Emitter and Rear Total area diffused) included a dopant-diffused region over the entire rear surface to get better passivation than using a back-surface oxide alone. It also included an extra-heavy diffusion over the regions near the metal contacts for lower contact resistance and improved contact passivation. These cells still required the penetration of the

passivating oxide layer in order to open conducting paths to the rear metal contacts.



From Ph.D. Thesis of Aihua Wang, UNSW, 1992

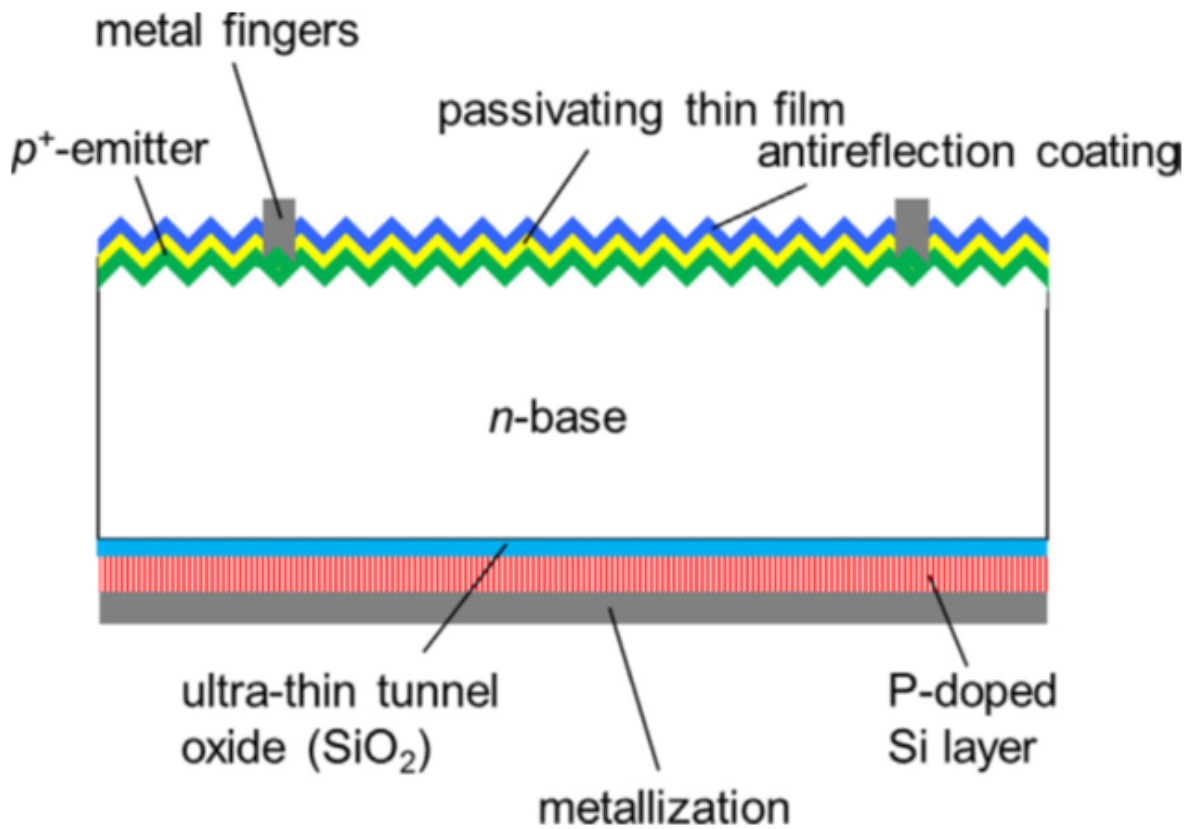
74. This is where the technology stood for many years until the invention of the TOPCon cell (Tunnel Oxide Passivated rear Contact).

2. TOPCon Solar Cells

75. The term TOPCon was coined by researchers at the Fraunhofer Institute for Solar Energy Systems (Fraunhofer ISE) in 2013. *See, e.g.*, Ex. 2010 (Feldmann, et al., “A Passivated Rear Contact for High-Efficiency n-Type Silicon

Solar Cells Enabling High VocS and FF > 82%” (28th European PV Solar Energy Conference & Exhibition, Paris, Sept. 30 – Oct. 4, 2013)).

76. Ex. 2010 includes the Figure below:



TOPCon cell (Tunnel Oxide Passivated Rear Contact).

77. In this cell design, the back heavily diffused c-Si region of the PERT cell has been replaced by two layers: an ultra-thin tunnel oxide and a deposited phosphorus-doped N-type poly-Si layer.

a. Tunnel Oxides

78. Tunnel oxides are high-quality SiO_2 layers that are extremely thin, about 1.5nm, just about three atomic monolayers that cover the entire back side surface of the substrate. They are so thin that due to alignment of Si-SiO₂ bandgaps, majority carriers in the Si (the same polarity as the n-type substrate -- electrons in this case) can pass through them with very low resistance, while minority carriers (holes) are nearly all blocked. This significantly reduces the number of minority carriers in the poly-Si and at the metal contacts and suppresses recombination there. The high quality of the tunnel oxide layer (no dangling bonds or impurities) keeps recombination at the c-Si-SiO₂ interface low.

79. Tunneling can take place when the wave function of the electrons penetrates the oxide layer according to quantum theory. This can only occur to a substantial degree when the oxide layer is less than 2 nm.

80. Quantum tunneling enables majority carrier movement across the interface and almost completely blocks minority carriers. Due to its thinness, electrons can “tunnel” through the oxide layer rather than being blocked like the holes are.

81. The tunneling mechanism is described in U.S. Patent Pub. No. 2002/0142500 to Foglietti. Ex. 1042. Although Foglietti relates to bipolar transistors, the tunneling mechanism it describes also applies to solar cells.

82. According to Foglietti, interfacial oxides (tunnel oxides) are “generally less restrictive with respect to majority carriers (electrons) moving from the emitter region of the transistor into the base region than minority carriers (holes) moving from the base region into the emitter region. This phenomenon is due to the tunneling probability of electrons being greater than the tunneling probability of holes.” Ex. 1042, ¶3.

83. According to Foligetti, the majority carrier “can tunnel through the interfacial oxide, Ex. 1042, ¶4, whereas holes are blocked from passing the interfacial oxide, *id.* at ¶5. Thus, Foglietti concludes, “under appropriate circumstances,” interfacial oxides (tunnel oxides) “may be modeled as a selective diode . . . wherein the electrons [] see a forward biased, conductive path, and the holes [] see a reverse-biased, non-conductive path.” *Id.* at ¶5. This tunneling mechanism improves transistor gain in Foglietti’s system. *Id.* at ¶¶4-5.

84. Notably, Foglietti specifies this improvement (provided by tunneling) “is substantially dependent upon various properties of the interfacial oxide.” Ex. 1042, ¶6. For one, the interfacial oxide (tunnel oxide) cannot be “too thick,” otherwise “the number of electrons which can tunnel through from the emitter into the base is reduced substantially.” *Id.* On the other hand, the interfacial oxide (tunnel oxide) cannot be “too thin,” otherwise “an insufficient barrier exists to block the hole current.” *Id.*

85. Moreover, the interfacial oxide (tunnel oxide) must also maintain integrity:

For example, since the interfacial oxide is subject to various types of subsequent thermal processing (e.g., subsequent poly CVD processing, metal deposition, anneal steps, etc.), the interfacial oxide may lose its integrity, that is, the oxide may exhibit non-uniform characteristics spatially across which in some cases may negatively impact the transistor performance. For example, if the interfacial oxide is fractured or becomes discontinuous, resulting in oxide islands, such fractures will be random and not repeatable from device to device; consequently, such fracturing causes unreliable transistor gain performance.

Ex. 1042, ¶7.

b. The Polycrystalline Silicon Layer

86. In a TOPCon structure, a layer of polysilicon heavily doped with N-type dopants is formed on the tunnel oxide. Polycrystalline silicon consists of many small, randomly oriented Si crystals. However, the band gap remains roughly the same as that of c-Si. The combination of a tunnel oxide and a doped polycrystalline silicon layer provides excellent passivation and carrier selectivity on the N-type substrate.

VII. THE '053 PATENT

87. The '053 patent discloses and claims a novel front contact solar cell with formed emitter. Ex. 1001, Title.

88. The '053 patent describes, with reference to Figure 1, a cross-section of a solar cell in accordance with an embodiment of the present invention. Ex. 1001, 2:6-7.

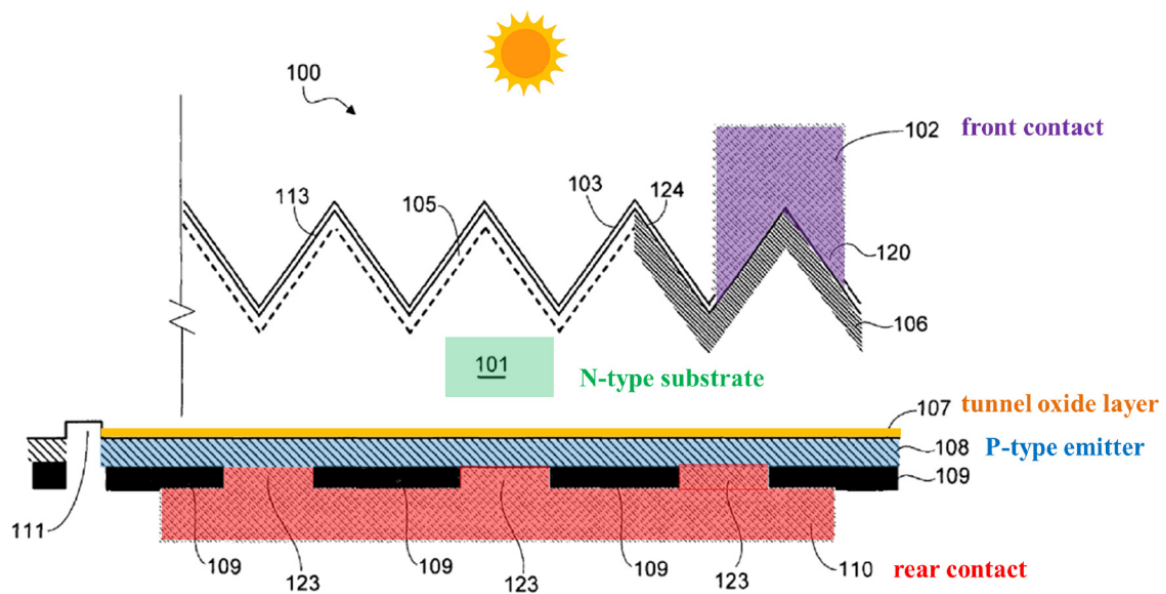


FIG. 1

Paper 3, 14 (citing Ex. 1001, Fig. 1) (annotations in Petition).

89. In this exemplary embodiment, an N-type silicon substrate 101 is formed from a silicon wafer, is etched to remove damaged surfaces. Ex. 1001, 3:59-64. The front side of the substrate is located at the top of Figure 1 and faces the sun, the back side of the substrate is on the bottom of Figure 1 and faces away

from the sun. *Id.* at 2:33-34. A tunnel oxide 107, which can be silicon dioxide, is provided on the back surface of the substrate 101. *Id.* at 4:4-8.

90. A layer of polysilicon 108 is deposited on the tunnel oxide layer 107 to form the polysilicon emitter 108 (formed on the back side). Ex. 1001, 4:9-11. A dopant source layer 461 (not shown in Figure 1) is formed on the polysilicon emitter 108 (i.e., formed on the back side of the polysilicon emitter) and the dopant is later driven into the polysilicon with a drive-in step. *Id.* at 4:14-27. A capping layer 462 (not shown in Figure 1) is formed over this dopant layer to keep the dopants from escaping during the dopant drive in process. *Id.* at 4:18-21. An edge isolation trench 111 is formed near the edge of the substrate 101 and is cut through the capping layer all the way through to contact a small area of the substrate 101. *Id.* at 4:28-35.

91. Exposed surfaces of the substrate 101 (on the front side) are etched to form pyramid 113 like structures. Ex. 1001, 4:36-41. This etching step removes the previously applied layers 401 and 402, as can be seen in Figs. 4D and 4E. An N-type dopant source 412 is formed on the textured surface of the substrate. *Id.* at 4:42-46. The N-type dopants from dopant layer 412 are then driven-in to the substrate 101 forming N-type doping regions 105 and 106. This drive-in step also drives in the dopants from the doping source layer 461, into the back side of the

polysilicon (polysilicon emitter 108). This forms a heterojunction, referred to in claims 9 and 16 as a “backside junction.” *Id.* at 2:43-45, 4:60-5:1.

92. The drive in step may be formed in-situ, which the patent explains is “a single manual (i.e., by fabrication personnel) loading of the substrate 101 in a furnace or other single chamber of multi-chamber processing tool.” *Id.* at 5:9-16. After this drive in step, layers 461 and 462 become silicon dioxide layer 109 and the front side of the silicon becomes N-doped region 106. *Id.* at 4:66-67, 2:43-45. A thin thermal silicon dioxide layer 124 is provided as a passivation layer on the surface of the silicon substrate 101. *Id.* at 5:6-8.

93. An antireflective (also serving as a dielectric) coating of silicon nitride layer 103 is formed over the textured surface 113 after removal of the N-type dopant source layer 412. Ex. 1001, 5:28-34. A front contact mask is then provided on the silicon nitride layer 103 to create a pattern for forming contact holes 102. *Id.* at 5:36-40. A back contact mask 422 is used on the silicon dioxide layer 109 to create a pattern for the back side contact holes 123. The holes 102 and 123 are then etched away. *Id.* at 5:46-46-55.

94. A back side metal contact 110 is formed on the silicon dioxide layer 109 to fill the contact holes 123 and make electrical connection to the polysilicon emitter 108. Ex. 1001, 5:56-63. Finally, a front side metal contact 120 is formed on

the silicon nitride layer 103 to fill contact holes 120 and make electrical connection to the substrate 101. *Id.* at 5:64-66.

95. While Figure 1 illustrates a solar cell with an N-type substrate and a P-type polysilicon emitter forming a backside junction, the patent claims are broader than that and can encompass an N-type substrate and an N-type polysilicon emitter forming a backside junction. This is shown in the below comparison of the independent claims 1, 9, and 16.

Claim 1	Claim 9	Claim 16
1. A method of fabricating a solar cell having a front side facing the sun to collect solar radiation during normal operation and a backside opposite the front side, the method comprising:	9. A method of fabricating a solar cell comprising	16. A method of fabricating a solar cell comprising:
		forming an oxide layer over a back surface of a silicon substrate;
forming a layer of polysilicon over a back surface of an N-type silicon substrate on the back side of the solar cell;	forming a layer of polysilicon over a back surface of a silicon substrate;	forming a layer of polysilicon over the oxide layer;
forming a P-type dopant source over the layer of polysilicon;	forming a first dopant source layer over the layer of polysilicon;	
forming a capping layer over the P-type dopant source;		

Claim 1	Claim 9	Claim 16
diffusing P-type dopants from the P-type dopant source to the layer of polysilicon to form a backside junction with the N-type silicon substrate;	diffusing dopants from the first dopant source layer to the layer of polysilicon to form a backside junction with the silicon substrate;	diffusing dopants into the layer of polysilicon to form a backside junction with the silicon substrate;
diffusing N-type dopants into a front surface of the N-type silicon substrate; and	diffusing dopants into a front surface of the silicon substrate, the front surface of the silicon substrate facing the sun during normal operation; and	diffusing dopants into a front surface of the silicon substrate, the front surface of the silicon substrate facing the sun during normal operation; and
forming a metal contact on the front side of the solar cell, wherein the metal contact is electrically coupled to the N-type silicon substrate.	forming a metal contact on the front surface of the silicon substrate, wherein the metal contact is electrically coupled to the silicon substrate.	forming metal contacts on the front surface of the silicon substrate, wherein the metal contact is electrically coupled to the silicon substrate.

Ex. 1001, claims 1 (6:13-29), 9 (6:52-65), and 16 (7:19-8:6) (emphasis added).

96. As is shown above, claim 1 is directed toward specific N-type and P-type dopant sources in the silicon and polysilicon layers, respectively. Claims 9 and 16, on the other hand, are silent with respect to the types of dopant sources used to dope the silicon and polysilicon layers. Therefore, at least with respect to the dopant sources, claims 9 and 16 are broader in scope than claim 1. Therefore, I

understand that claims 9 and 16 are not limited to N-type silicon and P-type polysilicon layers.

VIII. PERSON OF ORDINARY SKILL IN THE ART

97. Petitioner asserts the following qualifications for a POSITA:

A POSITA at the priority date of the '053 patent (February 20, 2008) would have had (i) an advanced degree in electrical engineering, mechanical engineering, applied physics, chemistry, materials science, or a related discipline and (ii) at least one year of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. Alternatively, a POSITA would have had (i) a bachelor's degree in the aforementioned disciplines and (ii) at least two years of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. Less work experience may be compensated by a higher level of education, and vice versa.

Paper 3, 16.

98. For this declaration, Patent Owner's counsel asked me to apply Petitioner's qualifications for a POSITA.

IX. CLAIM CONSTRUCTION

99. Patent Owner's counsel provided me with legal principles that are relevant to claim construction. *See* §V above. I considered those legal principles in forming my opinions in this section.

100. Patent Owner’s counsel asked me to consider claim construction as of the date of the invention. *See* §IV.A, above. My opinions are the same regardless of which date is used.

101. For this declaration, Patent Owner’s counsel asked me to adopt Petitioner’s proposal to apply the plain and ordinary meaning of the claims. Paper 3, 17.

X. THE CITED REFERENCES

A. Froitzheim (Ex. 1004)

102. European Patent Publication EP1732142 (“Froitzheim”), published in 2006, is titled “Si solar cell and its manufacturing method.” Ex. 1004, Cover.

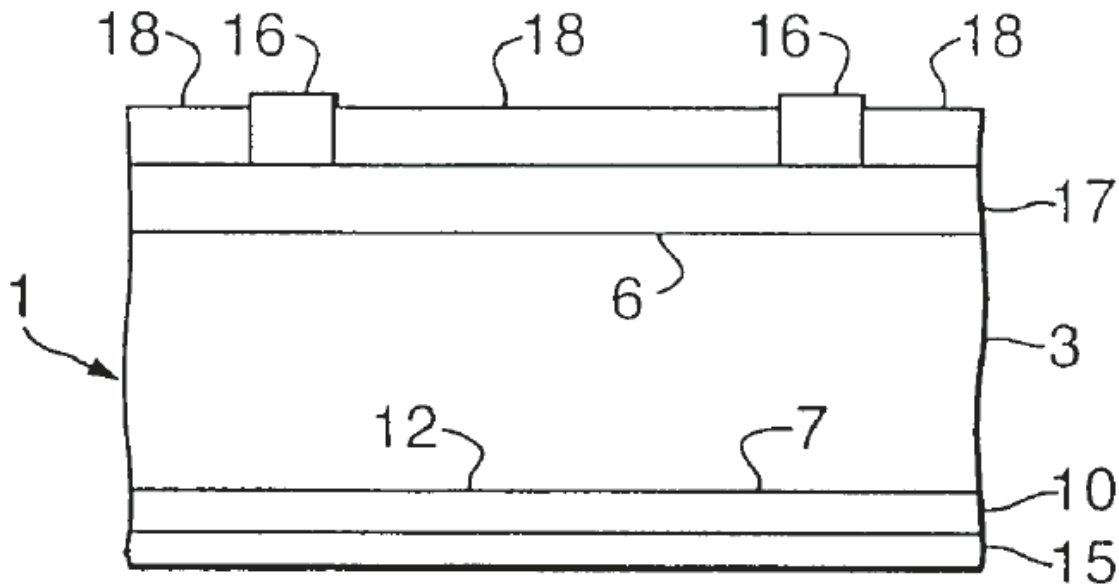
103. Froitzheim’s Abstract states:

A solar cell comprising a silicon body layer of n-type bulk doping having a front side and a rear side; a non-alloyed p-type doped region at the rear side of the body layer and forming a p/n-junction therewith; a rear side contact in electrical connection with the p-type doped region; and a front side contact in electrical connection with the n-type silicon body layer, and a method of manufacturing such a solar cell.

Ex. 1004, Abstract.

104. Below is a first embodiment of Froitzheim’s cell:

Fig. 1.



Ex. 1004, Fig. 1.

105. Froitzheim describes Figure 1 as follows:

[0024] Reference is made to Figure 1 showing schematically a cross-section through a first embodiment of a solar cell 1 according to the invention. The solar cell 1 comprises a silicon body layer 3 of n-type bulk doping having a front side 6 and a rear side 7. The silicon body layer 3 is made from crystalline silicon, and can be of the mono-, multi- or polycrystalline type. Preferably, Czochralski grown Silicon is used. The thickness of the body layer can be typically between 10 and 400 μm , suitably between 100 and 300 μm , preferably between 150-250 μm . A suitable dopant is for example phosphorous. The

doping level is generally in the range of 10^{13} - 10^{18} atoms per cm^3 , typically in the order of 10^{15} - 10^{16} . Suitably, the doping is such that a resistivity higher than 0.5 and lower than 150 Ohm.cm is obtained, preferably higher than 1 and lower than 20, more preferably lower than 10 Ohm.cm.

[0025] At the rear side 7, a p-doped layer 10 is arranged suitably such as discussed further below, and a p/n-junction 12 with the body layer is formed.

...

[0027] A rear side contact 15 is arranged in electrical connection with the p-doped layer 10. The rear side contact is shown covering a large part or substantially all of the rear side of the cell.

[0028] At the front side 6, screen-printed front side contacts 16 are provided in electrical connection with the n-type silicon body layer. The front side contacts form part of a finger structure 19 such as sketched in top view in Figure 2 covering typically around 10% of the front surface when screen printed contacts are used. The electrical connection is provided via a shallow n⁺ doped layer 17 on the front side 6, i.e. between the front contact and the n-type silicon body layer.

...

[0030] The front surface is further provided with a passivation layer 18. The passivation layer can for example be an oxide such as SiO_2 a nitride such as SiN, undoped amorphous silicon, or mildly n⁺ doped amorphous silicon layer, which can be arranged using methods known in the art. It is a further advantage of the present invention that n or n⁺ doped layers can generally easier and better be passivated than p or p⁺

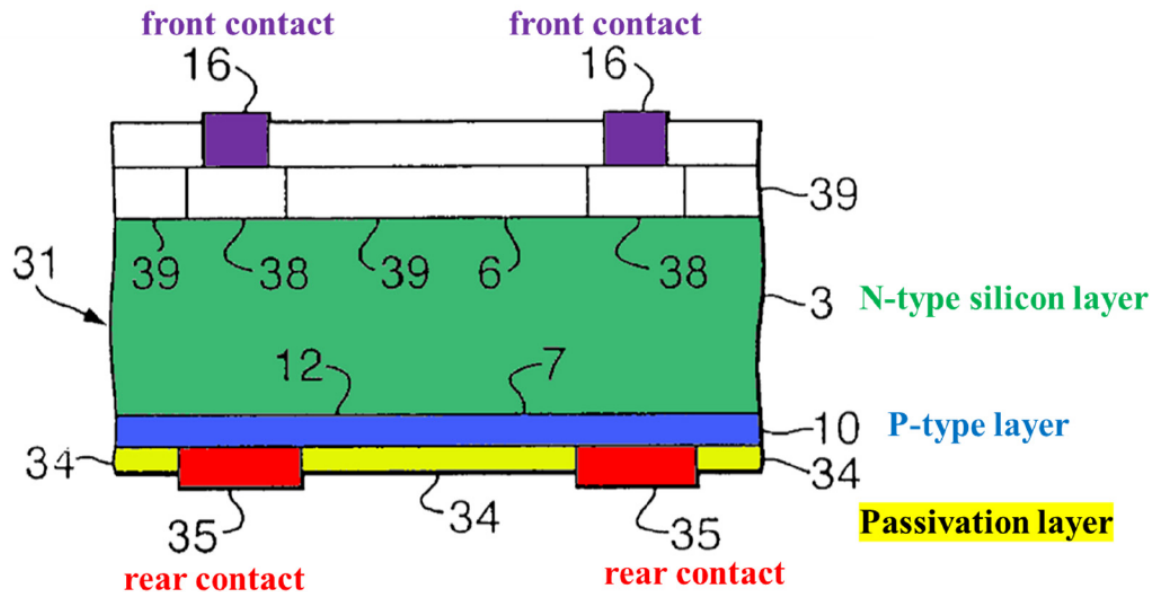
doped layers. An advantage of using SiN as passivation layer is that it has intrinsic charges.

[0031] Suitably further, an anti-reflection coating is provided as known in the art.

[0032] During normal operation of the solar cell 1 the front side 6 faces the sun and light is received through the area of the front surface that is not covered by the front contact 16. Light is absorbed predominantly in the n-doped body layer 3, and excess hole-electron pairs are created. The holes form minority charge carriers in the n-type material and travel towards the rear side over the p/n-junction 12 where they become majority carriers in the p-layer that are withdrawn at the rear side contact thereby providing photocurrent. The photogenerated excess electrons are prevented from diffusing to the front contacts by the field exerted by the n+/n junction leading between the body layer 3 and the p+ layer 18.

Ex. 1004, ¶¶24-32.

106. Froitzheim discloses a second embodiment , which Petitioner references:



Paper 3, 18 (citing Ex. 1004, Fig. 3) (annotations in Petition).

107. Froitzheim describes Figure 3 as follows:

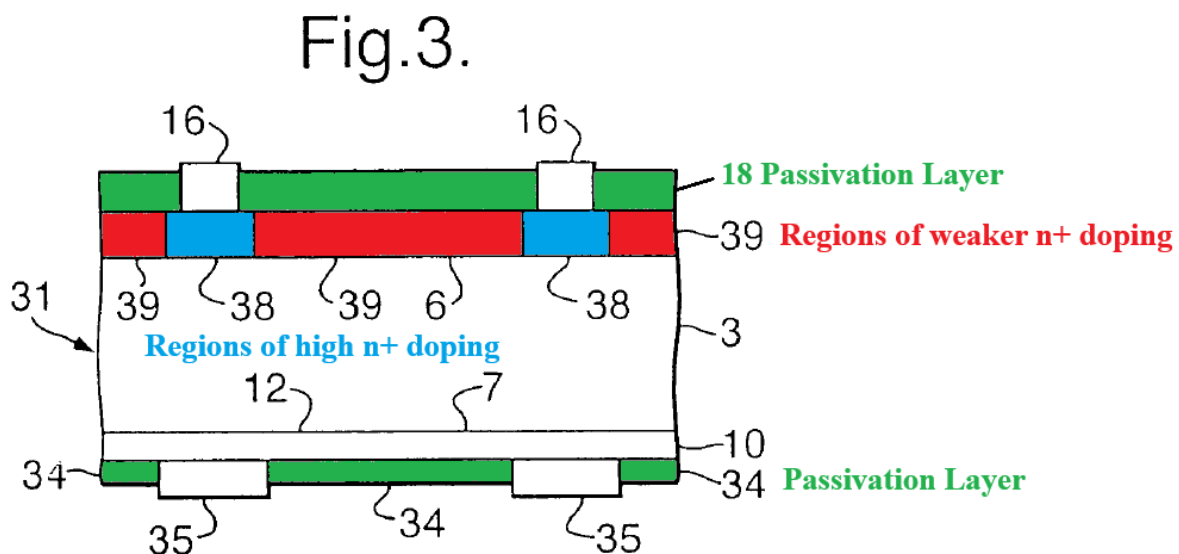
[0033] Reference is made to Figure 3 showing a second embodiment of a solar cell 31 according to the invention. Cell 31 differs from cell 1 of Figure 1 in that the rear contacts 35 are arranged in a finger structure covering only part of the rear side, e.g. similar to that of Figure 2. A typical coverage is in the range of 10-40% of the rear surface. Between the fingers a passivation layer 34 is arranged, for which the same type of layers can be used as for the front side. If the cell is suitably arranged for operation such that reflected or diffracted light is received at the rear side not facing the sun, additional photocurrent can be created by photons absorbed predominantly in the body layer 3 from the rear side.

[0034] A further difference with the cell of Figure 1 is the structured front surface field. Regions 38 of high n+ doping are arranged

surrounding the front contacts 16, and regions 39 of weaker n+ doping in between front contact fingers, wherein the weaker n+ doping can be achieved by a doping concentration intermediate between that of the n-type body layer and that of the n+ doped regions 18, and/or in that regions 39 are shallower than regions 38

Ex. 1004, ¶¶33-34.

108. Based on the description above, additional labels to Figure 3 of Froitzheim are shown below:



Ex. 1004, Fig. 3 (annotated); *see also* Ex. 1004, Fig. 1 (illustrating layer 18).

B. Gan (Ex. 1005)

109. First, it should be understood that there are two Gan publications relevant to the Petition. The first publication is Gan et al., “*Polysilicon Emitters for Silicon Concentrator Solar cells*,” Proceedings of the 21st IEEE-PVSC (1990) (“Gan”).

Ex. 1005, 245. Gan is cited in the Petition and used in combination with Froitzheim, Paper 3, 24, and separately with Li, *id.* at 73.

110. The second publication is Gan, “*Polysilicon emitters for silicon concentrator solar cells*,” a dissertation submitted to the Department of Material Science and Engineering and the Committee on Graduate Studies of Stanford University in 1990 (“Gan Thesis”). Ex. 2003, Cover. The Gan Thesis was published and publicly available on the shelves in the Stanford Library on April 10, 1991, which is prior to the priority date of the ’053 patent. *See* Ex. 2026, ¶23. I understand that it can be assumed that a POSITA would have had knowledge of the Gan Thesis before that priority date. As explained below, the Gan Thesis is important for several reasons, including telling the complete story of why the technology disclosed in Gan was experimental, could not be reliably reproduced, and was not suitable for use in commercial concentrator cells.

111. In both Gan (Ex. 1005) and the Gan Thesis (Ex. 2003), the common author, Gan, is describing experiments trying to thread a needle to produce the optimum temperature to break up an interfacial oxide a little, but not too much. This interfacial oxide layer is formed between a crystalline silicon substrate and a polysilicon layer applied over the rear surface of the substrate. Gan tried different anneal temperatures and durations, and determines that above 900°C, the oxide breakup becomes too much. *See, e.g.*, Ex. 1005, 248 (“Considering the significant

increase of J_o caused by increasing the drive-in temperature from 900 to 1000°C. . .”); *see also id.* at (Table 1). Gan is not describing building an actual one sun solar cell, rather, Gan is describing experiments on poly-Si emitters that might be useful in a concentrator solar cell.

112. Gan discloses manufacturing steps to create test devices that include “[p]olysilicon emitters with a thermally grown interfacial oxide.” Ex. 1005, Abstract. Gan uses these test devices to measure the emitter saturation current density (J_o) and contact resistivity (ρ_c) of its polysilicon emitter when annealed under various conditions. *Id.* Specifically, Gan discloses a test device using FZ wafers to measure J_o , and a test device using CZ wafers to measure ρ_c . *Id.* at 245.

113. Petitioner proposes a Froitzheim-Gan combination that includes “fabrication steps to incorporate Gan’s polysilicon emitter and oxide layer.” Paper 3, 27.

114. Gan discloses manufacturing steps to create test devices that include “[p]olysilicon emitters with a thermally grown interfacial oxide.” Ex. 1005, Abstract. Gan uses these test devices to measure the emitter saturation current density (J_o) and contact resistivity (ρ_c) of its polysilicon emitter when annealed under various conditions. *Id.* Specifically, Gan discloses a test device using FZ wafers to measure J_o , and a test device using CZ wafers to measure ρ_c . *Id.* at 245.

115. Gan discloses the following steps to create its test devices.

1. Field oxidation (2000 Å)*.
2. Polysilicon-substrate contact opening*.
3. Thin thermal oxide growth at 800 °C*. (10-minute oxygen flow)[.]
4. Polysilicon deposition (6000 Å) and first-step anneal (1050 °C)*.
5. First-step anneal*.
6. Polysilicon finger definition.
7. Undoped glass deposition (2000 Å).
8. Metal-polysilicon and metal-substrate contact opening.
9. Doped glass deposition on both sides of the wafer*.
10. Drive-in; 900-1000 °C*.
11. Doped glass stripping and Al-1% Si alloy deposition.
12. Metal finger definition.

Ex. 1005, 246 (emphasis added). According to Gan, “the J_o and ρ_c were measured independently for each type of polysilicon emitter (or contact). J_o was measured with photoconductivity decay method. . .” and “the steps marked with “*” are the steps for J_o -measurement samples.” *Id.*

116. I understand that Petitioner’s expert testified that the proposed Froitzheim-Gan combination would use steps 3, 4, 9, and 10 from Gan’s 12 step fabrication process.

Q Below this paragraph we just looked at there are 12 steps in Gan.

Do you see that?

A I do.

Q Can you tell me which of these steps would be used in the Froitzheim-Gan combination?

A Yes. As I described previously, it's not required for a POSITA to make a one-to-one copying of steps for particular instances but, rather, to take the teachings of a whole to implement them. But as an example, Step 3, Thin thermal oxide growth, that's referring to the formation of Gan's tunnel oxide. That tunnel oxide is used in my combination of Froitzheim and Gan. That's important. The fourth step, polysilicon deposition, it's also important to -- or is required in my Froitzheim-Gan combination.

And then some subsequent steps, such as Step 9 and Step 10, are about doping that polysilicon layer to turn it into an emitter. And as I say in my declaration, my combination is Gan's oxide and polysilicon emitter. And so those steps teach how to dope the polysilicon to make an emitter.

As we discussed previously, Froitzheim also teaches steps about how to make a P-type diffusion.

Ex. 2029, 167:16-168:21.

117. Step 4 (the anneal performed at 1050°C) causes breakup of the oxide layer. This step and step 10, the drive-in step, were the subject of Gan's measurements to try to achieve acceptably low J_o values. Ex. 1005, 246. The anneal of step 4 is used to break up the thin oxide layer, and the second anneal of step 10 is used in Gan to drive in the dopants. In Gan's Table 1 below, the reference to "the second-step anneal" relates to Step 10. Ex. 1005, 248.

Table 1: The effect of the second-step anneal on J_o and ρ_c .

	N-type		P-type	
	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$
900 °C-4 hour	2.4	18	3.5	18
1000 °C-30 min	4.5	~ 6	8.2	3.8
1000 °C-60 min	7.9		10.5	

Ex. 1005, 248, Table 1.

118. Gan teaches that it is optimal to have low values for both J_o [emitter saturation current density] and ρ_c [contact resistivity], and this is achieved when “when both carriers are mostly blocked by the interfacial oxide.” Ex. 1005, 245, 249. In that regard, Table 1 of Gan shows that as you increase the temperature and time in the second step appeal, the value of J_o increases, which means more recombination and lower cell efficiency and is not a desired result.

119. Gan (Ex. 1005) and the Gan Thesis (Ex. 2003) both describe experiments that focused on trying to find the optimum temperature to be used in creating an interfacial oxide between a crystalline silicon substrate and a polysilicon layer and, more specifically, on how to break up the interfacial oxide a little, but not too much. Gan tried different anneal temperatures and durations and determined that above 900°C, the oxide breakup becomes too much. Ex. 1005, 248 (“Considering the significant increase of J_o caused by increasing the drive-in temperature from 900 to 1000°C, it is beneficial to use the two-step anneal to optimize J_o .”); *id.* at (Table 1).

120. As discussed in the Petition, Gan teaches “polysilicon emitters with a thermally grown interfacial oxide” for solar cells. Paper 3, 18 (citing Ex. 1005, 245-26). Gan also taught that “a very thin oxide (interfacial oxide)” “[a]lways exists” between the polysilicon emitter and the substrate.” Ex. 1005, 245. More importantly, the Gan Thesis teaches that “solar cells that were modeled or made in this study all suffered high contact resistance” and that “in the real solar cell runs, the situation grew even worse.” *See, e.g.*, Ex. 2003, 129 (110 in original); *see also id.* at 135-136 (116-117 in original). Thus, the Gan Thesis refutes Petitioner’s narrative that Gan successfully formed an interfacial oxide layer between a silicon substrate and a polysilicon layer. Paper 3, 30 (citing Ex. 1005, 249); Ex. 1003, ¶¶ 130, 190.

121. Substantively, Gan is specific about the effect of a high temperature anneal on the interfacial oxide layer between the silicon substrate and the polysilicon layer:

In either case, the oxide is not thermally stable; *i.e.*, it tends to break up during high temperature anneals. The breakup of the interfacial oxide has direct impact on both majority and minority carrier transport in the polysilicon emitter. This can be seen from the dependence on the specific contact resistivity (ρ_c) [6] and the emitter saturation current density (J_0) [1,2,3,4,5,6,7] upon either the anneal condition or the oxide integrity.

Ex. 1005, 245.

122. Gan specifically says that when the anneal temperature is high and the oxide layer loses its integrity, the ρ_c is low and the J_o is high:

With the effect of the interfacial oxide is negligible, such as when the interfacial oxide loses its integrity in high temperature anneals, the ρ_c is low ($\sim 2 \times 10^{-7} \text{ -cm}^2$) [6] and the J_o is high ($\sim 1 \times 10^{-12}$) [1,3].

Conversely, when both the carriers are mostly blocked by the interfacial oxide, like for an intact chemical oxide ($\sim 15 \text{ \AA}$), the ρ_c is high and the J_o is low.

Ex. 1005, 245.

123. Gan teaches that it is optimal to have low values for both J_o (emitter saturation current density] and ρ_c (contact resistivity], and this is achieved when “when both carriers are mostly blocked by the interfacial oxide.” Ex. 1005, 245, 249. What Gan is trying to determine are values for “ ρ_c and J_o when only a small fraction of the interfacial oxide is broken.” *Id.* According to Gan “there always exists a very thin oxide (interfacial oxide), which can be the by-product of the cleaning process or is grown intentionally . . . In either case, the oxide is not thermally stable, i.e., it tends to break up during the high temperature anneals.” *Id.* at 245 (emphasis added). Gan explains that “[t]he first-step anneal, which serves to break up the oxide, was performed at higher temperature than that for the second-step anneal which aims for the dopant drive-in.” *Id.*

124. Gan ran multiple experiments for combinations of temperatures for the first anneal (oxide break up) and the second anneal (dopant drive in) and reported the results in Figure 6, which is a plot of ρ_c v. J_o , with a key in the top right that shows “the type of polysilicon emitter, the first-step anneal (temperature/minute), and the second-step anneal (temperature/minute).” Ex. 1005, 249, Fig. 6. The goal was to achieve low J_o .

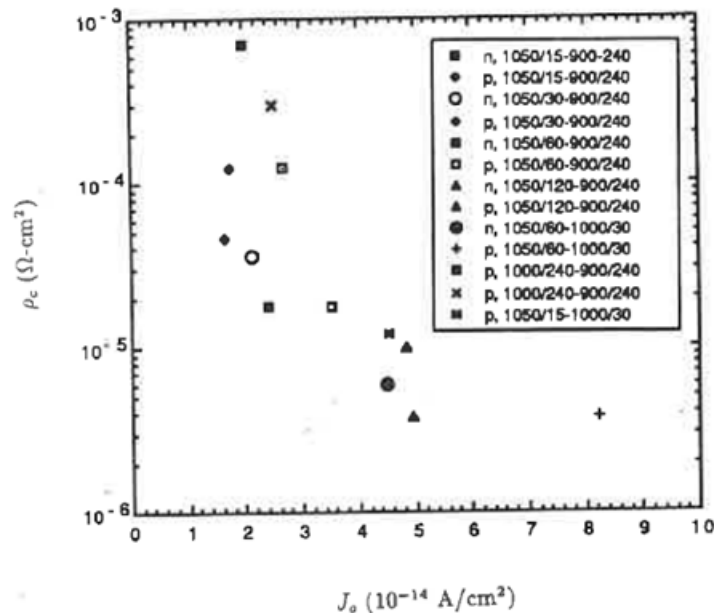


Figure 6: ρ_c - J_o of this work.

Ex. 1005, Fig. 6.

125. This graph shows that the higher the temperature of the second step anneal (the anneal to drive the dopants into the polysilicon), the higher the J_o . In fact, this figure shows much lower J_o values for the 900 °C second anneal (“regime 1”) than for the 1000°C second anneal (“regime 2”). Gan then discusses this figure

and observes for regimes 1 (900°C) “ J_o is almost constant while ρ_c drops drastically” and for regime 2 (1000°C) “ ρ_c decreases very slowly and J_o increases in much faster pace.” Ex. 1005, 249.

126. Gan also explains that the second step anneal is optimal when performed at “900 °C for 4 hours.” Ex. 1005, 247. Gan further says “[considering the significant increase of J_o caused by increasing the drive-in temperature from 900 to 1000 °C, it is beneficial to use the two-step anneal to optimize J_o .” *Id.*

127. Gan provided further analysis of the experimental results in Table 1, below. These results show that the higher the temperature of the second-step anneal and the longer its duration the worse the device works.

Table 1: The effect of the second-step anneal on J_o and ρ_c .

	N-type		P-type	
	$J_{o,e}$ ($\times 10^{-14}$ A/cm ²)	ρ_c ($\mu\Omega\text{-cm}^2$)	$J_{o,e}$ ($\times 10^{-14}$ A/cm ²)	ρ_c ($\mu\Omega\text{-cm}^2$)
900 °C-4 hour	2.4	18	3.5	18
1000 °C-30 min	4.5	~ 6	8.2	3.8
1000 °C-60 min	7.9		10.5	

Ex. 1005, Table 1

128. Gan shows that as the temperature increases above 900°C, ρ_c decreases but J_o increases rather than decreases, such that annealing at a temperature of >900°C results in a rapid decrease in the efficacy of the system.

C. Gan Thesis (Ex. 2003)

129. Jon-Yiew Gan’s thesis titled “*Polysilicon emitters for silicon concentrator solar cells*,” published by the Stanford University in July 1990, provides a more comprehensive review of the experiments and methodologies described in Gan (Ex. 1004), *see, e.g.*, Ex. 2003, Chapter 5, and provides significantly more details about the theory, experimental results, and conclusions set forth in Gan (Ex. 1004).

130. I understand that the Gan Thesis was published and publicly available in the Stanford Library on April 10, 1991, which is prior to the priority date of the ’053 patent (as discussed in § IV.A). *See* Ex. 2026, ¶23. I further understand that it can be assumed that a POSITA would have had knowledge of the information in the Gan Thesis before that priority date. It is my understanding that a librarian expert confirmed public availability. *Id.*

131. The Gan Thesis acknowledges inconsistent oxide growth during “ramp-up” and “stand-by” periods, and explains that “it is possible that the thin-oxide growth can be improved by performing the oxidation at lower temperatures such that the oxide rate can be controlled more precisely.” Ex. 2003, 112 (emphasis added).

132. At best, the Gan Thesis suggested that “[t]heoretically, it is possible to make a polysilicon SIS emitter with an intact inter-facial oxide having low J_o and

“acceptable” ρ_c simultaneously.” Ex. 2003, 53 (emphasis added). Gan Thesis also stated “[t]heoretically, a model was proposed to make the polysilicon emitter with both low J_o ($\sim 3 \times 10^{-14} \text{ A/cm}^2$) and low contact resistance ($\rho_c \leq 1 \times 10^{-5} \Omega\text{-cm}^2$).” *Id.* at Abstract (emphasis added). Also, “[t]he polysilicon emitter with low J_o and ρ_c can be made with a very small fraction of interfacial oxide breakup.” *Id.* at 107 (emphasis added). And “[w]ith a few percentages of the interfacial oxide being broken, the ρ_c will be negligible for the application in concentrator solar cells. Under such a condition, there is a regime in which the J_o will not be affected by the oxide breakup because it is dominated by the recombination at the oxide interface. Thus it is possible for polysilicon SIS emitter to have both low J_o and ρ_c .” *Id.* at 69 (emphasis added).

133. Stepping back, however, a POSITA would recognize these musings in the Gan Thesis were theories that fell far short of being reproducible. In context, the lack of consistent success in experimental results derived from testing these theories fell far short of supporting a reasonable expectation of success. This is particularly true because the Gan Thesis reproduced experimental data showing poor results when implementing the theories.

134. For example, the Gan Thesis discloses the following:

It appears that the oxide breakup depends **critically** on the interfacial oxide thickness. The thin-oxide growth recipe used in this work was

not reliable; the oxide thickness between 15 and 20 Å have been found with the same growth condition. As a result, this contributes to the fluctuation of the ρ_c results. It is then clear that a more reliable way of growing the thin oxide is needed.

Ex. 2003, 119 (emphasis added).

Although a thermally grown interfacial oxide seems **essential** for a polysilicon emitter to have both low J_o and ρ_c , the breakup process is still difficult to control. On several occasions, we have encountered reproducibility problems. For example, we find that the ρ_c is quite different between two separate experiments with identical processing conditions. Even worse, solar cells that were made in this study all suffered high contact resistance. The problem is primarily due to insufficient oxide breakup, and is caused by the fluctuation of the thickness of the interfacial oxide.

Ex. 2003, 107 (emphasis added).

As shown in the figure, the cell is in fact plagued by two things: the high surface recombination velocity ($S = 58$ cm/sec), and high emitter resistance ($\rho_{cm} + \rho_{cp} = 1 \times 10^{-3} \Omega\text{-cm}^2$). . . From the low emitter recombination and high emitter resistance, it is clear that the interfacial oxide did not break as expected.”

Ex. 2003, 110 (emphasis added); *see also id.* (“Later in the real solar cell runs, the situation grew even worse. . . Although the $(J_{on} + J_{op})$ measured from those cells are between 8×10^{-14} and 4×10^{-14} A/cm², the cell efficiency is greatly degraded by such a high emitter resistance.”); *id.* at 111 (“Although these results can be

attributed to many other reasons, the following experiment shows that the effect of the oxide thickness cannot be ignored. This, combined with the non-reliable oxide-growth recipe gives rise to the mishap of our solar-cell runs.”) (emphasis added); *id.* at 114 (“It becomes clear that the wide fluctuation of our results is mainly due to the poor control over the oxide thickness.”); *id.* at 114-17 (“[W]e found that a consistent result of ρ_c is difficult to reproduce for the polysilicon emitter with a thermally grown interfacial oxide. This is mainly attributed to the fact that our thin-oxide recipe is not reliable.”) (emphasis added); *id.* at 56 (“With a window so narrow, it is not possible to have good control over the characteristics of a polysilicon SIS emitter.”).

135. Simply, the Gan Thesis established that the processes found in Gan would not achieve good results consistently or reliably, especially at the temperatures used by Froitzheim. Consequently, a POSITA would not have had a reasonable expectation of success, and therefore would not have been motivated to combine Froitzheim and Gan.

D. Smith (Ex. 1007)

136. U.S. Patent No. 6,998,288 to Smith et al. (“Smith”) is titled “Use of Doped Silicon Dioxide in the Fabrication of Solar Cells.” Ex. 1007, Cover.

137. Smith’s Abstract states:

In one embodiment, a method of forming doped regions in a substrate of a back side contact solar cell includes the steps of depositing a first doped oxide layer on a back side of a substrate, depositing a first undoped oxide layer over the first doped oxide layer, diffusing a first dopant from the first doped oxide layer into the substrate to form a first doped region in the substrate, and diffusing a second dopant into the substrate by way of a front side of the substrate, wherein the diffusion of the first dopant and the second dopant into the substrate are performed in-situ. The method may further include the steps of patterning the first doped and undoped oxide layers to expose portions of the back side of the substrate and depositing a second doped and undoped oxide layers on the back side of the substrate.

Ex. 1007, Abstract.

138. In its “Description of the Background Art,” Smith describes the “back side contact solar cell” as follows:

Solar cells are well known devices for converting solar radiation to electrical energy. They may be fabricated on a semiconductor wafer using semiconductor processing technology. Generally speaking, a solar cell may be fabricated by forming p-doped and n-doped regions in a silicon substrate. Solar radiation impinging on the solar cell creates electrons and holes that migrate to the p-doped and n-doped regions, thereby creating voltage differentials between the doped regions. In a back side contact solar cell, the doped regions are coupled to metal contacts on the back side of the solar cell to allow an external electrical circuit to be coupled to and be powered by the solar

cell. Back side contact solar cells are also disclosed in U.S. Pat. Nos. 5,053,083 and 4,927,770, which are both incorporated herein by reference in their entirety.

Ex. 1007, 1:21-35 (emphasis added).

139. Smith discloses “a method of fabricating a solar cell in accordance with an embodiment of [its] invention.” Ex. 1007, 2:29-31.

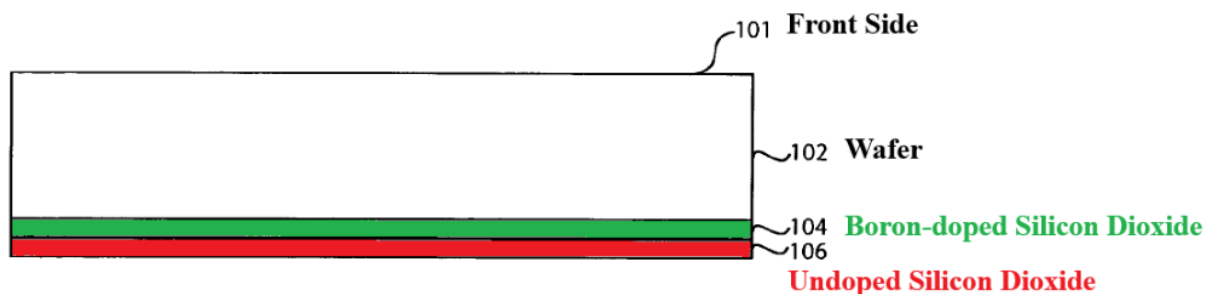
140. Specifically, Smith discloses processing “an N-type FZ silicon wafer 102,” which “services as the substrate of the solar cell being fabricated. Wafer 102 has a front side 101 and a back side 103.” Ex. 1007, 2:32-37.

141. Referencing Figure 2, Smith discloses:

In FIG. 2, a boron-doped silicon dioxide (SiO_2) (“BSG”) **104** is deposited on the back side of wafer **102**. In one embodiment, boron-doped silicon dioxide **104** is deposited to a thickness of about 1000 Angstroms using an atmospheric pressure chemical vapor deposition process (APCVD). The thickness of boron-doped silicon dioxide **104**, and other materials disclosed herein, may be varied depending on the application. For example, boron-doped silicon dioxide **104** may also be deposited to a thickness of about 500 Angstroms by APCVD. Thereafter, an undoped silicon dioxide **106** is deposited over boron-doped silicon dioxide **104**. In one embodiment, undoped silicon dioxide **106** is deposited to a thickness of about 1200 Angstroms also by APCVD. The use of a deposition process, such as APCVD, to deposit the boron-doped silicon dioxide and the undoped silicon dioxide advantageously allows for one-sided deposition. This is

particularly useful in the manufacture of back side contact solar cells where only one side of the solar cell is textured. Note that depending on the application, doped silicon dioxide **104** may also be doped with P-type dopants other than boron.

Ex. 1007, 46-64.



Ex. 1007, Fig. 2 (annotated).

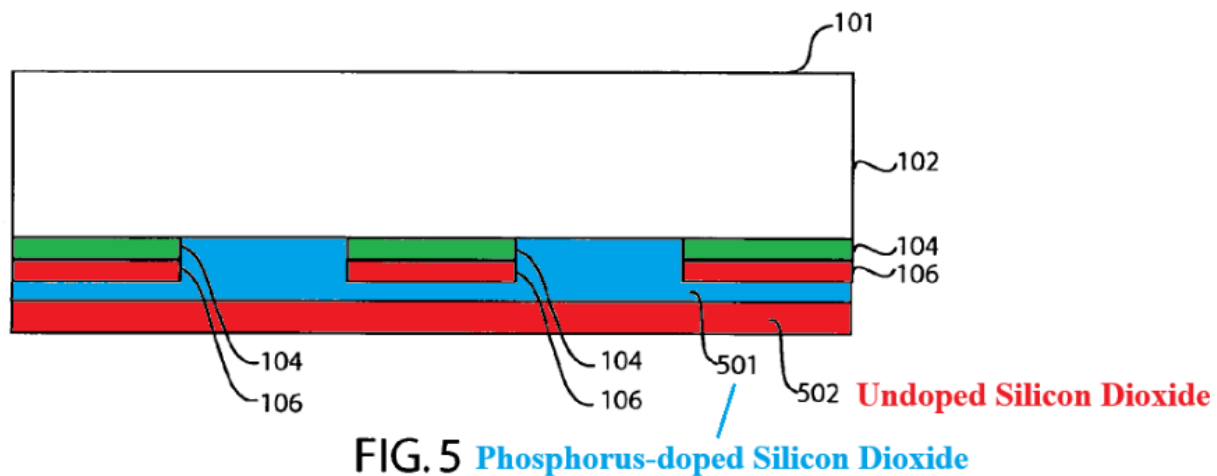
142. Smith discloses forming a mask 108 “over the silicon dioxide stack comprising the boron-doped and undoped silicon dioxide. Mask **108** will be used in a subsequent etch process (see FIG. 4) exposing the would be N+region of the wafer.” Ex. 1007, 2:65-3:1. According to Smith, “mask 108 is employed in patterning the silicon dioxide stack comprising boron-doped silicon dioxide 104 and undoped silicon dioxide 106.” *Id.* at 3:11-13.

143. Referencing Figure 5, Smith discloses:

In FIG. 5, a phosphorus-doped silicon dioxide **501** is deposited over the sample of FIG. 4. Thereafter, an undoped silicon dioxide **502** is deposited over phosphorus-doped silicon dioxide **501**. In one embodiment, phosphorus-doped silicon dioxide **501** is deposited to a

thickness of about 500 Angstroms by APCVD, while undoped silicon dioxide **502** is deposited to a thickness of about 2400 Angstroms also by APCVD. Note that depending on the application, doped silicon dioxide **501** may also be deposited with N-type dopants other than phosphorus. Phosphorus-doped silicon dioxide **501** and undoped silicon dioxide **502** are preferably conformal to their respective underlying layers.

Ex. 1007, 3:19-30.



Ex. 1007, Fig. 5 (annotated).

144. Referencing Figure 7, Smith discloses:

In FIG. 7, the sample of FIG. 6 is subjected to in-situ steps. The steps are in-situ in that they are performed in one loading of wafer **102** into the wafer processing tool. In one embodiment, the in-situ steps are performed in a furnace. In the first in-situ step, wafer **102** is heated to about 1000° C. for one hour to diffuse dopants from boron-doped silicon dioxide **104** and phosphorus-doped silicon dioxide **501** into

wafer **102**. This results in the formation of P+ regions **702** (due to boron-doped silicon dioxide **104**) and N+ regions **703** (due to phosphorus-doped silicon dioxide **501**) in wafer **102**. Note that during the first in-situ step, undoped silicon dioxide **106** beneficially prevents phosphorus from phosphorus-doped silicon dioxide **501** from diffusing into boron-doped silicon dioxide **104**. Also, undoped silicon dioxide **502** beneficially prevents phosphorus from phosphorus-doped silicon dioxide **501** from diffusing into the furnace.

In the second in-situ step, the furnace conditions are changed to about 750° C. with an atmosphere containing phosphorus oxychloride, then to about 975° C. with an atmosphere containing oxygen to diffuse phosphorus as an N-type dopant into wafer **102** from its front side, and to grow a thin layer of silicon dioxide on both sides of wafer **102**. Front side **101** is now labeled as “**101B**” to indicate that there is a thin layer of silicon dioxide on its surface. The thin layer of silicon dioxide advantageously leads to better passivation of the front side and back side surfaces of wafer **102**. In FIG. 7, the front side diffusion of N-type dopants into wafer **102** is schematically represented by arrows **701**. As can be appreciated the use of in-situ steps to drive dopants into wafer **102** simplifies the fabrication process.

Ex. 1007, 3:39-4:2.

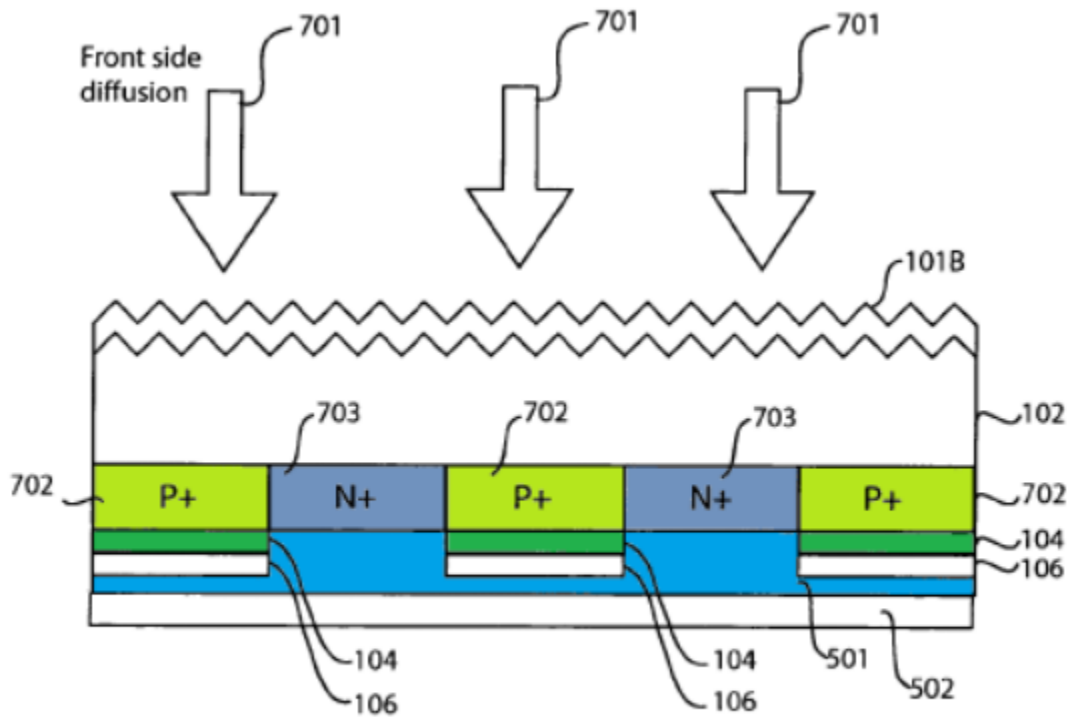


FIG. 7

Ex. 1007, Fig. 7 (annotated).

145. Smith discloses completing “the sample of FIG. 7” “using a back-end process to form electrodes coupled to the P+ and N+ regions of wafer **102** and to include an anti-reflective coating (e.g., silicon nitride) on front side **101B**.” Ex. 1007, 4:3-6.

E. Li (Ex. 1008)

146. Chinese Patent Application Publication No. CN1949545 (“Li”), published in 2007, is titled “Crystalline Silicon Solar Cell with Novel Structure.” Ex. 1008, Cover.

147. Li's Abstract states:

A crystalline silicon solar cell adopting an emitting region on a back surface of thin film silicon belongs to a photovoltaic cell with a novel structure. The crystalline silicon solar cell is characterized in that a layer of silicon thin film is deposited on a back surface of an N-type monocrystalline silicon substrate to form a heterogeneous PN junction so as to replace a homogeneous PN junction prepared on a front surface of the cell by a conventional diffusion method. The silicon thin film deposited in the present invention can be an amorphous thin film, a microcrystalline thin film, or a nanocrystalline thin film. The heterogeneous PN junction in the present invention can be a P-type silicon thin film directly deposited on the N-type monocrystalline silicon, or can also be a P-type silicon thin film deposited on a layer of intrinsic silicon thin film which is first deposited on the N-type monocrystalline silicon. By adopting the cell structure in the present invention, cell efficiency can reach 20% or above.

Ex. 1008, Abstract.

148. In its "Background Art" section, Li describes conventional crystalline silicon solar cells as having a homogenous PN junction and being disadvantaged by high-temperature diffusion:

Crystalline silicon solar cells account for more than 90% of photovoltaic market shares in the global world. Such cells generally adopt P-type crystalline silicon to form an N-type emitting region through high-temperature diffusion and belong to homogeneous PN

junction solar cells. However, such cells have the disadvantages that the high-temperature diffusion may cause more defects in silicon materials, and when pollution is caused in a high-temperature process, cell efficiency will be greatly reduced. Thus, higher requirements are put forward for both materials and a production environment. In addition, back surfaces of such cells are free of effective passivation and an effective light trapping structure. Thus, recombination on the back surfaces is relatively serious, and a part of light penetrates an active region of the cells and is not absorbed. These disadvantages are reasons that limit improvement of the efficiency of conventional solar cells.

Ex. 1008, 3.

149. As its name implies, a homogeneous PN junction is a junction formed by the same type of material with the same crystal structure on both sides of the junction. Thus, for example, according to Li's description, Froitzheim would have a homogeneous PN junction because its emitter layer is "a non-alloyed p-type doped region at the rear side of the body layer [substrate] and forming a p/n-junction therewith." Ex. 1004, Abstract.

150. Because the emitter layer is formed on the substrate, high anneal temperature (typically above 850° C) is used in homogeneous PN junctions to drive in/diffuse dopants. The dopants are diffused into the substrate to form the doped region. *See, e.g.*, Ex. 1004, ¶¶40-42 (disclosing high anneal temperature to

diffuse boron into “the rear surface of the body layer” to form a “p-type doped region”).

151. Li also describes “amorphous silicon/crystalline silicon heterojunction solar cell (HIT cell)” and its advantages:

In recent years, an amorphous silicon/crystalline silicon heterojunction solar cell (HIT cell) has been developed by Sanyo in Japan. Such cell adopts an N-type monocrystalline silicon wafer and deposits an amorphous silicon thin film on a surface of the silicon wafer. An emitting region is a P-type amorphous silicon thin film deposited on a front surface of the silicon wafer. A front surface structure of the cell is a metal grid/transparent conductive thin film (TCO)/P-type amorphous silicon/intrinsic amorphous silicon/monocrystalline silicon wafer. The structure makes full use of a good surface passivation effect of the amorphous silicon, and the efficiency of the prepared cell reaches 20% or above.

Adoption of N-type silicon has the advantages that the N-type silicon wafer generally has a long minority carrier lifetime, and the silicon wafer with high quality is easy to obtain. The N-type silicon is also more tolerant to impurities than the P-type silicon. For solar cells, P-type silicon cells will have efficiency attenuation to a certain degree after long-term exposure to light, and the attenuation is related to boron-oxygen defects in materials. After the N-type silicon is used, the problem no longer exists.

Adoption of the amorphous silicon emitting region has the advantage that the amorphous silicon has a good surface passivation

effect. Moreover, a deposition temperature is low (200°C), and a process is relatively simple, such that a high-temperature process is avoided, and the manufacturing cost of the cell is reduced.

Ex. 1008, 3.

152. As its name implies, a heterogenous PN junction is a junction formed by two different materials on the two sides of the junction. In Li's case, both sides are silicon, but they have different crystal structures:

A layer of silicon thin film is deposited on a back surface of N-type monocrystalline silicon to form an emitting region (a P-type silicon thin film can be deposited on a layer of intrinsic silicon thin film which is first deposited on the back surface of the N-type monocrystalline silicon, or a P-type silicon thin film can be directly deposited on the N-type monocrystalline silicon).

Ex. 1008, 4; *see also id.* at Abstract.

153. Because the emitter layer is already of P-type, high anneal temperature (used to drive in/diffuse dopants) is not used in construction of Li's heterogeneous PN junction structure. Thus, Li teaches that its heterogeneous PN junction "is prepared by a low-temperature deposition method, which avoids a conventional diffusion process at 800-1000°C." Ex. 1008, 4.

154. Li describes the purported benefits of its purported invention:

A layer of silicon thin film is deposited on a back surface of N-type monocrystalline silicon to form an emitting region (a P-type silicon

thin film can be deposited on a layer of intrinsic silicon thin film which is first deposited on the back surface of the N-type monocrystalline silicon, or a P-type silicon thin film can be directly deposited on the N-type monocrystalline silicon). The silicon thin film can be prepared by any deposition method, and the silicon thin film can be an amorphous silicon thin film, a microcrystalline silicon thin film, or a nanocrystalline silicon thin film. Compared with conventional homojunction P-type crystalline silicon solar cells, the use of the structure not only effectively avoids influence of boron-oxygen defects in P-type cells, but also effectively passivates the back surface. In addition, a metal electrode layer on the back surface can re-reflect light that penetrates the cell back into the cell, thereby increasing an absorption rate of the light by the cell. Compared with foreign amorphous silicon/crystalline silicon heterojunction solar cells (HIT cells), the emitting region of the structure is on the back surface of the cell, and a front surface no longer requires a transparent conductive thin film to collect current, such that efficiency loss caused by absorption of incident solar energy by a silicon thin film and the transparent conductive thin film on the front surface can be avoided. By adopting the cell structure in the present invention, cell efficiency can reach 20% or above.

Ex. 1008, 4.

155. I note that only a-Si passivates the junction because of its higher bandgap, poly-Si does not.

156. Further, a metal layer does not provide good reflection unless the metal is offset from the Si by an oxide or other dielectric layer. In any case, all cells have metal on the backside, so this is no different.

XI. THE PETITION DOES NOT SHOW THAT ANY CHALLENGED CLAIM IS UNPATENTABLE

A. Ground I: Claims 9-12, 14, and 16-20 Are Patentable Under Froitzheim and Gan

157. In my opinion, a POSITA would not have combined Froitzheim and Gan.

1. The Gan Thesis Failed to Reliably Implement Gan's Interfacial Oxide Layer

158. In my opinion, a POSITA would not have had a reasonable expectation of success in modifying the structure of Froitzheim to include the oxide and polysilicon emitter of Gan.

159. Gan proposes forming a tunnel oxide layer and then breaking it ever so slightly to achieve acceptable values for J_o and ρ_c . However, the Gan Thesis explains that this requires a degree of precision in forming and breaking the oxide layer that Gan never consistently achieved and documents the consistent failure to do so.

160. The Gan Thesis documents consistent failures to achieve Gan's theoretical results. In its "Conclusion" chapter, the Gan Thesis states:

In this chapter, we found that a consistent result of ρ_c is difficult to reproduce for the polysilicon emitter with a thermally grown interfacial oxide. This is mainly attributed to the fact that our thin-oxide growth recipe is not reliable. With the same oxidation schedule, a wide variation of oxide thicknesses have been found for different times. Experimentally, the interfacial oxide breakup was also found to be dependent on the oxide thickness critically. Such an oxide-thickness dependence of the breakup process can be explained by a “silicon cluster nucleation” process. In order to have predictable results, it appears that a precise control of the oxide thickness is necessary.

Ex. 2003, 116-17 (emphasis added).

161. Gan Thesis was trying to get a low J_o of 1×10^{-14} A/cm² to 2×10^{-14} A/cm². For example, in its Abstract, the Gan Thesis states:

Recently, a single-crystal silicon point-contact solar cell has been shown to have energy conversion efficiency of 28% at 100 suns. Such a cell has been fully analyzed; and it appears that the cell efficiency can be increased more than one absolute percentage by eliminating the emitter recombination. In order to do this, the emitter saturation current density (J_o), which characterizes the dopant-diffused region recombination, of both n- and p- type emitters has to be kept around 2×10^{-14} A /cm². Unfortunately, such low J_o cannot be obtained by the diffused emitters formed in the single-crystal silicon. Polysilicon emitters, n-type in particular, have been reported to have very low J_o ($\sim 1 \times 10^{-14}$ A/cm²); therefore, they can be a very useful substitute for

the diffused emitters for high efficiency solar cells. Nevertheless, some problems in the polysilicon emitter itself have to be resolved before they can be used in silicon concentrator solar cells. One is the high contact resistance. For the polysilicon emitter to have low J_o , a thin interfacial oxide has to be placed in between the polysilicon and the substrate. However, such an interfacial oxide also causes high contact resistance ($\rho_c \geq 1 \times 10^{-4} \Omega\text{-cm}^2$). Another is the high J_o of the p-type polysilicon emitter. Prior to this work, the lowest J_o of the p-type polysilicon emitter reported was $\sim 3 \times 10^{-13} \text{ A/cm}^2$ which is high for a solar cell application. The other is the complexity of the oxide breakup during a high temperature anneal, which appears to increase the J_o of the polysilicon emitter. In this work, both the minority and the majority carrier transport of the polysilicon emitter are closely examined. Theoretically, a model was proposed to make the polysilicon emitter with both low J_o ($\sim 3 \times 10^{-14} \text{ A/cm}^2$) and low contact resistance ($\rho_c \leq 1 \times 10^{-5} \Omega\text{-cm}^2$). Experimentally, such polysilicon emitters for both types were successfully demonstrated.

Ex. 2003, Abstract (emphasis added).

162. The Gan Thesis further states:

The cell efficiency, as shown in the figure, is hardly affected by the emitter recombination when J_o is below $1 \times 10^{-14} \text{ A/cm}^2$; however, it falls off rapidly as the J_o increases over $1 \times 10^{-14} \text{ A/cm}^2$. If we allow the emitters to cover the entire backside surface, then the total J_o is $4.5 \times 10^{-13} \text{ A/cm}^2$, and the cell efficiency will be limited to about 27% at the incident power density of 10 watts/cm². In contrast, the

efficiency of the point contact cell is increased to 28% by scaling the emitter areal-coverage fraction to 20% such that the total J_o of the cell is effectively reduced to about 1×10^{-13} A/cm².

Ex. 2003, 3 (emphasis added).

163. The Gan Thesis also states:

As we reduce the J_o down to 1×10^{-14} A /cm², and enlarge the emitter contact area, the cell performance is improved globally. This is shown in Figure 2.5 where the cell efficiency of three IBC cells are plotted against the incident power density. In the figure, cell (a) has 5 μ m line contact and J_o of 4.5×10^{-13} A /cm², cell (b) has the same contact size as cell (a) but J_o is 1×10^{-14} A/cm², and cell (c) has the same J_o as cell (b) but with wider contact lines—15 μ m. The curve for the cell (b) is less clear, it is first merged with that for cell (c) at low incident power density and change to that for cell (a) at high incident power density. By comparing cell (a) with (b), the better performance of cell (b) results from the lower J_o which is consistent with the results shown in Figure 1.3. However, the advantage of low J_o diminishes as the incident power density increases over 50 watts/cm².

The comparison between cell (b) and (c) is even more interesting. First, the cell efficiency of both cells stays the same at low incident power density, which indicates that the emitter recombination will be negligible as the J_o is below 1×10^{-14} A/cm². Secondly, note that the cell (c) starts to outperform the cell (b) at 10 watts/cm². This implies that the low internal series resistance is important even at the incident power density as low as 10 watts/cm², and becomes more

obvious in the regime of high incident power density where the better current-collection capability of the large-contact cell lessens the power loss through the Auger recombination.

It now becomes obvious to see what an emitter should be for the concentrator solar cells. Low J_o is of course the primary requirement. As shown in Figure 1.2, the total emitter saturation current density below 1×10^{-14} A/cm² shows negligible effect. Take this value and assume the emitter areal coverage fraction is 30% for each type, this means that the J_o of each type of emitters should be around 2×10^{-14} A/cm².

Ex. 2003, 22 (emphasis added).

164. This is understandable because Gan (Ex. 1005) and the Gan Thesis are both trying to solve the same problem, namely a very small and consistent breakup of the interfacial oxide to achieve low J_o .

165. In fact, the Gan Thesis showed that there was no known method for getting the oxide thickness sufficiently reliable to obtain acceptable results based on the following disclosures:

It appears that the oxide breakup depends critically on the interfacial oxide thickness. The thin-oxide growth recipe used in this work was not reliable; the oxide thickness between 15 and 20 Å have been found with the same growth condition. As a result, this contributes to the fluctuation of the ρ_c results. It is then clear that a more reliable way of growing the thin oxide is needed.

Ex. 2003, 119 (emphasis added).

Although a thermally grown interfacial oxide seems **essential** for a polysilicon emitter to have both low J_o and ρ_c , the breakup process is still difficult to control. On several occasions, we have encountered reproducibility problems. For example, we find that the ρ_c is quite different between two separate experiments with identical processing conditions. Even worse, solar cells that were made in this study all suffered high contact resistance. The problem is primarily due to insufficient oxide breakup, and is caused by the fluctuation of the thickness of the interfacial oxide.

Ex. 2003, 107 (emphasis added).

Later, in the real solar cell runs, the situation got even worse. The solar cells made in the experiment are the 15- μ m-contact-line IBC which have been shown and simulated in Chapter 2. We found that, with the OCVD measurement, the total specific contact resistivity ($p_n + p_p$) was higher than $1 \times 10^{-3} \Omega\text{-cm}^2$. Although the $(J_{on} + J_{op})$ measured from those cells are between 8×10^{-14} and 4×10^{-14} A/cm², the cell efficiency is greatly degraded by such a high emitter resistance.

Ex. 2003, 110 (emphasis added).

As shown in the figure, the cell is in fact plagued by two things: the high surface recombination velocity ($S = 58$ cm/sec), and high emitter resistance ($\rho_{cm} + \rho_{cp} = 1 \times 10^{-3} \Omega\text{-cm}^2$). The effect of high emitter resistance is shown by the difference of the cell efficiency between the curve (b) and the curve (c), while the difference between the curve (a) and the curve (c) shows the projected effect of the high

surface recombination velocity. Without the high surface recombination velocity and the emitter resistance, the cell performance would be the curve formed by the maximum efficiency between the curve (a) and the curve (b) which is the ultimate performance we can have for the cell with polysilicon emitters.

From the low emitter recombination and high emitter resistance, it is clear that the interfacial oxide did not break as expected.”

Ex. 2003, 110 (emphasis added); *see also id.* at 111 (“Although these results can be attributed to many other reasons, the following experiment shows that the effect of the oxide thickness cannot be ignored. This, combined with the non-reliable oxide-growth recipe gives rise to the mishap of our solar-cell runs.”) (emphasis added); *id.* at 114 (“It becomes clear that the wide fluctuation of our results is mainly due to the poor control over the oxide thickness.”); *id.* at 114-17 (“[W]e found that a consistent result of ρ_c is difficult to reproduce for the polysilicon emitter with a thermally grown interfacial oxide. This is mainly attributed to the fact that our thin-oxide recipe is not reliable.”) (emphasis added); *id.* at 56 (“With a window so narrow, it is not possible to have good control over the characteristics of a polysilicon SIS emitter.”).

166. In my opinion, a POSITA would have considered Gan with the benefit of the Gan Thesis and determined that the experiments discussed in Gan produced

unreliable results, created “mishap[s],” and suffered from reproducibility problems.

Any results Gan teaches were purely theoretical.

167. The Gan Thesis documented its own failure to implement the polysilicon emitter and interfacial oxide structure in a real solar cell:

Later, in the real solar cell runs, the situation got even worse. The solar cells made in the experiment are the 15- μm -contact-line IBC which have been shown and simulated in Chapter 2. We found that, with the OCVD measurement, the total specific contact resistivity ($\rho_n + \rho_p$) was higher than $1 \times 10^{-3} \Omega\text{-cm}^2$. Although the ($J_{on} + J_{op}$) measured from those cells are between 8×10^{-14} and $4 \times 10^{-14} \text{ A/cm}^2$, the cell efficiency is greatly degraded by such a high emitter resistance. . .

As shown in the figure, the cell is in fact plagued by two things: the high surface recombination velocity ($S = 50 \text{ cm/sec}$), and high emitter resistance ($\rho_n + \rho_p = 1 \times 10^{-3} \Omega\text{-cm}^2$). . .

From the low emitter recombination and high emitter resistance, it is clear that the interfacial oxide did not break as we expected.

Ex. 2003, 110.

168. In my opinion, in the Gan Thesis, the author Gan attempted to implement the structure of Gan (Ex. 1005) in a real solar cell, but failed to do so reliably. Thus, a POSITA would not have been motivated to combine Gan’s test structure with Froitzheim’s solar cell.

2. *Polysilicon Emitters and Tunnel Oxide Layers Were Not Known Elements in Solar Cells*

169. Petitioner's assertion that fabricating Froitzheim's solar cell with Gan's polysilicon emitters and interfacial oxide "was simply substituting one known element for another to obtain predictable results," Paper 3, 32, is not supported by any references that show a POSITA how to add an interfacial oxide layer (tunnel oxide) to a solar cell.

170. First, Petitioner cites "Ex.1005-Gan, 246." As discussed in § X.B, Gan does not teach the fabrication of a solar cell, but rather, a test device that does not even have a PN junction.

171. Second, Petitioner cites "Ex.1006-Borden-575, [0026]-[0027]." Those two paragraphs disclose an optional tunnel oxide layer grown in Borden-575's contact holes, which do not exist in the Froitzheim-Gan combination. See Paper 3, generally; *see also* Ex. 2029, 246:4-10 (discussing an identical Froitzheim-Gan combination in Petitioner's IPR2024-01203). And importantly, Borden-575 admits solar cells with tunnel oxides "have not been commercially introduced, possibly because of the difficulty of reliably forming a thin tunnel oxide." Ex. 1006, ¶5.

172. Third, Petitioner cites "Ex.1004-Froitzheim, [0030]." Neither this paragraph nor the rest of Froitzheim mention interfacial or tunnel oxide. Instead,

Froitzheim's [0030] discloses a front surface passivation layer 18 that may be an oxide.

173. Fourth, Petitioner cites "Ex.1015-Swanson, 2:50-53." This portion of Swanson mentions adjusting the thickness of a back side tunnel oxide, but does not teach a POSITA how to add one to a solar cell. Swanson mentions forming a tunnel oxide layer on the back surface, but does not mention how.

B. Ground II: Claims 1-20 Are Patentable Under Froitzheim, Gan, and Smith

174. In my opinion, a POSITA also would not have been motivated to further combine the proposed Froitzheim-Gan combination with Smith because Smith caters to an entirely different solar cell structure.

1. A POSITA Would Not Have Had a Reasonable Expectation of Success in Combining Froitzheim and Gan

175. As discussed in § XI.A, a POSITA would not have been motivated to combine Froitzheim and Gan because the Gan Thesis teaches that Gan's interfacial oxide could not be reliably grown. The proposed additions of Smith's manufacturing steps, Paper 3, 51-52, do not remedy those problems, *id.* at 51 (in its motivation to combine Froitzheim, Gan, and Smith section, Petitioner incorporates section X.A.1 of the Petition (motivation to combine Froitzheim and Gan).

176. A POSITA would not have had a motivation to combine the oxide and polysilicon from Gan into Froitzhheim because, as discussed in § XI.A.1, the Gan

Thesis teaches that the oxide layer growth is unreliable and inconsistent negating the benefits for combining Gan with Froitzheim. For the same reasons, a POSITA would not have had a motivation to combine Froitzheim, Gan, and Smith because Smith does not teach either an oxide layer or a polysilicon layer. The purpose of the proposed Smith combination is to add dopants.

2. *A POSITA Would Not Have Used Smith's One-Sided APCVD Deposition Because Its Purported Benefits Does Not Apply to Froitzheim's Structure*

177. Smith discloses that its one-sided APCVD deposition “is particularly useful in the manufacture of back side contact solar cells where only one side of the solar cell is textured.” Ex. 1007, 60-62. The proposed Froitzheim-Gan-Smith structure, using Froitzheim's solar cell, is not a back side contact solar cell.

178. Smith describes its one-sided APCVD deposition as depositing both **boron-doped silicon dioxide 104** and **phosphorus-doped silicon dioxide 501** on the back side of the wafer. Ex. 1007, 2:45-49; *see also id.* at 3:19-20. Then, the wafer 102 is heated to diffuse the dopants from both silicon dioxides 104, 501 into the wafer 102, forming “**P+ regions 702** (due to boron-doped silicon dioxide 104) and **N+ regions 703** (due to phosphorus doped silicon dioxide 501).” *Id.* at 3:43-50.

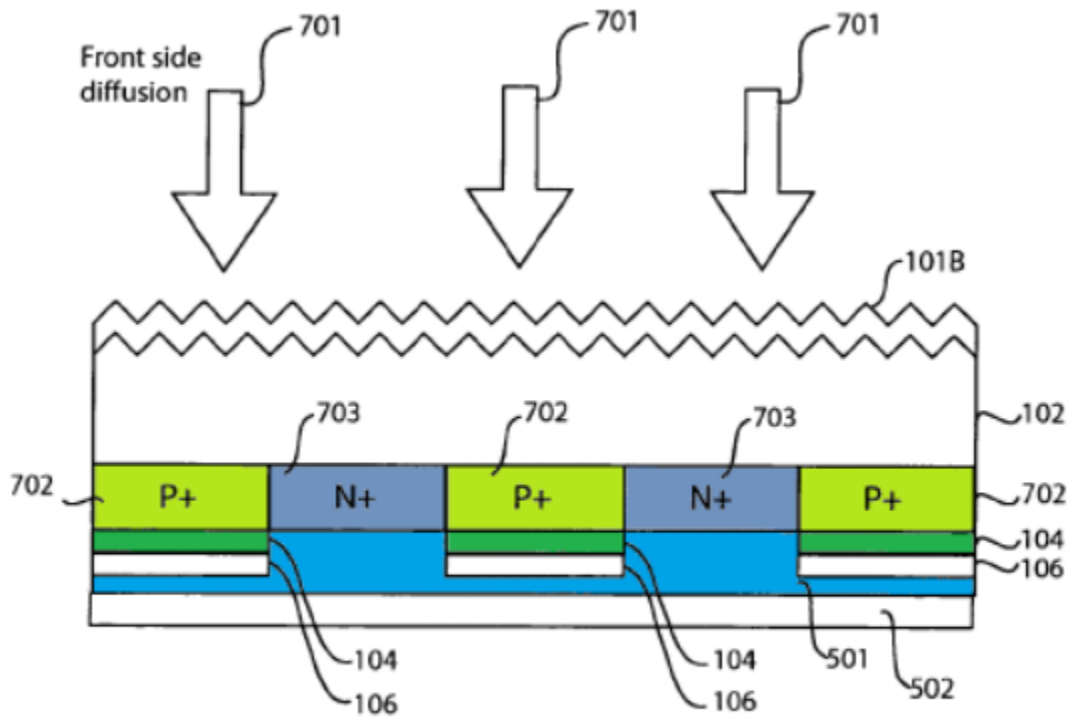


FIG. 7

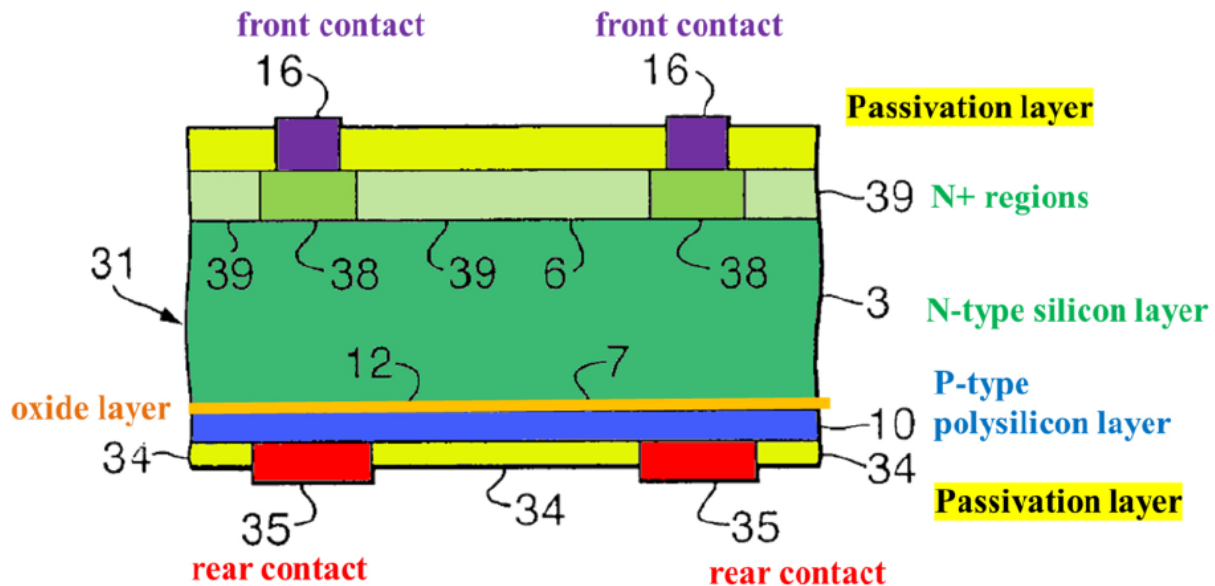
Ex. 1007, Fig. 7 (annotated).

179. One-sided APCVD deposition is compatible with Smith’s solar cell, which is a back side contact cell. According to Smith, “[i]n a back side contact solar cell, the doped regions are coupled to metal contacts on the back side of the solar cell to allow an external electrical circuit to be coupled to and be powered by the solar cell.” Ex. 1007, 1:29-33. In this back contact structure, electrodes (metal contacts) are formed and coupled to the P+ and N+ regions 702, 703. *Id.* at 4:3-5; *see also* Ex. 1003, ¶66 (equating “metal contacts” to “electrodes”). And because

both regions 702, 703 are on the back side, the metal contacts are also on the back side.

180. In contrast, Froitzheim's solar cell (and thus, the solar cell of the proposed Froitzheim-Gan-Smith combination) does not have both P+ and N+ regions on its back side, or both metal contacts on its backside. *See, e.g.*, Ex. 1004, Fig. 3; *see also id.* at ¶34 (discussing the front contact fingers of Figure 3). It is simply not a back contact solar cell and so APCVD deposition of a single-polarity backside doping layer provides no benefit.

181. Petitioner's own illustration of the proposed combination makes this clear:



Paper 3, 25 (citing Ex. 1004, Fig. 3; Ex. 1005, 245, 249) (annotations in Petition); *see also id.* at 51 (incorporating section X.A.1 of the Petition, which features the illustration above).

C. Ground III: Claims 9-20 Are Patentable Under Li, Gan, and Smith

1. A POSITA Would Not Have Had a Reasonable Expectation of Success in Combining Li and Gan

182. As discussed in § XI.A, a POSITA would not have been motivated to implement Gan’s polysilicon emitter and interfacial oxide structure in an actual solar cell because the Gan Thesis teaches that Gan’s interfacial oxide could not be reliably grown. Replacing Li with Froitzheim, or adding Smith’s manufacturing steps, do not remedy those problems.

2. Li Teaches Away from Gan and Smith

183. In my opinion, a POSITA would not have been motivated to (1) modify “Li’s method of making a backside junction solar cell to incorporate Gan’s methods of using a polysilicon emitter and oxide layer structure,” Paper 3, 73, or (2) “to obtain the manufacturing efficiencies Smith teaches,” *id.* at 75. Li’s disclosure conflicts with both.

184. Li’s purported invention is a solar cell with a heterogeneous PN junction:

A layer of silicon thin film is deposited on a back surface of N-type monocrystalline silicon to form an emitting region (a P-type silicon thin film can be deposited on a layer of intrinsic silicon thin film which is first deposited on the back surface of the N-type monocrystalline silicon, or a P-type silicon thin film can be directly deposited on the N-type monocrystalline silicon).

Ex. 1008, 4; *see also id.* at Abstract.

185. Li teaches that its heterogeneous PN junction “is prepared by a low-temperature deposition method, which avoids a conventional diffusion process at 800-1000°C.” Ex. 1008, 4.

186. Li describes the purported benefits of its purported invention:

A technical means adopted in the present invention is to achieve an emitting region by depositing the silicon thin film on the back surface of the cell. Compared with a P-type silicon wafer diffused N-type emitting region used in most factories at present, the N-type silicon can effectively reduce the generation of boron-oxygen defects under illumination and resulting attenuation of conversion efficiency. In addition, a PN junction is prepared by a low-temperature deposition method, which avoids a conventional diffusion process at 800-1000°C. Such high-temperature process will cause more defects or contamination in a silicon material, which will affect the improvement of cell efficiency. In addition, the silicon thin film deposited on the back surface of the silicon wafer, whether it is amorphous silicon, microcrystalline silicon, or nanocrystalline silicon, can achieve a

passivation effect on the back surface, thereby improving the cell efficiency. At least one surface of the front surface or the back surface of the structure can be subjected to texturing treatment to reduce light reflection and improve a light trapping effect, which is conducive to improving the photoelectric conversion efficiency of the cell. An anti-reflection film can be prepared on the texturing surface to further improve the photoelectric conversion efficiency of the cell.

Ex. 1008, 4 (emphasis added).

187. One such advantage, underlined above, is that Li's heterogeneous PN junction solar cell "is prepared by a low-temperature deposition method, which avoids a conventional diffusion process at 800-1000°C." Ex. 1008, 4.

188. Li's own structure uses low-temperature deposition, which results in fewer defects and contamination in silicon materials, improved efficiency, and reduced manufacturing cost. Ex. 1008, 4 ("[Homogeneous PN junction solar] cells have the disadvantages that the high-temperature diffusion may cause more defects in silicon materials, and when pollution is caused by a high-temperature process, cell efficiency will be greatly reduced."); *id.* ("[A] deposition [of amorphous silicon] temperature is low (200°C)", and a process is relatively simple, such that a high-temperature process is avoided, and the manufacturing cost of the cell is reduced."); *id.* ("[Conventional diffusion process at 800-1000°C] will cause more

defects or contamination in a silicon material, which will affect the improvement of cell efficiency.”).

189. In the context of Li’s disclosure, then, a POSITA would not have been motivated to implement Gan’s polysilicon emitter and oxide layer. Construction of Gan’s polysilicon emitter and oxide layer would repeatedly require the kind of high temperature that Li seeks to avoid.

190. Specifically, in Gan’s 12-step process to construct its experimental device, step 3 is “[t]hin thermal oxide growth at 800 °C,” step 4 is “[p]olysilicon deposition (6000 Å) and first-step anneal at 1050 °C,” and step 10 is “[dopant d]rive-in; 900-1000 °C.” Ex. 1005, 246; Ex. 2029, 216:22-217:8 (testifying that Gan’s steps 3, 4, 9, 10 would be implemented in Li)

191. Similarly, a POSITA would not have been motivated to apply Smith’s “in-situ diffusion process,” Paper 3, 75, which also involves the kind of high temperature that Li expressly seeks to avoid:

In FIG. 7, the sample of FIG. 6 is subjected to in-situ steps. The steps are in-situ in that they are performed in one loading of wafer **102** into the wafer processing tool. In one embodiment, the in-situ steps are performed in a furnace. In the first in-situ step, wafer **102** is heated to about 1000° C. for one hour to diffuse dopants from boron-doped silicon dioxide **104** and phosphorus-doped silicon dioxide **501** into wafer **102**. This results in the formation of P+ regions **702** (due to

boron-doped silicon dioxide **104**) and N⁺ regions **703** (due to phosphorus-doped silicon dioxide **501**) in wafer **102**. Note that during the first in-situ step, undoped silicon dioxide **106** beneficially prevents phosphorus from phosphorus-doped silicon dioxide **501** from diffusing into boron-doped silicon dioxide **104**. Also, undoped silicon dioxide **502** beneficially prevents phosphorus from phosphorus-doped silicon dioxide **501** from diffusing into the furnace.

Ex. 1007, 3:39-55 (emphasis added).

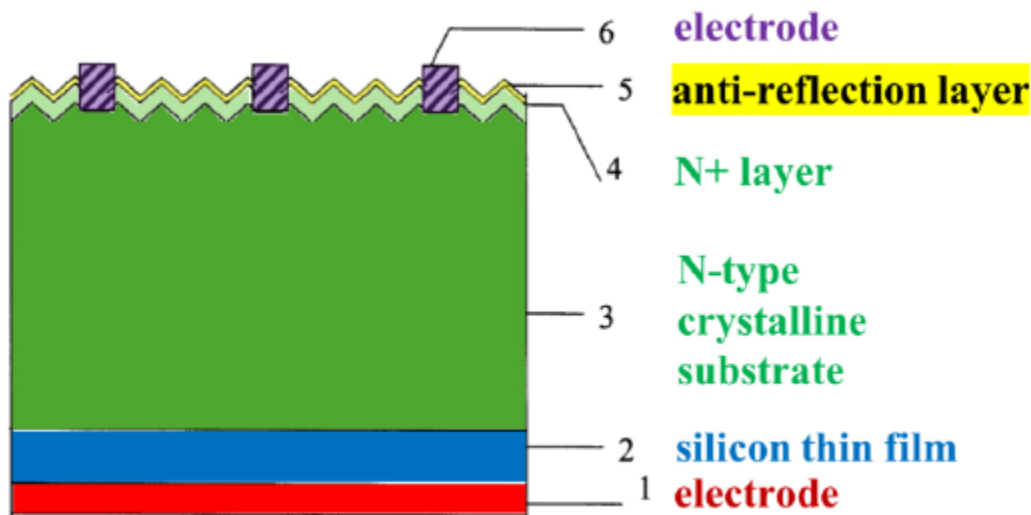
In the second in-situ step, the furnace conditions are changed to about 750° C. with an atmosphere containing phosphorus oxychloride, then to about 975° C. with an atmosphere containing oxygen to diffuse phosphorus as an N-type dopant into wafer **102** from its front side, and to grow a thin layer of silicon dioxide on both sides of wafer **102**. Front side **101** is now labeled as “**101B**” to indicate that there is a thin layer of silicon dioxide on its surface. The thin layer of silicon dioxide advantageously leads to better passivation of the front side and back side surfaces of wafer **102**. In FIG. 7, the front side diffusion of N-type dopants into wafer **102** is schematically represented by arrows **701**. As can be appreciated the use of in-situ steps to drive dopants into wafer **102** simplifies the fabrication process.

Ex. 1007, 3:56-4:2 (emphasis added).

192. Thus, in my opinion, Li’s teaching is in conflict with Gan and Smith’s teachings, and a POSITA would not have combined the three references.

3. *A POSITA Would Not Have Been Motivated to Combine Li and Gan with Smith*

193. For the same reasons discussed in § XI.B.1, the proposed Li-Gan-Smith combination is not an all back contact solar cell. As Petitioner illustrates below, Li's structure, like Froitzheim's structure, includes metal contacts on both sides of the solar cell:



Paper 3, 23 (citing Ex. 1008, Fig. 1) (annotations in Petition); *see also* Ex. 1003, ¶66 (equating “metal contacts” to “electrodes”).

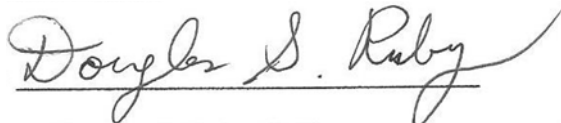
194. As a result, for the same reasons discussed in § XI.A.2, a POSITA would not have been motivated to combine Smith with Li and Gan

XII. CONCLUSION

195. In my opinion, based on my review of the '053 patent, the materials referenced above, and my knowledge of what a POSITA would have known at the time of the invention, the Petition fails to show that any claim is unpatentable.

196. I declare that all statements made herein of my own knowledge are true, and that statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on May 22, 2025 in Albuquerque, New Mexico.

A handwritten signature in cursive script that reads "Douglas S. Ruby". The signature is written in dark ink and is positioned above a horizontal line.

Douglas Ruby, Ph.D.