



Hanwha Solutions Corp. v. Maxeon Solar Pte. Ltd.

IPR2024-01199 (U.S. Patent No. 8,878,053)

IPR2024-01203 (U.S. Patent No. 8,222,516)

Patent Owner's Oral Argument (December 3, 2025)

Maxeon's Exhibit 2030
DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

Summary of Grounds

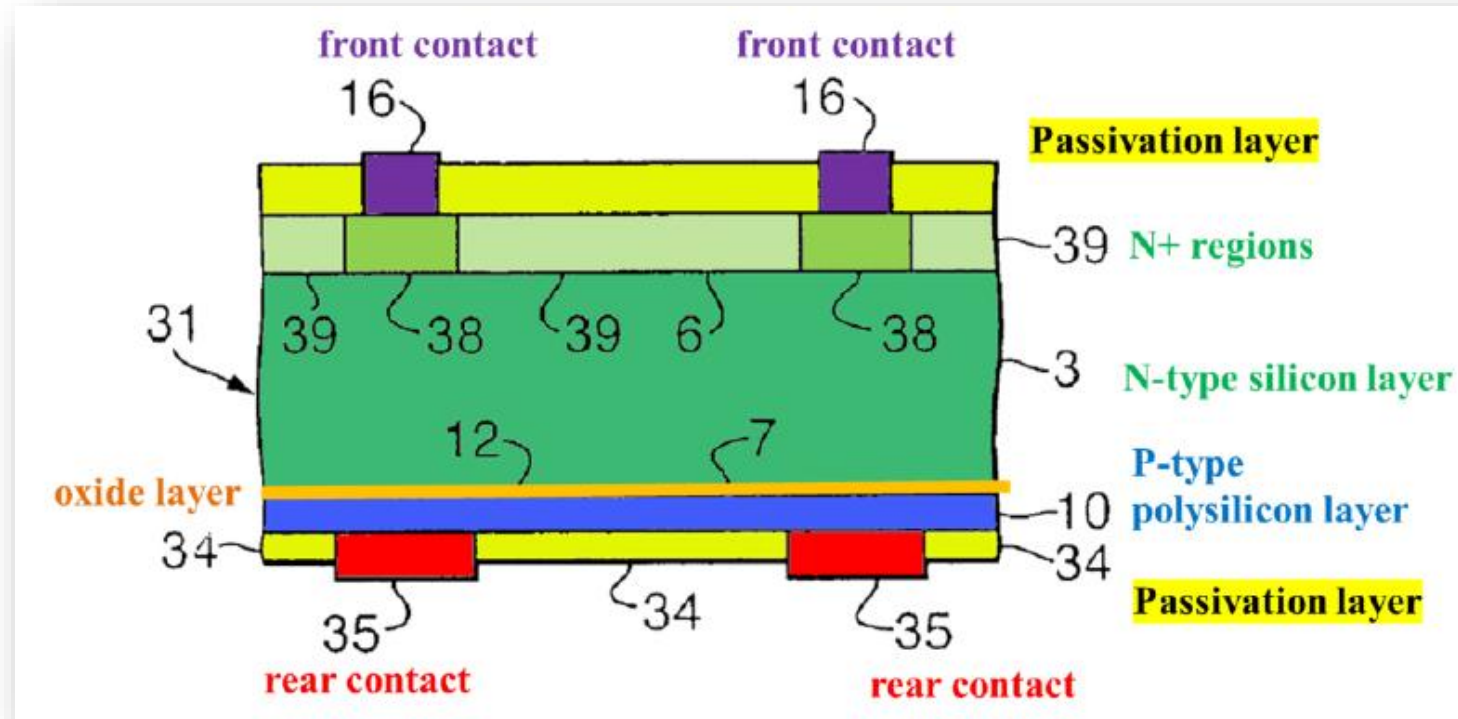
IPR2024-01199 (re the '053 patent)

- Ground I: Froitzheim and Gan (Claims 9-12, 14, 16-20) (Paper 3-Petition, 24-50);
- Ground II: Froitzheim, Gan, and Smith (Claims 1-20) (Paper 3, 50-72);
- Ground III: Li, Gan, and Smith (9-20) (paper 3, 73-88).

IPR2024-01203 (re the '516 patent)

- Ground I: Froitzheim and Gan (Claims 1-4, 6-12) (Paper 3-Petition, 27-60);
- Ground II: Froitzheim, Gan, and Sheats (Claim 5) (Paper 3, 60-63);
- Ground III: Froitzheim and Borden-575 (Claims 1-4, 6-12) (Paper 3, 64-77);
- Ground IV: Froitzheim, Borden-575, and Sheats (Claim 5) (Paper 3, 77-78);
- Ground V: Li and Gan (Claims 1-2, 8-11) (Paper 3, 78-93).

Arguments Against the Proposed Froitzheim-Gan Combination

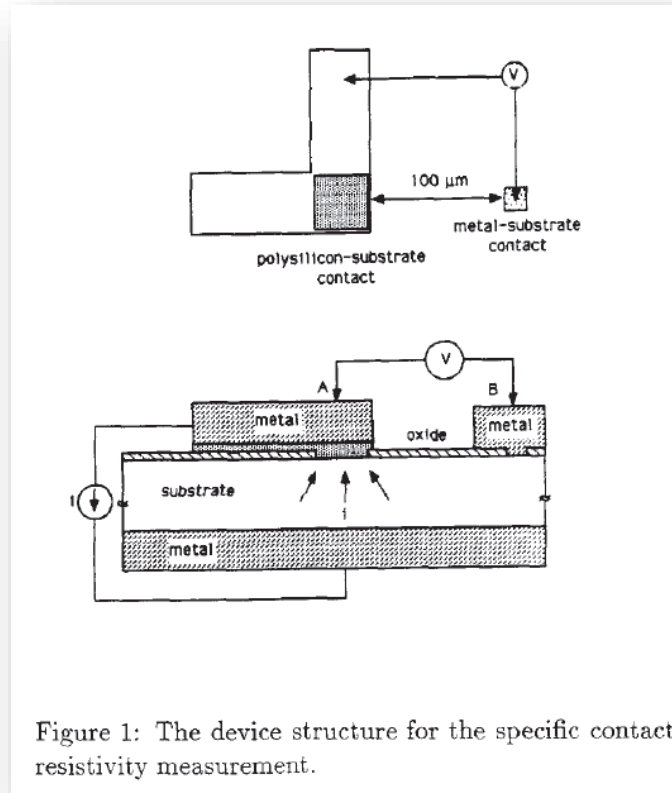


Applicable to:

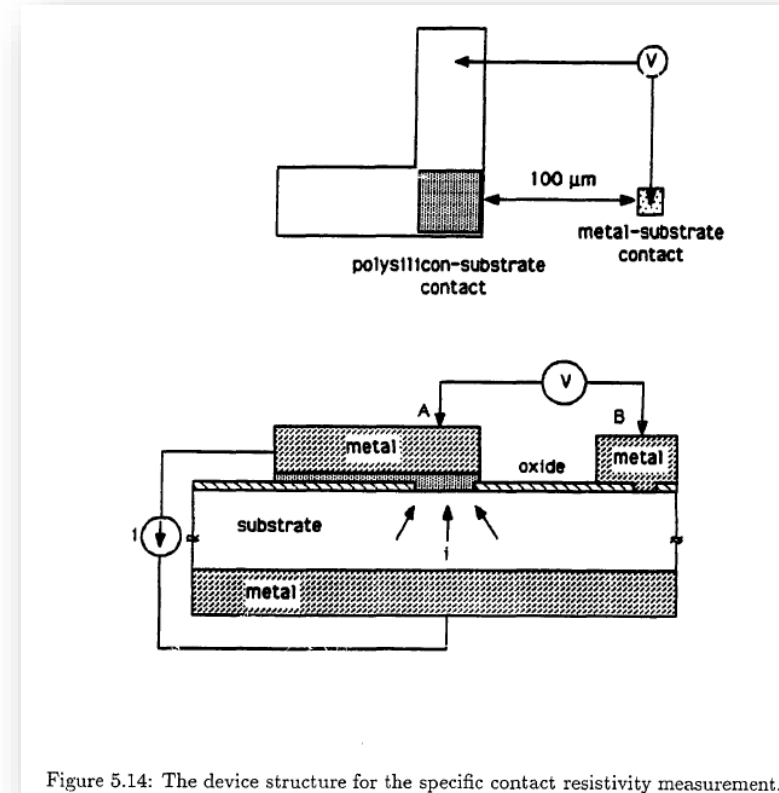
- IPR2024-01199 Ground I (Froitzheim and Gan);
- IPR2024-01199 Ground II (Froitzheim, Gan, and Smith);
- IPR2024-01203 Ground I (Froitzheim and Gan);
- IPR2024-01203 Ground II (Froitzheim, Gan, and Sheats).

The Proposed Froitzheim-Gan Combination
(illustrated in IPR2024-01199, Paper 3-Petition, 25;
see also IPR2024-01203, Paper 3-Petition, 28)

The Gan Thesis Discusses Gan's Structure



Ex. 1005-Gan, Fig. 1



Ex. 2003-The Gan Thesis, 93

(both cited in IPR2024-01199, Paper 40-PO's Sur-Reply, 6)

The Gan Thesis Discusses Gan's Structure

1. Field oxidation (2000 Å)*.
2. Polysilicon-substrate contact opening*.
3. Thin thermal oxide growth at 800 °C*. (10-minute oxygen flow)
4. Polysilicon deposition (6000 Å) and first-step anneal (1050 °C)*.
5. First-step anneal*.
6. Polysilicon finger definition.
7. Undoped glass deposition (2000 Å).
8. Metal-polysilicon and metal-substrate contact opening.
9. Doped glass deposition on both sides of the wafer*.
10. Drive-in; 900-1000 °C*.
11. Doped glass stripping and Al-1% Si alloy deposition.
12. Metal finger definition.

- Left: Ex. 1005-Gan, 246;
- Top right: Ex. 2003-The Gan Thesis, 92;
- Bottom right: Ex. 2003, 79;

(all cited in IPR2024-01199, Paper 40-Sur-Reply, 6).

1. Field oxidation (2000 Å)*.
2. Polysilicon-substrate contact opening*.
3. Thin thermal oxide growth*. (10-minute oxygen flow)
4. Polysilicon deposition (6000 Å) and first-step anneal (1050 °C)*.
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11. Metal finger definition.

J_0 of the p-type polysilicon SIS emitter. With this in mind, a very thin thermally grown oxide was used in the hope that it would have a lower interface defect state density. The procedure of sample preparation is shown as followings.

1. $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$ (4:1) clean 10 minutes at 90 °C.
2. DI water rinse 10 minutes.
3. $\text{HCl} + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$ (1:1:5) clean 10 minutes at 70 °C.
4. DI water rinse 10 minutes.
5. 50:1 HF dip until wafer is hydrophobic.
6. DI water rinse 10 minutes.
7. Thermal oxidation 10 minutes at 800 °C.
8. LPCVD Undoped polysilicon deposition at 600 °C for 6000 Å.
9. Doped-glass deposition
 - Boron-doped glass for p-type.
 - Phosphorus-doped glass for n-type.
10. Drive-in at 900 °C for 4 hours.
11. Forming gas anneal (FGA) 30 minutes at 400 °C.

The Gan Thesis Documents Problems with Oxide Breakup

Although a thermally grown interfacial oxide seems essential for a polysilicon emitter to have both low J_0 and ρ_c , the breakup process is still difficult to control. On several occasions, we have encountered reproducibility problems. For example, we find that the ρ_c is quite different between two separate experiments with identical processing conditions. Even worse, solar cells that were made in this study all suffered high contact resistance.

The problem is primarily due to insufficient oxide breakup, and is caused by the fluctuation of the thickness of the interfacial oxide. In the next section, we first show

Later, in the real solar cell runs, the situation got even worse. The solar cells made in the experiment are the 15- μm -contact-line IBC which have been shown and simulated in Chapter 2. We found that, with the OCVD measurement, the total specific contact resistivity ($\rho_n + \rho_p$) was higher than $1 \times 10^{-3} \Omega\text{-cm}^2$. Although the ($J_{on} + J_{op}$) measured from those cells are between 8×10^{-14} and $4 \times 10^{-14} \text{ A/cm}^2$, the cell efficiency is greatly degraded by such a high emitter resistance. Figure 6.2 is

As shown in the figure, the cell is in fact plagued by two things: the high surface recombination velocity ($S = 58 \text{ cm/sec}$), and high emitter resistance ($\rho_{cn} + \rho_{cp} = 1 \times 10^{-3} \Omega\text{-cm}^2$). The effect of high emitter resistance is shown by the difference of the cell efficiency between the curve (b) and the curve (c), while the difference between the curve (a) and the curve (c) shows the projected effect of the high surface recombination velocity. Without the high surface recombination velocity and the emitter resistance, the cell performance would be the curve formed by the maximum efficiency between the curve (a) and the curve (b) which is the ultimate performance we can have for the cell with polysilicon emitters.

From the low emitter recombination and high emitter resistance, it is clear that the interfacial oxide did not break as we expected.

- Top left: Ex. 2027-The Gan Thesis, 107;
- Bottom left: Ex. 2027, 110;
- Right: Ex. 2027, 110;

(all cited in IPR2024-01199, Paper 29-POR, 28-29; see also IPR2024-01203, Paper 29-POR, 32-33).

The Gan Thesis Documents

Problems with Oxide Thickness

In practice, there is another difficulty we may have to face if the tunnel barrier height is around the range shown in Figure 4.3. Figure 4.3 is the transmission probability of both electrons and holes plotted with the tunneling barrier height reported by Kasprzak *et al.*. As shown in the figure, for the T_h and T_e specified in the beginning of this section, it corresponds to an oxide-thickness window 15 ± 2 Å. With a window so narrow, it is not possible to have good control over the characteristics of a polysilicon SIS emitter.

Although these results can be attributed to many other reasons, the following experiment shows that the effect of the oxide thickness cannot be ignored. This, combined with the non-reliable oxide-growth recipe gives rise to the mishap of our solar-cell runs.

It becomes clear that the wide fluctuation of our results is mainly due to the poor control over the oxide thickness. From Eqn. (4.21) (p. 61), ρ_c does not depend on the oxide thickness once the oxide breaks up. Consequently, the oxide-thickness dependence of ρ_c must result from the oxide breakup process. To see how the oxide

- Top left: Ex. 2027-The Gan Thesis, 56;
- Middle left: Ex. 2027, 111;
- Bottom left: Ex. 2027, 114;

(all cited in IPR2024-01199, Paper 29-POR, 27-29; see also IPR2024-01203, Paper 29-POR, 31-33).

6.5 Conclusion

In this chapter, we found that a consistent result of ρ_c is difficult to reproduce for the polysilicon emitter with a thermally grown interfacial oxide. This is mainly attributed to the fact that our thin-oxide growth recipe is not reliable. With the same oxidation schedule, a wide variation of oxide thicknesses have been found for different times. Experimentally, the interfacial oxide breakup was also found to depend on the oxide thickness critically. Such an oxide-thickness dependence of the breakup process can be explained by a “silicon cluster nucleation” process. In order to have reproducible results, it appears that a precise control of the oxide thickness is necessary.

7.2 Suggestions for Future Study

It appears that the oxide breakup depends critically on the interfacial oxide thickness. The thin-oxide growth recipe used in this work was not reliable; the oxide thicknesses between 15 to 20 Å have been found with the same growth condition. As a result, this contributes to the fluctuation of the ρ_c results. It is then clear that a more reliable way of growing the thin oxide is needed.

- Top right: Ex. 2027, 116-17;
- Bottom right: Ex. 2027, 119.

Individually Known Elements Do Not Overcome Obviousness

(a) The TSM test captures a helpful insight: A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art. Although common sense directs caution as to a patent application claiming as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the art to combine the elements as the new invention does. Inventions usually rely upon building blocks long since uncovered, and claimed discoveries almost necessarily will be combinations of what, in some sense, is already known. Helpful insights,

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 401 (2007)
(cited in IPR2024-01199, Paper 29-POR, 31;
see also IPR2024-01203, Paper 29-POR, 35)

[20] To be sure, “to have a reasonable expectation of success, one must be motivated to do more than merely to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful.” *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed.Cir.2006) (internal quotations omitted). Pfizer argues that, if anything, amlodipine in its besylate salt form would at most be “obvious to try,” i.e., to vary all parameters or try each of numerous possible choices to see if a successful result was obtained. *O’Farrell*, 853 F.2d at 903.

Pfizer, Inc. v. Apotex Inc., 480 F.3d 1348, 1365 (Fed. Cir. 2007)
(cited in IPR2024-01199, Paper 40-Sur-Reply, 8;
see also IPR2024-01203, Paper 40-Sur-Reply, 6)

Arguments Against Applying Smith's Processes

A POSITA would have understood that Smith's APCVD, diffusion barrier, and in-situ diffusion processes applied to Froitzheim's and Gan's methods would have been desirable because the front side and the back side of the wafers could be doped at the same time, decreasing cost and the number of required steps.

IPR2024-01199, Paper 3-Petition, 55 (ground I); *see also id.* at 75 (ground III)

Applicable to:

- IPR2024-01199 Ground II (Froitzheim, Gan, and Smith);
- IPR2024-01199 Ground III (Li, Gan, and Smith).

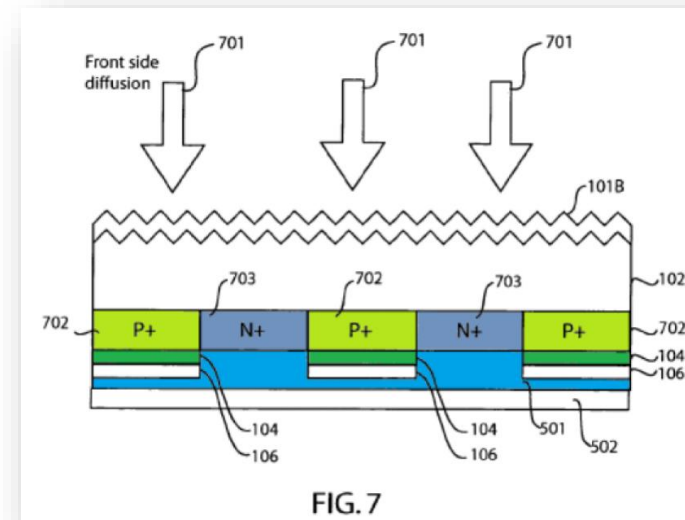
Argument Against the Applicability of Smith's APCVD

For instance, Smith teaches that dopants can be deposited on the substrate using “APCVD.” Ex.1007-Smith, 2:44-49. APCVD creates a layer of dopants on one side of the solar cell intended to be doped, which serves as a dopant source. After APCVD, “an undoped silicon dioxide” layer can be placed on the dopant source. Ex.1007-Smith, 2:53-60. The undoped silicon dioxide layer acts as a barrier to diffusion, meaning that the dopants are diffused only in the intended target region. *Id.*, 3:50-55. Smith teaches that these steps “advantageously allow[] for one-sided deposition,” which is “particularly useful in the manufacture of back side contact solar cells where only one side of the solar cell is textured.” *Id.*, 2:58-62. Ex.1003-Decl., ¶¶205-206.

IPR2024-01199, Paper 3-Petition, 25

regions. In a back side contact solar cell, the doped regions are coupled to metal contacts on the back side of the solar cell to allow an external electrical circuit to be coupled to and be powered by the solar cell. Back side contact solar

Ex. 1007-Smith, 1:29-33 (quoted in IPR2024-01199, Paper 29, 45)



Ex. 1007, Fig. 7 (annotated in IPR2024-01199, Paper 29-POR, 44)

Argument Against the Applicability of Smith's In-Situ Steps

In FIG. 7, the sample of FIG. 6 is subjected to in-situ steps. The steps are in-situ in that they are performed in one loading of wafer 102 into the wafer processing tool. In one

A POSITA also would have been motivated to apply Smith's "in-situ steps" to the combination of Froitzheim and Gan to drive in the dopants to their target regions, which "simplifies the fabrication process." Ex.1007-Smith, 3:40-4:2. Smith explains that in-situ diffusion means that the steps are "performed in one loading of [the] wafer [] into the wafer processing tool." *Id.*, 3:40-42. A POSITA would have found this advantageous because it would simplify the process and decrease costs.

Ex.1003-Decl., ¶209.

209. A person of ordinary skill in the art would have also been motivated to manufacture the combination of Froitzheim and Gan using Smith's "in-situ" diffusion process. Smith's teaching of "in-situ" diffusion to "simplif[y] the fabrication process" would have been another motivating reason to use Smith's processes to create the combined structure of Froitzheim and Gan. Ex.1007-Smith, 3:40-4:2. Smith states that "in-situ" diffusion means that the steps are "performed in one loading of wafer [] into the wafer processing tool." Ex.1007-Smith, 3:40-42.¹¹ A person of ordinary skill in the art would have found in-situ diffusion (and the simultaneous diffusion from multiple dopant sources, or "co-diffusion," in general) advantageous because it would simplify fabrication by reducing processing steps, thereby decreasing costs. For example, Krygowski reported in 1997 that the

- Left: IPR2024-01199, Paper 3-Petition, 55;
- Top right: Ex. 1007-Smith, 3:40-42;
- Bottom right: Ex. 1003-Holman Decl., ¶ 209 (partial).

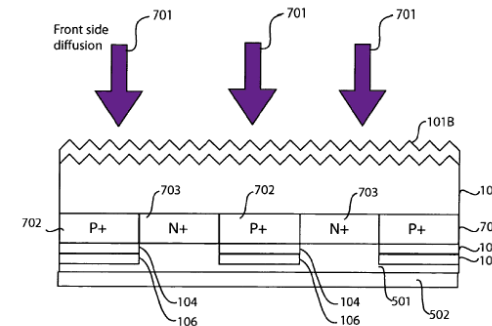
Improperly Incorporating Smith Elements

As discussed in Section X.B.2.c, Smith teaches the first doped oxide layer 104 (i.e., first dopant source layer) is “boron-doped silicon dioxide (SiO₂) (‘BSG’),” which is a p-type dopant source. Ex.1007-Smith, 2:44-64; see also Ex.1001-USP053, 4:21-24 (discussing BSG).



Ex.1007-Smith, Fig.2. As discussed in Section X.B.1, a POSITA would have been motivated to modify the combination of Froitzheim and Gan to implement Smith’s diffusion methods with a reasonable expectation of success, which would involve forming a first dopant source layer comprising borosilicate glass to dope the polysilicon emitter. Ex.1003-Decl., ¶230.

Smith also teaches these elements. See Section X.B.2.d. Smith’s Figure 7 teaches a method of diffusing phosphorus dopants into the front surface of the silicon substrate comprising forming second dopant source layer (phosphorus dopant layer) over the silicon substrate and diffusing dopants from the second dopant source layer into the silicon substrate. The arrows (“front side diffusion” 701) below indicate dopant being driven into substrate by diffusion. Smith explains that in step 701, “phosphorus oxychloride” (POCl₃) is used, which involves (1) forming a layer of glass with phosphorous dopants at the silicon surface (i.e., forming a second dopant source layer), and (2) diffusing phosphorous dopants from the glass layer into the silicon substrate (i.e., diffusing dopants). Ex.1007-Smith, 3:56-60, claims 1, 9, 14, 17, 20; e.g., Ex.1052-Avery, 1:19-31.



Ex.1007-Smith, Fig.7. As discussed in Section X.B.1, a POSITA would have been motivated to modify the combination of Froitzheim and Gan to implement Smith’s diffusion methods with a reasonable expectation of success. Ex.1003-Decl., ¶¶232-234.

- Left: IPR2024-01199, Paper 3-Petition, 60-61 (discussing claim 11);
- Right: IPR2024-01199, Paper 3, 61-62 (discussing claim 12).

Improperly Raising New Arguments

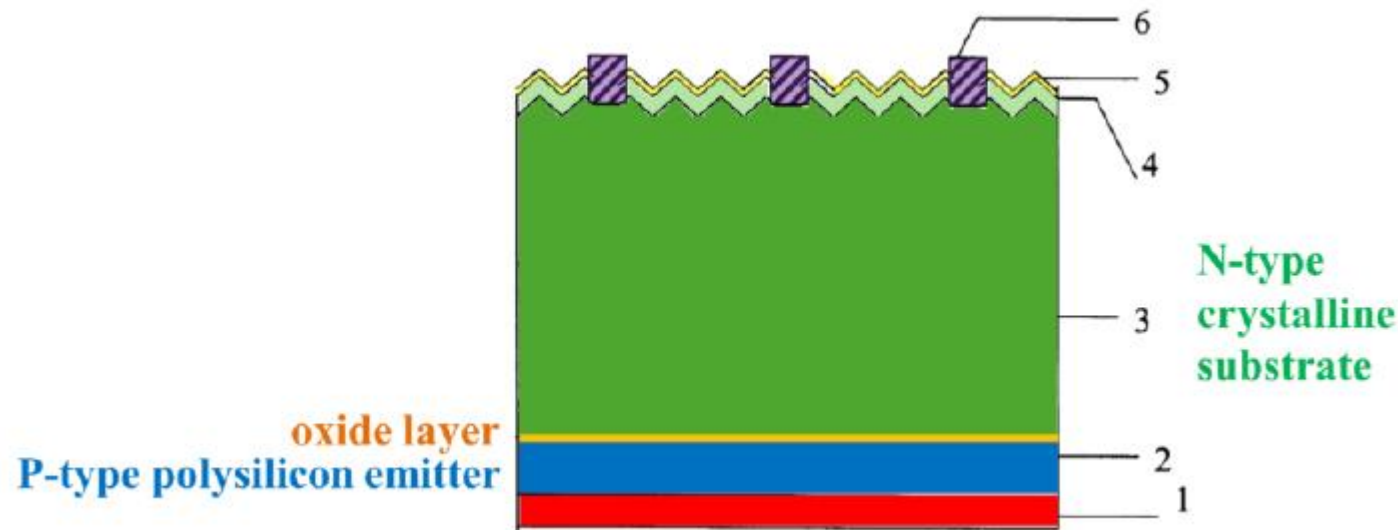
The Petition also explains how Smith teaches the recited features of claims 2-5 and 11-14 and why such features are obvious in the combination of Froitzheim, Gan, and Smith. Specifically, claims 2-4 and 11-13 recite routine manufacturing steps (which Maxeon does not dispute), and Smith's teachings that Petitioner relies on for these claims are within the context of Smith's APCVD teachings. Pet., 54-56. Thus, because the Petition explains a POSITA would have been motivated to apply Smith's APCVD teachings to manufacture the combination of Froitzheim and Gan, Maxeon's assertion that the Petition is deficient lacks merit. *Id.* Similarly,

A POSITA would have understood that Smith's APCVD, diffusion barrier, and in-situ diffusion processes applied to Froitzheim's and Gan's methods would have been desirable because the front side and the back side of the wafers could be doped at the same time, decreasing cost and the number of required steps. Otherwise, the wafer would have to be removed from the machine, prepared for the next loading (such as by applying masking layers to protect previously doped surfaces), reloaded into the machine, and then further processed (such as by removing the masking layers), increasing cost from the added steps. Ex.1003-Decl., ¶210.

Finally, in addition to the reasons in Section X.A.1, a POSITA would have reasonably expected success at using Smith's manufacturing techniques to manufacture the combination of Froitzheim and Gan, including because the references teach compatible manufacturing steps and the manufacturing steps were well-known and routine steps that were within a POSITA's skillset. *Uber*, 957 F.3d at 1339. Thus, using Smith's teachings to manufacture the combination of Froitzheim and Gan simply involves using known manufacturing techniques to improve known solar cell designs in a similar way. *KSR*, 550 U.S. at 417; *Tokai*, 632 F.3d at 1372. Ex.1003-Decl., ¶¶211-213.

- Left: IPR2024-01199, Paper 37-Reply, 26;
- Right: IPR2024-01199, Paper 3-Petition, 55-56.

Arguments Against the Proposed Li-Gan-Smith Combination



Applicable to:

- IPR2024-01199 Ground III (Li, Gan, and Smith);
- IPR2024-01203 Ground V (Li and Gan).

The Proposed Li-Gan-Smith Combination
(illustrated in IPR2024-01199, Paper 3-Petition, 77);
see also IPR2024-01203, Paper 3-Petition, 86)

The Standard for Finding Teaching Away

Patent Owner's Case:

[9] Substantial evidence, moreover, supports the Board's finding that Gross does not otherwise teach away from the claimed method. "A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 27 F.3d 551, 553 (Fed.Cir.1994). Although Gross generally discloses a relatively longer reaction time that results in fiber capable of forming stable dispersions, Gross does not criticize or discredit the use of a shorter reaction time. Accordingly, we conclude that the Board did not err in affirming the Examiner's decision that claims 43–50 and 52–68 of the '614 application would have been obvious over the cited references.

In re Urbanski, 809 F.3d 1237, 1244 (Fed. Cir. 2016)
(cited in IPR2024-01199, Paper 29-POR, 51;
see also IPR2024-01203, Paper 29-POR, 67)

Petitioner's Case:

reference. Under the proper legal standard, a reference will teach away when it suggests that the developments flowing from its disclosures are unlikely to produce the objective of the applicant's invention. *In re Gurley*, 27 F.3d 551, 553 (Fed.Cir.1994). A statement that a particular combination is not a preferred embodiment does not teach away absent clear discouragement of that combination. *In re Fulton*, 391 F.3d at 1199–1200.

Syntex (U.S.A.) LLC v. Apotex, Inc., 407 F.3d 1371, 1380 (Fed. Cir. 2005)
(cited in IPR2024-01199, Paper 37-Reply, 27;
see also IPR2024-01203, Paper 37-Reply, 25)

Li Teaches Away from High-Temperature Diffusion

II. Background Art

Crystalline silicon solar cells account for more than 90% of photovoltaic market shares in the global world. Such cells generally adopt P-type crystalline silicon to form an N-type emitting region through high-temperature diffusion and belong to homogeneous PN junction solar cells. However, such cells have the disadvantages that the high-temperature diffusion may cause more defects in silicon materials, and when pollution is caused in a high-temperature process, cell efficiency will be greatly reduced. Thus, higher requirements are put forward for both materials and a production environment. In addition, back surfaces of such cells are free of effective passivation and an effective light trapping structure. Thus, recombination on the back surfaces is relatively serious, and a part of light penetrates an active region of the cells and is not absorbed. These disadvantages are reasons that limit improvement of the efficiency of conventional solar cells.

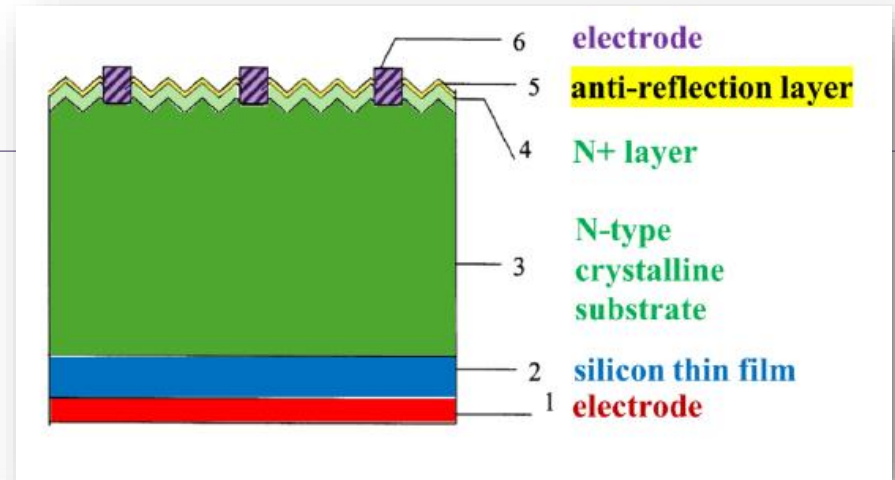
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Adoption of the amorphous silicon emitting region has the advantage that the amorphous silicon has a good surface passivation effect. Moreover, a deposition temperature is low (200°C), and a process is relatively simple, such that a high-temperature process is avoided, and the manufacturing cost of the cell is reduced.

Ex. 1008-Li Translation, 3
(quoted in IPR2024-01199, Paper 29-POR, 52;
see also IPR2024-01203, Paper 29-POR, 67-68)

Li Uses Low-Temperature Diffusion

Top/Right: Ex. 1008-Li Translation, Fig. 1
(illustrated in IPR2024-01199, Paper 3-Petition, 23;
see also IPR2024-01203, Paper 3-Petition, 24)
(annotations in Petitions)



A technical means adopted in the present invention is to achieve an emitting region by depositing the silicon thin film on the back surface of the cell. Compared with a P-type silicon wafer diffused N-type emitting region used in most factories at present, the N-type silicon can effectively reduce the generation of boron-oxygen defects under illumination and resulting attenuation of conversion efficiency. In addition, a PN junction is prepared by a low-temperature deposition method, which avoids a conventional diffusion process at 800-1000°C. Such high-temperature process will cause more defects or contamination in a silicon material, which will affect the improvement of cell efficiency. In addition, the silicon thin film deposited on the back surface of the silicon wafer, whether it is amorphous silicon, microcrystalline silicon, or nanocrystalline silicon, can achieve a passivation effect on the back surface, thereby improving the cell efficiency. At least one surface of the front surface or the back surface of the structure can be subjected to texturing treatment to reduce light reflection and improve a light trapping effect, which is conducive to improving the photoelectric conversion efficiency of the cell. An anti-reflection film can be prepared on the texturing surface to further improve the photoelectric conversion efficiency of the cell.

Bottom/Left: Ex. 1008, 4
(quoted in IPR2024-01199, Paper 29-POR, 52; see
also IPR2024-01203, Paper 29-POR, 67-68)

Gan Uses High Temperature Diffusion

1. Field oxidation (2000 Å)*.
2. Polysilicon-substrate contact opening*.
3. Thin thermal oxide growth at 800 °C*. (10-minute oxygen flow)
4. Polysilicon deposition (6000 Å) and first-step anneal (1050 °C)*.
5. First-step anneal *.
6. Polysilicon finger definition.
7. Undoped glass deposition (2000 Å).
8. Metal-polysilicon and metal-substrate contact opening.
9. Doped glass deposition on both sides of the wafer*.
10. Drive-in; 900-1000 °C*.
11. Doped glass stripping and Al-1% Si alloy deposition.
12. Metal finger definition.

Ex. 1005-Gan, 246
(cited in IPR2024-01199, Paper 29-POR, 52;
see also IPR2024-01203, Paper 29-POR, 68)

22 Q In this Li-Gan-Smith combination, are we
1 still implementing Gan's Steps 3, 4, 5, 9, and 10
2 that we discussed earlier?
3 A We are certainly implementing Gan's
4 teaching for oxide layer and P-type polysilicon
5 emitter. And those teachings are -- one
6 embodiment of those teachings are shown in Gan's
7 3, 4, 9, 10. Were those the numbers that you
8 mentioned?

Ex. 2029-Holman Dep. Tr., 216:22-217:8
(cited in IPR2024-01199, Paper 29, 52-53 (citing Ex. 2029, 216:22-217:7).

Smith Uses High Temperature Diffusion

As discussed in Section X.B.1, a POSITA would have been motivated to obtain the manufacturing efficiencies Smith teaches. As with Froitzheim, a POSITA looking to manufacture Li's rear junction solar cell with Gan's polysilicon emitter and oxide layer would have known that decreasing manufacturing costs was, like increasing cell efficiency, an important consideration. For instance, a POSITA would have understood that Smith's APCVD, diffusion barrier, and in-situ diffusion processes applied to Li's and Gan's methods would have been desirable because the front side and the back side of the wafers could be doped at the same time, decreasing cost and the number of required steps. Section X.B.1. Therefore, a POSITA would have been motivated to manufacture the combination of Li and Gan using Smith's techniques because doing so would improve the efficiency of Li's cell and simplify the manufacturing process. Ex.1003-Decl., ¶¶287-288.

In FIG. 7, the sample of FIG. 6 is subjected to in-situ steps. The steps are in-situ in that they are performed in one loading of wafer 102 into the wafer processing tool. In one embodiment, the in-situ steps are performed in a furnace. In the first in-situ step, wafer 102 is heated to about 1000° C.

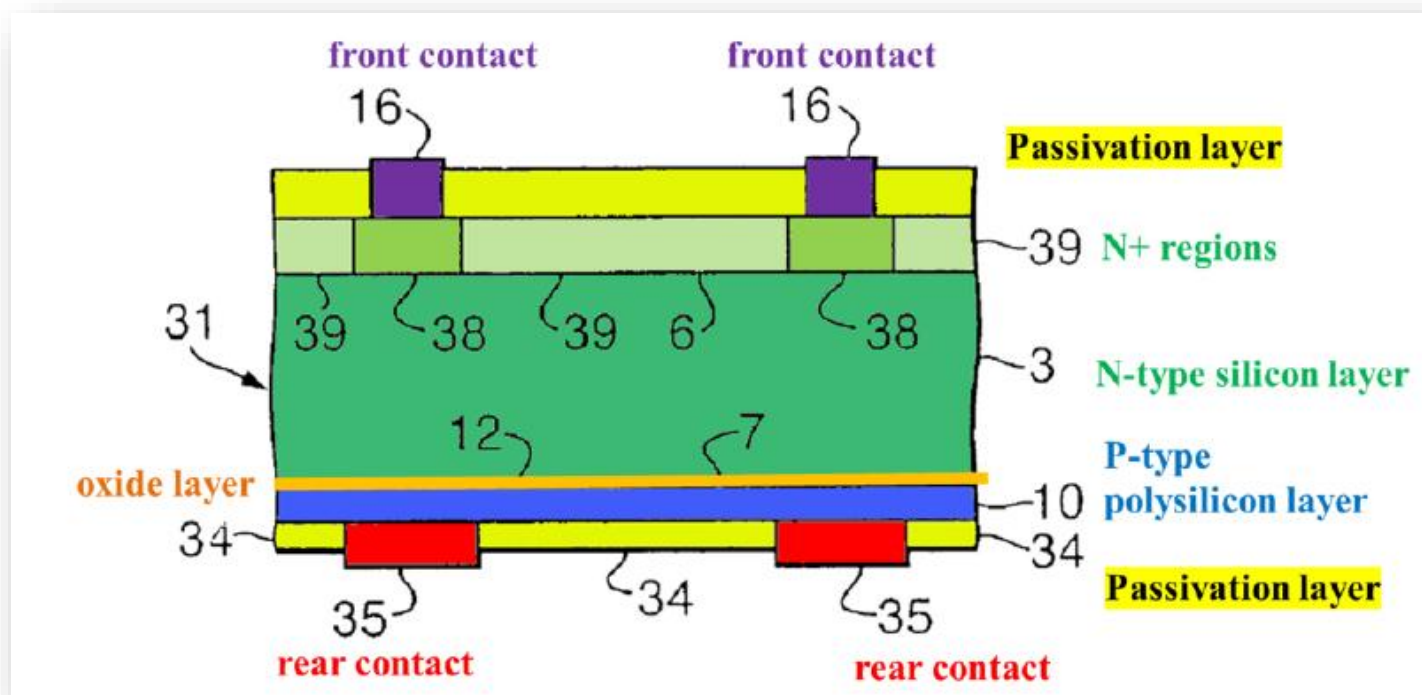
In the second in-situ step, the furnace conditions are changed to about 750° C. with an atmosphere containing phosphorus oxychloride, then to about 975° C. with an atmosphere containing oxygen to diffuse phosphorus as an N-type dopant into wafer 102 from its front side, and to grow a thin layer of silicon dioxide on both sides of wafer 102.

- Top: Ex. 1007-Smith, 3:40-44 (cited in IPR2024-01199, Paper 29-POR, 53);
- Bottom: Ex. 1007, 3:56-61 (cited in IPR2024-01199, Paper 29, 53).

Arguments Against the Proposed Froitzheim-Borden-575 Combination

Applicable to:

- IPR2024-01203 Ground III (Froitzheim and Borden-575);
- IPR2024-01203 Ground IV (Froitzheim, Borden-575, and Sheats).



The Proposed Froitzheim-Borden-575 Combination
(illustrated in IPR2024-01203, Paper 3-Petition, 65)

Unclear Whether Borden-575's Buried Oxide Is Included

Maxeon's "impermissibly vague" argument attempts to fabricate ambiguity where none exists. POR, 51-55. As the Petition explains (Pet., 69-70), Borden-575's "buried oxide" and "tunnel oxide" each meet the challenged claims' oxide limitation. See also Ex.1006-Borden-575, claim 10 (buried oxide "layer is less than about 20Å thick"), [0022] (tunnel oxide "typically 8 to 15Å thick"). Maxeon offers no claim construction that would suggest otherwise. POR, 27. The Petition's motivation to combine analysis properly focuses on why a POSITA would have been motivated to obtain benefits by "implementing Borden-575's polysilicon emitter and tunnel oxide layer to the backside configuration taught by Froitzheim." Pet., 65.

IPR2024-01203, Paper 37-Reply, 20

Petitioner's Arguments Fail Either Way

The proposed Froitzheim-Borden-575 combination is impermissibly vague:
Does it include Borden-575's buried oxide or not?
(argued in Paper 29-POR, 51-53)

Yes

Petitioner failed to show why a POSITA would have used Borden-575's buried oxide
(argued in Paper 29, 54-55)

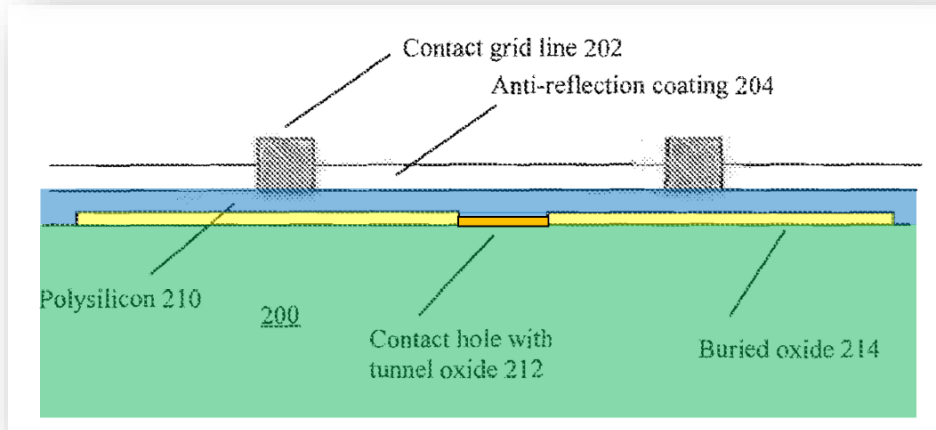
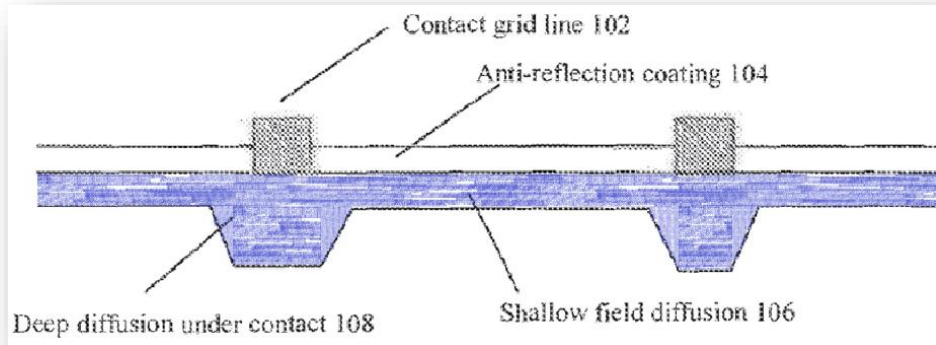
No

A POSITA would not have implemented Borden-575's polysilicon emitter without Borden-575's buried oxide
(argued in Paper 29, 59-62)

And

Borden-575's buried oxide requires contact holes
(which are not in the proposed combination)
(argued in Paper 29, 63-65)

Borden-575's Polysilicon Emitter and Buried Oxide Go Together



- Top left: Ex. 1006-Borden-575, Fig. 1 (annotated in Paper 29, 60);
- Bottom left: Ex. 1006, Fig. 2 (annotated in Paper 3-Petition, 68);
- Top right: Ex. 1006, ¶ [0019] (quoted in Paper 29, POR, 61);
- Bottom right: Ex. 1006, ¶ [0024] (quoted in Paper 29, POR, 61 (citing Ex. 1006, ¶ [0003] [sic])).

[0019] FIG. 2 shows an example cell structure in accordance with embodiments of the invention. As shown in FIG. 2, the cell structure includes an insulating (e.g. oxide) layer 214 under the doped region 210 and the contact 202. This insulating layer 214 isolates the contact 202 from the substrate 200. According to some aspects of the invention, if the insulating layer 214 is made using a material that passivates silicon, such as thermal SiO₂, then the solar cell surface has very good passivation and a low surface recombination velocity, both in the field region 210 and under the contacts 202. Contact holes 212 are provided in the insulating layer 212 to allow for photocurrent flow. In embodiments described in more detail below, contact holes 212 include a tunnel oxide. However, this is not necessary in all embodiments.

[0024] It should be noted that, according to aspects of the invention, the contact metal 202 is blocked from reaching the substrate 200 by the buried oxide 214. This enables contacting to the thin emitter without use of a sophisticated contact process.

Borden-575's Buried Oxide and Contact Holes Go Together

[0002] Conventional silicon (Si) based solar cells comprise a base layer of crystalline Si doped with boron. At the side facing the sun during normal operation (the front side), an n-doped layer is provided e.g. by diffusion of phosphorous into the base layer. This so-called emitter layer forms a p/n-junction with the p-doped base layer. Front and rear side contacts are arranged that are in electrical connection with the n-doped layer and the p-doped base layer, respectively, to withdraw a photocurrent from both sides of the p/n-junction.

[0008] In furtherance of these and other aspects, a solar cell according to embodiments of the invention includes an emitter layer formed on a semiconductor substrate; and an insulating layer between the emitter layer and a surface of the substrate, the insulating layer being patterned to include contact holes that allow current flow therethrough.

[0009] In additional furtherance of these and other aspects, a method of fabricating a solar cell according to embodiments of the invention includes forming an insulating layer on a surface of a semiconductor substrate; patterning contact holes in the insulating layer that allow current flow therethrough; and forming an emitter layer on the insulating layer.

- Top: Ex. 1004-Froitzheim, ¶ [0002] (quoted in Paper 29-POR, 64-65);
- Bottom: Ex. 1006-Borden-575, ¶¶ [0008, 8] (quoted in Paper 29, 63-64).

Argument Against Implementing Borden-575's Tunnel Oxide

[0005] Another method to passivate contacts is to place a thin tunnel oxide – typically 15Å thick – under the metal contacts. Such types of contacts are also well known, and have been used commercially by Schott solar to manufacture MIS solar cells. However, such solar cells have not been commercially introduced, possibly because of the difficulty of reliably forming a thin tunnel oxide.

- Left: Ex. 1006-Borden-575, ¶ [0005];
- Top right: Ex. 1006, ¶ [0019];
- Bottom right: Ex. 1006, ¶ [0026];

(all cited in IPR2024-01203, Paper 29-POR, 56-57).

[0019] FIG. 2 shows an example cell structure in accordance with embodiments of the invention. As shown in FIG. 2, the cell structure includes an insulating (e.g. oxide) layer 214

...

layer 212 to allow for photocurrent flow. In embodiments described in more detail below, contact holes 212 include a tunnel oxide. However, this is not necessary in all embodiments.

[0026] FIG. 4 shows an example embodiment of the process flow for fabricating a solar cell structure according to aspects of the invention. First in step S402, the wafer is

...

is then removed. The wafer is then cleaned and, in one embodiment shown in FIG. 4, a tunnel oxide is grown in the contact holes using a process such as ISSG or Radox in the step S406. Another embodiment does not use the tunnel oxide, and processing advances directly from step S404 to S408.

Argument Against Implementing Borden-575's Tunnel Oxide

[0022] In embodiments, the doped region 210 is formed using polysilicon, which may be deposited at a temperature on the order of 630°C and is in-situ doped. A short anneal at 1050°C for 30 seconds after deposition activates the dopants. As mentioned above, in some embodiments a thin tunnel oxide may be included between the substrate 200 and the polysilicon 210 in the contact holes 212. This oxide – typically 8 to 15Å thick – provides passivation between the substrate and the polysilicon, while allowing for tunnel current flow.

Table 1: The effect of the second-step anneal on J_o and ρ_c .

	N-type		P-type	
	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$
900 °C-4 hour	2.4	18	3.5	18
1000 °C-30 min	4.5	~ 6	8.2	3.8
1000 °C-60 min	7.9		10.5	

- Top left: Ex. 1006-Borden-575, ¶ [0022];
- Bottom left: Ex. 1005-Gan, Table 1.
- Right: Ex. 1005, Fig. 6;

(all cited in IPR2024-01203, Paper 29-POR, 57-58).

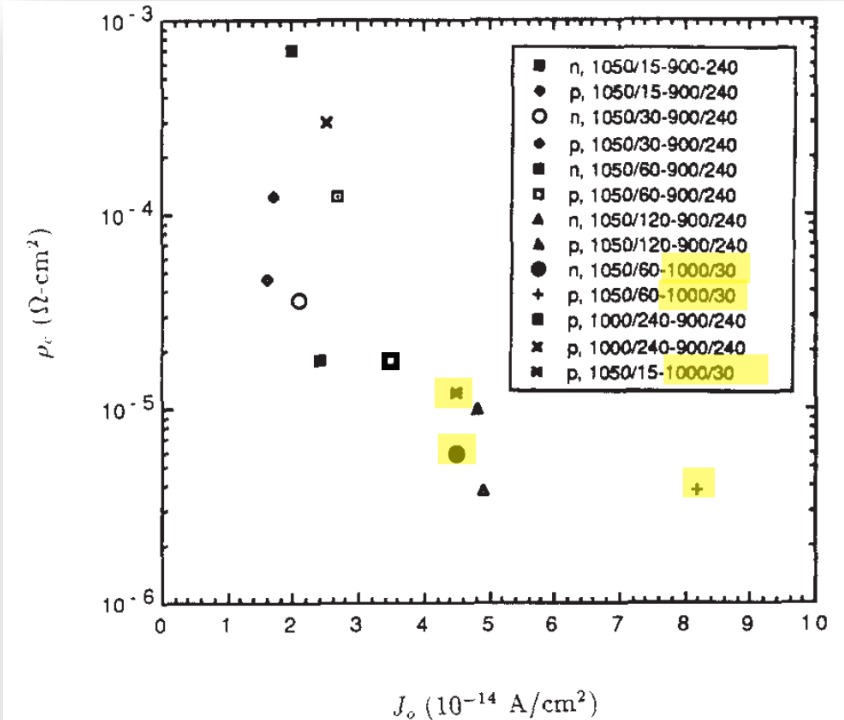
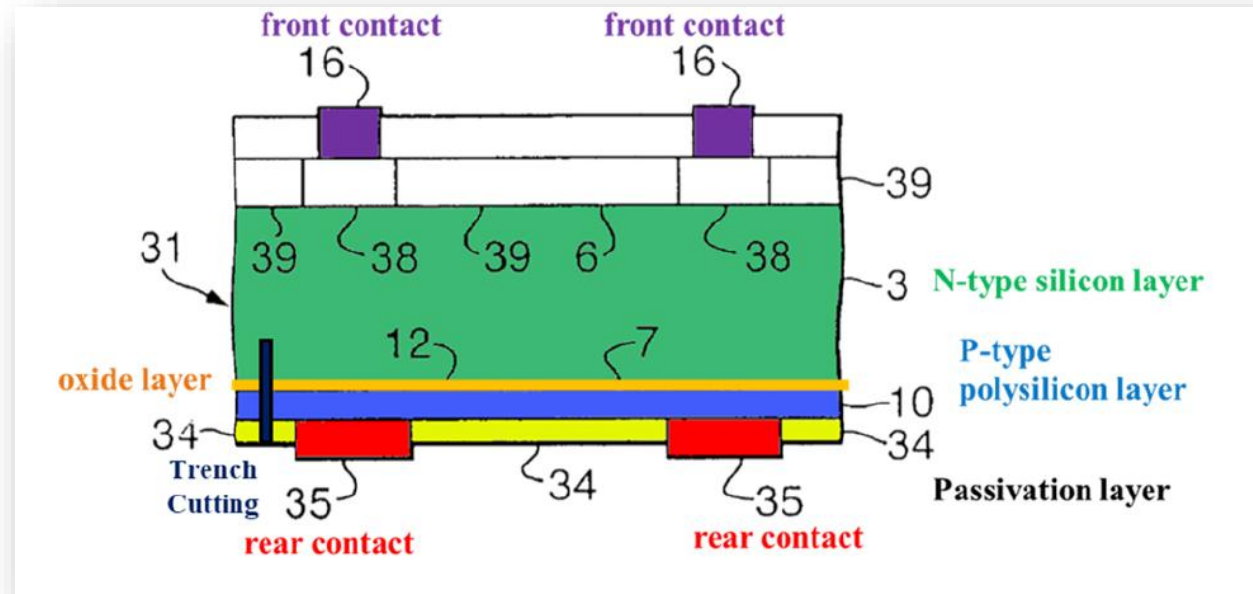


Figure 6: ρ_c - J_o of this work.

Arguments Against Implementing Sheats' Trench



Applicable to:

- IPR2024-01203 Ground II (Froitzheim, Gan, and Sheats);
- IPR2024-01203 Ground IV (Froitzheim, Borden-575, and Sheats).

The Proposed Froitzheim-Gan-Sheats Combination
(illustrated in IPR2024-01203, Paper 3-Petition, 61;
see also id. at 78 (illustrating the proposed Froitzheim-Borden-575-Sheats Combination))

Edge Isolation as Motivation to Combine

Second, a POSITA would have been motivated to combine Froitzheim, Gan, and Sheats. It was well known that solar cells could short circuit, and one known way to address short circuits in solar cells was to include a trench near the edge of the cell. *E.g.*, Ex.1063-Houser, 1739; Ex.1065-Mason, 6:11-7:16; Ex.1066-

215. I understand that during prosecution of the '516 patent, the applicant did not dispute that Sheats teaches claim 5. In particular, on December 24, 2009, the Examiner found that Sheats teaches a solar cell having an **isolation trench 516**, which creates “edge isolation which prevents short circuits on the outside walls of the device.” Ex. 1002-USP516FH, 81-82. I also understand that the applicant’s response on March 19, 2010 was silent regarding Sheats’ disclosure. Ex. 1002-USP516FH, 112.

216. A person of ordinary skill in the art would have incorporated an **isolation trench** to the combined structure of Froitzheim (back-junction solar cell) and Gan (polysilicon emitter and oxide layer), as shown in the modified Figure 3 of Froitzheim below. The figure below shows an **isolation trench** in the combined

- Left: IPR2024-01203, Paper 3-Petition, 62;
- Right: IPR2024-01203, Ex 1003-Holman Dec., ¶¶ 215-16 (partial) (cited in Paper 3, 61-62).

Froitzheim Already Has Edge Isolation

[0047] If required after the formation of the n+ doped layer, a separation at the edge of the wafer may be performed, e.g. in a plasma.

19 A So Paragraph 47 of Froitzheim describes
20 what is generally referred to as edge isolation.
21 And it's a method to make sure that there aren't
22 any shunts, which is the word we use for
1 electrical shorts, in the positive and negative --
2 positive and negative regions or P-type and N-type
3 regions inadvertently touch each other. And
4 Froitzheim is describing a method to make sure
5 that that doesn't happen, your edge isolation.

- Top: Ex. 1004-Froitzheim, ¶ [0047];
- Bottom: Ex. 2029-Holman Dep. Tr., 154:19-158:5;

(both cited in IPR2024-01203, Paper 29-POR, 43).

Froitzheim's Plasma Etching Is Common and Effective

14 Q The last word of Paragraph 47 is plasma.

15 Is this referring to plasma etching?

16 A I think that that is likely. That is how

17 I read it. Removal of material via plasma are

18 commonly called etching. This is one way to do

19 edge isolation, and that's why Froitzheim

20 introduces it with a e.g., for example.

- Top left: Ex. 2029-Holman Dep. Tr., 159:14-20;
- Bottom left: Ex. 1063-Houser, Abstract;
- Bottom right: Ex. 1066-Wenham, 7:38-41;

(all cited in IPR2024-01203, Paper 29, 43-44).

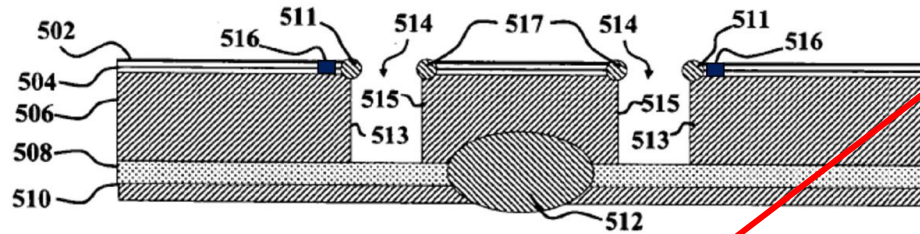
ABSTRACT: In most industrial type solar cell processes the edge isolation is an important step. After most emitter diffusion techniques, especially the POCl_3 diffusion, the front contact is connected with the back contact through the emitter around the edge of the solar cell. As a common technique in industry this shunt is removed by plasma etching of the wafer stack. Other techniques which were investigated are: the grinding of the wafer edge with sandpaper, the cutting of isolation trenches with a wafer dicing saw and the laser separation by inserting trenches, the latter two techniques applied on both sides of the wafer. All these technologies are compared concerning their impact on the solar cell performance of industrial type screen printed solar cells. Using IV measurement (illuminated and dark), laser beam induce current (LBIC) and lock-in thermography it is shown that isolation by laser still suffers from too low fill factors and sawing, grinding, or plasma etching are preferable. A good correlation between decreasing shunt resistance and increasing amount of detected shunts using in-lock thermography or LBIC is found.

Keywords: Edge Isolation - 1: Shunts - 2: Laser Processing - 3

Finally, plasma etched edge isolation can be carried out by coin stacking the solar cells in the plasma system. This is the technique believed to be used very effectively by several commercial enterprises. 40

Sheats' Trench Isolates Edges Between Solar Cells

As the Examiner found and the applicant did not dispute, Sheats teaches a solar cell having “an **isolation trench 516**” “formed through the transparent conductive layer [front contact] and the active layer [emitter/substrate].”



Ex.1012-Sheats, [0003]-[0004], [0058]-[0059], **Fig.5D**; Ex.1002-FH516, 81-82, 112. Ex.1003-Decl., ¶¶214-215.

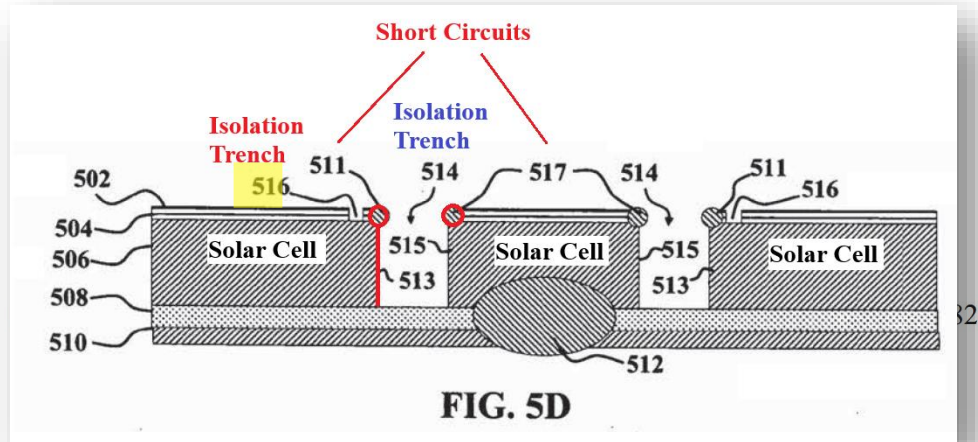
A POSITA would have been motivated to modify Froitzheim to include a **trench cutting** through the dielectric layer and the P-type polysilicon emitter and into a portion of the N-type silicon substrate on the backside of the solar cell with a reasonable expectation of success to result in the following solar cell:

- Left: IPR2024-01203, Paper 3-Petition, 60-61;
- Right: Ex. 2029-Holman Dep. Tr., 240:1-18 (quoted in IPR2024-01203, Paper 29-POR, 48).

1 Q **Figure 5D** shows three rectangular blocks
2 listed on top of Layers 508 and 510. Right?
3 A Yes.
4 Q And the isolation trench 516 is
5 illustrated in two of those three rectangular
6 blocks. Right?
7 A That is correct.
8 Q Is it accurate to say that those three
9 rectangular blocks represent three solar cells?
10 A I am turning to Sheats. Just give me one
11 moment.
12 (Exhibit 1012, previously marked, not
13 attached.)
14 A Yes, it would be appropriate to call each
15 of the blocks a solar cell, and more particularly
16 the layer identified as 504 is the intended
17 absorber layer of the solar cell, going back to
18 our previous discussion.

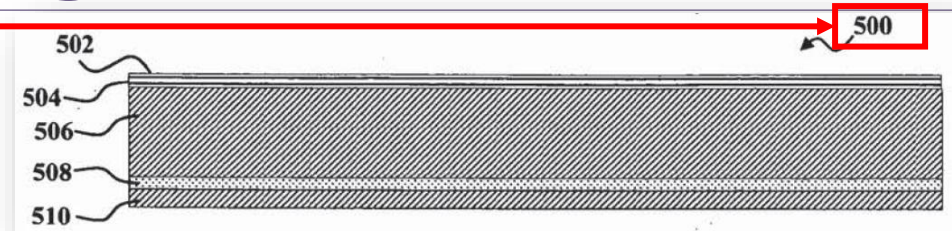
Sheats' Trench Isolates Edges Between Solar Cells

As the Examiner found and the applicant did not dispute, Sheats teaches a solar cell having “an isolation trench 516” “formed through the transparent conductive layer [front contact] and the active layer [emitter/substrate].”



A POSTA would have been motivated to modify Frotzheim to include a **trench cutting** through the dielectric layer and the P-type polysilicon emitter and into a portion of the N-type silicon substrate on the backside of the solar cell with a reasonable expectation of success to result in the following solar cell:

- Bottom Layer: IPR2024-01203, Paper 3-Petition, 60-61;
- Top Layer: Ex. 1012-Sheats, Fig. 5D (annotated in IPR2024-01203, Paper 29-POR, 49).



[0059] The process of forming the isolation trench may cause electrical short-circuits 511, 517 between the transparent conductive layer 502 and the bottom electrode 506. To electrically isolate undesirable short circuits 511 formed on an outside wall 513 of the trench 514 an isolation trench 516 is formed through the transparent conductive layer and the active layer to the bottom electrode 506 as shown in FIG. 5D. The isolation trench 516 surrounds the closed-loop trench 514 and electrically isolates the short circuits 511 on the outside wall 513 of the trench from the rest of the structure 500. A laser scribing process may form the isolation trench 516. A lesser thickness of material being scribed reduces the likelihood of undesired short circuits resulting from formation of the isolation trench 516.

- Top: Ex. 1012, Fig. 5A (cited in IPR2024-1203, Paper 29, 26)
- Bottom: Ex. 1012, ¶ [0059] (quoted in IPR2024-01203, Paper 29, 48-49)

Arguments Against the Limitations of Claim 12

12. The solar cell of claim 9 wherein the second metal contact comprises silver **formed over** a layer of silicon dioxide.

IPR2024-01203, Ex. 1001-The '516 Patent, Claim 12
(quoted in IPR2024-01203, Paper 29-POR, 37)

Applicable to:

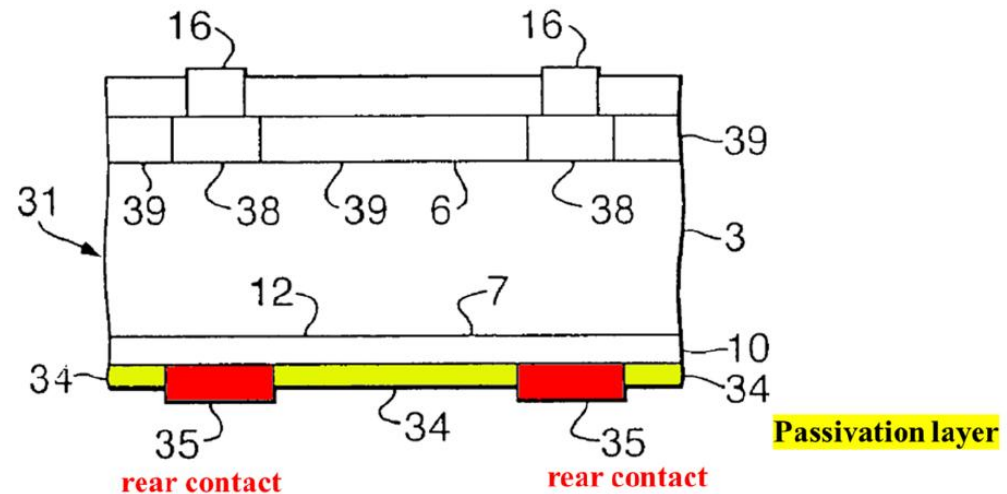
- IPR2024-01203 Ground I (Froitzheim and Gan);
- IPR2024-01203 Ground III (Froitzheim and Borden-575).

Froitzheim's Screen Printing

5 [0033] Reference is made to Figure 3 showing a second embodiment of a solar cell 31 according to the invention. Cell 31 differs from cell 1 of Figure 1 in that the rear contacts 35 are arranged in a finger structure covering only part of the rear side, e.g. similar to that of Figure 2. A typical coverage is in the range of 10-40% of the rear surface. Between the fingers a passivation layer 34 is arranged, for which the same type of layers can be used as for the front side. If the cell is suitably arranged for operation such that reflected or diffracted light is received at the rear side not facing the sun, additional photocurrent can be created by photons absorbed predominantly in the body layer 3 from the rear side.

10 Q. After firing through does the metal completely
11 etch through the anti-reflection or passivation coating?
12 A. Yes.

- Top: Ex. 1004-Froitzheim, ¶ [0033] (cited in IPR2024-01203, Paper 29-POR, 38);
- Bottom left: Ex. 1075-Ruby Dep. Tr., 118:10-12 (cited in IPR2024-01203, Paper 40-Sur-Reply, 11);
- Bottom right: Ex. 1004-Froitzheim, Fig. 3 (annotated in IPR2024-01203, Paper 3-Petition, 31 (discussing claim 12)).



Argument Against Metal Paste Residue

8 Most of the paste resides on top of or
9 over the antireflection coating. But in the
10 fire-through process some of -- some of it will
11 reach through the antireflection coating and touch
12 the wafer surface, thereby electrically connecting
13 the wafer to the paste through the antireflection
14 coating. But the majority of the antireflection
15 coating between the paste or metal contact and the
16 wafer will be intact.

62. The metallic top contacts are necessary to collect the current generated by a solar cell. “Busbars” are connected directly to the external metal ribbons in a solar panel, while “gridline-fingers” are fine areas of metallization which collect current for delivery to the busbars. A tradeoff is made by having sufficient metal coverage to reduce series resistance without shading too much of the cell, which reduces the capture of sunlight and, therefore, reduces current.

[0028] At the front side 6, screen-printed front side contacts 16 are provided in electrical connection with the n-type silicon body layer. The front side contacts form part of a finger structure 19 such as sketched in top view in Figure 2 covering typically around 10% of the front service when screen printed contacts are used. The electrical connection is provided via a shallow n+ doped layer 17 on the front side 6, i.e. between the front contact and the n-type silicon body layer.

...

[0049] The squeegee paste for rear side contacts can contain silver particles, filler, oxides, and also an amount of Aluminium. It will be understood that at firing the paste in order to make electrical contact with the p region, a thin alloy might be formed at the interface between the p-doped region and the contact, but that the p-doped region itself towards the p/n junction is still a non-alloyed p-doped region. The front side contact is also suitably produced by screen printing and firing.

- Top left: Ex. 2029-Holman Dep. Tr., 85:8-16 (cited in IPR2024-01203, Paper 37-Reply, 15-16);
- Top right: Ex. 2027-Ruby Decl., ¶ 62 (cited in IPR2024-01203, Paper 40-Sur-Reply, 12);
- Bottom: Ex. 1004-Froitzheim, ¶¶ [0028, 49] (cited in IPR2024-01203, Paper 40, 11-12).

Importing Process Limitation to Product Claim Is Improper

Hazani argues that the “chemically engraved” claims are product-by-process claims. We agree with the respondents, however, that those claims are best characterized as pure product claims, since the “chemically engraved” limitation, read in context, describes the product more by its structure than by the process used to obtain it. See *In re Moore*, 439 F.2d 1232, 1236, 58 C.C.P.A. 1042, 169 USPQ 236, 239 (1971); *In re Garner*, 412 F.2d 276, 278–79, 56 C.C.P.A. 1289, 162 USPQ 221, 223 (1969). As such, the claims are anticipated, because the claimed products are found in the prior art.

Hazani v. U.S. Int’l Trade Comm’n, 126 F.3d 1473, 1479 (Fed. Cir. 1997)

[4] The method of manufacture, even when cited as advantageous, does not of itself convert product claims into claims limited to a particular process. We agree with the district court that the word “integral” describes the relationship between the elastomeric layers, not the means of joining them. This word did not limit the claim to the manufacturing process set forth in the specification. A novel product that meets the criteria of patentability is not limited to the process by which it was made. See 3 Donald S. Chisum, *Chisum* *1373 on Patents § 8.05, at 8–79 (2000) and cases cited therein.

Vanguard Prods. Co. v. Parker Hannifin Corp., 234 F.3d 1370, 1372–73 (Fed. Cir. 2000)

[8] In the specification, 3M clearly acted as its own lexicographer, and the definition provided requires only that the “two or more embossing patterns” be “superimposed.” ‘930 patent, col. 2, ll. 1–2. Despite Avery’s arguments to the contrary, the use of “superimposed” in this definition neither transforms claim 1 into a product-by-process claim nor even limits the scope of the claim to a serial method of manufacture; it describes only the structural relationship between the embossing patterns. See *Webster’s Third New International Dictionary* 2294 (1993) (defining “superimposed” as “layered”). Furthermore, even words of limitation that can connote with equal force a structural characteristic of the product or a process of manufacture are commonly and by default interpreted in their structural sense, unless the patentee has demonstrated otherwise. See *Hazani v. United States Int’l Trade Comm’n*, 126 F.3d 1473, 1479 (Fed. Cir. 1997) (concluding that “chemically engraved” was *1372 not a process term); *Vanguard Prods. Co. v. Parker Hannifin Corp.*, 234 F.3d 1370, 1372 (Fed. Cir. 2000) (holding that the claim term “integral” describes a structural relation, not the particular manufacturing process related in the specification); cf. *id.* (“A novel product that meets the criteria of patentability is not limited to the process by which it was made.” (citing 3 Donald S. Chisum, *Chisum on Patents* § 8.05, at 8–79 (2000))).

3M Innovative Props. Co. v. Avery Dennison Corp., 350 F.3d 1365, 1371 (Fed. Cir. 2003)

[26] [27] Before we conclude our analysis of the intrinsic evidence, we note that in order to read a process limitation into a product claim, it must meet one more criterion. Generally, “[a] novel product that meets the criteria of patentability is not limited to the process by which it was made.” *Vanguard Prods. Corp. v. Parker Hannifin Corp.*, 234 F.3d 1370, 1372–73 (Fed. Cir. 2000). “However, process steps can be treated as part of a product claim if the patentee has made clear that the process steps are an essential part of the claimed invention.” *Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1375 (Fed. Cir. 2007). For the same reasons that the statements relied upon by the district court do not show that the patentee clearly and unmistakably disavowed claim scope, they also do not make clear that the repeated desmear process is “an essential part” of the claimed electrical device having a tooth structure. *Id.* Far from being essential, the statements from the intrinsic evidence merely indicate a preference for using Probelec XB 7081 and include comparisons with the prior art techniques. Because the patentee has not “made clear” that the repeated desmear process is “an essential part of the claimed invention,” *id.*, it was improper for the district court to read this process limitation into the product claims for this additional reason.

Cont’l Cirs. LLC v. Intel Corp., 915 F.3d 788, 799 (Fed. Cir. 2019)