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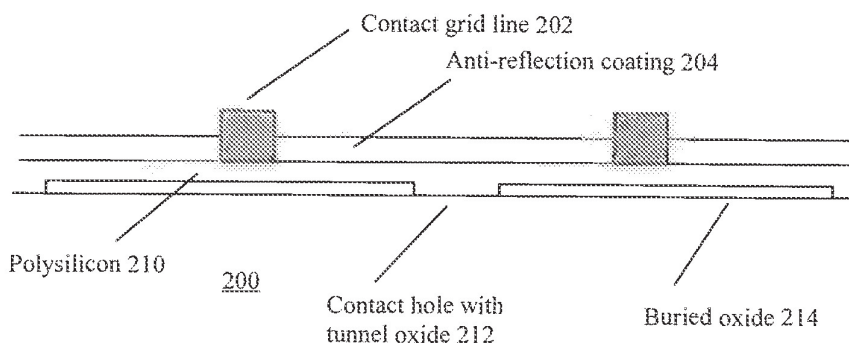


FIG. 2

(57) **Abstract:** The present invention relates to methods and apparatuses for providing a buried insulator isolation for solar cell contacts. According to certain aspects, the invention places a buried oxide under the emitter of a polysilicon emitter solar cell. The oxide provides an excellent passivation layer over most of the surface. Holes in the oxide provide contact areas, increasing the current density to enhance efficiency. The oxide isolates the contacts from the substrate, achieving the advantage of a selective emitter structure without requiring deep diffusions. The oxide further enables use of screen printing on advanced shallow emitter cells. Positioning of the grid lines close to the openings also enables use of a very thin emitter to maximize blue response.

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BURIED INSULATOR ISOLATION FOR SOLAR CELL CONTACTS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority to U.S. Prov. Appln. No. 61/023,354, the contents of which are incorporated herein by reference in their entirety.

FIELD OF THE INVENTION

[0002] The present invention relates to forming contacts in a semiconductor device, and more particularly to methods and apparatuses for providing a buried insulator isolation for polysilicon emitter solar cell contacts.

BACKGROUND

[0003] To obtain high efficiency in silicon solar cells, it is considered advantageous to eliminate surface recombination. Such recombination comes from both unpassivated surfaces and from metal contacts. A measure of recombination is the surface recombination velocity (SRV), which is the rate of minority carrier recombination at the surface. For a reference value, <100 cm/sec provides a well passivated surface needed for a high efficiency cells. By contrast, a metal contact will have an SRV of 10^7 cm/sec, five orders of magnitude higher. If the metal covers 3% of the surface, then the effective surface recombination velocity is 3×10^5 cm/sec, more than 3 orders of magnitude larger than desired. Therefore, contact passivation is essential.

[0004] One well known method to isolate the contacts from the bulk is to use a selective emitter, shown in FIG. 1. As shown in FIG. 1, the area away from the contacts 102 has a shallow emitter diffusion 106 (n-type, typically with Phosphorous doping, on a p-type substrate, for example). The shallow emitter 106 provides good blue response, as blue photons are absorbed near the surface. This emitter might be 0.3 to 0.5 μm thick. On the

other hand, deep diffusions 108 – 2-3 μm thick – are placed under the contacts. These provide isolation so that the high recombination contact surfaces do not affect the cell performance. However, such structures are difficult to form as they require aligned patterning of the contact holes and the metal lines, as well as a several hour diffusion to obtain such a deep junction. Therefore, selective emitters are rarely used in commercial solar cells.

[0005] Another method to passivate contacts is to place a thin tunnel oxide – typically 15Å thick – under the metal contacts. Such types of contacts are also well known, and have been used commercially by Schott solar to manufacture MIS solar cells. However, such solar cells have not been commercially introduced, possibly because of the difficulty of reliably forming a thin tunnel oxide.

[0006] Therefore, there remains a need in the art for a commercially feasible method and apparatus for providing contact passivation in a solar cell.

SUMMARY

[0007] The present invention relates to methods and apparatuses for providing a buried insulator isolation for solar cell contacts. According to certain aspects, the invention places a buried oxide under the emitter of a polysilicon emitter solar cell. The oxide provides an excellent passivation layer over most of the surface. Holes in the oxide provide contact areas, increasing the current density to enhance efficiency. The oxide isolates the contacts from the substrate, achieving the advantage of a selective emitter structure without requiring deep diffusions. The oxide further enables use of screen printing on advanced shallow emitter cells. Positioning of the grid lines close to the openings also enables use of a very thin emitter to maximize blue response.

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[0008] In furtherance of these and other aspects, a solar cell according to embodiments of the invention includes an emitter layer formed on a semiconductor substrate; and an insulating layer between the emitter layer and a surface of the substrate, the insulating layer being patterned to include contact holes that allow current flow therethrough.

[0009] In additional furtherance of these and other aspects, a method of fabricating a solar cell according to embodiments of the invention includes forming an insulating layer on a surface of a semiconductor substrate; patterning contact holes in the insulating layer that allow current flow therethrough; and forming an emitter layer on the insulating layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] These and other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures, wherein:

[0011] FIG. 1 shows a prior art selective emitter cell.

[0012] FIG. 2 shows a buried oxide cell structure according to embodiments of the invention.

[0013] FIG. 3 shows aspects of the operation of a buried oxide cell with an offset contact structure according to embodiments of the invention.

[0014] FIG. 4 is a flowchart showing an example buried oxide cell process flow according to embodiments of the invention.

DETAILED DESCRIPTION

[0015] The present invention will now be described in detail with reference to the drawings, which are provided as illustrative examples of the invention so as to enable those

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skilled in the art to practice the invention. Notably, the figures and examples below are not meant to limit the scope of the present invention to a single embodiment, but other embodiments are possible by way of interchange of some or all of the described or illustrated elements. Moreover, where certain elements of the present invention can be partially or fully implemented using known components, only those portions of such known components that are necessary for an understanding of the present invention will be described, and detailed descriptions of other portions of such known components will be omitted so as not to obscure the invention. In the present specification, an embodiment showing a singular component should not be considered limiting; rather, the invention is intended to encompass other embodiments including a plurality of the same component, and vice-versa, unless explicitly stated otherwise herein. Moreover, applicants do not intend for any term in the specification or claims to be ascribed an uncommon or special meaning unless explicitly set forth as such. Further, the present invention encompasses present and future known equivalents to the known components referred to herein by way of illustration.

[0016] In general, the invention provides a buried oxide under the emitter of a polysilicon emitter solar cell. The oxide provides an excellent passivation layer over most of the surface. Holes in the oxide provide contact areas, increasing the current density to enhance efficiency. The oxide isolates the contacts from the substrate, achieving the advantage of a selective emitter structure without requiring deep diffusions.

[0017] The present inventors recognize that a point contact solar cell provides improved efficiency. This is because the current flow is concentrated into a small region, providing a higher current density. The open circuit voltage V_{OC} is given by the equation:

$$V_{OC} = kT/q \ln (J_L/J_0 + 1)$$

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[0018] where k is Boltzmann's constant, T the temperature, q the electron charge, J_L the short circuit current density, and J_0 the diode saturation current. Therefore, an increase in short circuit current density provides an increase in voltage and, hence, efficiency.

[0019] FIG. 2 shows an example cell structure in accordance with embodiments of the invention. As shown in FIG. 2, the cell structure includes an insulating (e.g. oxide) layer 214 under the doped region 210 and the contact 202. This insulating layer 214 isolates the contact 202 from the substrate 200. According to some aspects of the invention, if the insulating layer 214 is made using a material that passivates silicon, such as thermal SiO_2 , then the solar cell surface has very good passivation and a low surface recombination velocity, both in the field region 210 and under the contacts 202. Contact holes 212 are provided in the insulating layer 212 to allow for photocurrent flow. In embodiments described in more detail below, contact holes 212 include a tunnel oxide. However, this is not necessary in all embodiments.

[0020] In embodiments, substrate 200 is comprised of silicon, and is low-doped with p- or n-type impurities. Many other substrate materials can be used and this and many other methods for obtaining a desired polarity concentration and type are possible, as will be appreciated by those skilled in the art. It should be noted that the term contact hole should be construed broadly so as to relate to many types of openings through insulating layer 214 and many types of solar cell contacts. For example, the holes can provide for point contacts or they can provide for grid line contacts. Those skilled in the art of solar cell contacts will appreciate how the teachings of the invention can be applied to these and other various types of contacts and openings.

[0021] In embodiments such as shown in FIG. 2, the contacts 202 are positioned approximately in the middle between two holes 212. Photocurrent flows through contact

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holes 212 patterned in the oxide layer 214. This concentrates the current flow, providing an increased current density at the junction. The collected current then flows laterally to the contacts 202. Typical dimensions of the openings 212 can be 20 to 200 μm and spacing between openings 212 can be 1-5 mm. The ratio of the spacing to opening width provides the concentration, which is limited by series resistance due to current crowding at the contact holes. Concentration ratios on the order of 5 to 20 are typical. The openings can be lines parallel to the contact grid lines, or holes of shape such as rectangles or circles. Larger openings can be patterned without lithography, using screen printing. Laser ablation can also be used.

[0022] In embodiments, the doped region 210 is formed using polysilicon, which may be deposited at a temperature on the order of 630°C and is in-situ doped. A short anneal at 1050°C for 30 seconds after deposition activates the dopants. As mentioned above, in some embodiments a thin tunnel oxide may be included between the substrate 200 and the polysilicon 210 in the contact holes 212. This oxide – typically 8 to 15Å thick – provides passivation between the substrate and the polysilicon, while allowing for tunnel current flow.

[0023] In another embodiment, the contact lines 202 are not centered with respect to the holes, but offset so as to be closer to respective holes 212, as shown in FIG. 3. Now the current path from the contact holes 212 to the contact grid lines 202 is shortened. This path may be typically 50 to 200 μm long, so that the metal grid lines 202 are well isolated from the contact holes 212, but the series resistance between the contact and the hole is low because of the short path length. This enables use of a thinner emitter layer 210 – on the order of 500 to 1000Å thick – reducing absorption of blue light in the emitter and improving blue response.

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[0024] It should be noted that, according to aspects of the invention, the contact metal 202 is blocked from reaching the substrate 200 by the buried oxide 214. This enables contacting to the thin emitter without use of a sophisticated contact process.

[0025] The buried oxide is preferably relatively thin so that it does not provide an optical element that reduces light transmission into the cell. A thickness of 100 to 150Å is adequate, although thinner layers may be used. A thickness >20Å is desirable, as thinner layers may support leakage through tunnel currents. This thickness provides some contrast, so that the contact hole position can be identified for alignment of the grid lines, but has a negligible affect on light transmission into the cell.

[0026] FIG. 4 shows an example embodiment of the process flow for fabricating a solar cell structure according to aspects of the invention. First in step S402, the wafer is cleaned and the buried oxide formed, using a process such as thermal oxidation or RadOx® from Applied Materials. Next in step S404, the contact holes are formed. For example, an etch mask layer is screen printed on the cell and the buried oxide is etched in HF. The resist is then removed. The wafer is then cleaned and, in one embodiment shown in FIG. 4, a tunnel oxide is grown in the contact holes using a process such as ISSG or Radox in the step S406. Another embodiment does not use the tunnel oxide, and processing advances directly from step S404 to S408.

[0027] In step S408, the doped polysilicon is then deposited. On p-type substrates, this is 500 to 1000Å of n-type poly, doped with either As or P for example. On n-type substrates, the layer is doped with B for example. In step S410, the antireflection coating is also deposited, which may be a 750Å layer of silicon nitride. In the preferred embodiment, in step S412 the wafer is then annealed at 450°C for 30 minutes in forming gas to provide

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hydrogen passivation. However, this is not necessary in all embodiments, and processing may advance directly from step S410 to S414.

[0028] In step S414, holes are then patterned in the AR coating using screen printing and etching, for example. Plating may be used to form Ni/Ag contacts, which are then annealed. In another embodiment, silver paste is screen printed on the AR coating and fired in, with the buried oxide blocking the fired paste from reaching the substrate.

[0029] The described structure may be formed on the front of the cell. In an alternate embodiment, it is formed on the back of the cell. This is advantageous if the front of the cell has a texture, as the structure can be made on a planar surface. The textured surface exposes the $\langle 111 \rangle$ plane which has a higher atom density than the $\langle 100 \rangle$ plane and also has 1.7 times of the area of planar surface. The textured surface has a higher SRV than planar surface and is more difficult to passivate. It is desirable to form such structures on the planar surface on the back of the cell.

[0030] The opposite side of the cell also requires a contact structure. In one embodiment, aluminum is deposited on the back and fired in using a laser to form laser fired contacts, which are well known in the prior art. In another embodiment, the front structure is repeated on the back, using polysilicon with the same doping type as the substrate.

[0031] It should be noted that the cell operates in forward bias. For example, if the poly layer is p-type and the substrate is n-type, then the poly layer is positive with respect to the substrate. Therefore, the surface will be accumulated (high electron concentration). This provides a means to passivate the surface, as holes will not be present, and both holes and electrons are needed to recombine at interface traps.

[0032] To operate in inversion, it is necessary to form the dielectric with a fixed charge that provides a threshold voltage shift greater than the cell operating voltage.

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[0033] Note, also, that the buried layer can be made of more than one material. For example, one can form a thin oxide to passivate the surface, followed by a thicker silicon nitride. The nitride can provide charge and hydrogen, and can be an improved barrier to block metal atoms from diffusing from the contacts into the substrate when the contacts are annealed.

[0034] Although the present invention has been particularly described with reference to the preferred embodiments thereof, it should be readily apparent to those of ordinary skill in the art that changes and modifications in the form and details may be made without departing from the spirit and scope of the invention. It is intended that the appended claims encompass such changes and modifications.

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WHAT IS CLAIMED IS:

1. A solar cell comprising:
an emitter layer formed on a semiconductor substrate; and
an insulating layer between the emitter layer and a surface of the substrate, the insulating layer being patterned to include contact holes that allow current flow therethrough.
2. A solar cell according to claim 1 wherein the insulating layer comprises silicon dioxide.
3. A solar cell according to claim 2 wherein the silicon dioxide is thermally grown.
4. A solar cell according to claim 3 wherein the insulating layer is less than about 20Å thick.
5. A solar cell according to claim 1 wherein the emitter layer comprises doped polysilicon.
6. A solar cell according to claim 1 wherein the contact holes include a tunnel insulator between the emitter layer and the underlying substrate, wherein the tunnel insulator is thin enough to allow current therethrough.
7. A solar cell according to claim 1, further comprising:
a contact structure formed over the emitter layer, the contact structure being offset a non-zero lateral distance from the contact holes with respect to the surface of the substrate.

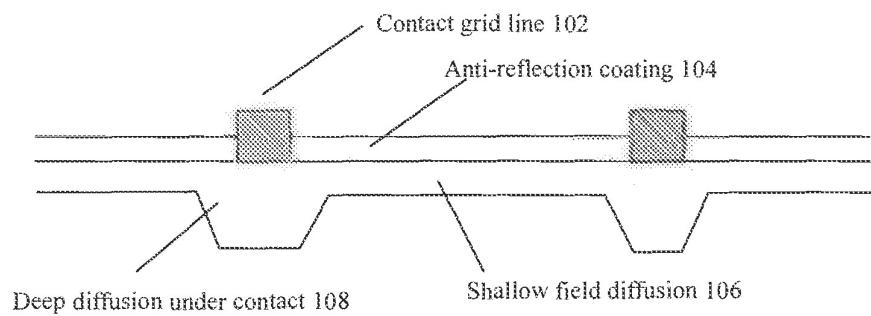
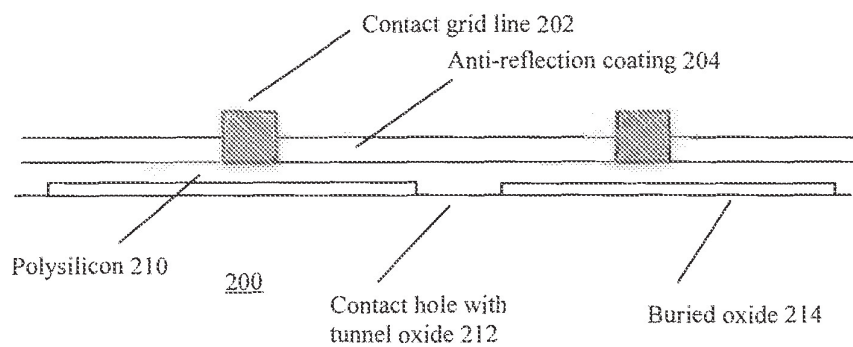
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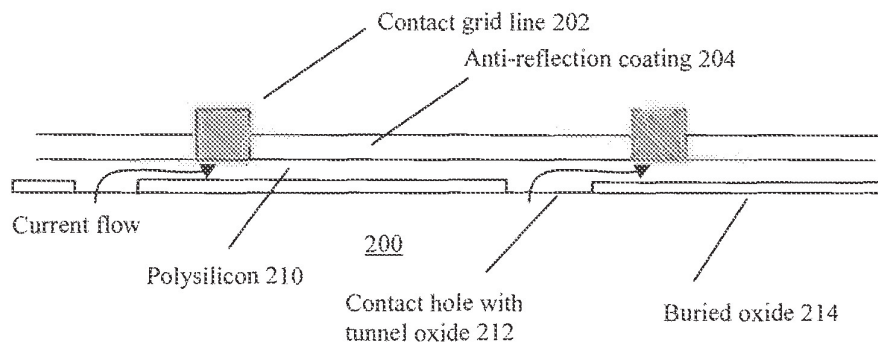
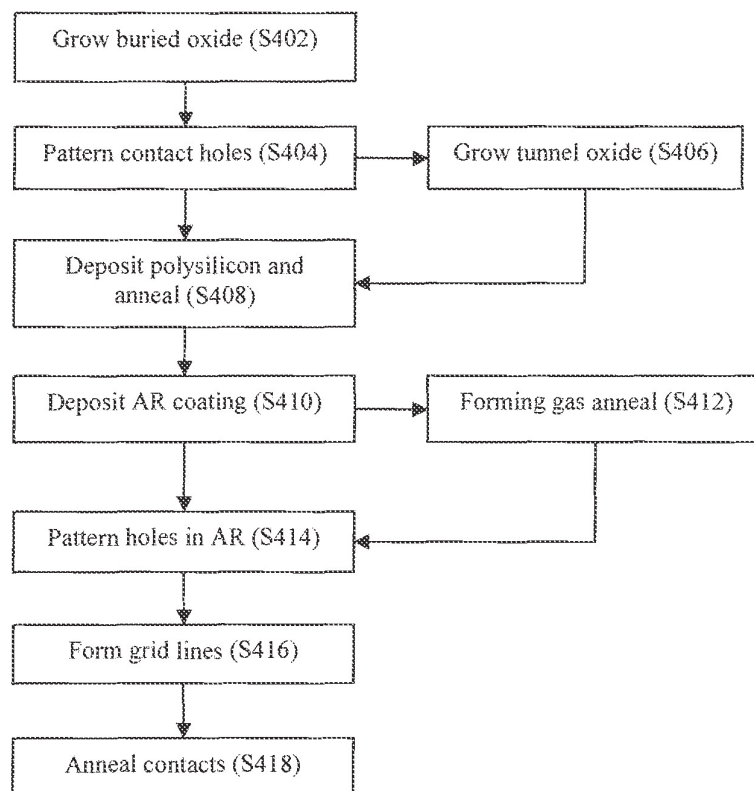
8. A method of fabricating a solar cell comprising:
- forming an insulating layer on a surface of a semiconductor substrate;
 - patterning contact holes in the insulating layer that allow current flow therethrough;
 - and
 - forming an emitter layer on the insulating layer.
9. A method according to claim 8 wherein the insulating layer comprises silicon dioxide, and wherein the step of forming the insulating layer includes performing thermal oxidation.
10. A method according to claim 9 wherein the insulating layer is less than about 20Å thick.
11. A method according to claim 9, wherein the step of forming the emitter layer comprises depositing a doped polysilicon layer.
12. A method according to claim 9, further comprising forming a tunnel insulator in the contact holes between the emitter layer and the underlying substrate, wherein the tunnel insulator is thin enough to allow current therethrough.
13. A method according to claim 9, further comprising:
- forming a contact structure over the emitter layer.
14. A method according to claim 13, wherein the step of forming the contact structure includes offsetting the contact structure a non-zero lateral distance from the contact holes with respect to the surface of the substrate.

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15. A method according to claim 9, further comprising:

annealing the substrate after the layers have been formed to provide hydrogen passivation.

**FIG. 1 (PRIOR ART)****FIG. 2**

**FIG. 3****FIG. 4**