

Low Cost, high volume production of >22% efficiency silicon solar cells

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ABSTRACT: SunPower is a high volume producer of low cost, high efficiency silicon solar cells and solar panels. This tradition continues with the start-up of high volume production of a new low cost technology that produces 22.4% silicon solar cells and >315W solar panels. This significant increase in silicon solar cell efficiency from 20.6% to 22.4% has resulted from improved patterning techniques. These enable lower series resistance and carrier recombination losses through smaller feature sizes, tighter alignment and a fundamental re-optimization of the cell design. The improvement in module power is the result of several changes made in addition to the improved cell efficiency: use of 165mm diameter semi-square wafers, change to a 96-Cell module format and use of an anti-reflection coating. This paper reports recent progress in the high volume manufacturing, and provides an analysis of the design optimization that achieved these significant improvements in silicon solar cell efficiency and solar panel power.

Keywords: Back Contact, High Efficiency, Silicon

1 BACKGROUND

SunPower's original high efficiency back-contact solar cells were designed for applications such as high concentration [1] or solar powered high altitude airplanes [2], for which high efficiency is more critical than low manufacturing costs. Those cells, which reached 22.7% independently confirmed efficiency under AM1.5 conditions, were manufactured using high lifetime float-zone silicon and processing methods common to the semiconductor industry, including photolithography and double metal layers.

In 2003 SunPower introduced the A-300, a back-contact solar cell with greater than 20% efficiency made with a process suitable for mass production with low cost patterning technologies and a single metal layer [3]. The minimum feature size increased from 5 to 200 microns and the alignment tolerance increased from 2 to 75 microns. This caused the mode of the efficiency distribution to drop from 22.1% to 20.6%.

Since then, SunPower has significantly improved its patterning technology and re-optimized the cell layout and process to minimize the detrimental effects of using low cost patterning. The latest production line, with an annual capacity of 33 MW, is now producing 149 and 155 cm² cells with an efficiency mode of 22.4%. This is higher than the efficiency mode of our original high efficiency 21cm² cells made with expensive, low throughput semiconductor industry type processing and equipment [4].

The efficiency of Sunpower solar panel was also improved. The module size was increased from 72-cell to 96-cell to minimize the non active areas e.g. frames. Further an anti-reflection coating was added to minimize front reflection. The result of these improvements was a total area efficiency of 20.1%, confirmed by Sandia laboratories.

The purpose of this paper is to describe the layout improvements and to analyze the impact of each design parameter on cell efficiency. Using both simulations and cell characterization, we investigate how finger pitch, base diffusion width, diffusion at the perimeter, size of solder pads and busbar design affect the cell efficiency. We also provide additional technical information such as field data of total energy delivery.

2 CELL EFFICIENCY AND CELL DESIGN

The dimensional features of an all back contact solar cell have a significant impact on the efficiency losses as a result of 2-dimensional carrier transport mechanisms. The most important dimensional features in this respect are the contact coverage fraction, the dimensions of the base diffusion and the pitch of the diffusions. The busbars and edge design provide an additional efficiency loss mechanism that is 2-dimensional in nature.

The contact coverage has a detrimental effect on the open circuit voltage. If the contact coverage is high, a heavy or deep diffusion is needed to shield the bulk from the high surface recombination velocity at the silicon/metal interface under the contact openings [5]. Unfortunately, heavy and opaque diffusions have a high emitter saturation density (J_0e) that also negatively affects the open circuit voltage. The only solution is to limit the size of the contact openings as much as possible and to conduct a careful optimization of the back side diffusions.

The effect of the diffusion pitch, defined as the distance between two base diffusions (Figure 1), has a large impact on the internal series resistance. When the pitch is larger than the wafer thickness, as is the case when using low cost patterning technologies, the majority carriers above the emitter (P-diffusion in figure 1) drift laterally and are collected by the base diffusion. The simulated equivalent series resistance caused by lateral transport of majority carriers is shown in figure 2 (curve with square markers).

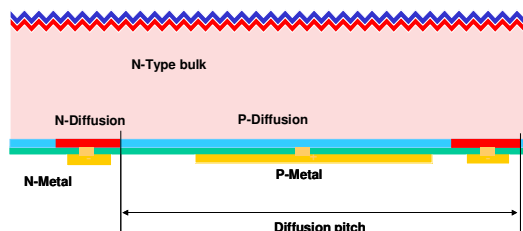


Figure 1: Cross section of SunPower back-contact solar cell (dimensions are not to scale)

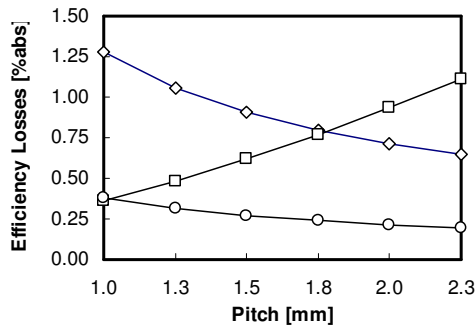


Figure 2: Simulated losses caused by internal series resistance vs. backside diffusion pitch, caused by additional recombination over the base (diamond markers for a full base width; circle markers for a half base width)

While reducing the pitch decreases the internal resistive losses, it also increases recombination losses above the base diffusion. When the width of the base diffusion is larger than the wafer thickness, the minority carriers generated above a base diffusion will diffuse laterally to be collected by the nearest emitter diffusion [6]. This diffusion current is possible only if a gradient of minority carriers is present. This raises the minority carrier concentration above the base diffusions. Figure 3 shows the result of numerical simulations of the average minority carrier concentration above the base diffusion, for carrier concentration corresponding to maximum power. The y-axis is the minority carrier concentration, averaged across the wafer thickness. The x-axis is the horizontal distance from the emitter diffusion. From the profile of figure 3, one can easily compute the additional carrier recombination and the efficiency loss caused by this increase of carrier concentration. Results of those simulations are shown in figure 2 (diamond markers)

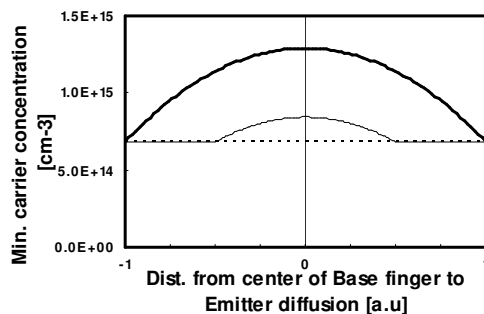


Figure 3: Profile of minority carrier concentration (averaged across wafer thickness) above base diffusion, for a full base width (heavy curve) and half base width (thin curve). $x = -1$ and $x = +1$ represent the left and right boundaries of the base.

In order to limit these losses, the width of the base diffusion must be made as narrow as the printing technology allows and the area coverage of the base diffusion must be kept at a minimum. This unfortunately conflicts with minimizing the series resistance losses generated by the lateral transport of the majority carriers. A compromise must be found to minimize overall losses. The optimum pitch is a trade off between the lateral

resistive losses and the additional recombination over the base diffusion.

Recent progress in our patterning process has allowed us to reduce features sizes and improve layer-to-layer alignment. By reducing the area of the base diffusions, both resistive losses and losses associated with the base diffusion area can be significantly reduced. The thin line in figure 3 is the average minority carrier above the base in the case of a reduction of the base width by a factor of 2. The extra carrier concentration (and hence the extra recombination) is reduced of a factor much larger than 2. Simulation results of the losses versus pitch for this reduced base diffusion area are plotted in Figure 2 (circle markers). The optimum between internal series resistance and recombination losses now lies at a much smaller pitch, and both series resistance and recombination losses are reduced.

The following figures are photoluminescence images of the A-300 and the new design. The dark stripes on the right side figure 4 show increased recombination above the base fingers, which is only minimally detected for our new design, as shown in the left image of figure 4.

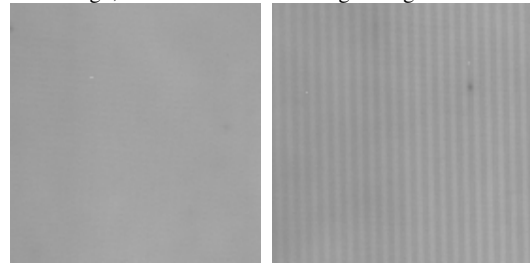


Figure 4: Photoluminescence images demonstrating the significant reduction in recombination as a result of diffusion and layout optimization in the new generation design (left) compared to the A300 (right). Photoluminescence images are courtesy of Thorston Trupke at the University of New South Wales.

Similar loss mechanisms occurs under the busbars and at the wafer edges, where there are large areas of base diffusion. When the minority carrier must travel a long horizontal distance to be collected by the emitter (more than a few mm), the carrier concentration will increase up to the point where carrier generation equals carrier recombination. No current is generated and that part of the cell is, in effect, at open circuit condition. This occurs under the busbars and at the wafer edge and causes a significant drop in cell efficiency.

A re-design of the cell layout has resulted in a significant reduction of our efficiency losses. Simulation of those losses for the old and new design is shown in figure 5.

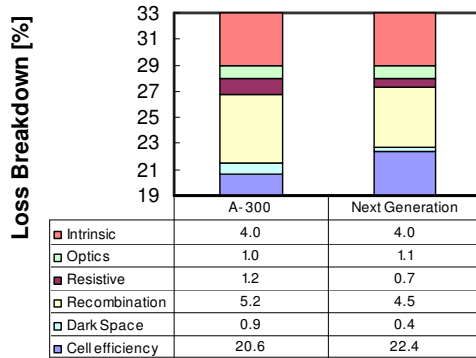


Figure 5: Estimated breakdown of losses and resulting efficiency of our latest generation and the A-300 cells.

The theoretical maximum efficiency is estimated at 33% for a single band-gap semi-conductor at 1-sun AM1.5 illumination [7]. The intrinsic losses, estimated at 4%, include the effect of the non-optimum silicon band-gap and the inevitable Auger and radiative recombination.

In addition to the reduction of the recombination losses associated with the reduction of the base diffusion area, recombination losses have also decreased as a result of the use of thinner silicon (165 microns instead of 195). This thickness reduction, however, has a detrimental effect on the cell internal optics, and optical losses have been increased by an estimated 0.1% efficiency point.

One line of our cell production factory in Laguna, Philippines has been converted to this new generation of cells. Over several hundred thousand wafers have been produced so far. A representative efficiency distribution shown in figure 6 (solid histogram), using data from a full day of production. It has a mode of 22.4%. We are now in the process of installing and ramping production on another four production lines totaling 140MW of capacity. Those new lines will be entirely dedicated to our latest cell technology.

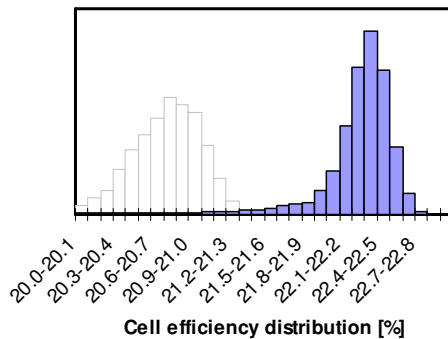


Figure 6: Efficiency Distribution of one day of production of SunPower's latest cell generation (solid histogram) and the A-300 cells (unfilled histogram).

The efficiency distribution of our new design is now better than the efficiency distribution our 1996 production of specialty cells made for Honda for the Solar World Challenge [4] (figure 7), even though those specialty cells were made with low throughput and expensive semi-conductor type processes and equipment,

including photolithography and double metal layer, they did suffer from higher perimeter losses, because the wafer edge was un-passivated (saw-cut from 4" round wafers) and the ratio of the perimeter over area was higher. Perimeter losses from this design was estimated at 1.5% absolute, compared to less than 0.4% for our latest design.

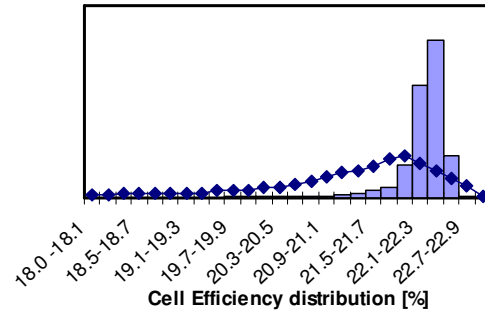


Figure 7: Efficiency Distribution of one day of production of our latest cell generation (histogram) and the entire 1996 production of the specialty cells made for the Solar World Challenge (line).

In 1996, SunPower had not reached the level of process control and characterization that we have today. In 1996, while the efficiency of the best cells was above 23%, the distribution was much wider, spreading from 20 to 23%. Today, the mode of our efficiency distribution is at 22.4%, and 85% of our cells are higher than 22.0%.

3. MODULE EFFICIENCY

In addition to improved cell efficiency, the module efficiency has been improved by using anti-reflection glass and 154cm² wafers cut from 165mm diameter ingot, which increases the packing density of the module.

The use of AR glass has been found to increase efficiency by 2.7% and energy gain by 4%. The energy gain is higher than the efficiency gain because of enhanced off-angle performance which improves the gain for non-normal sun angles and diffuse illumination. A side-to-side comparison of system efficiency of modules made with our next generation cells and modules made with A-300 cells is under way at Arizona State University, at ASU-PTL. A comparison of energy delivery of the two systems is shown in figure 8. Both module strings are made of 72-cell modules, without AR glass. This data shows that even without the extra-boost of the AR glass, our next generation device delivers close to 7% more energy.

SunPower produced a 327.6W 96-cell panel, which corresponds to a total-area (including frame) module efficiency of 20.1%. The cells and module have been entirely fabricated in our production lines on a production process. This efficiency has been independently confirmed by Sandia National Laboratories (Figure 9).

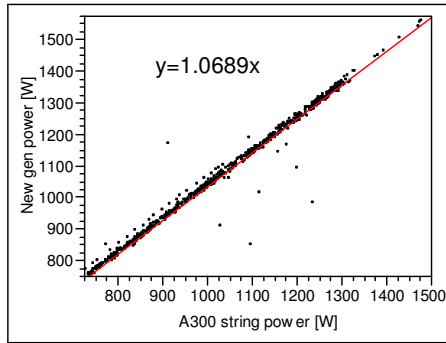


Figure 8: Energy delivery of module strings made with our next generation device (y-axis) vs. A-300 (x-axis).

Photovoltaic Systems Evaluation Laboratory

Sandia National Laboratories, Albuquerque, New Mexico 87185
8/29/07

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File: SUN070827aALL (1276 observations)
Title: SunPower 96 cell AR Module#2
      Michael Quintana; 844-0474      Test Date: 27 Aug 2007
no n/n,AR Coated, 96-Cell C65AR      Item: 2290 Request:708.03
Test: Electrical Performance

////////// Absolute Air Mass = 1.5 //////////

SEC Conditions: 1000 W/m², Cell Temp.= 25°C
ISC(A) Voc(V) Imp(A) Vmp(V) Pmp(W) FF Eff(%) Vmp/Voc Imp/Iscc
6.296 66.099 5.906 55.464 327.59 .787 20.10 .839 .938
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Figure 9: 327.6W 96-cell module, 20.10% total area efficiency as measured by Sandia National Laboratories.

4. CONCLUSIONS

SunPower will continue to scale up its production capacity with a new low cost technology that produces >22% silicon solar cells and 315W solar panels. The cell efficiency improvement has resulted from improved lithography techniques and re-optimization of the back side design. Additional improvements in module efficiency were achieved by using 125mm semi-square wafers cut from a 165mm diameter ingot, by change to a 96-cell module format and by the use of anti-reflection glass.

5. ACKNOWLEDGMENTS

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