

A Simple Method to Control Bipolar Polysilicon Emitter Interfacial Oxide

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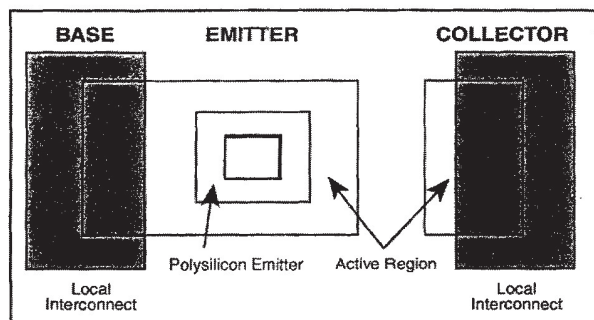
ABSTRACT

Polysilicon emitters are prevalent in today's advanced BiCMOS processes. Electrical and materials analysis have been used to demonstrate the increase in npn current gain, for polysilicon emitters, with an increasing interfacial "oxide" thickness. This interfacial "oxide" thickness has been tailored by the polysilicon push temperature into an LPCVD vertical thermal reactor. The interfacial "oxide" thickness has been shown to affect the npn current gain by modulating the base current without significantly impacting the collector current.

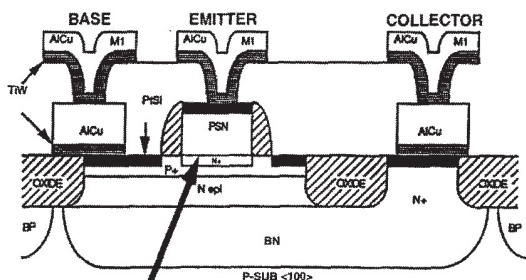
Polysilicon emitters are becoming more prevalent in today's advanced Bipolar/BiCMOS integrated circuit processes. In addition to increasing the packing density they have been shown to exhibit high current gain.^{1,2} In this technology, the interface between the polysilicon and single-crystal silicon plays a crucial role, and it has now been generally accepted in the literature that the interface condition is important for achieving high current gain. There have been reports of difficulty in controlling this interfacial layer, and various solutions have been proposed.^{3,4}

In this paper we present a simple method for modifying the interfacial oxide thickness in a polysilicon emitter technology incorporated in a BiCMOS process. This allows an increase in the bipolar npn transistor current gain without adversely impacting other device parameters. This methodology has been developed and is now utilized in manufacturing for our advanced BiCMOS products.

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Top View



Polysilicon to Monosilicon Interface

Cross Section

Fig. 1. Top and cross-sectional view of the bipolar nonwalled npn transistor.

Experimental

The characterization of the interface formation was done on P<100> 150 mm silicon wafers using an advanced BiCMOS process.⁵ This technology has polysilicon emitters with an emitter arsenic concentration of $2.0 \times 10^{20} \text{ cm}^{-3}$, a boron base concentration of $3.0 \times 10^{18} \text{ cm}^{-3}$ and a phosphorus collector concentration of $1.0 \times 10^{17} \text{ cm}^{-3}$.

The interfacial clean process, prior to polysilicon deposition, consisted of a standard RCA chemistry except that the 50:1 HF dip was performed last. There was no attempt made to intentionally grow an interfacial oxide in the pre-clean. In order to ensure the validity of the experiments, a queue time limit of 2 h was enforced between the interfacial clean and the polysilicon deposition.

The polysilicon deposition was performed by an LPCVD process in an SVG-7000 vertical thermal reactor at 550°C. At this temperature the as-deposited film is amorphous. However, due to the fact that subsequent processing makes this film polycrystalline we also refer to the deposited film as polysilicon.

Associated with this deposition technology is an unavoidable amount of backstreaming of room air that occurs as the wafers are being pushed (loaded) into the furnace. This always results in the formation of some interfacial "oxide." We viewed this backstreaming as an opportunity to grow an intentional "oxide," provided it could be done in a controlled fashion. Extensive experimentation was performed around the polysilicon furnace conditions in order to optimize and control the interfacial "oxide" thickness. To ensure manufacturability, care must be taken to maintain a uniformity of the interfacial "oxide" throughout the polysilicon deposition furnace tube.

In the initial screening experiment the following deposition parameters were varied: nitrogen purge rate during the push (3 vs. 7 lpm), the push rate (5.6 vs. 10.2 cm/min), the sit time in the reactor prior to pumpdown (4 s vs.

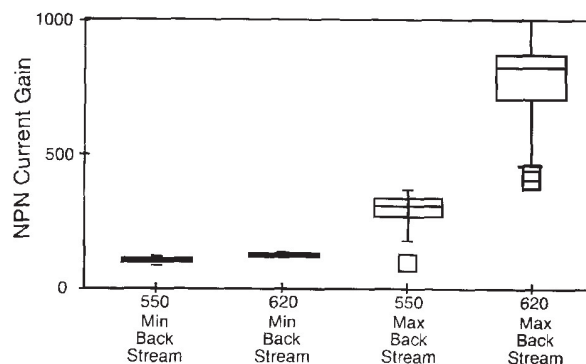


Fig. 2. Effect of minimum and maximum backstreaming conditions at two different push temperatures on npn current gain.

Polysilicon Push Conditions °C HANWHA 1035

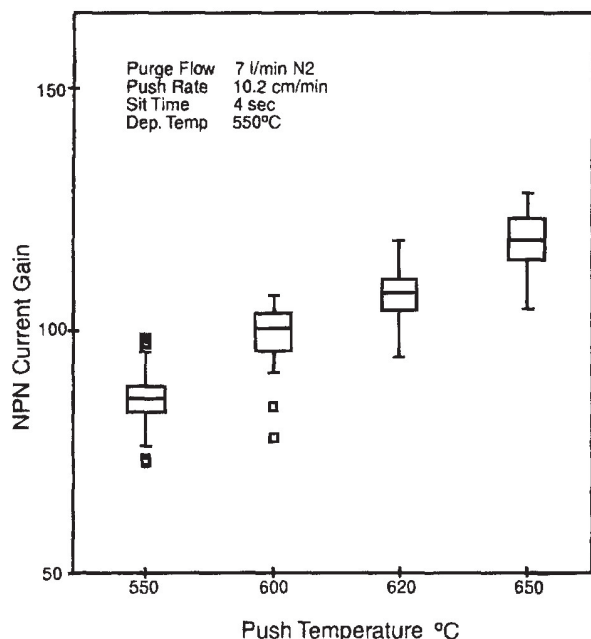


Fig. 3. Effect of increasing push temperature on npn current gain.

20 min), and the push temperature (550–620°C). This allowed us to vary the amount of atmospheric oxygen backstreaming during the push and to vary the push temperature.

For the final set of experiments, the push temperature was varied from 550 to 650°C, while the nitrogen purge rate, push rate and sit time prior to pumpdown were 7 lpm, 10.2 cm/min and 4 s, respectively.

Materials analysis was performed using high resolution transmission electron microscopy (HRTEM) and secondary ion mass spectrometry (SIMS).

Cross-sectional TEM samples of the polysilicon emitter were prepared by mechanical thinning followed by ion-milling at 5 kv and 15° angle. During mechanical thinning, the samples were supported on a tripod polisher and imperial diamond lapping films with diamond particles varying from 15 to 0.5 μm in size were used to polish the samples. A detailed procedure is described elsewhere.⁶ TEM observations were carried out on a Philips CM30 transmission electron microscope operating at 300 kv with the sample oriented along the $\langle 110 \rangle$ zone axis.

The SIMS analysis was done using a Cameca IMS-4F secondary ion mass spectrometer. The profiles (phosphorus, arsenic, and boron) were measured separately and overlaid after acquisition. The $^{11}\text{B}^+$ and $^{75}\text{As}^+$ was monitored from a 60 μm field using 10.5 keV O_2^+ at 37° from normal. High mass resolution was used to discriminate $^{75}\text{As}^+$ from $(^{28}\text{Si}^{+30}\text{Si}^{+16}\text{O})^+$. The $^{31}\text{P}^-$ was monitored also from a 60 μm field using 14.5 keV Cs^+ at 30° from normal. High mass resolution was necessary to discriminate the $^{31}\text{P}^-$ from $(^{30}\text{Si}^{+1}\text{H})^-$.

Results and Discussion

Vertical thermal reactors, by virtue of their design, eliminate many of the sources of oxygen contamination commonly found with horizontal reactors. With horizontal reactors considerable effort is needed to minimize the growth of an interfacial oxide. The challenge with vertical reactors is to grow an interfacial oxide thick enough to achieve the required current gain without sacrificing other device parameters.

The electrical test data presented in this paper is from a bipolar nonwalled npn transistor with a polysilicon emitter that is $2.4 \times 2.4 \mu\text{m}$. The top view and cross sections are shown in Fig. 1.

In the initial screening experiment process recipes were created which resulted in minimum and maximum backstreaming of air. The set of conditions which minimized

backstreaming were 7 l/min N_2 purge flow, 10.2 cm/min push rate and 4 s sit time prior to pumpdown. The set which maximized backstreaming were 3 l/min N_2 purge flow, 5.6 cm/min push rate and 20 min sit time prior to pumpdown. Figure 2 shows the effect of the minimum and maximum backstreaming conditions at two different push temperatures on the bipolar npn current gain. The effect of increasing the push temperature into the reactor was to increase the npn current gain. The effect of increasing the oxygen backstreaming rate was to increase the current gain and its variability. In a follow-up experiment each of the backstreaming parameters was individually varied. While they all increased the npn current gain they also increased its variability. Since control of the npn current gain variability is important, the subsequent results focus on the effect of varying the push temperature only under the minimum backstreaming conditions.

Figure 3 shows the effect of increasing the push temperature on the npn current gain. Under these minimum backstreaming conditions there is an increase in the current gain of approximately 40 points within the range examined without sacrificing variability. Gummel plots of collector and base current vs. emitter-base voltage ($V_{\text{be}} = 0$) were generated. The Gummel plots of individual transistors at the two extremes of push temperatures examined (550 and 650°C) show good bipolar characteristics with no current gain decreases even at low currents (Fig. 4).

Figure 5 shows the collector and base currents as a function of the push temperature. It is interesting to note that within the push temperature range examined the collector current does not appreciably change while the base current

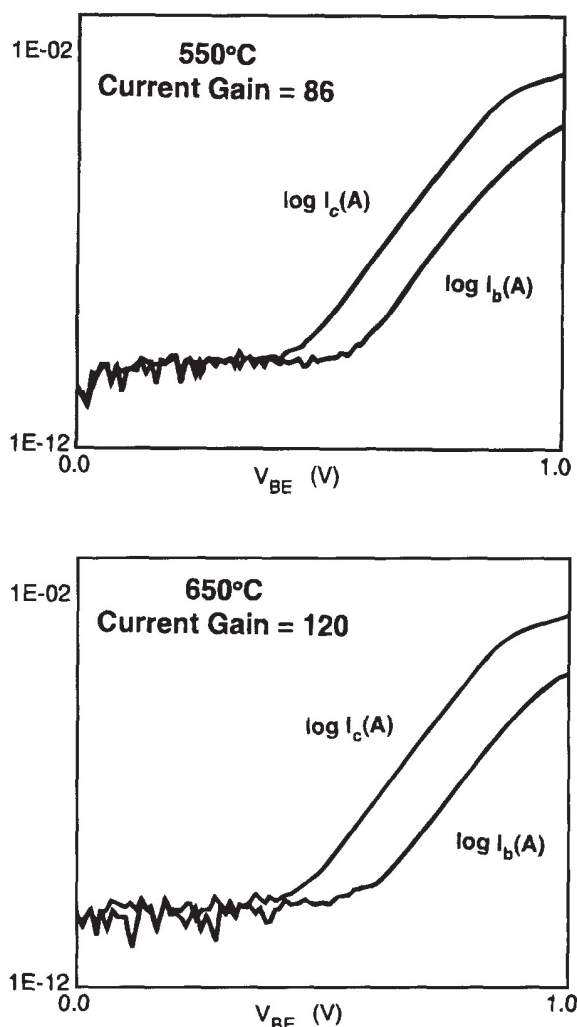


Fig. 4. Gummel plots of transistors with 550 and 650°C push temperatures, respectively.

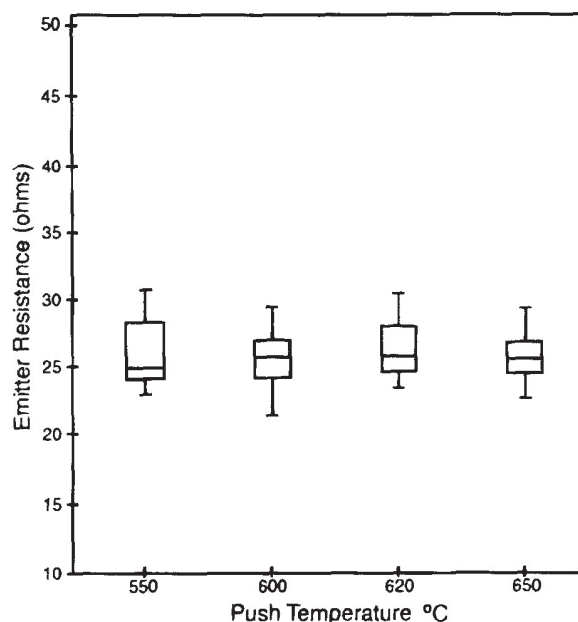
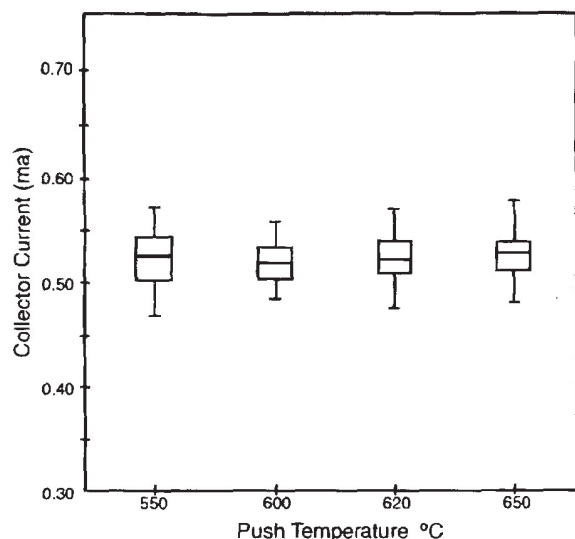


Fig. 6. Emitter resistance as a function of push temperature.

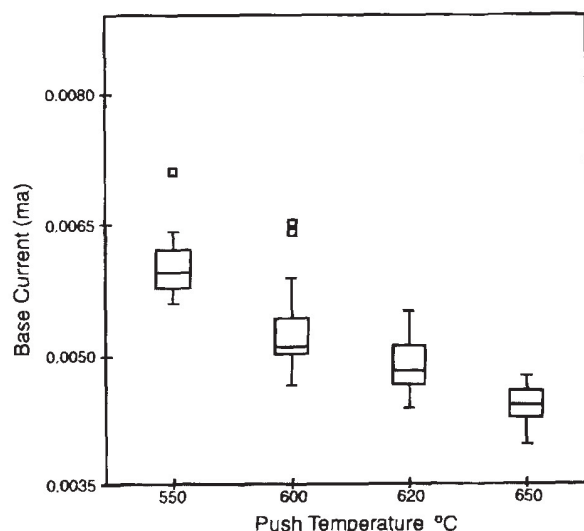


Fig. 5. (top) Collector and (bottom) base currents as a function of push temperature.

decreases with increasing push temperature. In the literature this has been postulated to be due to a small increase in the interfacial oxide thickness.^{7,9}

Figures 6 and 7 show the effect of push temperature on emitter resistance and pinched base resistance, respectively. It is significant that the push temperature does not appreciably impact the emitter resistance. It is important that the factors which increase current gain do not simultaneously deteriorate the emitter resistance. There is however a decrease in R_{pinch} (sheet resistance of the base region between the emitter and collector) with increasing push temperature. This would be consistent if the arsenic diffusion into the base was inhibited by an increase in the interfacial oxide thickness resulting in a greater base width and consequently a lower pinched base resistance.

In order to examine whether these results remain valid over a wider range of process conditions, experiments were run where both the emitter dose and push temperature were varied. Figure 8 is a response surface plot of the collector and base currents as a function of the above parameters. The collector current is seen to increase with increasing emitter dose. This is due to the increased electron

concentration available for injection from the emitter through the base to the collector. The collector current is still seen to be invariant over the push temperature range examined. The base current is again seen to decrease with increasing push temperature. The base current is also seen to increase with increasing emitter dose, probably due to increased electron-hole recombination in the emitter. Thus the effect of the interfacial "oxide" is to present a barrier to holes (from the base) while remaining transparent to electrons (from the emitter).

Various mechanisms for this hole blocking property have been proposed.⁷ One mechanism for this hole blocking property depends on the local arsenic concentration peak at the polysilicon/monosilicon interface (see SIMS profile, Fig. 11). The arsenic peak, resulting from the arsenic segregation at the polysilicon/monosilicon interface, acts as a positive potential barrier for holes but not for electrons.⁸ Of course, if the oxide interface is too thick then bipolar npn current gain will be low and emitter resistance will be high. This is because the oxide interface then forms a significant

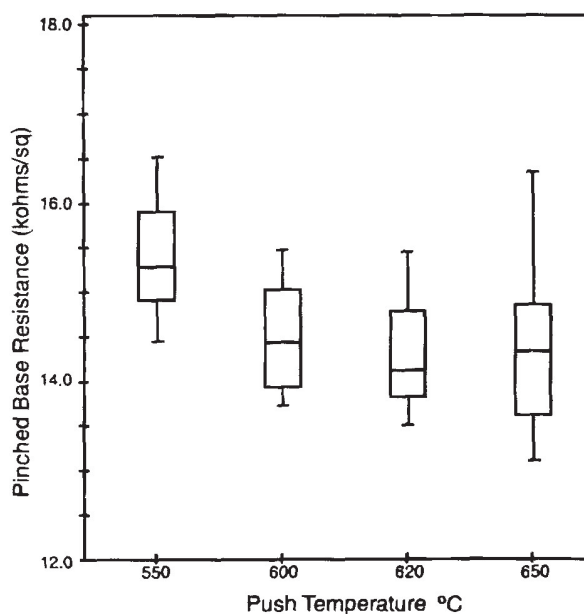


Fig. 7. Base resistance as a function of push temperature.

Fig. 8. Response surface plot of the collector and base currents as a function of the emitter dose and push temperature.

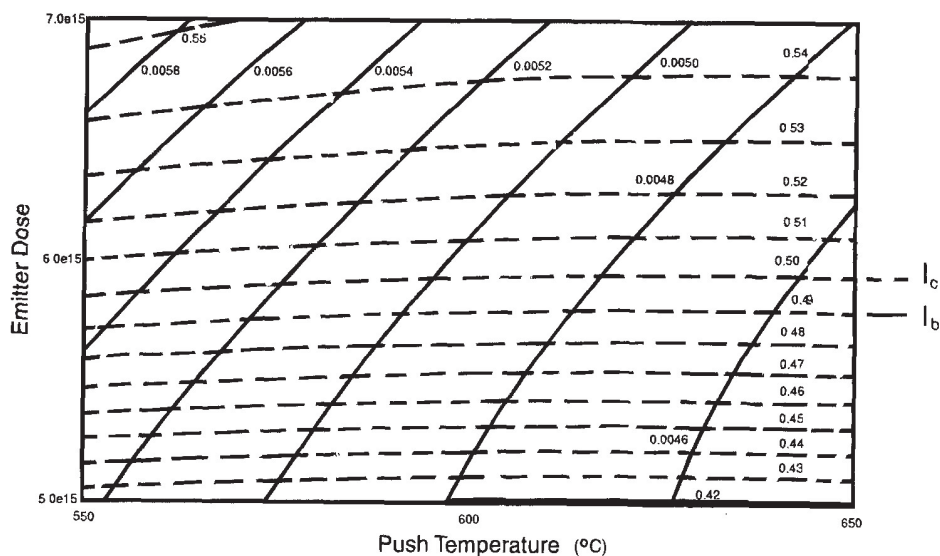


Fig. 9. HRTEM image of polysilicon emitter interface with the monosilicon for a 550°C polysilicon push temperature.

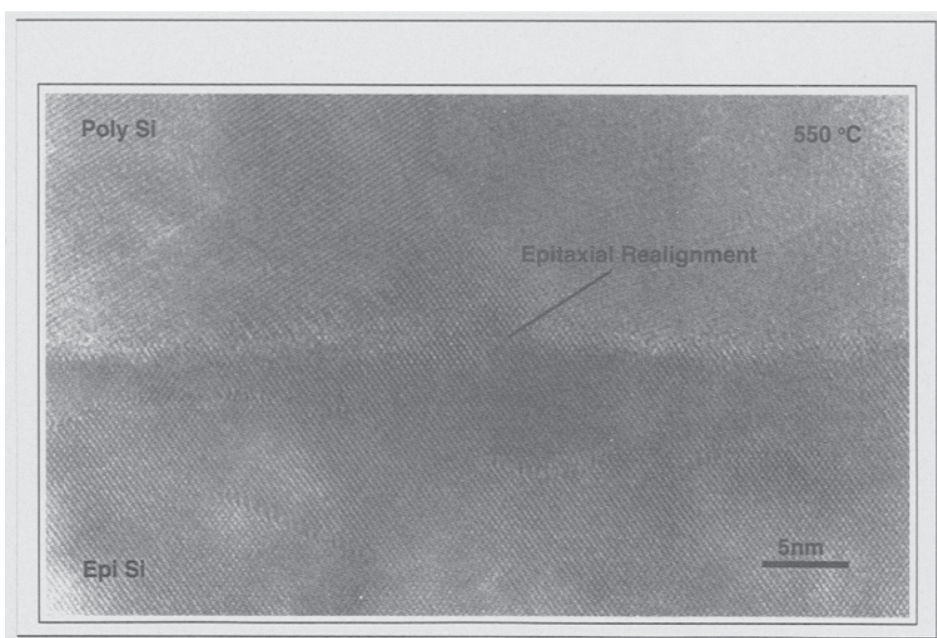
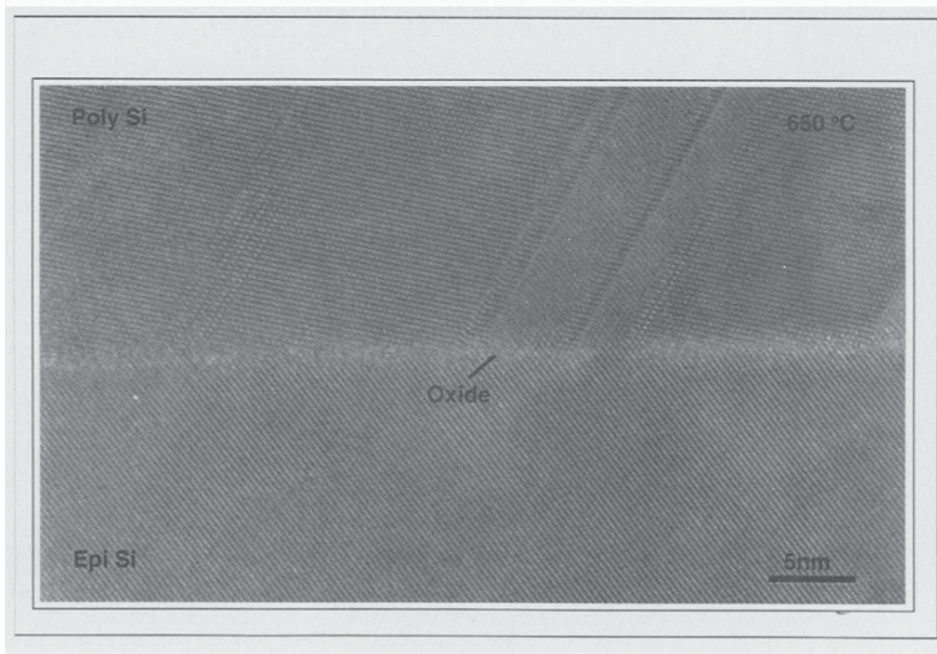


Fig. 10. HRTEM image of polysilicon emitter interface with the monosilicon for a 650°C polysilicon push temperature.



barrier to electron transport as well as to hole transport. Others have found that the detrimental effects of thicker interfacial "oxide" can be corrected by doing a final rapid

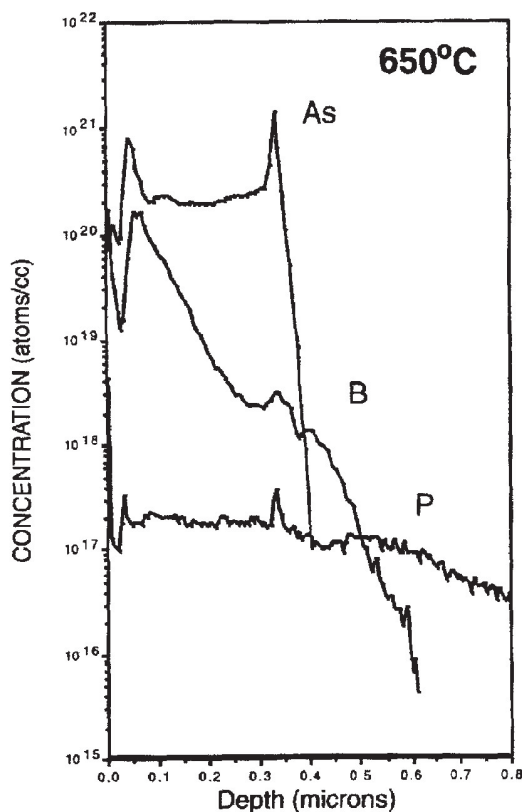
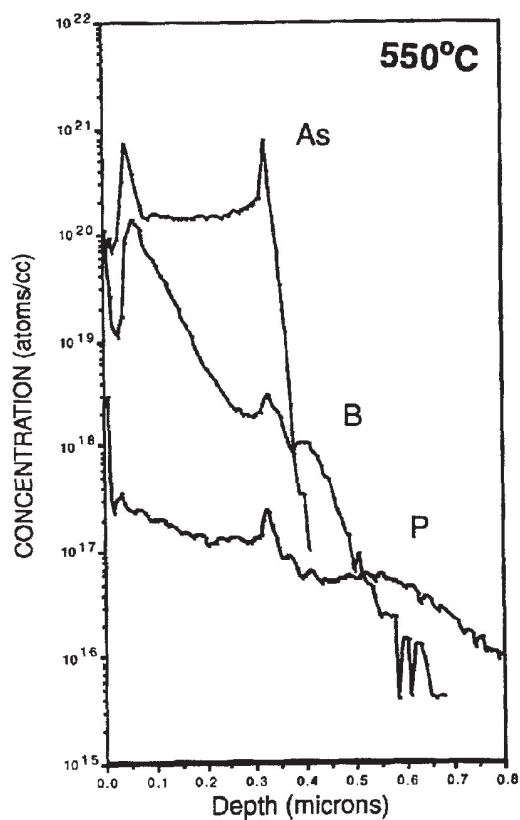


Fig. 11. SIMS profiles of the npn transistor for a (top) 550°C and (bottom) 650°C polysilicon push temperature.

Table I. Coefficient of variability from production data for current gain and emitter resistance.

	Lot to lot	Wafer to wafer	Within wafer
Current gain coefficient of variation	0.124	0.113	0.078
Emitter resistance coefficient of variation	0.046	0.048	0.044

thermal anneal while retaining the improvement in the npn current gain.¹⁰

To corroborate the electrical results and correlate them to other studies, some materials analysis was performed using cross-sectional HRTEM and SIMS. The HRTEM images are from fully processed wafers on the same structures from which the previously shown electrical data were obtained. The HRTEM images taken from similar structures directly after LPCVD deposition are not presented as it is difficult to differentiate between the LPCVD silicon (deposited at 550°C and the interfacial "oxide," both of which are amorphous.

Figure 9 is a HRTEM image of the polysilicon emitter interface with the single-crystal silicon for a 550°C polysilicon push temperature. The light band, which is amorphous, is the interfacial "oxide." It can clearly be seen that this film is not continuous throughout the region. As shown in the figure, there are regions where epitaxial regrowth of the polysilicon has occurred, *i.e.*, where the lines of atomic planes are continuous across the interface. This indicates that the initial interfacial "oxide" film was either not continuous, or more likely, was broken up during subsequent annealing.

Figure 10 is a HRTEM of the polysilicon emitter interface with the single-crystal silicon for a 650°C polysilicon push temperature. The interfacial "oxide" is clearly continuous throughout the region. Thus it appears that with this push temperature there is sufficient initial oxide thickness to prevent its breakup into separate islands during the subsequent anneal cycles.

Figure 11 shows the results of a SIMS investigation of whether any retardation in the arsenic diffusion through the interface could be observed for the two extremes of push temperature. Within the resolution of the instrument it was not possible to observe any significant difference in the diffusion of the arsenic through the interface.

Nevertheless, from the Rpinch data there appears to be a difference in the amount of arsenic diffusion through the interface for the different push temperatures. The HRTEM images show more discontinuity in the interfacial "oxide" at the lower push temperatures. This suggests either a less uniform potential barrier for hole transport or a lower diffusion barrier for the arsenic. This would be consistent with more diffusion of arsenic through the interface causing less of the arsenic to pile up at the interface. Consequently there is a lower potential barrier for holes which results in an increased base current and lower npn current gain.

Two sensitive measures of npn bipolar polysilicon emitter interface control are variations in the current gain and emitter resistance. An examination of production data for current gain and emitter resistance as a function of the coefficient of variation are shown in Table I. The coefficient of variation is defined as the sample standard deviation divided by the sample mean. As can be seen from Table I, our method of growing the interfacial oxide gives adequate control of current gain and emitter resistance. This level of variation was achieved without employing special controls on fabrication area ambient temperature or humidity.

Conclusions

In this paper we have used electrical and material analysis to demonstrate a simple method to tailor and control the interfacial oxide thickness for a polysilicon emitter technology in an advanced BiCMOS process. We have shown that increasing the push temperature when loading the wafers into an LPCVD vertical furnace for polysilicon de-

position increases the interfacial "oxide" thickness. We have confirmed that the npn current gain increases with interfacial oxide thickness without adversely impacting other device parameters. This interfacial oxide has been shown to increase the current gain by inhibiting hole transport but not inhibiting electron transport. Finally, this current gain increase has not occurred at the expense of variability, as long as minimum backstreaming conditions are employed.

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Phosphor Development for α -Silicon Liquid Crystal Light Valve Projection Display

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ABSTRACT

This paper describes the development of a phosphor suitable for efficiently activating an α -silicon photoconductor. The photoconductor is employed to modulate a liquid crystal layer for use in a real-time television projection system. A thorough evaluation of available phosphors disclosed their unsuitability for this use. The major requirement for this material is that: the spectral emission closely match the α -silicon responsivity curve, have sufficient radiance to activate the photoconductor efficiently, be resistant to thermal degradation, and exhibit fast decay. An yttrium aluminum oxide phosphor with the yttrium aluminum garnet (YAG) crystal structure and activated by chromium satisfied the above requirements. The process of making this phosphor is described with emphasis on producing the YAG phase by the most practical means. Products were evaluated for radiance, spectral distribution, crystal structure, decay time, and ease of screen preparation.

The basic components of a liquid crystal light valve (LCLV) display unit¹ is shown in Fig. 1. It consists of a cathode ray tube (CRT) that provides the input image which is coupled to an LCLV through a fiber optic faceplate. A xenon arc lamp provides the output light which is filtered by a UV filter and linearly polarized before reaching the light valve. The image produced on the LCLV output screen passes through a polarizing mirror, a prism wedged window, and then through a projection lens where it forms an enlarged image in a screen which is not shown.

The LCLV is shown in diagrammatic cross section in Fig. 2. It is a thin-film sandwich with an ac voltage applied across it. The unit consists of an amorphous silicon photoconductor layer, a liquid crystal layer, and several other thin films. The photosensor detects an input light image and impresses a replica voltage pattern on the liquid crystal. The voltage pattern of the image on the liquid crystal then electrically alters the optical properties (birefringence) of the layer to modulate the polarization properties of the output laser light beam.

The light valve performs this function at near-video rates while maintaining the resolution and gray scale quality of the image. Between the liquid crystal and photosensor, a combination light-blocking layer/dielectric mirror is

placed to isolate the input and output light beams. The dielectric mirror serves to reflect the output light back through liquid crystal and the light-blocking layer prevents residual output light leakage to the photosensor.

Finally, an analyzer is placed externally in the output laser beam to convert the modulated polarization state into a visible multigray level image. The analyzer can be a high extinction ratio nonabsorptive MacNeille-type polarizing beam splitter which also provides a convenient way of directing output light into the light valve.

The input side of the LCLV consists of a thin layer of a hydrogenated amorphous silicon photoconductor. This layer must change the light image produced by the CRT to an electrical image which is then able to modulate the voltage across a liquid crystal layer providing the image that is projected onto the screen. A requirement for the CRT screen is to supply an image with a spectral distribution which can efficiently activate the α -silicon photoconductor. By matching the spectral distribution of the phosphor to the sensitivity curve of the photoconductor, less current is needed from the electron gun, and improved resolution results.

The requirements of major concern are: (i) spectral peak matched to the response of the amorphous silicon; (ii) maximized radiant energy output in the spectral range of interest; (iii) decay time less than approximately 10 ms meas-

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