

Silicon Heterojunction Solar Cell: A New Buffer Layer Concept With Low-Temperature Epitaxial Silicon

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Abstract—Amorphous silicon/crystalline silicon heterojunction solar cells, deposited by the plasma-enhanced chemical vapor deposition (PECVD) technique, have been fabricated using different technologies to passivate defects at the heterointerface: without treatment, the insertion of a thin intrinsic amorphous layer or that of a thin intrinsic epitaxial layer. The open circuit voltage of heterojunction solar cells fabricated including an intrinsic amorphous buffer layer is strangely lower than in devices with no buffer layer. The structure of the amorphous buffer layer is investigated by high resolution transmission electron microscope observations. As an alternative to amorphous silicon, the insertion of a fully epitaxial silicon layer, deposited at low temperature with conventional PECVD technique in a hydrogen–silane gas mixture, was tested. Using the amorphous silicon/crystalline silicon (p a-Si/i epi-Si/n c-Si) heterojunction structure in solar cells, a 13.5% efficiency and a 605-mV open circuit voltage were achieved on flat Czochralski silicon substrates. These results demonstrate that epitaxial silicon can be successfully used to passivate interface defects, allowing for an open circuit voltage gain of more than 50 mV compared to cells with no buffer layer. In this paper, the actual structure of the amorphous silicon buffer layer used in heterojunction solar cells is discussed. We make the hypothesis that this buffer layer, commonly considered amorphous, is actually epitaxial.

Index Terms—Amorphous materials, epitaxial growth, photovoltaic cells, semiconductor heterojunctions.

I. INTRODUCTION

THE AMORPHOUS silicon/crystalline silicon (a-Si:H/c-Si) heterojunction (HJ) solar cell is one of the most interesting technological solutions for the photovoltaic market, basically due to the excellent performance and the simple low-temperature production process. A key factor of this technology is the insertion of a thin intrinsic amorphous silicon layer between the amorphous emitter and the crystalline base: the HJ with intrinsic thin layer (HIT) concept of the Sanyo group [1]. This buffer layer, thanks to excellent passivating properties, allows very high open circuit voltages and efficiencies. Based on this technology, Sanyo has recently produced panels with a very high efficiency of 17% [2].

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Both the n a-Si:H/p c-Si and p a-Si:H/n c-Si structures can be used. The main advantage of using a p-type silicon wafer as a substrate is its greater minority carrier diffusion length compared to an n-type silicon wafer, resulting in higher short circuit currents, while using n-type silicon wafers, the degradation of carrier lifetime caused by the metastable defects related to boron doping does not apply [3]. The best solution [4], [5] is still a subject of discussion. However, the highest efficiency has been demonstrated by Sanyo using the p/n structure.

In a previous work [6], some epitaxial-like growth during the deposition of intrinsic a-Si:H layers on c-Si, using the plasma enhanced chemical vapor deposition (PECVD) technique and a silane-hydrogen mixture, was observed. Many groups use this gas mixture to deposit by PECVD the i buffer layer in their structures (both p/n and n/p). However, to our knowledge, limited data are available in literature regarding the microstructure of the i layer grown on c-Si substrates. We think that the intrinsic buffer layer used in heterojunction solar cells, commonly considered an amorphous layer, is actually an epitaxial layer.

In the first part of this paper, the structural composition of an intrinsic a-Si:H layer deposited by PECVD on top of a c-Si substrate is investigated in detail, including the effect of the i layer on the solar cell performance. In the second part, the experimental results on solar cell devices with a complete epitaxial Si (epi-Si) buffer layer are discussed. The structural characterization of the buffer layers is carried out by cross section high resolution transmission electron microscopy (HR-TEM), to discern between the amorphous and epitaxial phases. The role of different deposition parameters for the epitaxial layer on solar cell performance is amply analyzed.

II. EXPERIMENTAL

The samples were deposited by PECVD on Czochralski (CZ) (100) n-type $1\text{-}\Omega \cdot \text{cm}$ $500\text{-}\mu\text{m}$ -thick, polished silicon wafers. The c-Si wafers were etched in 0.5% diluted hydrofluoric acid before the introduction in the PECVD vacuum system. Separate chambers for the deposition of intrinsic n-type and p-type layers were used. The deposition conditions are reported in Table I. The plasma frequency for all the samples was 13.56 MHz. Then $1 \times 1 \text{ cm}^2$ solar cells were fabricated using the structure Ag/ITO/p a-Si:H/buffer layer/n c-Si/n⁺ $\mu\text{c-Si}/\text{Al}$. The Ag front grid and the Al back contact were evaporated. The indium tin oxide (ITO) film was deposited by RF (13.56 MHz) magnetron sputtering at 0.5 W/cm^2 power density, in a 0.021 mbar

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TABLE I
PECVD DEPOSITION CONDITIONS: PLASMA POWER DENSITY (P), PRESSURE (p), SUBSTRATE TEMPERATURE (T), AND GAS FLOWS

layer	P	p	T	flow rates			
	(mW/ cm ²)	(mb)	(°C)	(sccm)			
				SiH ₄	B ₂ H ₆	H ₂	PH ₃
p a-Si	28	0.532	120	2.5	0.04	21.46	–
i a-Si	28	0.6	200	20	–	–	–
i epi-Si	28	1	100-250	0.6-4.8	–	90-94	–
n ⁺ μ c-Si	111	1	170	1.96	–	100	0.04

ultrapure Ar atmosphere, at 250 °C. The electrical characteristics of the p layer (deposited on Corning glass) were: dark conductivity $\sigma_{\text{dark}} = 2 \cdot 10^{-3}$ S/cm, and activation energy $E_a = 0.25$ eV. The 50-nm n⁺ μ c-Si layer was deposited by PECVD, at low temperature, on the rear surface of the device, to reduce the contact resistance and form a back surface field (BSF) for photogenerated carriers (for this purpose, the use of a dopant diffusion is not appropriate, as it would introduce a high temperature fabrication step). Different buffer layer solutions were investigated: no buffer layer at all, i a-Si:H buffer layer, i epi-Si buffer layer. The electrical characteristics of the i a-Si:H layer (deposited on Corning glass) were: dark conductivity $\sigma_{\text{dark}} = 2 \cdot 10^{-11}$ S/cm, activation energy $E_a = 0.91$ eV, and photo/dark conductivity ratio $\sigma_{\text{light}}/\sigma_{\text{dark}} = 2 \cdot 10^6$. The a-Si:H layer thicknesses were evaluated by simulating the experimental ultraviolet-visible reflectance spectra. The simulation makes use of the Bruggemann effective medium approximation and a multilayer model based on Fresnel formulation [7]. The solar cell current density–voltage (J – V) characteristics under illumination were measured at 100 mW/cm² AM1.5G irradiance. The HR-TEM observations were performed in cross section geometry.

III. RESULTS AND DISCUSSION

Heterojunction solar cells with different p a-Si:H emitter thicknesses (7, 14, and 30 nm) and with no intrinsic buffer layer at the a-Si:H/c-Si interface were deposited. The experimental J – V curves under illumination are shown in Fig. 1. The short-circuit current density (J_{sc}) decreases as the emitter thickness increases. This was foreseen because the amorphous emitter layer acts mainly as a “dead layer” [8] in which almost all the absorbed light does not generate photocurrent. A dependence of the open circuit voltage (V_{oc}) on emitter thickness is also evidenced. The V_{oc} decreases from about 590 mV for a 30-nm-thick emitter down to 550 mV for a 7-nm-thick emitter. Sawada *et al.* [9], in contrast to our results, do not report any dependence. The V_{oc} trend can be explained by a partial or complete charge depletion of the p-doped emitter layer, with a consequent decrease of the device built-in potential [10]. By thinning the emitter, the depletion region extends to the whole emitter, and the V_{oc} suffers from the built-in potential decrease. Such behavior can be caused by two factors: 1) the electronic quality of our p-doped a-Si layer is too low, due to a large

defect density, and the emitter is easily charge-depleted, 2) the transparent conductive oxide (TCO) on the top of the device has a low work function and the band bending at the TCO/a-Si interface strongly contributes to the emitter depletion, resulting in a large decrease of the built-in potential even with a good quality emitter layer [11]. The dominant factor has not been established yet and is currently under investigation.

As reported in the literature, the deposition of a thin intrinsic amorphous silicon (i a-Si:H) layer on the c-Si substrate, in order to passivate its surface, is considered one of the key factors of the HJ solar cell technology to attain very high efficiencies. On that basis, the i a-Si:H layer growth on top of n-type c-Si wafers has been studied, using the deposition conditions reported in Table I, which result in good quality a-Si:H on glass. A large number of samples were deposited with different deposition times and the corresponding optically evaluated thicknesses (the procedure is described in Section II) are shown in Fig. 2.

The measured i-layer thicknesses increase linearly only with the deposition time longer than 30 s. As the fitting line does not intersect the axis origin, a slower growth at the early stages or even an initial incubation time can be inferred. The intersection of the fitting line with the x axis in Fig. 2 (roughly at 17 s) is assumed as the incubation time. HR-TEM cross section images of an i a-Si:H/c-Si sample, at different magnifications, are shown in Fig. 3. In Fig. 3(a), three main regions are identified: the c-Si structure on the top, the amorphous glue at the bottom, and the deposited layer, previously assumed completely amorphous, in the middle. The resulting thickness of the a-Si:H layer is approximately 11 nm, in agreement with that expected from the results in Fig. 2. However, the interface between the c-Si substrate and the a-Si:H layer is not clear-cut. Some crystalline grains with a sawtooth structure extend from the crystalline into the amorphous phase. This sawtooth grain structure is shown in detail in Fig. 3(b), a magnification of the region surrounded by a white box in Fig. 3(a). The same crystallographic orientation of the c-Si substrate is preserved in the grains: continuous crystalline Si planes crossing the interface formed during the PECVD process are shown in the HR-TEM image, suggesting an epitaxial-like growth. The following growth kinetics can be inferred by the nanostructure of the layer (Fig. 3) and by the deduction of an incubation time (Fig. 2): at the beginning, the layer starts growing epitaxially on c-Si and is indistinguishable from the c-Si phase employing optical measurements [12]. For

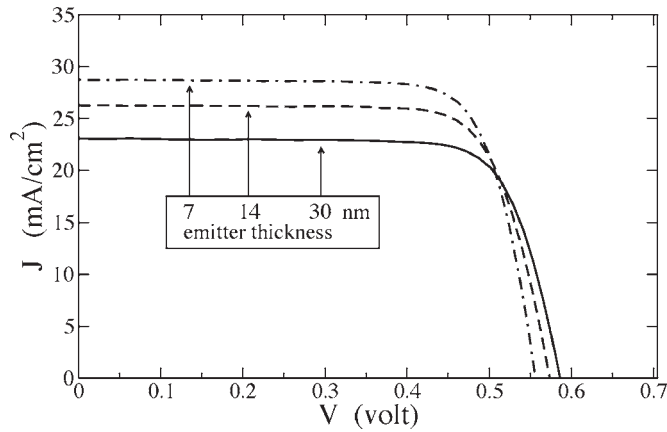


Fig. 1. Experimental J - V curves under illumination of p a-Si/n c-Si heterojunction solar cells having various emitter thicknesses and no buffer layer.

this reason, its thickness is optically undetectable. After a specific time (the incubation time) the deposition rate increases, the growth becomes more disordered and continues with an amorphous phase, whose thickness can be optically evaluated.

Some p (30-nm) a-Si:H/i a-Si:H/n c-Si devices were deposited with different i a-Si:H buffer layer thicknesses, on the basis of the calibration shown in Fig. 2. The experimental J - V curves under illumination are shown in Fig. 4. The device with no buffer layer reveals the higher V_{oc} , while the insertion of an intrinsic buffer layer, deposited using the plasma conditions to obtain a good quality a-Si:H on glass, is detrimental to the V_{oc} . Such result is unexpected taking into account the very different findings reported by T. Tanaka *et al.* [1], which show that the insertion of an i a-Si:H layer, about 5 nm thick, improves the device performance. However, it must be pointed out that Tanaka *et al.* used hydrogen diluted gas mixtures to deposit the a-Si:H buffer layer. Basing on our results that demonstrate an epitaxial growth and the presence of an incubation time even for undiluted plasma conditions, and recalling that the incubation time is expected to increase if hydrogen dilution is applied [13], we believe that fully epitaxial silicon layers, rather than amorphous layers, are actually grown in the plasma conditions used in [1]. It is worth noting that on Corning glass (very often used to test and tailor the deposition conditions) the same deposition parameters would give rise to a completely amorphous layer, because the substrate itself is amorphous and no crystal seed at the beginning drives the growth.

According to these considerations, we decided to investigate the possibility of using fully intrinsic epitaxial silicon as a buffer layer (see also [6] and [14]). The epitaxial growth was further favored by introducing a high H_2 dilution in the gas mixture, close to the chemical equilibrium condition, i.e. when the etching rate is equal to the deposition rate [13].

The p a-Si:H/i epi-Si/n c-Si devices with different deposition times of the intrinsic epitaxial silicon layer, using a 7-nm-thick p layer, were deposited. The deposition conditions for the i layer are: 200 °C, 0.6 sccm SiH_4 , 94 sccm H_2 (other parameters can be found in Table I). The experimental V_{oc} as a function of the deposition time of the i epi-Si layer is shown in Fig. 5. In this case, the deposition time is used, because the thickness of

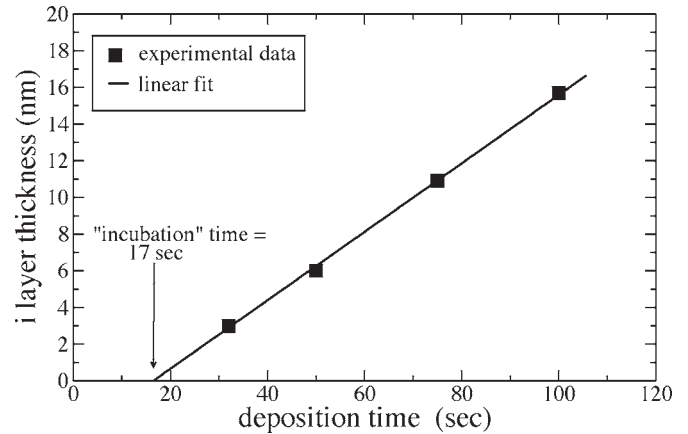


Fig. 2. Intrinsic amorphous silicon layer thickness as a function of deposition time. The substrate is crystalline silicon, thickness is optically evaluated (see Section II).

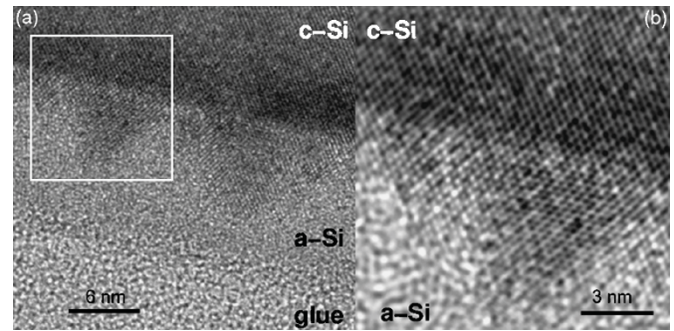


Fig. 3. Cross section HR-TEM images, at different magnifications, of an intrinsic amorphous silicon layer deposited on top of a crystalline silicon wafer. For this sample the expected thickness according to the calibration curve of Fig. 2 was 11 nm. In Fig. 3(a) the white box indicates an epitaxial grain embedded in the amorphous layer, which is shown at a higher magnification in Fig. 3(b).

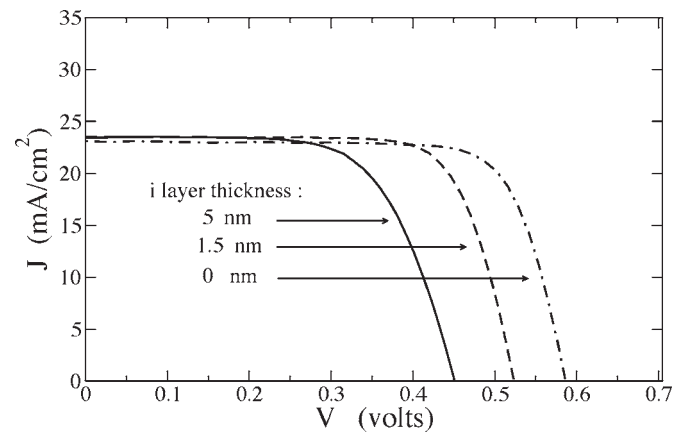


Fig. 4. Experimental J - V curves under illumination of p a-Si/i a-Si/n c-Si heterojunction solar cells with various intrinsic amorphous layer thicknesses. The p emitter layer thickness is 30 nm.

an epitaxial Si layer on crystalline Si cannot be evaluated by means of optical techniques but, as discussed previously, is obtainable by HR-TEM analysis. Without any intrinsic buffer layer (0 min) the V_{oc} is about 550 mV, then it increases with the deposition time, remaining constant after 3 min, with a gain of about 30 mV. We remark that the V_{oc} behavior, with the increasing of

the buffer layer thickness (i.e., the deposition time), is the same as that reported in [1]. The other cell parameters do not show any evident dependence on the deposition time, stable values of $J_{sc} = 29 \text{ mA/cm}^2$ and $FF = 77\%$ are measured. The V_{oc} improvement can be explained by a reduction of defect states on the surface of the c-Si substrate, with a resulting reduction in carrier recombination in this zone. Since the deposited layer is epitaxial, no significant change in the energy band structure, compared to the underlying c-Si, is expected. In this case the recombination current of electrons diffusing from the base to the emitter cannot be reduced by a conduction band offset (contrary to the case of the i a-Si buffer layer). We believe that, depositing in conditions close to the chemical equilibrium (the deposition rate is almost zero), a rearrangement of the c-Si surface resulting in a reduction of surface defect density is more likely to occur than a passivation of such defects.

The effect of the deposition temperature of the i layer on the solar cell parameters was also investigated. Taking into account the results shown in Fig. 5, a set of devices with a 3-min i epi-layer (0.6 sccm SiH_4 , 94 sccm H_2) was fabricated (the p a-Si:H emitter thickness was 7 nm). The experimental V_{oc} versus deposition temperature of the intrinsic layer is shown in Fig. 6. The V_{oc} increases when the temperature is decreased, then it remains almost constant between 150 °C and 100 °C, with a gain of about 25 mV from 250 °C to 150 °C. Once again J_{sc} and FF do not show any dependence on the deposition temperature. Using the i layer deposited at 150 °C for 3 min, a V_{oc} of more than 600 mV is obtained, with a gain of about 50 mV compared to the case with no intrinsic layer. This value is comparable with the results reported in literature for p a-Si:H/i a-Si:H/n c-Si hetero-structures using an amorphous buffer layer, an n-type CZ crystalline silicon substrate and no texturization of the c-Si substrate [8].

It is not clear why a reduction in the deposition temperature of the i epi-layer improves the V_{oc} . However, the same result is found in the case of microcrystalline p-i-n solar cells, where a low temperature deposition of the intrinsic layer is preferred in order to get high V_{oc} . For p-i-n $\mu\text{c-Si}$ devices, Das *et al.* [15] suggest that the higher temperature facilitates the incorporation in the film of oxygen that can form defect states, acting as carrier recombination centers. Similar behavior of oxygen incorporation in the epitaxial buffer layer can be guessed at, due to the presence of a large number of defects in the crystalline structure of epitaxial silicon.

Another deposition parameter has a crucial effect on the i-layer passivation properties on the c-Si surface, i.e., the silane concentration in the gas mixture, $[\text{SiH}_4]/([\text{SiH}_4] + [\text{H}_2])$. A set of devices with a 7-nm-thick p a-Si:H layer and a 3 min i epi-layer was fabricated, varying the silane concentration in the gas mixture during the deposition of the i epi-layer. The temperature was chosen as 150 °C, which was shown to be optimal in Fig. 6. Experimental V_{oc} and FF as a function of silane concentration are shown in Fig. 7. A pure hydrogen plasma treatment (no silane) allows the achievement of a high V_{oc} , up to about 600 mV, but has a detrimental effect on the FF. In fact the cell current under illumination starts falling off in voltages much lower than the V_{oc} , resulting in an S-shaped J - V characteristic (not shown here) and a very low fill factor.

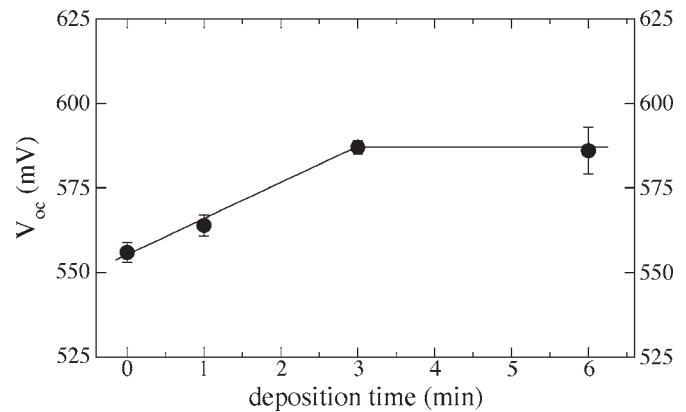


Fig. 5. Experimental V_{oc} of p a-Si/i epi-Si/n c-Si heterojunction solar cells as a function of i epi-Si layer deposition time. The p emitter layer thickness is 7 nm; the i layer deposition temperature and silane concentration are $T = 200^\circ\text{C}$ and $[\text{SiH}_4]/([\text{SiH}_4] + [\text{H}_2]) = 0.6\%$, respectively.

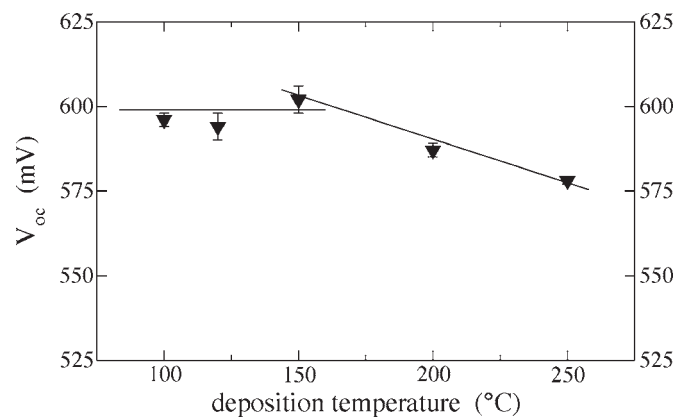


Fig. 6. Experimental V_{oc} of p a-Si/i epi-Si/n c-Si heterojunction solar cells vs. deposition temperature of the intrinsic epitaxial layer. The p emitter layer thickness is 7 nm; the i layer deposition time and silane concentration are $t = 3 \text{ min}$ and $[\text{SiH}_4]/([\text{SiH}_4] + [\text{H}_2]) = 0.6\%$, respectively.

The high V_{oc} obtained indicates that a pure hydrogen plasma is able to remove the kind of defects giving carrier recombination, as expected by an etching action. On the other hand, the presence of an S-shape on the J - V characteristics indicates that some charge defects, not acting as recombination centers, are also generated. This result confirms the damaging effect of a hydrogen plasma treatment before the p layer deposition, as reported by Ulyashin *et al.* [16].

Very low silane concentration results both in a good V_{oc} and a good FF. As mentioned before, the deposition condition at very low silane concentration (close to the chemical equilibrium) is expected to give the best result. Since etching and deposition act at the same rate, there is no net etching and consequently no formation of charged defects (no S-shape, good FF). Moreover, the very low deposition rate permits a surface structure rearrangement resulting in a net reduction of recombination centers (high V_{oc}). Increasing the silane concentration both FF and V_{oc} decrease. For a 2.5% silane concentration the spread of the measured V_{oc} values for different cells on the same wafer indicates the presence of surface inhomogeneities. Moving away from the chemical equilibrium conditions, the growth of an amorphous phase is favored and can occur in

some wafer regions, preventing the formation of a fully epitaxial layer. For a 5% silane concentration the V_{oc} value is as low as 470 mV, which is approximately the value measured on cells with a 5-nm i a-Si layer deposited without H_2 dilution. The drop in V_{oc} can be correlated with the growth of an amorphous phase mixed with some epitaxial grains, with a sawtooth amorphous/crystalline interface (see Fig. 3), due to the higher silane concentration. This morphology gives rise to recombination paths along the intrinsic layer which negatively affect the V_{oc} . The results in Fig. 7 show that the 0.6% silane concentration, used in the previous experiments, was already a good choice.

To check whether the V_{oc} is limited by the emitter layer quality or by the TCO/emitter interface properties rather than by the recombination in the base bulk or at the emitter/base interface, a p a-Si:H/i epi-Si/n c-Si device with a thicker emitter layer was deposited. The purpose was to investigate whether the V_{oc} dependence on the emitter thickness, observed in devices without the buffer layer (see Fig. 1), is still present. The device with the i epi-Si layer and 30-nm-thick emitter has shown a V_{oc} increase of about 10 mV, compared to the device having a 7-nm-thick emitter. This indicates that a further increase of the V_{oc} , by an appropriate optimization of the p layer and TCO properties, is possible. A valid alternative to improve the emitter quality is the use of a better microcrystalline emitter instead of the amorphous one. A p-doped microcrystalline silicon (μ c-Si) emitter gives rise to a high built-in potential. Moreover, due to its better electronic quality (higher doping level and carrier diffusion length) with respect to amorphous silicon, it does not suffer from eventual charge depletion at the junction with TCO front contact [17]. In a previous work [12], heterojunction devices with a p μ c-Si emitter and an i a-Si:H buffer layer were fabricated. A remarkable result of 640-mV open-circuit voltage was achieved, due to the higher built-in potential of the device. However, the deposition of μ c-Si on an epitaxial buffer layer can be very difficult, resulting in unwanted epitaxial growth of the emitter too. An attempt to get over this technological difficulty, using a double layer emitter (p a-Si/p μ c-Si), is under investigation.

The highest efficiencies of p a-Si/i epi-Si/n c-Si cells were obtained using a 7-nm-thick p layer. The external quantum efficiency QE and the J - V curve under illumination of one of the best devices with i epi-Si layer, with 13.5% efficiency, 0.79 FF, 28.2 mA/cm^2 J_{sc} and 605 mV V_{oc} , are shown in Fig. 8. This result is comparable with the state of the art for p/n heterojunction solar cells on flat CZ silicon wafers fabricated with a completely low temperature process (no dopant diffusion on the back of the cell, temperature lower than 250°C) [8].

A HR-TEM cross section image of the same device (J - V and QE in Fig. 8) can be seen in Fig. 9. In the image, three main regions can be recognized: the c-Si structure on the top, the ITO layer at the bottom (darker region) and the p a-Si:H layer in the middle. The thickness of the p a-Si:H layer, evaluated from the HR-TEM image, is about 7 nm and confirms the optically measured thickness. The interface between the p a-Si:H and c-Si, in contrast with Fig. 3, is more clear-cut. Moreover, at the interface, the figure shows a brighter zone

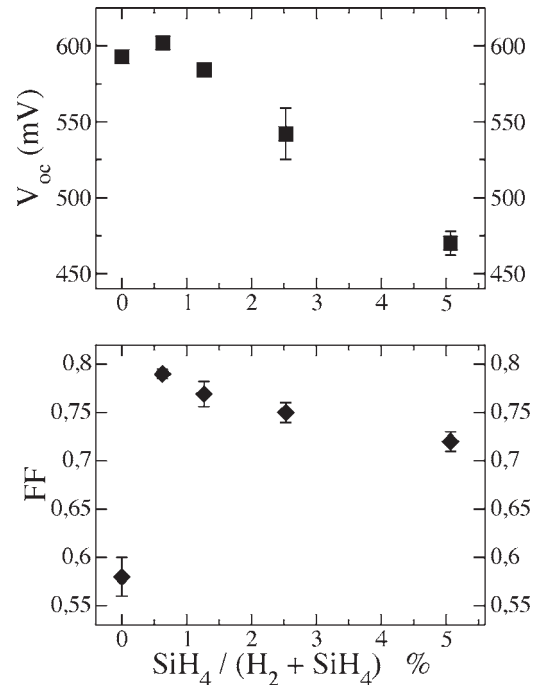


Fig. 7. Experimental V_{oc} and FF of p a-Si/i epi-Si/n c-Si heterojunction solar cells versus silane concentration during the i epi-Si deposition. The p emitter layer thickness is 7 nm; the i layer deposition time and temperature are $t = 3 \text{ min}$ and $T = 150^\circ\text{C}$, respectively.

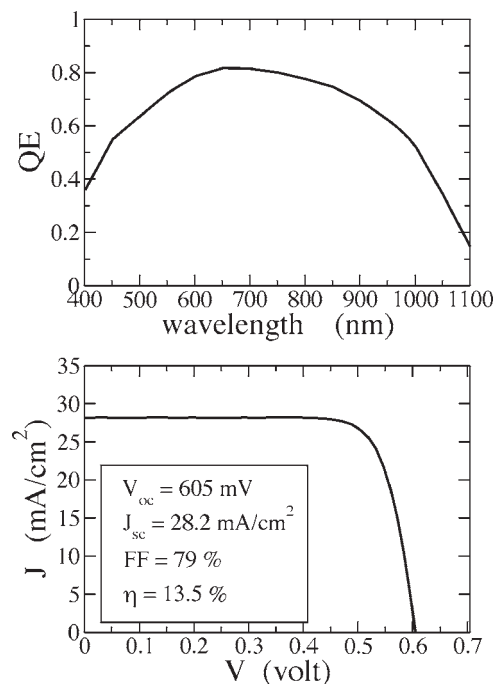


Fig. 8. External quantum efficiency QE and J - V curve under illumination of one of the best devices having an i epi-Si buffer layer. The p emitter thickness is 7 nm.

of a few monoatomic layers in which the crystalline matrix is still visible. This region can be associated with the intrinsic epitaxial layer. The very fine thickness of the i epi-Si is in agreement with a deposition rate close to zero, i.e. deposition conditions close to chemical equilibrium.

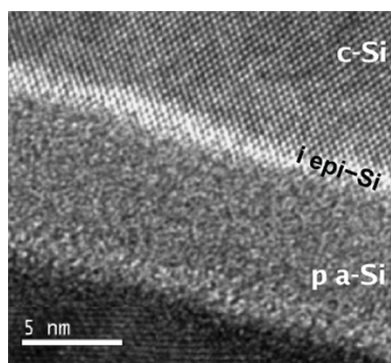


Fig. 9. Cross section HR-TEM image of the same device shown in Fig. 8.

IV. CONCLUSION

The HR-TEM cross section observations of our a-Si:H/c-Si heterojunction solar cells show that the typical deposition conditions used to deposit an i-a-Si:H buffer layer on top of c-Si can actually lead to the formation of a partial or even complete epitaxial layer. We suggest that, epitaxial silicon, rather than amorphous silicon, is often unknowingly deposited as a buffer layer in heterojunction solar cells, because the epitaxial growth is favored in hydrogen diluted plasmas (commonly used in intrinsic buffer layer deposition). To our knowledge, no HR-TEM observation of the i buffer layers deposited on c-Si has ever been shown in literature, whereas the HR-TEM is one of the best techniques that can distinguish the amorphous phase from the epitaxial phase in these structures. Using a very thin intrinsic epitaxial buffer layer deposited by PECVD, a gain of more than 50 mV in open circuit voltage, compared to the cell with no buffer layer, is demonstrated. This gain is equivalent to the best results reported in literature, further confirming the hypothesis that the intrinsic (usually considered “amorphous”) buffer layer used in heterojunction solar cells is actually an epitaxial layer.

The epitaxial silicon layer has been deposited at low temperature (the best cell performance is with the 150 °C epi-Si layer), resulting in a completely low temperature process for the fabrication of the solar cell. A reproducible 13.5% efficiency is achieved.

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