

Exhibit 2027

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HANWHA SOLUTIONS CORPORATION,

Petitioner

v.

MAXEON SOLAR PTE. LTD.,

Patent Owner

Case No. IPR2024-01203

U.S. Patent No. 8,222,516

**DECLARATION OF DOUGLAS RUBY, PH.D. IN SUPPORT OF
PATENT OWNER'S RESPONSE**

IPR2024-01203
Maxeon Exhibit 2027

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I, Douglas Ruby, Ph.D., declare as follows:

I. INTRODUCTION

1. I have been asked by counsel for Patent Owner Maxeon Solar Pte. Ltd. to provide my opinions on certain matters raised in the Petition for *Inter Partes* Review, Paper 3, filed by Petitioner Hanwha Solutions Corporation with respect to U.S. Patent No. 8,222,516 (Ex. 1001, “the ’516 patent”) and the declaration of Dr. Zachary Holman in support of the Petition, Ex. 1003. This declaration sets forth the opinions that I have reached to date regarding these matters.

2. My independent expert consulting services are being billed at the rate of \$450/hour (plus reasonable expenses) for consulting, review, preparation, and \$475/hour (plus reasonable expenses) for depositions. My compensation is not contingent on the outcome of my review and analysis. I have no financial interest in Patent Owner.

II. QUALIFICATIONS

3. Exhibit 2028 is a true and correct copy of my *curriculum vitae* (CV).

4. As set forth in my CV, I have over 30 years of experience leading teams, managing R&D projects, and advancing solar energy technologies.

5. The following is a brief summary of my relevant qualifications and professional experience.

6. In 1978, I received my Bachelor of Science degree in Physics from the Massachusetts Institute of Technology (MIT). My Bachelor's Thesis, titled *A Study of Linewidths in Rydberg States of Atomic Sodium*, discussed light emissions from highly excited states of sodium atoms. In 1980, I received my Master's degree in Semiconductor Physics from the University of Illinois. And in 1985, I received my Ph.D. in Semiconductor Physics from the University of Illinois. My Ph.D. Thesis, titled *A Study of Electron Traps in VPE GaAs Grown With Added Oxygen*, discussed impurities and defects in semiconductors.

7. I am currently a consultant to the photovoltaics ("PV") industry, specializing in PV cell and system design and performance modeling, PV cell and module test procedures, measurement protocols and performance analysis, and PV cell module fabrication process development. My work typically includes but is not limited to (1) working with PV cell manufacturers to improve the performance and reduce the cost of their cell designs and fabrication processes, (2) providing due diligence and technical expertise on technology selection, conceptual layouts, specification development, and energy production estimates for PV power plant proposals, (3) using numerical modeling to pinpoint sources of loss mechanisms and to determine technical requirements necessary for cost-effective PV cell and module performance, (4) providing expert witness services for legal proceedings requiring photovoltaic technology expertise, (5) writing and presenting short

courses on Silicon PV Manufacturing and Technology to PV manufacturers worldwide, and (6) providing PV module, array and system performance measurements and comparison with energy-production model predictions.

8. From 1985 to 2008, I was a principal member of the technical staff at the Sandia National Laboratories in Albuquerque, NM. The work I performed there include but is not limited to (1) acting as Team Leader of PV Cell Development Team and the \$2M/year semiconductor fabrication facility, where I directed 7 team members, authored annual operating plan, directed all PV cell research projects, and was responsible for tasks and milestones of Si cell research and maintaining quality control, (2) acting as director of Crystalline Silicon Research Cooperative, a government/industry consortium for mutually beneficial research consisting of representatives from the entire US Si-PV manufacturing and research communities, (3) acting as contract monitor and advisor for several R&D contracts in the DOE Concentrator Initiative Program from 1990 to 1993, where I was closely involved and providing technical feedback for manufacturers developing Concentrator Photovoltaics systems, (4) acting as a charter member of the PV Manufacturing Technology Program Implementation Committee, a DOE/National Lab group directing \$11M/year in industry-contracted DOE research, (5) successfully led two 3-year competitively awarded projects as Principal Investigator in silicon solar cell processing, submitting original proposals, building

successful interdisciplinary teams, authoring review presentations, and meeting all milestones. (6) initiated and directed a graduate student research program at the University of New Mexico with Professor Charles Fleddermann, resulting in several graduate student thesis projects in solar cell fabrication processing to improve solar cell performance, (7) authored competitively evaluated proposal to DOE Hydrogen Program to lead a multidisciplinary team in a project to improve efficiency and cost-effectiveness of PV-powered water-electrolysis for hydrogen production, (8) served as subarea chairman of 2000 IEEE PV Specialists Conference in Silicon Cell Processing, (9) served as Session Chairman of PV session at 1999 ASME Renewable Energy Conference, (10) directed graduate student research program contract at Georgia Institute of Technology with Professor Ajeet Rohatgi, and managed a \$2.8M solar cell research and development contract, and (11) initiated and successfully conducted several direct industry joint experiments with most major US Si solar cell manufacturers, resulting in numerous publications and several process improvements adopted by industry into manufacturing production lines.

9. Beyond my academic experience, I have significant professional experience in the field of PV technology. In 1993, I designed and fabricated the world's first 20% efficient Si concentrator solar cell on low-cost Si. In 1999, I received the Best Paper Award at the ASME Renewable Energy Conference.

10. My work has been published in over 60 publications since 1981, including over 50 publications on my work with solar cell technologies. A complete list of my publications and publication metrics are listed on pages 12-18 of my CV.

11. I am an inventor on 5 issued U.S. patents related to solar cell technologies. A complete list of my patents can be found on pages 6-7 of my CV.

III. DOCUMENTS CONSIDERED

12. In formulating my opinions, I have considered the documents cited in this declaration and the following:

- Petition for *Inter Partes* Review of U.S. Patent No. 8,822,516 (Paper 3)
- U.S. Patent No. 8,822,516 (Ex. 1001)
- File History of U.S. Patent No. 8,822,516 (Ex. 1002)
- Declaration of Dr. Zachary Holman Regarding U.S. Patent No. 8,822,516 B2 (Ex. 1003)
- EP17322142A1 to Armin Froitzheim (“Froitzheim”) (Ex. 1004)
- Gan and Swanson, *Polysilicon Emitters for Silicon Concentrator Solar Cells*, IEEE Conference on Photovoltaic Specialists, Vol. 1, Pages 245-240 (1990) (“Gan”) (Ex. 1005)
- WO 2009/094575 A2 (“Borden-575”) (Ex. 1006)
- U.S. Patent No. 6,998,288 to Smith (“Smith”) (Ex. 1005)
- CN 1949545A to Li (Translation) (“Li”) (Ex. 1008)
- Zachary C. Holman, *Electron Transport in Amorphous Silicon* (May 2005) (Thesis Presented to The Division of Mathematics and Natural Sciences, Reed College) (“Holman-Thesis”) (Ex. 1010)
- U.S. Provisional Appl. No. 61/023,354 (“Borden-Provisional”) (Ex. 1011)
- U.S. Patent App. Pub. No. 2006/0157103 (“Sheats”) (Ex. 1012)
- U.S. Patent No. 7,468,485 to Swanson (“Swanson”) (Ex. 1015)

- R. J. Komp, Practical Photovoltaics Electricity From Solar Cells, 3rd Ed. (2002) (“Komp”) (Ex. 1016)
- BP Solar Global Marketing, BP-MSX-120, 120-Watt Multicrystalline Photovoltaic Module (“BP-MSX-120”) (Ex. 1017)
- J. Nelson, *The Physics of Solar Cells*, Imperial College Press (2003) (“Nelson”) (Ex. 1018)
- T. Krygowski, A. Rohatgi, D. Ruby, *Simultaneous P and B Diffusion, In-Situ Surface Passivation, Impurity Filtering and Gettering for High-Frequency Silicon Solar Cells*, SAND-97-2620C; CONF-970953- (“Krygowski”) (Ex. 1019)
- A. Luque, S. Hegedus, *Handbook of Photovoltaic Science and Engineering*, Wiley (2003) (“Luque”) (Ex. 1020)
- J. Gordon, *Solar Energy the State of the Art*, ISES (2001) (“Gordon”) (Ex. 1021)
- U.S. Patent No. 6,262,359 to Meier (“Meier”) (Ex. 1022)
- U.S. Patent No. 4,525,593 to Yablonovitch (“Yablonovitch”) (Ex. 1023)
- WO 2009/094578 A2 (“Borden-578”) (Ex. 1024)
- U.S. Patent No. 4,665,277 to Sah (“Sah”) (Ex. 1025)
- D. Chapin et al., *A New Silicon P-N Junction Photocell for Converting Solar Radiation into Electrical Power*, J. Appl. Phys. 25, 676 (1954) (“Chapin”) (Ex. 1026)
- W. Shockley, H. J. Queisser, *Detailed Balance Limit of Efficiency of pn Junction Solar Cells*, J. Appl. Phys. 32, 510 (1961) (“Shockley”) (Ex. 1027)
- A. Metz, R. Meyer, B. Kuhlmann, M. Grauvogl, R. Hezel, *18.5% Efficient First-Generation MIS Inversion-Layer Silicon Solar Cells*, 26th PVSC (1997) (“Metz”) (Ex. 1029)
- D. De Ceuster, P. Cousins, D. Rose, D. Vicente, P. Tipones, W. Mulligan, *Low Cost, High Volume Production of >22% efficiency silicon solar cells*, 22nd European Photovoltaic Solar Energy Conference, 3-7 September 2007, Milan, Italy, pp. 816-819 (“De-Ceuster”) (Ex. 1029)
- J. Benick, J. Rentsch, Ch. Schetter, C. Voyer, D. Biro, R. Preu, *PECVD PSG as a Dopant Source for Industrial Solar Cells*, Presented at the 21st European Photovoltaic Solar Energy Conference, September 4-8, 2006, Dresden (2CV.4.26) (“Benick”) (Ex. 1030)
- Translation Declaration for JP07-106611 to Okayasu (Ex. 1032)

- Robert F. Pierret, *Semiconductor Device Fundamentals*, Addison Wesley Longman (Part I) (1996) (“Pierret”) (Ex. 1033)
- A. I. A. Rahim, C. D. Marsh, P. Ashburn, G. R. Booker, *Impact of Ex-Situ and In-Situ Cleans on the Performance of Bipolar Transistors With Low Thermal Budget In-Situ Phosphorus-Doped Polysilicon Emitter Contacts*, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 48, NO. 11 (November 2001) (“Rahim”) (Ex. 1034)
- N. S. Parekh, R. V. Taylor, D. O. Massetti, *A Simple Method to Control Bipolar Polysilicon Emitter Interfacial Oxide*, J. Electrochem. Soc., Vol. 141, No. 11, pp. 3167-3172 (1994) (“Parekh”) (Ex. 1035)
- E. Yablonovitch, T. Gmitter, R. M. Swanson, Y. H. Kwark, *A 720 mV open circuit voltage SiO_x:c-Si:SiO₂ double heterostructure solar cell*, Appl. Phys. Lett. 47, 1211–1213 (1985) (“Yablonovitch-1985”) (Ex. 1036)
- File History of U.S. Patent App. No. 14/504,771 (“771FH”) (Ex. 1039)
- U.S. Patent Appl. Pub. No. 2002/0142500 A1 (“Foglietti”) (Ex. 1042)
- Mark John Kerr, *Surface, Emitter and Bulk Recombination in Silicon and Development of Silicon Nitride Passivated Solar Cells* (2002) (Ph.D. Thesis, The Australian National University) (“Kerr”) (Ex. 1043)
- M. Green, *Silicon Solar Cells Advanced Principles & Practice*, Centre for Photovoltaic Devices and Systems (1995) (“Green-1995”) (Ex. 1045)
- Y. H. Kwark, R. M. Swanson, *N-Type Sipos and Poly-Silicon Emitters*, Solid-State Electronics Vol. 30, No. 11, pp. 1121-25 (1987) (“Kwark”) (Ex. 1046)
- G. R. Wolstenholme, N. Jorgensen, P. Ashburn, G. R. Booker, *An investigation of the thermal stability of the interfacial oxide in polycrystalline silicon emitter bipolar transistors by comparing device results with high-resolution electron microscopy observations*, J. Appl. Phys. 61, 225-33 (1987) (“Wolstenholme”) (Ex. 1047)
- M. Green, *Solar Cells Operating Principles Technology and System Applications* (1986) (“Green-1986”) (Ex. 1049)
- N. G. Tarr, *A polysilicon emitter solar cell*, IEEE Electron Device Letters, vol. 6, no. 12, pp. 655-658, Dec. 1985 (“Tarr”) (Ex. 1050)
- R. M. Swanson, *Point Contact Solar Cells: Modeling and Experiment*, Solar Cells, 17, pp. 85-118 (1986) (“Swanson-1986”) (Ex. 1051)

- U.S. Patent No. 7,144,751 to Gee (“Gee”) (Ex. 1054)
- WO 2006/097303 A1 (“Agostinelli”) (Ex. 1056)
- R. M. Swanson, R. A. Sinton, *High-Efficiency Silicon Solar Cells, Advances in Solar Energy: An Annual Review of Research and Development*, vol. 6. Chapter 4 (1990) (“Swanson-1990”) (Ex. 1058)
- G. Lubberts, B. C. Burkey, F. Moser, E. A. Trabka, *Optical properties of phosphorus-doped polycrystalline silicon layers*, J. Appl. Phys. 52(11), (Nov. 1981) (“Lubberts”) (Ex. 1059)
- U.S. Patent No. 6,352,876 to Bordogna (“Bordogna”)
- E. Centurioni, D. Iencinella, R. Rizzoli, F. Zignani, *Silicon Heterojunction Solar Cell: A New Buffer Layer Concept With Low-Temperature Epitaxial Silicon*, IEEE Transactions on Electron Devices, Vol. 51, No. 11 (November 2004) (“Centurioni”) (Ex. 1061)
- M. Farrokh-Baroughi, H. El-Gohary, S. Sivoththaman, *Optical, Electrical, and Structural Properties of PECVD Quasi Epitaxial Phosphorous Doped Silicon Films on Crystalline Silicon Substrate*, Canadian Solar Buildings Conference (August 20-24, 2004) (“Farrokh-Baroughi”) (Ex. 1062)
- A. Hauser, G. Hahn, M. Spiegel, H. Feist, O. Breitenstein, J.P. Rakotoniaina, P. Fath, E. Bucher, *Comparison of Different Techniques for Edge Isolation*, 17th European Photovoltaic Solar Energy Conference (October 2001) (“Hauser”) (Ex. 1063)
- U.S. Patent No. 7,071,018 to Mason (“Mason”) (Ex. 1065)
- U.S. Patent No. 4,748,130 to Wenham (“Wenham”) (Ex. 1066)
- Gan, Jon-Yiew, Polysilicon emitters for silicon concentrator solar cells, Stanford University (July 1990) (“Gan Thesis”) (Ex. 2003)
- Feldmann, et al., “A Passivated Rear Contact for High-Efficiency n-Type Silicon Solar Cells Enabling High VocS and FF > 82%” (28th European PV Solar Energy Conference & Exhibition, Paris, Sept. 30 – Oct. 4, 2013) (Ex. 2010)
- Declaration of Mary K. Bolin, Ph.D. (Ex. 2026)
- Transcript of Deposition of Dr. Zachary Holman, taken May 8, 2025 (Ex. 2029)

IV. ASSUMPTIONS

A. Date of Invention

13. Patent Owner's counsel asked me to assume that the date of the inventions of the claims of the '516 patent was February 20, 2008.

B. Person of Ordinary Skill in the Art

14. I have been asked to apply the skill level of a person of ordinary skill in the art ("POSITA") that is proposed in the Petition, which is "someone with an advanced degree involving the discipline of electrical engineering, applied physics, chemistry, or materials science, and at least two years of experience designing, developing, or researching in the field." Petition, 3.

15. At the time of the inventions of the claims of the '516 patent, I was aware of the understandings and capabilities of a person having the skill level described above. This awareness was informed by my experience in academia where I worked with many persons that possessed such a level of skill at and around the time of the invention.

V. RELEVANT PATENT LAW STANDARDS

A. Claim Construction

16. I understand that patent claim terms are generally given their ordinary and customary meaning as understood by a POSITA in the art when read in the context of the specification and prosecution history. Two exceptions are when (1)

the patentee acts as their own lexicographer, or (2) the patentee disavows the full scope of the claim term.

17. I also understand that, in construing the claims, the analysis should focus on the words of the claims. However, patent claims are not read in a vacuum and should instead be read in view of the specification and prosecution history, i.e., the back-and-forth correspondence between the patent applicant and the U.S. Patent and Trademark Office. I further understand that the patent specification is the single best guide to the meaning of a claim term. Thus, a construction that is not supported by the specification should be rejected, even if that construction is plausible, if divorced from the specification. However, it is improper to read limitations from the specification into a claim absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited. At bottom, the interpretation to be given a claim term can be determined and confirmed only with a full understanding of what the inventors actually invented and intended to envelop with the claim.

B. Obviousness

18. I understand that a determination that a claim is “obvious” is based on underlying factual issues including the content of the prior art and the level of skill in the art. I understand that for a single prior art reference or a combination of prior art references to render a claim obvious, and thus unpatentable, a POSITA in the

art must have been able to arrive at the claim by altering or combining the references. I have been informed that all elements of a claim must be considered in an obviousness analysis.

19. I further understand that when considering the obviousness of a patent claim, one should consider whether a teaching, suggestion, or motivation to combine the references exists so as to avoid impermissibly applying hindsight when combining or modifying the prior art. I understand that this test should not be applied rigidly, but that the test can be important to avoid such hindsight.

20. I have been informed that, for a claim to have been obvious, a POSITA must have had a reasonable expectation of success in combining or modifying prior art references to arrive at the claim. I understand that absolute predictability is not required. I further understand that the test is reasonable probability of success not some degree of unpredictability.

C. Standard of Proof

21. I understand that the standard to prove unpatentability is by a preponderance of the evidence, which means more likely than not.

VI. BACKGROUND OF THE '516 PATENT AND RELATED TECHNOLOGY

22. The '516 patent "relates generally to solar cells." Ex. 1001, 1:21. According to the '516 patent, "[s]olar cells are well known devices for converting

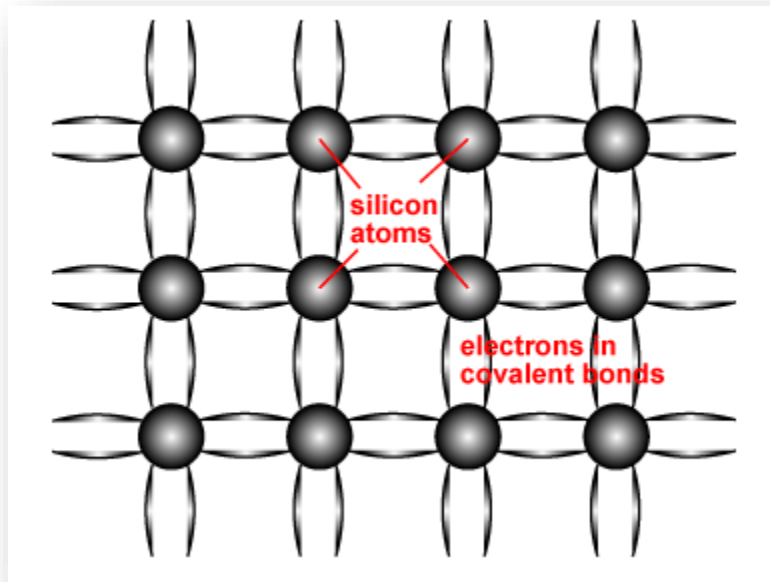
solar radiation to electrical energy.” Ex. 1001, 1:19-20. This field is also known as photovoltaics.

A. Theory of Converting Solar Energy into Electricity

23. Sunlight is composed of a flux of individual particles called photons. A photon is characterized by its wavelength, λ , or its energy, E . The total radiant power emitted from the sun is composed not of a single wavelength, but of many wavelengths and, therefore, does not appear as individual colors to the human eye.

24. According to the '516 patent, solar cells “may be fabricated on a semiconductor wafer.” Ex. 1001, 1:20-22. One type of semiconductor uses a silicon (Si) substrate which is made up of individual Si atoms bonded together in a regular, periodic structure to form an arrangement whereby each atom is surrounded by eight electrons. Each silicon atom has four valence electrons which are individually shared with those of four neighboring Si atoms, forming four covalent bonds with the four surrounding Si atoms.

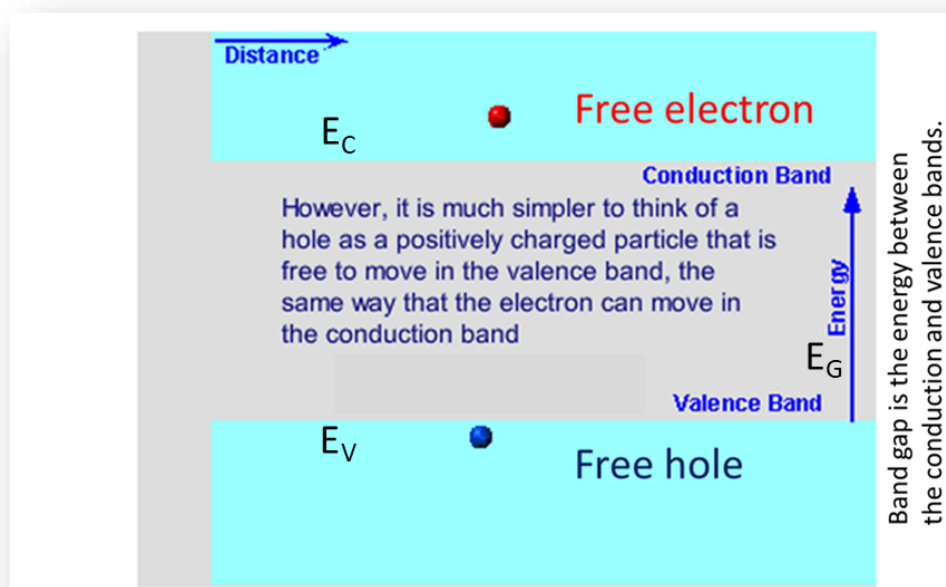
25. Below is a schematic representation of covalent bonds in a silicon crystal lattice. Each line connecting the atoms represents an electron being shared between two atoms. Two electrons being shared are what form the covalent bond.



26. The lowest energy position for an electron to be in is its bound state. If the electron has enough thermal energy to break free of its bond, then it becomes free and available for electric conduction (in the conduction band). The electron cannot attain energy values intermediate to these two levels; it is either at a low energy position in the valence band (valence electron) or it has gained enough energy to break free and contribute to conduction (jumps to conduction band). The minimum energy required is the difference between conduction and valence band energies and is called the “band gap” of a semiconductor.

27. The vacancy left behind by an electron that has been promoted to the conduction band allows the empty covalent bond to move freely from one atom to another, acting like a positive charge moving through the crystal lattice, much like

a bubble moving through a liquid. This empty bond is commonly called a “hole” and acts like a positive charge with unique properties such as mass and mobility, and also contributes to conduction. The lower energy level is E_V and the energy level at which an electron can be considered free is E_C . The band gap (E_G) is the energy difference between the conduction band and valence band.



B. Doping

28. It is possible to shift the balance of electrons and holes in a silicon crystal lattice by “doping” it with other atoms. Donor atoms with one more valence electron than silicon are used to produce “N-type” semiconductor material, which adds electrons to the conduction band and hence increases the number of free electrons (negatively charged carriers). Acceptor atoms with one fewer valence

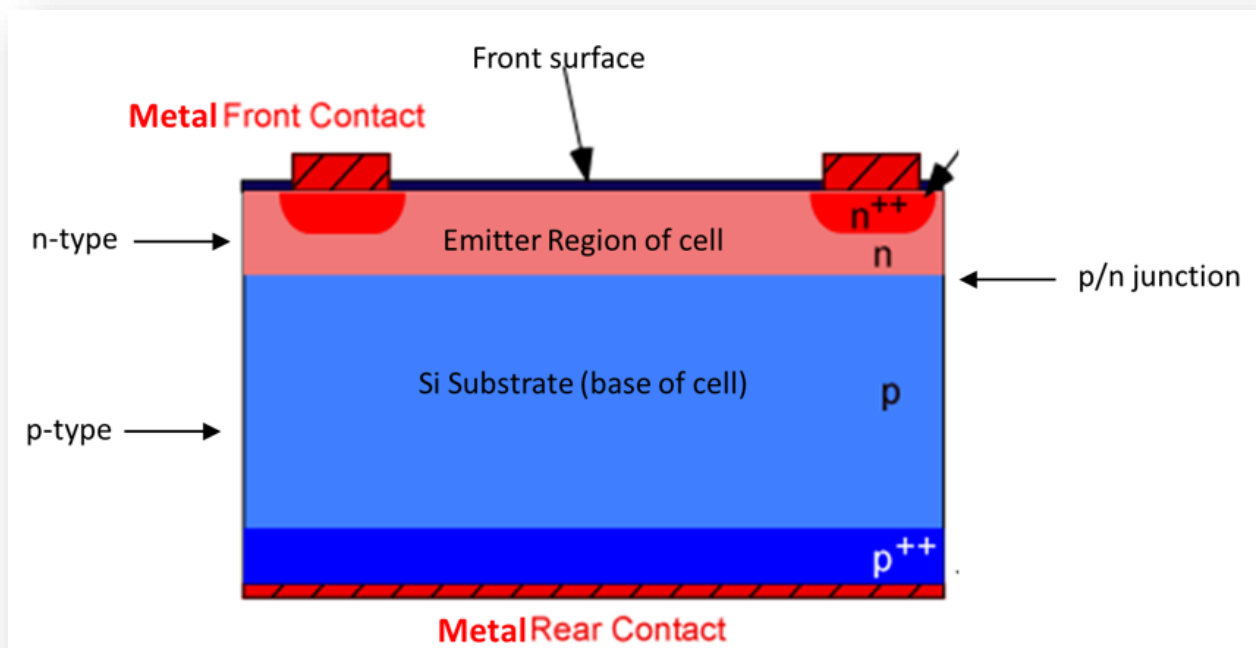
electron result in “P-type” material. In P-type material, the number of electrons missing from covalent bonds is higher, thus effectively increasing the number of free holes (positively charged carriers). In doped material, there is always more of one type of carrier than the other and the type of carrier with the higher concentration is called a “majority carrier,” while the carrier with lower concentration is called a “minority carrier.”

C. Annealing

29. Annealing is a general term for a process during which the atoms of a material are given enough time and thermal energy to find and relax into their lowest energy state.

D. Solar Cell Structure

30. According to the '516 patent, a solar cell has a “front side” that “faces the sun during normal operation to collect solar radiation.” Ex. 1001, 1:32-34. Opposite the front side is the backside. *Id.* at 1:34. This is illustrated in the following diagram of a generic solar cell.

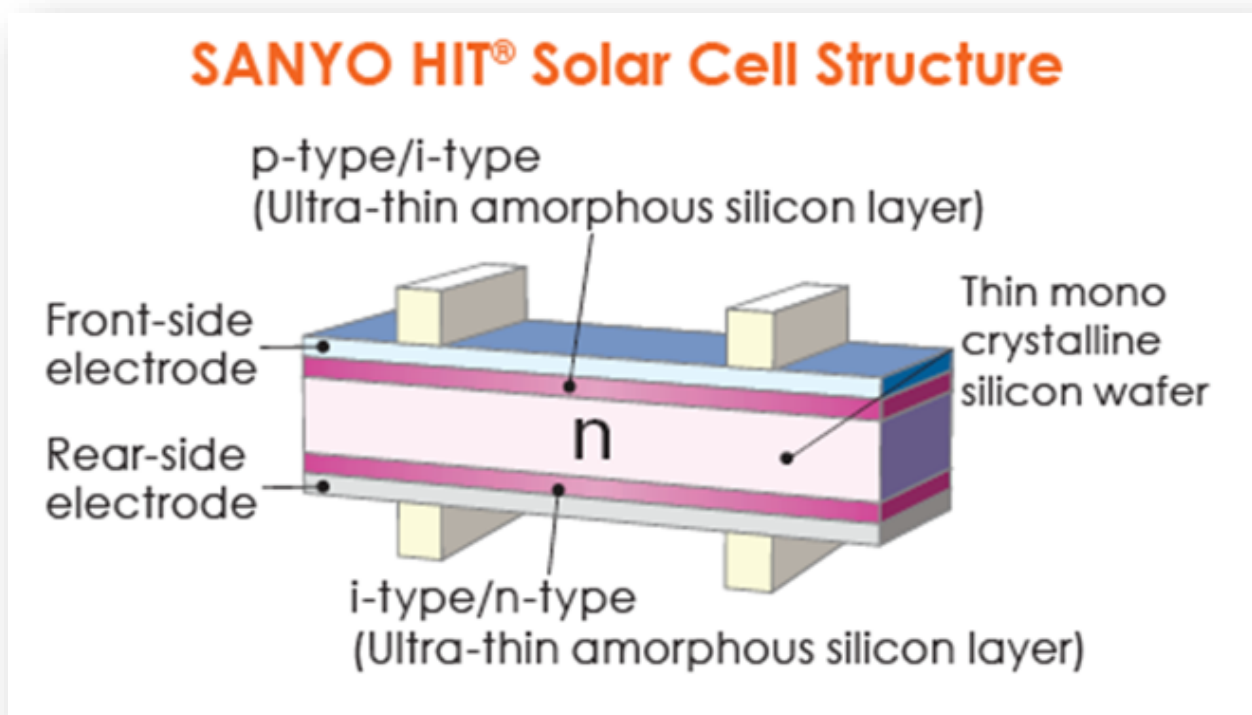


1. Junctions

31. A junction is a general term for a region of a semiconductor device where the properties of the material on one side are dissimilar in some way from those on the other side. These can include homojunctions where the two regions are each made of the same material but have different electrical properties, or heterojunctions where the two regions are actually made of different materials with differences in crystal structure, chemical composition, bandgap, or other molecular properties. Claim 9 in '516 patent recite forming a poly-Si layer on a Si substrate. This material discontinuity constitutes a heterojunction.

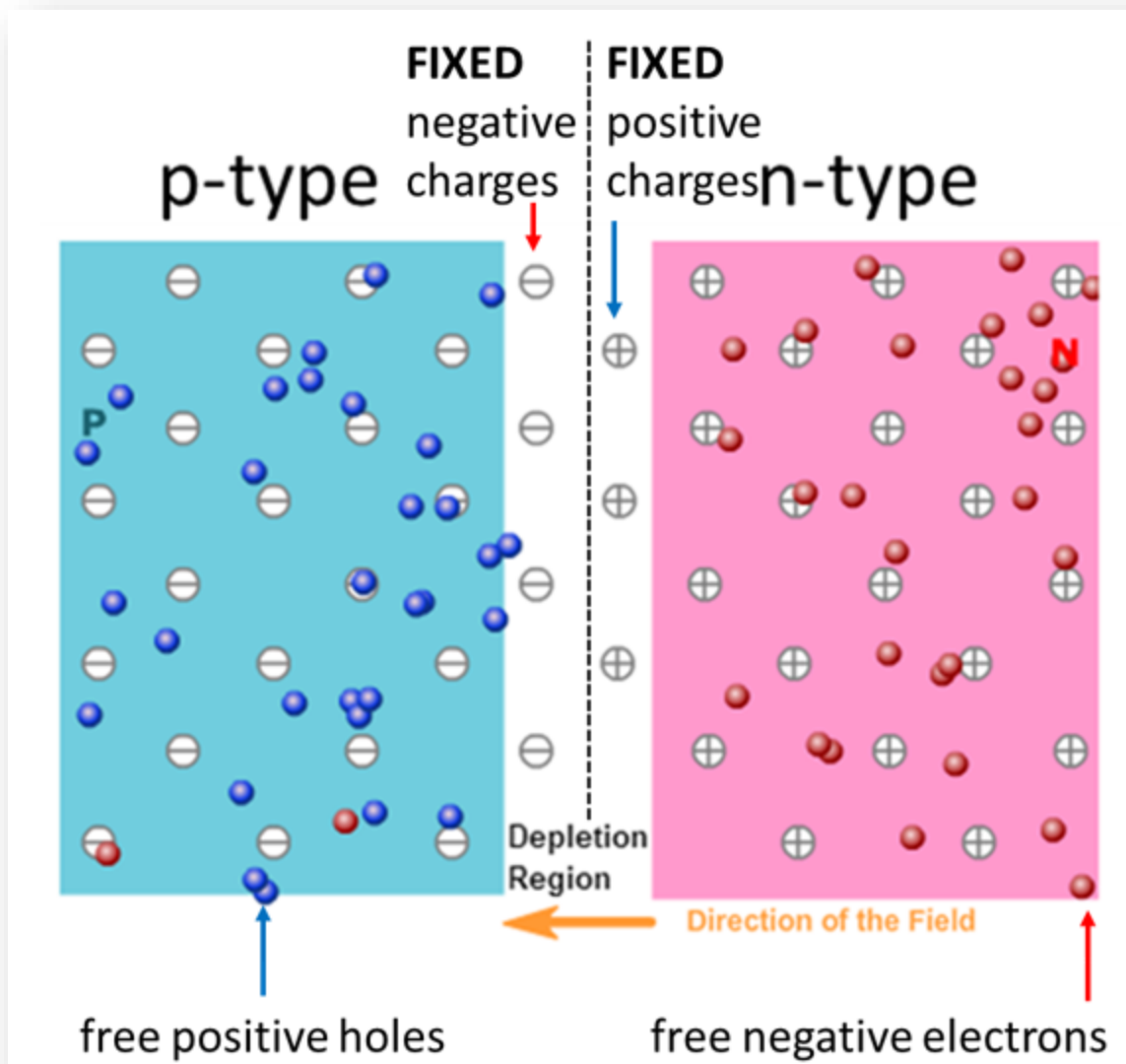
a. Heterojunction

32. As noted, a heterojunction is formed by joining of dissimilar materials in contact with a semiconductor substrate. This can be a poly-Si layer, as in the '516 patent, or an amorphous Si (a-Si) layer as shown below in the famous heterojunction cell invented by Sanyo Corporation. It is the abrupt change in material properties between the c-Si and the a-Si which lead to the excellent performance of this type of solar cell, which held the world record for energy conversion efficiency for many years.



b. P-N Junction

33. An example of a P-N junction is that region of a solar cell where a P-type Si base adjoins directly with an N-type emitter region. This can be created by heavily doping a P-type Si substrate with N-type dopant atoms until a shallow layer of N-type Si is formed near the surface of the substrate. Since the N-type region has a high electron concentration and the P-type a high hole concentration, electrons diffuse from the N-type side to the P-type side and holes flow by diffusion from the P-type side to the N-type side. Diffusion in semiconductors is the motion of charge carriers due to their concentration gradient.



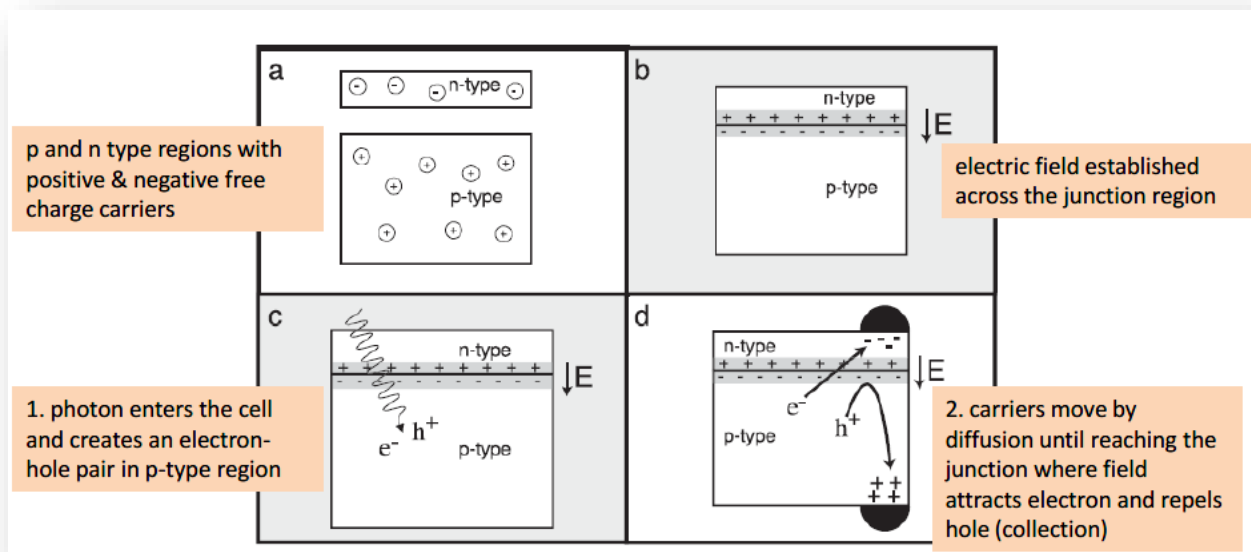
34. After the electrons and holes move to the other side of the P-N junction, they leave behind exposed charges on dopant atom sites, which are fixed in the crystal lattice and are unable to move. On the N-type side, positive ion cores are exposed with donor charge density N_D . On the P-type side, negative ion cores are exposed with acceptor charge density N_A .

35. A built-in electric field $\hat{E}$ forms between the positive ion cores in the N-type material and negative ion cores in the P-type material. This region is called the "depletion region" since the electric field there quickly sweeps any free carriers across, hence the region is depleted of free carriers. This region extends further into the more lightly doped side to expose an equal number of fixed ion cores as on the more heavily doped side.

36. A solar cell absorbs light to generate electric power. This is a three-step process: First, it absorbs as much sunlight as possible through the front side of the solar cell to photogenerate electrons and holes. In a doped region, the increase in photogenerated majority carriers is just a tiny fraction of the majority carriers already present, so these have little effect.

37. Second, since the photogenerated minority carriers represent a large increase in the number of minority carriers present, the process of diffusion of these minority carriers towards the depletion region at the P-N junction naturally takes place. These minority carriers diffuse a distance of what is called the minority carrier diffusion length, which is the average distance they can diffuse before recombining during the average minority carrier lifetime.

38. Third, the electric field present at the junction then sweeps the minority carriers across, at which point they are collected and simply need to pass through contacts into the external circuit.



39. As shown above, in box (a), the basic structure of a solar cell may include an N-type region with negative free charge carriers on the front side, and P-type region with positive free charge carriers on the backside.

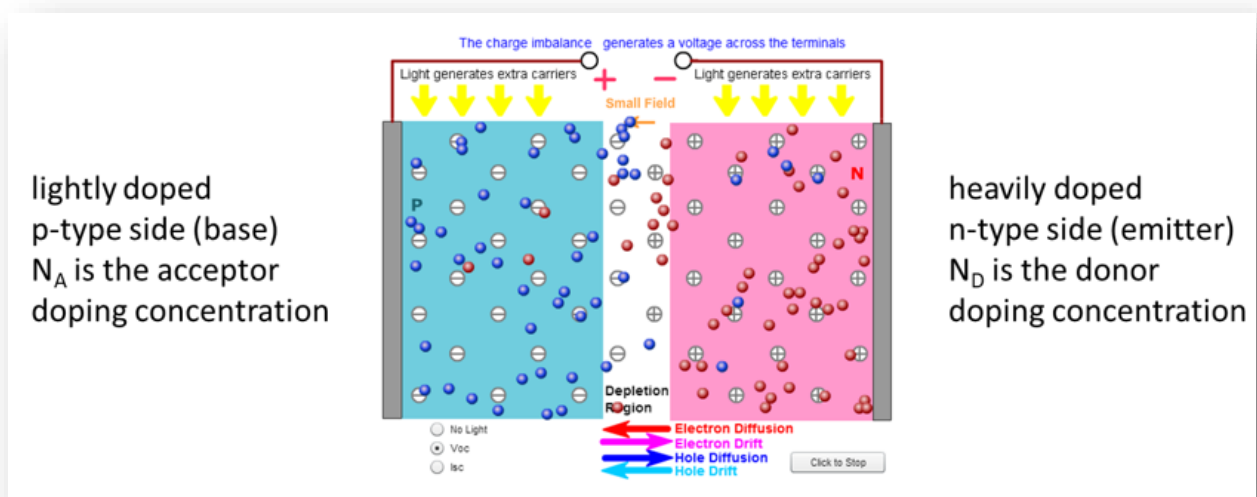
40. In box (b), a built-in electric field is shown to be established across the P-N junction region.

41. In box (c), upon absorbing sunlight, a photon enters the solar cell. If the photon has an energy greater than that of the band gap, an electron-hole pair can be photogenerated, in this instance, in the p-type region.

42. In box (d), the minority carrier electrons move by diffusion until reaching the P-N junction region where they are swept across by the built-in electric field there. Specifically in the case shown here, the electron is swept across the junction and becomes a majority carrier in the N-region where it can then no

longer recombine since there are so few holes present there. The photogenerated hole is repelled by the junction electric field and increases the majority carrier hole concentration slightly in the P-region. This buildup of charged majority carriers creates a voltage across the P-N junction. If an external circuit is present, these excess majority carriers can be pushed through low-resistance metal contacts, thereby generating a negative photocurrent in the circuit and delivering electric power.

43. To generate power, a voltage must be generated as well as a current. If light-generated carriers are prevented from leaving the solar cell (such as in the case of an open-circuit shown below), the number of electrons on the N-side and holes on the P-side increase. This creates an electric field at the P-N junction opposite to the built-in field.



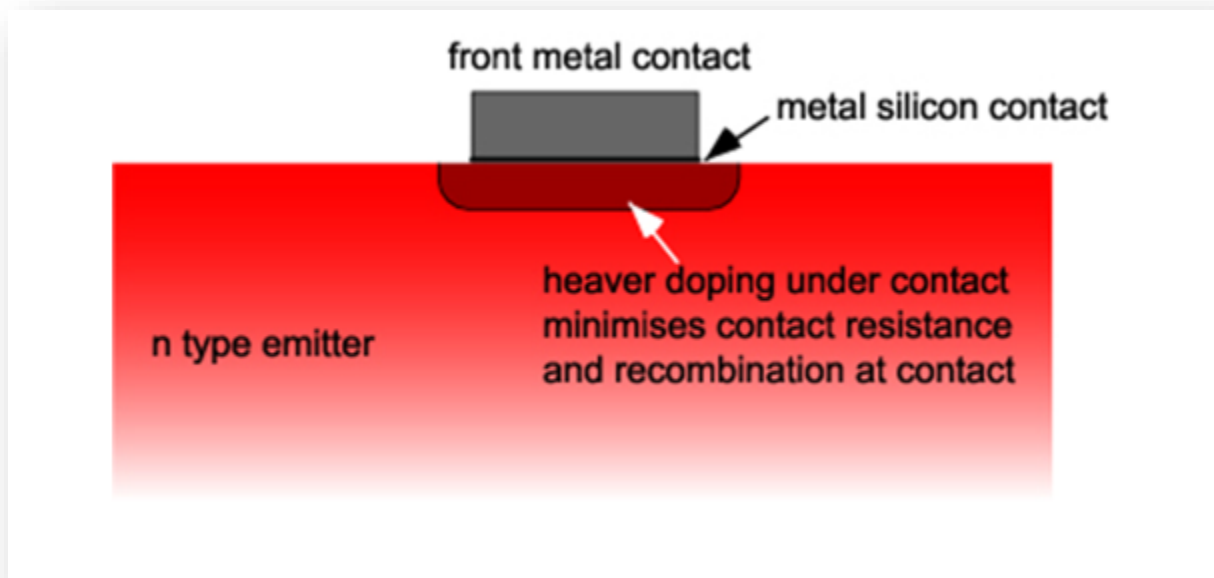
44. This forward voltage across the junction creates a forward bias current, which exactly balances the negative photogenerated current, so the net current is zero at open circuit. The voltage to cause these two currents to exactly balance is called the “open-circuit voltage.” In actual operation, the voltage across the cell is maintained at a slightly lower value so that current can be delivered to an external circuit at the maximum power point. These operating parameters are known as the max power voltage and max power current.

45. The above discussion assumes a P-type substrate doped with N-type dopants to form the emitter. A P-N junction can also be formed with “a P-type polysilicon emitter formed over [an] N-type silicon substrate.” Non-asserted claim 1 of the ’516 patent is directed to such a junction structure. Ex. 1001, 6:12-14. Moreover, as recited in claim 9, providing “an emitter layer formed over a back surface of [a] substrate” also forms a junction, *i.e.*, a heterojunction. *Id.* at 6:46-48.

2. *Emitter*

46. In a semiconductor device, the emitter of the device is usually defined as the region which is doped to have the opposite majority carrier polarity compared to the substrate. However, as in claim 9 of the ’516 patent, the emitter can be a polysilicon layer on the back side of the substrate. Ex. 1001, 6:46-48.

3. *Contacts*



47. The contacts of a solar cell are metal regions deposited on the cell surface intended to conduct the photogenerated current from the semiconductor to an external circuit.

E. Types of Solar Cells: One Sun and Concentrator Solar Cells

48. Solar cells designed for use on earth rather than in outer space are called terrestrial cells as opposed to space cells. Terrestrial cells can be further divided into cells designed to use normal sunlight (one-sun cells) and those designed to use concentrated sunlight (concentrator cells).

49. The distinguishing characteristic of concentrator cells is that they generate many times more free carriers than one sun solar cells do, requiring

concentrator solar cells to have a much lower series resistance from the substrate through the emitter, contacts, and gridlines than in a one sun solar cell.

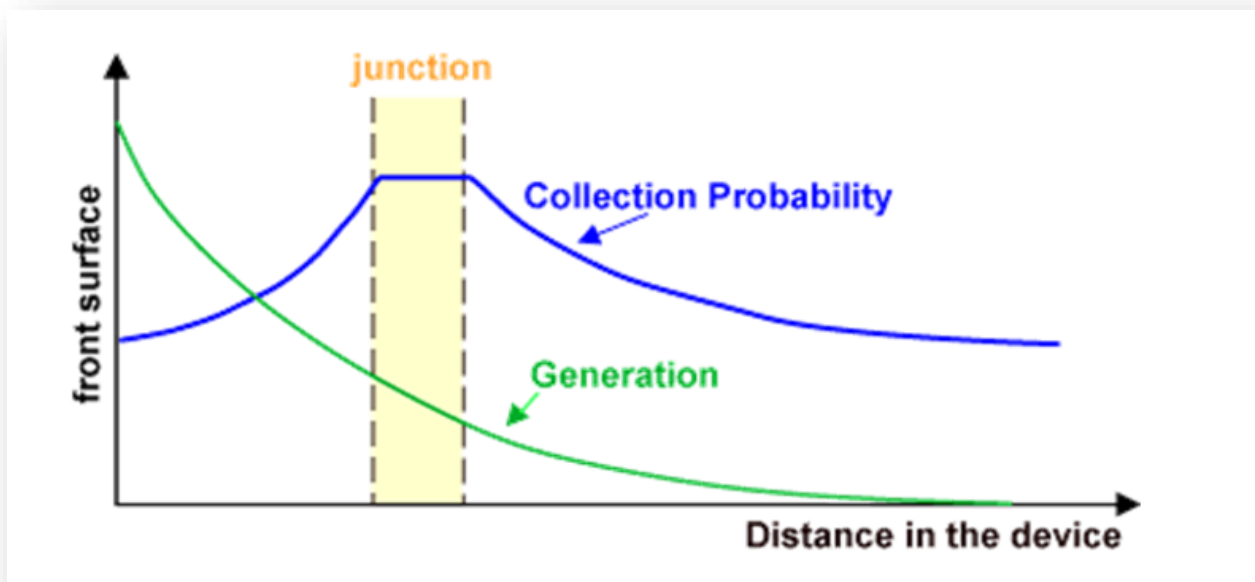
50. In particular, the contact resistances must be much lower than those of one-sun cells, and the metal gridlines are usually much thicker to reduce gridline resistance.

F. Solar Cell Efficiency

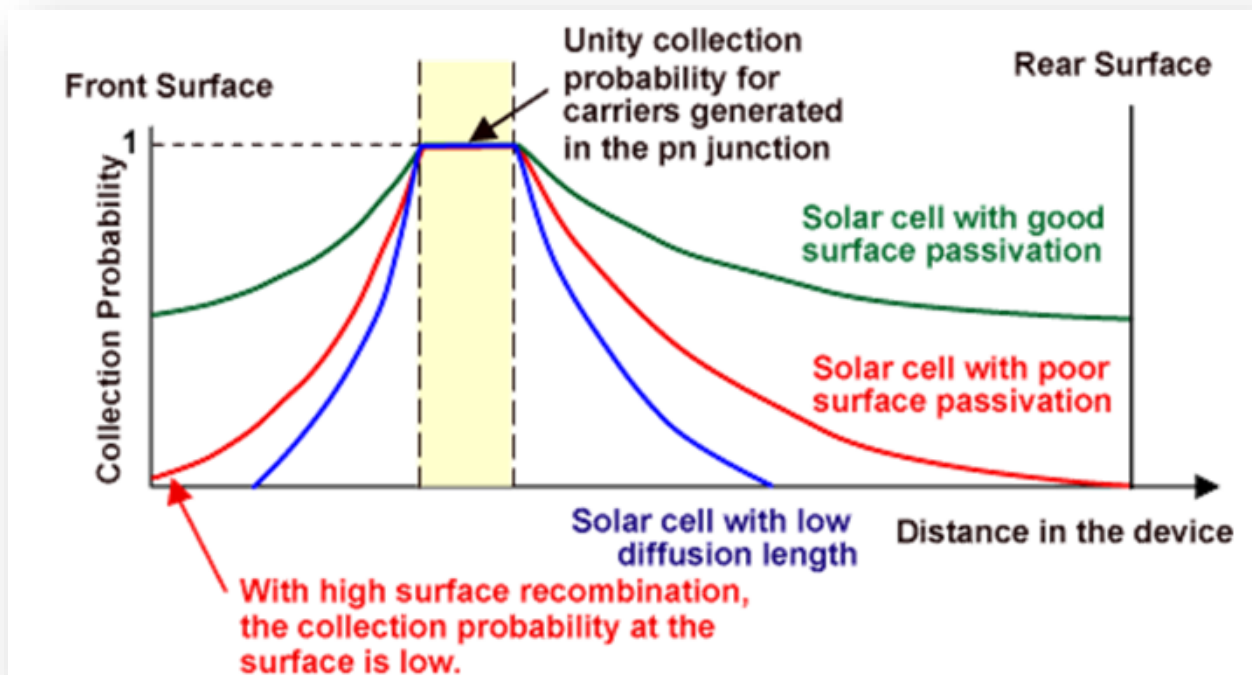
51. The overarching goal of the solar cell industry is to increase the efficiency of the solar cell, which is the ratio of electrical power output at the max power point to the photo power incident in the incoming sunlight. This is achieved by maximizing light absorption, reducing photocarrier recombination to increase current and voltage, and maintaining low electrical resistance within the cell.

1. Recombination and Passivation

52. The free electrons photogenerated by absorbed sunlight can recombine with any free holes present by falling back into the covalent bond vacancies, in which case neither free carrier can contribute to conduction any longer. Most photogeneration takes place close to the front surface of the cell where the light is mainly absorbed. The probability that photocarriers will be collected by the junction decreases with distance from the junction.

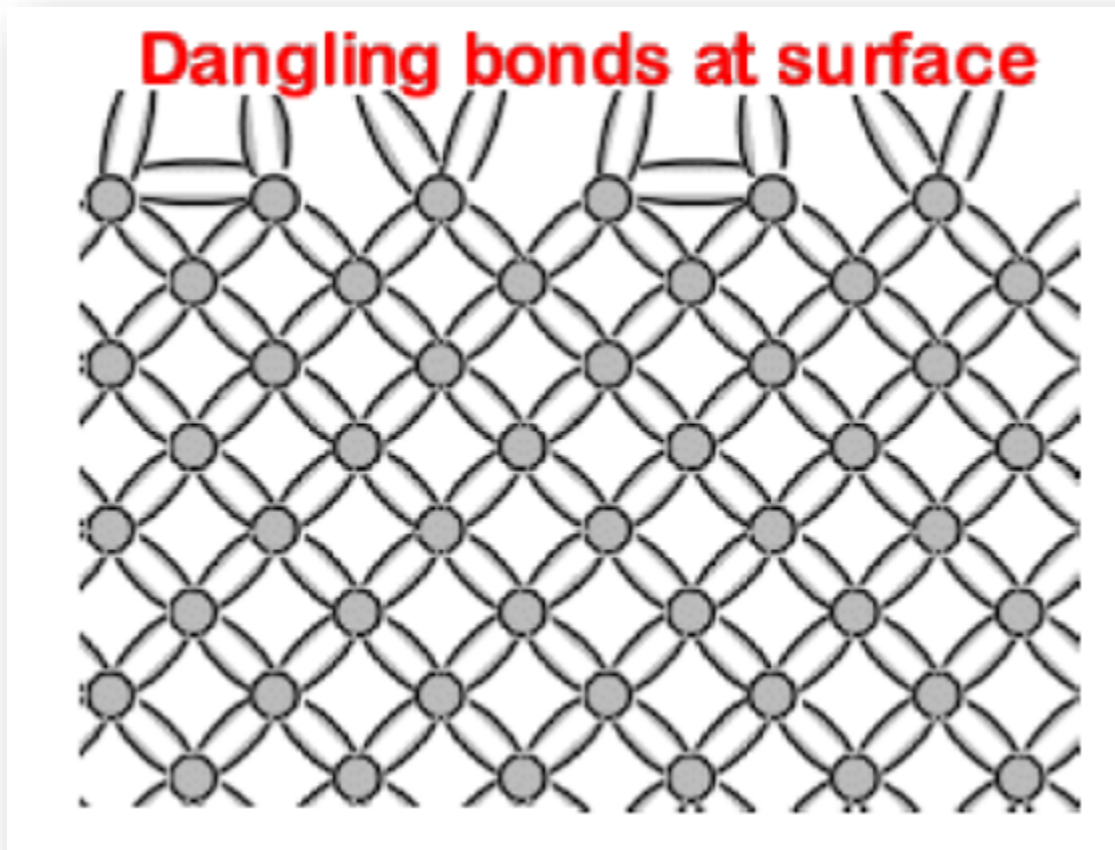


53. The mean time that free carriers exist before recombination is called the minority carrier lifetime. The distance they can diffuse during this time is called the minority carrier diffusion length. This is sometimes measured as a saturation current density called J_0 . The goal of effective solar cell design is to minimize this recombination by maximizing carrier lifetimes and diffusion lengths, thereby keeping J_0 low.



54. Defects at either surface of the semiconductor wafer or impurities within it increase the level of recombination occurring in each of these areas, thereby decreasing the concentration of photogenerated carriers available to generate current and voltage. Each of these regions can be characterized by its own J_0 value, which all add together to determine overall cell efficiency. Effective solar cell design implements the invention and inclusion of critical features to reduce the amount of recombination occurring at surfaces, which is known as surface passivation.

55. The surface of a solar cell represents a severe disruption of the periodic crystal lattice, and these surfaces of the solar cell are a site of particularly high recombination unless they are effectively passivated.



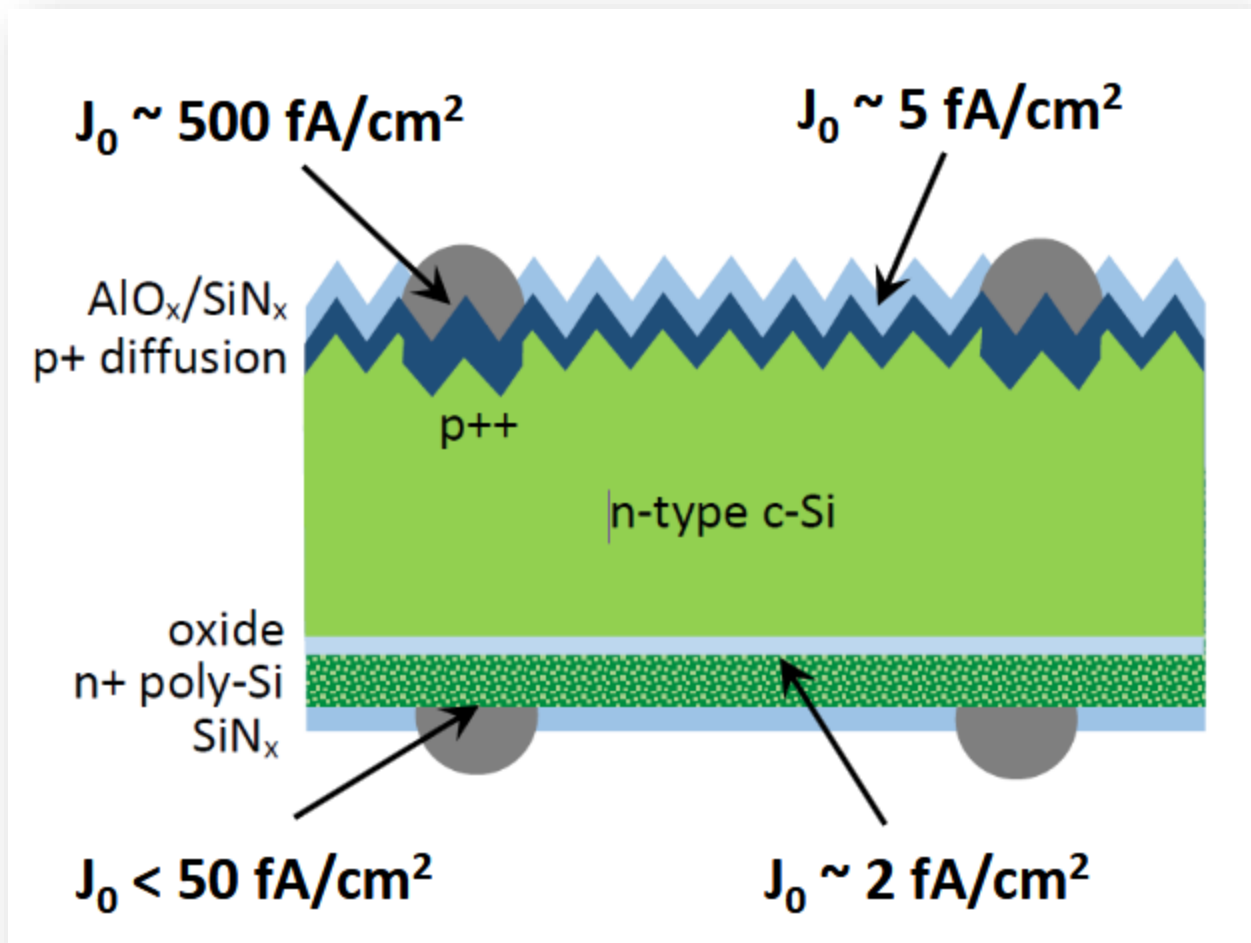
56. The defects at a semiconductor surface are caused by the interruption to the periodicity of the crystal lattice, which causes dangling bonds to form at the semiconductor surface where high levels of recombination can occur. The high recombination rate in the vicinity of a surface reduces the concentration of minority carriers in this region.

57. The reduction of the number of dangling bonds, and hence surface recombination, is often achieved by carefully growing a matching layer on top of the semiconductor surface, whose chemical structure is perfect for tying up some of these dangling bonds. This reduction of dangling bonds is known as surface passivation. Thermally grown silicon dioxide (SiO_2) is an excellent match for passivating Si surfaces. This oxide is carefully grown at high temperatures in a clean environment containing only oxygen and possibly some inert gas. This thermal oxide needs to be differentiated from the many other types of oxides that can be found on Si surfaces, such as chemical oxides produced at room temperature.

58. The amount of recombination can be quantified by measuring J_0 , which represents recombination in a region of the cell, and is related to the voltage a cell can deliver. Specifically, it is related to the mean lifetime of minority carriers before they recombine. A low J_0 indicates less recombination. This means that more carriers migrate outside the cell and deliver useable power, thereby increasing cell conversion efficiency.

59. A good TOPCon one sun cell, shown in the literature in 2023, such as the one shown by MacDonald in Figure 1 below has rear surface J_0 of $2 \text{ fA/cm}^2 = 2 \times 10^{-15} \text{ A/cm}^2$. This is about 5-30 times lower than that of the concentrator cell, which is the subject of Kwark's experiments (discussed below), and 10-25 times

lower than the results of Gan's experiments. Gan is also directed to a concentrator cell.

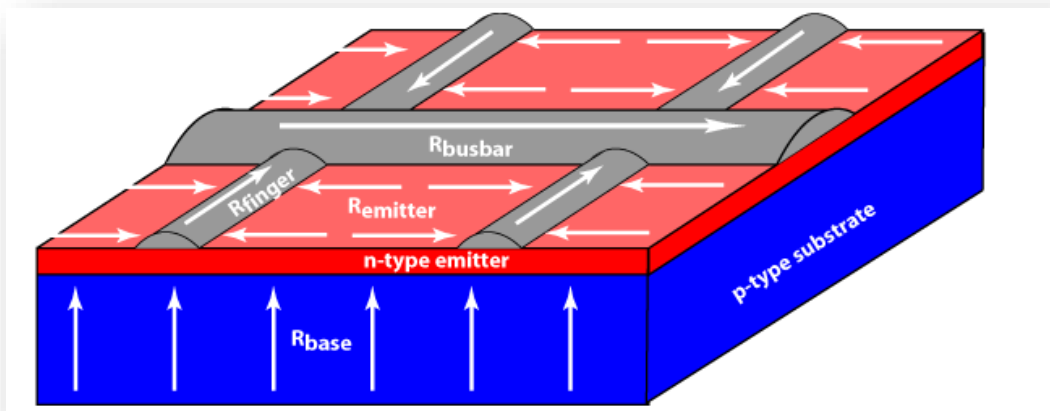


D. MacDonald, Achieving 26% silicon solar cells in mass production with passivating contacts – TOPCon or heterojunctions? Australian National University, UNSW School of Photovoltaic & Renewable Energy Engineering (Sept. 2023) (<https://www2.pv.unsw.edu.au/videos/Daniel-Macdonald-7September2023/slides/UNSW-SPREE-seminar-Sept-2023-DanM.pdf>).

2. Resistance

60. Series resistance in solar cells reduces their efficiency by dissipating power in the cell that would otherwise be delivered to an external circuit. The most common parasitic resistances are series resistance and shunt resistance.

61. Series resistance in a solar cell has three causes: (1) the movement of current through the emitter and base of the solar cell; (2) the contact resistance between the metal contacts and the substrate; and (3) the resistance of the top and rear metal contacts. The diagram below illustrates the components of series resistance:



62. The metallic top contacts are necessary to collect the current generated by a solar cell. “Busbars” are connected directly to the external metal ribbons in a solar panel, while “gridline-fingers” are fine areas of metallization which collect current for delivery to the busbars. A tradeoff is made by having

sufficient metal coverage to reduce series resistance without shading too much of the cell, which reduces the capture of sunlight and, therefore, reduces current.

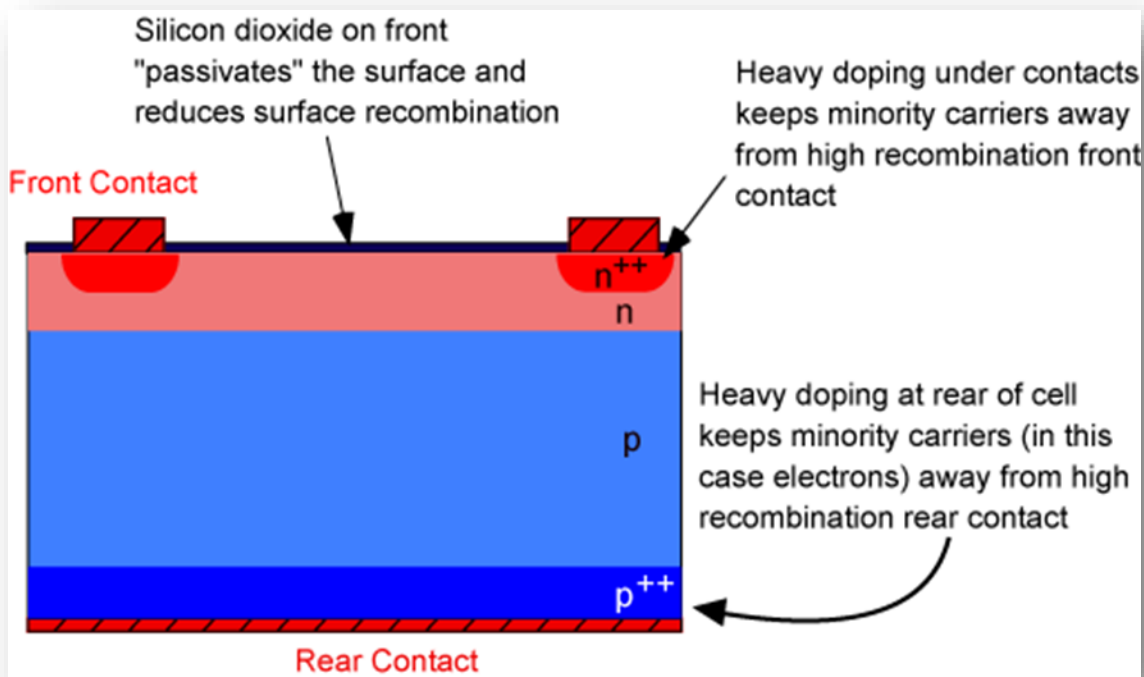
63. Series resistance due to contacts can be quantified as ρ_c , which represents the contact resistivity of any contact of a given area and is due to forcing the current from the Si to the metal of the contact. It is measured by sending current through the contact, and measuring the voltage across the contact for various values of the current, or measuring the resistance of contacts of different areas, using Ohms Law, *i.e.*, $R=V/I$.

64. A high ρ_c results in excessive loss of power and lower efficiency. Total series resistance for one-sun cells such as described in the '516 patent typically needs to be less than 1 ohm-cm². Back contact resistance typically makes up about 1% of this, so it should be less than 1×10^{-2} ohm-cm². This is only one component of total series resistance, and all need to be optimized simultaneously along with allowing maximum light collection at the front surface to maximize cell efficiency. This involves several tradeoffs and careful optimization.

65. Series resistance is particularly problematic for concentrator solar cells. Concentrator solar cells use external optics to concentrate high intensity sunlight on a cell front surface resulting in much higher current generation. Due to Ohm's law, higher currents make it necessary to significantly reduce series resistance to keep voltage losses low. Simply put, the high level of current

generated in concentrator cells increases the losses due to series resistance proportional to the ratio of the concentration intensity. For so-called concentrator cells, the series resistance needs to be made lower by the same ratio as the solar concentration ratio. For this reason, concentrator cells have a very different metal gridline structure than that of the one-sun cell shown above. Using the example of acceptable contact resistivity for one-sun cells mentioned above, back contact resistivity for a concentrator cell operating at 100 suns concentration should be less than 1×10^{-4} ohm-cm².

66. A commonly used method to reduce contact resistivity is to selectively provide especially heavy doping concentration in emitter regions of the cell that are in direct contact with the metal contacts. This not only reduces contact resistivity, but also produces a slight electric field between the heavily doped region and the more lightly doped regions of the cell, which repels some of the minority carriers away from the metal contacts where they would otherwise certainly recombine.



67. This method of surface and contact passivation is known as field effect passivation because the weak electric field between the heavily and lightly doped regions does introduce a small barrier to minority carriers. The minority carrier concentration is then maintained at higher levels in the base region.

G. Solar Cell Design Principles

68. For one sun silicon solar cells, the design constraints caused by surface reflection, carrier collection, recombination, and resistance result in a maximum device efficiency of about 26%. To optimize solar cell performance, each objective must be pursued concurrently.

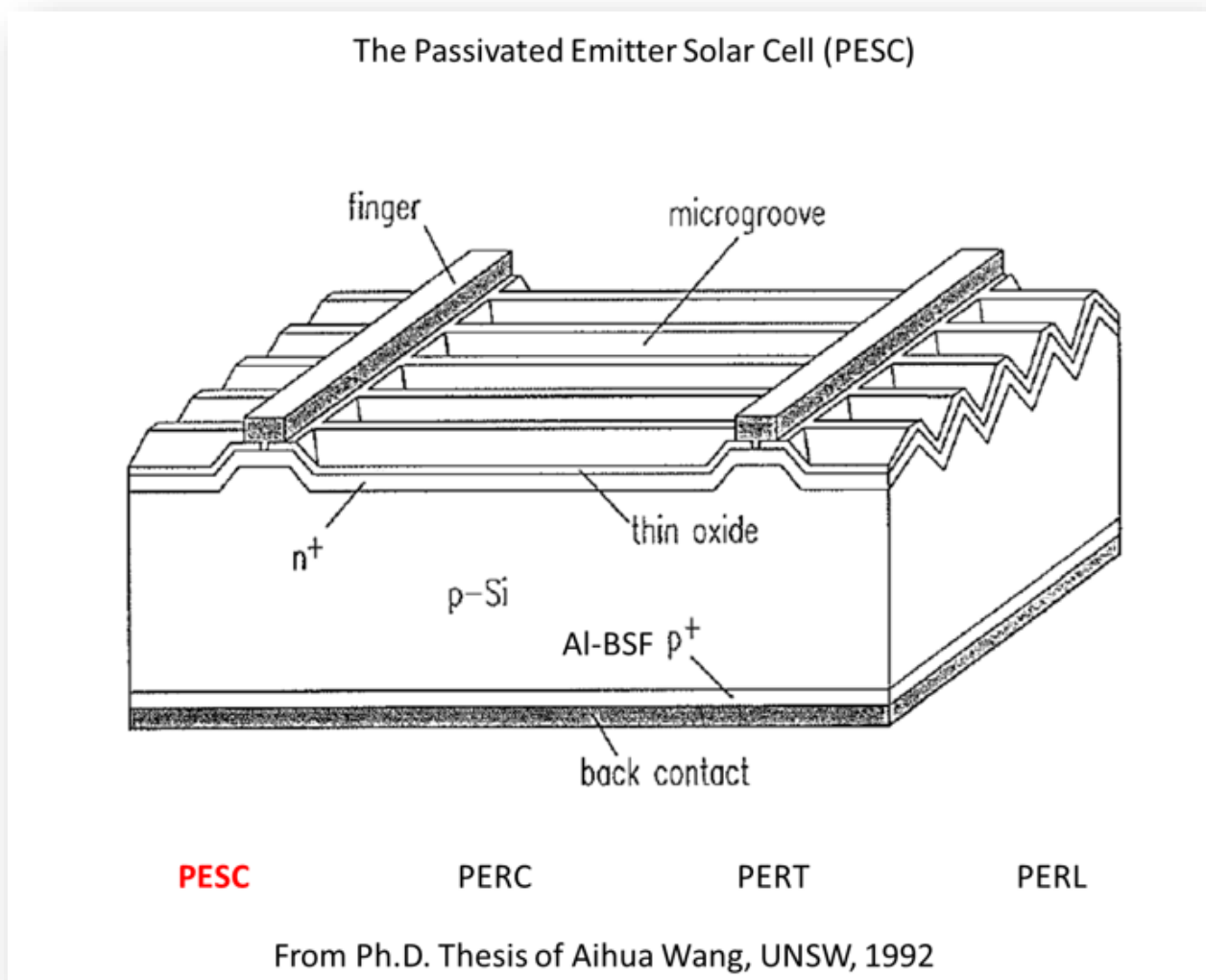
- Maximize the absorption of light and the generation of free carriers;

- Optimize collection of the photocarriers to deliver a current;
- Minimize recombination to generate a larger voltage; and
- Minimize dissipation of power in parasitic resistances.

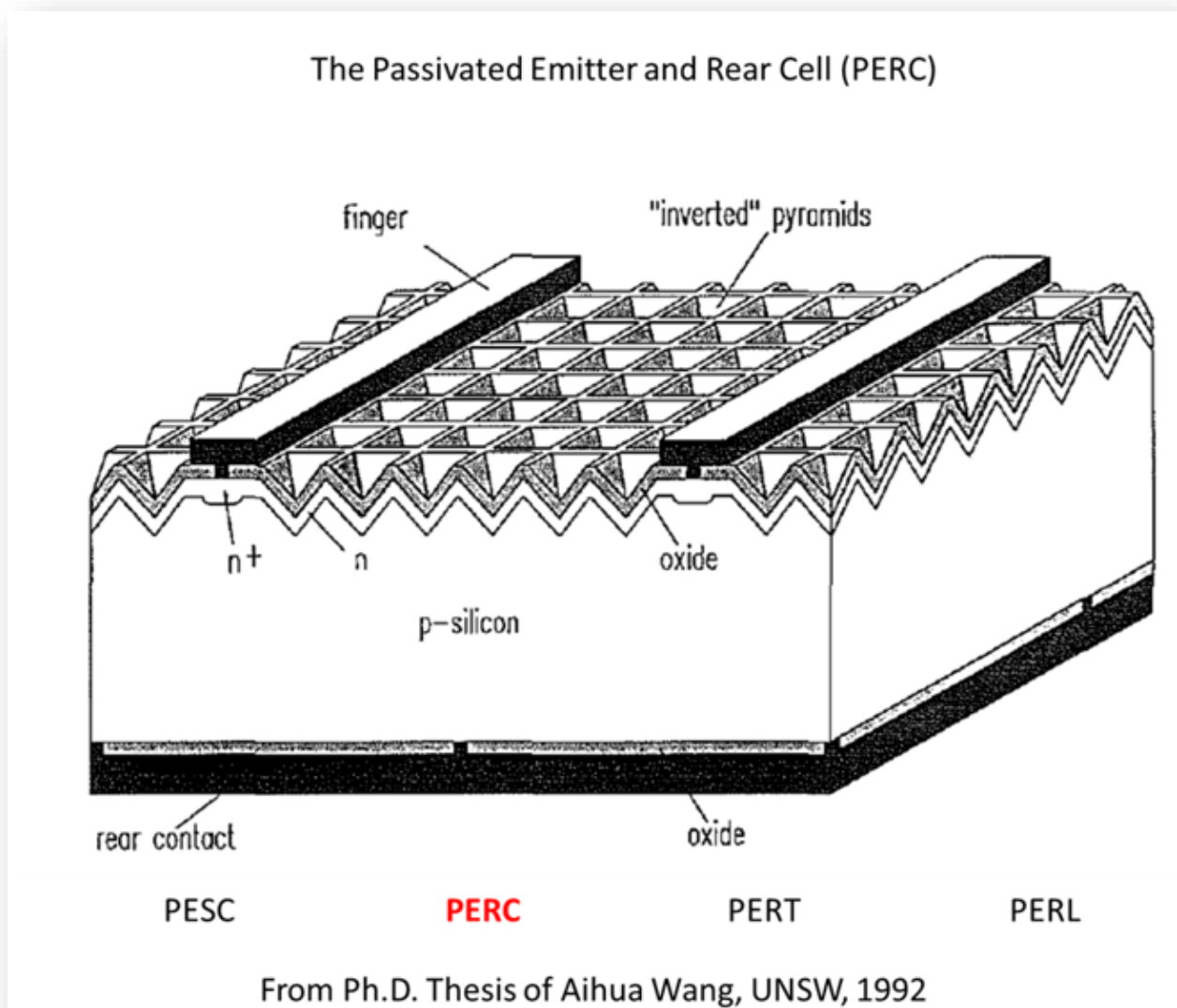
69. The '516 patent describes the process for making a solar cell that addresses improvements pertaining to the last two of these points, reducing recombination and parasitic resistance by reconfiguring the back surface of the cell to substantially reduce recombination there while still allowing the current to pass to the metal contacts with acceptably low resistance. This is done using a new method for back surface design by introducing two elements on the back surface and forming a heterojunction comprised of a tunnel oxide layer and a heavily doped polysilicon (poly-Si) layer.

1. Passivated Emitter Solar Cells

70. Prior to the introduction of TOPCon solar cells, the most prevalent type of Si cells commercially produced were of the PESC, PERC or PERT type. The PESC (Passivated Emitter Solar Cell) was primarily focused on passivating the front emitter of the cell where most of the photogeneration takes place. A simple rear heavily diffused region using alloyed Al formed the back contact with a Back Surface Field (BSF).

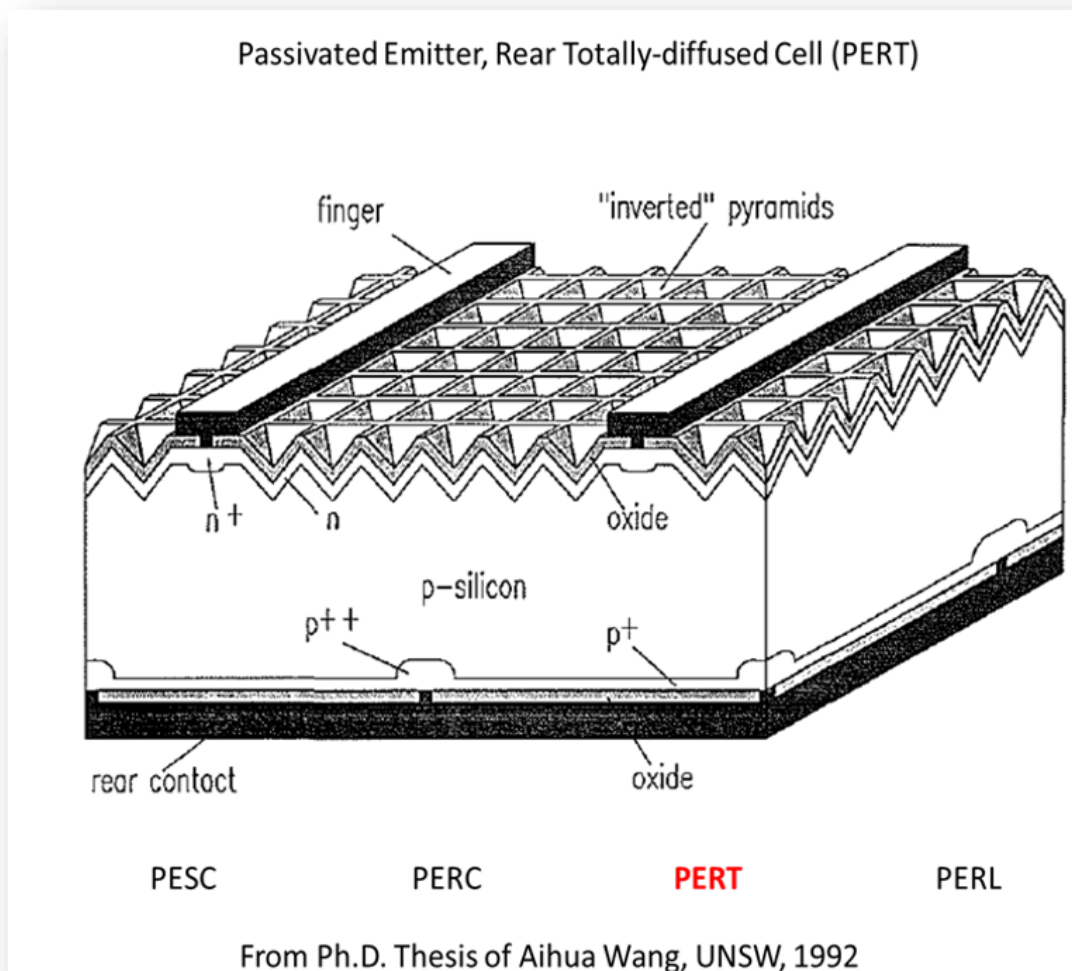


71. The PERC (Passivated Emitter and Rear Cell) was the next historical improvement in solar cell technology. This cell used a high-quality thermal oxidation on the rear of the cell to passivate most of its surface far more effectively than a simple Al-alloyed BSF was able to achieve. However, small holes had to be formed in this passivating oxide layer in order to make low-resistance contact to the metal beneath.



72. Eventually, cell producers were able to get even better results by using an additional doping diffusion on the back surface specifically to get better BSF passivation there. The PERT (Passivated Emitter and Rear Total area diffused) included a dopant-diffused region over the entire rear surface to get better passivation than using a back-surface oxide alone. It also included an extra-heavy diffusion over the regions near the metal contacts for lower contact resistance and

improved contact passivation. These cells still required the penetration of the passivating oxide layer in order to open conducting paths to the rear metal contacts.

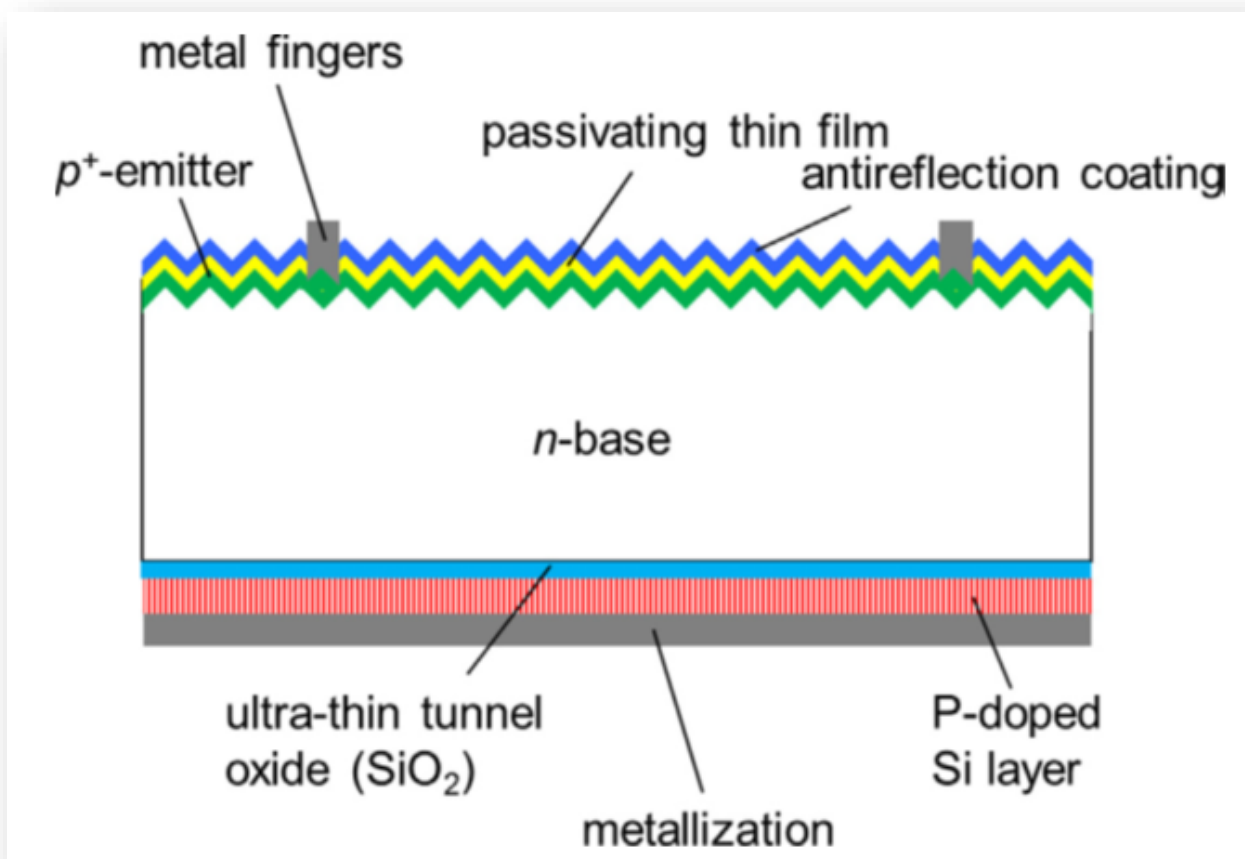


73. This is where the technology stood for many years until the invention of the TOPCon cell (Tunnel Oxide Passivated rear Contact).

2. TOPCon Solar Cells

74. The term TOPCon was coined by researchers at the Fraunhofer Institute for Solar Energy Systems (Fraunhofer ISE) in 2013. *See, e.g., Ex. 2010* (Feldmann, et al., “A Passivated Rear Contact for High-Efficiency N-Type Silicon Solar Cells Enabling High VocS and FF > 82%” (28th European PV Solar Energy Conference & Exhibition, Paris, Sept. 30 – Oct. 4, 2013)).

75. Exhibit 2010 includes the Figure below:



TOPCon cell (Tunnel Oxide Passivated Rear Contact).

76. In this cell design, the back heavily diffused c-Si region of the PERT cell has been replaced by two layers: an ultra-thin tunnel oxide and a deposited phosphorus-doped N-type poly-Si layer.

a. Tunnel Oxides

77. Tunnel oxides are high-quality SiO₂ layers that are extremely thin, about 1.5nm, just about three atomic monolayers that cover the entire back side surface of the substrate. They are so thin that due to alignment of Si-SiO₂ bandgaps, majority carriers in the Si (the same polarity as the n-type substrate -- electrons in this case) can pass through them with very low resistance, while minority carriers (holes) are nearly all blocked. This significantly reduces the number of minority carriers in the poly-Si and at the metal contacts and suppresses recombination there. The high quality of the tunnel oxide layer (no dangling bonds or impurities) keeps recombination at the c-Si-SiO₂ interface low.

78. Tunneling can take place when the wave function of the electrons penetrates the oxide layer according to quantum theory. This can only occur to a substantial degree when the oxide layer is less than 2 nm.

79. Quantum tunneling enables majority carrier movement across the interface and almost completely blocks minority carriers. Due to its thinness, electrons can “tunnel” through the oxide layer rather than being blocked like the holes are.

80. The tunneling mechanism is described in U.S. Patent Pub. No. 2002/0142500 to Foglietti. Ex. 1042. Although Foglietti relates to bipolar transistors, the tunneling mechanism it describes also applies to solar cells.

81. According to Foglietti, interfacial oxides (tunnel oxides) are “generally less restrictive with respect to majority carriers (electrons) moving from the emitter region of the transistor into the base region than minority carriers (holes) moving from the base region into the emitter region. This phenomenon is due to the tunneling probability of electrons being greater than the tunneling probability of holes.” Ex. 1042, ¶3.

82. According to Foligetti, the majority carrier “can tunnel through the interfacial oxide, Ex. 1042, ¶4, whereas holes are blocked from passing the interfacial oxide, *id.* at ¶5. Thus, Foglietti concludes, “under appropriate circumstances,” interfacial oxides (tunnel oxides) “may be modeled as a selective diode . . . wherein the electrons [] see a forward biased, conductive path, and the holes [] see a reverse-biased, non-conductive path.” *Id.* at ¶5. This tunneling mechanism improves transistor gain in Foglietti’s system. *Id.* at ¶¶4-5.

83. Notably, Foglietti specifies this improvement (provided by tunneling) “is substantially dependent upon various properties of the interfacial oxide.” Ex. 1042, ¶6. For one, the interfacial oxide (tunnel oxide) cannot be “too thick,” otherwise “the number of electrons which can tunnel through from the emitter into

the base is reduced substantially.” *Id.* On the other hand, the interfacial oxide (tunnel oxide) cannot be “too thin,” otherwise “an insufficient barrier exists to block the hole current.” *Id.*

84. Moreover, the interfacial oxide (tunnel oxide) must also maintain integrity:

For example, since the interfacial oxide is subject to various types of subsequent thermal processing (e.g., subsequent poly CVD processing, metal deposition, anneal steps, etc.), the interfacial oxide may lose its integrity, that is, the oxide may exhibit non-uniform characteristics spatially thereacross which in some cases may negatively impact the transistor performance. For example, if the interfacial oxide is fractured or becomes discontinuous, resulting in oxide islands, such fractures will be random and not repeatable from device to device; consequently, such fracturing causes unreliable transistor gain performance.

Ex. 1042, ¶7.

b. The Polycrystalline Silicon Layer

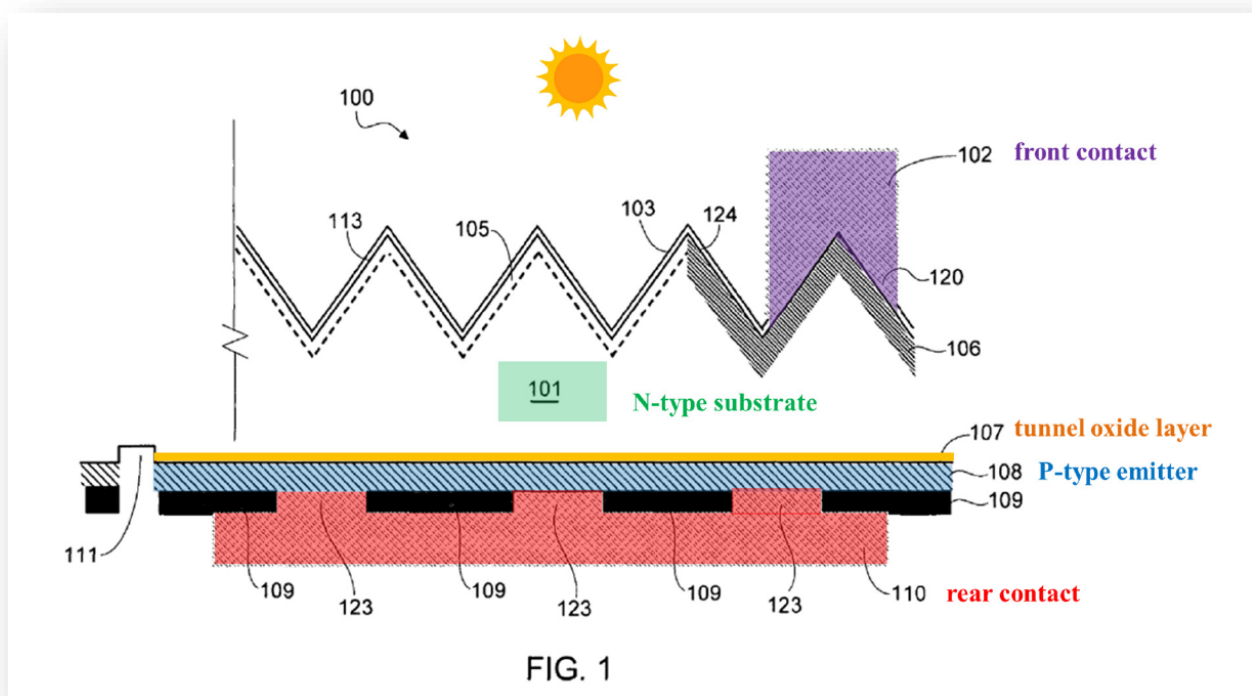
85. In a TOPCon structure, a layer of polysilicon heavily doped with N-type dopants is formed on the tunnel oxide. Polycrystalline silicon consists of many small, randomly oriented Si crystals. However, the band gap remains roughly the same as that of c-Si. The combination of a tunnel oxide and a doped

polycrystalline silicon layer provides excellent passivation and carrier selectivity on the N-type substrate.

VII. THE '516 PATENT

86. The '516 patent discloses and claims a novel front contact solar cell with former emitter. Ex. 1001, Title.

87. The '516 patent describes, with reference to Fig. 1, a cross-section of a solar cell in accordance with an embodiment of the present invention. Ex. 1001, 1:66-67.



Paper 3, 15 (citing Ex. 1001, Fig. 1) (annotation in Petition).

88. In this embodiment, an N-type silicon substrate 101 is formed from a crystalline silicon wafer. Ex. 1001, 3:50-54. The front side of the substrate is located at the top of Fig. 1 and faces the sun, the back side of the substrate is at the bottom of Fig. 1 and faces away from the sun. *Id.* at 2:27. A tunnel oxide 107, which can be silicon dioxide, is provided on the back side of the substrate 101. *Id.* at 3:62-66.

89. A layer of polysilicon 108 is deposited on the tunnel oxide layer 107 to form the polysilicon emitter 108. Ex. 1001, 3:66-4:2. A dopant source layer 461 (not shown in Fig. 1) is formed on the polysilicon emitter 108 (i.e., formed on the back side of the polysilicon emitter) and the dopant is later driven into the polysilicon with a drive-in step. *Id.* at 4:5-58. A capping layer 462 (not shown in Fig. 1) is formed over this dopant layer to keep the dopants from escaping during the dopant drive in process. *Id.* at 4:10-13. An edge isolation trench 111 is formed near the edge of the substrate 101 and is cut through the capping layer all the way through to contact a small area of the substrate 101. *Id.* at 4:20-27.

90. Exposed surfaces of the substrate 101 (on the front side) are etched to form pyramid 113 like structures. Ex. 1001, 4:28-33. This etching step removes the previously applied layers 401 and 402, as can be seen in Figs. 4D and 4E. An N-type dopant source 412 is formed on the textured surface of the substrate. *Id.* at 4:35-38. The N-type dopants from dopant layer 412 are then driven-in to the

substrate 101 forming N-type doping regions 105 and 106. This drive-in step also drives in the dopants from the doping source layer 461 into the back side of the polysilicon (polysilicon emitter 108), thus forming a **backside junction**. *Id.* at 2:28-31, 4:52-65. This drive-in step may be formed in-situ, which the patent explains is “a single manual (i.e., by fabrication personnel) loading of the substrate 101 in a furnace or other single chamber of multi-chamber processing tool.” *Id.* at 4:58-68. After this drive-in step, layers 461 and 462 become silicon dioxide layer 109 and the front side of the silicon becomes N-doped region 106. *Id.* at 4:58-65, 2:28-31. A thin thermal silicon dioxide layer 124 is provided as a passivation layer on the surface of the silicon substrate 101. *Id.* at 4:65-67.

91. An antireflective (also serving as a dielectric) coating of silicon nitride layer 103 is formed over the textured surface 113 after removal of the N-type dopant source layer 412. Ex. 1001, 5:20-26. A front contact mask is then provided on the silicon nitride layer 103 to create a pattern for forming contact holes 102. *Id.* at 5:28-32. A back contact mask 422 is used on the silicon dioxide layer 109 to create a pattern for the back side contact holes 123. The holes 102 and 123 are then etched away. *Id.* at 5:33-43.

92. A back side metal contact 110 is formed on the silicon dioxide layer 109 to fill the contact holes 123 and make electrical connection to the polysilicon emitter 108. Ex. 1001, 5:48-55. Finally, front side metal contact 120 is formed on

the silicon nitride layer 103 to fill contact holes 120 and make electrical connection to the substrate 101. *Id.* at 5:56-58.

93. While the above description may describe a solar cell with an N-type substrate and a P-type polysilicon emitter forming a backside junction, the patent claims are broader than that and can encompass an N-type crystalline substrate having an N-type polysilicon emitter forming a heterojunction, which is the “backside junction” of claim 9. This is shown in the below comparison of the independent claims 1 and 9 below.

Claim 1	Claim 9
1. A solar cell having a front side facing the sun to collect solar radiation during normal operation and a backside opposite the front side, the solar cell comprising: an N-type silicon substrate; a textured surface on the N-type silicon substrate on the front side of the solar cell;	9. A solar cell having a front side facing the sun to collect solar radiation during normal operation and a backside opposite the front side, the solar cell comprising: a substrate having a textured front surface;

Claim 1	Claim 9
an antireflective layer over the textured surface of the N-type silicon substrate; a P-type polysilicon emitter formed over the N-type silicon substrate and forming a backside junction with the N-type silicon substrate; an oxide layer formed between the P-type polysilicon emitter and the N-type silicon substrate; a negative polarity metal contact making an electrical connection to the N-type silicon substrate from the front side of the solar cell; and a positive polarity metal contact making an electrical connection to the P-type polysilicon emitter from the back-side of the solar cell.	an emitter layer formed over a back surface of the substrate, the emitter layer formed over a backside junction with the substrate; an oxide layer formed between the back surface of the substrate and the emitter layer; a first metal contact making an electrical connection to the substrate on the front side of the solar cell; and a second metal contact making an electrical connection to the emitter layer of the backside of the solar cell, the first metal contact and the second metal contact being configured to allow an external electrical circuit to be powered by the solar cell.

Ex. 1001, claims 1 (6:4-22), 9 (6:42-57) (emphasis added).

94. As is shown above, claim 1 is directed toward specific N-type and P-type dopant sources in the silicon and polysilicon layers, respectively. Claim 9, on the other hand, is silent with respect to the types of dopant sources used to dope the silicon and polysilicon layers. Therefore, at least with respect to the dopant sources, claim 9 is broader in scope than claim 1. Therefore, I understand that claim 9 is not limited to N-type silicon and P-type polysilicon layers.

VIII. THE '516 PATENT PROSECUTION HISTORY AND RELATED APPLICATIONS

95. During prosecution of the '516 patent's application, the Examiner issued a restriction requirement between the claims "drawn to a solar cell" and those "drawn to a method of making a solar cell." Ex. 1002, 61. SunPower elected the solar cell claims for the '516 patent and filed a divisional application to pursue the method claims challenged here. Ex. 1002.

96. Original claim 9 (application claim 17) recited all elements is claim 9 except for "an oxide layer formed between the backside of the substrate and the emitter layer." Ex. 1002, 19. The examiner rejected this original claim. Ex. 1002, 76-78. Applicant amended the original claim to recite "an oxide layer formed between the back surface of the substrate and the emitter layer." Ex. 1002, 135. The Examiner then allowed the amended claims 17-20 in the application (claims 9-12 of the '516 patent. Ex. 1002, 152.

97. Patent Owner then filed the application that led to U.S. Patent No. 8,878,053 (the other subject of the divisional required by the Examiner) on July 13, 2012. Ex. 1038, 8.

98. After allowance of the '516 patent, three continuations were filed seeking additional claims of varying scope:

- U.S. Patent Application No. 14/504,771 (the “’771 application”), filed October 2, 2014, claiming “a doped diffusion region in the substrate” and “a front electrode that is coupled to the doped diffusion region on the front surface of the substrate.” Ex. 1005, 470. This application was abandoned after an appeal of the Examiner’s decision to the Board. *Id.*, 506-520, 522.
- U.S. Patent Application No., 16/460,035 (the “’035 application”), filed July 2, 2019, claiming “a plurality of dot-shaped N-type doped regions in the N-type silicon substrate under the antireflective layer, each of the plurality of dot-shaped doped regions having a dot shape as seen from a plan view of the solar cell” and “a first metal contact disposed on the front surface of the N-type silicon substrate, wherein the first metal contact is in electrical contact with the plurality of dot-shaped N-type doped regions.” Ex. 1018, 235. This application was abandoned after an appeal of the Examiner’s decision to the Board. *Id.*, 285-293, 295.

- U.S. Patent Application No. 17/870,268 (the “’268 application”), filed July 21, 2022, filed with claims directed towards a solar cell including a dielectric layer. Ex. 2013, 25-27. The ’268 application is currently under examination. *Id.*, 287-304 (a Final Rejection was issued September 16, 2024).

IX. PERSON OF ORDINARY SKILL IN THE ART

99. Petitioner asserts the following qualifications for a POSITA:

A POSITA at the priority date of the ’053 patent (February 20, 2008) would have had (i) an advanced degree in electrical engineering, mechanical engineering, applied physics, chemistry, materials science, or a related discipline and (ii) at least one year of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. Alternatively, a POSITA would have had (i) a bachelor’s degree in the aforementioned disciplines and (ii) at least two years of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. Less work experience may be compensated by a higher level of education, and vice versa.

Paper 3, 16.

100. For the purposes of this declaration, I have applied Petitioner’s qualifications for a POSITA.

X. CLAIM CONSTRUCTION

101. Patent Owner's counsel provided me with legal principles that are relevant to claim construction. *See* § V.A above. I considered those legal principles in forming my opinions in this section.

102. Patent Owner's counsel asked me to consider claim construction as of the date of the invention. *See* § IV.A, above. My opinions are the same regardless of which date is used.

103. For the purpose of this declaration, Patent Owner's counsel asked me to adopt Petitioner's proposal to apply the plain and ordinary meaning of the claims. Paper 3, 18.

XI. THE CITED REFERENCES AND OTHER PRIOR ART

A. Froitzheim (Ex. 1004)

104. European Patent Publication EP1732142 ("Froitzheim"), published in 2006, is titled "Si solar cell and its manufacturing method." Ex. 1004, Cover.

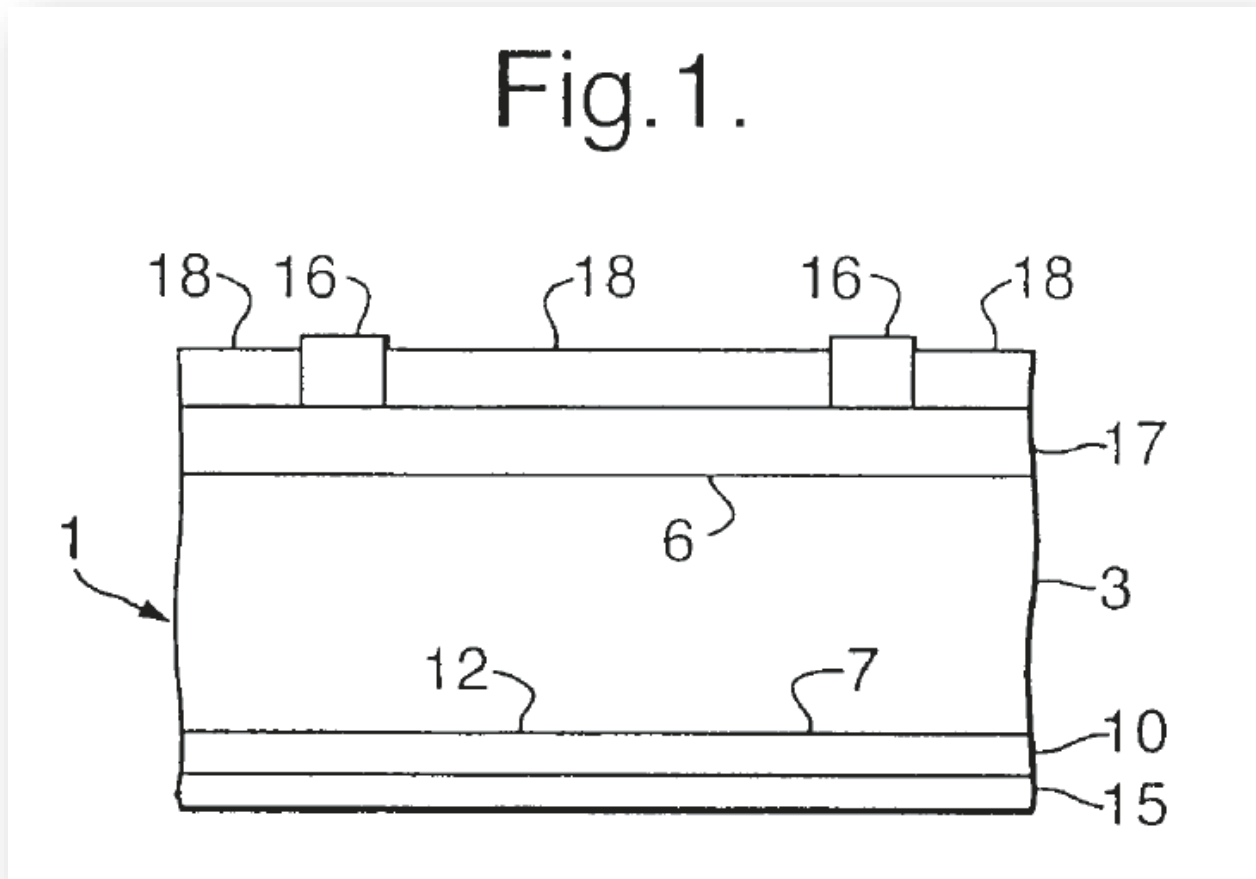
105. Froitzheim's Abstract states:

A solar cell comprising a silicon body layer of n-type bulk doping having a front side and a rear side; a non-alloyed p-type doped region at the rear side of the body layer and forming a p/n-junction therewith; a rear side contact in electrical connection with the p-type doped region; and a front side contact in electrical connection with the n-

type silicon body layer, and a method of manufacturing such a solar cell.

Ex. 1004, Abstract.

106. Below is a first embodiment of Froitzheim's cell:



Ex. 1004, Fig. 1.

107. Froitzheim describes Figure 1 as follows:

[0024] Reference is made to Figure 1 showing schematically a cross-section through a first embodiment of a solar cell 1 according to the invention. The solar cell 1 comprises a silicon body layer 3 of n-type

bulk doping having a front side 6 and a rear side 7. The silicon body layer 3 is made from crystalline silicon, and can be of the mono-, multi- or polycrystalline type. Preferably, Czochralski grown Silicon is used. The thickness of the body layer can be typically between 10 and 400 μm , suitably between 100 and 300 μm , preferably between 150-250 μm . A suitable dopant is for example phosphorous. The doping level is generally in the range of 10^{13} - 10^{18} atoms per cm^3 , typically in the order of 10^{15} - 10^{16} . Suitably, the doping is such that a resistivity higher than 0.5 and lower than 150 Ohm-cm is obtained, preferably higher than 1 and lower than 20, more preferably lower than 10 Ohm-cm.

[0025] At the rear side 7, a p-doped layer 10 is arranged suitably such as discussed further below, and a p/n-junction 12 with the body layer is formed.

...

[0027] A rear side contact 15 is arranged in electrical connection with the p-doped layer 10. The rear side contact is shown covering a large part or substantially all of the rear side of the cell.

[0028] At the front side 6, screen-printed front side contacts 16 are provided in electrical connection with the n-type silicon body layer. The front side contacts form part of a finger structure 19 such as sketched in top view in Figure 2 covering typically around 10% of the front surface when screen printed contacts are used. The electrical connection is provided via a shallow n+ doped layer 17 on the front side 6, i.e. between the front contact and the n-type silicon body layer.

...

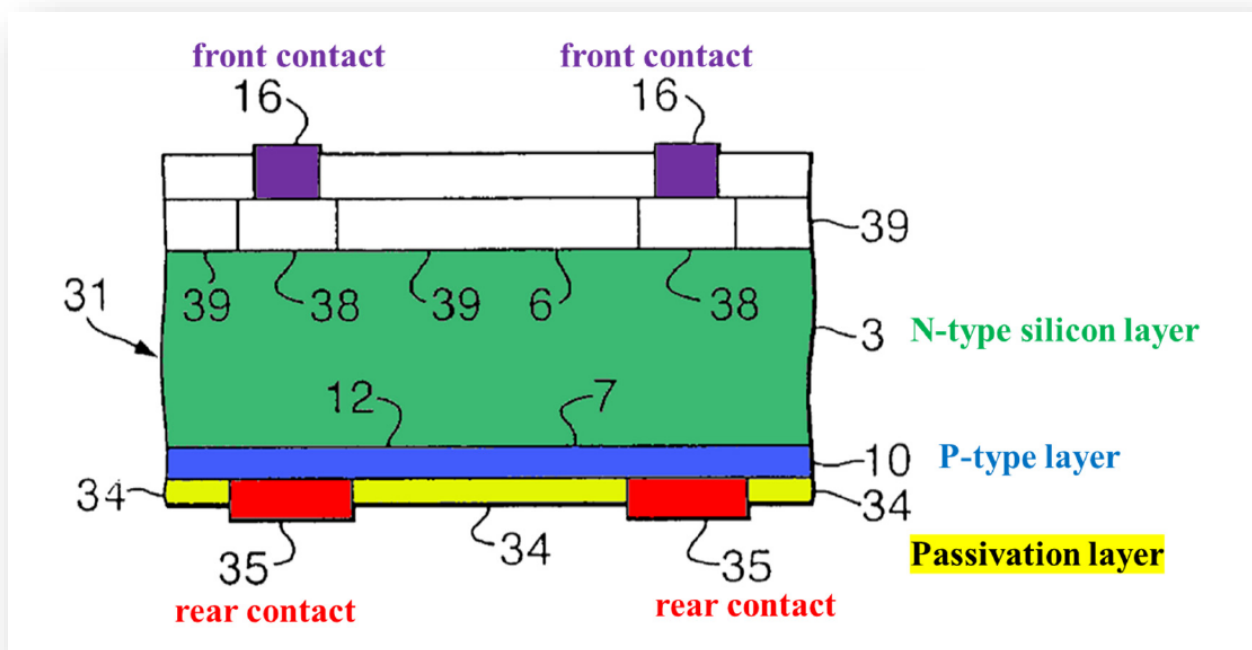
[0030] The front surface is further provided with a passivation layer 18. The passivation layer can for example be an oxide such as SiO₂ a nitride such as SiN, undoped amorphous silicon, or mildly n⁺ doped amorphous silicon layer, which can be arranged using methods known in the art. It is a further advantage of the present invention that n or n⁺ doped layers can generally easier and better be passivated than p or p⁺ doped layers. An advantage of using SiN as passivation layer is that it has intrinsic charges.

[0031] Suitably further, an anti-reflection coating is provided as known in the art.

[0032] During normal operation of the solar cell 1 the front side 6 faces the sun and light is received through the area of the front surface that is not covered by the front contact 16. Light is absorbed predominantly in the n-doped body layer 3, and excess hole-electron pairs are created. The holes form minority charge carriers in the n-type material and travel towards the rear side over the p/n-junction 12 where they become majority carriers in the p-layer that are withdrawn at the rear side contact thereby providing photocurrent. The photogenerated excess electrons are prevented from diffusing to the front contacts by the field exerted by the n⁺/n junction leading between the body layer 3 and the p⁺ layer 18.

Ex. 1004, ¶¶24-32.

108. Froitzheim discloses a second embodiment , which Petitioner references:



Paper 3, 19 (citing Ex. 1004, Fig. 3) (annotations in Petition).

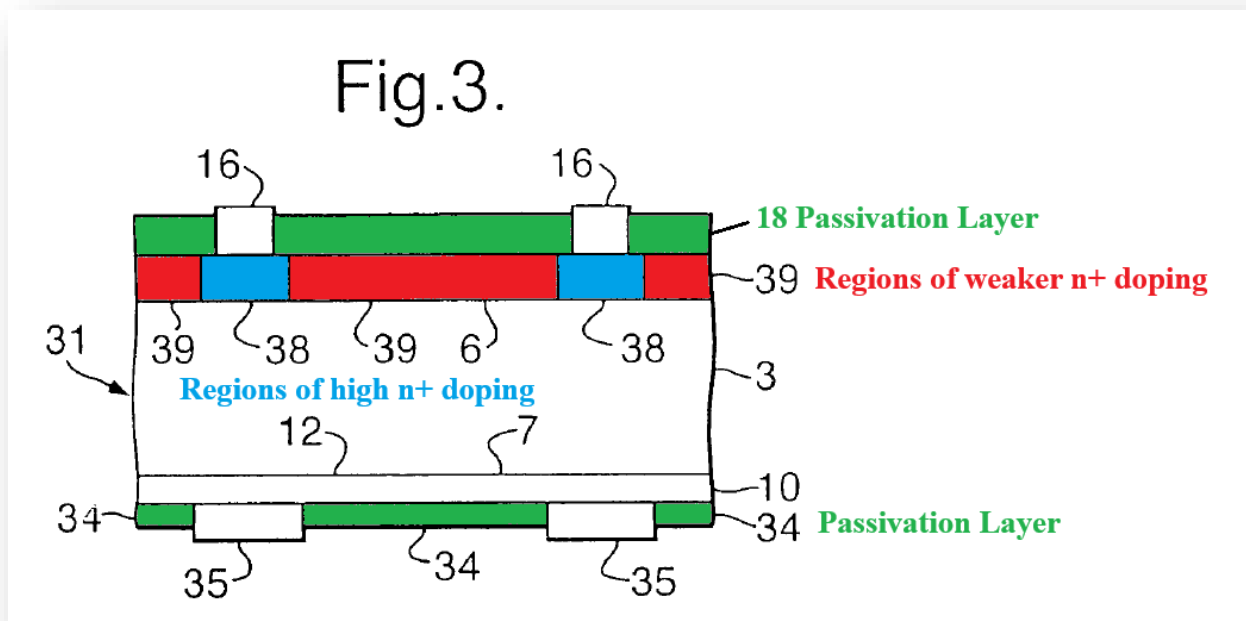
109. Froitzheim describes Figure 3 as follows:

[0033] Reference is made to Figure 3 showing a second embodiment of a solar cell 31 according to the invention. Cell 31 differs from cell 1 of Figure 1 in that the rear contacts 35 are arranged in a finger structure covering only part of the rear side, e.g. similar to that of Figure 2. A typical coverage is in the range of 10-40% of the rear surface. Between the fingers a passivation layer 34 is arranged, for which the same type of layers can be used as for the front side. If the cell is suitably arranged for operation such that reflected or diffracted light is received at the rear side not facing the sun, additional photocurrent can be created by photons absorbed predominantly in the body layer 3 from the rear side.

[0034] A further difference with the cell of Figure 1 is the structured front surface field. Regions 38 of high n+ doping are arranged surrounding the front contacts 16, and regions 39 of weaker n+ doping in between front contact fingers, wherein the weaker n+ doping can be achieved by a doping concentration intermediate between that of the n-type body layer and that of the n+ doped regions 18, and/or in that regions 39 are shallower than regions 38

Ex. 1004, ¶¶33-34.

110. Based on the description above, additional labels to Figure 3 of Froitzheim are shown below:



Ex. 1004, Fig. 3 (annotated); *see also* Ex. 1004, Fig. 1 (illustrating layer 18).

B. Gan (Ex. 1005)

111. First, it should be understood that there are two Gan publications relevant to the Petition. The first publication is Gan et al., “*Polysilicon Emitters for Silicon Concentrator Solar cells*,” Proceedings of the 21st IEEE-PVSC (1990) (“Gan”). Ex. 1005, 245. Gan is cited in the Petition and used in combination with Froitzheim, Paper 3, 27, with Froitzheim and Sheats, *id.* at 60, and with Li, *id.* at 78.

112. The second publication is Gan, “*Polysilicon emitters for silicon concentrator solar cells*,” a dissertation submitted to the Department of Material Science and Engineering and the Committee on Graduate Studies of Stanford University in 1990 (“Gan Thesis”). Ex. 2003, Cover. The Gan Thesis was published and publicly available on the shelves in the Stanford Library on April 10, 1991, which is prior to the priority date of the ’053 patent. *See* Ex. 2026, ¶23. I understand that it can be assumed that a POSITA would have had knowledge of Gan and the Gan Thesis before that priority date. As explained below, the Gan Thesis is important for several reasons, including telling the complete story of why the technology disclosed in Gan was experimental, could not be reliably reproduced, and was not suitable for use in commercial concentrator cells.

113. In both Gan (Ex. 1007) and the Gan Thesis (Ex. 2003), the common author, Gan, is describing experiments trying to thread a needle to produce the

optimum temperature to break up an interfacial oxide a little, but not too much. This interfacial oxide layer is formed between a crystalline silicon substrate and a polysilicon layer applied over the rear surface of the substrate. Gan tried different anneal temperatures and durations, and determines that above 900°C, the oxide breakup becomes too much. *See, e.g.*, Ex. 1007, 248 (“Considering the significant increase of J_o caused by increasing the drive-in temperature from 900 to 1000°C. . .”); *see also id.* at (Table 1). Gan is not describing building an actual one sun solar cell, rather Gan is describing experiments on poly-Si emitters that might be useful in a concentrator solar cell.

114. Petitioner proposes a Froitzheim-Gan combination that includes “fabrication steps to incorporate Gan’s polysilicon emitter and oxide layer.” Paper 3, 27.

115. Gan discloses manufacturing steps to create test devices that include “[p]olysilicon emitters with a thermally grown interfacial oxide.” Ex. 1005, Abstract. Gan uses these test devices to measure the emitter saturation current density (J_o) and contact resistivity (ρ_c) of its polysilicon emitter when annealed under various conditions. *Id.* Specifically, Gan discloses a test device using FZ wafers to measure J_o , and a test device using CZ wafers to measure ρ_c . *Id.* at 245.

116. Gan discloses the following steps to create its test devices.

1. Field oxidation (2000 Å)*.

2. Polysilicon-substrate contact opening*.
3. Thin thermal oxide growth at 800 °C*. (10-minute oxygen flow)[.]
4. Polysilicon deposition (6000 Å) and first-step anneal (1050 °C)*.
5. First-step anneal*.
6. Polysilicon finger definition.
7. Undoped glass deposition (2000 Å).
8. Metal-polysilicon and metal-substrate contact opening.
9. Doped glass deposition on both sides of the wafer*.
10. Drive-in; 900-1000 °C*.
11. Doped glass stripping and Al-1% Si alloy deposition.
12. Metal finger definition.

Ex. 1005, 246 (emphasis added). According to Gan, “the J_o and ρ_c were measured independently for each type of polysilicon emitter (or contact). J_o was measured with photoconductivity decay method. . .” and “the steps marked with “*” are the steps for J_o -measurement samples.” *Id.*

117. I understand that Petitioner’s expert testified that Gan’s steps 3, 4, 9, and 10 relate to the implementation of Gan’s oxide layer and Gan’s polysilicon emitter:

Q Can you go to Page 79 of your declaration?

A I’m there.

Q This is, here on this page you provide an illustration of the Froitzheim-Gan combination. Correct?

A Yes.

Q And you draw an oxide layer in orange. Correct?

A Correct.

Q This is referring to Gan's oxide layer. Correct?

A That's correct.

Q Now, which of the 12 steps in Gan disclose the formation of that oxide layer?

A Gan describes in Step 3 how to form an oxide layer, thin thermal oxide growth at 800 degrees C, parentheses, ten minute oxygen flow. And as I mentioned, many other -- many, many other reports of how to form tunnel oxide layers have the same function as Gan's.

Q Going back to Page 79 of your declaration, you also illustrate a P-type polysilicon layer in dark blue. Right?

A Correct.

Q This would be Gan's polysilicon layer. Is that right?

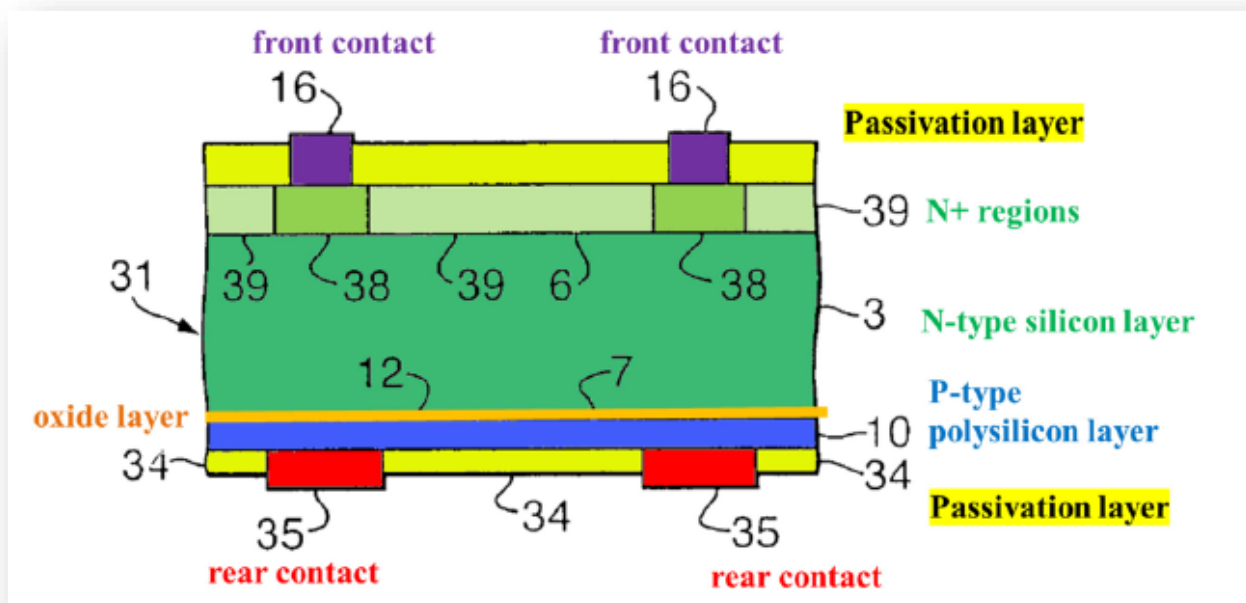
A That's what I describe, the implementation of Gan's oxide layer and polysilicon emitter into Froitzheim's back junction solar cell is shown in the below figure, which is the one you're referring to.

Q Now, which steps in Gan's 12 steps disclose the formation of a polysilicon layer?

A Gan describes the deposition of a polysilicon layer in Step 4 of his sequence, and the subsequent doping of that to form an emitter in Steps 9 and 10.

Ex. 2029, 236:3-237:18.

118. I understand the illustration below was what was discussed in the quote above:



Ex. 1003, ¶122.

119. Step 4 (the anneal performed at 1050°C) causes breakup of the oxide layer. This step and step 10, the drive-in step, were the subject of Gan's measurements to try to achieve acceptably low J_o values. Ex. 1007, 246. The anneal of step 4 is used to break up the thin oxide layer, and the second anneal performed at step 10 is used in Gan to drive in the dopants. This step 10 anneal is referred to as "the second-step anneal" in Gan's table 1 below. Ex. 1007, 248.

Table 1: The effect of the second-step anneal on J_o and ρ_c .

	N-type		P-type	
	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$
900 °C-4 hour	2.4	18	3.5	18
1000 °C-30 min	4.5	~ 6	8.2	3.8
1000 °C-60 min	7.9		10.5	

Ex. 1005, 248, Table 1.

120. Gan teaches that it is optimal to have low values for both J_o [emitter saturation current density] and ρ_c [contact resistivity], and this is achieved “when both carriers are mostly blocked by the interfacial oxide.” Ex. 1005, 245, 249. In that regard, Table 1 of Gan shows that as you increase the temperature and time in the second step anneal, the value of J_o increases, which means more recombination and lower cell efficiency, which are not desired results.

121. Gan (Ex. 1005) and the Gan Thesis (Ex. 2003) both describe experiments that focused on trying to find the optimum temperature to be used in creating an interfacial oxide between a crystalline silicon substrate and a polysilicon layer and, more specifically, on how to break up the interfacial oxide a little, but not too much. Gan tried different anneal temperatures and durations and determined that above 900°C, the oxide breakup becomes too much. Ex. 1005, 248 (“Considering the significant increase of J_o caused by increasing the drive-in

temperature from 900 to 1000°C, it is beneficial to use the two-step anneal to optimize J_o .”); *id.* at (Table 1).

122. As discussed in the Petition, Gan “teaches a solar cell structure with a ‘polysilicon emitters with a thermally grown interfacial oxide’ over a silicon substrate.” Paper 3, 19 (citing Ex. 1005, 245-46). Gan also taught that “a very thin oxide (interfacial oxide)” “[a]llways exists” between the polysilicon emitter and the substrate.” Ex. 1005, 245. More importantly, Gan Thesis teaches that “solar cells that were modeled or made in this study all suffered high contact resistance” and that “in the real solar cell runs, the situation grew even worse.” *See, e.g.*, Ex. 2003, 129 (110 in original); *see also id.* at 135-136 (116-117 in original). Thus, the Gan Thesis refutes Petitioner’s narrative that Gan successfully formed in a solar cell an interfacial oxide layer between a silicon substrate and a polysilicon layer. Paper 3, 32-33 (citing Ex. 1005, 246, 248-49); Ex. 1003, ¶¶ 130, 132.

123. Substantively, Gan is specific about the effect of a high temperature anneal on the interfacial oxide layer between the silicon substrate and the polysilicon layer:

In either case, the oxide is not thermally stable; *i.e.*, it tends to break up during high temperature anneals. The breakup of the interfacial oxide has direct impact on both majority and minority carrier transport in the polysilicon emitter. This can be seen from the dependence on the specific contact resistivity (ρ_c) [6] and the emitter saturation

current density (J_o) [1,2,3,4,5,6,7] upon either the anneal condition or the oxide integrity.

Ex. 1005, 245.

124. Gan specifically says that when the temperature is high and the oxide loses its integrity, the ρ_c is low and the J_o is high:

With the effect of the interfacial oxide is negligible, such as when the interfacial oxide loses its integrity in high temperature anneals, the ρ_c is low ($\sim 2 \times 10^{-7} \text{ } \Omega\text{-cm}^2$) [6] and the J_o is high ($\sim 1 \times 10^{-12}$) [1,3].

Conversely, when both the carriers are mostly blocked by the interfacial oxide, like for an intact chemical oxide ($\sim 15 \text{ } \text{\AA}$), the ρ_c is high and the J_o is low.

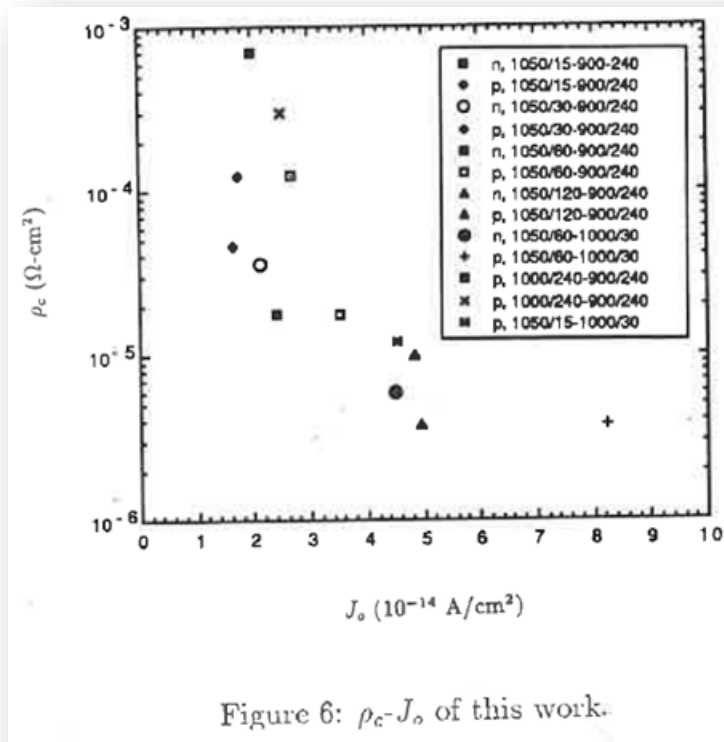
Ex. 1005, 245.

125. Gan teaches that it is optimal to have low values for both J_o (emitter saturation current density] and ρ_c (contact resistivity], and this is achieved “when both carriers are mostly blocked by the interfacial oxide.” Ex. 1005, 245, 249.

What Gan is trying to determine are values for “ ρ_c and J_o when only a small fraction of the interfacial oxide is broken.” *Id.* According to Gan “there always exists a very thin oxide (interfacial oxide), which can be the by-product of the cleaning process or is grown intentionally . . . In either case, the oxide is not thermally stable, i.e., it tends to break up during the high temperature anneals.” *Id.* at 245 (emphasis added). Gan explains that “[t]he first-step anneal, which serves to

break up the oxide, was performed at higher temperature than that for the second-step anneal which aims for the dopant drive-in.” *Id.*

126. Gan ran multiple experiments for combinations of temperatures for the first anneal and the second anneal (for dopant drive in) and reported the results in Figure 6, which is a plot of ρ_c v. J_o , with a key in the top right that shows “the type of polysilicon emitter, the first-step anneal (temperature/minute), and the second-step anneal (temperature/minute).” Ex. 1007, 249, Fig. 6. The goal was to provide low values for J_o .



Ex. 1005, Fig. 6.

127. This graph shows that the higher the temperature of the second step anneal (the anneal to drive the dopants into the polysilicon), the higher the J_o . In fact, this figure shows much lower J_o values for the 900 °C second anneal (“regime 1”) than for the 1000°C second anneal (“regime 2”). Gan then discusses this figure and observes for regimes 1 (900°C) “ J_o is almost constant while ρ_c drops drastically” and for regime 2 (1000°C) “ ρ_c decreases very slowly and J_o increases in much faster pace.” Ex. 1005, 249.

128. Gan also explains that the second step anneal is optimal when performed at “900 °C for 4 hours.” Ex. 1005, 247. Gan further says “[considering the significant increase of J_o caused by increasing the drive-in temperature from 900 to 1000 °C, it is beneficial to use the two-step anneal to optimize J_o .” *Id.*

129. Gan provided further analysis of the experimental results in Table 1, below. These results show that the higher the temperature of the second-step anneal and the longer its duration the worse the device works.

Table 1: The effect of the second-step anneal on J_o and ρ_c .

	N-type		P-type	
	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$
900 °C-4 hour	2.4	18	3.5	18
1000 °C-30 min	4.5	~ 6	8.2	3.8
1000 °C-60 min	7.9		10.5	

Ex. 1005, Table 1

130. Gan shows that as the temperature increases above 900°C, ρ_c decreases but J_o increases rather than decreases, such that annealing at a temperature (>900°C) results in a rapid decrease in the efficacy of the system.

C. Gan Thesis (Ex. 2003)

131. Jon-Yiew Gan's thesis titled "*Polysilicon emitters for silicon concentrator solar cells*," published by the Stanford University in July 1990, provides a more comprehensive review of the experiments and methodologies described in Gan (Ex. 1004), *see, e.g.*, Ex. 2003, Chapter 5, and provides significantly more details about the theory, experimental results, and conclusions set forth in Gan (Ex. 1004).

132. I understand that the Gan Thesis was published and publicly available on the shelves in the Stanford Library on April 10, 1991, which is prior to the priority date of the '053 patent (as discussed in § IV.A). *See* Ex. 2026, ¶23. I further understand that it can be assumed that a POSITA would have had knowledge of the information in the Gan Thesis before that priority date. It is my understanding that a librarian expert confirmed public availability. *Id.*

133. The Gan Thesis acknowledges inconsistent oxide growth during "ramp-up" and "stand-by" periods, and explains that "it is possible that the thin-oxide growth can be improved by performing the oxidation at lower temperatures

such that the oxide rate can be controlled more precisely.” Ex. 2003, 112 (emphasis added).

134. At best, the Gan Thesis suggested that “[t]heoretically, it is possible to make a polysilicon SIS emitter with an intact inter-facial oxide having low J_o and “acceptable” ρ_c simultaneously.” Ex. 2003, 53 (emphasis added). Gan Thesis also stated “[t]heoretically, a model was proposed to make the polysilicon emitter with both low J_o ($\sim 3 \times 10^{-14}$ A/cm²) and low contact resistance ($\rho_c \leq 1 \times 10^{-5}$ Ω -cm²).” *Id.* at Abstract (emphasis added). Also, “[t]he polysilicon emitter with low J_o and ρ_c can be made with a very small fraction of interfacial oxide breakup.” *Id.* at 107 (emphasis added). And “[w]ith a few percentages of the interfacial oxide being broken, the ρ_c will be negligible for the application in concentrator solar cells. Under such a condition, there is a regime in which the J_o will not be affected by the oxide breakup because it is dominated by the recombination at the oxide interface. Thus it is possible for polysilicon SIS emitter to have both low J_o and ρ_c .” *Id.* at 69 (emphasis added).

135. Stepping back, however, a POSITA would recognize these musings in the Gan Thesis were theories that fell far short of being realized and reproducible in practice. In context, the lack of consistent success in experimental results derived from testing these theories fell far short of supporting a reasonable expectation of success. This is particularly true because the Gan Thesis reproduced

experimental data showing poor results when implementing the theories set forth in Gan.

136. For example, the Gan Thesis discloses the following:

It appears that the oxide breakup depends critically on the interfacial oxide thickness. The thin-oxide growth recipe used in this work was not reliable; the oxide thickness between 15 and 20 Å have been found with the same growth condition. As a result, this contributes to the fluctuation of the ρ_c results. It is then clear that a more reliable way of growing the thin oxide is needed.

Ex. 2003, 119 (emphasis added).

Although a thermally grown interfacial oxide seems **essential** for a polysilicon emitter to have both low J_o and ρ_c , the breakup process is still difficult to control. On several occasions, we have encountered reproducibility problems. For example, we find that the ρ_c is quite different between two separate experiments with identical processing conditions. Even worse, solar cells that were made in this study all suffered high contact resistance. The problem is primarily due to insufficient oxide breakup, and is caused by the fluctuation of the thickness of the interfacial oxide.

Ex. 2003, 107 (emphasis added).

As shown in the figure, the cell is in fact plagued by two things: the high surface recombination velocity ($S = 58$ cm/sec), and high emitter resistance ($\rho_{cm} + \rho_{cp} = 1 \times 10^{-3} \Omega\text{-cm}^2$). . . From the low emitter

recombination and high emitter resistance, it is clear that the interfacial oxide did not break as expected.”

Ex. 2003, 110 (emphasis added); *see also id.* (“Later in the real solar cell runs, the situation grew even worse. . . Although the $(J_{on} + J_{op})$ measured from those cells are between 8×10^{-14} and 4×10^{-14} A/cm², the cell efficiency is greatly degraded by such a high emitter resistance.”); *id.* at 111 (“Although these results can be attributed to many other reasons, the following experiment shows that the effect of the oxide thickness cannot be ignored. This, combined with the non-reliable oxide-growth recipe gives rise to the mishap of our solar-cell runs.”) (emphasis added); *id.* at 114 (“It becomes clear that the wide fluctuation of our results is mainly due to the poor control over the oxide thickness.”); *id.* at 114-17 (“[W]e found that a consistent result of ρ_c is difficult to reproduce for the polysilicon emitter with a thermally grown interfacial oxide. This is mainly attributed to the fact that our thin-oxide recipe is not reliable.”) (emphasis added); *id.* at 56 (“With a window so narrow, it is not possible to have good control over the characteristics of a polysilicon SIS emitter.”).

137. Simply, the Gan Thesis established that the processes found in Gan would not achieve good results consistently or reliably, especially at the temperatures used by Froitzheim. Consequently, a POSITA would not have had a

reasonable expectation of success and, therefore, would not have been motivated to combine Froitzheim and Gan.

D. Borden-575 (Ex. 1006)

138. International Publication No. WO 2009/094575 (“Borden-575”), published in 2009, is titled “Buried Insulator Isolation for Solar Cell Contacts.” Ex. 1006, Cover.

139. Borden-575’s Abstract states:

The present invention relates to methods and apparatuses for providing a buried insulator isolation for solar cell contacts. According to certain aspects, the invention places a buried oxide under the emitter of a polysilicon emitter solar cell. The oxide provides an excellent passivation layer over most of the surface. Holes in the oxide provide contact areas, increasing the current density to enhance efficiency. The oxide isolates the contacts from the substrate, achieving the advantage of a selective emitter structure without requiring deep diffusions. The oxide further enables use of screen printing on advanced shallow emitter cells. Positioning of the grid lines close to the openings also enables use of a very thin emitter to maximize blue response.

Ex. 1006, Abstract.

140. Borden-575 is concerned with contact isolation in solar cells, and the difficulty of implementing prior art selective emitter structures that provide contact isolation. Specifically, Borden-575 states:

[0003] To obtain high efficiency in silicon solar cells, it is considered advantageous to eliminate surface recombination. Such recombination comes from both unpassivated surfaces and from metal contacts. A measure of recombination is the surface recombination velocity (SRV), which is the rate of minority carrier recombination at the surface. . .

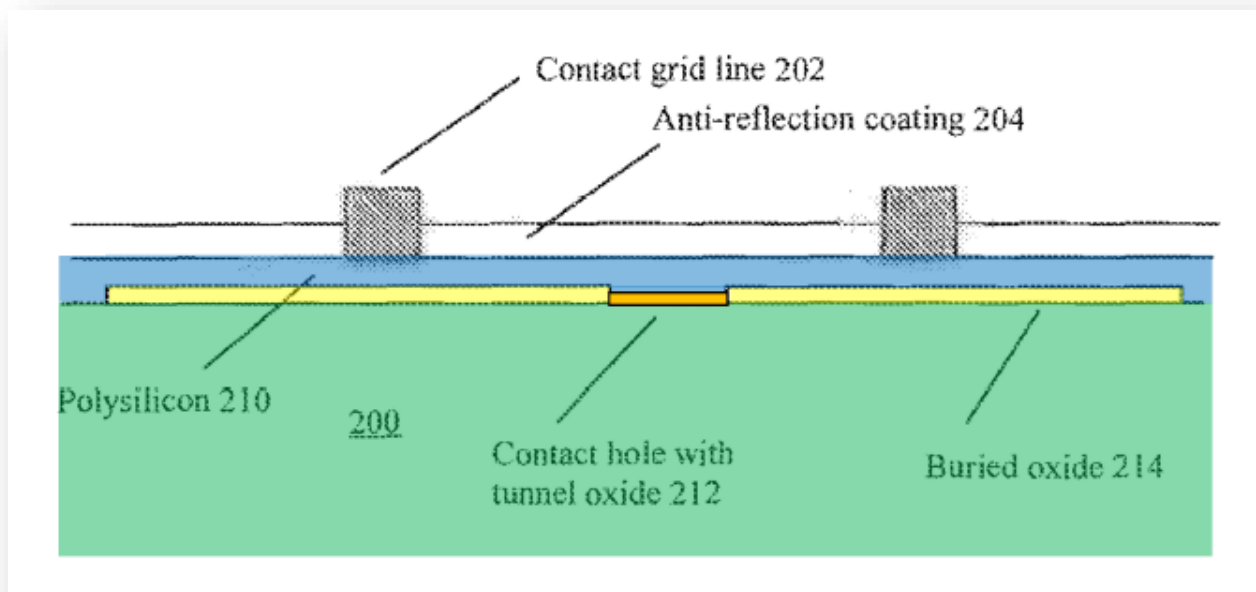
[0004] One well known method to isolate the contacts from the bulk is to use a selective emitter, shown in FIG. 1. As shown in FIG. 1, the area away from the contacts 102 has a shallow emitter diffusion 106 (n-type, typically with Phosphorous doping, on a p-type substrate, for example). The shallow emitter 106 provides good blue response, as blue photons are absorbed near the surface. . .

[0005] Another method to passivate contacts is to place a thin tunnel oxide – typically 15Å thick - under the metal contacts. Such types of contacts are also well known, and have been used commercially by Schott solar to manufacture MIS solar cells. However, such solar cells have not been commercially introduced, possibly because of the difficulty of reliably forming a thin tunnel oxide.

[0006] Therefore, there remains a need in the art for a commercially feasible method and apparatus for providing contact passivation in a solar cell.

Ex. 1006, ¶¶3-6.

141. Borden-575's purported innovation is a "buried oxide under the emitter of a polysilicon emitter solar cell." Ex. 1006, Abstract.



Paper 3, 68 (citing Ex. 1006, Fig. 2) (annotation in Petition).

142. Borden-575 describes Figure 2 as follows:

FIG. 2 shows an example cell structure in accordance with embodiments of the invention. As shown in FIG. 2, the cell structure includes an insulating (e.g. oxide) layer 214 under the doped region 210 and the contact 202. This insulating layer 214 isolates the contact 202 from the substrate 200. According to some aspects of the invention, if the insulating layer 214 is made using a material that passivates silicon, such as thermal SiO_2 , then the solar cell surface has very good passivation and a low surface recombination velocity, both in the field region 210 and under the contacts 202. Contact holes 212 are provided in the insulating layer 212 to allow for photocurrent flow. In embodiments described in more detail below, contact holes

212 include a tunnel oxide. However, this is not necessary in all embodiments.

Ex. 1006, ¶19.

143. Borden-575's structure has the following purported benefits:

In general, the invention provides a buried oxide under the emitter of a polysilicon emitter solar cell. The oxide provides an excellent passivation layer over most of the surface. Holes in the oxide provide contact areas, increasing the current density to enhance efficiency. The oxide isolates the contacts from the substrate, achieving the advantage of a selective emitter structure without requiring deep diffusions.

Ex. 1006, ¶16.

144. The buried oxide 214 features contact holes 212 that “allow current flow” between the emitter and the substrate. For example, Borden-575 states:

[0008] In furtherance of these and other aspects, a solar cell according to embodiments of the invention includes an emitter layer formed on a semiconductor substrate; and an insulating layer between the emitter layer and a surface of the substrate, the insulating layer being patterned to include contact holes that allow current flow therethrough.

[0009] In additional furtherance of these and other aspects, a method of fabricating a solar cell according to embodiments of the invention includes forming an insulating layer on a surface of a semiconductor substrate; patterning contact holes in the insulating layer that allow

current flow therethrough; and forming an emitter layer on the insulating layer.

...

[0019] . . . Contact holes 212 are provided in the insulating layer 212 [sic]¹ to allow for photocurrent flow. . .

[0021] In embodiments such as shown in FIG. 2, the contacts 202 are positioned approximately in the middle between two holes 212.

Photocurrent flows through contact holes 212 patterned in the oxide layer 214. This concentrates the current flow, providing an increased current density at the junction. The collected current then flows laterally to the contacts 202. Typical dimensions of the openings 212 can be 20 to 200 μm and spacing between openings 212 can be 1-5 mm. The ratio of the spacing to opening width provides the concentration, which is limited by series resistance due to current crowding at the contact holes. Concentration ratios on the order of 5 to 20 are typical. The openings can be lines parallel to the contact grid lines, or holes of shape such as rectangles or circles. Larger openings can be patterned without lithography, using screen printing. Laser ablation can also be used.

¹ The label “212” here appears to be an error. The “insulating layer” is labelled as “214” throughout Borden-575, Ex. 1006, ¶¶18-21, and appears to be used interchangeably with the term “buried oxide,” *id.* at Figs. 2, 3, ¶24.

Ex. 1006, ¶¶8-9, 19-21 (emphasis added).

145. Borden-575 further describes its current holes as follow, and emphasizes a broad construction of the term “contact hole:”

[0020] In embodiments, substrate 200 is comprised of silicon, and is low-doped with p- or n-type impurities. Many other substrate materials can be used and this and many other methods for obtaining a desired polarity concentration and type are possible, as will be appreciated by those skilled in the art. It should be noted that the term contact hole should be construed broadly so as to relate to many types of openings through insulating layer 214 and many types of solar cell contacts. For example, the holes can provide for point contacts or they can provide for grid line contacts. Those skilled in the art of solar cell contacts will appreciate how the teachings of the invention can be applied to these and other various types of contacts and openings.

[0021] In embodiments such as shown in FIG. 2, the contacts 202 are positioned approximately in the middle between two holes 212. Photocurrent flows through contact holes 212 patterned in the oxide layer 214. This concentrates the current flow, providing an increased current density at the junction. The collected current then flows laterally to the contacts 202. Typical dimensions of the openings 212 can be 20 to 200 μm and spacing between openings 212 can be 1-5 mm. The ratio of the spacing to opening width provides the concentration, which is limited by series resistance due to current crowding at the contact holes. Concentration ratios on the order of 5 to 20 are typical. The openings can be lines parallel to the contact grid

lines, or holes of shape such as rectangles or circles. Larger openings can be patterned without lithography, using screen printing. Laser ablation can also be used

Ex. 1006, ¶¶20-21 (emphasis added).

146. Borden-575 also discloses an optional thin tunnel oxide in the contact holes.

[0019] FIG. 2 shows an example cell structure in accordance with embodiments of the invention. . . In embodiments described in more detail below, contact holes 212 include a tunnel oxide. However, this is not necessary in all embodiments.

[0022] In embodiments, the doped region 210 is formed using polysilicon, which may be deposited at a temperature on the order of 630⁰C and is in-situ doped. A short anneal at 1050⁰C for 30 seconds after deposition activates the dopants. As mentioned above, in some embodiments a thin tunnel oxide may be included between the substrate 200 and the polysilicon 210 in the contact holes 212. This oxide - typically 8 to 15A thick - provides passivation between the substrate and the polysilicon, while allowing for tunnel current flow.

[0026] FIG. 4 shows an example embodiment of the process flow for fabricating a solar cell structure according to aspects of the invention. First in step S402, the wafer is cleaned and the buried oxide formed, using a process such as thermal oxidation or RadOx® from Applied Materials. Next in step S404, the contact holes are formed. For example, an etch mask layer is screen printed on the cell and the buried oxide is etched in HF. The resist is then removed. The wafer is

then cleaned and, in one embodiment shown in FIG. 4, a tunnel oxide is grown in the contact holes using a process such as ISSG or Radox in the step S406. Another embodiment does not use the tunnel oxide, and processing advances directly from step S404 to S408.

Ex. 1006, ¶¶19, 22, 26 (emphasis added).

147. But Borden-575 notes the hardship of reliably forming thin tunnel oxides:

Another method to passivate contacts is to place a thin tunnel oxide – typically 15Å thick - under the metal contacts. Such types of contacts are also well known, and have been used commercially by Schott solar to manufacture MIS solar cells. However, such solar cells have not been commercially introduced, possibly because of the difficulty of reliably forming a thin tunnel oxide.

Ex. 1006, ¶5 (emphasis added).

E. Li (Ex. 1008)

148. Chinese Patent Application Publication No. CN1949545 (“Li”), published in 2007, is titled “Crystalline Silicon Solar Cell with Novel Structure.”

Ex. 1008, Cover.

149. Li’s Abstract states:

A crystalline silicon solar cell adopting an emitting region on a back surface of thin film silicon belongs to a photovoltaic cell with a novel structure. The crystalline silicon solar cell is characterized in that a layer of silicon thin film is deposited on a back surface of an N-type

monocrystalline silicon substrate to form a heterogeneous PN junction so as to replace a homogeneous PN junction prepared on a front surface of the cell by a conventional diffusion method. The silicon thin film deposited in the present invention can be an amorphous thin film, a microcrystalline thin film, or a nanocrystalline thin film. The heterogeneous PN junction in the present invention can be a P-type silicon thin film directly deposited on the N-type monocrystalline silicon, or can also be a P-type silicon thin film deposited on a layer of intrinsic silicon thin film which is first deposited on the N-type monocrystalline silicon. By adopting the cell structure in the present invention, cell efficiency can reach 20% or above.

Ex. 1008, Abstract.

150. In its “Background Art” section, Li describes conventional crystalline silicon solar cells as having a homogenous PN junction and being disadvantaged by high-temperature diffusion:

Crystalline silicon solar cells account for more than 90% of photovoltaic market shares in the global world. Such cells generally adopt P-type crystalline silicon to form an N-type emitting region through high-temperature diffusion and belong to homogeneous PN junction solar cells. However, such cells have the disadvantages that the high-temperature diffusion may cause more defects in silicon materials, and when pollution is caused in a high-temperature process, cell efficiency will be greatly reduced. Thus, higher requirements are put forward for both materials and a production environment. In addition, back surfaces of such cells are free of effective passivation

and an effective light trapping structure. Thus, recombination on the back surfaces is relatively serious, and a part of light penetrates an active region of the cells and is not absorbed. These disadvantages are reasons that limit improvement of the efficiency of conventional solar cells.

Ex. 1008, 3.

151. As its name implies, a homogeneous PN junction is a junction formed by the same materials on both sides of the junction. Thus, for example, according to Li's description, Froitzheim would have a homogeneous PN junction because its emitter layer is "a non-alloyed p-type doped region at the rear side of the body layer [substrate] and forming a p/n-junction therewith." Ex. 1004, Abstract.

152. Because the emitter layer is formed on the substrate, high anneal temperature (typically above 850° C) is used in homogeneous PN junctions to drive in/diffuse dopants. The dopants are diffused into the substrate to form the doped region. *See, e.g.*, Ex. 1004, ¶¶40-42 (disclosing high anneal temperature to diffuse boron into "the rear surface of the body layer" to form a "p-type doped region").

153. Li also describes "amorphous silicon/crystalline silicon heterojunction solar cell (HIT cell)" and its advantages:

In recent years, an amorphous silicon/crystalline silicon heterojunction solar cell (HIT cell) has been developed by Sanyo in

Japan. Such cell adopts an N-type monocrystalline silicon wafer and deposits an amorphous silicon thin film on a surface of the silicon wafer. An emitting region is a P-type amorphous silicon thin film deposited on a front surface of the silicon wafer. A front surface structure of the cell is a metal grid/transparent conductive thin film (TCO)/P-type amorphous silicon/intrinsic amorphous silicon/monocrystalline silicon wafer. The structure makes full use of a good surface passivation effect of the amorphous silicon, and the efficiency of the prepared cell reaches 20% or above.

Adoption of N-type silicon has the advantages that the N-type silicon wafer generally has a long minority carrier lifetime, and the silicon wafer with high quality is easy to obtain. The N-type silicon is also more tolerant to impurities than the P-type silicon. For solar cells, P-type silicon cells will have efficiency attenuation to a certain degree after long-term exposure to light, and the attenuation is related to boron-oxygen defects in materials. After the N-type silicon is used, the problem no longer exists.

Adoption of the amorphous silicon emitting region has the advantage that the amorphous silicon has a good surface passivation effect. Moreover, a deposition temperature is low (200°C), and a process is relatively simple, such that a high-temperature process is avoided, and the manufacturing cost of the cell is reduced.

Ex. 1008, 3.

154. As its name implies, a heterogenous PN junction is a junction formed by two different materials on the two sides of the junction . In Li's case, both sides are silicon, but they have different crystal structures:

A layer of silicon thin film is deposited on a back surface of N-type monocrystalline silicon to form an emitting region (a P-type silicon thin film can be deposited on a layer of intrinsic silicon thin film which is first deposited on the back surface of the N-type monocrystalline silicon, or a P-type silicon thin film can be directly deposited on the N-type monocrystalline silicon).

Ex. 1008, 4; *see also id.* at Abstract.

155. Because the emitter layer is already of P-type, high anneal temperature (used to drive in/diffuse dopants) is not used in construction of Li's heterogeneous PN junction structure. Thus, Li teaches that its heterogeneous PN junction "is prepared by a low-temperature deposition method, which avoids a conventional diffusion process at 800-1000°C." Ex. 1008, 4.

156. Li describes the purported benefits of its purported invention:

A technical means adopted in the present invention is to achieve an emitting region by depositing the silicon thin film on the back surface of the cell. Compared with a P-type silicon wafer diffused N-type emitting region used in most factories at present, the N-type silicon can effectively reduce the generation of boron-oxygen defects under illumination and resulting attenuation of conversion efficiency. In addition, a PN junction is prepared by a low-temperature deposition

method, which avoids a conventional diffusion process at 800-1000°C. Such high-temperature process will cause more defects or contamination in a silicon material, which will affect the improvement of cell efficiency. In addition, the silicon thin film deposited on the back surface of the silicon wafer, whether it is amorphous silicon, microcrystalline silicon, or nanocrystalline silicon, can achieve a passivation effect on the back surface, thereby improving the cell efficiency. At least one surface of the front surface or the back surface of the structure can be subjected to texturing treatment to reduce light reflection and improve a light trapping effect, which is conducive to improving the photoelectric conversion efficiency of the cell. An anti-reflection film can be prepared on the texturing surface to further improve the photoelectric conversion efficiency of the cell.

Ex. 1008, 4.

F. Sheats (Ex. 1012)

157. US Patent Application Publication No. 2006/0157103 (“Sheats”), published in 2006, is titled “Optoelectronic Architecture Having Compound Conducting Substrate Cross-Reference to Related Application.” Ex. 1012, Cover.

158. Sheats’ Abstract states:

Optoelectronic device modules, arrays optoelectronic device modules and methods for fabricating optoelectronic device modules are disclosed. The device modules are made using a starting substrate having an insulator layer sandwiched between a bottom electrode made of a flexible bulk conductor and a conductive back plane. An

active layer is disposed between the bottom electrode and a transparent conducting layer. One or more electrical contacts between the transparent conducting layer and the back plane are formed through the transparent conducting layer, the active layer, the flexible bulk conductor and the insulating layer. The electrical contacts are electrically isolated from the active layer, the bottom electrode and the insulating layer.

Ex. 1012, Abstract.

159. According to Sheats, solar cells are one example of optoelectronic devices: “This invention relates to optoelectronic devices and more particularly to mass-manufacture of optoelectronic devices such as solar cells.” Ex. 1012, ¶2.

160. Sheats discusses the need to connect optoelectronic devices (connecting solar cells into solar cell arrays), and the problems that come with it:

[0005] A further problem associated with existing solar fabrication techniques arises from the fact that individual optoelectronic devices produce only a relatively small voltage. Thus, it is often necessary to electrically connect several devices together in series in order to obtain higher voltages in order to take advantage of the efficiencies associated with high voltage, low current operation (e.g. power transmission through a circuit using relatively higher voltage, which reduces resistive losses that would otherwise occur during power transmission through a circuit using relatively higher current).

...

[0007] A further problem associated with series interconnection of optoelectronic devices arises from the high electrical resistivity associated with the TCO used in the transparent electrode. The high resistivity restricts the size of the individual cells that are connected in series. To carry the current from one cell to the next the transparent electrode is often augmented with a conductive grid of busses and fingers formed on a TCO layer. However, the fingers and busses produce shadowing that reduces the overall efficiency of the cell. In order for the efficiency losses from resistance and shadowing to be small, the cells must be relatively small. Consequently, a large number of small cells must be connected together, which requires a large number of interconnects and more space between cells. Arrays of large numbers of small cells are relatively difficult and expensive to manufacture. Further, with flexible solar modules, shingling is also disadvantageous in that the interconnection of a large number of shingles is relatively complex, time-consuming and labor-intensive, and therefore costly during the module installation process.

Ex. 1012, ¶¶5, 7.

161. Sheats discusses the drawbacks of solar cell arrays manufactured from a single substrate, where holes are cut into the substrate to form multiple solar cells:

[0010] For example FIG. 6A illustrates a portion of a prior art solar cell array **600**. The array 600 is manufactured on a flexible insulating substrate 602. . .

[0011] FIG. 6B depicts another prior art array **620** that is a variation on the array **600**. The array **620** is also manufactured on a flexible insulating substrate **622**. . .

[0012] There are two significant drawbacks to manufacturing solar cell arrays as shown in FIGS. 6A-6B. First, the metal layers are deposited by sputtering, which is a vacuum technique. Vacuum techniques are relatively, slow, difficult and expensive to implement in large scale roll-to-roll manufacturing environments. Secondly, the manufacturing process produces a monolithic array and sorting of individual cells for yield is not possible. This means that only a few bad cells can ruin the array and therefore increase cost. In addition, the manufacturing process is very sensitive to the morphology and size of the holes. Since the front to back electrical conduction is along the sidewall of the hole, making the holes larger does not increase conductivity enough. Thus, there is a narrow process window, which can add to the cost of manufacture and reduce yield of usable devices. Furthermore, although vacuum deposition is practical for amorphous silicon semiconductor layers, it is impractical for highly efficient solar cells based, e.g., on combinations of Copper, Indium, Gallium and Selenium or Sulfur, sometimes referred to as CIGS cells. To deposit a CIGS layer, three or four elements must be deposited in a precisely controlled ratio. This is extremely difficult to achieve using vacuum deposition processes.

Ex. 1012, ¶¶10-12 (emphasis added); *see also id.* at Figs. 6A, 6B.

162. Sheats' purported solutions all relate to solar cell arrays (structure of at least two solar cells):

[0015] FIG. 1A is a vertical cross-sectional schematic diagram of a portion of an array of optoelectronic devices according to an embodiment of the present invention;

...

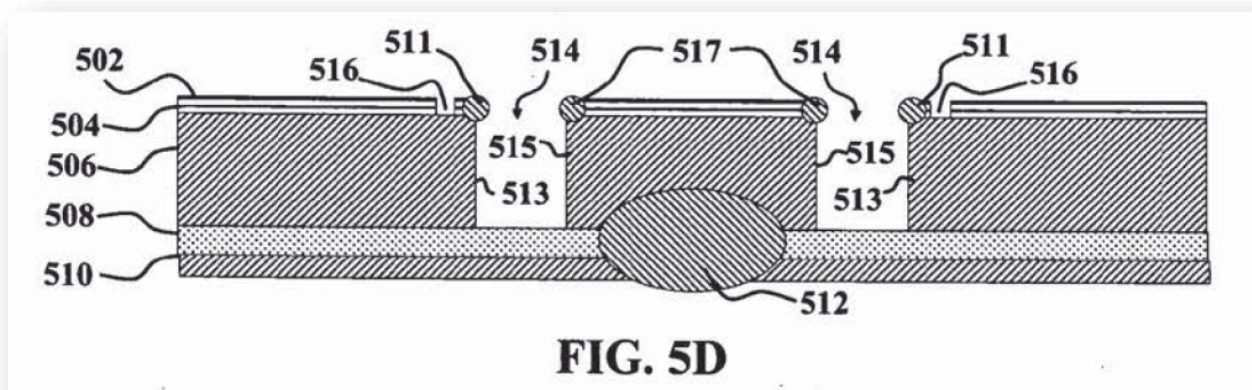
[0018] FIG. 2 is a sequence of schematic diagrams illustrating fabrication of an array of optoelectronic devices according to an embodiment of the present invention.

[0019] FIG. 3 is an exploded view schematic diagram illustrating fabrication of an array of optoelectronic devices according to an alternative embodiment of the present invention.

[0020] FIG. 4A is an exploded view schematic diagram illustrating fabrication of an array of optoelectronic devices according to another alternative embodiment of the present invention.

Ex. 1012, ¶¶15, 18-20, 40; *see also id.* at ¶40 (discussing fabrication of the two solar cells); *id.* at Fig. 1A (illustrating two solar cells).

163. One of Sheats' embodiments includes a single structure separated into multiple solar cells by a trench (514). *Id.* at Figs. 5A-I; *see also id.* at ¶¶56-60.



Ex. 1012, Fig. 5D.

In this embodiment, Sheats discusses, among other things, cutting an isolation trench 516 to prevent short circuit between the separated solar cells at points 511 and 517 during the formation of trench 514:

The process of forming the isolation trench may cause electrical short-circuits 511, 517 between the transparent conductive layer 502 and the bottom electrode 506. To electrically isolate undesirable short circuits 511 formed on an outside wall 513 of the trench 514 an isolation trench 516 is formed through the transparent conductive layer and the active layer to the bottom electrode 506 as shown in FIG. 5D. The isolation trench 516 surrounds the closed-loop trench 514 and electrically isolates the short circuits 511 on the outside wall 513 of the trench from the rest of the structure 500. A laser scribing process may form the isolation trench 516. A lesser thickness of material being scribed reduces the likelihood of undesired short circuits resulting from formation of the isolation trench 516.

Ex. 1012, ¶59.

**XII. PETITIONER FAILED TO DEMONSTRATE A REASONABLE
LIKELIHOOD OF SUCCESS ON THE MERITS OF GROUNDS I TO
V**

**A. Ground I: Petitioner’s Challenge of Claims 1-4 and 6-12 Based on
Froitzheim and Gan Fails**

*1. A POSITA Would Not Have Had a Reasonable Expectation of
Success in Combining Froitzheim and Gan*

164. In my opinion, a POSITA would not have combined Froitzheim and
Gan.

a. The Gan Thesis Failed to Reliably Implement Gan’s
Interfacial Oxide Layer

165. In my opinion, a POSITA would not have had a reasonable
expectation of success in modifying the structure of Froitzheim to include the
interfacial oxide layer of Gan.

166. Gan proposes forming a tunnel oxide layer and then breaking it
slightly to achieve acceptable values for J_o and ρ_c . However, the Gan Thesis
explains that this requires a degree of precision in forming and breaking the oxide
layer that Gan never consistently achieved and documents the consistent failure to
do so.

167. The Gan Thesis documents consistent failures to achieve Gan’s
theoretical results. In its “Conclusion” chapter, the Gan Thesis states:

In this chapter, we found that a consistent result of ρ_c is difficult to
reproduce for the polysilicon emitter with a thermally grown

interfacial oxide. This is mainly attributed to the fact that our thin-oxide growth recipe is not reliable. With the same oxidation schedule, a wide variation of oxide thicknesses have been found for different times. Experimentally, the interfacial oxide breakup was also found to be dependent on the oxide thickness critically. Such an oxide-thickness dependence of the breakup process can be explained by a “silicon cluster nucleation” process. In order to have predictable results, it appears that a precise control of the oxide thickness is necessary.

Ex. 2003, 116-17 (emphasis added).

168. The Gan Thesis was trying to get a low J_o of 1×10^{-14} A/cm² to 2×10^{-14} A/cm². For example, in its Abstract, the Gan Thesis states:

Recently, a single-crystal silicon point-contact solar cell has been shown to have energy conversion efficiency of 28% at 100 suns. Such a cell has been fully analyzed; and it appears that the cell efficiency can be increased more than one absolute percentage by eliminating the emitter recombination. In order to do this, the emitter saturation current density (J_o), which characterizes the dopant-diffused region recombination, of both n- and p- type emitters has to be kept around 2×10^{-14} A /cm². Unfortunately, such low J_o cannot be obtained by the diffused emitters formed in the single-crystal silicon. Polysilicon emitters, n-type in particular, have been reported to have very low J_o ($\sim 1 \times 10^{-14}$ A/cm²); therefore, they can be a very useful substitute for the diffused emitters for high efficiency solar cells. Nevertheless, some problems in the polysilicon emitter itself have to be resolved

before they can be used in silicon concentrator solar cells. One is the high contact resistance. For the polysilicon emitter to have low J_o , a thin interfacial oxide has to be placed in between the polysilicon and the substrate. However, such an interfacial oxide also causes high contact resistance ($\rho_c \geq 1 \times 10^{-4} \Omega\text{-cm}^2$). Another is the high J_o of the p-type polysilicon emitter. Prior to this work, the lowest J_o of the p-type polysilicon emitter reported was $\sim 3 \times 10^{-13} \text{ A/cm}^2$ which is high for a solar cell application. The other is the complexity of the oxide breakup during a high temperature anneal, which appears to increase the J_o of the polysilicon emitter. In this work, both the minority and the majority carrier transport of the polysilicon emitter are closely examined. Theoretically, a model was proposed to make the polysilicon emitter with both low J_o ($\sim 3 \times 10^{-14} \text{ A/cm}^2$) and low contact resistance ($\rho_c \leq 1 \times 10^{-5} \Omega\text{-cm}^2$). Experimentally, such polysilicon emitters for both types were successfully demonstrated.

Ex. 2003, Abstract (emphasis added).

169. The Gan Thesis further states:

The cell efficiency, as shown in the figure, is hardly affected by the emitter recombination when J_o is below $1 \times 10^{-14} \text{ A/cm}^2$; however, it falls off rapidly as the J_o increases over $1 \times 10^{-14} \text{ A/cm}^2$. If we allow the emitters to cover the entire backside surface, then the total J_o is $4.5 \times 10^{-13} \text{ A/cm}^2$, and the cell efficiency will be limited to about 27% at the incident power density of 10 watts/cm². In contrast, the efficiency of the point contact cell is increased to 28% by scaling the

emitter areal-coverage fraction to 20% such that the total J_o of the cell is effectively reduced to about 1×10^{-13} A/cm².

Ex. 2003, 3 (emphasis added).

170. The Gan Thesis also states:

As we reduce the J_o down to 1×10^{-14} A /cm², and enlarge the emitter contact area, the cell performance is improved globally. This is shown in Figure 2.5 where the cell efficiency of three IBC cells are plotted against the incident power density. In the figure, cell (a) has 5 μ m line contact and J_o of 4.5×10^{-13} A /cm², cell (b) has the same contact size as cell (a) but J_o is 1×10^{-14} A/cm², and cell (c) has the same J_o as cell (b) but with wider contact lines—15 μ m. The curve for the cell (b) is less clear, it is first merged with that for cell (c) at low incident power density and change to that for cell (a) at high incident power density. By comparing cell (a) with (b), the better performance of cell (b) results from the lower J_o which is consistent with the results shown in Figure 1.3. However, the advantage of low J_o diminishes as the incident power density increases over 50 watts/cm².

The comparison between cell (b) and (c) is even more interesting. First, the cell efficiency of both cells stays the same at low incident power density, which indicates that the emitter recombination will be negligible as the J_o is below 1×10^{-14} A/cm². Secondly, note that the cell (c) starts to outperform the cell (b) at 10 watts/cm². This implies that the low internal series resistance is important even at the incident power density as low as 10 watts/cm², and becomes more obvious in the regime of high incident power density where the better

current-collection capability of the large-contact cell lessens the power loss through the Auger recombination.

It now becomes obvious to see what an emitter should be for the concentrator solar cells. Low J_o is of course the primary requirement. As shown in Figure 1.2, the total emitter saturation current density below 1×10^{-14} A/cm² shows negligible effect. Take this value and assume the emitter areal coverage fraction is 30% for each type, this means that the J_o of each type of emitters should be around 2×10^{-14} A/cm².

Ex. 2003, 22 (emphasis added).

171. This is understandable because Gan (Ex. 1005) and the Gan Thesis are both trying to solve the same problem, namely a very small and consistent breakup of the interfacial oxide to achieve low J_o .

172. In fact, the Gan Thesis showed that there was no known method for getting the oxide thickness sufficiently reliable to obtain acceptable results based on the following disclosures:

It appears that the oxide breakup depends **critically** on the interfacial oxide thickness. The thin-oxide growth recipe used in this work was not reliable; the oxide thickness between 15 and 20 Å have been found with the same growth condition. As a result, this contributes to the fluctuation of the ρ_c results. It is then clear that a more reliable way of growing the thin oxide is needed.

Ex. 2003, 119 (emphasis added).

Although a thermally grown interfacial oxide seems **essential** for a polysilicon emitter to have both low J_o and ρ_c , the breakup process is still difficult to control. On several occasions, we have encountered reproducibility problems. For example, we find that the ρ_c is quite different between two separate experiments with identical processing conditions. Even worse, solar cells that were made in this study all suffered high contact resistance. The problem is primarily due to insufficient oxide breakup, and is caused by the fluctuation of the thickness of the interfacial oxide.

Ex. 2003, 107 (emphasis added).

Later, in the real solar cell runs, the situation got even worse. The solar cells made in the experiment are the 15- μm -contact-line IBC which have been shown and simulated in Chapter 2. We found that, with the OCVD measurement, the total specific contact resistivity ($p_n + p_p$) was higher than $1 \times 10^{-3} \Omega\text{-cm}^2$. Although the $(J_{on} + J_{op})$ measured from those cells are between 8×10^{-14} and $4 \times 10^{-14} \text{ A/cm}^2$, the cell efficiency is greatly degraded by such a high emitter resistance.

Ex. 2003, 110 (emphasis added).

As shown in the figure, the cell is in fact plagued by two things: the high surface recombination velocity ($S = 58 \text{ cm/sec}$), and high emitter resistance ($\rho_{cm} + \rho_{cp} = 1 \times 10^{-3} \Omega\text{-cm}^2$). . . From the low emitter recombination and high emitter resistance, it is clear that the interfacial oxide did not break as expected.

Ex. 2003, 110; *see also id.* at 111 (“Although these results can be attributed to many other reasons, the following experiment shows that the effect of the oxide thickness cannot be ignored. This, combined with the non-reliable oxide-growth recipe gives rise to the mishap of our solar-cell runs.”); *id.* at 114 (“It becomes clear that the wide fluctuation of our results is mainly due to the poor control over the oxide thickness.”) (emphasis added); *id.* at 114-17 (“[W]e found that a consistent result of ρ_c is difficult to reproduce for the polysilicon emitter with a thermally grown interfacial oxide. This is mainly attributed to the fact that our thin-oxide recipe is not reliable.”) (emphasis added); *id.* at 56 (“With a window so narrow, it is not possible to have good control over the characteristics of a polysilicon SIS emitter.”).

173. In my opinion, a POSITA would have considered Gan with the benefit of the Gan Thesis and determined that the experiments discussed in Gan produced unreliable results, created “mishap[s],” and suffered from reproducibility problems.

174. The Gan Thesis documented its own failure to implement the polysilicon emitter and interfacial oxide structure in a real solar cell:

Later, in the real solar cell runs, the situation got even worse. The solar cells made in the experiment are the 15- μm -contact-line IBC which have been shown and simulated in Chapter 2. We found that, with the OCVD measurement, the total specific contact resistivity ($\rho_n + \rho_p$) was higher than $1 \times 10^{-3} \Omega\text{-cm}^2$. Although the (J_{on}

+ J_{op}) measured from those cells are between 8×10^{-14} and 4×10^{-14} A/cm², the cell efficiency is greatly degraded by such a high emitter resistance. . .

As shown in the figure, the cell is in fact plagued by two things: the high surface recombination velocity ($S = 50$ cm/sec), and high emitter resistance ($\rho_n + \rho_p = 1 \times 10^{-3} \Omega\text{-cm}^2$). . .

From the low emitter recombination and high emitter resistance, it is clear that the interfacial oxide did not break as we expected.

Ex. 2003, 110.

175. In my opinion, in the Gan Thesis, the author Gan attempted to implement the structure of Gan (Ex. 1005) in a real solar cell, but failed to do so reliably. Thus, a POSITA would not have been motivated to combine Gan's test structure with Froitzheim's solar cell.

b. Polysilicon Emitters and Tunnel Oxide Layers Were Not Known Elements in Solar Cells

176. Petitioner's assertion that fabricating Froitzheim's solar cell with Gan's polysilicon emitters and interfacial oxide "was simply substituting one known element for another to obtain predictable results," Paper 3, 34, is not supported by any references that show a POSITA how to add an interfacial oxide layer (tunnel oxide) to a solar cell.

177. First, Petitioner cites “Ex.1005-Gan, 246.” As discussed in § XI.B, Gan does not teach the fabrication of a solar cell, but rather, a test device that does not even have a PN junction.

178. Second, Petitioner cites “Ex.1006-Borden-575, [0026].” That paragraph disclose an optional tunnel oxide layer grown in Borden-575’s contact holes, which do not exist in the Froitzheim-Gan combination. *See* Paper 3, generally; *see also* Ex. 2029, 246:4-10. And importantly, Borden-575 admits solar cells with tunnel oxides “have not been commercially introduced, possibly because of the difficulty of reliably forming a thin tunnel oxide.” Ex. 1006, ¶5.

179. Third, Petitioner cites “Ex.1004-Froitzheim, [0030].” Neither this paragraph nor the rest of Froitzheim mention interfacial or tunnel oxide. Instead, Froitzheim’s [0030] discloses a front surface passivation layer 18 that may be an oxide.

180. Fourth, Petitioner cites “Ex.1015-Swanson, 2:50-53.” This portion of Swanson mentions adjusting the thickness of a back side tunnel oxide, but does not teach a POSITA how to add one to a solar cell. Swanson mentions forming a tunnel oxide layer on the back surface, but does not mention how.

2. *The Proposed Froitzheim-Gan Combination Would Not Have Met Limitations in Claim 12 of the '516 Patent*

181. The proposed Froitzheim-Gan Combination does not include backside contacts with “silver formed over a layer of silicon dioxide” as recited in claim 12 of the '516 patent.

182. Petitioner asserts that Froitzheim’s passivation layer is applied before contact formation, and incorrectly concludes Froitzheim backside contact must be formed over the passivation layer. Paper 3, 51 (citing Ex. 1004 ¶50).

183. In reality, Froitzheim discloses forming metal contacts by firing a paste. If the passivation layer is applied before contact formation, as Petitioner asserts, then the firing would cause metal contacts to form between the passivation layer. For example, Froitzheim discloses that its metal contacts are formed by screen printing and firing:

[0048] Front and rear side contacts are preferably screen-printed in an industrial production process, and contacting is done at elevated temperatures. These can be 700-800 degree centigrade, but lower temperatures are also possible.

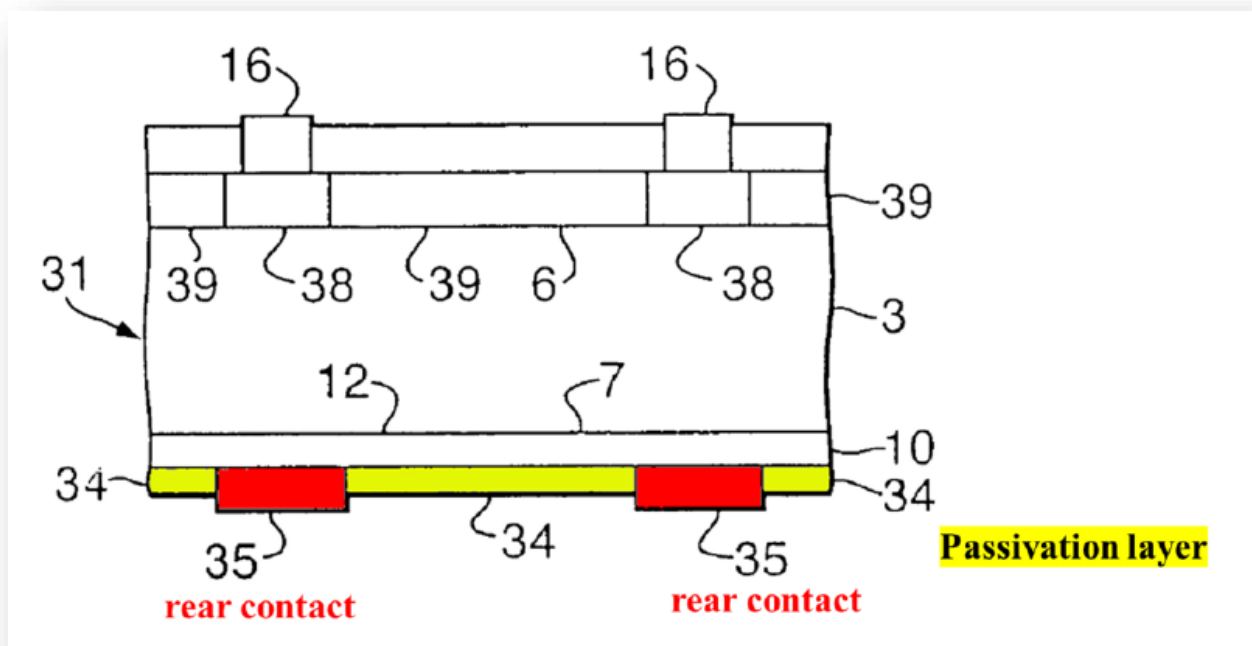
[0049] The squeegee paste for rear side contacts can contain silver particles, filler, oxides, and also an amount of Aluminium. It will be understood that at firing the paste in order to make electrical contact with the p region, a thin alloy might be formed at the interface between the p-doped region and the contact, but that the p-doped region itself towards the p/n junction is still a non-alloyed p-doped

region. The front side contact is also suitably produced by screen printing and firing.

Ex. 1004, ¶¶48-49 (emphasis added).

184. I note that Petitioner’s argument regarding, and Froitzheim’s description of, front contact formation also apply to Froitzheim’s rear contact formation. Froitzheim discloses that both contacts are made by screen printing and firing. Ex. 1004, ¶49 (following description of formation of rear contact, disclosing “[t]he front side contact is also suitably produced by screen printing and firing.”).

185. Froitzheim also discloses and illustrates that its passivation layer 34 is arranged “[b]etween the [rear contact 35] fingers.” Ex. 1004, ¶33.



Paper 3, 51 (citing Ex. 1004, Fig. 3) (annotations in Petition).

186. As shown above, the metal contacts (purple) are formed between the passivation layer (green), with no portion of the purple components being positioned directly above (or below) the green components. This is the situation after firing, when the metal paste fires through the passivation layer. Before firing, the metal paste lies on top of the passivation layer.

187. In my opinion, where Froitzheim's passivation is applied before contact formation, as Petitioner suggests, Paper 3, 51, a POSITA would have understood that a paste is fired through the passivation layer.

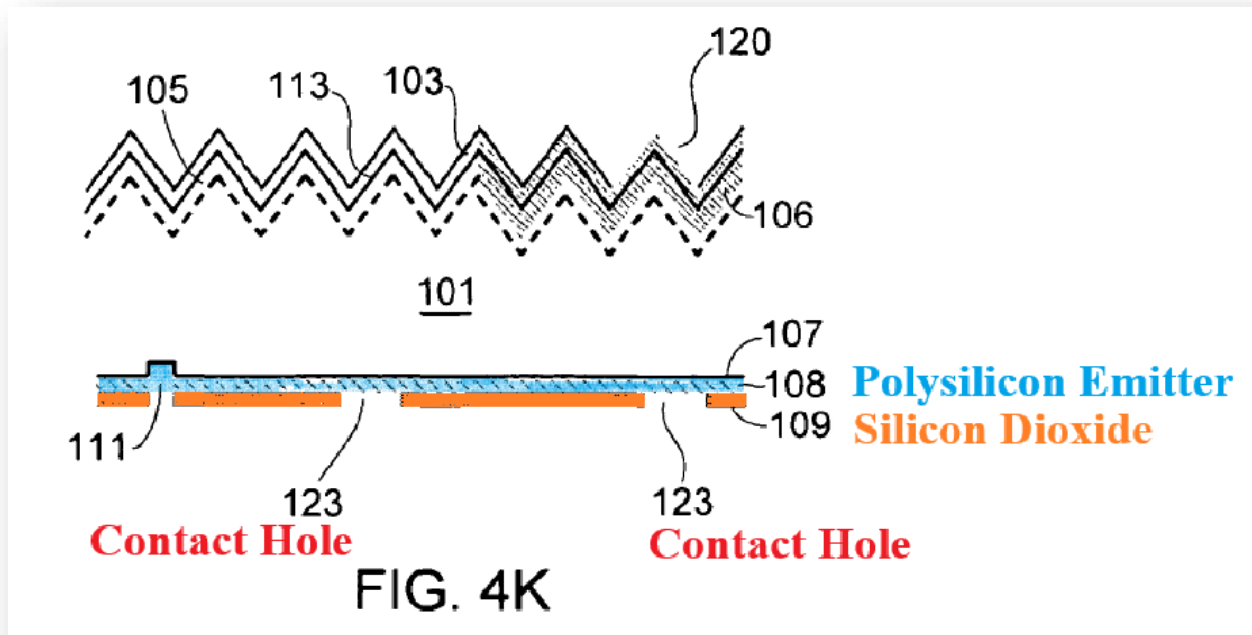
188. In contrast, claim 12 requires that the backside contact be formed over a layer of silicon dioxide. Ex. 1001, 6:63-65. Although the claim language speaks for itself, the '516 patent also provides a helpful description and illustration of the contact forming over the silicon dioxide layer, in contrast to Froitzheim.

189. The '516 patent describes that, first, contact holes 120 and 123 are formed:

In FIG. 4K, contact holes 120 and 123 are formed by removing exposed portions of the silicon nitride layer 103 and the silicon dioxide 109 in a contact etch step. In one embodiment, the contact holes 120 are formed by using a selective etch process that removes exposed portions of the silicon nitride layer 103 and stops on the substrate 101. The same etch process removes exposed portions of the

silicon dioxide 109 and stops on the polysilicon emitter 108. In one embodiment, the etch process comprises a BOE (buffered oxide etch).

Ex. 1001, 5:38-47 (emphasis added).



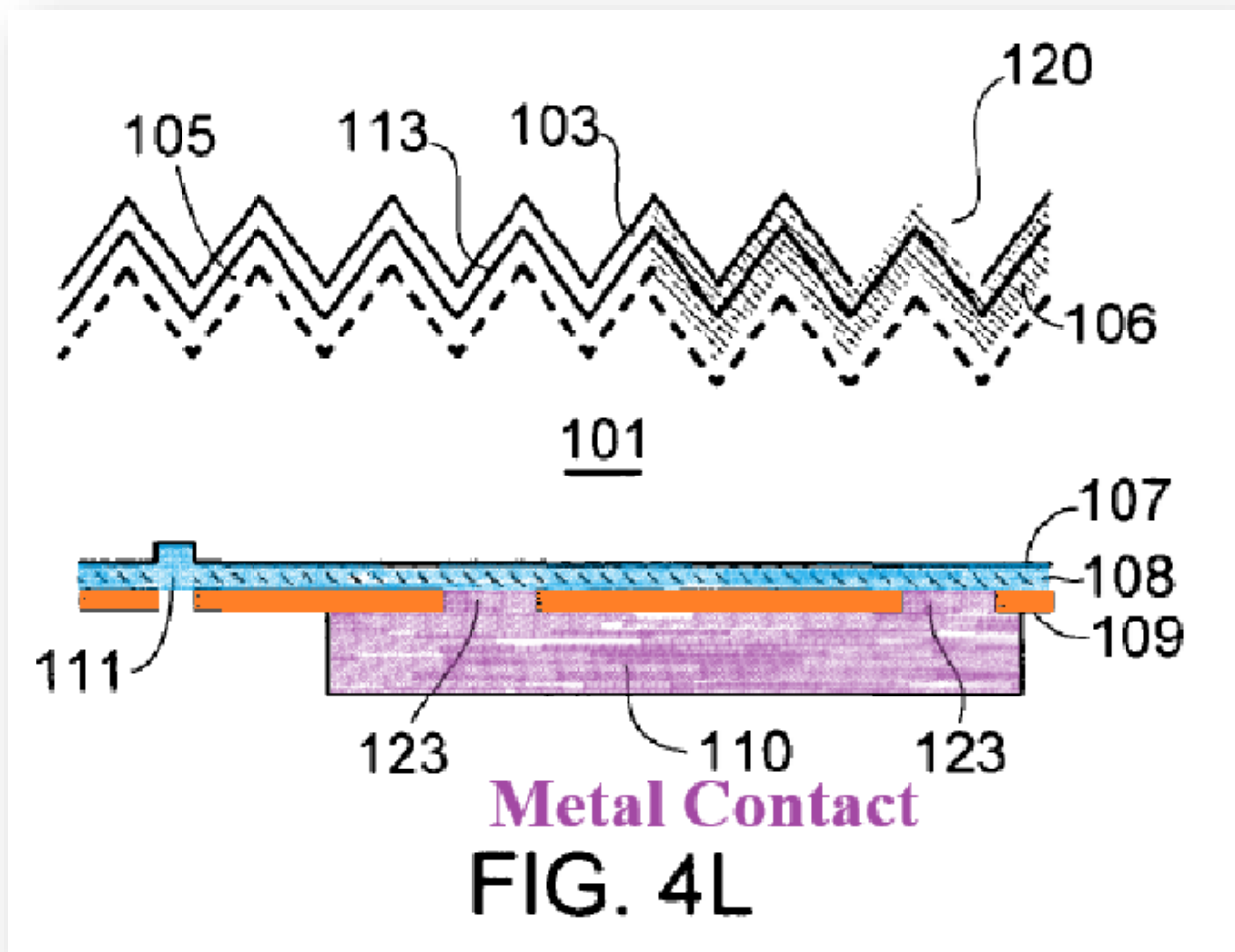
Ex. 1001, Fig. 4K (annotated).

190. The '516 patent describes that, next, metal contact 110 is formed to fill the contact holes 123 and make electrical connection to the polysilicon emitter 108:

In FIG. 4L, the metal contact **110** is formed on the silicon dioxide layer **109** to fill the contact holes **123** and make electrical connection to the polysilicon emitter **108**. The metal contact **110** may be formed using a printing process. The metal contact **110** may comprise silver, which, together with the silicon dioxide layer **109**, makes an excellent

backside infrared reflector. Other metals may also be used as a metal contact **110**, such as aluminum, for example.

Ex. 1001, 5:48-55 (emphasis added).



Ex. 1001, Fig. 4L (annotated).

191. As shown above, while parts of the metal contact 110 are formed over the silicon dioxide layer 109, the rest directly contacts the polysilicon emitter 108.

A POSITA would have known that the direct physical contact of the metal contact 110 and the polysilicon emitter 108 direct is needed to establish current flow.

192. For this same reason, Froitzheim specifies that its squeegee paste is fired “to make electrical contact with the p region.” Ex. 1004, ¶49.

193. Thus, in the proposed Froitzheim-Gan combination, the rear contact would not be formed on a silicon dioxide passivating layer as Petitioner asserts, and as a result, would not meet the limitation of “the second metal contact comprises silver formed over a layer of silicon dioxide” as recited in claim 12. Ex. 1001, 6:63-65.

B. Grounds II, IV: Petitioner’s Challenges of Claim 5 Based on Froitzheim, Gan/Borden-575, and Sheats Fail

1. Edge Isolation Would Have Been Superfluous in Any Proposed Froitzheim Combinations

194. Edge isolation is optional in Froitzheim’s invention: “If required after the formation of the n+ doped layer, a separation at the edge of the wafer may be performed, e.g. in a plasma.” Ex. 1004, ¶47.

195. Petitioner’s expert testified that Froitzheim discloses edge isolation, and I agree:

A So Paragraph 47 of Froitzheim describes what is generally referred to as edge isolation. And it’s a method to make sure that there aren’t any shunts, which is the word we use for electrical shorts, in the positive and negative -- positive and negative regions or P-type and

N-type regions inadvertently touch each other. And Froitzheim is describing a method to make sure that that doesn't happen, your edge isolation.

Ex. 2029, 157:19-158:5.

196. Thus, in my opinion, if edge isolation is needed, then Froitzheim discloses one. Ex. 1004, ¶47.

197. Froitzheim's optional edge isolation is consistent with Petitioner's reference Houser, which teaches that there are "several approaches to avoid" edge isolation. Paper 3, 62 (citing Ex. 1063). Houser states:

A very simple but important step in most solar cell processes is the edge isolation. There are several approaches to avoid this step (co-diffusion [1], diffusion barriers by means of printing [2] or silicon nitride (SiN), one-sided emitter, . . .) but most solar cells still have to be isolated. In industry the plasma etching of wafer stacks is very common, but this step is not in-line capable and undesired chemicals have to be used. Therefore there is a demand for other possibilities, which can be performed inline, are easy to implement and cheap to realize. Besides the physical ability of each technique to remove the shunts also the advantages and disadvantages for an industrial usage are for interest.

Ex. 1063, 1739 (emphasis added).

198. Thus, in my opinion, a POSITA would not “have been motivated to isolate the edge of Froitzheim’s modified solar cell to prevent short circuits.” Paper 3, 62.

199. Indeed, if modifying Froitzheim’s solar cell (in which edge isolation is optional) with Gan would cause short circuit concerns, and a POSITA would not have combined the two references in the first place. A POSITA would not have made the modification to create additional problems (short circuits) that require additional manufacturing steps (edge isolation) to resolve.

2. *Even If Additional Edge Isolation Is Justified, a POSITA Would Not Have Used Trenches*

200. Petitioner’s own references teach that trenches are one of many edge isolation techniques, and not the most common one.

201. According to Houser (Ex. 1063), plasma etching is the most common technique. For example, in its Abstract, Houser states:

In most industrial type solar cell processes the edge isolation is an important step. After most emitter diffusion techniques, especially the POCl₃ diffusion, the front contact is connected with the back contact through the emitter around the edge of the solar cell. As a common technique in industry this shunt is removed by plasma etching of the wafer stack. Other techniques which were investigated are: the grinding of the wafer edge with sandpaper, the cutting of isolation trenches with a wafer dicing saw and the laser separation by inserting

trenches, the latter two techniques applied on both sides of the wafer.

All these technologies are compared concerning their impact on the solar cell performance of industrial type screen printed solar cells. Using IV measurement (illuminated and dark), laser beam induce current (LBIC) and lock-in thermography it is shown that isolation by laser still suffers from too low fill factors and sawing, grinding, or plasma etching are preferable. A good correlation between decreasing shunt resistance and increasing amount of detected shunts using in-lock thermography or LBIC is found.

Ex. 1063, Abstract (emphasis added).

202. The “Motivation” section includes the same reference to Houser that plasma etching is common:

A very simple but important step in most solar cell processes is the edge isolation. There are several approaches to avoid this step (co-diffusion [1], diffusion barriers by means of printing [2] or silicon nitride (SiN), one-sided emitter, . . .) but most solar cells still have to be isolated. In industry the plasma etching of wafer stacks is very common, but this step is not in-line capable and undesired chemicals have to be used. Therefore there is a demand for other possibilities, which can be performed inline, are easy to implement and cheap to realize. Besides the physical ability of each technique to remove the shunts also the advantages and disadvantages for an industrial usage are for interest.

Ex. 1063, 1739 (emphasis added).

203. In its “Summary” section, Houser again repeats that plasma etching is most common:

In most solar cell processes edge isolation is an important step. In industry this is mostly done by plasma etching of a wafer stack. Because this treatment is not inline capable and unwanted chemicals have to be used, there is a demand for alternatives. In this investigation 7 different techniques for edge isolation were examined using IV, LBIC and lock-in thermography measurements.

Ex. 1063, 1742 (emphasis added).

204. Another one of Petitioner’s references, Wenham (Ex. 1066), agrees. Paper 3, 62 (citing Ex. 1066). For example, in its “Edge isolation” section, Wenham states:

In the laboratory all edge isolations are carried out by scribing the rear of the solar cell and then cleaving off the edges. This gives superior results to a front surface laser scribed edge junction isolation and is essential for prototype small area cells which have been made. For larger cells however, leakage around the edge is not as important thus making a front surface scribe suitable.

Another alternative is to scribe a groove (200-300 μm) right around the wafer edge at the same time as the grooves are put in for the metal. The edge bits will then require cleaving at the end and will need to be done with considerable care because they become somewhat more difficult to snap after the scribe has been cleaned out with the sodium hydroxide etch.

Finally, plasma etched edge isolation can be carried out by coin stacking the solar cells in the plasma system. This is the technique believed to be used very effectively by several commercial enterprises.

Ex. 1066, 7:23-41 (emphasis added).

205. I also note that Froitzheim discloses plasma etching: “If required after the formation of the n+ doped layer, a separation at the edge of the wafer may be performed, e.g. in a plasma.” Ex. 1004, ¶47 (emphasis added).

206. Petitioner’s expert testified that the last word of Froitzheim paragraph 47 refers to plasma etching, and I agree:

Q The last word of Paragraph 47 is plasma. Is this referring to plasma etching?

A I think that that is likely. That is how I read it. Removal of material via plasma are commonly called etching. This is one way to do edge isolation, and that's why Froitzheim introduces it with a e.g., for example.

Ex. 2029, 159:14-20.

207. Even if a POSITA were to ignore the most common technique, plasma etching, the POSITA would still have been aware of yet additional alternatives.

208. For example, in its “Summary” section, Houser states that it investigated seven different edge isolation techniques:

In most solar cell processes edge isolation is an important step. In industry this is mostly done by plasma etching of a wafer stack. Because this treatment is not inline capable and unwanted chemicals have to be used, there is a demand for alternatives. In this investigation 7 different techniques for edge isolation were examined using IV, LBIC and lock-in thermography measurements.

Ex. 1063, 1742 (emphasis added).

209. Wenham discloses two alternatives:

In the laboratory all edge isolations are carried out by scribing the rear of the solar cell and then cleaving off the edges. This gives superior results to a front surface laser scribed edge junction isolation and is essential for prototype small area cells which have been made. For larger cells however, leakage around the edge is not as important thus making a front surface scribe suitable.

Another alternative is to scribe a groove (200-300 μm) right around the wafer edge at the same time as the grooves are put in for the metal. The edge bits will then require cleaving at the end and will need to be done with considerable care because they become somewhat more difficult to snap after the scribe has been cleaned out with the sodium hydroxide etch.

Finally, plasma etched edge isolation can be carried out by coin stacking the solar cells in the plasma system. This is the technique believed to be used very effectively by several commercial enterprises.

Ex. 1066, 7:23-41 (emphasis added).

210. Another one of Petitioner’s references, Luque, Paper 3, 62 (citing Ex. 1020, 290), illustrates “[a] typical processing sequence” for solar fabrication based on screen printing. Ex. 1020, Fig. 7.6 (description). As shown below, the “edge isolation” step of that illustration does not involve any trenches.



Ex. 1020, Fig. 7.6.

211. In my opinion, without the guidance of claim 5, a POSITA would not have been motivated to select trenches over the common and popular plasma etching technique and the many other alternatives.

3. *A POSITA Would Not Have Looked to Sheats, Directed to Solar Arrays, for Edge Isolation for a Single Solar Cell*

212. In my opinion, even if a POSITA elected to modify Froitzheim with trenches, the POSITA would still not have looked to Sheats.

213. To be clear, Petitioner claims a POSITA would want “to isolate the edge of Froitzheim’s modified solar cell to prevent short circuits.” Paper 3, 62. To do so, the POSITA would modify Froitzheim to include a trench as taught by

Sheats, specifically “‘an isolation trench 516’ formed through the transparent conductive layer and the active layer.” *Id.* at 60-61.

214. In my opinion, in a single solar cell (such as Froitzheim), edge isolation electrically isolates the front and rear surfaces of the solar cell, preventing unwanted current pathways or shunts that may cause short circuit within.

215. In my opinion, Sheat’s isolation trench 516 is to prevent short circuit between solar cells in array formation.

a. Sheats Is About Solar Cell Arrays

216. In my opinion, a POSITA would have understood the distinction between the isolation trench 516 of Sheats and the edge isolation trench 111 of the ’516 patent if provided with the full context of Sheats.

217. Sheats is directed to the interconnection of solar cells to obtain higher output voltages. Sheats teaches that individual cells must be connected to produce enough electricity:

A further problem associated with existing solar fabrication techniques arises from the fact that individual optoelectronic devices produce only a relatively small voltage. Thus, it is often necessary to electrically connect several devices together in series in order to obtain higher voltages in order to take advantage of the efficiencies associated with high voltage, low current operation (e.g. power transmission through a circuit using relatively higher voltage, which

reduces resistive losses that would otherwise occur during power transmission through a circuit using relatively higher current).

Ex. 1012, ¶5.

218. Sheats comments on the problems that exist in conventional interconnected solar cells:

[0007] A further problem associated with series interconnection of optoelectronic devices arises from the high electrical resistivity associated with the TCO used in the transparent electrode. . .

[0008] To overcome this, optoelectronic devices have been developed with electrically isolated conductive contacts that pass through the cell from a transparent “front” electrode through the active layer and the “back” electrode to an electrically isolated electrode located beneath the back electrode . . .

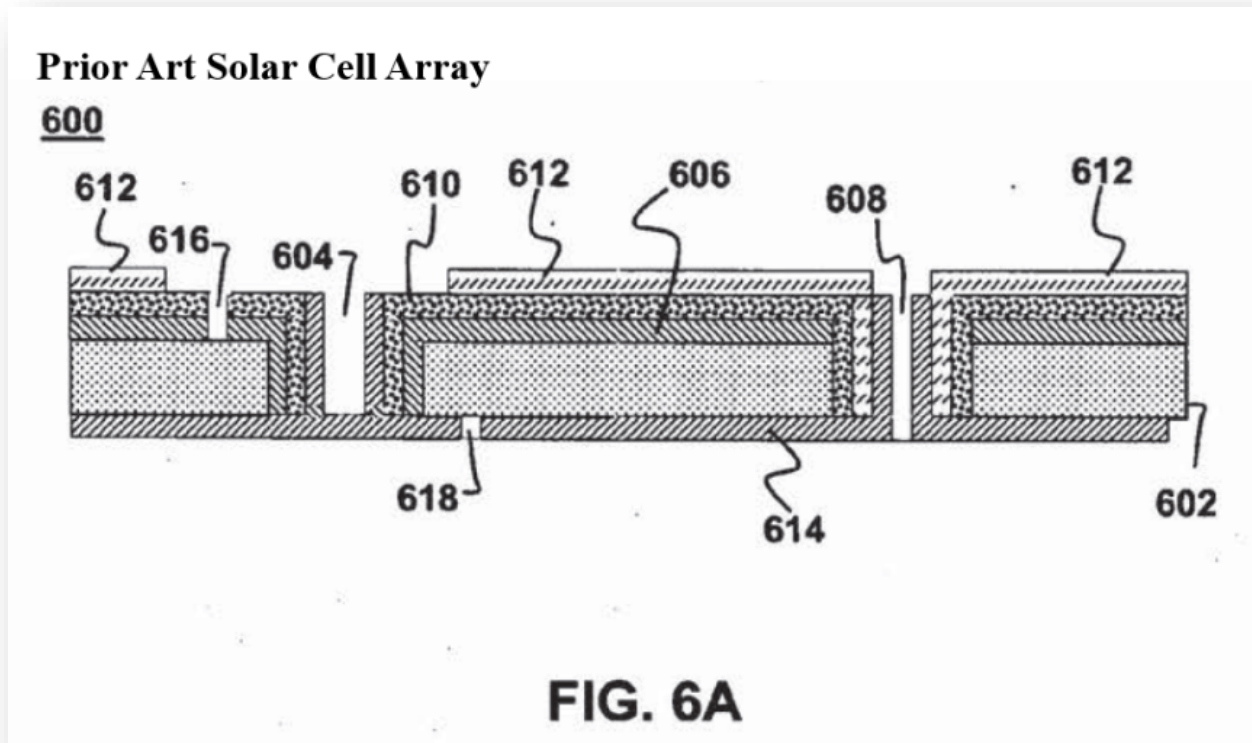
[0009] This has led solar cell researchers and manufacturers to develop different types of solar cells that can be fabricated less expensively and on a larger scale than conventional silicon-based solar cells. . .

. . .

[0013] Thus, there is a need in the art, for an optoelectronic device architecture that overcomes the above disadvantages and a corresponding method to manufacture such cells.

Ex. 1012, ¶¶7-13 (emphasis added).

219. In particular, Sheats focuses on the drawbacks of solar cell arrays (e.g., 600 below) manufactured from a single substrate (e.g., 602 below), where holes (e.g., 604, 608 below) are cut into the substrate to form multiple solar cells:



Ex. 1012, Fig. 6A (annotated); *see also id.* at Fig. 6B.

220. Specifically:

[0010] For example FIG. 6A illustrates a portion of a prior art solar cell array **600**. The array **600** is manufactured on a flexible insulating substrate **602**. Series interconnect holes **604** are formed through the substrate **602** and a bottom electrode layer **606** is deposited, e.g., by sputtering, on a front surface of the substrate and on sidewalls of the holes. Current collection holes **608** are then formed through the

bottom electrode and substrate at selected locations and one or more semiconductor layers **610** are then deposited over the bottom electrode **606** and the sidewalls of the series interconnect holes **604** and current collection holes **608**. . .

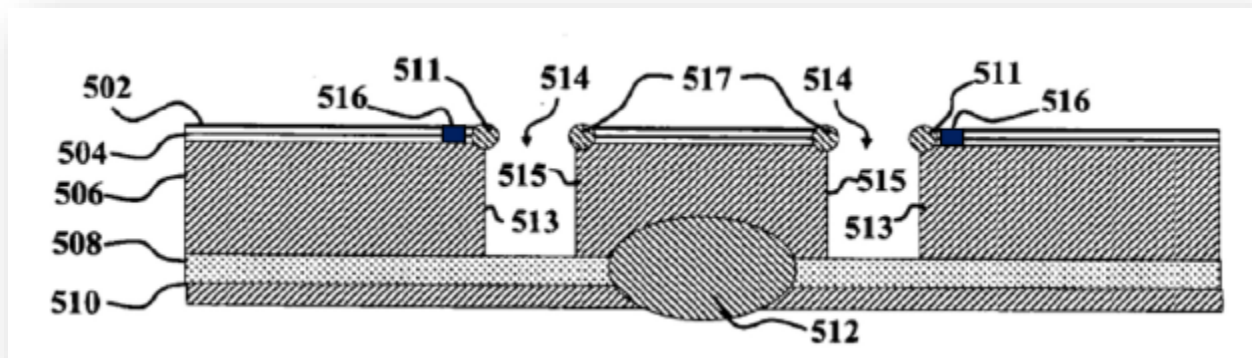
[0011] FIG. 6B depicts another prior art array **620** that is a variation on the array **600**. The array **620** is also manufactured on a flexible insulating substrate **622**. . .

[0012] There are two significant drawbacks to manufacturing solar cell arrays as shown in FIGS. 6A-6B. First, the metal layers are deposited by sputtering, which is a vacuum technique. Vacuum techniques are relatively, slow, difficult and expensive to implement in large scale roll-to-roll manufacturing environments. Secondly, the manufacturing process produces a monolithic array and sorting of individual cells for yield is not possible. This means that only a few bad cells can ruin the array and therefore increase cost. In addition, the manufacturing process is very sensitive to the morphology and size of the holes. Since the front to back electrical conduction is along the sidewall of the hole, making the holes larger does not increase conductivity enough. Thus, there is a narrow process window, which can add to the cost of manufacture and reduce yield of usable devices. Furthermore, although vacuum deposition is practical for amorphous silicon semiconductor layers, it is impractical for highly efficient solar cells based, e.g., on combinations of Copper, Indium, Gallium and Selenium or Sulfur, sometimes referred to as CIGS cells. To deposit a CIGS layer, three or four elements must be deposited in a precisely

controlled ratio. This is extremely difficult to achieve using vacuum deposition processes.

Ex. 1012, ¶¶10-12 (emphasis added).

221. One of the embodiments of Sheats' purported solutions, which Petitioner relied on, similarly includes a single structure (500) separated into multiple solar cells.



Paper 3, 61 (citing Ex. 1012, ¶¶3-4, 58-59) (illustrating Ex. 1012, Fig. 5D).

222. Petitioner's expert testified that Figure 5D illustrates multiple solar cells, and I agree:

Q Figure 5D shows three rectangular blocks listed on top of layers 508 and 510. Right?

A Yes.

Q And the isolation trench 516 is illustrated in two of those three rectangular blocks. Right?

A That is correct.

Q Is it accurate to say that those three rectangular blocks represent three solar cells?

A I am turning to Sheats. Just give me one moment.

(Exhibit 1012, previously marked.)

A Yes, it would be appropriate to call each of the blocks a solar cell, and more particularly the layer identified as 504 is the intended absorber layer of the solar cell, going back to our previous discussion.

Ex. 2029, 240:1-18.

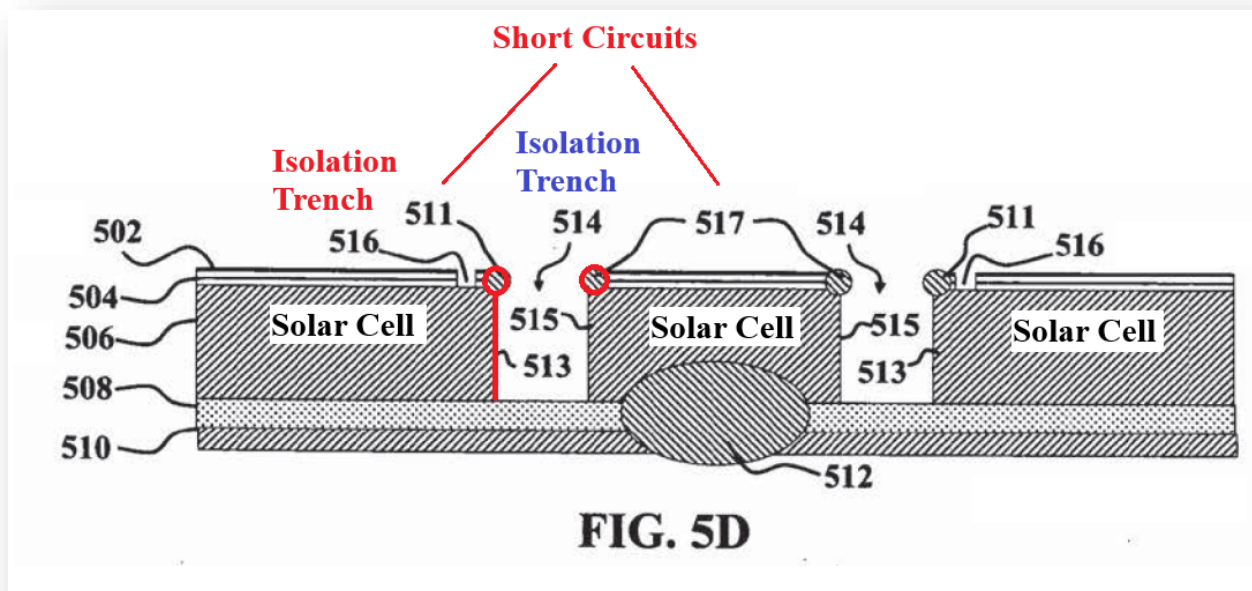
b. Sheats' Trench 516 Isolates Two Solar Devices

223. In the full context of Sheats, a POSITA would have known that the function of isolation trench 516 is to prevent short circuit between points 511 and 517 during the formation of trench 514:

The process of forming the isolation trench [514] may cause electrical short- circuits 511, 517 between the transparent conductive layer 502 and the bottom electrode 506. To electrically isolate undesirable short circuits 511 formed on an outside wall 513 of the trench 514 an isolation trench 516 is formed through the transparent conductive layer and the active layer to the bottom electrode 506 as shown in FIG. 5D. The isolation trench 516 surrounds the closed-loop trench 514 and electrically isolates the short circuits 511 on the outside wall 513 of the trench from the rest of the structure 500.

Ex. 1012, ¶¶59 (emphasis added).

224. In other words, the function of isolation trench 516 is to prevent short circuit between solar cells in an array, during the formation of the gap (514) that separates these two solar cells:



Ex. 1012, Fig. 5D (annotated).

225. Thus, in my opinion, a POSITA modifying Froitzheim with a trench to prevent short circuit within the single solar cell, Paper 3, 62 (“A POSITA would have been motivated to isolate the edge of Froitzheim’s modified solar cell to prevent short circuits”), would not have based their modification on Sheats disclosing a trench to prevent short circuit between two solar cells.

C. Ground III: Petitioner’s Challenge of Claims 1-4 and 6-12 Based on Froitzheim and Borden-575 Fails

1. Petitioner Failed to Show Why a POSITA Would Have Been Motivated to Combine Froitzheim and Borden-575

226. I note that Petitioner’s proposal to implement “Borden-575’s polysilicon emitter and tunnel oxide layer to the backside configuration taught by Froitzheim” is vague.

227. On the one hand, Petitioner appears to propose implementing Borden-575’s tunnel oxide. *See, e.g.*, Paper 3, 65-66 (multiple references to a “tunnel oxide layer”). On the other hand, Petitioner repeatedly refers to a tunnel oxide “layer” and labels its proposed combination with an “oxide layer,” *see, e.g., id.* at 65, 70, 71, 73, 76 (illustrating an “oxide layer”), while also referencing Borden-575’s buried oxide in section X.C.2.c of the Petition (discussing claim limitation 9[c]), *id.* at 69 (highlighting “buried oxide” three times).

228. I understand that Petitioner’s expert testified that Petitioner’s illustration of the proposed Froitzheim-Borden-575 includes a label for “oxide layer” that is intentionally vague to represent both the tunnel oxide layer and the buried oxide layer:

Q On Page 146, above Paragraph 224, you illustrate this Froitzheim-Borden 575 combination. Right?

A Above Paragraph 226.

Q Yes.

A Yes.

Q And the orange line labeled as oxide layer is referring to the tunnel oxide layer as taught by Borden 575. Right?

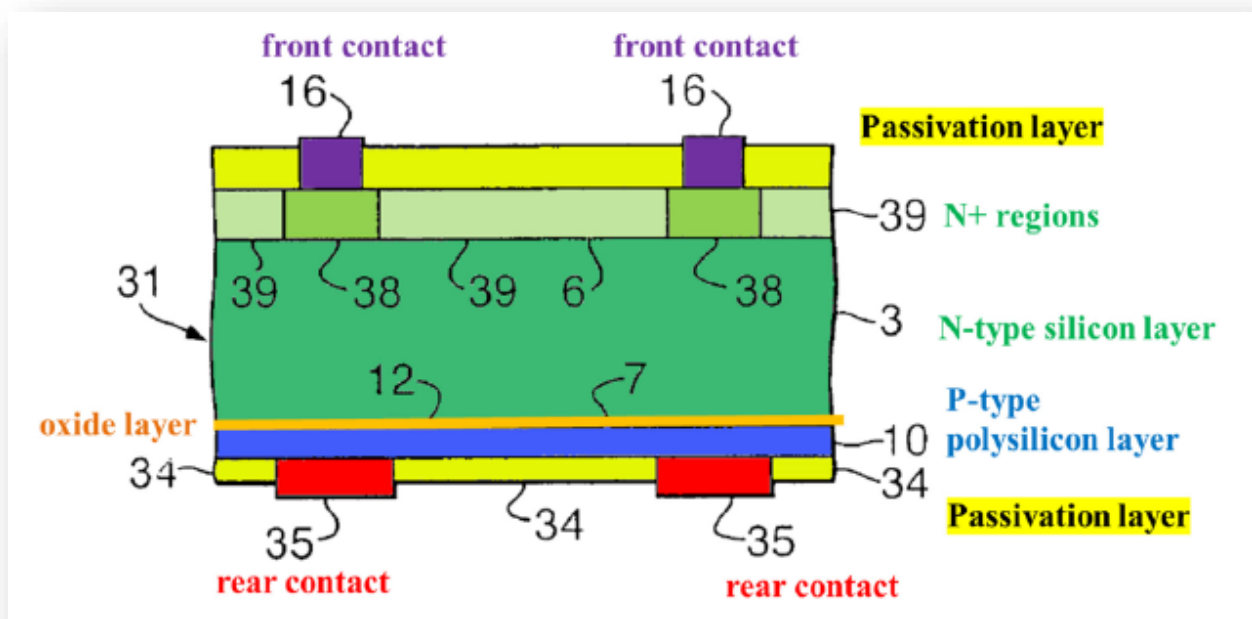
A Borden teaches two oxide layers, and this oxide layer shown in the figure is purposefully labeled oxide layer. As I say in the text, we require Borden 575's tunnel oxide layer in order to make a functioning solar cell. But Borden teaches that its tunnel oxide layer doesn't necessarily have to cover the entire wafer surface, and that its other oxide layer may also occupy some of the wafer surface. So this figure labeling the oxide layer as oxide layer recognizes that Borden's tunnel oxide layer is required, as described in the text, but doesn't limit Borden's teachings to his tunnel oxide layer.

Q So in the Froitzheim-Borden 575 combination are you incorporating Borden 575's other oxide layer as well?

A I -- I leave that possibility, as Borden teaches both. I am incorporating at least Borden's tunnel oxide layer.

Ex. 2029, 242:22-244:6

229. I understand the illustration discussed in the quote above is as follows:



Ex. 1003, ¶225.

230. In my opinion, regardless of whether the proposed Frotizheim-Borden-575 combination uses Borden-575's tunnel oxide, or buried oxide, or both, any of those combinations would be fatally flawed.

a. Borden-575's Tunnel Oxide Would Have Been Too Difficult to Implement

231. If Petitioner proposes implementing Borden-575's tunnel oxide, then a POSITA would not have been motivated to do so because it would have been too difficult and demonstrably unreliable for the same reasons discussed in § XII.A.1.a.

232. The futility in forming a reliable and reproducible tunnel oxide is documented in the Gan Thesis's disclosure of the struggle to control the oxide thickness to be between 15 to 20 Å:

It appears that the oxide breakup depends critically on the interfacial oxide thick-ness. The thin-oxide growth recipe used in this work was not reliable; the oxide thicknesses between 15 to 20 Å have been found with the same growth condition. As a result, this contributes to the fluctuation of the pc results. It is then clear that a more reliable way of growing the thin oxide is needed.

Ex. 2003, 119 (emphasis added).

233. Compounding this problem, Borden-575 requires its tunnel oxide to be even thinner:

In embodiments, the doped region 210 is formed using polysilicon, which may be deposited at a temperature on the order of 630°C and is in-situ doped. A short anneal at 1050°C for 30 seconds after deposition activates the dopants. As mentioned above, in some embodiments a thin tunnel oxide may be included between the substrate 200 and the polysilicon 210 in the contact holes 212. This oxide - typically 8 to 15Å thick - provides passivation between the substrate and the polysilicon, while allowing for tunnel current flow.

Ex. 1006, ¶22 (emphasis added).

234. This is perhaps why the tunnel oxide is optional in Borden-575:

Borden-575 does not answer Gan Thesis's question of how to reliably grow the thin oxide.

[0019] FIG. 2 shows an example cell structure in accordance with embodiments of the invention. . . In embodiments described in more detail below, contact holes 212 include a tunnel oxide. However, this is not necessary in all embodiments.

[0022] In embodiments, the doped region 210 is formed using polysilicon, which may be deposited at a temperature on the order of 630⁰C and is in-situ doped. A short anneal at 1050⁰C for 30 seconds after deposition activates the dopants. As mentioned above, in some embodiments a thin tunnel oxide may be included between the substrate 200 and the polysilicon 210 in the contact holes 212. This oxide - typically 8 to 15A thick - provides passivation between the substrate and the polysilicon, while allowing for tunnel current flow.

[0026] FIG. 4 shows an example embodiment of the process flow for fabricating a solar cell structure according to aspects of the invention. First in step S402, the wafer is cleaned and the buried oxide formed, using a process such as thermal oxidation or RadOx® from Applied Materials. Next in step S404, the contact holes are formed. For example, an etch mask layer is screen printed on the cell and the buried oxide is etched in HF. The resist is then removed. The wafer is then cleaned and, in one embodiment shown in FIG. 4, a tunnel oxide is grown in the contact holes using a process such as ISSG or Radox

in the step S406. Another embodiment does not use the tunnel oxide, and processing advances directly from step S404 to S408.

Ex. 1006, ¶¶19, 22, 26 (emphasis added).

235. In fact, Borden-575 states outright that the same problems with the oxide layer in the Gan Thesis are present in Borden's embodiment with the tunnel oxide layer:

Another method to passivate contacts is to place a thin tunnel oxide - typically 15Å thick – under the metal contacts. Such types of contacts are also well known, and have been used commercially by Schott solar to manufacture MIS solar cells. However, such solar cells have not been commercially introduced, possibly because of the difficulty of reliably forming a thin tunnel oxide.

Ex. 1006, ¶ 5 (emphasis added).

236. Therefore, in my opinion, a POSITA would not have been motivated to combine the tunnel oxide layer of Borden-575 with Froitzheim because the tunnel oxide layer is hard to reproduce with consistent and reliable thickness.

237. Further, Borden-575 uses the same high temperatures that the Gan thesis warns about:

In embodiments, the doped region 210 is formed using polysilicon, which may be deposited at a temperature on the order of 630° C and is in-situ doped. A short anneal at 1050° C for 30 seconds after deposition activates the dopants. As mentioned above, in some

embodiments a thin tunnel oxide may be included between the substrate 200 and the polysilicon 210 in the contact holes 212.

Ex. 1006, ¶ 22 (emphasis added).

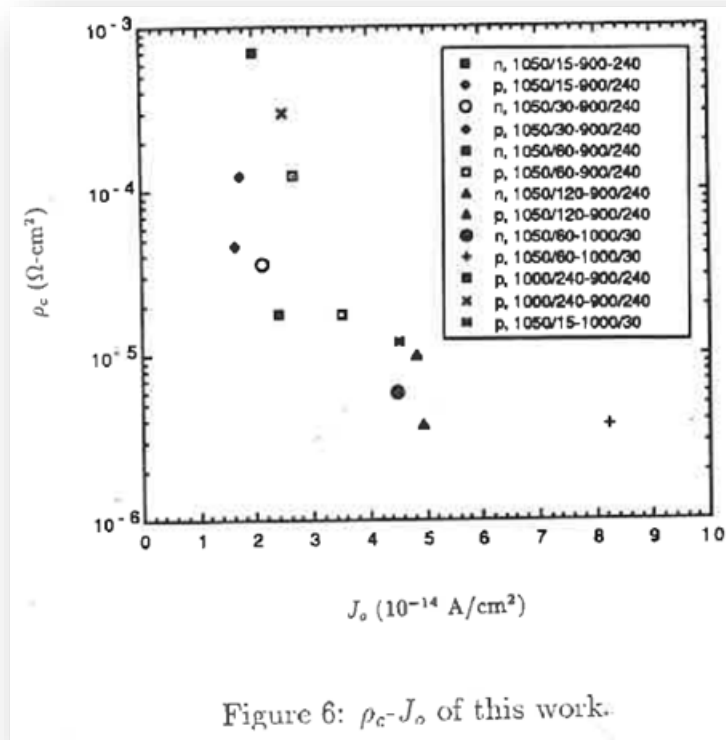
238. As I discussed in §XI.B, Gan teaches the higher the temperatures and time for the second step anneal, the worse the value of J_o :

Table 1: The effect of the second-step anneal on J_o and ρ_c .

	N-type		P-type	
	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$
900 °C-4 hour	2.4	18	3.5	18
1000 °C-30 min	4.5	~ 6	8.2	3.8
1000 °C-60 min	7.9		10.5	

Ex. 1005, Table 1.

239. As shown below, Gan showed that a second step anneal at only 1000° C were the worst temperatures tested:



Ex. 1005, Fig. 6.

240. Although Borden-575 discloses a shorter anneal time than Gan, Gan is clear that temperatures above 1000° C are prohibitive, and Borden-575 comes to the same conclusion as the Gan Thesis that using the tunnel oxide is not commercially viable. Ex. 1006, ¶ 5 (“[S]uch solar cells have not been commercially introduced, possibly because of the difficulty of reliably forming a thin tunnel oxide.”) (emphasis added).

241. Thus, in my opinion, a POSITA would not have been motivated to modify Froitzheim with the tunnel oxide layer or a combination of the tunnel oxide layer and buried oxide layer of Borden-575.

b. A POSITA Would Not Have Implemented Borden-575's Polysilicon Emitter Without Borden-575's Buried Oxide

242. In my opinion, a POSITA also would not have implemented Borden-575's polysilicon emitter in Froitzheim. There is no reasonable expectation of success from using Borden-575's polysilicon emitter without its complimentary buried oxide.

243. Borden-575 emphasizes the importance of isolating contacts in solar cells:

To obtain high efficiency in silicon solar cells, it is considered advantageous to eliminate surface recombination. Such recombination comes from both unpassivated surfaces and from metal contacts. A measure of recombination is the surface recombination velocity (SRV), which is the rate of minority carrier recombination at the surface. For a reference value, <100 cm/sec provides a well passivated surface needed for a high efficiency cells. By contrast, a metal contact will have an SRV of 10^7 cm/sec, five orders of magnitude higher. If the metal covers 3% of the surface, then the effective surface recombination velocity is 3×10^5 cm/sec, more than 3 orders of magnitude larger than desired. Therefore, contact passivation is essential.

Ex. 1006, ¶3 (emphasis added).

244. Borden-575 discusses prior art selective emitter structures that provide contact isolation, and its disadvantages:

One well known method to isolate the contacts from the bulk is to use a selective emitter, shown in FIG. 1. As shown in FIG. 1, the area away from the contacts 102 has a shallow emitter diffusion 106 (n-type, typically with Phosphorous doping, on a p-type substrate, for example). The shallow emitter 106 provides good blue response, as blue photons are absorbed near the surface. This emitter might be 0.3 to 0.5 μm thick. On the other hand, deep diffusions 108 - 2-3 μm thick - are placed under the contacts. These provide isolation so that the high recombination contact surfaces do not affect the cell performance. However, such structures are difficult to form as they require aligned patterning of the contact holes and the metal lines, as well as a several hour diffusion to obtain such a deep junction. Therefore, selective emitters are rarely used in commercial solar cells.

Ex. 1006, ¶4 (emphasis added).

245. Below is the prior art selective emitter structure featuring deep diffusion 108:

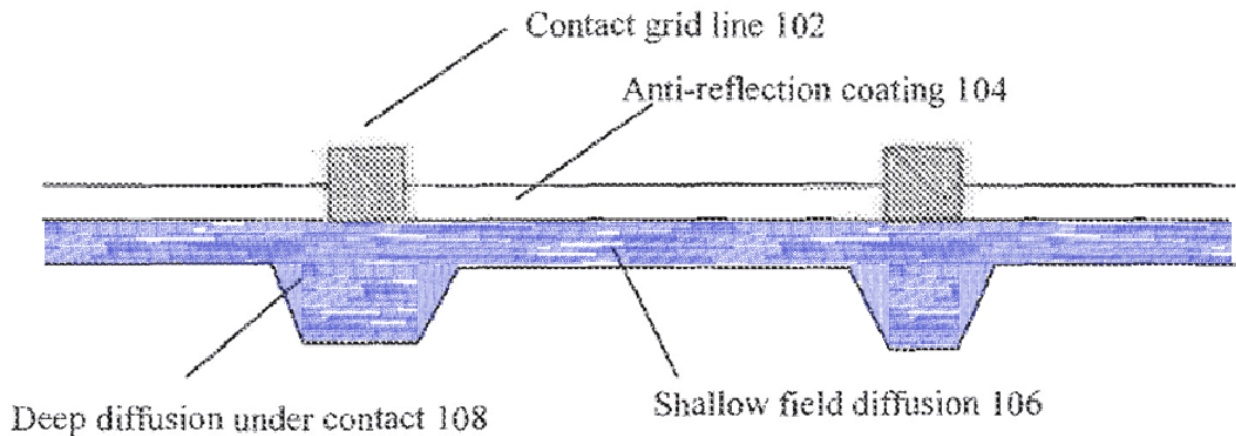


FIG. 1 (PRIOR ART)

Ex. 1006, Fig. 1 (annotated).

246. Borden-575's purported innovation is to place a "buried oxide under the emitter of a polysilicon emitter solar cell":

The present invention relates to methods and apparatuses for providing a buried insulator isolation for solar cell contacts.

According to certain aspects, the invention places a buried oxide under the emitter of a polysilicon emitter solar cell. The oxide provides an excellent passivation layer over most of the surface. Holes in the oxide provide contact areas, increasing the current density to enhance efficiency. The oxide isolates the contacts from the substrate, achieving the advantage of a selective emitter structure without requiring deep diffusions. The oxide further enables use of screen

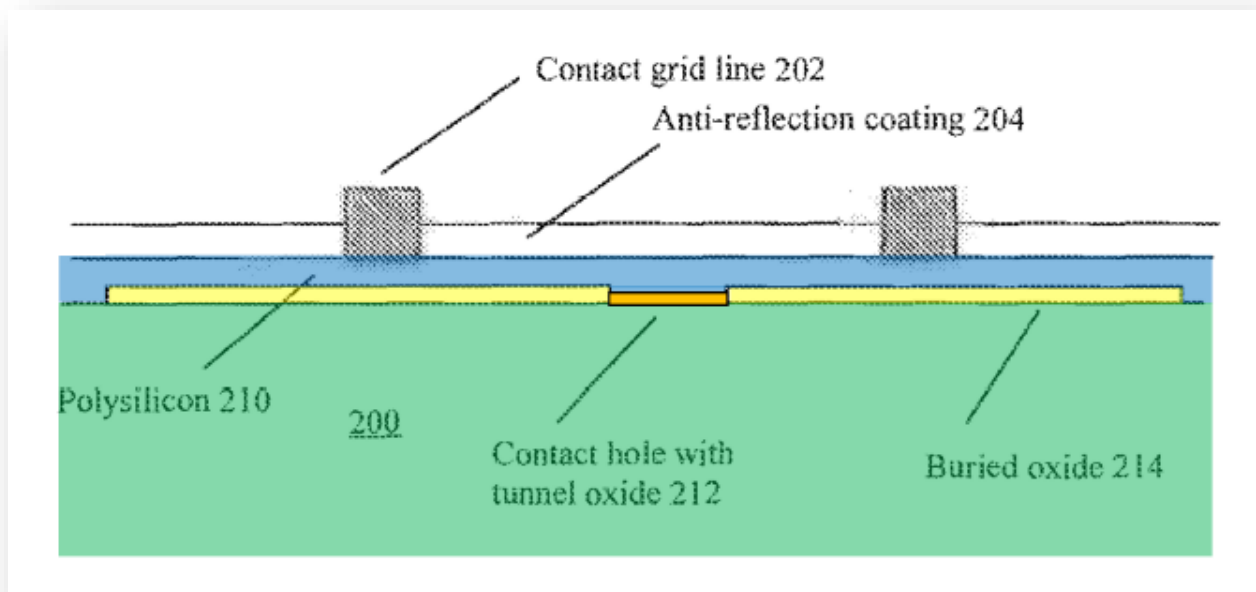
printing on advanced shallow emitter cells. Positioning of the grid lines close to the openings also enables use of a very thin emitter to maximize blue response.

Ex. 1006, Abstract (emphasis added).

247. According to Borden, the advantage of this structure is that it is “a selective emitter structure without requiring deep diffusions”:

The present invention relates to methods and apparatuses for providing a buried insulator isolation for solar cell contacts. According to certain aspects, the invention places a buried oxide under the emitter of a polysilicon emitter solar cell. The oxide provides an excellent passivation layer over most of the surface. Holes in the oxide provide contact areas, increasing the current density to enhance efficiency. The oxide isolates the contacts from the substrate, achieving the advantage of a selective emitter structure without requiring deep diffusions. The oxide further enables use of screen printing on advanced shallow emitter cells. Positioning of the grid lines close to the openings also enables use of a very thin emitter to maximize blue response.

Ex. 1006, Abstract (emphasis added); *see also id.* at ¶16.



Paper 3, 68 (citing Ex. 1006, Fig. 2) (annotation in original).

248. Borden-575 describes the structure above:

FIG. 2 shows an example cell structure in accordance with embodiments of the invention. As shown in FIG. 2, the cell structure includes an insulating (e.g. oxide) layer 214 under the doped region 210 and the contact 202. This insulating layer 214 isolates the contact 202 from the substrate 200. According to some aspects of the invention, if the insulating layer [buried oxide] 214 is made using a material that passivates silicon, such as thermal SiO₂, then the solar cell surface has very good passivation and a low surface recombination velocity, both in the field region 210 and under the contacts 202. Contact holes 212 are provided in the insulating layer 212 to allow for photocurrent flow. In embodiments described in more

detail below, contact holes 212 include a tunnel oxide. However, this is not necessary in all embodiments.

Ex. 1006, ¶3.

249. I note a few differences between Borden-575's buried oxide and the tunnel oxide layer of the '516 patent. First, Borden-575 uses a buried oxide between the poly-Si and the Si substrate over almost the entire wafer except where contact holes with tunnel oxide are used. In the '516 patent, tunnel oxide is covering almost the entire backside of the wafer except when cut through by the isolation trenches. The thick oxide of the '516 patent is on top of the poly-Si, not buried underneath it, and is used to limit the contact area between the metal and the poly-Si and provide improved light reflectance.

250. The buried oxide may then combat the high surface recombination velocity of a metal contact, thereby achieving the essential contact passivation that Borden-575 emphasizes. Ex. 1012, ¶3.

251. Thus, it is important that the buried oxide be placed on the substrate under each metal contact. As Borden-575 notes, "the contact metal 202 is blocked from reaching the substrate 200 by the buried oxide 214. This enables contacting to the thin emitter without use of a sophisticated contact process." Ex. 1006, ¶3. In other words, polysilicon emitter 210 functions properly in Borden-575 because of buried oxide 214.

252. The buried oxide is not to be confused with an optional “thin tunnel oxide,” which Borden-575 separately discloses. *Compare* Ex. 1006, Abstract and ¶¶7, 16 (disclosing “buried oxide”) *with id.* at ¶¶19, 22 (disclosing a “thin tunnel oxide.”); *see also* Paper 3, 69 (separately coloring the two components).

253. This distinction is important because, at least in its motivation to combine section, Petitioner’s proposed Froitzheim-Borden-575 combination does not include the crucial buried oxide. *See, e.g.,* Paper 3, 65-66 (multiple references to a “tunnel oxide layer”). On the other hand, Froitzheim’s own oxide layer is no suitable substitute because it is removed after doping. Ex. 1004, ¶¶44-45.

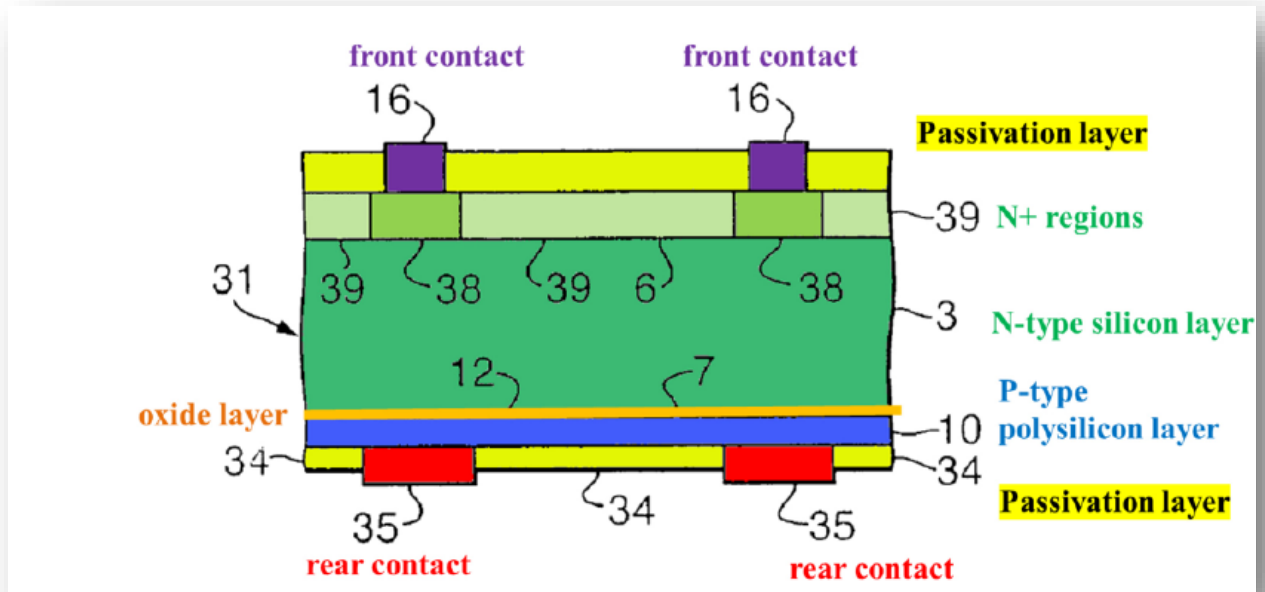
254. Without the buried oxide, Borden-575’s thin emitter would need “a sophisticated contact process,” such as the deep diffusion of Borden-575’s prior art, to reach the metal contact. Ex. 1006, ¶3. Froitzheim discloses no sophisticated contact process, and the Petition does not propose a solution to bridge this gap.

255. Thus, in my opinion, a POSITA would not have reasonably expected to succeed in implementing Borden-575’s barebone emitter to Froitzheim.

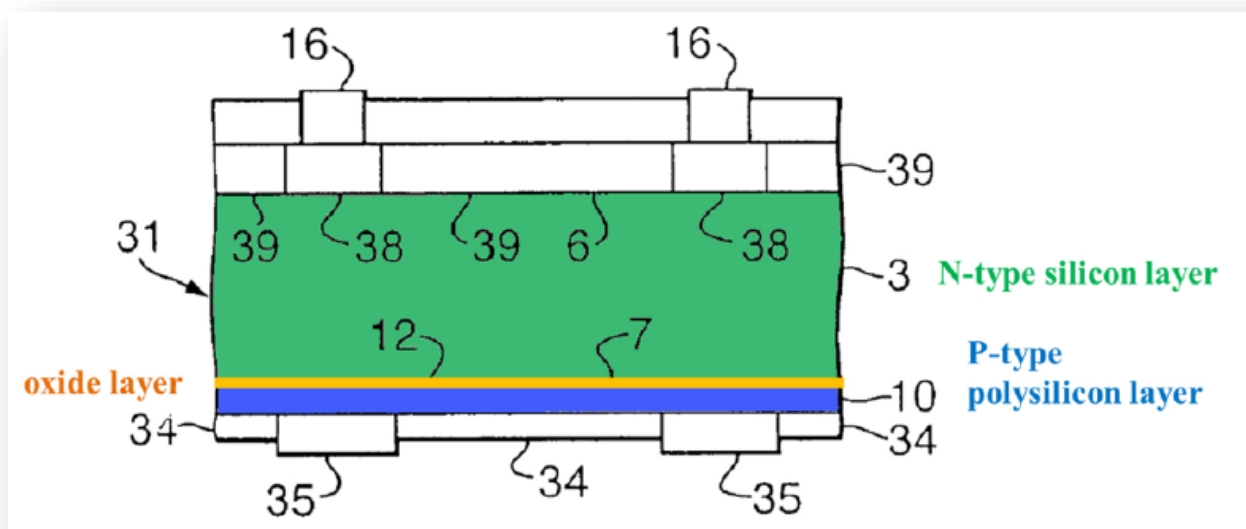
c. Borden-575’s Buried Oxide Requires Contact Holes

256. To the extent Petitioner proposes implementing Borden-575’s buried oxide instead of Borden-575’s tunnel oxide, there would still be no reasonable expectation of success because Petitioner omitted the contact holes taught by Borden-575 in its proposed combination of Froitzheim-Borden-575. Without the

contact holes taught by Borden-575 in Petitioner's proposed Froitzheim-Borden-575 combination, current could not flow between the emitter and the substrate.



Paper 3, 65 (illustrating the Froitzheim-Borden-575 combination with an “oxide layer” but no contact holes).



Paper 3, 70 (illustrating the Froitzheim-Borden-575 combination with an “oxide layer” but no contact holes).).

257. I understand that Petitioner’s expert also testified that the proposed Froitzheim-Borden-575 combination did not include Borden-575’s contact holes:

Q Let's go to Exhibit 1006, Borden 575. And I would like to direct you to Paragraph 22.

A Okay.

Q Paragraph 22 specifies a thin tunnel oxide would be included between the substrate 200 and the polysilicon 210 in the contact holes 212. Right?

A Correct.

Q Are contact holes incorporated in the Froitzheim-Borden 575 combination?

A Contact holes are not included in my combination because contact holes are not recited in the claims. It's not one of the limitations of the claims, at least at the back side of the solar cell.

Borden teaches this tunnel oxide layer. Borden teaches another oxide layer that can have contact holes in it, with a tunnel oxide in those contact holes. Contact holes are not part of the recited claims.

Ex. 2029, 245:18-246:15.

258. This omission is fatal.

259. Borden-575 defined the term “contact hole” broadly to include many types of openings:

In embodiments, substrate 200 is comprised of silicon, and is low-doped with p- or n-type impurities. Many other substrate materials can be used and this and many other methods for obtaining a desired polarity concentration and type are possible, as will be appreciated by those skilled in the art. It should be noted that the term contact hole should be construed broadly so as to relate to many types of openings through insulating layer 214 and many types of solar cell contacts. For example, the holes can provide for point contacts or they can provide for grid line contacts. Those skilled in the art of solar cell contacts will appreciate how the teachings of the invention can be applied to these and other various types of contacts and openings.

Ex. 1006, ¶20 (emphasis added).

260. But Borden-575 does not contemplate the possibility of there being no opening at all. This is because contact holes are a crucial feature; they “allow current flow” between the emitter and the substrate:

[0008] In furtherance of these and other aspects, a solar cell according to embodiments of the invention includes an emitter layer formed on a semiconductor substrate; and an insulating layer between the emitter layer and a surface of the substrate, the insulating layer being patterned to include contact holes that allow current flow therethrough.

[0009] In additional furtherance of these and other aspects, a method of fabricating a solar cell according to embodiments of the invention includes forming an insulating layer on a surface of a semiconductor substrate; patterning contact holes in the insulating layer that allow current flow therethrough; and forming an emitter layer on the insulating layer.

...

[0019] . . . Contact holes 212 are provided in the insulating layer 212[sic] to allow for photocurrent flow. . .

[0021] In embodiments such as shown in FIG. 2, the contacts 202 are positioned approximately in the middle between two holes 212. Photocurrent flows through contact holes 212 patterned in the oxide layer 214. This concentrates the current flow, providing an increased current density at the junction. The collected current then flows laterally to the contacts 202. Typical dimensions of the openings 212 can be 20 to 200 μm and spacing between openings 212 can be 1-5

mm. The ratio of the spacing to opening width provides the concentration, which is limited by series resistance due to current crowding at the contact holes. Concentration ratios on the order of 5 to 20 are typical. The openings can be lines parallel to the contact grid lines, or holes of shape such as rectangles or circles. Larger openings can be patterned without lithography, using screen printing. Laser ablation can also be used.

Ex. 1006, ¶¶8-9, 19-21 (emphasis added).

261. I note that the label “insulating layer 212” in the quote of Borden-575’s paragraph 19 above appears to be an error. The “insulating layer” is labelled as “214” throughout Borden-575, Ex. 1006, ¶¶18-21, and appears to be used interchangeably with the term “buried oxide,” *id.* at Figs. 2, 3, ¶24

262. Further, the buried oxide is an “insulating (*e.g.*, oxide) layer 214 under the doped region 210 and the contact 202. This insulating layer 214 isolates the contact 202 from the substrate 200.” Ex. 1006, ¶19. Thus, contact holes are needed to permit current flow from the substrate to reach the metal contacts.

263. A POSITA would have known that, without that current flow, the metal contacts would not be able to withdraw photocurrent from the p/n junction.

As Froitzheim explains in its background section:

Conventional silicon (Si) based solar cells comprise a base layer of crystalline Si doped with boron. At the side facing the sun during normal operation (the front side), an n-doped layer is provided e.g. by

diffusion of phosphorous into the base layer. This so-called emitter layer forms a p/n-junction with the p-doped base layer. Front and rear side contacts are arranged that are in electrical connection with the n-doped layer and the p-doped base layer, respectively, to withdraw a photocurrent from both sides of the p/n-junction.

Ex. 1004, ¶2 (emphasis added).

264. For the same reason, in Borden-575's structure, if the buried oxide has no contact holes, then the metal contacts are rendered inoperable, and no power could be drawn out of the solar cell.

265. Thus, to the extent Petitioner proposes implementing Borden-575's buried oxide, Petitioner's failure to identify contact holes in the proposed Froitzheim-Borden-575 combination would reduce a POSITA's expectation of success to zero.

2. *The Proposed Froitzheim-Borden-575 Combination Would Not Have Met the Limitation of Claim 12 of the '516 Patent*

266. I understand that, with respect to claim 12, the Petition states: "Petitioner incorporates Section X.C.2 [Petitioner's argument from the Froitzheim-Gan combination, in which Froitzheim alone satisfies the limitation of claim 12]. The combination of Froitzheim-Borden-575 teaches this element for the reasons in Section X.A.5 [arguing that Froitzheim alone satisfies the limitation of claim 12]." Paper 3, 74. Thus, I understand that Petitioner did not argue that aspects of Borden-575 would satisfy the limitation of claim 12.

267. As discussed in § XII.A.3, Froitzheim, and thus the proposed Froitzheim-Gan combination, fail to satisfy the limitation of having backside contacts with “silver formed over a layer of silicon dioxide” as recited in claim 12 of the ’516 patent. Replacing Gan with Borden-575 does not mitigate the shortcoming of Petitioner’s argument that Froitzheim alone satisfies the limitation of claim 12. Froitzheim alone does not satisfy the limitation of claim 12.

D. Ground V: Petitioner’s Challenge of Claims 1-2 and 8-11 Based on Li and Gan Fails

268. In my opinion, a POSITA would not have been motivated to modify Li using Gan’s polysilicon emitter and oxide layer, Paper 3, 79, because Li and Gan’s teachings are in conflict.

269. Li’s purported invention is a solar cell with a heterogeneous PN junction:

A layer of silicon thin film is deposited on a back surface of N-type monocrystalline silicon to form an emitting region (a P-type silicon thin film can be deposited on a layer of intrinsic silicon thin film which is first deposited on the back surface of the N-type monocrystalline silicon, or a P-type silicon thin film can be directly deposited on the N-type monocrystalline silicon).

Ex. 1008, 4; *see also id.* at Abstract.

270. Li teaches that its heterogeneous PN junction “is prepared by a low-temperature deposition method, which avoids a conventional diffusion process at 800-1000°C.” Ex. 1008, 4.

271. Li describes the purported benefits of its purported invention:

A technical means adopted in the present invention is to achieve an emitting region by depositing the silicon thin film on the back surface of the cell. Compared with a P-type silicon wafer diffused N-type emitting region used in most factories at present, the N-type silicon can effectively reduce the generation of boron-oxygen defects under illumination and resulting attenuation of conversion efficiency. In addition, a PN junction is prepared by a low-temperature deposition method, which avoids a conventional diffusion process at 800-1000°C. Such high-temperature process will cause more defects or contamination in a silicon material, which will affect the improvement of cell efficiency. In addition, the silicon thin film deposited on the back surface of the silicon wafer, whether it is amorphous silicon, microcrystalline silicon, or nanocrystalline silicon, can achieve a passivation effect on the back surface, thereby improving the cell efficiency. At least one surface of the front surface or the back surface of the structure can be subjected to texturing treatment to reduce light reflection and improve a light trapping effect, which is conducive to improving the photoelectric conversion efficiency of the cell. An anti-reflection film can be prepared on the texturing surface to further improve the photoelectric conversion efficiency of the cell.

Ex. 1008, 4 (emphasis added).

272. One such advantage, underlined above, is that Li's heterogeneous PN junction solar cell "is prepared by a low-temperature deposition method, which avoids a conventional diffusion process at 800-1000°C." Ex. 1008, 4.

273. Li's own structure uses low-temperature diffusion, which results in fewer defects and contamination in silicon materials, improved efficiency, and reduced manufacturing cost. Ex. 1008, 3 ("[Homogeneous PN junction solar] cells have the disadvantages that the high-temperature diffusion may cause more defects in silicon materials, and when pollution is caused by a high-temperature process, cell efficiency will be greatly reduced."); *id.* ("[A] deposition [of amorphous silicon] temperature is low (200°C)", and a process is relatively simple, such that a high-temperature process is avoided, and the manufacturing cost of the cell is reduced."); *id.* at 4 ("[Conventional diffusion process at 800-1000°C] will cause more defects or contamination in a silicon material, which will affect the improvement of cell efficiency.").

274. In the context of Li's disclosure, a POSITA would not have been motivated to implement Gan's polysilicon emitter and oxide layer. Construction of Gan's polysilicon emitter and oxide layer would repeatedly require the kind of high temperature that Li seeks to avoid.

275. Specifically, in Gan's 12-step process to construct its experimental device, step 3 is "[t]hin thermal oxide growth at 800 °C," step 4 is "[p]olysilicon

deposition (6000 Å) and first-step anneal at 1050 °C,” and step 10 is “[dopant d]rive-in; 900-1000 °C.” Ex. 1005, 246.

276. I understand Petitioner’s expert testified that the proposed Li-Gan combination uses Gan’s polysilicon emitter and oxide layer:

Q Can we go to Page 171 of your ’516 declaration.

A Page 171. Okay.

Q Here you illustrate a combination of Li and Gan. Right?

A That is correct.

Q You have in this illustration an oxide layer in orange. Right?

A Correct.

Q This is referring to Gan's oxide layer. Right?

A Yes. As I say in Paragraph 272, the implementation of Gan's tunnel oxide layer and polysilicon emitter to Li is shown in the figure below.
In the below figure.

Q And in this figure you also show a polysilicon emitter in dark blue.
Right?

A Correct.

Q And this is referring to Gan’s polysilicon emitter. Right?

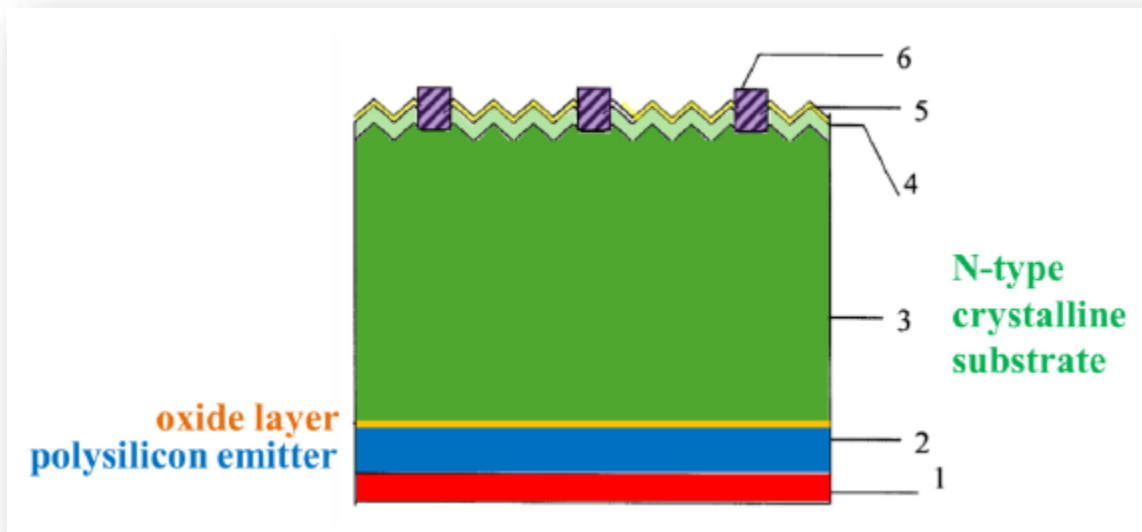
A I can read the same sentence again. The implementation of Gan’s tunnel oxide layer and polysilicon emitter to Li is shown in the below.

Q Well, is that a yes to my question?

A This is an oxide layer and polysilicon emitter as taught by Gan implemented in Li, yes.

Ex. 2029, 238:4-239:7.

277. I understand the illustration discussed in the quote above is as follows:



Ex. 1003, ¶272.

278. I understand Petitioner's expert testified that Gan's step 3 discloses the formation of an oxide layer:

Q Now, which of the 12 steps in Gan disclose the formation of that oxide layer?

A Gan describes in Step 3 how to form an oxide layer, thin thermal oxide growth at 800 degrees C, parentheses, ten minute oxygen flow.

Ex. 2029, 236:16-20.

279. I understand Petitioner's expert testified that Gan's steps 4, 9, and 10 disclose the formation of a polysilicon emitter:

Q Now, which steps in Gan's 12 steps disclose the formation of a polysilicon layer?

A Gan describes the deposition of a polysilicon layer in Step 4 of his sequence, and the subsequent doping of that to form an emitter in Steps 9 and 10.

Ex. 2029, 237:13-18.

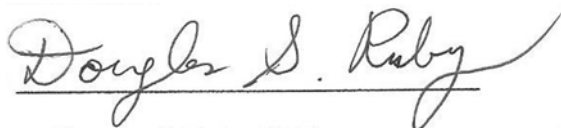
280. Thus, in my opinion, Li and Gan's teachings are in conflict, and a POSITA would not have combined the two references.

XIII. CONCLUSION

281. In my opinion, based on my review of the '516 patent, the materials referenced above, and my knowledge of what a POSITA would have known at the time of the invention, the Petition fails to show that any claim is unpatentable.

282. I declare that all statements made herein of my own knowledge are true, and that statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on May 22, 2025 in Albuquerque, New Mexico.

A handwritten signature in cursive script that reads "Douglas S. Ruby". The signature is written in dark ink and is positioned above a horizontal line.

Douglas Ruby, Ph.D.