

MIS Solar Cells: A Review

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Abstract—The metal-thin-film insulator-semiconductor (MIS) structure is currently receiving much attention in solar-cell studies. Both theoretical and practical investigations indicate that this structure offers a means of overcoming the principal deficiency of Schottky barrier solar cells, namely low open-circuit photovoltage, while maintaining the attractive features that have led the metal-semiconductor junction to be considered as a possible alternative to the p-n junction for large-area, terrestrial, solar-cell applications.

The thin insulating layer allows control over not only the magnitude of the dark current flowing through the diode, but also the dominant type (majority or minority carrier) of this current. Desirably low values of dark current have been postulated for majority carrier devices incorporating suitable charge-trapping centres, located either within the insulator or at the semiconductor-insulator interface, and for minority carrier devices employing suitable insulator thicknesses, metal work functions, and semiconductor resistivities.

Theories based on these models are reviewed in this paper and their relevance to explaining photovoltage enhancement in practical Si and GaAs MIS cells is examined. The factors affecting other salient solar-cell properties (photocurrent, fill factor, conversion efficiency) are also considered and suggestions as to the parameters limiting present device performance are given.

I. INTRODUCTION

SOLAR CELLS utilizing homojunctions in Si and heterojunctions with GaAs and CdS have already demonstrated the effectiveness of photovoltaics in generating electricity on Earth. However, if photovoltaics is to emerge as a method capable of being accommodated in the generation mix used by utilities to provide large-scale electric power, then a cost reduction of around 50 times must be achieved in the solar cells (or solar cells plus concentrators in concentrated sunlight systems) [1]. One possibility for cost reduction lies in the method of junction fabrication and the idea of a simple deposited metal-semiconductor junction is, at first sight, very attractive. Metal deposition methods are consistent with high yield, fast throughput processing, and also involve low substrate temperatures, thus avoiding degradation of semiconductor minority carrier properties and suggesting a compatibility with thin film and nonsingle crystalline substrates. In practice, however, intimate contact metal-semiconductor solar cells exhibit a serious deficiency in the form of very poor photovoltage response. This stems from the fact that the usual thermionic emission dark current in Schottky barrier junctions leads to a considerably higher dark current than in many homojunction and heterojunction structures. It is possible to overcome this disadvantage, yet still preserve the attractive features of Schottky barrier technology, by allowing a very thin insulating layer to separate the metal and

semiconductor. The deliberate introduction of such a layer yields a metal-insulator-semiconductor (MIS) solar cell.

In the MIS structure the thermionic emission dark current can be reduced by either increasing the effective metal-semiconductor barrier height, decreasing the probability of majority carrier tunneling, encouraging interface states with a large capture cross section for majority carriers, or reducing the number of majority carriers at the semiconductor surface [2].

From a theoretical standpoint, the four effects above are readily understood, but how they might be capitalized upon in a practical sense is not so straightforward. There is a substantial amount of experimental data on MIS solar cells but the relationships that these data bear to theories based on the above four effects are not always evident. This review represents an attempt to examine existing practical data in the light of the various MIS solar-cell theories and, in so doing, arrive at a fuller understanding of MIS cells and a knowledge of the factors presently limiting device performance.

The present theories are reviewed in the next section and, after a section on the preparation and properties of thin insulating layers, the relevance of the theories to explaining photovoltage enhancement in single-crystal Si and GaAs cells is examined. Succeeding sections treat the other salient MIS solar-cell properties of photocurrent response, fill factor, conversion efficiency, and applicability to nonsingle crystalline substrates.

II. GENERAL THEORY

The conversion efficiency of a solar cell can be expressed as

$$\eta = \frac{I_{sc} \cdot V_{oc} \cdot FF}{P_{in} \cdot a} \quad (1)$$

where I_{sc} is the short-circuit current, V_{oc} is the open-circuit voltage, FF is the fill factor, P_{in} is the input solar power density, and a is the total front surface area of the cell.

In MIS solar cells the insulator energy bandgap is considered to be too high to lead to any sunlight absorption and, providing the insulator is kept thin enough (≤ 20 Å in silicon MIS cells [3]–[5]), tunneling through the insulator does not cause a photocurrent bottleneck. Thus in the absence of photocarrier recombination via surface states introduced at the semiconductor-insulator interface [6], the factors that govern the attainable value of I_{sc} can be the same in MIS cells as for intimate contact metal-semiconductor solar cells, i.e., photon absorption and reflection by the metal barrier layer, minority carrier transport in the front surface field regions and in the neutral base region of the semiconductor [7], [8]. The reflection problem can be overcome by judicious choice of anti-reflection (AR) coatings, with reflection losses being theoretically as low as 6 percent for Si and GaAs cells employing

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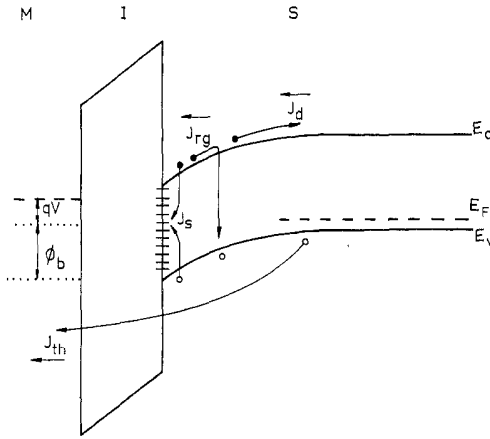


Fig. 1. Dark-current components in forward biased MIS (p-type) diode.

covering layers of refractive index greater than 2.1 [9], [10]. Thus short-circuit currents in MIS cells should closely match that of p-n junction cells, for which maximum AM1 values are [11] $\sim 41 \text{ mA} \cdot \text{cm}^{-2}$ for Si and $\sim 30 \text{ mA} \cdot \text{cm}^{-2}$ for GaAs. Any increased reflection losses in the surface junction cells could be offset by an improved blue response [12]–[14].

With regard to fill factor, the important parameters in any solar cell are saturation dark-current density J_0 , series resistance R_s , and shunt resistance R_{sh} [11], [15]. The only leakage path unique to MIS solar cells that might lead to low R_{sh} values is that caused by edge conduction via high-conductivity channels induced by charge within the insulating layer around the sides of the cell. However, simple heating or chemical treatments can remove this possibility [16], [17]. The presence of a thin insulating layer will only affect R_s at insulator thicknesses sufficient to cause photocurrent suppression [4], [18], [19]. This leaves, then, J_0 as the factor most likely to cause FF values in MIS cells to be different from those in other types of cell.

J_0 is also the major factor influencing the value of open-circuit voltage, as can be appreciated from the following expression:

$$J_p + \Sigma_D J_0 = \Sigma_D J_0 \exp(qV_{oc}/\gamma kT) \quad (2)$$

where J_p is the photocurrent density, γ is the factor that modifies the junction voltage to an extent that depends on the particular dark-current transport mechanism, and the summations are carried out for the dark-current components relevant to the particular solar cell. Equation (2) expresses the fact that on open circuit there is no net current flow in the solar cell and assumes that superposition of the dark and light currents is valid. Fig. 1 illustrates the possible dark-current mechanisms in an MIS (p-type semiconductor) diode, and the total dark current is given by

$$J_D = J_{th} + J_{rg} + J_d + J_s \quad (3)$$

where J_{th} arises from the thermionic emission of holes into the metal, J_{rg} is the depletion layer recombination-generation current density, J_d is the injection-diffusion current density, and J_s represents the surface state current density due to

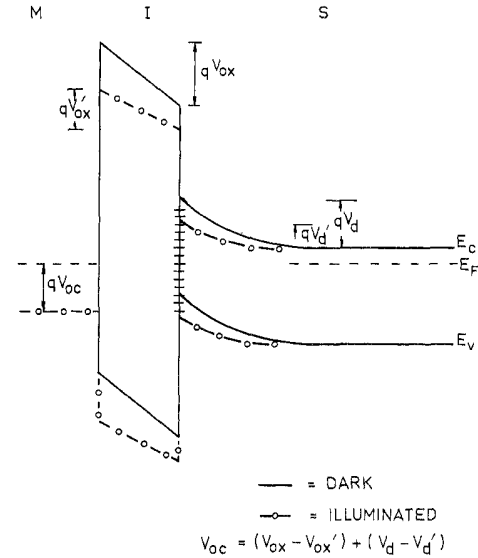


Fig. 2. V_{oc} enhancement due to filling of acceptor-type surface states on optical biasing of MIS (n-type) diode.

charge exchange between the metal and semiconductor band edges via surface states. With the possible exception of J_s , which is not amenable to a general treatment, the current component of potentially greatest magnitude is J_{th} .

$$J_{th} = \Theta A^{**} T^2 \exp(-q\phi_b/kT) [\exp(qV_j/nkT)] \quad (4)$$

where A^{**} is Richardson's constant, ϕ_b is the zero bias barrier height, n the ideality factor, and Θ the majority carrier tunneling coefficient [20]. In traditional Si and GaAs Schottky barrier diodes ϕ_b is pinned by the surface states at the interface between the spontaneously occurring native oxide and the semiconductor, such that the resulting values of J_{th} are too high for solar cell purposes [8]. However, intentional growth of an insulating layer affords an opportunity for increasing ϕ_b [2]; e.g., an oxide that passivates the semiconductor surface states would allow ϕ_b to be dictated by the metal work function [21]; an oxide that contained positive charge [22] or encouraged donor-type surface states [5] would be beneficial when the substrate was p-type (negative oxide charge or acceptor-type surface states [23] would be advantageous in the n-type case). Particular types of surface state would also allow reduction of J_{th} via the n -factor [23]. For example, in the n-type case shown in Fig. 2, acceptor-like surface states that became filled on optical biasing would decrease the voltage drop across the oxide and provide an electrostatic addition to the terminal voltage that would otherwise be related solely to the induced change in semiconductor band bending. The practical difficulty with this approach is that, although J_{th} may be reduced, dark-current flow via surface states (J_s in Fig. 1) will become more likely. Reduction of J_{th} via Θ is also possible and could be accomplished by increasing the oxide thickness [18], [20]. Such a measure would not generally lead to an effective solar cell as the minority carrier tunneling probability factor would be reduced also. An exception would arise if a current path not involving direct tunneling could be created for minority

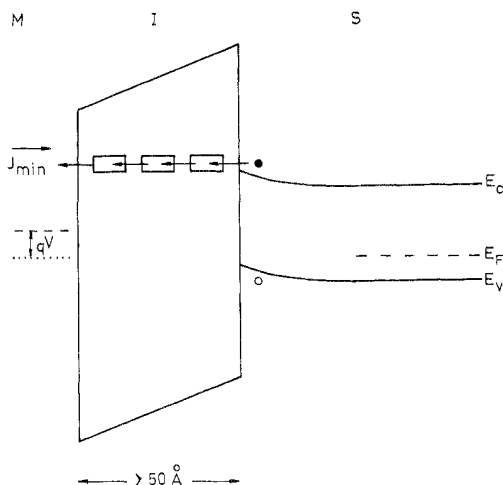


Fig. 3. Trap-assisted minority carrier current flow in illuminated MIS (p-type) diode. Note that it is not necessary to postulate the existence of a depletion layer in this mode of operation.

carrier transport alone. One possibility is shown in Fig. 3 and allows for minority carrier conduction via trap-assisted tunneling through suitably located charge centers within the oxide [24], [25].

The diode structure shown in Fig. 3 would produce a minority carrier solar cell with the dark current approaching the ideal value ($J_s = 0, J_{rg} \rightarrow 0, J_{th} \rightarrow 0$) of

$$J_{D, \min} = J_d \quad (5)$$

and characteristics equivalent to that of p-n junction diodes would result. To obtain p-n-like behavior from a simple surface junction structure is an exciting prospect for solar-cell development. Such devices can also materialize from structures with very thin ($< 20\text{-}\text{\AA}$) oxides and in which the majority carrier current is suppressed by the expedient of ensuring that essentially no majority carriers are available at the semiconductor-insulator interface to communicate with the metal; i.e., by creating an inversion layer at the semiconductor interface [16], [18], [21], [26]. In such a device employing a p-type substrate, a low work function metal is required, and the conduction band edge is bent down so as to be, at its extremity, nearly opposite the metal Fermi level. Large electronic tunnel currents can thus flow in both directions across the oxide and the net current is determined by current transport within the semiconductor, i.e., $J_D = J_d + J_{rg}$, with the latter term arising because of the presence of a depletion layer in the semiconductor.

In MIS solar cells there is evidence that, when substituting values of J_{th} and J_{rg} into (2), the correct values of ϕ_b , n , and J_{rg} to use are not the values as determined from dark I - V measurements [27], [28]. Optical biasing, as opposed to voltage biasing, can lead to different conditions at the semiconductor-insulator interface as regards both charge and minority carrier concentration, resulting in effective values of J_{th} and J_{rg} which can be higher than those measured in the dark. This does not invalidate (2) but merely serves to reemphasize the necessity of reducing factors that contribute to J_{th} and J_{rg} (and J_s) in order to obtain high values of V_{oc} .

III. THE INSULATING LAYER

In general, the insulator growth method used in MIS solar-cell fabrication must provide in a reproducible fashion a very thin (10–40 Å), stable, insulating layer with low defect density and low density of surface states at the interface with the semiconductor. Some of the first MIS solar cells used the spontaneously occurring native oxide of the semiconductor for this purpose [29], [30] but, while this demonstrated the advantages of MIS cells over previous MS cells, the device yield was low. Greater control over the oxide thickness and other properties has subsequently been achieved by a variety of deliberate oxidation processes, see Table I.

In all the gaseous oxidation methods, particularly those involving short growth times, the oxidation process is likely to be incomplete. Thus in the case of Si for example, a Si-rich region near the semiconductor-insulator interface will be present. Spontaneously occurring native oxides apparently have the stoichiometry $\text{SiO}_{0.4}$, and the SiO_2 structure is not attained until thicknesses of around 50 Å [31]. This emphasizes the fact that many insulating layers incorporated in Si MIS cells are not homogeneous. This could lead to continued oxygen incorporation into the oxide during subsequent device processing or operation, with the case of oxygen migration through thin gold barrier metal films being a particular example [43]. This phenomenon may be responsible for the ageing effect recorded in some Au-n-Si MIS devices, in which initially poor photoresponse, as would result from an accumulation layer induced by the Si-rich region in the oxide, gradually improves (over several hours) on exposure of the device to air [31]. Although the valence electrons weakly bonded to excess Si atoms correspond to donor-like states, conversion to acceptor-like states is possible by incorporation of $(\text{OH})^-$ radicals into the oxide [24]. For MIS cells on n-type Si, acceptor states are generally to be preferred over donor states on account of the increase in semiconductor band bending brought about by the former [5], [23]. The converse is true for devices on p-type Si and it would, therefore, appear advantageous to exclude water vapor during insulator formation by thermal oxidation of p-Si. There is some experimental data available to support this hypothesis [44], and a related fact is that oxidation in pure oxygen, or using a heat treatment in H_2 after oxidation in air (which can convert a "wet" oxide to a "dry" one [24]), leads to MIS solar cells of superior stability to those fabricated from oxides known to contain water [36].

For deposited oxides and those grown in strong oxidizing agents complete oxidation, and hence homogeneous insulating layers, are possible. These properties do not appear to have been realized in some MIS cells formed on n-Si that have utilized either deposition from an SiO source or chemical oxidation in HNO_3 to construct the thin oxide [31], [45]. However, oxidation in a solution of $(\text{H}_3\text{O})_2\text{SiF}_6$ seems very promising [24], [33]; the growth is self-limiting, oxides of low defect density are produced, and the introduction of fluorine into the oxide (in the form of SiOF_2) can be expected to greatly reduce the interface state density.

In the case of insulator formation on compound semicon-

TABLE I
INSULATING LAYER GROWTH METHODS USED IN MIS CELLS

Semiconductor	Method	Time	Reference
Si	hot HNO ₃	~8 min	[13], [31]
"	boiling H ₂ O		[13]
"	10-percent HF in H ₂ O	<1 min	[32]
"	SiO ₂ in 40-percent HF	1.5-2 min	[33]
"	anodization		[13], [23]
"	evaporation of SiO		[31]
"	150°C in air	5-70 h	[19]
"	400°C in air	5-60 min	[34]
"	620°C in air	15-30 min	[35]
"	420°C in dry oxygen	10 min	[36]
"	420°C in wet oxygen	5-40 min	[37]
"	514°C in oxygen	12 min	[23]
"	450°C in wet nitrogen	15-30 min	[38]
"	450°C in N ₂ /O ₂	~10 min	[39]
"	480-500°C in N ₂ /O ₂	~30 min	[40]
"	700-900°C in steam	<5 min	[16], [28]
GaAs	evaporation of Sb ₂ O ₃		[41]
"	oxygen plasma	10-20 s	[42]
"	anodization in buffered 3-percent H ₃ PO ₄	~10 min	[42]
"	anodization in acetone/KMnO ₄	<1 min	[42]
"	120°C in ozone	20 min	[42]
"	25°C in H ₂ O/O ₂	50-100 h	[42]
"	105°C in air	70 h	[30]

ductors, the range of possible oxide compositions is increased. For example, in GaAs the native oxide comprises a mixture of As₂O₃, Ga₂O₃, and GaAsO₄ [46]. Which of these oxides will dominate in the deliberately grown native oxide in GaAs MIS cells depends upon the method of oxidation and the substrate single-crystal orientation [42]. In oxides produced from ozone, for example, As₂O₃:Ga₂O₃ ratios of less than unity, as can be obtained using Ga-rich (111) surfaces, give higher values of V_{oc} than oxides formed on As-rich ($\bar{1}\bar{1}\bar{1}$) surfaces and exhibiting As₂O₃:Ga₂O₃ ratios greater than unity [42]. However, the best results using native oxides on GaAs have been obtained with films grown at room temperature by exposure to oxygen saturated with water vapor; and in this instance, the major constituent of the oxide is As₂O₃ [46]. As n -values for MIS cells using this oxidation procedure are close to unity (<1.10), while for diodes with ozone-grown oxides n is in the range 1.15-1.85, it appears that surface state effects resulting from the oxidation treatment, and not the actual oxide composition, could be responsible for the observed differences in photovoltaic performance. For the best cells with As₂O₃-rich oxides there is an increase in free arsenic concentration on moving towards the oxide-semiconductor interface [46], suggesting the presence of acceptor-like surface states and the possibility of improved photovoltaic performance with n -type substrates.

Formation of nonnative oxides is of interest for MIS cells as it offers a flexibility in design and also as possible deposition processes (e.g., vacuum evaporation, sputtering) are attractive for improving the throughput and perhaps economics of the overall solar-cell fabrication process. For Si cells, Si₃N₄ is one possibility under consideration [47], and for GaAs, high-efficiency cells have already been realized using evaporated layers of Sb₂O₃ [41].

The growth of any thin insulator will be influenced by the preparation of the semiconductor surface prior to oxidation.

For MIS cells on single-crystal Si, standard cleaning sequences involving hydrogen peroxide and formic acid followed by an HF etch are commonly used. For MIS cells formed on Si EFG ribbon, a significant degree of surface state passivation has been found to result from growing a thick thermal oxide film, sometimes after a pre-etch in H₂O:HF:CH₃COOH (1:1:1) with a few drops of HNO₃ added, and then removing the oxide in HF before continuing with the normal cleaning process [44]. For GaAs MIS cells, an etch involving NH₄OH:H₂O:H₂O₂ (10:1:1) for 15 s followed by H₂SO₄:H₂O₂:H₂O (10:1:1) for 30-60 s appears superior to the bromine/methanol etch more usually associated with GaAs in that it leaves behind a more uniform native oxide layer and is freer of carbonaceous contamination [41].

As a final treatment to the insulator-semiconductor structure, annealing could be advantageous in reducing surface state densities or stabilizing the system. Annealing of Si devices in nitrogen at 300-500°C for about 30 min is sometimes used [13], [29], [48], but similar steps are apparently not used in present GaAs MIS cells.

IV. RESULTS AND DISCUSSION

A. Open-Circuit Voltage

To obtain enhancement of V_{oc} through introducing a thin insulating layer into the Schottky diode structure, the oxide must be thick enough to allow the beneficial effects of current transport control, or modifications to n or ϕ_b to take place, yet not so thick that photocurrent suppression occurs. Thus for a given diode structure and fabrication procedure there is an optimum value of oxide thickness δ . Fig. 4 demonstrates this for MIS cells on p - and n -type Si substrates.

The fact that in Fig. 4 V_{oc} values are larger on the p -Si cells cannot, in this case, be attributed to a substrate doping-type effect as the surface orientations, barrier metal materials, and

TABLE II
 V_{oc} VALUES FOR Si MIS CELLS

Substrate			Barrier Metal	Oxidation Method ¹	V_{oc} (mV)	Reference
Type	Orientation	Resistivity ($\Omega \cdot \text{cm}$)				
p	100	1	Al	Th	615	[39]
p	100	0.1	Al	Th	610	[39]
p	100	0.2	Al	Th	600	[49]
p	100	2	Cr	Th	600	[50]
p		1	Al	Th	560	[36]
p		35.1	(SiO ₂)	Th	554	[51]
p	100	1	Ti	Chem	550	[13]
p	100	2-8	Al	Th	470	[19]
p		3-15	Al	Nat	470	[29]
n	111	1-10	Au	Dep	536	[45]
n	100	0.15-0.25	Au	Th	444	[23]
n	100	8-19	Au	Anod	427	[23]
n	111	5	Au	Th	420	[34]
n	111	5-10	Pt	Th	410	[37]
n	111	1-10	Au	Chem	400	[45]

¹Th = thermal, Chem = Chemical, Nat = natural oxide (spontaneous), Dep = evaporated, Anod = anodized.

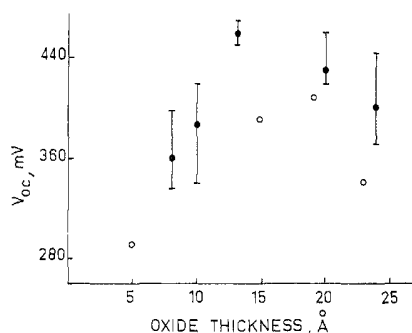


Fig. 4. Dependence of V_{oc} on oxide thickness for experimental Si MIS solar cells. ● = p-type (after Pulfrey [19]), ○ = n-type (after Lillington and Townsend [34]).

oxide fabrication treatments were not the same for both sets of devices. However, it does appear that, in general, MIS cells on p-Si can give higher values of V_{oc} than are obtainable with n-Si substrates, see Table II. This is perhaps not surprising as most of the oxidation methods used in Si MIS diode fabrication are likely to produce an Si-rich region close to the insulator-semiconductor interface (see Section III). The donor-like surface states [5] or positive charge in the oxide [22] associated with this excess Si region, would both induce unfavorable decreases in band bending in n-type substrates. It is probably significant that the only MIS n-Si cells to exhibit $V_{oc} > 450$ mV utilized deposited oxides [45], in which the presence of an Si-rich region could not definitely be ascertained [31]. In these devices, the modification to the dark current was achieved via a decrease in the electron tunneling probability factor Θ (see (4)) and also by the creation of a favorable distribution of surface states that gave $n = 1.34$. Devices prepared in the same way, except that oxides were grown in hot nitric acid, yielded similar reductions in J_{th} but generally lower values of n [45]. It is not clear at present why oxides deposited by the slow evapora-

tion of SiO should produce desirable surface state densities, with presumably an acceptor-like character [23].

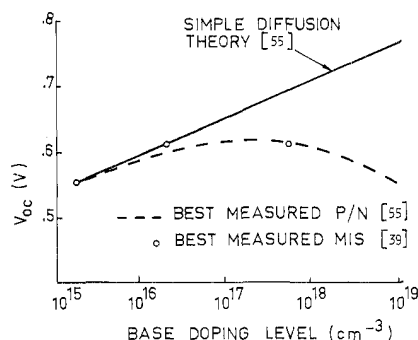
One way whereby the performance of MIS n-Si diodes might be improved is by operation in a minority carrier tunnel mode, in which the role of interface states is of reduced importance [4]. To achieve this would require use of a high work function barrier metal. The fact that neither Au nor Pt (Table II) seem capable of meeting this requirement indicates that in practical n-Si devices zero bias barrier height suppression is occurring. As previously mentioned, oxide positive charge or interface donor states could both induce such an effect.

To turn the apparently recalcitrant Si-rich region to advantage in MIS cells it follows that p-type substrates should be used. In this case, a low work function metal, Al for example, can induce an inversion layer at the semiconductor surface and lead to minority carrier tunnel diodes. The first three devices listed in Table II have all been claimed to operate in this mode. It is conceivable that the cells fabricated by Anderson's group [50], for which $V_{oc} = 600$ mV, are also minority carrier diodes. The slowly evaporated Cr barrier metal layer used in these cells has a low value of work function (~ 4.1 eV) which would be sufficient to cause inversion in the $2\text{-}\Omega \cdot \text{cm}$ substrates used. Alternative explanations of the high photovoltage performance of Cr-p-Si cells have been given in terms of zero bias barrier height enhancement [22] with an added contribution from the n -factor [52]. Dark conduction characteristics would assist in resolving this issue as minority carrier diodes display $\ln I$ - V curves with inverse slopes around 2 for low bias and 1 for high bias [16], [19], [39] whereas in the case of a dominant thermionic emission current a single exponential curve results with inverse slope (n -factor) between 1 and 2.¹

¹Very recent data [53] for the Cr-Si cells show inverse slopes of ≈ 2.5 for $V < 0.35$ V and ≈ 1.3 for $V > 0.35$ V, supporting the minority carrier diode description.

TABLE III
 V_{oc} VALUES FOR Au/GaAs MIS CELLS

Substrate			Oxidation Method	δ (nm)	J_0 ($A \cdot cm^{-2}$)	n	ϕ_b (eV)	V_{oc} (mV)	Reference
Type	Orientation								
1	n	B $\bar{1}\bar{1}\bar{1}$	O ₃		1.5×10^{-9}	1.85	1.035	655	[42]
2	n	100	O ₃		6×10^{-12}	1.15	1.025	680	[42]
3	n	A111	O ₃		8×10^{-11}	1.56	1.032	741	[42]
4	n	100	H ₂ O/O ₂ , 114 h	3.4	1×10^{-10}	1.40	1.033	758	[42]
5	n	100	H ₂ O/O ₂ , 42 h	3.1	6×10^{-14}	1.045		733	[57]
6	n	100	Sb ₂ O ₃	2.8	$10^{-12} - 10^{-14}$	<1.10		794	[46]


 Fig. 5. Variation of V_{oc} with substrate doping density for Si solar cells.

This p-n junction type behavior from p-Si MIS cells suggests that two features recently used in enhancing the photovoltage response of Si homojunction cells could also be applied to the surface junction devices, i.e., the use of low resistivity base material, or the employment of back surface fields with high resistivity base material. In Si homojunctions, the dark current decreases with increase in base doping density until the back injection current component (holes diffusing from the base to the surface layer in n^+p cells) dominates. Due to the very heavily doped nature of the surface layer, bandgap shrinkage [54] and an increased intrinsic carrier concentration [55] are likely to impose a lower bound on the back injection current. However, these high doping density effects are not present in minority carrier MIS cells, owing to the induced nature of the equivalent surface layer. In principle at least, then, it is possible that the diffusion current in MIS minority carrier diodes can be reduced (and thus V_{oc} increased) as the base layer doping density increases in the manner predicted by simple diffusion theory [55], see Fig. 5. Present data for MIS p-Si cells are also shown in Fig. 5 and it is evident that there has not yet been any improvement, with respect to p-n cell performance, at low base resistivities. This may be because a barrier metal with a lower work function than that of Al is needed to guarantee inversion at the higher values of doping density [56].

If suitable trapping centers can be generated in the oxide then minority carrier MIS devices not exhibiting an inversion layer can result, see Fig. 3. It is possible that the $(H_3O)_2SiF_6$ oxidation process described in Section III may produce oxides containing the required type of electron trapping center [24], [33]. However, the self-limiting nature of this oxidation reaction may be such as to not allow formation of sufficiently

thick oxides ($>50 \text{ \AA}$) to completely suppress the thermionic emission current. In this event, the creation of an inversion layer by employment of a suitable barrier metal will again be necessary.

No semiconductor material rivals Si as far as diversity of MIS cell data is concerned. In fact, n-type GaAs is the only other material for which there is any detailed data on MIS solar cell performance, see Table III. With this material V_{oc} values are higher than in Si, as would be expected from the larger bandgap of GaAs.

For cells utilizing oxides grown in ozone, some enhancement (with respect to cells fabricated without deliberate oxidation) of barrier height is achieved, but an increase in the n-factor appears to be accompanied by an increase in the saturation dark current; see samples 1, 2, 3, Table III. The semiconductor surface orientation differed between samples 1, 2, and 3, and this doubtless led to different surface state properties, with the Ga-rich (111) face producing the most favorable situation as regards photovoltage response. The data set for the ozone oxides exhibit some of the features that might be expected from a surface state distribution that spanned the entire semiconductor bandgap, with a zero bias neutral level that was below the Fermi level for Ga-rich surfaces and above the Fermi level for As-rich surfaces [23]. However, ϕ_b for these cells is insensitive to the orientation of the surface and so the differences in J_0 would appear to arise from currents that are not thermionic in origin. This suggests that the surface states are not only acting in an electrostatic fashion, but are also playing an active role in carrier recombination and generation of surface state tunnel currents.

Such effects are also present in cells using oxides grown in oxygen saturated with water vapor on surfaces etched in bromine/methanol (sample 4, Table III) [57], but are greatly reduced in cells etched as described in Section III; see sample 5, Table III. The thickness difference between samples 4 and 5 may be significant as V_{oc} values for GaAs MIS cells are still rapidly increasing with thickness at δ values as high as $35 \text{ \AA}$, [46]. Oxides grown in this manner are rich in As_2O_3 and show an increase in free arsenic concentration towards the oxide-semiconductor interface [46]. This suggests the possibility of negative charge in the oxide or acceptor-like surface states, both conditions that would be advantageous for photovoltaic action with n-type substrates. Data for MIS cells on p-type GaAs are not available but would, no doubt, be of assistance in evaluating the importance of the free arsenic presence.

It seems likely that the factors limiting V_{oc} in present GaAs MIS cells are associated in some manner with the native oxide and the degree to which it passivates the GaAs surface. More insight into the nature of these factors can be expected on detailed evaluation of the performance of cells employing non-native oxides. Preliminary results from MIS cells using oxide layers of boat-evaporated Sb_2O_3 (sample 6, Table III) indicate that improvements in V_{oc} can be obtained [41], [46].

B. Short-Circuit Current Density

Thus far, MIS solar-cell development has emphasized enhancement of V_{oc} , but attainment of high values of J_{sc} is by no means trivial. The first requirement is to use thin enough insulating layers so that photocurrent suppression effects (decreasing tunnel transmission coefficient or increasing effective series resistance) are avoided. For Si, oxide thicknesses less than 25 Å are required [3], [4], [19], [34] unless suitable minority carrier tunneling sites exist in the insulator (Fig. 3). For GaAs slightly thicker (28–35-Å) oxides can be tolerated [46].

On satisfaction of the oxide thickness requirement J_{sc} in MIS cells is affected principally by coupling of light into the semiconductor and recombination of photocarriers in the surface and bulk regions of the semiconductor. As the highest temperature involved in MIS cell processing need only be about 500°C (for ohmic contact alloying), it should be possible to maintain values of minority carrier lifetime appropriate to the starting material. This suggests good long-wavelength response. Good short-wavelength response should materialize through the action of the surface field in devices possessing depletion or inversion layers at the semiconductor surface [18], and through the avoidance of "dead" layers associated with some diffused junction devices. This is demonstrated in Fig. 6 [13], where the blue response of an MIS cell is shown to be superior to that of a diffused n⁺-p cell made from similar Si starting material. The slightly reduced red response of the MIS cell has been attributed to absorption in the Ti barrier metal used in this instance [13].

It is the existence of a highly reflective barrier metal layer that presents the major impediment to attainment of high J_{sc} values in MIS cells. Antireflection (AR) coatings are clearly required, and single-layer coatings with refractive index (n_R) greater than 2.1 can theoretically give reflection losses as low as 6 percent for both Si and GaAs [9], [10]. The ideal for GaAs would be an AR coating of $n_R = 2.34$, but the use of practical coatings with n_R less than this (e.g., Ta_2O_5 , $n_R = 2.2$; Sb_2O_3 , $n_R \approx 2.0$) still enables collection efficiencies to approach 80 percent in MIS cells [46]. The desirable properties of Ta_2O_5 have led to its employment in both GaAs and Si MIS cells [44], [57], but the electron-beam method of depositing this material is not recommended as degradations in V_{oc} ensue. Stirn has suggested [57] that this effect may be caused by scattered electrons or soft X-rays from the electron gun, or be due to dissociation of the dielectric coupled with heat-induced migration of the metallic species through the oxide during evaporation. Laser flash evaporation or boat evaporation avoids these problems and 1-cm² GaAs MIS cells using the latter method for deposition of Sb_2O_3 as an AR coating

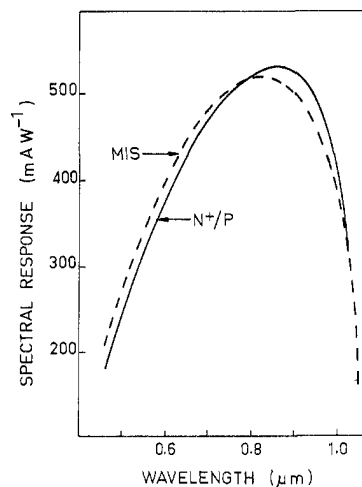


Fig. 6. Spectral responses of MIS cell and diffused junction n⁺-p cell made from similar Si starting material. After Fabre [13].

have yielded $J_{sc} = 25.7 \text{ mA} \cdot \text{cm}^{-2}$ (simulated AM1 conditions) [46]. This value is very close to the highest reported values for other solar-cell systems employing GaAs, e.g., $28.5 \text{ mA} \cdot \text{cm}^{-2}$ (AM0 sunlight) for $\text{GaAl}_{1-x}\text{As}_x/\text{p-n GaAs}$ [58] and $28 \text{ mA} \cdot \text{cm}^{-2}$ ($\sim$ AM1.35 sunlight) for AlAs/GaAs [59]. The high value of J_{sc} attained in the GaAs MIS cells attests to the good photon coupling, low series resistance, and high minority carrier diffusion length ($\sim 3.5 \mu\text{m}$) in the base layer [60]. The surface field structure of MIS cells is particularly suited to GaAs and related compounds as the high absorption coefficients ensure photocarrier generation in the regions of high field strength. Present GaAs MIS cells use an Au barrier metal thickness of 60 Å. Further reduction in this thickness would cause degradation in J_{sc} due to series resistance effects [8], unless fine-grid patterns were used. Thus any further improvement in J_{sc} for GaAs MIS cells would seem to require either a double-layer AR coating or a single-layer coating with refractive index close to the ideal of 2.34.

For Si MIS cells the situation is not so clearcut as there is considerable variation in reported values of J_{sc} for $\sim$ AM1 sunlight, see Table IV. Part of the spread can be attributed to the wide range of barrier metal areas that have been used. Collection of photocarriers from regions peripheral to the barrier metal layer will tend to produce artificially high values of J_{sc} in small-area devices [62]. An effective minority carrier collection length Δ (yielding an effective diameter of $d + 2\Delta$ for a circular contact of metal diameter d) can be defined and will depend on the semiconductor surface treatment and oxide preparation method. Conditions that produce a depletion region under the bare oxide will give low values of Δ , whereas higher values of Δ will tend to result when inversion or accumulation layers are present [62]. Using $\Delta = 100 \mu\text{m}$ for p-Si and $\Delta = 200 \mu\text{m}$ for n-Si [62] and basing J_{sc} calculations on total barrier metal area plus extra peripheral collection area, the reported data reduce to column 9 of Table IV. This maneuver removes much of the variation in the as-reported results and highlights the good photoresponse of the $\text{TiO}_2/\text{Ti}/\text{SiO}_x/\text{p-Si}$ system [13] as shown in Fig. 6. The use of starting material with long minority carrier diffusion length ($\sim 100 \mu\text{m}$) and very

TABLE IV
 J_{sc} VALUES FOR Si MIS CELLS

Type	AR Coating		Barrier Metal		Total Area (cm ²)	Peripheral Area ¹ %	J_{sc}		Reference
	Material	Thickness (nm)	Material	Thickness (nm)			Quoted (mA · cm ⁻²)	Corrected	
p	TiO ₂		Ti	5	3.0	1	28.6	28.3	[13]
p			SiO ₂	100	1.1	0	30.3	30.3	[51]
p	SiO	67	Cr/Cu/Cr	4/6/0.5	1.0	3	22.3	21.6	[35]
n			Au	10	0.33	13	24.0	21.2	[34]
p			Al		0.3	7	23.0	21.5	[39]
n			Au		0.196	19	22.1	18.6	[23]
n			Au	10	0.18	20	23.3	19.4	[45]
n	In ₂ O ₃	70	Pt	8	0.12	23	29.2	23.7	[37]
p	SiO/ZnS	60/45	Al	10	0.026	25	26.5	21.2	[29]
p			Au	7	0.019	74 ²	43.7	25.1	[32]
n			Au		0.0078	96	42.0	21.4	[61]

¹Computed as in [62], taking $\Delta = 100 \mu\text{m}$ for p-type and $\Delta = 200 \mu\text{m}$ for n-type.

² Δ taken as $200 \mu\text{m}$ in this case because of likely inverted surface due to "dry" oxide [32].

thin (50-Å) Ti layer undoubtedly contributes to the good performance of this device. Also, the refractive index of TiO₂ (2.25) is well suited to Si MIS cells [9], and this material is probably superior to the commonly used SiO, which exhibits significant UV absorption [44]. At 50 Å, Ti has a sheet resistance of about $800 \Omega/\square$ [13] and many contact fingers are required to reduce the series resistance to acceptable values. An alternative approach to reducing the series resistance in cells using Cr barrier metal films ($\sim 1000 \Omega/\square$ for 50-Å thick layers [12]), has involved deposition of a covering layer (60 Å) of high-conductivity copper. Resulting sheet resistances are around $20 \Omega/\square$ and few contact fingers (5-10/cm) are required. After coating with SiO, reflection from the composite metallic surface is still significant but steady improvements on progressively reducing the Cr thickness have been obtained [63].

The highest J_{sc} value reported in Table IV is for an inversion layer cell using no barrier metal layer. This highlights the fact that reflection from the metallic surface is the factor presently limiting J_{sc} in Si MIS cells. Development of conducting metal oxide technology can be expected to lead to some improvement in this regard as such an oxide, deposited on top of a very thin barrier metal, would combine the features of AR coating and series resistance reduction in one film.

C. Fill Factor

For Si MIS cells fill factors as high as 0.73-0.75 have been reported [19], [34], [45], [49], while for GaAs the best devices yield FF values in the range 0.79-0.83 [41]. These higher values for GaAs reflect the lower values of I_0 that can be obtained with this material. Using semiconductor material with a high bandgap also slightly reduces the dependence of FF on series resistance, although the importance of shunt resistance effects increases correspondingly. However, attaining a high value of R_{sh} is not usually a problem with the MIS structure [16], [17].

The fact that low values of J_{sc} (7-22 mA · cm⁻²) were associated with the high FF single-crystal Si cells reported above indicates the presence of either series resistance effects or ex-

TABLE V
EFFICIENCY OF GaAs AND MIS CELLS

Semiconductor	Maximum Reported Values				Present Technology η_{max}
	V_{oc} (mV)	J_{sc} ¹ (mA · cm ⁻²)	FF	η ¹ (%)	
GaAs	830	27	0.82	17.0	18.4
Si	615	28.3	0.75	10.2	13.1

¹Based on total collector area.

cessively thick barrier metal or oxide layers. While amelioration of the latter two items requires only closer control over deposition conditions, reduction of R_s suggests the need for more elaborate top contact metallization patterns, at least for large-area cells.

D. Efficiency

The highest reported values of V_{oc} , J_{sc} (based on total area), and FF for Si and GaAs cells are given in Table V. Attainment of these values in a single cell would yield $\eta = 13.1$ percent for Si and $\eta = 18.4$ percent for GaAs. Practical cells have reached efficiencies (based on total area) of 10.2 percent for Si [13], [53] and 17 percent for GaAs [41]. In principle, the maximum attainable efficiency is close to that of p-n junction cells, i.e., ~ 20 percent for Si and ~ 24 percent for GaAs.

In present GaAs MIS cells, the limiting factor is V_{oc} and it has been suggested in Sections III and IV that this is related to the poor passivation properties of the native oxide. Use of nonnative oxides offers the prospect of improvements in this regard [41], [46]. In Si MIS cells, J_{sc} is the factor presently limiting overall performance. Enhancement of this factor would seem to require more appropriate antireflection coatings, multifinger grid contacts, and, perhaps, thinner barrier metal layers.

E. MIS Solar Cells on Nonsingle Crystalline Substrates

One of the attractions of the MIS structure is its compatibility with potentially cheap nonsingle crystalline semiconductor

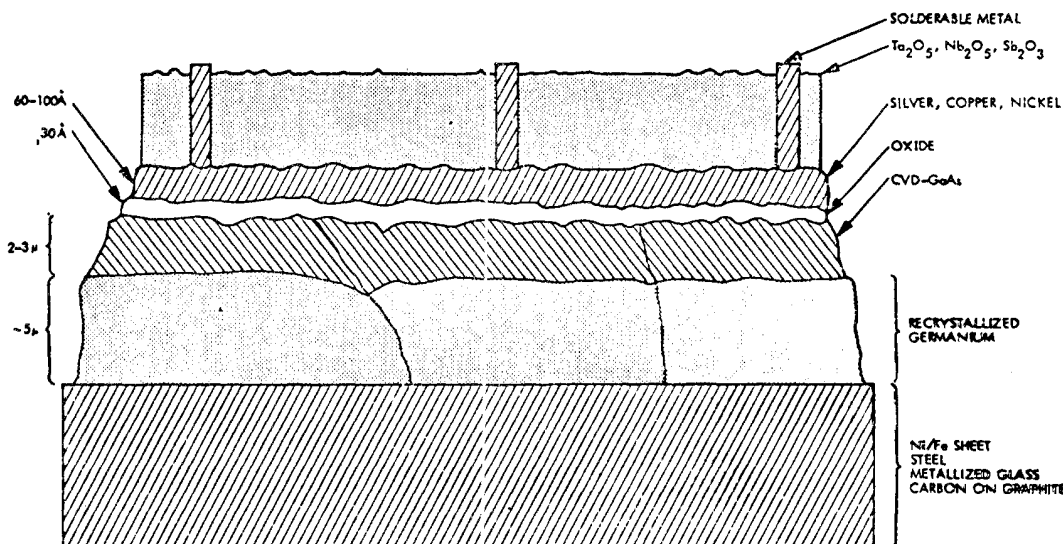


Fig. 7. Schematic of a thin-film GaAs MIS solar cell. After Stirn [46].

substrates, e.g., see Fig. 7. Actual experimental data for cells on such substrates are only now beginning to appear as work up until recently has concentrated on elucidating the basic parameters affecting MIS performance, and has thus utilized single-crystal substrates.

MIS cells of area $\sim 1.6 \text{ cm}^2$ on EFG ribbon have yielded $J_{sc} \sim 20 \text{ mA} \cdot \text{cm}^{-2}$, FF values up to 0.71, and V_{oc} values up to 540 mV [44], [50]. The low value of V_{oc} indicates a high density of unfavorable surface states [50], and a partial passivation treatment involving thick oxide growth and subsequent etch-back has proved necessary to raise V_{oc} to the value previously quoted. J_{sc} is also low in this device and, while this may be because of a nonoptimized top contact pattern and front surface optical properties, effects due to the quality of the semiconductor bulk material, e.g., low minority carrier lifetime, are possibly responsible.

MIS cells utilizing substrates of recently developed cast polycrystalline ("granular") silicon have great potential and the first reported results show $J_{sc} = 17.7 \text{ mA} \cdot \text{cm}^{-2}$ (based on total area of 1 cm^2), $FF = 0.76$, and $V_{oc} = 523 \text{ mV}$ [36]. It has not yet been established to what extent the substrate bulk properties are responsible for the relatively low values of J_{sc} and V_{oc} , but it would appear from the high value of FF that grain boundary shunting effects are negligible. From the surface roughness of these substrates and also on account of the presence of a variety of crystallographic orientations, some nonuniformity in oxide layer properties can be expected and this may be presently placing a limit on V_{oc} .

In small-area (0.2-cm^2) MIS cells on polycrystalline GaAs, J_{sc} values $\sim 25 \text{ mA} \cdot \text{cm}^{-2}$ and FF values of ~ 0.78 have been attained with substrates comprising grains of either $100\text{-}500 \mu\text{m}$ or some millimeters [46]. The associated values of V_{oc} were ~ 705 and $\sim 790 \text{ mV}$, respectively. The increase in V_{oc} with grain size may indicate a reduction in grain boundary recombination dark current but this is not supported by the lack of variation in FF . Surface state effects related to the orientation of preferential grains may thus be a relevant factor.

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C-V Profiling of GaAs FET Films

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Abstract—The depletion layer capacitance of a Schottky barrier on a GaAs FET film can only be measured in series with the resistance of the undepleted portion of the film. This inherent series resistance may be significant at all values of bias and causes large errors in C - V profile determinations. By treating the depletion layer capacitance and the series resistance as a distributed RC transmission line, it is possible to define an effective series resistance which can be related directly to the resistivity of the film. Using parameters typical of epitaxial films grown for GaAs FET applications, general criteria are developed for the profilability of these films. It is shown that, in general, films with small pinchoff voltages (i.e., films intended for low-noise FET applications)

are much more difficult to profile accurately than films with large pinchoff voltages.

I. INTRODUCTION

CAPACITANCE-VOLTAGE (C - V) profiling [1]–[4] is probably the single most important method used to characterize GaAs films grown on semi-insulating substrates for MESFET [5] applications. The reasons for the wide acceptance of this measurement technique are clear: 1) many common metals form excellent Schottky barriers on GaAs without elaborate surface preparation, passivation, or guarding; 2) one relatively simple measurement provides the material parameters of greatest interest to the crystal grower and de-

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