

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Hanwha Solutions Corporation

v.

Maxeon

Inter Partes Review

Nos. IPR2024-01199 and IPR2024-01203

U.S. Patent Nos. 8,878,053 & 8,222,516

Petitioner's Oral Argument – December 3, 2025

Proposed Agenda

- Overview of the Grounds and Challenged Claims
- Disputed Issues
 - 1 Motivation to combine Froitzheim and Gan & Froitzheim, Gan, and Smith
 - 2 Froitzheim Discloses Claim 12
 - 3 Motivation to combine Froitzheim and Borden-575
 - 4 Motivation to combine Li and Gan & Li, Gan, and Smith
 - 5 Sheats Discloses Claim 5

Overview of the Grounds and Challenged Claims

Overview of Grounds

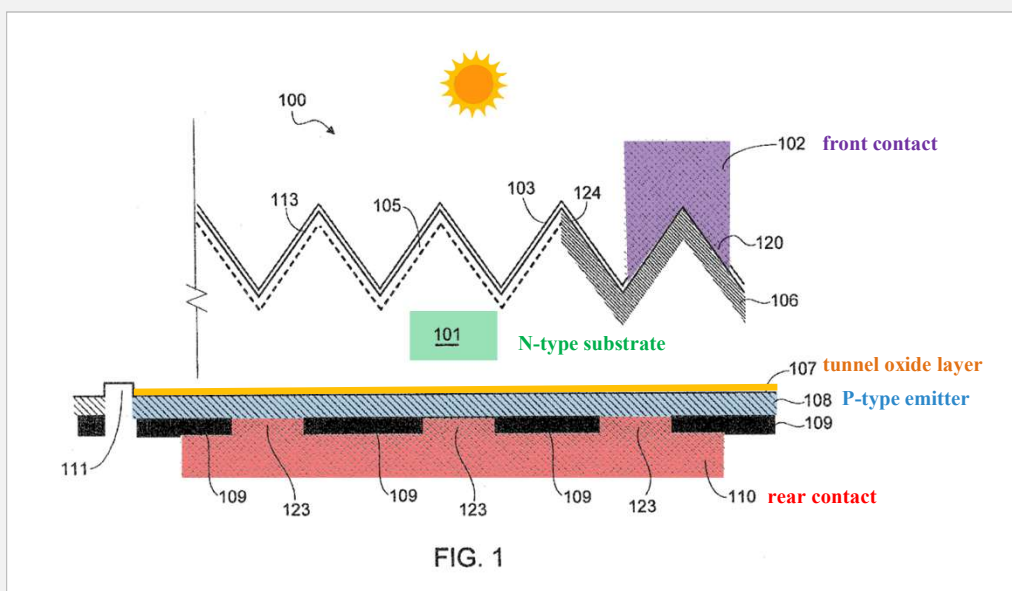
IPR No.	Ground	Claims	References
2024-1203 ('516 patent)	I	1-4, 6-12	Froitzheim and Gan
2024-1203 ('516 patent)	II	5	Froitzheim, Gan, and Sheats
2024-1203 ('516 patent)	III	1-4, 6-12	Froitzheim and Borden-575
2024-1203 ('516 patent)	IV	5	Froitzheim, Borden-575, and Sheats
2024-1203 ('516 patent)	V	1-2, 8-11	Li and Gan
2024-1199 ('053 patent)	I	9-12, 14, 16-20	Froitzheim and Gan
2024-1199 ('053 patent)	II	1-20	Froitzheim, Gan, and Smith
2024-1199 ('053 patent)	III	9-20	Li, Gan, and Smith

Differences Between Hanwha IPRs and Canadian Solar IPR Nos. 2024-01039, -01040

- Hanwha's and CSI's Petitions are completely independent
- Hanwha's Petitions Challenge All Claims
 - CSI's IPR for the '516 patent does not address claims 1-8
 - CSI's IPR for the '053 patent does not address claims 1-8
- Hanwha's Petitions Rely on Different References
 - Sheats, Borden-575, Li, & Smith
- Hanwha relies on different expert testimony
- Hanwha relies on different supporting references

See, e.g., '516 Petition, 5-7; '053 Petition, 5-7

Challenged Claims: Representative Independent Claim 9 of the '516 Patent



9. A solar cell having a front side facing the sun to collect solar radiation during normal operation and a backside opposite the front side, the solar cell comprising:

a substrate having a textured front surface;

an emitter layer formed over a back surface of the substrate, the emitter layer forming a backside junction with the substrate;

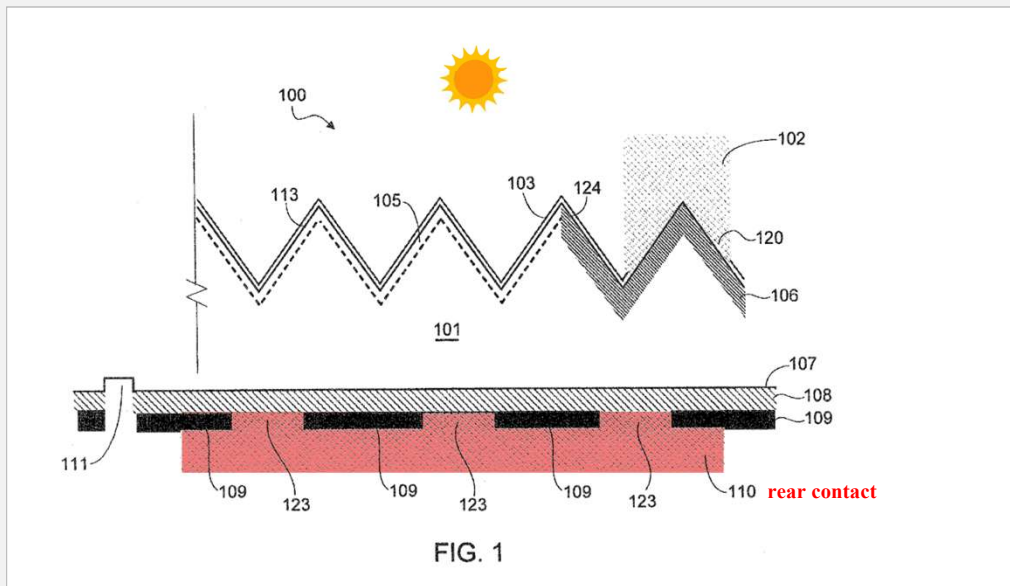
an oxide layer formed between the back surface of the substrate and the emitter layer;

a first metal contact making an electrical connection to the substrate on the front side of the solar cell; and

a second metal contact making an electrical connection to the emitter layer on the backside of the solar cell, the first metal contact and the second metal contact being configured to allow an external electrical circuit to be powered by the solar cell.

'516 Ex.1001 ('516 Patent), Fig.1, claim 9; '516 Petition, 15

Challenged Claims: Dependent Claim 12 of the '516 Patent

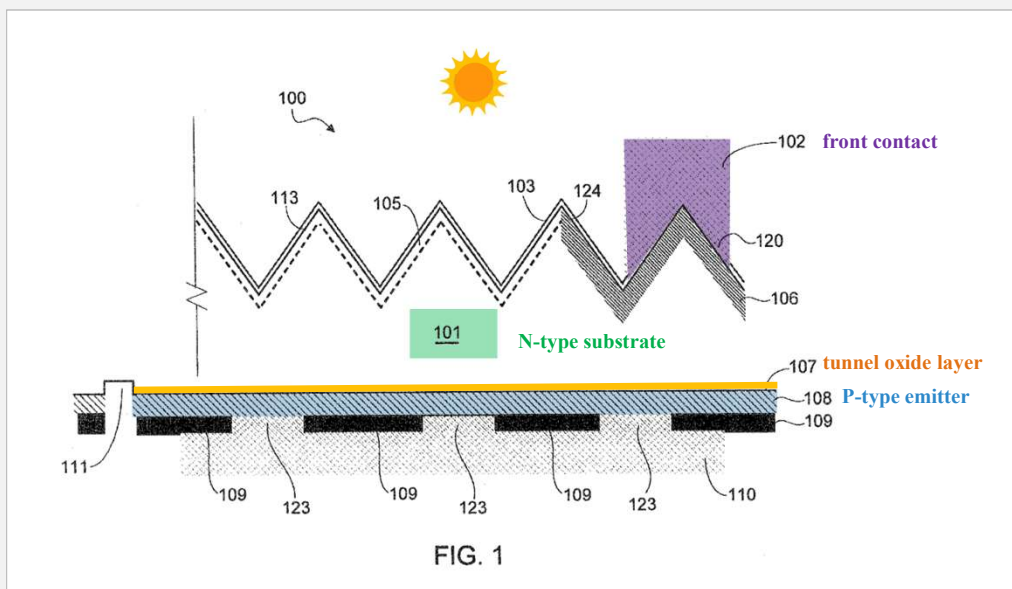


electrical connection to the polysilicon emitter 108. The metal contact 110 may be formed using a printing process.

12. The solar cell of claim 9 wherein the second metal contact comprises silver formed over a layer of silicon dioxide.

'516 Ex.1001 ('516 Patent), Fig.1, 5:50-51, claim 12; '516 Petition, 15, 50-51; '516 Petitioner's Reply, 15-16

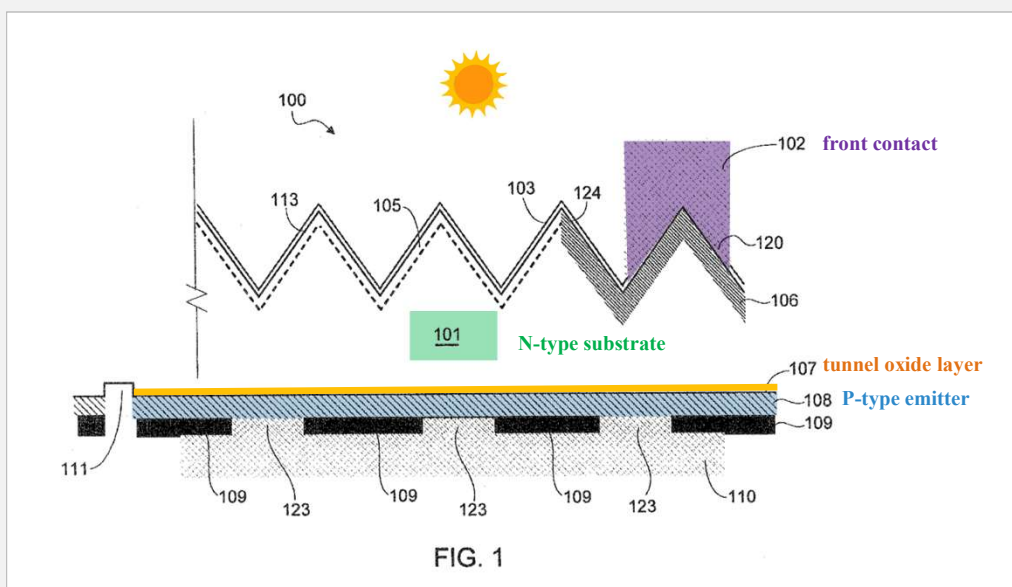
Challenged Claims: Representative Independent Claim 16 of the '053 Patent



16. A method of fabricating a solar cell comprising:
forming an oxide layer over a back surface of a silicon substrate;
forming a layer of polysilicon over the oxide layer;
diffusing dopants into the layer of polysilicon to form a backside junction with the silicon substrate;
diffusing dopants into a front surface of the silicon substrate, the front surface of the silicon substrate facing the sun during normal operation; and
forming a metal contact on the front surface of the silicon substrate, wherein the metal contact is electrically coupled to the silicon substrate.

'053 Ex.1001 ('053 Patent), Fig.1, claim 16; '053 Petition, 14

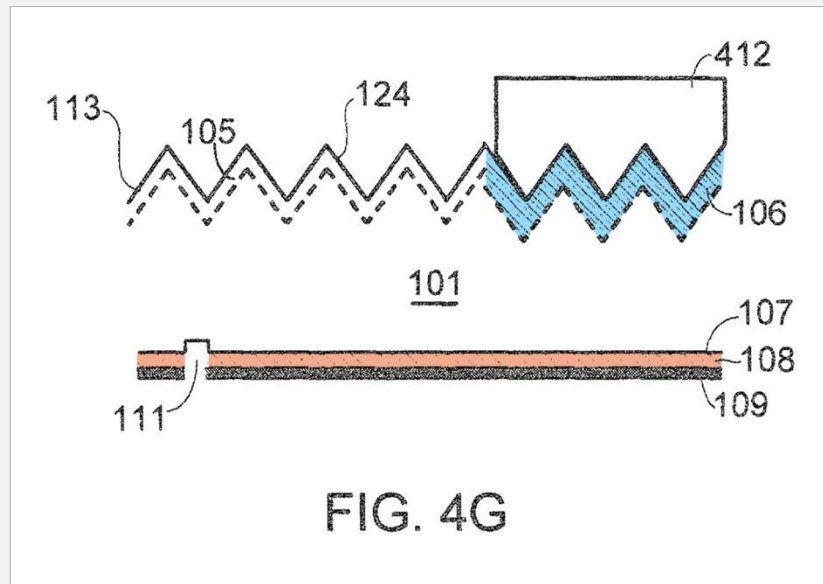
Challenged Claims: Representative Independent Claim 9 of the '053 Patent



9. A method of fabricating a solar cell comprising:
forming a layer of polysilicon over a back surface of a silicon substrate;
forming a first dopant source layer over the layer of polysilicon;
diffusing dopants from the first dopant source layer to the layer of polysilicon to form a backside junction with the silicon substrate;
diffusing dopants into a front surface of the silicon substrate, the front surface of the silicon substrate facing the sun during normal operation; and
forming a metal contact on the front surface of the silicon substrate, wherein the metal contact is electrically coupled to the silicon substrate.

'053 Ex.1001 ('053 Patent), Fig.1, claim 9; '053 Petition, 14

Challenged Claims: Dependent Claim 15 of the '053 Patent



The drive-in step to dope the polysilicon emitter **108** on the backside and to form the N-type doped regions **105** and **106** on the front side may be **formed in-situ**, which in the context of the present disclosure means a single manual (i.e., by fabrication personnel) loading of the substrate **101** in a furnace or other single chamber or multi-chamber processing tool. In one embodiment, the drive-in step is performed in a diffusion furnace. The preceding sequence of steps leading to the drive-in step allows for in-situ diffusion, which advantageously helps in lowering fabrication cost.

15. The method of claim **9** wherein the diffusion of dopants from the first dopant source layer to the layer of polysilicon and the diffusion of dopants into the front surface of the silicon substrate are performed in situ.

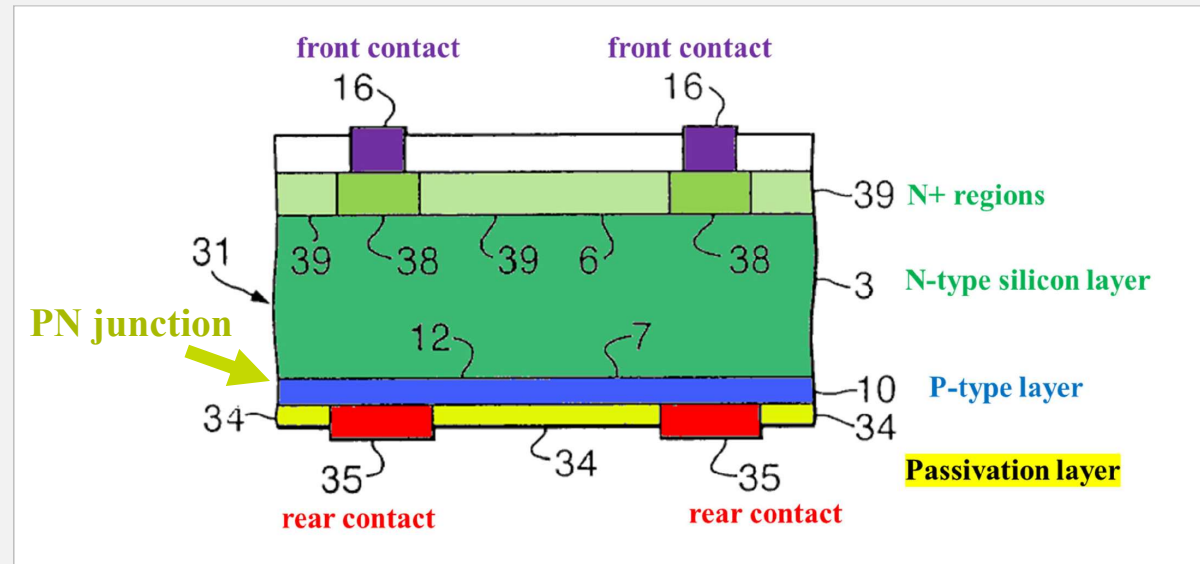
'053 Ex.1001 ('053 Patent), Fig.1, 5:9-18, claim 15; '053 Petition, 15, 65; '053 Ex.1003, ¶91

Disputed Issues

Froitzheim and Gan
IPR2024-01203 – Ground I
IPR2024-01199 – Ground I

Froitzheim's Undisputed Solar Cell Structure

- ✓ Backside PN junction
- ✓ Diffused emitter
- ✓ Front and rear contacts
- ✓ Anti-reflective coating
- ✓ N+ front surface field
- ✓ Textured front surface



Ex.1004, Fig. 3

Ex.1004, [0010]-[0011], [0019], [0024]-[0034], [0050]; '516 Ex.1003, ¶¶103-105; '516 Petition, 18-19, 29-30; '053 Ex.1003, ¶¶106-108; '053 Petition, 17-18; 26-27

Undisputed that Froitzheim teaches dopant layers for diffusion and screen printing for the metal contacts

"In general terms, a diffusion source layer that contains boron as a dopant is applied, e.g. spun, only onto the back of the n- doped silicon wafer. The diffusion source layer is one that contains boron and out of which the boron is thermally driven."

“Front and rear side contacts are preferably screen-printed in an industrial production process, and contacting is done at elevated temperatures.”

The diagram shows a cross-section of a solar cell with the following layers and components from top to bottom:

- front contact**: Two purple rectangular contacts at the top, labeled 16.
- N+ regions**: Two light green rectangular regions on the top surface, labeled 39.
- N-type silicon layer**: A large green rectangular layer in the center, labeled 3.
- P-type layer**: A thin blue horizontal layer below the N-type silicon layer, labeled 10.
- Passivation layer**: A yellow horizontal layer at the bottom, labeled 34.
- rear contact**: Two red rectangular contacts at the bottom, labeled 35.

Other labels include 31 (pointing to the N-type silicon layer), 38 (pointing to the N-type silicon layer), 6 (pointing to the N-type silicon layer), 7 (pointing to the N-type silicon layer), 12 (pointing to the N-type silicon layer), and 3 (pointing to the N-type silicon layer).

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Gan's Undisputed Polysilicon Emitter and Oxide Layer

Gan teaches that replacing a diffused emitter with a polysilicon emitter and oxide layers improves cell performance

Polysilicon emitters with a thermally grown interfacial oxide are examined in great detail. Both J_o and ρ_c are measured for the polysilicon emitter (contact) which is annealed under various conditions. $J_o \leq 5 \times 10^{-14}$ A/cm² and $\rho_c \sim 1 \times 10^{-5}$ Ω -cm² are obtained for both n- and p-type polysilicon emitters. The results also indicate that the interfacial oxide is only broken by a very small fraction in order to have $\rho_c \sim 1 \times 10^{-5}$ Ω -cm². Under such a condition, J_o is primarily dominated by the recombination at the oxide interface.

Ex.1005, 245

With the extent of the oxide breakup between these two extremes, various combinations of ρ_c and J_o can be obtained. It is of particular interest to know the ρ_c and the corresponding J_o when only a small fraction of the interfacial oxide is broken. For silicon solar cells operated under high concentrated sunlight, the emitter recombination is one of the main recombination that limit the solar cell performance [8]. This is because the diffused-emitter, which is formed with dopant diffusion into the base (substrate), has high J_o ($=4.5 \times 10^{-13}$ A/cm²). Consequently, the cell performance can be improved if the diffused-emitter is replaced with the polysilicon emitter, of which the J_o is less than 4.5×10^{-13} A/cm² and the ρ_c is low enough.

Ex.1005, 245

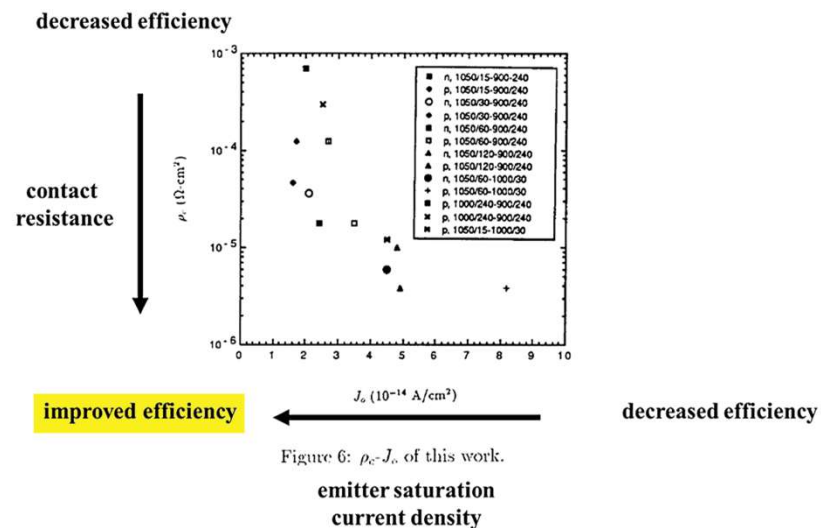
'516 Petition, 19-21, 30-33; '516 Ex.1003, ¶¶106-109, 128-132; '053 Petition, 18-20, 27-31; '053 Ex.1003, ¶¶109-112, 125-132

Gan Teaches That Its Disclosed Structure Is Beneficial

Undisputed that Gan teaches a polysilicon emitter and oxide layer are beneficial for silicon solar cells

The data shown in Fig. 6 are quite useful for silicon solar cells. First, most of J_o are below 5×10^{-14} A/cm² which is about one order magnitude lower than that of diffused-emitters. Second, most of ρ_c are also lower than 5×10^{-5} Ω -cm². This means that the potential drop across the contact is negligible as long as the current density is less than 100 A/cm². It is interesting to see how much of the cell efficiency can be improved with polysilicon emitters of characteristics given here. With the cell modeling, which is similar to the one reported by Sinton [8], more than one absolute percent of the cell efficiency is obtained for a backside contact solar cell with polysilicon emitters with characteristics shown here ($J_o=2 \times 10^{-14}$ A/cm² for the n-type, $J_o=3.5 \times 10^{-14}$ A/cm² for the p-type, and $\rho_c=1 \times 10^{-5}$ Ω -cm² for both types).

Ex.1005, 249

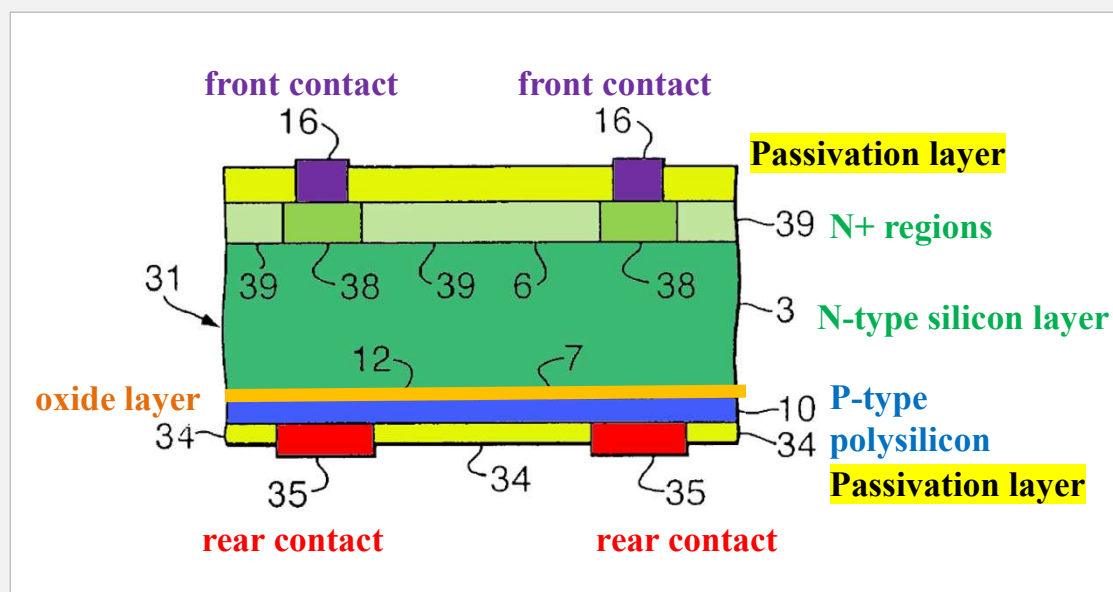


Ex.1005, Fig.6

Ex.1005, 245-246, 249, Figs.4-5; '516 Petition, 19-20; '516 Ex.1003, ¶¶61-64, 78, 81, 86, 106; '053 Petition, 18-19; '053 Ex.1003, ¶¶61-64, 77, 80, 85, 108

POSITA Would Be Motivated to Combine Froitzheim and Gan with a Reasonable Expectation of Success

- ✓ Gan teaches that a polysilicon emitter and oxide layer have improved performance over a diffused emitter
- ✓ Gan teaches that its structure is useful for solar cells with backside PN junctions like Froitzheim
- ✓ Combination improves solar cell efficiency



'516 Petition, 29; '516 Ex.1003-Decl., ¶124; '053 Petition, 26; '053 Ex.1003-Decl., ¶124

Disputed Issues for the Combination of Froitzheim and Gan

Disputes for each IPR:

- 1 Whether Gan Thesis negates the motivation to combine Froitzheim and Gan with a reasonable expectation of success
- 2 Whether polysilicon emitters and oxide layers were known features in semi-conductor technology

Additional disputes for the '053 IPR:

- 1 Whether the *Wands* factors negate the motivation to combine Froitzheim and Gan with a reasonable expectation of success
- 2 Whether Claim 9 is obvious

Experts Agree POSITAs Would Have Been Motivated to Improve Solar Cell Efficiency



Zachary Holman, Ph.D.

Hanwha Expert

76. Since the first modern solar cell was created in 1954 by Bell Laboratories (Ex.1026-Chapin), skilled artisans have worked continuously to improve cell efficiency. When the modern solar cell was initially created, the

'516 Ex.1003, ¶76; '053 Ex.1003, ¶75



Douglas Ruby, Ph.D.

Maxeon Expert

Q. Let me try another one: Is there a goal for improved solar efficiency that you try to reach?

A. **Generally speaking, an improvement of even one-tenth of a percent in efficiency is worthwhile.**

Ex.1075, 69:6-9

'516 Petition, 12; '516 Petitioner's Reply, 5; '516 Ex.1077, ¶23; '053 Petition, 12; '053 Petitioner's Reply, 5; '053 Ex.1077, ¶22

Experts Agree Reducing J_o and ρ_c Improved Solar Cell Efficiency



Zachary Holman, Ph.D.
Hanwha Expert

substrate. Ex.1005-Gan, 245. Gan specifically discusses two metrics: (i) J_o , which is the emitter saturation current density, and (ii) ρ_c , which is the contact resistivity. See Ex.1005-Gan, 249. It was well known that lower J_o indicates less recombination, and lower ρ_c indicates less contact resistance. Lower J_o and ρ_c values therefore provide for a solar cell to have higher efficiency. Ex.1005-Gan, 245; Ex.1043-Kerr, 18-19, 81-84; Ex.1020-Luque, 274-275.

'516 Ex.1003, ¶107; '053 Ex.1003, ¶110



Douglas Ruby, Ph.D.
Maxeon Expert

53. The mean time that free carriers exist before recombination is called the minority carrier lifetime. The distance they can diffuse during this time is called the minority carrier diffusion length. This is sometimes measured as a saturation current density called J_o . The goal of effective solar cell design is to minimize this recombination by maximizing carrier lifetimes and diffusion lengths, thereby keeping J_o low.

'516 Ex.2027, ¶153; '053 Ex.2027, ¶154

64. A high ρ_c results in excessive loss of power and lower efficiency.

Total series resistance for one-sun cells such as described in the '516 patent typically needs to be less than 1 ohm-cm². Back contact resistance typically makes up about 1% of this, so it should be less than 1x10⁻² ohm-cm². This is only one component of total series resistance, and all need to be optimized simultaneously along with allowing maximum light collection at the front surface to maximize cell efficiency. This involves several tradeoffs and careful optimization.

'516 Ex.2027, ¶164; '053 Ex.2027, ¶165

'516 Petition, 20; '516 Petitioner's Reply, 5-6; '516 Ex.1077, ¶23; '053 Petition, 19; '053 Petitioner's Reply, 5; '053 Ex.1077, ¶22

Experts Agree POSITAs Would Have Known How to Implement Oxide Layers



Zachary Holman, Ph.D.

Hanwha Expert

136. A person of ordinary skill in the art would have known how to add oxide layers to silicon surfaces, as doing so was well-known and routine by 2008. *E.g.*, Ex.1005-Gan, 246; Ex.1006-Borden-575, [0026]; Ex.1004-Froitzheim, [0030]; Ex.1015-Swanson, 1:50-2:61; *see also* Section VII.B (Overview of Solar Cell Efficiency). A person of ordinary skill in the art would have also readily understood

'516 Ex.1003, ¶136; '053 Ex.1003, ¶136



Douglas Ruby, Ph.D.

Maxeon Expert

- Q. By 2008, a person of ordinary skill in the art of the '516 and '053 patents would have known how to add a tunnel oxide to a transistor, correct?
- A. Yes.
- Q. And by 2008, a person of ordinary skill in the art of the '516 and '053 patents would have known how to add a tunnel oxide to a solar cell, correct?
- A. I presume so, yes.

Ex. 1075, 107:12-19

'516 Petition, 34-35; '516 Petitioner's Reply, 5; '516 Ex.1077, ¶32; '053 Petition, 32; '053 Petitioner's Reply, 5; '053 Ex.1077, ¶31

Experts Agree POSITAs Would Have Known the Benefits of Polysilicon Emitters and Oxide Layers



Douglas Ruby, Ph.D.

Maxeon Expert

Q. Of course. By 2008, it was known that the combination of a tunnel oxide and doped polycrystalline silicon layer provides excellent passivation and carrier selectivity on the N-type substrate, correct?

A. It was not widely known.

Q. But it was known, correct?

A. It was known by some.

Q. In fact, Gan teaches that, right?

A. That's what he was working to prove.

Ex.1075, 109:1-9; '516 Petitioner's Reply, 11-12; '516 Ex.1077, ¶34; '053 Petitioner's Reply, 10-12; '053 Ex.1077, ¶32

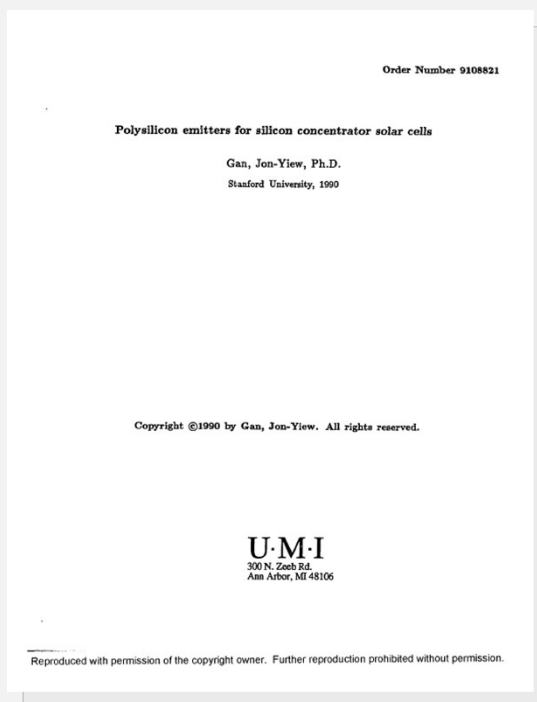
The Board Correctly Rejected Maxeon's Gan Thesis Argument to Apply a Heighted Obviousness Standard

Patent Owner's additional arguments that Petitioner's contentions are expressly contradicted by the Gan Thesis, at this time, are similarly unpersuasive.¹⁶ Prelim. Resp. 18. Patent Owner's arguments that "the breakup process is still *difficult to control*" and "*reproducibility problems*" exist (*id.*) appears to advocate for a heightened standard for success. However, under the proper inquiry, "obviousness cannot be avoided by a showing of some degree of unpredictability in the art so long as there was a reasonable probability of success." *Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1364 (Fed. Cir. 2007). Furthermore, though the Gan Thesis acknowledges inconsistent oxide growth during "ramp-up" and "stand-by" periods, the Gan Thesis also explains that "it is possible that the thin-oxide growth can be improved by performing the oxidation at lower temperatures such that the oxidation rate can be controlled more precisely." Ex. 1005, 112. Finally, Patent Owner's argument relies on the Gan Thesis, *not* Gan itself. Prelim. Resp. 18–19 (citing Ex. 2003).

'516 Institution Decision, 34;
'053 Institution Decision, 34;
'516 Petitioner's Reply, 7;
'053 Petitioner's Reply, 6-7

Gan Thesis Corroborates the Froitzheim and Gan Combination

Gan studies a polysilicon emitter and oxide layer



'516 Petitioner's Reply, 7-11; '053 Petitioner's Reply, 7-10

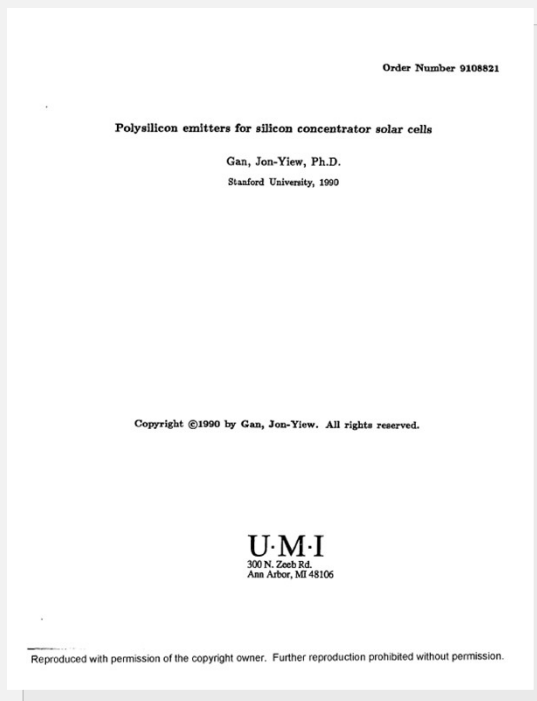
minimum level. Above all, obtaining small broken areal fraction of the interfacial oxide seems to be a very promising method for making polysilicon emitters of both types useful for concentrator solar cells, and is the approach of this work.

To carry out the task, the cell modeling is given in the next chapter. This serves two purposes in this work. First, it gives an idea how the cell performance is related to the emitter and its design. Second, The requirements for a good emitter substitute can also be sought from the simulation. Chapter 3 starts a thorough review of the work done on the polysilicon emitter. In particular, the review will point out all the problems of the polysilicon emitter for use in silicon concentrator solar cells. Chapter 4 is dedicated to the derivations of carrier transport mechanisms for the polysilicon SIS emitters. In particular, it shows that, under certain conditions, a polysilicon SIS emitter with low J_o and ρ_c can be obtained by breaking a very small fraction of interfacial oxide. Chapter 5 is the demonstration of the experimental results. The results shown in this chapter are very much like what are predicted in Chapter 4. In practice, there are some technical problems in controlling the oxide breakup process. They are discussed in Chapter 6 for the polysilicon emitter with low J_o and ρ_c . In the final chapter, a summary of contributions of this study and suggestions for future work are given.

Ex.2003, 10

Gan Thesis Teaches Solutions for Improved Manufacturing Techniques

Gan Thesis explains an improved furnace would improve reliability



It appears that the oxide breakup depends critically on the interfacial oxide thickness. The thin-oxide growth recipe used in this work was not reliable; the oxide thicknesses between 15 to 20 Å have been found with the same growth condition. As a result, this contributes to the fluctuation of the ρ_c results. It is then clear that a more reliable way of growing the thin oxide is needed.

Ex.2003, 119

From the above, it appears that the variation of the oxide thickness results mainly from the oxide-growth step. If this is the case, it is possible that the thin-oxide growth can be improved by performing the oxidation at lower temperature such that the oxidation rate can be controlled more precisely.

Ex.2003, 112

'516 Petitioner's Reply, 9-11; '516 Ex.1077, ¶¶30-31; '053 Petitioner's Reply, 9-10; '053 Ex.1077, ¶¶29-30

Experts Agree Oxide Layers Were Known in Transistors



Zachary Holman, Ph.D.

Hanwha Expert

138. Finally, a person of ordinary skill in the art would have been aware of the plethora of teachings explaining the use and benefits of polysilicon emitters, including with interfacial oxide layers and including for solar cells and transistors.

Section VII.B (Overview of Solar Cell Efficiency). For example, Foglietti disclosed

'516 Ex.1003, ¶138; '053 Ex.1003, ¶138



Douglas Ruby, Ph.D.

Maxeon Expert

80. The tunneling mechanism is described in U.S. Patent Pub. No. 2002/0142500 to Foglietti. Ex. 1042. Although Foglietti relates to bipolar transistors, the tunneling mechanism it describes also applies to solar cells.

81. According to Foglietti, interfacial oxides (tunnel oxides) are “generally less restrictive with respect to majority carriers (electrons) moving from the emitter region of the transistor into the base region than minority carriers (holes) moving from the base region into the emitter region. This phenomenon is

'516 Ex.2027, ¶¶80-81; '053 Ex.2027, ¶¶81-82

'516 Petition, 35-36;

'053 Petition, 33;

'516 Petitioner's Reply, 12;

'053 Petitioner's Reply, 11

Experts Agree Transistor Technology Is Applicable to Solar Cells



Douglas Ruby, Ph.D.
Maxeon Expert

Q. Do principles applicable generally to semiconductors often apply to solar cells?

A. Yes.

Q. Can you explain why?

A. **As I said, solar cells are made using semiconductors, so the principles of semiconductor physics which apply to all semiconductor devices apply to solar cells.**

Q. Is a transistor a semiconductor device?

A. Yes.

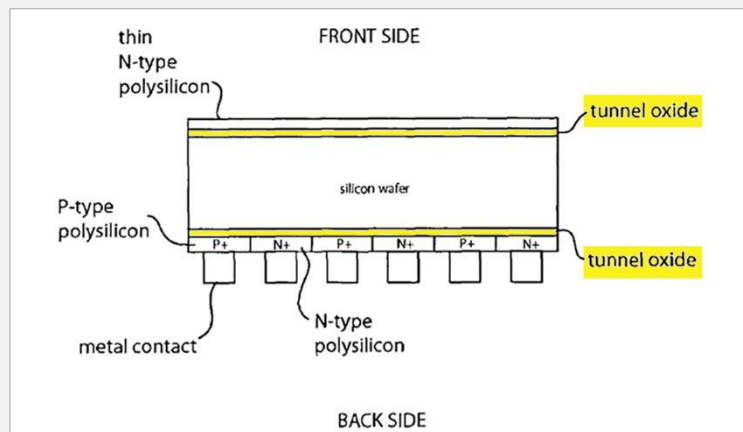
Ex.1075, 27:13-22; '516 Ex.1077, ¶27; '516 Petitioner's Reply, 8; '053 Ex.1077, ¶26; '053 Petitioner's Reply, 7-8

Polysilicon Emitters and Tunnel Oxide Layers Were Known Features In Semiconductor Technology

U.S. Patent No. 7,468,485 to Swanson (Ex.1015)

(54) BACK SIDE CONTACT SOLAR CELL WITH DOPED POLYSILICON REGIONS

the p-type and n-type regions therein. A tunnel oxide layer may be formed on the back side of the wafer directly between the wafer and the back side polysilicon layer. The tunnel



Ex.1015, Title, 2:41-43; Fig.1



Douglas Ruby, Ph.D.

Q. Q. And Gan teaches an oxide layer formed between the back surface of the substrate and the emitter layer, correct?

A. Yes.

Ex.1075, 180:20-181:1

'516 Petition, 34-36; '516 Petitioner's Reply, 11-14; '516 Ex.1077, ¶35; '053 Petition, 31-33; '053 Petitioner's Reply, 10-14; '053 Ex.1077, ¶33;

Maxeon Advances Legally Incorrect Arguments

Maxeon conflates anticipation with obviousness



“The question in an obviousness inquiry is whether it would have been obvious to a person of ordinary skill in the art to combine the relevant disclosures of the two references, not whether each individual reference discloses all of the necessary elements.”

Game & Tech. Co. v. Wargaming Grp. Ltd., 942 F.3d 1343, 1352 (Fed. Cir. 2019) (citation omitted)

Commercial availability is not required to demonstrate obviousness



“Nothing in the statute or our case law requires [the Patent Challenger] to prove obviousness by starting with a prior art commercial embodiment and then providing motivation to alter that commercial embodiment.”

Galderma Lab'ys, L.P. v. Tolmar, Inc., 737 F.3d 731, 737 (Fed. Cir. 2013) (citation omitted)

“[N]o requirement that the closest prior art be commercialized.”

Trs. of Columbia Univ. v. Illumina, Inc., 620 F. App'x 916, 932 (Fed. Cir. 2015) (citation omitted)

'516 Petitioner's Reply, 13-14; '053 Petitioner's Reply, 12-14

Dr. Ruby Applied the Incorrect Standard for Reasonable Expectation of Success



Douglas Ruby, Ph.D.
Maxeon Expert

- A. Well, I know what reasonable expectation of success means in plain English.
- Q. What is your understanding of the plain English meaning of “reasonable expectation of success”?
- A. It means that the probability of success is close to 100 percent.
- Q. Do you have an understanding of the legal standard required to demonstrate reasonable expectation of success?
- A. Yeah I’m not that familiar with legal standards.

Ex.1075, 165:17-166:8; '516 Petitioner's Reply, 3; '053 Petitioner's Reply, 3

Maxeon's *Wands* Factors Argument Is Legally Flawed ('053 IPR)

The *Wands* factors concern enablement, NOT obviousness



“We, therefore, turn to Petitioner’s evidence and arguments that [prior art reference] is enabled” and considering parties’ arguments regarding the *Wands* factors.

Packers Plus Energy Servs. Inc., v. Baker Hughes Oilfield Ops. LLC, IPR2016-01003, Paper 33, 23-30 (Nov. 6, 2017)



“The applications in this case satisfy the enablement requirement only if one skilled in the art, after reading their disclosures, could practice the invention Claimed in the '561 patent without undue experimentation.”

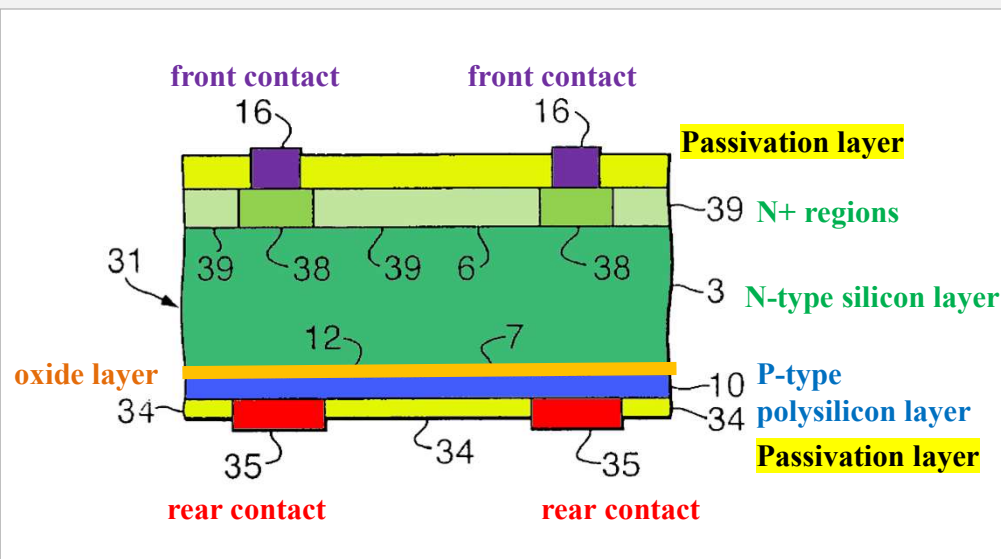
Chiron Corp. v. Genentech, Inc., 363 F.3d 1247, 1253 (Fed. Cir. 2004)

'053 Petitioner's Reply, 14

The Petition Demonstrates That Claim 9 Is Obvious ('053 IPR)

Froitzheim and Gan teach the manufacturing method of Claim 9, which does not recite an oxide layer

9. A method of fabricating a solar cell comprising:
forming a layer of polysilicon over a back surface of a silicon substrate;
forming a first dopant source layer over the layer of polysilicon;
diffusing dopants from the first dopant source layer to the layer of polysilicon to form a backside junction with the silicon substrate;
diffusing dopants into a front surface of the silicon substrate, the front surface of the silicon substrate facing the sun during normal operation; and
forming a metal contact on the front surface of the silicon substrate, wherein the metal contact is electrically coupled to the silicon substrate.



'053 Ex.1001 ('053 Patent), claim 9; '053 Petitioner's Reply, 16-18

Dr. Holman's Deposition Testimony Regarding Claim 9 Was Accurate and Comprehensive



Zachary Holman, Ph.D.

Hanwha Expert

Q. So in Paragraph 148 when you talk about the combination of Froitzheim and Gan, do you envision a combination that includes Gan's oxide layer?

* * *

A. A combination that includes Gan's oxide layer would also meet the limitation of the Claim, as would one in which it was not omitted. Because in both cases the combined teachings of Froitzheim and Gan including forming a layer of polysilicon over a back surface of a silicon substrate.

Q. Are you saying in this paragraph when you talk about the combination of Froitzheim and Gan you mean — you could mean a combination that does not include Gan's oxide layer?

* * *

A. This Claim, which is directed towards a method of manufacture of the structure, is about forming a layer of polysilicon over a back surface of a silicon substrate. And as I describe here, **Gan teaches forming a layer over a polysilicon over a back surface of a silicon substrate, and the combination of Gan and Froitzheim teaches that. Gan also then teaches Apex — teaches an oxide layer. That oxide layer is not required to meet this Claim limitation.**

Ex.2029, 187:13-188:17; '053 Petitioner's Reply, 17-18; '053 Ex.1077, ¶¶37-38

Maxeon Incorrectly Quotes Petitioner's Reply

Maxeon incorrectly attributes a quote from Canadian Solar Inc. to Hanwha

cell). To that end, Petitioner's mere suggestion that "a POSITA would have readily reconciled the teachings of Gan and Froitzheim regarding processing temperatures," Reply, 4, or other missing components or variables for that matter, is not sufficient to show an expectation of success. *Grunenthal GMBH v. Alkem*

MAXEON SOLAR PTE. LTD.,
Patent Owner

Case IPR2024-01199
U.S. Patent No. 8,878,053

PATENT OWNER SUR-REPLY

'053 Sur-Reply, 7; '516 Sur-Reply, 5-6

lower temperature of Gan.¹ POR at 47. Thus, a POSITA would have readily reconciled the teachings of Gan and Froitzheim regarding processing temperatures by selecting the lower end of the Froitzheim range. *Id.*, ¶11.

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

CANADIAN SOLAR INC.,
Petitioner,

v.

MAXEON SOLAR PTE. LTD.
Patent Owner

Inter Partes Review No. IPR2024-01040
Patent No. 8,878,053

PETITIONER'S REPLY TO PATENT OWNER RESPONSE

Canadian Solar's '053 Reply, 4; Canadian Solar's '516 Reply, 3-4

Froitzheim, Gan, and Smith IPR2024-01199 – Ground II

Smith Ground Addresses Routine Manufacturing Steps Recited in Challenged Claims

9. A method of fabricating a solar cell comprising:
forming a layer of polysilicon over a back surface of a silicon substrate;
forming a first dopant source layer over the layer of polysilicon;
diffusing dopants from the first dopant source layer to the layer of polysilicon to form a backside junction with the silicon substrate;
diffusing dopants into a front surface of the silicon substrate, the front surface of the silicon substrate facing the sun during normal operation; and
forming a metal contact on the front surface of the silicon substrate, wherein the metal contact is electrically coupled to the silicon substrate.

12. The method of claim 9 wherein diffusing dopants into the front surface of the silicon substrate comprises forming a second dopant source layer over the silicon substrate and diffusing dopants from the second dopant source layer into the silicon substrate.

13. The method of claim 12 wherein the second dopant source layer comprises phosphorus doped silicon dioxide.

15. The method of claim 9 wherein the diffusion of dopants from the first dopant source layer to the layer of polysilicon and the diffusion of dopants into the front surface of the silicon substrate are performed in situ.

'053 Ex.1001 ('053 Patent), claims 9, 12, 13, 15; '053 Petition, 50-51; '053 Ex.1003, ¶197

Undisputed That Smith Teaches Manufacturing Techniques for Solar Cells

1. Field of the Invention

The present invention relates generally to solar cells, and more particularly but not exclusively to methods and apparatus for fabricating solar cells.

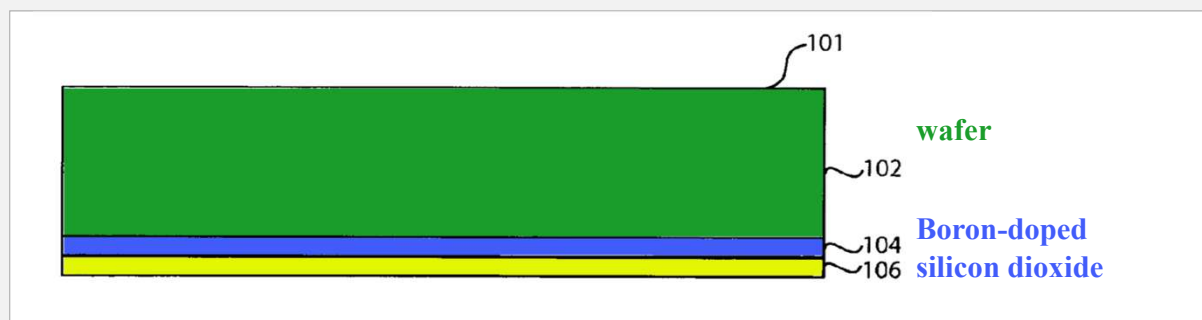
In FIG. 2, a boron-doped silicon dioxide (SiO_2) (“BSG”) **104** is deposited on the back side of wafer **102**. In one embodiment, boron-doped silicon dioxide **104** is deposited to a thickness of about 1000 Angstroms using an atmospheric pressure chemical vapor deposition process (APCVD). The thickness of boron-doped silicon dioxide

17. A method of fabricating a solar cell, the method comprising:

diffusing a first dopant from a first doped oxide layer into a back side of a substrate to form a first doped region of a solar cell in the substrate;

diffusing a second dopant into the substrate from a front side of the substrate;

wherein the diffusion of the first dopant and the second dopant are performed in one loading of the substrate into a processing tool.

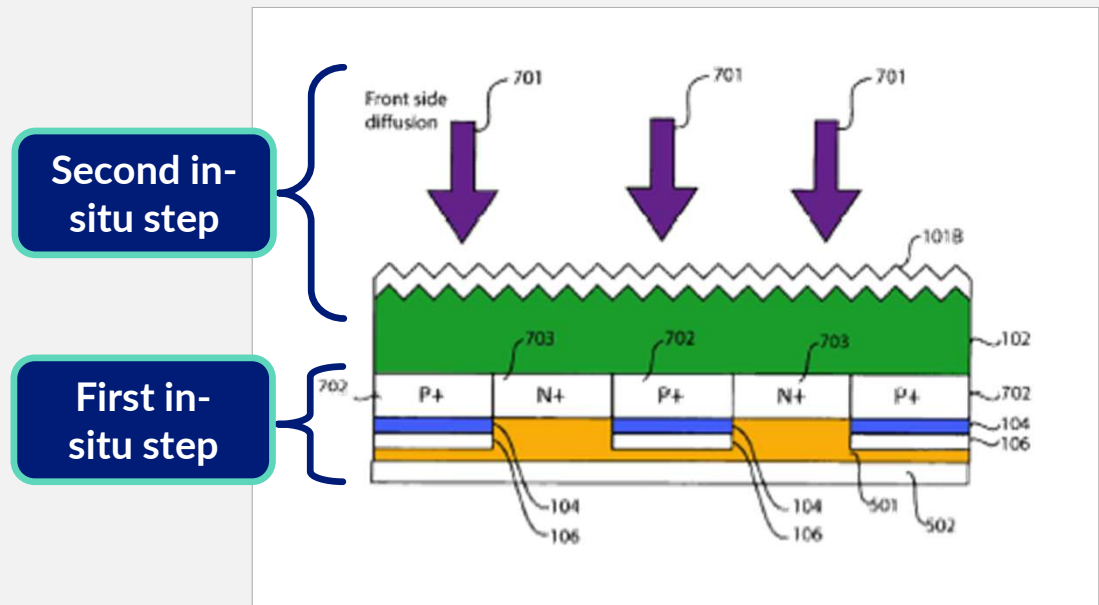


Ex.1007, 1:16-20, 2:44-49, Claim 17; '053 Petition, 20-22; '053 Ex.1003, ¶¶113-116

Undisputed That Smith Teaches In-Situ Diffusion

In FIG. 7, the sample of FIG. 6 is subjected to in-situ steps. The steps are in-situ in that they are performed in one loading of wafer 102 into the wafer processing tool. In one embodiment, the in-situ steps are performed in a furnace. In the first in-situ step, wafer 102 is heated to about 1000° C. for one hour to diffuse dopants from boron-doped silicon dioxide 104 and phosphorus-doped silicon dioxide 501 into wafer 102. This results in the formation of P+ regions 702 (due to boron-doped silicon dioxide 104) and N+ regions 703 (due to phosphorus-doped silicon dioxide 501) in wafer 102. Note that during the first in-situ step, undoped silicon

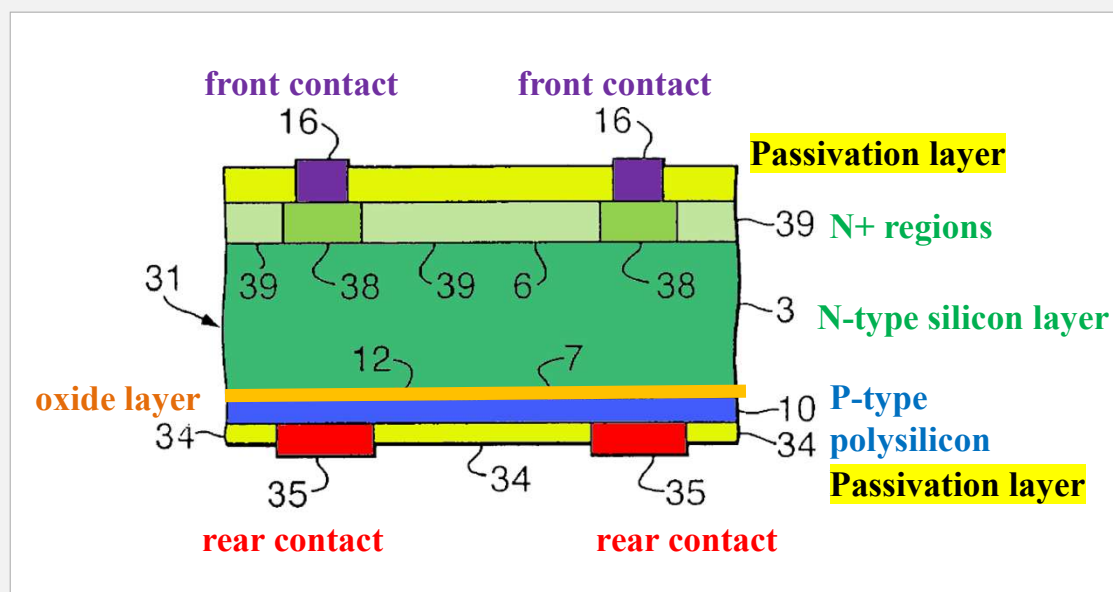
In the second in-situ step, the furnace conditions are changed to about 750° C. with an atmosphere containing phosphorus oxychloride, then to about 975° C. with an atmosphere containing oxygen to diffuse phosphorus as an N-type dopant into wafer 102 from its front side, and to grow a thin layer of silicon dioxide on both sides of wafer 102. Front side 101 is now labeled as "101B" to indicate that there is a thin layer of silicon dioxide on its surface. The thin layer of silicon dioxide advantageously leads to better passivation of the front side and back side surfaces of wafer 102. In FIG. 7, the front side diffusion of N-type dopants into wafer 102 is schematically represented by arrows 701. As



Ex.1007, 3:40-67, Fig.7;
'053 Petition, 20-22, 64-67; '053 Ex.1003, ¶¶113-116, 239-247;
'053 Petitioner's Reply, 18; '053 Ex.1077, ¶39

POSITA Would Be Motivated to Combine Froitzheim, Gan, and Smith with a Reasonable Expectation of Success

- ✓ Smith teaches reducing the number of steps for solar cell manufacturing
- ✓ Smith's deposition techniques would ensure that dopants would be introduced in the correct layers
- ✓ Smith's deposition techniques were compatible with Froitzheim and Gan



'053 Petition, 51-56; '053 Ex.1003, ¶¶198-213

Experts Agree APCVD Deposition and In-Situ Diffusion Were Known



Douglas Ruby, Ph.D.

Maxeon Expert

Q. Would you agree that by 2009, a person of ordinary skill in the art of the '516 and '053 Patents would have known how to perform APCVD?

A. Yes.

* * *

Q. During your time at Sandia did you ever work on solar cells made with an in-situ diffusion process?

A. **That's the one I just mentioned.**

Q. What is an in-situ diffusion process?

A. **It would be a process where you do, you can conduct multiple operations without removing the wafers from the furnace.**

Ex.1075, 49:11-17, 159:17-20; '053 Petitioner's Reply, 19, 22, 24; '053 Ex.1077, ¶¶42, 45, 51

Experts Agree That Decreasing Manufacturing Costs Was Desirable



Douglas Ruby, Ph.D.

Maxeon Expert

Q. Did you ever face a trade-off between solar cell efficiency on the one hand that reduced cost on the other?

A. I would say we always geared our designs for both increased efficiency and reduced cost.

* * *

Q. And your patent explains, “The most obvious is that the fewer discrete operations required, the lower will be the cost of final product.”

A. Yes.

Q. And this explains it was obvious that if you decrease the number of discrete operations, the cost of the solar cell would be lower, right?

A. Right.

Ex.1075, 32:6-9, 146:16-147:1; '053 Petitioner's Reply, 21, 23-24; '053 Ex.1077, ¶¶45-46, 51-52

Experts Agree In-Situ Diffusion Was Desirable



Douglas Ruby, Ph.D.
Maxeon Expert

- Q. The furnace steps will be, “The steps performed in one loading of the wafer into the furnace,” right?
- A. Yes.
- Q. The steps will be performed using a single loading of the substrate in a furnace, right?
- A. Yes.
- Q. And the patent explains that this is a simplification that greatly reduces both processing time and the set-up cost for the processing line?
- A. Yes.

Ex.1075, 148:2-11; '053 Petitioner's Reply, 23-24; '053 Ex.1077, ¶¶50-52

Disputed Issues for the Combination of Froitzheim, Gan, and Smith

- 1 Whether Smith's teachings are limited to "back contact" solar cells
- 2 Whether a POSITA would have applied Smith's in-situ teachings to the combination of Froitzheim and Gan

Smith's Teachings Are Not Limited to Back Contact Cells

Smith's teachings relate to solar cells generally and recite Claims that are not limited to back contact cells

1. Field of the Invention

The present invention relates generally to solar cells, and more particularly but not exclusively to methods and apparatus for fabricating solar cells.

9. A method of fabricating a solar cell, the method comprising:

- providing a substrate having a front side and a back side, the front side of the substrate being configured to receive solar radiation for a solar cell;
- forming a first doped oxide layer on the back side of the substrate;
- diffusing a first dopant from the first doped oxide layer into the substrate to form a first doped region of the solar cell; and
- diffusing a second dopant into the substrate from the front side of the substrate in-situ with the diffusion of the first dopant from the first doped oxide layer.

17. A method of fabricating a solar cell, the method comprising:

- diffusing a first dopant from a first doped oxide layer into a back side of a substrate to form a first doped region of a solar cell in the substrate;
- diffusing a second dopant into the substrate from a front side of the substrate;
- wherein the diffusion of the first dopant and the second dopant are performed in one loading of the substrate into a processing tool.

Ex.1007, 1:16-19, claims 9, 17; '053 Petitioner's Reply, 19-20; '053 Ex.1077, ¶¶43-44

Dr. Ruby Agrees That APCVD Is Not Limited to Back Contact Solar Cells

Dr. Ruby published an article in 1993 that used APCVD on a solar cell with front and rear contacts



Douglas Ruby, Ph.D.

Maxeon Expert

Q. You were using APCVD to deposit an oxide on the front surface of the wafer?

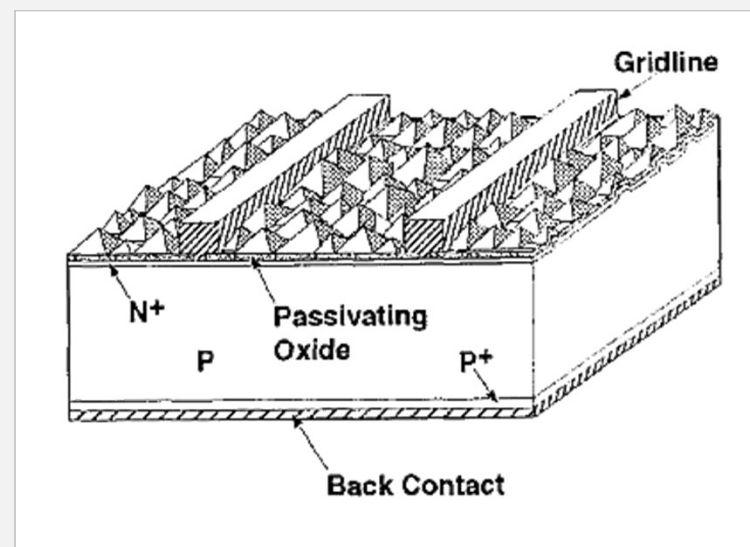
A. Yes.

* * *

Q. And you were using APCVD to deposit an oxide on the rear surface of the wafer, correct?

A. Yes, that's right.

Ex.1075, 158:18-20, 159:3-5



Ex.1074, 173

'053 Petitioner's Reply, 19-20; '053 Ex.1077, ¶44

Maxeon's Interpretation of Smith Is Legally Flawed



“A reference must be considered for everything that it teaches, not simply the described invention or a preferred embodiment.”

CRFD Rsch., Inc. v. Matal, 876 F.3d 1330, 1349 (Fed. Cir. 2017)
(quoting *In re Applied Materials, Inc.*, 692 F.3d 1289, 1299 (Fed. Cir. 2012))



“[A] reference must be considered for everything it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect.”

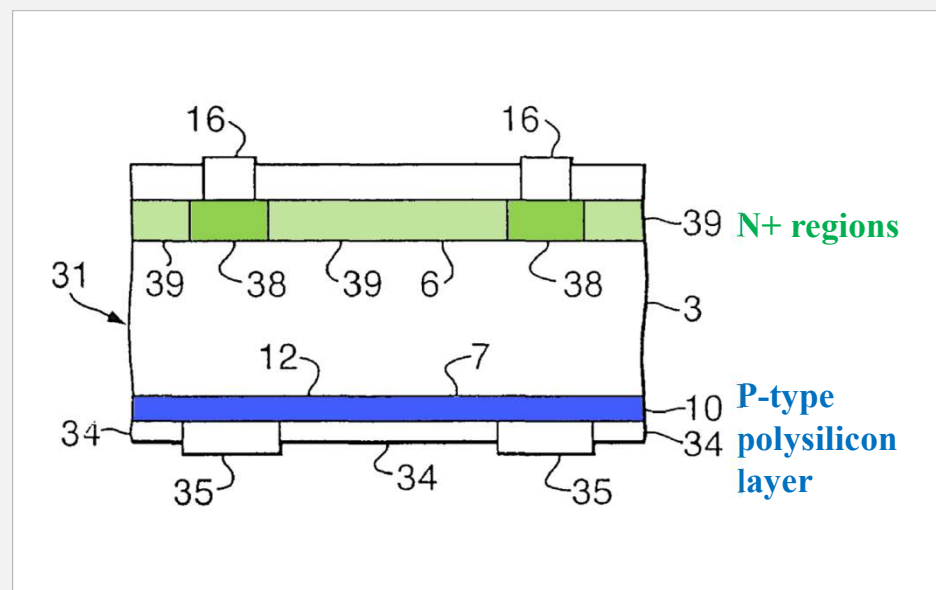
Belden Inc. v. Berk-Tek LLC, 805 F.3d 1064, 1076 (Fed. Cir. 2015)
(quoting *EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985))

'053 Petitioner's Reply, 20

A POSITA Would Have Been Motivated to Apply Smith's In-situ Teachings to the Combination of Froitzheim and Gan

A POSITA also would have been motivated to apply Smith's "in-situ steps" to the combination of Froitzheim and Gan to drive in the dopants to their target regions, which "simplifies the fabrication process." Ex.1007-Smith, 3:40-4:2. Smith explains that in-situ diffusion means that the steps are "performed in one loading of [the] wafer [] into the wafer processing tool." *Id.*, 3:40-42. A POSITA would have found this advantageous because it would simplify the process and decrease costs. Ex.1003-Decl., ¶209.

A POSITA would have understood that Smith's APCVD, diffusion barrier, and in-situ diffusion processes applied to Froitzheim's and Gan's methods would have been desirable because the front side and the back side of the wafers could be doped at the same time, decreasing cost and the number of required steps.



'053 Petition, 55; '053 Ex.1003, ¶¶209-210;
'053 Petitioner's Reply, 23; '053 Ex.1077, ¶¶49-50

Petition Established Claims 2-3, 5, 11-12, and 14 Are Obvious in View of the Froitzheim, Gan, and Smith Combination

Petition incorporated its Ground I Froitzheim disclosure and explained that Smith also teaches these limitations

12. The method of claim 9 wherein diffusing dopants into the front surface of the silicon substrate comprises forming a second dopant source layer over the silicon substrate and diffusing dopants from the second dopant source layer into the silicon substrate.

'053 Ex.1001 ('053 Patent), claim 12

5. Claim 12

Claim 12 depends from claim 9. Petitioner incorporates Section X.B.2. As discussed in Section X.A.5, Froitzheim teaches these elements. Ex.1003-Decl., ¶231.

Smith also teaches these elements. See Section X.B.2.d. Smith's Figure 7

Ex.1007-Smith, Fig.7. As discussed in Section X.B.1, a POSITA would have been motivated to modify the combination of Froitzheim and Gan to implement Smith's diffusion methods with a reasonable expectation of success. Ex.1003-Decl., ¶¶232-234.

'053 Petition, 61-62

'053 Petition, 60-64, 71-72; '053 Ex.1003, ¶¶229-234, 236-238, 270-271, 273; '053 Petitioner's Reply, 25-27; '053 Ex.1077, ¶¶53-56

Petition Established Claims 4 and 13 Are Obvious in View of the Froitzheim, Gan, and Smith Combination

Petition established a POSITA would have been motivated to apply Smith's diffusion techniques, which included a dopant source layer of phosphorous doped silicon dioxide

4. The method of claim 3 wherein the N-type dopant source comprises phosphorus doped silicon dioxide.

13. The method of claim 12 wherein the second dopant source layer comprises phosphorus doped silicon dioxide.

'053 Ex.1001 ('053 Patent), claims 4 and 13

6. Claim 13

Claim 13 depends from claim 12. Petitioner incorporates Section X.B.5. The combination of Froitzheim, Gan, and Smith teaches this element. As discussed in Section X.B.5, Smith teaches forming a layer of glass with phosphorous dopants (i.e., *phosphorus doped silicon dioxide*) as part of the POCl₃ diffusion. Ex.1003-Decl., ¶235.

'053 Petition, 62

'053 Petition, 62, 71; '053 Ex.1003, ¶¶235, 272; '053 Petitioner's Reply, 25-27; '053 Ex.1077, ¶¶53-56

Petition Established Claims 5 and 14 Are Obvious in View of the Froitzheim, Gan, and Smith Combination

Petition incorporated its Ground I Froitzheim disclosure and explained that Smith also teaches these limitations

5. The method of claim 1 further comprising:
texturing the front surface of the N-type silicon substrate;
and
forming an antireflective layer over the textured front surface of the N-type silicon substrate.

14. The method of claim 9 further comprising:
texturing the front surface of the silicon substrate; and
forming an antireflective layer over the textured front surface of the silicon substrate.

'053 Ex.1001 ('053 Patent), claims 5 and 14

7. Claim 14

Claim 14 depends from claim 9. Petitioner incorporates Section X.B.2. As discussed in Section X.A.6, Froitzheim teaches this element. Ex.1003-Decl., ¶236. Smith also teaches claim 14. Smith Figure 6 depicts texturing the front side “using a wet etch process.” Ex.1007-Smith, 3:32-38, 2:60-62. The textured surface

Ex.1007-Smith, Fig.7. As discussed in Section X.B.1, a POSITA would have been motivated to modify Froitzheim to implement Smith’s manufacturing methods with a reasonable expectation of success, including texturing and anti-reflective coating (which were common features). Ex.1003-Decl., ¶¶237-238.

'053 Petition, 63-64

'053 Petition, 63-64, 72; '053 Ex.1003, ¶¶236-238, 273; '053 Petitioner’s Reply, 25-27; '053 Ex.1077, ¶¶53-56

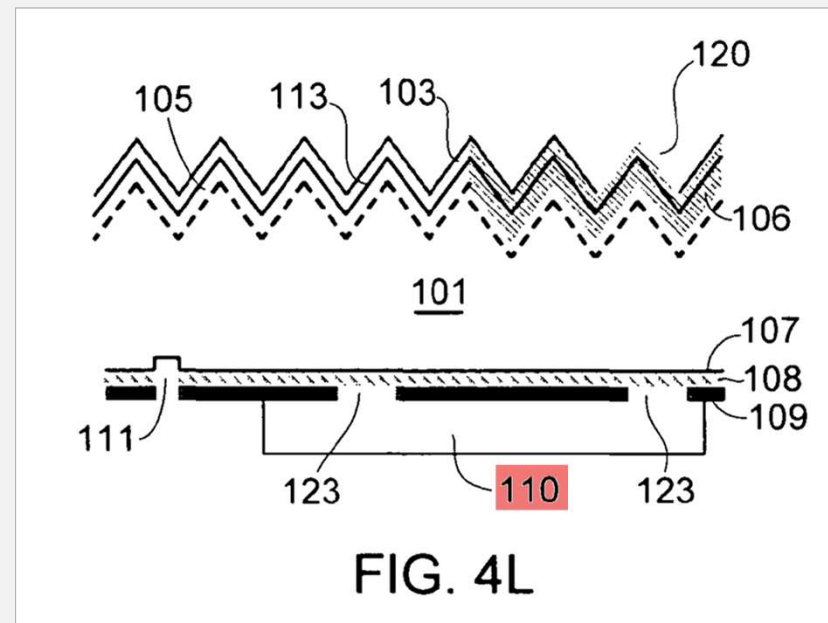
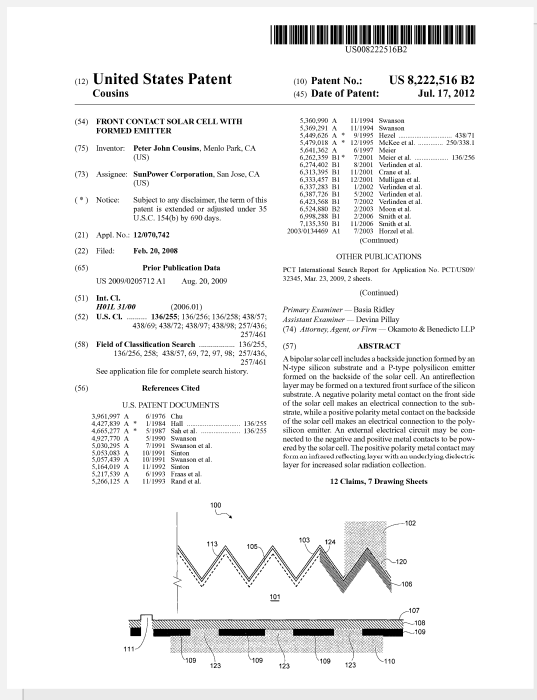
**Froitzheim and Gan
'516 Patent Claim 12
IPR2024-01203 – Grounds I, III**

Disputed Issues for Claim 12

- 1 Whether Froitzheim discloses “wherein the second metal contact comprises silver formed over a layer of silicon dioxide”

Claim 12 is not limited to the specific configurations depicted in the '516 patent

12. The solar cell of claim 9 wherein the second metal contact comprises silver formed over a layer of silicon dioxide.



'516 Ex.1001 ('516 Patent), claim 12, Fig.4L; '516 Petitioner's Reply, 15-16; '516 Ex.1077, ¶¶37-40

Claim 12 Is Taught by Froitzheim

Froitzheim and the '516 patent each teach screen printed metal contacts

'516 Patent

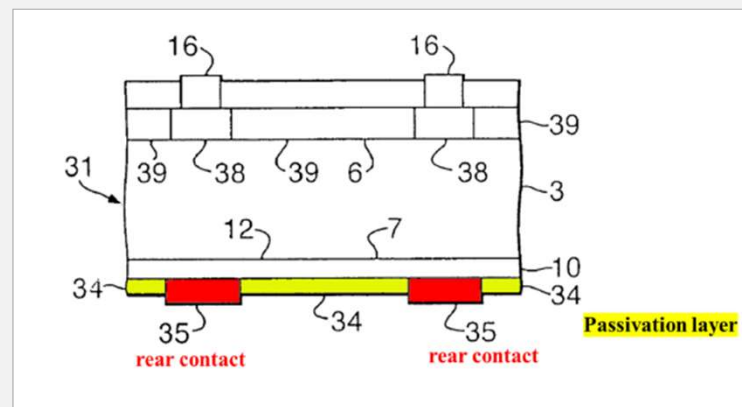
12. The solar cell of claim 9 wherein the second metal contact comprises silver formed over a layer of silicon dioxide.

'516 Ex.1001 ('516 Patent), Claim 12

electrical connection to the polysilicon emitter 108. The metal contact 110 may be formed using a printing process.

'516 Ex.1001 ('516 Patent), 5:50-51

Froitzheim



[0048] Front and rear side contacts are preferably screen-printed in an industrial production process, and contacting is done at elevated temperatures.

Ex.1004, [0048], Fig.1

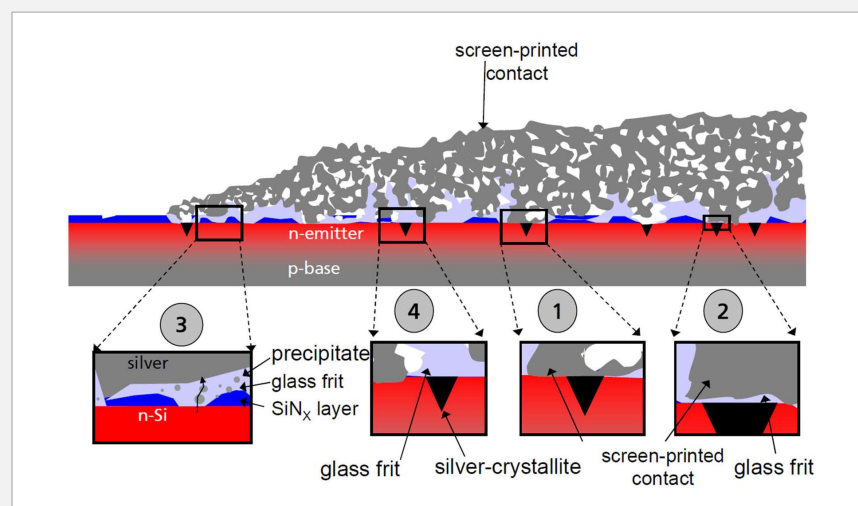
'516 Petition, 50-51; '516 Petitioner's Reply, 15-16; '516 Ex.1003 ¶¶165, 176, 182-184; '516 Ex.1077, ¶¶37-40

Froitzheim Teaches Claim 12 Even if It Requires a Specific Structural Relationship

Dr. Holman testified that the silicon dioxide layer is not completely removed during screen printing as alleged by Maxeon

41. **Second**, the analysis in Dr. Ruby's declaration mischaracterizes Froitzheim's disclosure of screen printing rear metal contacts. Ex.2027-Ruby-Decl., ¶¶185-187. Froitzheim's Figure 3 is a drawing in a patent document that is not drawn to scale. Contrary to Dr. Ruby's assertion, a POSITA would have understood that the metal paste that forms Froitzheim's rear contacts would not completely "fire through" the silicon dioxide layer. Instead, only a portion of the metal paste would "fire through" the silicon dioxide layer to create an electrical connection with the emitter, with most of the metal paste remaining over the silicon dioxide layer on which it was first applied.

'516 Ex.1077, ¶41



Ex.1081, Fig.14

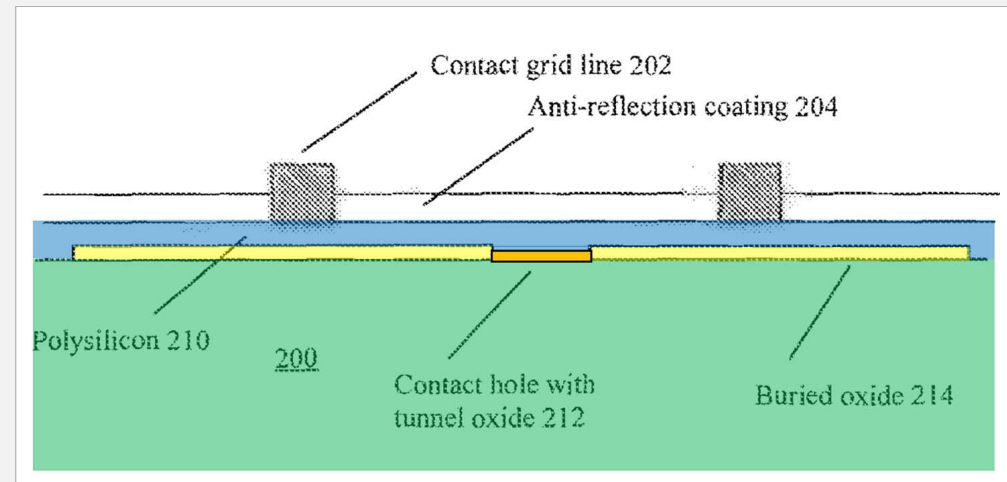
Ex.2029, 84:13-85:16; '516 Petitioner's Reply, 16-17; '516 Ex.1077, ¶¶41-43

Froitzheim and Borden-575 IPR2024-01203, Ground III

Borden-575's Undisputed Polysilicon Emitter and Oxide Layer

1050°C for 30 seconds after deposition activates the dopants. As mentioned above, in some embodiments a thin tunnel oxide may be included between the substrate 200 and the polysilicon 210 in the contact holes 212. This oxide – typically 8 to 15Å thick – provides passivation between the substrate and the polysilicon, while allowing for tunnel current flow.

Ex.1006, [0022]

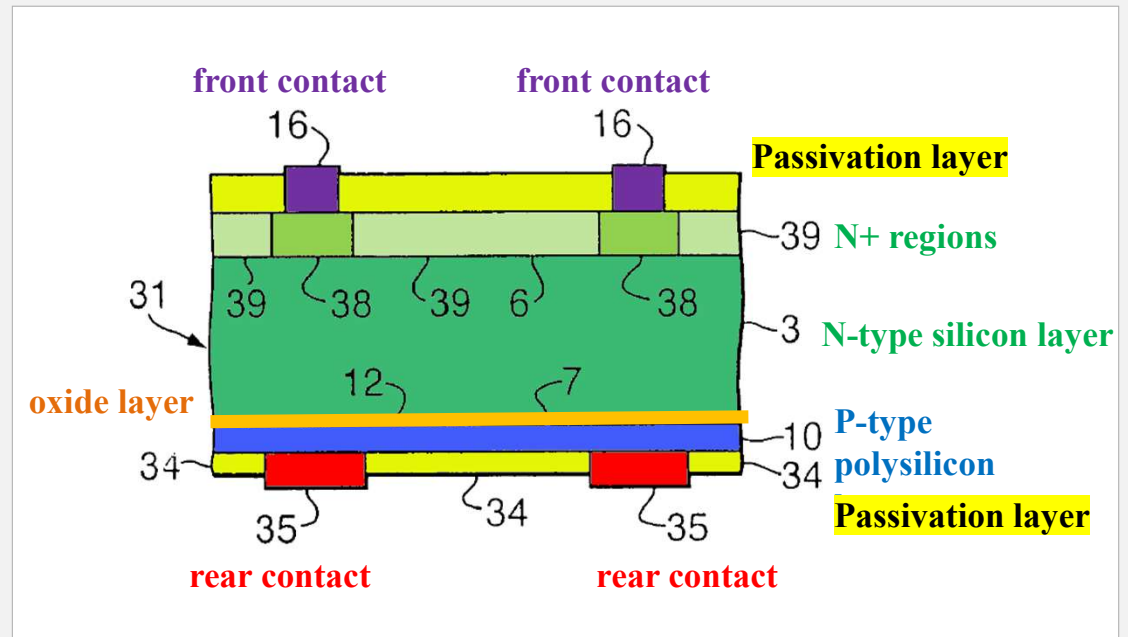


Ex.1006, Fig.2

Ex.1006, [0022], Fig.2; '516 Petition, 25; '516 Ex.1003, ¶¶113-114

Froitzheim's and Borden-575's Undisputed Teachings

- ✓ Froitzheim teaches backside PN junction
- ✓ Froitzheim teaches metal contacts
- ✓ Froitzheim teaches texturing and anti-reflective coating
- ✓ Borden-575 teaches polysilicon emitter and tunnel oxide layer



'516 Petition, 65

Ex.1004, [0010]-[0011], [0019], [0024]-[0034], [0050], Fig.3; Ex.1006, [0016]-[0031], Figs.2-4; '516 Petition, 18-19, 24-24, 64-65; '516 Ex.1003, ¶¶103-105, 113-14, 224-225

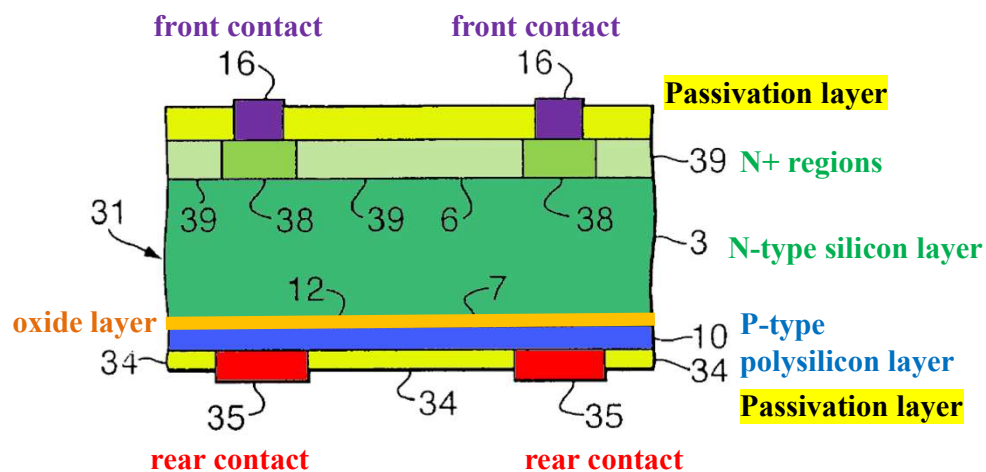
POSITA Would Be Motivated to Combine Froitzheim and Borden-575 With a Reasonable Expectation of Success

applied to a backside configuration. *See* Section X.A.1. A POSITA would have been motivated to obtain these benefits by implementing Borden-575's polysilicon emitter and tunnel oxide layer to the backside configuration taught by Froitzheim. Section X.A.1. In view of a POSITA's knowledge and the art's teachings of how

'516 Petition, 65

Moreover, Borden-575 teaches that its polysilicon emitter and tunnel oxide layer were compatible with a back-junction solar cell (e.g., Froitzheim). Borden-

'516 Petition, 66



'516 Petition, 65

'516 Petition, 64-67; '516 Ex.1003, ¶¶223-231; '516 Petitioner's Reply 22-24; '516 Ex.1077, ¶¶54-61

Disputed Issues for the Combination of Froitzheim and Borden-575

- 1 Whether Borden-575 is prior art
- 2 Petitioner's reliance on Borden-575's tunnel oxide
- 3 Whether a POSITA would have been motivated to combine Borden-575 and Froitzheim with a reasonable expectation of success

Borden-575 Is Entitled to the Filing Date of Its Provisional Application

1. Borden Provisional provides written description support for at least one claim in the non-provisional application

Amgen Inc. v. Sanofi, 872 F.3d 1367, 1380 (Fed. Cir. 2017)

2. Borden Provisional provides written description support for the subject matter relied on by Petitioner

Forescout Tech., Inc. v. Fortinet, Inc., IPR2021-01328, Paper 12, 8-9 (P.T.A.B. Jan. 27, 2022)



“The written description requirement does not require identical descriptions of [what is claimed], but it requires enough disclosure in the patent to show one of skill in this art that the inventor ‘invented what is Claimed.’”

Union Oil Co. of Cal. v. Atl. Richfield Co., 208 F.3d 989, 1001 (Fed. Cir. 2000)

'516 Petition 21-24; '516 Ex.1003, ¶¶110-112; '516 Petitioner's Reply, 17-19; '516 Ex.1077, ¶¶46-49

The Borden-575 Provisional Discloses Tunnel Oxides

Borden-575

[0022] In embodiments, the doped region 210 is formed using polysilicon, which may be deposited at a temperature on the order of 630°C and is in-situ doped. A short anneal at 1050°C for 30 seconds after deposition activates the dopants. As mentioned above, in some embodiments a thin tunnel oxide may be included between the substrate 200 and the polysilicon 210 in the contact holes 212. This oxide – typically 8 to 15Å thick – provides passivation between the substrate and the polysilicon, while allowing for tunnel current flow.

Ex.1006, [0022]

Borden Provisional

[0018] The doped region is formed using polysilicon, which may be deposited at a temperature on the order of 630°C and is in-situ doped. A short anneal at 1050°C for 30 seconds after deposition activates the dopants. A thin tunnel oxide may be included between the substrate and the polysilicon in the contact holes. This oxide – typically 8 to 15Å thick – provides passivation between the substrate and the polysilicon, as described in the prior art.

Ex.1011, [0018]

'516 Petition 21-24; '516 Ex.1003, ¶¶110-112; '516 Petitioner's Reply, 18-19, 23-24; '516 Ex.1077, ¶¶49, 61

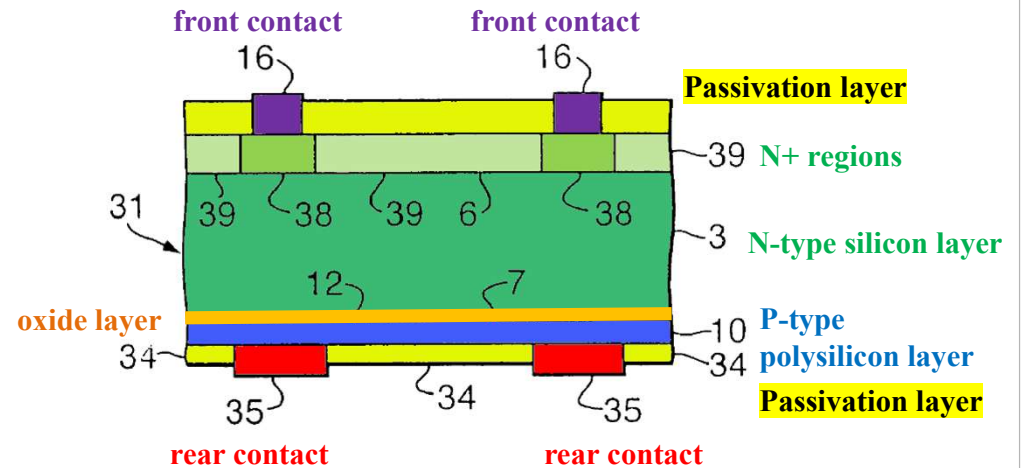
Petitioner Relied on Borden-575's Tunnel Oxide

53. Consequently, I disagree with Dr. Ruby's characterization of the buried oxide as "crucial" and the tunnel oxide as "optional." Ex.2027-Ruby-Decl., ¶¶251-253. In my opinion, a POSITA would have understood that the tunnel oxide layer must cover at least some of the interface between the emitter and the substrate, or else no current would flow. Ex.2029-Holman-Tr., 243:9-17 ("Borden teaches two

* * *

also occupy some of the wafer surface." A POSITA would also have known how to construct a cell in which the tunnel oxide covered the entire area, omitting the buried oxide layer (e.g., omitting steps S402 and S404 in Borden-575). And a POSITA would have understood that the fraction of the area covered by the tunnel oxide and the buried oxide in Borden-575 is a design tradeoff. See Ex.1006-Borden-

Ex.1077, ¶53



'516 Petition 65

'516 Petition 64-65; '516 Ex.1003, ¶¶224-225; '516 Petitioner's Reply 19-20; '516 Ex.1077 ¶¶50-53

Implementing Borden-575's Polysilicon Emitter and Tunnel Oxide Layer in Froitzheim Would Have Been Straightforward



Douglas Ruby, Ph.D.

Maxeon Expert

Q. Your declaration doesn't cite or identify any articles from before 2008 that suggest that tunnel oxides are incompatible with solar cells, correct?

A. **They are not incompatible, no.**

Q. They are compatible, correct?

A. **They are compatible.**

Q. And that was known by 2008, correct?

A. **Yes.**

Ex.1075, 107:20-108:5; '516 Petitioner's Reply, 22-23; '516 Ex.1077 ¶¶55-56, 58-59

Gan and Gan Thesis Would Not Dissuade a POSITA From Implementing Borden-575's Tunnel Oxide in Froitzheim's Solar Cell

Borden-575, Gan, and Gan Thesis Disclose Overlapping Processing Temperatures



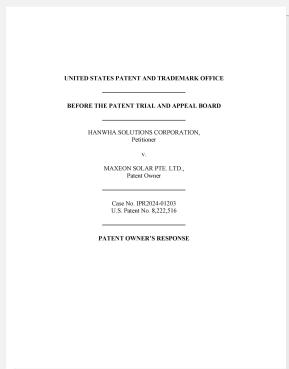
Zachary Holman, Ph.D.

Hanwha Expert

58. *Third*, Dr. Ruby incorrectly asserts that “Borden-575 uses the same high temperatures that the Gan thesis warns about...” Ex.2027-Ruby-Decl., ¶237. Gan and the Gan Thesis do not “warn about” using temperatures at or above 1000 °C. Borden-575 teaches that “[a] short anneal at 1050 °C for 30 seconds after deposition activates the dopants.” Ex.1006-Borden-575, [0022]. Both Gan and the Gan Thesis list device fabrication procedures, including: “4. Polysilicon deposition (6000 Å) and first-step anneal (1050 °C).” Ex.1005-Gan, 246; Ex.2003-Gan-Thesis, 92. Therefore, Gan and the Gan Thesis teach processing steps at the exact same temperature (1050 °C) that Borden-575 teaches. Furthermore, Gan and the Gan

'516 Ex.1077, ¶¶58-59; '516 Petitioner's Reply, 22-23

Commercial Viability Is Not Required



teaches annealing at the even higher temperature of 1050°C. A POSITA with armed with the knowledge of the Gan Thesis would have rejected using Borden-575 because a tunnel oxide is not commercially viable if Borden-575 is followed. Ex.

'516 POR, 58



“Nothing in the statute or our case law requires [patent challenger] to prove obviousness by starting with a prior art commercial embodiment and then providing motivation to alter that commercial embodiment.”

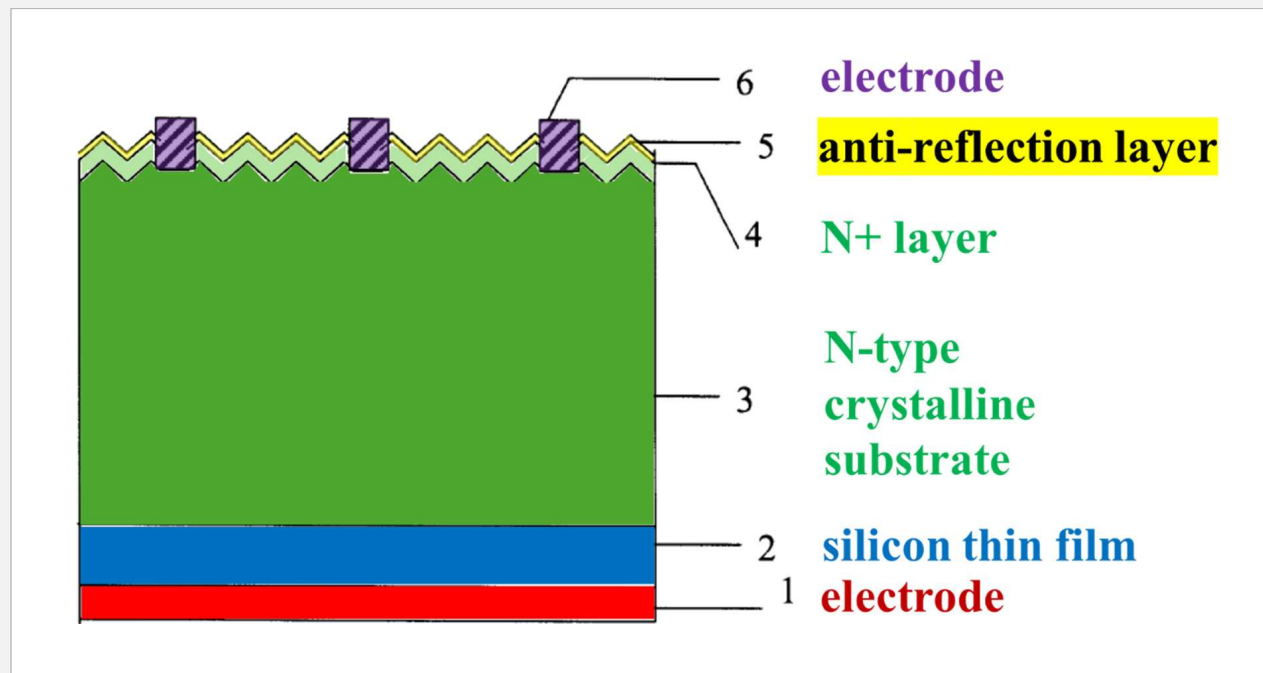
Galderma Lab'ys, L.P. v. Tolmar, Inc., 737 F.3d 731, 737 (Fed. Cir. 2013);
see also *Trs. of Columbia Univ. v. Illumina, Inc.*, 620 F. App'x 916, 932 (Fed. Cir. 2015)

'516 Petitioner's Reply, 14, 22

**Li and Gan & Li, Gan, and Smith
IPR2024-01203, Ground V
IPR2024-01199, Ground III**

Li's Undisputed Solar Cell Structure

- ✓ Backside PN junction
- ✓ Front and rear contacts
- ✓ Anti-reflective coating
- ✓ N+ front surface field
- ✓ Textured front surface



Ex.1008, 5, Fig.1

'516 Petition, 25-26; '516 Ex.1003, ¶¶115-118; '053 Petition, 23-24; '053 Ex.1077, ¶¶117-119

Disputed Issue

Patent Owner advances one unique argument for the combination of Li and Gan and Li, Gan, and Smith:

- 1 Whether Li teaches away from Gan and Smith**

Li's Teachings Are Not Limited to "Low Temperature Diffusion"

oxygen defects under illumination and resulting attenuation of conversion efficiency. In addition, a PN junction is prepared by a low-temperature deposition method, which avoids a conventional diffusion process at 800-1000°C. Such high-temperature process will cause more defects or contamination in a silicon material, which will affect the improvement of cell efficiency. In addition, the silicon thin film deposited on the back surface

Ex.1008, 4



“A statement that a particular combination is not a preferred embodiment does not teach away absent clear discouragement of that combination.”

Syntex (U.S.A.) LLC v. Apotex, Inc., 407 F.3d 1371, 1380 (Fed. Cir. 2005)

'516 Petitioner's Reply, 25-26; '516 Ex.1077 ¶¶61-62; '053 Petitioner's Reply, 27-28; '053 Ex.1077 ¶¶66-67

Li Teaches High Temperature Diffusion



Zachary Holman, Ph.D.

Hanwha Expert

1000 °C. Ex.1008-Li, 4. Moreover, Li also teaches high-temperature diffusion as a step in fabricating its solar cell, stating that “[a]fter surfaces are cleaned and textured by a standard industrial process, a highly doped N⁺ layer (4) with a sheet resistance of 100–300 Ω/□ is first diffused on the front surface....” *Id.* A POSITA would have understood that this phosphorus diffusion step requires higher temperatures such as the temperature range disclosed by Gan. *E.g.*, Ex.1019-Krygowski, 20 (phosphorous diffusion at 1000 °C); Ex.1043-Kerr, 136 (phosphorous diffusion between 840 and 925 °C); Ex.1086-Ruby-1990, 4 (phosphorous diffusion at 800 °C). The fact that Li teaches diffusion at higher temperatures further demonstrates that Li is not limited to a temperature range below 800-1000 °C.

'516 Ex.1077, ¶¶66; '053 Ex.1077, ¶¶61

'516 Petitioner's Reply, 25-26; '053 Petitioner's Reply, 27-28

Experts Agrees That a POSITA Would Know How to Perform Dopant Diffusion



Douglas Ruby, Ph.D.

Maxeon Expert

- Q. What is a dopant diffusion?
- A. Dopant diffusion is introducing these dopant atoms, usually — well, as — by providing a dopant source, and then sending that wafer through a high-temperature furnace where those dopants were then able to diffuse into the silicon and create a doped region.
- Q. When did you first become aware of dopant diffusion processes?
- A. Way back in my studies at University of Illinois.
- Q. Why were you and others at Sandia studying dopant diffusion?
- A. Why?
- Q. Yes.
- A. Because the dopant diffusion profile is an important parameter affecting the solar cell efficiency and performance.
-
- Q. And by 2008 a person of ordinary skill in the art of the '516 and '053 patents would have known how to perform POC1 diffusion?
- A. Yes.

Ex.1075, 46:22-47:16, 146:4-7; '516 Petitioner's Reply, 25-26; '516 Ex.1077, ¶¶66-67; '053 Petitioner's Reply, 27-28; '053 Ex.1077, ¶¶61-62

**Sheats Grounds
'516 Patent Claim 5
IPR2024-01203 – Grounds II, IV**

Undisputed That Sheats Teaches a “Trench” For Preventing Shorts

[0059] The process of forming the isolation trench may cause electrical short-circuits 511, 517 between the transparent conductive layer 502 and the bottom electrode 506. To electrically isolate undesirable short circuits 511 formed on an outside wall 513 of the trench 514 an isolation trench 516 is formed through the transparent conductive layer and the active layer to the bottom electrode 506 as shown in FIG. 5D. The isolation trench 516 surrounds the closed-loop trench 514 and electrically isolates the short circuits 511 on the outside wall 513 of the trench from the rest of the structure 500. A laser scribing process may form the isolation trench 516. A lesser thickness of material being scribed reduces the likelihood of undesired short circuits resulting from formation of the isolation trench 516.

Ex.1012, [0059]; see also *id.*, [0003]–[0004], [0058]

“isolation trench 516”

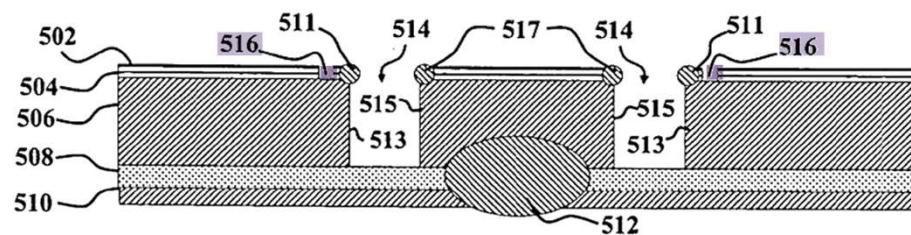


FIG. 5D

Ex.1012, Fig.5D

'516 Ex.1002 ('516 prosecution history), 81-82, 112; '516 Petition, 26, 60-63, 77-78; '516 Ex.1003, ¶¶119, 214-215; '516 Petitioner's Reply, 26-28; '516 Ex.1077, ¶69

Experts Agree Trenches Were Well Known



Zachary Holman, Ph.D.
Hanwha Expert

219. Edge isolation was therefore used by the industry to prevent a solar cell from short-circuiting, typically achieved by adding trenches, sometimes with insulating materials, near the edge of a solar cell. E.g., Ex.1065-Mason, 6:11-7:16 (“the undesired electrically conductive deposits of nickel and copper on the edges were removed by cutting a groove to a depth of 100-150 μ m into the silicon surface on the rear of the wafer and around the perimeter at a distance of 1 mm from the wafer edge.”); see also Ex.1066-Wenham, 7:23-40 (“Edge isolation”); Ex.1020-Luque, 290 (“Edge isolation by laser”). Sheats is another example that used this well-known edge isolation technique for its thin film structure. Ex.1012-Sheats, [0059] (“electrically isolate undesirable short circuits 511 formed on an outside wall 513”). As a result, a person of ordinary skill in the art would have been motivated

’516 Ex.1003, ¶219



Douglas Ruby, Ph.D.
Maxeon Expert

Q. When did you first become aware of solar cells with trench cutting?
A. Sometime when I was at Sandia.

* * *

Q. Would you agree that by 2008, a person of ordinary skill in the art would have known that trenches were one technique to prevent short-circuits?

A. It is one technique, yes.

Q. And a trench is an edge isolation technique, correct?

A. Yes, it is an example of an edge isolation technique.

* * *

Q. So trenches were known in the art before 2008, correct?

A. Oh, yes.

* * *

Q. Sheets discloses a trench, right?

A. Yes, he discloses trenches.

Ex.1075, 46:3-5, 191:6-13, 192:4-6, 196:18-19

’516 Petition, 62-63; ’516 Petitioner’s Reply, 26-28; ’516 Ex.1077 ¶69

Disputed Issue

- 1 Whether a POSITA would have been motivated to apply Sheats' trench to the Froitzheim's solar cell to prevent shorts

A POSITA Would Have Been Motivated to Implement Sheats' Trench in Froitzheim

Froitzheim's edge isolation technique would have motivated a POSITA to implement Sheats' trench

Froitzheim

[0047] If required after the formation of the n+ doped layer, a separation at the edge of the wafer may be performed, e.g. in a plasma.

Ex.1004, [0047]



Douglas Ruby, Ph.D.

Maxeon Expert

Q. Would you agree that by 2008, a person of ordinary skill in the art would have known that trenches were one technique to prevent short-circuits?

A. It is one technique, yes.

Ex.1075, 191:6-9

Q. And you'd agree that by 2008 a person of ordinary skill in the art of the '516 and '053 Patents would have been capable of adding a trench to a solar cell, correct?

A. It was well known. Different ways to do it.

Ex.1075, 194:1-4

'516 Petition, 62-63; '516 Petitioner's Reply, 27-28; '516 Ex.1077 ¶72

Sheats Teachings Are Applicable to Solar Cells

Experts agree that short circuits are issues for solar arrays



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to a particular example. However, a POSITA would have understood that Sheats' teachings regarding a trench were not limited to solar arrays. Dr. Ruby agrees that short circuits are a potential problem for both solar cells and solar arrays. Ex.1075-Ruby-Tr., 186:15-187:1, 188:10-13, 189:21-190:3. He also agrees that solar cells are connected together to form modules and arrays, and if a single solar cell short circuits, "it would reduce the output" of the solar cells to which it is connected. Ex.1075-Ruby-Tr., 187:2-18, 189:7-20. As a result, a POSITA would have understood that a trench is important not only to prevent a short circuit within a single solar cell but also to prevent a short circuit between connected cells. That is, a POSITA would have understood that a trench to prevent a short circuit in a single cell is physically and functionally similar to a trench for solar cells in an array because short circuits are a potential problem in either scenario. Therefore, a

'516 Ex.1077, ¶¶72



Douglas Ruby, Ph.D.
Maxeon Expert

Q. A short circuit is a potential problem for solar cells that are in a string of multiple solar cells, correct?

A. If a single solar cell is short-circuited in a string it would reduce the output of the string.

* * *

Q. And a short-circuit is a problem for solar cells that are on a solar array, correct?

A. A short circuit of what, an individual module?

Q. Yes.

A. That would be a problem for the array.

Ex.1075, 188:10-13, 189:21-190:3

'516 Petitioner's Reply, 28; '516 Ex.1077 ¶¶70-71

Person of Ordinary Skill in the Art

Definition of a POSITA Is Undisputed

Hanwha's POSITA	Maxeon's POSITA
“(1) an advanced degree in applied physics, chemistry, electrical engineering, materials science, mechanical engineering, or a related discipline and (2) at least one year of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. Alternatively, a person of ordinary skill in the art would have had (1) a bachelor's degree in one of the aforementioned disciplines and (2) at least two years of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. Additional work experience may compensate for less formal education, and vice versa.” '516 Petition, 17	“This Patent Owner Response (“POR”) applies the level of ordinary skill in the art proposed by Petitioner.” '516 POR, 27
	“I have been asked to apply the skill level of a person of ordinary skill in the art ('POSITA') that is proposed in the Petition, which is ‘someone with an advanced degree involving the discipline of electrical engineering, applied physics, chemistry, or materials science, and at least two years of experience designing, developing, or researching in the field.’” '516 Ex.2027 (Ruby Decl.) ¶14 (citing CSI's '516 Petition, 3.)

'516 Petition, 17; '516 POR, 27; '516 Ex.2027 ¶14 (citing CSI's '516 Petition, 3)
'053 Petition, 16; '053 POR, 24; '053 Ex.2027 ¶14