(19) Japan Patent Office (JP)

(12) **Unexamined Patent Publication (A)**

(11) Patent Application Publication No.

JP2004-266768

(P2004-266768)

(43) Publication date: September 24, 2004

(51) Int. Cl.[7]	FI		Theme code (Reference)
H04N 5/232	H04N 5/232	Z	5C022

Request for examination: Unrequested Number of claims: 14 OL (16 pages in total)

(21) Application No. 2003-57567 (P2003-57567)

(22) Application date: March 4, 2003

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F-terms (Reference) 5C022 AA13 AC54 AC69

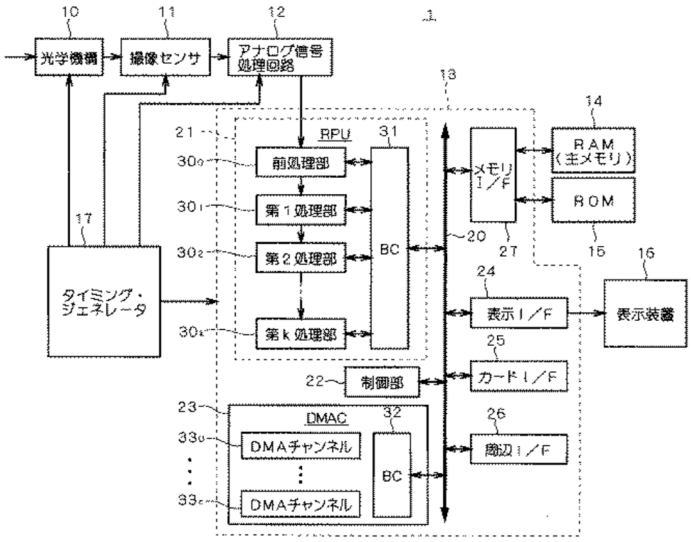
(54) [Title of the invention] Image processing system and digital camera

(57) [Abstract]

[Problem] To be able to change the geometric characteristics of image data with high real-time performance.

[Means of solving the problem] An RPU 21 in an image processing system 13 comprises an image processing unit that executes processing for geometrically changing image data, using correction data that has been provided. In addition, a data transfer control part (i.e., a DMAC) 23 reads out the correction data from a memory in accordance with the pixel position of the image data that is input to the image processing unit, and transfers it to the image processing unit of the RPU 21.

[Representative Drawing] Figure 1



[Claims]
[Claim 1]
An image processing system for changing the geometric characteristics of image data, characterized in comprising an image processing unit that executes the processes for geometrically changing image data, using correction data that has been provided, and a data transfer control part that reads out from a memory and transfers to the aforementioned image processing unit the aforementioned correction data in accordance with the pixel position of the image data that is input to the image processing unit.
[Claim 2]
An image processing system, wherein the aforementioned data transfer control part of the image processing system set forth in claim 1 comprises a direct memory access (DMA) controller that transfers the aforementioned correction data by a DMA procedure.
[Claim 3]
The image processing system set forth in claim 1 or 2, wherein the aforementioned data transfer control part has a function whereby some or all of the aforementioned correction data is shared among multiple pixels of the image data.
[Claim 4]
The image processing system set forth in any one of claims 1-3, wherein the aforementioned data transfer control part comprises a convolution calculator that samples a predetermined range of pixel data from the aforementioned input image data, and performs a convolution operation on the pixel data using a weighting coefficient.
[Claim 5]
The image processing system set forth in claim 4, wherein the aforementioned data transfer control part transfers the aforementioned weighting coefficient as the aforementioned correction data.
[Claim 6]
The image processing system set forth in claim 4, wherein the aforementioned image processing unit comprises a coefficient calculation circuit that calculates the aforementioned weighting coefficient on the basis of the aforementioned correction data.
[Claim 7]
The image processing system set forth in claim 6, wherein the aforementioned image processing unit has the functions of selecting multiple pixel data from within the aforementioned predetermined range on the basis of the aforementioned correction data, and performing the aforementioned convolution operation on the selected multiple pixel data.
[Claim 8]
The image processing system set forth in claim 7, wherein the aforementioned coefficient calculation circuit has the functions of calculating the aforementioned weighting coefficient corresponding to each said multiple pixel data selected, and setting zero as the aforementioned weighting coefficient corresponding to pixel data other than that within the aforementioned predetermined range.
[Claim 9]
The image processing system set forth in claim 7, wherein the aforementioned image processing unit comprises a selector that selects and outputs multiple pixel data from within the aforementioned predetermined range, and a calculation circuit that performs convolution operations only on said multiple pixel data output from the aforementioned selector, and the aforementioned coefficient calculation circuit computes, and supplies to the aforementioned calculation circuit, the aforementioned weighting coefficients corresponding only to said multiple pixel data selected by the aforementioned selector.
[Claim 10]
The image processing system set forth in any one of claims 1-9, wherein the aforementioned image processing unit comprises an interpolator that uses the transferred correction data to interpolate new correction data.
[Claim 11]
The image processing system set forth in any one of claims 1-10, wherein the aforementioned data transfer control part has the function of transferring correction data corresponding to a position that is

point-symmetrical with respect to the center point of the frame of the image data or the center point of a field constituting the frame.
[Claim 12]
The image processing system set forth in any one of claims 1-11, wherein the aforementioned data transfer control part has a function of transferring correction data corresponding to a position that is line-symmetrical with respect to a line segment passing through the center point of a frame of the image data or the center point of a field constituting the frame.
[Claim 13]
The image processing system set forth in any one of claims 1-12, comprising a real-time processing circuit that has multiple processing parts, connected serially, for performing multiple stages of image processing in parallel and in real time, the aforementioned image processing unit constituting a portion of the aforementioned multiple processing parts.
[Claim 14]
A digital camera equipped with the image processing system set forth in any one of claims 1-13.
[Detailed description of the invention]
[0001]
[Technical field of the invention]
The present invention relates to an image processing system that changes geometric characteristics such as aberration in an image captured by a digital camera or the like.
[0002]
[Prior art]
The light imaged by the optical system of a digital camera is detected by an image sensor comprising a solid-state imaging element such as a CCD or CMOS and converted to a digital signal, and then undergoes image processing such as color space conversion processing, pixel interpolation processing, filtering, and edge enhancement processing.
[0003]
Furthermore, image data captured by an image sensor includes various aberrations (chromatic aberration, spherical aberration, coma aberration, astigmatism, field curvature and distortion, etc.) attributable to the optical system. Techniques for correcting the effects of these aberrations are disclosed in, for example, Patent Document 1 (Japanese Unexamined Patent Application Publication No. H06-113309) and Patent Document 2 (Japanese Unexamined Patent Application Publication No. H05-3568). Since the amount of aberration caused by the optical system varies, depending on imaging conditions such as the focal length and aperture value of the optical system, the amount of correction must selected be in accordance with changes in imaging conditions.
[0004]
Spatial filters are also used for filtering as a means of correcting the above-mentioned aberrations. A spatial filter samples data, among input data, in a range of for example 3x3 pixels, and performs a convolution operation in which each sampled data is multiplied by a filter coefficient, and the results are summed.
[0005]
[Patent Document 1]
Japanese Unexamined Patent Application Publication No. H06-113309
[Patent Document 2]
Japanese Unexamined Patent Application Publication No. H05-3568
[0006]
[Problem to be solved by the invention]
When the amount of correction for aberration varies depending on pixel position within an image frame, the filter coefficient set for the spatial filter must be changed in accordance with the sampling range of the input data, but the process of setting the filter coefficient interrupts the sequence of image processing, becoming a cause of reduced processing speed. In the case of distortion aberration for example, it is necessary to change the filter coefficient settings dynamically, according to the filtering

target range, since the amount of aberration (distortion) in the center of the image frame differs from that in the periphery thereof.
[0007]
In view of the above circumstances, the object of the present invention is to provide an image processing system that makes it possible to change the geometric characteristics of image data with high real-time performance, and a digital camera equipped with the image processing system.
[0008]
[Means of solving the problem]
In order to achieve the abovementioned object, a first invention is an image processing system for changing the geometric characteristics of image data that is characterized in comprising an image processing unit that executes processing for geometrically changing image data, using correction data that has been provided, and a data transfer control part that reads out the correction data from a memory and transfers it to the image processing unit in accordance with the pixel position of the image data that is input to the image processing unit.
[0009]
In a second invention, the data transfer control part of the image processing system in the first invention comprises a direct memory access (DMA) controller that transfers the correction data by a DMA procedure.
[0010]
In a third invention, the data transfer control part of the image processing system in the first or second invention has a function whereby some or all of the correction data is shared among multiple pixels of the image data.
[0011]
In a fourth invention, the data transfer control part of the image processing system in any of the first to third inventions comprises a convolution calculator that samples a predetermined range of pixel data from the input image data and performs a convolution operation on the pixel data, using a weighting coefficient.
[0012]
In a fifth invention, the data transfer control part of the image processing system in the fourth invention transfers the weighting coefficient as the correction data.
[0013]
In a sixth invention, the image processing unit of the image processing system set forth in claim 4 comprises a coefficient calculation circuit that calculates the weighting coefficient on the basis of the correction data.
[0014]
In a seventh invention, the image processing unit of the image processing system in the sixth invention has the functions of selecting multiple pixel data from within the predetermined range on the basis of the correction data, and performing the convolution operation on the selected multiple pixel data.
[0015]
In an eighth invention, the coefficient calculation circuit of the image processing system in the seventh invention has the functions of calculating the weighting coefficient corresponding to each said multiple pixel data selected, and setting zero as the weighting coefficient corresponding to pixel data other than that within the predetermined range.
[0016]
In a ninth invention, the image processing unit of the image processing system in the seventh invention comprises a selector that selects and outputs multiple pixel data from within the predetermined range, and a calculation circuit that performs convolution operations only on the multiple pixel data output from the selector, and the coefficient calculation circuit computes, and supplies to the calculation circuit, the weighting coefficients corresponding only to the multiple pixel data selected by the selector.
[0017]
In a tenth invention, the image processing unit of the image processing system in any of the first to ninth inventions comprises an interpolator that uses the transferred correction data to interpolate new correction data.
[0018]
In an eleventh invention, the data transfer control part of the image processing system in any of the first to tenth inventions has the function of transferring correction data corresponding to a position that

is point-symmetrical with respect to the center point of the frame of the image data or the center point of a field that constitutes the frame.
[0019]
In a twelfth invention, the data transfer control part of the image processing system in any of the first to eleventh inventions has a function of transferring correction data corresponding to a position that is line-symmetrical with respect to a line segment passing through the center point of a frame of the image data or the center point of a field that constitutes the frame.
[0020]
In a thirteenth invention, the image processing system in any of the first to twelfth inventions comprises a real-time processing circuit that has multiple processing parts, connected serially, for performing multiple stages of image processing in parallel and in real time, the image processing unit constituting a portion of the multiple processing parts.
[0021]
Finally, a fourteenth invention is a digital camera equipped with the image processing system in any of the first to thirteenth inventions.
[0022]
[Embodiments of the invention]
Various embodiments of the present invention are described below.
[0023]
<Configuration of Digital Camera 1>
Figure 1 is a schematic block diagram showing the configuration of a digital camera 1 in an embodiment of the present invention. The digital camera 1 is provided with an optical mechanism 10, an image sensor 11, an analog signal processing circuit 12, a timing generator 17, an image processing LSI (integrated circuit) 13, a RAM (main memory) 14, a ROM 15, and a display device 16. Although not shown in the drawing, the digital camera 1 also is equipped with a ranging sensor and a strobe that emits flashing light or the like.
[0024]
The optical mechanism 10 is equipped with an optical lens, an aperture, etc. Incident light from a subject passes through the optical mechanism 10 and forms an image on a light receiving part of the image sensor 11. The image sensor 11 comprises a CCD area sensor or a CMOS area sensor, and receives light that has passed through the optical mechanism 10, photoelectrically converts it, generates an analog image signal, and outputs it to the analog signal processing circuit 12. The analog signal processing circuit 12 performs correlated double sampling (CDS) processing of the analog image signal input from the image sensor 11 to remove noise from the analog image signal, then performs automatic gain control (AGC) processing to amplify the analog image signal, converts it from an analog to a digital image signal, and outputs it to the image processing LSI 13.
[0025]
The timing generator 17 uses a reference clock signal supplied from a PLL circuit (not shown) to generate and supply a clock signal, required for operation, to modules such as the optical mechanism 10, the image sensor 11, the analog signal processing circuit 12, and the image processing LSI 13.
[0026]
The image processing LSI 13 comprises a real-time processing circuit (RPU) 21, a control unit 22 that includes a CPU, a direct memory access controller (DMAC) 23, a memory interface 27, a display interface 24, a card interface 25, and a peripheral interface 26. A bus 20 is provided with an address bus for transmitting address signals, a data bus for transmitting data signals, and a control bus for transmitting control signals, and electrically connects the components 21, 22, 23, 24, 25, 26, and 27 of the image processing LSI 13.
[0027]
The control unit 22 has a built-in CPU, and executes a program loaded from the ROM 15 to perform control processing for controlling each processing block in the RPU 21, as well as image processing, etc. The main memory 14 is also used as an area for temporarily storing data processed by the RPU 21 and data generated during operation of the control unit 22. In the present embodiments, the main

memory 14 and ROM 15 are arranged outside the image processing LSI 13, but the present invention is not limited thereto, and the main memory 14 and ROM 15 may both be mounted inside the image processing LSI 13.
[0028]
In addition, data transfer via the bus 20 is performed under the control of the control unit 22 or the DMAC 23. In the present specification, the term "data transfer control part" means the control unit 22 and/or the DMAC 23. The DMAC 23 comprises a bus control (BC) circuit 32 and multiple DMA channels 33_0 to 33_n (n: an integer 2 or greater), and when the DMAC 23 receives a DMA transfer request, a DMA channel 33_m (m = 0 to n) is assigned to the DMA transfer request, and the bus control circuit 32 acquires the bus 20. The bus control circuit 32 then executes a DMA transfer using the assigned DMA channel 33_m. After this DMA transfer is completed, control of the bus 20 is returned to the control unit 22 by the bus control circuit 32.
[0029]
The RPU 21 comprises multiple processing blocks 30_0, 30_1, 30_2, ..., 30_k, connected in series over k+1 stages (k: an integer 3 or greater), and a bus control (BC) circuit 31, and is a circuit that performs real-time image processing of the digital image signal input from the analog signal processing circuit 12. These processing blocks 30_1 to 30_k operate in parallel to execute pipeline processing, in which data input from the preceding processing block is processed and output to the next processing block or to the outside.
[0030]
The preprocessing unit 30_0 is a processing block that performs white balance adjustment, gain adjustment, defect signal correction, etc. of the digital image signal input from the analog signal processing circuit 12. The data output from the preprocessing unit 30_0 sequentially undergoes multiple stages of image processing by the first processing unit 30_1, second processing unit 30_2, ..., and kth processing unit 30_k, and is then output to the bus 20 via the bus control circuit 31. Processed data output from the RPU 21 to the bus 20 is transferred by the control unit 22 or the DMAC 23 to the memory interface 27, and buffered in the main memory 14.
[0031]
The display interface 24 has the function of converting the image data read out and transferred from the main memory 14 by the control unit 22 or the DMAC 23 into data in a format that the display device 16 can support. The display device 16 may be a dot sequential liquid crystal display or a field sequential drive electronic viewfinder (EVF), for example.
[0032]
The card interface 25 is a circuit that, under the control of the control unit 22, executes data input/output to/from a portable memory card (not shown) equipped with a non-volatile memory or the like. The control unit 22 compresses and encodes the image data read out from the main memory 14 and transfers it to the card interface 25, so that the compressed and encoded data can be recorded on the portable memory card. Conversely, the control unit 22 can also read out and decode the compressed and encoded data recorded on the portable memory card via the card interface 25. The peripheral interface 26 performs data input/output for peripheral modules such as a light control sensor.
[0033]
<Configuration of RPU 21>
Next, an outline of an example of a configuration of an RPU 21 corresponding to the image processing unit in the present embodiments is described below. Figure 2 is a schematic block diagram showing an example of an RPU 21 configuration. The RPU 21 is configured with the abovementioned preprocessing unit 30_0, a single pixel processing unit 30_1, a filtering unit 30_2, a pixel interpolation and gamma correction processing unit 30_3, a color space conversion and color suppression processing unit 30_4, a coring processor 30_5, a resolution converter 30_6, and a bus control circuit 31.
[0034]
The single pixel processing unit 30_1 has the function of processing the image data input from the preprocessing unit 30_0 on a pixel-by-pixel basis. Specifically, the single pixel processing unit 30_1 performs time-dependent averaging processing that averages input data over the course of multiple

frames or subframes, shading correction processing to correct uneven brightness in the image, etc. A subframe is a frame decomposed into multiple pieces. For example, when one frame is decomposed into an even field comprising only even lines and an odd field comprising only odd lines, the even field and odd field are considered to be subframes.
[0035]
The filtering unit 30_2, which comprises a register for internally storing filter coefficients for 25 points, samples a two-dimensional array of 25 data points in a 5x5-pixel range of input data, and performs a convolution operation (product-sum operation) in which data at each point is multiplied by the filter coefficients and the results are summed. Moreover, as will be described below, the filtering unit 30_2 can also perform processing to change the image data geometrically by adjusting the filter coefficients, as appropriate. This enables correction of various aberrations in the image data that are caused by the optical mechanism 10.
[0036]
The pixel interpolation and gamma correction processing unit 30_3 has the functions of performing pixel interpolation processing, in which color components missing in each pixel are interpolated using the surrounding pixels, and gamma correction processing, in which gamma characteristics are corrected. In general, with the exception of some imaging elements, an image sensor 11 equipped with only one imaging element can obtain only a single color component per pixel. For this reason, a known method such as nearest neighbor interpolation, bi-linear interpolation, or cubic convolution interpolation may be used to interpolate color components missing in each pixel, and thereby generate color image data with multiple color components.
[0037]
The color space conversion and color suppression processing unit 30_4 has the functions of executing color space conversion processing to convert the color space of the input data, and color suppression processing to suppress color development in bright and dark areas in an image where white balance is easily disturbed. In color space conversion processing, processing is performed for converting, for example, from a primary RGB color space to a YCbCr color space or a YUV color space comprising one luminance component and two color difference components per pixel.
[0038]
The coring processor 30_5 is a functional block that executes nonlinear processing (coring processing) for suppression of high-frequency components contained in the image data. The resolution converter 30_6 has the function of performing resolution conversion processing to reduce or enlarge the image size (resolution) of the input data. Note that the resolution converter 30_5 [sic] can also output the input data directly, without changing its resolution.
[0039]
Although the above processing blocks 30_0 to 30_6 cooperate to execute the abovementioned pipeline processing, each of processing blocks 30_0 to 30_6 can also perform image processing independently without cooperating with other processing blocks. For example, after the filtering unit 30_2 processes the image data transferred by the bus control circuit 31 under the control of the control unit 22, the data can be processed by being output to the bus control circuit 31 without being output to the pixel interpolation and gamma correction processing unit 30_3 in the next stage.
[0040]
<First embodiment: Configuration and operation of filtering unit 30_2>
The configuration and operation of filtering unit 30_2 of an image processing system in a first embodiment of a digital camera 1 (Figures 1 and 2) having the above-mentioned configuration is described below. Figure 3 is a schematic block diagram showing the configuration of a filtering unit 30_2.
[0041]
The filtering unit 30_2 is provided with a convolution calculator 41, and the convolution calculator 41 has the functions of sampling pixel data from the input image data within a predetermined range (referred to below as a filter range), and performing a convolution operation on the pixel data using filter coefficients (weighting coefficients). The convolution calculator 41 has a built-in coefficient

register 40 that holds coefficient data (correction data) comprising a two-dimensional array of filter coefficients. The convolution calculator 41 performs a convolution operation on the input data ID from the preceding processing block 30_1 using the filter coefficients supplied from the coefficient register 40, and outputs the resulting output data OD to the next processing block 30_3.

[0042]

Figure 4 is a schematic drawing that shows the coefficient data 42 stored in the coefficient register 40. The coefficient data 42 comprises filter coefficients γ(0,0), γ(0,1), ..., γ(4,4) of a two-dimensional array of 5 × 5 points (= 25 points). Figure 5 is a schematic drawing that shows the correspondence between the input data and the filter range 39. The drawing shows a filter range 39 of 5 x 5 pixels centered on the pixel of interest at column i, row j (where i, j are integers 0 or greater) of the input data. The filtering output value CP (i, j) for this pixel of interest is calculated in accordance with the following Formula (1).

[0043]

[Formula 1]

$$CP(i, j) = \sum_{m=0}^{4} \sum_{n=0}^{4} \gamma(m, n) \times P(i-2+m, j-2+n) / K \quad \cdots (1)$$

[0044]

In the above Equation (1), γ(m, n) represents the filter coefficient of the mth row and nth column shown in Figure 4, and P (i-2+m, j-2+n) represents the pixel value of the (i-2+m)th row and the (j-2+n)th column. Also in the above Equation (1), 1/K represents a division coefficient, which is set as appropriate.

[0045]

In this embodiment, the DMAC 23 reads out, from the main memory 14, coefficient data corresponding to the filter range of 5×5 pixels of input data sampled by the convolution calculator 41, and transfers the coefficient data to the RPU 21 by DMA. As shown in figure 6, the coefficient data 42 is transferred to the filtering unit 30_2 by DMA in pixel units, in accordance with the data input, and after being received by the bus control circuit 31 of the RPU 21, is input to the filtering unit 30_2. The coefficient data 42 is then stored and set in the coefficient register 40 (figure 3). The process of setting the coefficient data 42 can be executed for each filter coefficient while the processing blocks 30_0 to 30_6 of the RPU 21 are executing pipeline processing, without interrupting the pipeline processing. In other words, the coefficient register 40 can dynamically update the coefficient data stored therein with the coefficient data 42 input from the bus control circuit 31 on a pixel-by-pixel basis. Consequently, it is possible to dynamically update one or multiple filter coefficients γ(o,p) (where o and p are integers from 0 to 4) exclusively, designated from among the group of filter coefficients shown in Figure 4.

[0046]

As indicated above, the image processing system (image processing LSI 13) in the first embodiment can dynamically modify the coefficient data (correction data) in accordance with the pixel positions of the image data input to the filtering unit 30_2, thus enabling the geometric characteristics of the image data to be changed in high real-time. Since the coefficient data can be dynamically modified on a pixel-by-pixel basis, it is also possible to correct geometric characteristics, such as curvature aberration (distortion), of a specified area within an image frame or field. Furthermore, since the filter coefficients can be dynamically updated without interrupting the multi-stage image processing in the RPU 21, the operating speed of the image processing system can be increased.

[0047]

The filtering unit 30_2 is also able to share part or all of the coefficient data among a plurality of pixels of the image data. The amount of coefficient data transferred to the filtering unit 30_2 is thereby reduced, thus enabling reduction of the bandwidth used on the bus 20, and enabling increased overall processing speed of the image processing system.

[0048]
Next, an example of filtering processing using the abovementioned image processing LSI 13 will be described with reference to Figure 7. In this example, it is assumed that the input data has a distortion aberration that increases the imaging magnification from the center to the periphery of the image. This type of distortion aberration is called barrel aberration. The filter coefficients stored by the coefficient register 40 are dynamically updated to correct this barrel aberration.
[0049]
When the local data 46a in the upper left corner of one frame of input data 46 shown in Figure 7 is filtered, the X character data in the local data 46a is converted into X' character data near the pixel of interest in the corrected local data 46a' by filtering, using the coefficient data 47a. The coefficient data 47a shown in Figure 7 has a filter coefficient value represented in the center of each square.
[0050]
When the local data 46c at the center position of the input data 46 is filtered, the X character data in the local data 46c is converted to X' character data near the pixel of interest in the corrected local data 46c' by filtering, using the coefficient data 47c. When the local data 46b at the lower right corner of the input data 46 is filtered, the X character data in the local data 46b is converted to X' character data near the pixel of interest in the corrected local data 46b' by filtering, using the coefficient data 47b. In this way, the barrel aberration is corrected by dynamically changing the filter coefficients in accordance with the sampling range of input data 46.
[0051]
<Second embodiment>
Next, the configuration and operation of the filtering unit 30_2 of an image processing system will be described in a second embodiment of the present invention. Figure 8 is a schematic drawing that shows the circuit configuration of the filtering unit 30_2 in the present embodiment.
[0052]
The filtering unit 30_2 is configured to include a convolution calculator 41 and a coefficient calculation circuit 50. The coefficient calculation circuit 50 calculates nine filter coefficients (weighting coefficients), corresponding to 3x3 pixels on the basis of vector data VD (correction data) transferred from the main memory 14 by DMA, and supplies them to the convolution calculator 41. The convolution calculator 41 has the functions of sampling the input data ID in a filter range of 3×3 pixels, performing a convolution operation on the data, and outputting output data OD. Note however that while a filter range of 3×3 pixels is adopted in the present embodiment for convenience of explanation, the filter range in the present invention may be expanded to a size of 5×5 pixels or greater.
[0053]
The convolution calculator 41 comprises data registers 51A to 51I for 3×3 pixels connected in series, and two line memories 52A and 52B. The data registers 51A to 51I and the line memories 52A and 52B sequentially latch pixel data in a filter range of 3×3 pixels each time a pixel clock (not shown) is input. The symbols D00, D01, ..., D22 shown in the data registers 51A to 51I in the diagram represent pixel data values.
[0054]
The convolution calculator 41 also comprises nine coefficient registers 40A to 40I, corresponding respectively to the data registers 51A to 51I, and multipliers 54A to 54I. The symbols C00, C01, ..., C22 written in the coefficient registers 40A to 40I in the diagram represent the values of filter coefficients. Each time a pixel clock (not shown) is input, the coefficient registers 40A to 40I respectively latch the filter coefficients supplied from the coefficient calculation circuit 50, and supply them to the multipliers 54A to 54I. The multipliers 54A to 54I respectively multiply the pixel data input from the data registers 51A to 51I by the coefficient data input from the coefficient registers 40A to 40I, and supply the resulting operation data to an adder (Σ) 55.
[0055]

The adder 55 adds the calculation data input from the nine multipliers 54A to 54I and outputs the resulting data to a divider 56, and the divider 56 executes division processing by performing a right bit shift operation on the input data, and outputs the resulting data OD.
[0056]
Next, the processing of the coefficient calculation circuit 50 will be explained in detail. In the coefficient calculation circuit 50, a filter range of 3×3 pixels in the convolution calculator 41 is virtually divided into multiple areas. Figure 9 is a schematic drawing that shows a filter range SD of 3×3 pixels. This filter range SD is divided into a first area 57A of 2×2 pixels at the upper left, a second area 57B of 2×2 pixels at the upper right, a third area 57C of 2×2 pixels at the lower left, and a fourth area 57D of 2×2 pixels at the lower right.
[0057]
The filter coefficients are virtually arrayed at each grid point on the grid lines, as shown in Figure 10. In Figure 10, the values of the filter coefficients C00, C01, …, C22 are shown at grid points corresponding to the filter coefficients.
[0058]
The vector data VD designates a point VP on the two-dimensional grid space shown in Figure 10 and expressed as a pair of two numbers (α,β). The DMAC 23 can transfer the vector data VD to the filtering unit 30_2 on a pixel-by-pixel basis. The coefficient calculation circuit 50 selects the first area 57A (Figure 9) when the designated point VP specifies a range in the grid space demarcated by the filter coefficients of the upper left 2x2 points from among the filter coefficients of the 3x3 points, selects the second area 57B (Figure 9) when the designated point VP specifies a range demarcated by the filter coefficients of the upper right 2x2 points, selects the third area 57C (Figure 9) when the designated point VP specifies a range demarcated by the filter coefficients of the lower left 2x2 points, and selects the fourth area 57D (Figure 9) when the designated point VP specifies a range demarcated by the filter coefficients of the lower right 2x2 points. Figure 10 shows an example of specifying a range demarcated by the filter coefficients of the upper left 2×2 points.
[0059]
The coefficient calculation circuit 50 then sets the filter coefficient values selected in accordance with the designated point VP, and sets the non-selected filter coefficients to zero. In the example shown in Figure 10, the filter coefficient values C00, C01, C10, and C11 are set, and the non-selected filter coefficient values C02, C12, C20, C21, and C22 are set to zero values. All selected filter coefficient values may be set to the same value, or the filter coefficient values may be calculated in accordance with the distances R00, R01, R10, and R11 between the grid points, indicating the selected filter coefficients, and the designated points VP, as shown in Figure 10.
[0060]
Transferring the vector data (correction data) VD in this manner in the present embodiment enables generation of filter coefficients in accordance with input of image data to the filtering unit 30_2, thus making it possible to change the geometric characteristics of image data in high real-time. Since the coefficient data can be generated on a pixel-by-pixel basis, it is also possible to correct geometric characteristics, such as curvature aberration (distortion), of a specified area within an image frame or field. Furthermore, since the vector data VD is transferred to the filtering unit 30_2, the amount of data transferred is less than when filter coefficients are transferred directly. Bus bandwidth usage is thus curtailed, enabling increased overall processing speed of the image processing system.
[0061]
Furthermore, enabling geometric transformation processing of image data through use of the functions of the filtering unit 30_2 of the RPU 21 without addition of any new hardware makes smaller image processing system circuits feasible.
[0062]
<Third embodiment>
Next, the configuration and operation of the filtering unit 30_2 of an image processing system will be described in a third embodiment of the present invention. Figure 11 is a schematic drawing that shows the circuit configuration of the filtering unit 30_2 in the present embodiment.

[0063]
The filtering unit 30_2 comprises a convolution calculator 41 having the same configuration as the convolution calculator 41 shown in Figure 8, and also comprises an interpolator 60, a control unit 61, a coefficient calculation circuit 62, a first selector 63A to a fourth selector 63B, a first multiplier 64 to a fourth multiplier 64D, an adder 65, and a divider 56B.
[0064]
The convolution calculator 41 executes filtering processing by performance of a convolution operation on the input data ID from the preceding processing block, and outputs the resulting data OD1 to the next processing block. The interpolator 60, control unit 61, coefficient calculation circuit 62, selectors 63A to 63D, multipliers 64A to 64D, adder 65, and second divider 56B perform convolution operations, in parallel with filtering processing by the convolution calculator 41, to perform geometric transformation processing of the input data ID.
[0065]
The interpolator 60 executes interpolation processing to interpolate vector data VD (correction data) using the DMA-transferred vector data VD, and supplies the resultant vector data VD to the control unit 61 and the coefficient calculation circuit 62. This makes in unnecessary to transfer all of the vector data VD, so that bandwidth use on the bus 20 can be reduced, and thus the processing speed of the image processing system can be increased. The well-known nearest neighbor interpolation, bilinear interpolation, and cubic convolution interpolation methods are among the interpolation methods that can be used. The interpolator 60 also has a function for outputting vector data VD directly, without interpolation.
[0066]
The control unit 61 generates a selection control signal using the vector data VD supplied from the interpolator 60, and supplies it to each of the first to fourth selectors 63A to 63D. The first to fourth selectors 63A to 63D each select any of the pixel data transmitted from the data registers 51A to 51I of the convolution calculator 41 in accordance with the value of the selection control signal, and output it to the first to fourth multipliers 64A to 64D. The upper left pixel data in each of the first to fourth areas 57A to 57D shown in Figure 9 is input to the first selector 63A, the upper right pixel data in each of the first to fourth areas 57A to 57D shown in Figure 9 is input to the second selector 63B, the lower left pixel data in each of the first to fourth areas 57A to 57D shown in Figure 9 is input to the third selector 63C, and the lower right pixel data in each of the first to fourth areas 57A to 57D shown in Figure 9 is input to the fourth selector 63D.
[0067]
Meanwhile, the coefficient calculation circuit 62 generates weighting coefficients C1 to C4 using the vector data VD supplied from the interpolator 60, and outputs them to the first to fourth multipliers 64A to 64D, respectively. The first to fourth multipliers 64A to 64D respectively multiply the values of the input data from the selectors 63A to 63D by the weighting coefficients C1 to C4 provided by the coefficient calculation circuit 62, and supply the resulting data to an adder (Σ) 65. The adder 65 sums the data input from the first multiplier 64A to the fourth multiplier 64D, and outputs the result to the divider 56B, which processes the input data by division and outputs the data OD2 thus obtained. Thus, the convolution circuit of this embodiment comprises the first to fourth multipliers 64A to 64D, the adder 65, and the divider 56B.
[0068]
Next, the geometric transformation process of the present embodiment will be described. The coefficient calculation circuit 62 selects a first area 57A (Figure 9) when the point VP designated on the basis of the vector data VD designates a range demarcated by the upper left 2×2 weighting coefficients of the 3×3 weighting coefficients in the grid space shown in Figure 10, selects a second area 57B (Figure 9) when the designated point VP designates a range demarcated by the upper right 2×2 weighting coefficients, selects a third area 57C (Figure 9) when the designated point VP designates a range demarcated by the lower left 2×2 weighting coefficients, and selects a fourth area 57D (Figure 9) when the designated point VP designates a range demarcated by the lower right 2×2 weighting coefficients.

[0069]
The coefficient calculation circuit 62 then generates the values of weighting coefficients C1 to C4 selected in accordance with the designated point VP and supplies them to the first to fourth multipliers 64A to 64D, respectively.
[0070]
Meanwhile, the control unit 61 generates a selection control signal and supplies it to the first to fourth selectors 63A to 63D in order to select pixel data within the area selected using the designated point VP. In the example shown in Figure 10, a selection control signal is generated to select pixel data in the first area 57A (Figure 9) corresponding to the values C00, C01, C10, and C11.
[0071]
Thus, vector data (correction data) VD can be transferred to the filtering unit 30_2 in accordance with the pixel position of image data input to generate weighting coefficients in the present embodiment, making it possible to change the geometric characteristics of image data in high real-time. Since the vector data VD can be generated on a pixel-by-pixel basis, it is also possible to correct geometric characteristics of a specified area within an image frame or field. Furthermore, since the vector data VD is transferred to the filtering unit 30_2, the amount of data transferred is smaller than when the weighting coefficients are transferred directly. Bus bandwidth usage is thus curtailed, enabling increased overall processing speed of the image processing system.
[0072]
<Fourth embodiment>
Next to be described is an imaging system in a fourth embodiment of the present invention. This image processing system is characterized by transfer control processing by the DMAC 23 for transferring correction data such as vector data or coefficient data.
[0073]
Figure 12 is a schematic drawing that shows correction data 70 for one frame or one field. Correction data is read out along a scanning direction 71, corresponding to the range of data ID input to the convolution calculator 41 (Figures 3 and 8), and transferred from the memory to the RPU 21 by DMA. The scanning direction 71 in this example is from the left edge to the right edge, with the upper left corner of the correction data 70 as the start point, and when the scan reaches the right edge, it jumps to the next left edge, with the lower right edge as the end point. The amount of correction data transferred can be reduced by the transfer control process described below.
[0074]
As shown in Figure 13, the correction data 70 is virtually divided into multiple block areas that are in a point-symmetric relationship with respect to a center point CP, or in a line-symmetric relationship with respect to a line segment that passes through the center point. Figure 13 shows an example of correction data 70 divided into a first to fourth block areas 72A to 72D. The first block area 72A and fourth block area 72D are in a point-symmetric relationship with respect to the center point CP, and the second block area 72B and third block area 72C are also in a point-symmetric relationship with respect to the center point CP. The first block area 72A and second block area 72B, and the third block area 72C and fourth block area 72D, are in line-symmetrical relationships with respect to a horizontal line segment HL passing through the center point CP; and the first block area 72A and third block area 72C, and the second block area 72B and fourth block area 72D, are in line-symmetrical relationships with respect to a vertical line segment VL passing through the center point CP.
[0075]
The DMAC 23 has the function of transferring correction data corresponding to a point-symmetric or line-symmetric position with respect to the center point of a frame of the correction data 70 or the center point of a field constituting the frame. Specifically, when the correction data of one block area selected from the multiple block areas 72A to 72D (referred to below as the selected area) is transferred, the correction data is transferred directly from the memory to the RPU 21 by DMA. When coefficient data of a block area other than the selected area is to be transferred, the DMAC 23, instead of transferring said correction data, transfers, by DMA, correction data from within a selected area that is located point-symmetrically or line-symmetrically thereto.
[0076]

For example, when the first block area 72A is selected, only the correction data for the first block area 72A needs to be stored in the memory. When the DMAC 23 receives a transfer request for correction data in the first block area 72A, it transfers said correction data directly. As shown in Figure 14, when the DMAC 23 has received a transfer request for correction data P1 in the second block area 72B, the DMAC 23 reads out from the memory and transfers correction data P0 from within the selection area 72A, which is in a line-symmetric relationship with the correction data P1 with respect to the vertical line segment VL, instead of transferring the correction data P1. When the DMAC 23 receives a transfer request for correction data P2 in the third block area 72C, correction data P0 from within the selected area 72A, which is in line symmetry with the correction data P2 with respect to the horizontal line segment HL, is read out and transferred, instead of correction data P2. When the DMAC 23 receives a transfer request for correction data P3 in the fourth block area 72D, correction data P0 is read out and transferred from within the selected area 72A, which is in point symmetry with the correction data P3 with respect to the central point CP.

[0077]

Such a transfer control process renders unnecessary storage of correction data for all of the block areas 72A to 72D in the memory, and therefore, memory capacity for correction data storage can be reduced.

[0078]

[Effect of the invention]

As indicated above, the image processing system and digital camera equipped with the image processing system of the present invention enable dynamic updating of correction data to be used in an image processing unit, in accordance with data input to the image processing unit, and thus make it possible to change geometric characteristics of image data such as curvature aberration (distortion) with high real-time performance. Since the correction data can be dynamically modified on a pixel-by-pixel basis, it is also possible to make subtle changes in the geometric characteristics of a specified area within an image frame or field.

[Brief explanation of the drawings]

Figure 1 is a schematic block diagram showing the configuration of a digital camera 1 in an embodiment of the present invention.

Figure 2 is a schematic block diagram showing an example configuration of an RPU of the digital camera in an embodiment of the present invention.

Figure 3 is a schematic block diagram showing the configuration of a filtering unit in a first embodiment of the present invention.

Figure 4 is a schematic drawing that shows the coefficient data stored in the coefficient register.

Figure 5 is a schematic drawing that shows the correspondence between the input data and the filter range.

Figure 6 is a schematic drawing that shows a method of transferring coefficient data to a filtering unit.

Figure 7 is a drawing that illustrates an example of a filtering process in an embodiment of the present invention.

Figure 8 is a schematic drawing that shows the circuit configuration of the filtering unit in a second embodiment of the present invention.

Figure 9 is a schematic drawing that shows a filter range of 3×3 pixels.

Figure 10 is a schematic drawing that shows filter coefficients in a grid space.

Figure 11 is a schematic drawing that shows the circuit configuration of the filtering unit in a third embodiment of the present invention.

Figure 12 is a schematic drawing that shows correction data for one frame or one field.

Figure 13 is a schematic drawing that shows an example of correction data divided into multiple block areas.

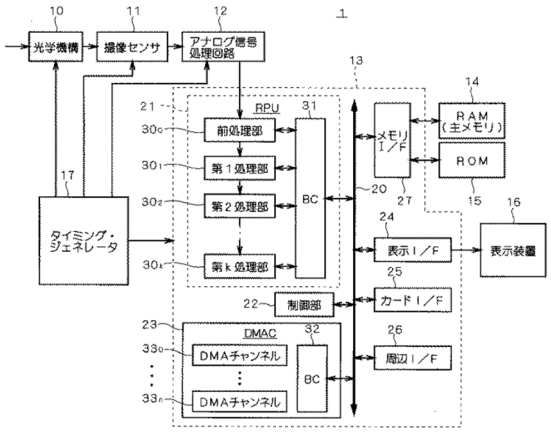
Figure 14 is a schematic drawing that shows an example of correction data divided into multiple block areas.

[Explanation of symbols]

1 Digital camera
10 Optical mechanism
11 Image sensor
12 Analog signal processing circuit

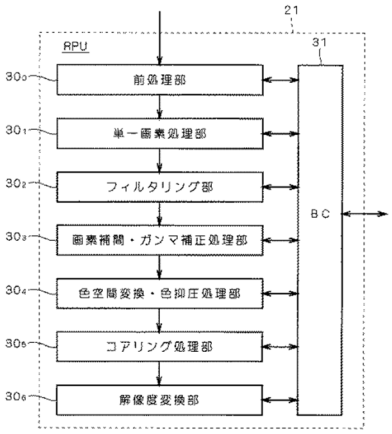
13 Image processing LSI
14 Main memory
15 ROM
16 Display device
17 Timing generator
20 Bus
21 RPU
22 Control unit
23 DMAC
24 Display interface
25 Card interface
26 Peripheral interface
27 Memory interface

[Figure 1]



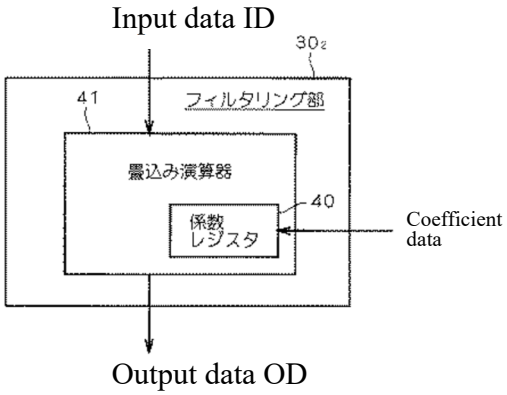
1: Digital camera
10: Optical mechanism
11: Image sensor
12: Analog signal processing circuit
13: Image processing LSI
14: Main memory
15: ROM
16: Display device
17: Timing generator
20: Bus
21: RPU
22: Control unit
23: DMAC
24: Display interface
25: Card interface
26: Peripheral interface
27: Memory interface
31: Bus control circuit
32: Bus control circuit
30_0: Preprocessing unit
30_1: First processing unit
30_2: Second processing unit
30k: kth processing unit
33_0: DMA channel
33_n: DMA channel

[Figure 2]



21: RPU
31: Bus control circuit
30_0: Preprocessing unit
30_1: Single pixel processing unit
30_2: Filtering unit
30_3: Pixel interpolation and gamma correction processing unit
30_4: Color space conversion and color suppression processing unit
30_5: Coring processor
30_6: Resolution converter

[Figure 3]



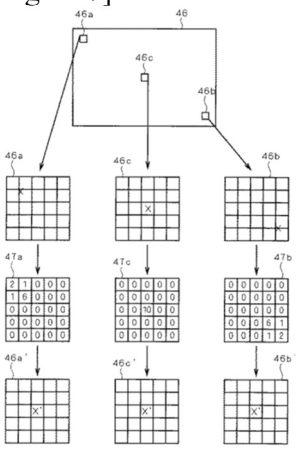
30_2: Filtering unit
40: Coefficient register
41: Convolution calculator

[Figure 4]

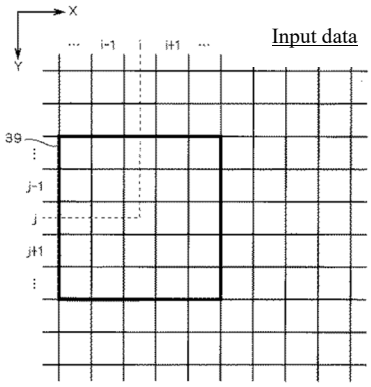
42

γ (0,0)	γ (0,1)	γ (0,2)	γ (0,3)	γ (0,4)
γ (1,0)	γ (1,1)	γ (1,2)	γ (1,3)	γ (1,4)
γ (2,0)	γ (2,1)	γ (2,2)	γ (2,3)	γ (2,4)
γ (3,0)	γ (3,1)	γ (3,2)	γ (3,3)	γ (3,4)
γ (4,0)	γ (4,1)	γ (4,2)	γ (4,3)	γ (4,4)

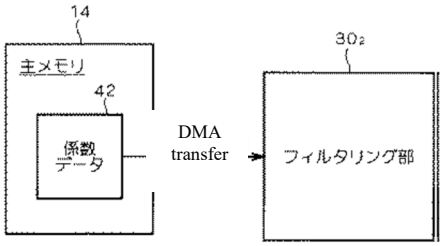
[Figure 7]



[Figure 5]

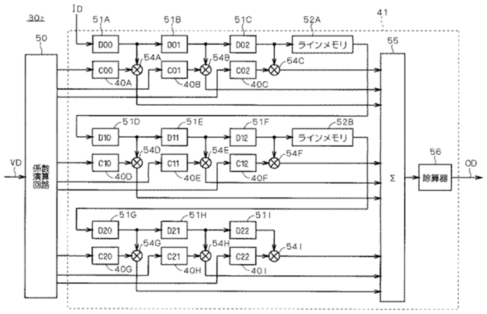


[Figure 6]



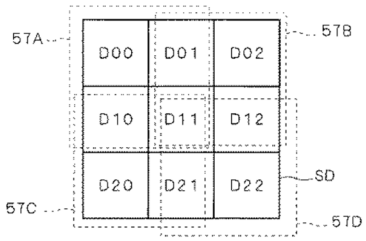
14: Main memory
30_2: Filtering unit
42: Coefficient data

[Figure 8]

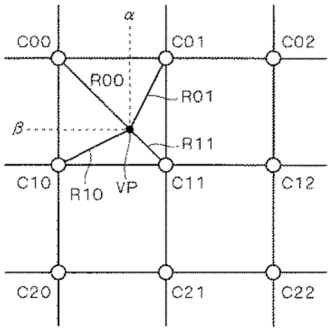


30_2: Filtering unit
41: Convolution calculator
50: Coefficient calculation circuit
52A: Line memory
52B: Line memory
56: Adder

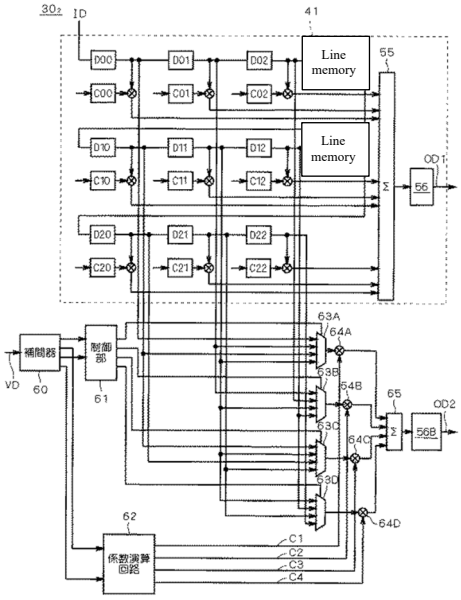
[Figure 9]



[Figure 10]

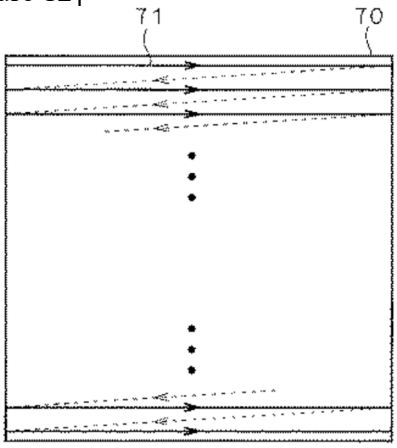


[Figure 11]

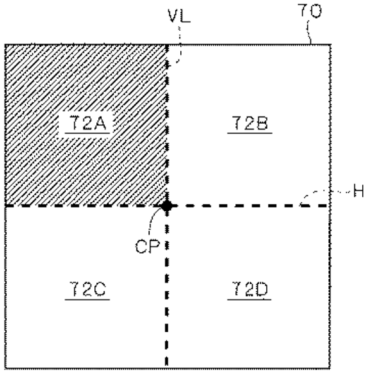


60: Interpolator
61: Control unit
62: Coefficient calculation circuit

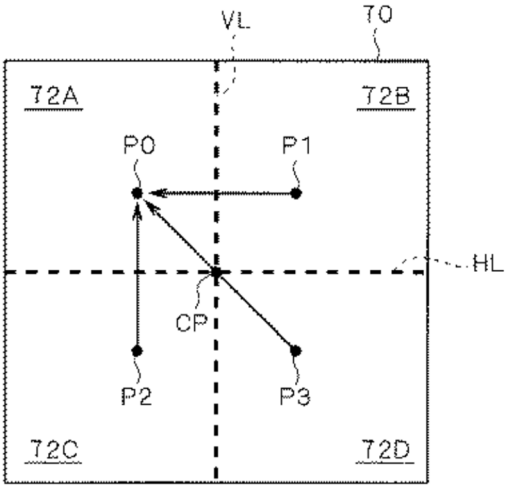
[Figure 12]



[Figure 13]



[Figure 14]



DECLARATION OF JEROME CONWAY

I, Jerome CONWAY, declare the following:

1. I am over 18 years of age and competent to make this declaration.

2. I am a qualified Japanese to English translator with more than 25 years of experience.

3. I have translated into English the attached document identified as "Japanese Unexamined Patent Application Publication No. JP 2004-266768A," bearing a publication date of September 24, 2004.

4. I affirm that the translated text has been translated and edited to the best of my ability and knowledge to accurately reflect the content, meaning, and style of the original text. I hereby certify under penalty of perjury under the laws of the United States of America that the foregoing constitutes, pursuant to my knowledge and belief, a true and correct translation of the original document.

5. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: July 25, 2024

Jerome Conway

Jerome CONWAY