

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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OLYMPUS CORPORATION, OM DIGITAL SOLUTIONS CORPORATION,  
FUJIFILM CORPORATION, FUJIFILM NORTH AMERICA CORPORATION,  
NIKON CORPORATION, PANASONIC ENTERTAINMENT &  
COMMUNICATION CO., LTD.,

Petitioners

v.

OPTIMUM IMAGING TECHNOLOGIES LLC,

Patent Owner

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Case IPR2024-01220

Patent No. 10,873,685

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**PATENT OWNER PRELIMINARY RESPONSE**

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Patent Trial and Appeal Board  
United States Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

| PATENT OWNER’S LIST OF EXHIBITS |                                                                                                                                                                   |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EX. 2001                        | Claim Construction Memorandum Opinion and Order, <i>Optimum Imaging Technologies LLC v. Canon Inc.</i> , No. 2:19-cv-00246-JRG, Dkt. 88 (E.D. Tex. June 11, 2020) |
| EX. 2002                        | U.S. Patent No. 7,612,805 (“the ’805 Patent”)                                                                                                                     |
| EX. 2003                        | U.S. Patent No. 8,451,339 (“the ’339 Patent”)                                                                                                                     |
| EX. 2004                        | Scheduling Order, <i>Optimum Imaging Technologies LLC v. Olympus Corporation et al.</i> , No. 4:23-cv-00924-ALM, Dkt. 41 (E.D. Tex. Oct. 2, 2024)                 |
| EX. 2005                        | Patent Owner Preliminary Response, IPR2024-00923, Paper 7 (PTAB Aug. 29, 2024)                                                                                    |

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**I. INTRODUCTION**

Patent Owner respectfully submits that the Board should deny institution for at least four reasons.

First, instituting this IPR would not be a good use of the Board's resources in view of related proceedings involving Patent No. 10,873,685 ("the '685 Patent").

Second, a POSA would not be motivated to combine the different embodiments of Iwasawa as proposed by Petitioners in their Combined IID.

Third, Petitioners' fail to establish that a POSA would have further modified Petitioners' proposed Combined IID based on the teachings of Enomoto.

Fourth, because Petitioners do not meet their burden in Grounds 1 and 2, Grounds 3-10 also fail.

**II. THE TIMING OF RELATED PROCEEDINGS SHOWS THAT INSTITUTING THIS IPR WOULD NOT BE AN EFFICIENT USE OF THE BOARD'S RESOURCES**

As reflected in Patent Owner's Updated Mandatory Notices (Paper 9), the '685 Patent is involved in multiple parallel district court proceedings and has been challenged by a different petitioner in IPR2024-00923.

The district court scheduling order set a final pretrial conference for October 29, 2025. EX. 2004 at 6. This conference will occur long before a final written

decision would be expected in this IPR in April 2026. All claims of the ‘685 Patent are asserted in the parallel district court proceedings. Additionally, Defendant Samsung Electronics Co., Ltd. has not filed an IPR challenging the ‘685 Patent and may pursue the same Grounds of invalidity as in this IPR. As such, instituting this IPR would not be a good use of the Board’s resources. The validity of the ‘685 Patent should be evaluated in district court.<sup>1</sup>

IPR2024-00923 involving different grounds was instituted on November 18, 2024. A final written decision in IPR2024-00923 will be entered long before a final written decision would be expected in this IPR in April 2026. Because the validity of the ‘685 Patent will already be evaluated by the Board in IPR2024-00923, instituting this IPR would not be a good use of the Board’s resources. This IPR involves ten Grounds and is extremely burdensome for the parties and the

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<sup>1</sup> Based on current law/policy, Patent Owner understands that a *Sotera*-style stipulation precludes discretionary denial under *Fintiv*. See, e.g., Former Director Vidal, Memorandum, ‘Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation’ dated June 21, 2022. If there is an intervening change in law/policy, Patent Owner expressly requests authorization for supplemental briefing to address the *Fintiv* factors in detail.

Board. Patent Owner should not be forced to repeatedly defend the validity of the ‘685 Patent in multiple IPRs.<sup>2</sup>

**III. THE ‘685 PATENT CLAIMS NOVEL AND NON-OBVIOUS SYSTEMS FOR CORRECTING ABERRATIONS IN A DIGITAL VIDEO CAMERA**

The ‘685 Patent claims systems that perform in-camera aberration correction using novel and non-obvious combinations of hardware and software. EX. 1001 at Abstract (“A system is disclosed for the automated correction of optical and digital aberrations in a digital imaging system.”)

“Though every major advance in photography has solved an important problem, there are still remaining photographic problems to be solved in order to

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<sup>2</sup> Based on current law/policy, Patent Owner understands that multiple petitions filed by different parties without a “significant relationship” precludes discretionary denial under *General Plastic*. See, e.g., *Videndum Production v. Rotolight*, IPR2023-01218, Paper 12 at 6 (PTAB Apr. 19, 2024). If there is an intervening change in law/policy or in facts/circumstances, Patent Owner expressly requests authorization for supplemental briefing to address the *General Plastic* factors and relevant facts/circumstances in detail.

meet the goals of *optimizing optical imaging quality* while *increasing simplicity and efficiency* and *lowering cost*.” EX. 1001 at 3:19-23 (emphasis added).

“The present system dramatically improves image quality. This digital imaging system eliminates, or minimizes, post-production processes. In addition, the system presents substantial cost savings as well as time savings relative to existing digital imaging systems because of the automation of integrated in-camera optical and digital corrections of aberrations.” EX. 1001 at 7:23-29.

To achieve the advantages described in the specification, the independent claims of the ‘685 Patent recite, *inter alia*, “a digital video camera”, “in-camera software”, “an integrated circuit”, “a digital signal processor”, and “a database management system”.

As claimed, “at least one optical image aberration” is identified by using the integrated circuit and the in-camera software. The database contains a “plurality of optical image aberration corrections”. Thus, the system can identify the specific aberrations and the specific solution for each aberration. The aberration is then corrected by the digital signal processor.

As explained in the ‘685 Patent, “[t]his in-camera corrective feature provides a powerful tool to rapidly manipulate an image without using post-production editing software tools.” EX. 1001 at 16:34-36.

The '685 Patent includes 30 claims, with claims 1, 6, and 14 being independent. Exemplary independent claim 1 is set forth below:

| <b>Claim 1<sup>3</sup></b> |                                                                                                                                                                                                                                                                                                                                                            |
|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1[pre]                     | A digital imaging system for correcting optical image aberrations in a digital video, comprising:                                                                                                                                                                                                                                                          |
| 1[a]                       | a digital video camera including in-camera software, an optical lens mechanism, at least one digital sensor for capturing the digital video, an integrated circuit including; a digital signal processor configured to access a database management system including a plurality of optical image aberration corrections, and a memory storage sub-system; |
| 1[b]                       | wherein the optical lens mechanism is a zoom lens or a fixed focal length lens;                                                                                                                                                                                                                                                                            |
| 1[c]                       | wherein the integrated circuit uses the in-camera software to identify at least one optical image aberration and to correct the at least one optical image aberration in at least one frame of the digital video using at least one of the plurality of optical image aberration corrections in the database;                                              |
| 1[d]                       | wherein the video is captured by the at least one digital sensor and is forwarded to the digital signal processor;                                                                                                                                                                                                                                         |
| 1[e]                       | wherein the video image file with the at least one optical image aberration is corrected by applying digital filtration using the digital signal processor; and                                                                                                                                                                                            |
| 1[f]                       | wherein the corrected video consisting of the digital data optimized from the at least one optical image aberration that are corrected from the original video image is stored in the memory storage sub-system.                                                                                                                                           |

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<sup>3</sup> Patent Owner uses the same annotations (*e.g.*, 1[pre], 1[a], etc.) as the petition for consistency. Petition at 83.

**A. PERSON OF ORDINARY SKILL IN THE ART (“POSA”)**

Petitioners propose a POSA would have had “a bachelor’s degree in electrical engineering, physics, or a related field, with at least two years of industry experience and/or research, both concerning digital camera system design and image processing.” Petition at 4.

In construing terms of the related ‘339 and ‘805 Patents<sup>4</sup>, the district court found that a POSA would have had “an electrical engineering degree and three years of relevant experience”. EX. 2001 at 6.

Patent Owner submits that the district court’s definition of a POSA should be adopted for purposes of determining institution. Patent Owner reserves all rights regarding the correct definition of a POSA.

**B. CLAIM CONSTRUCTION**

Petitioners identify no terms/phrases for construction. Petition at 4. Patent Owner does not believe that any constructions are necessary for purposes of

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<sup>4</sup> The ‘685 Patent, U.S. Patent No. 7,612,805 (“the ‘805 Patent,” EX. 2002), and U.S. Patent No. 8,451,339 (“the ‘339 Patent,” EX. 2003) issued from related continuation applications and claim priority to the same provisional application, No. 60/807,065 filed July 11, 2006.

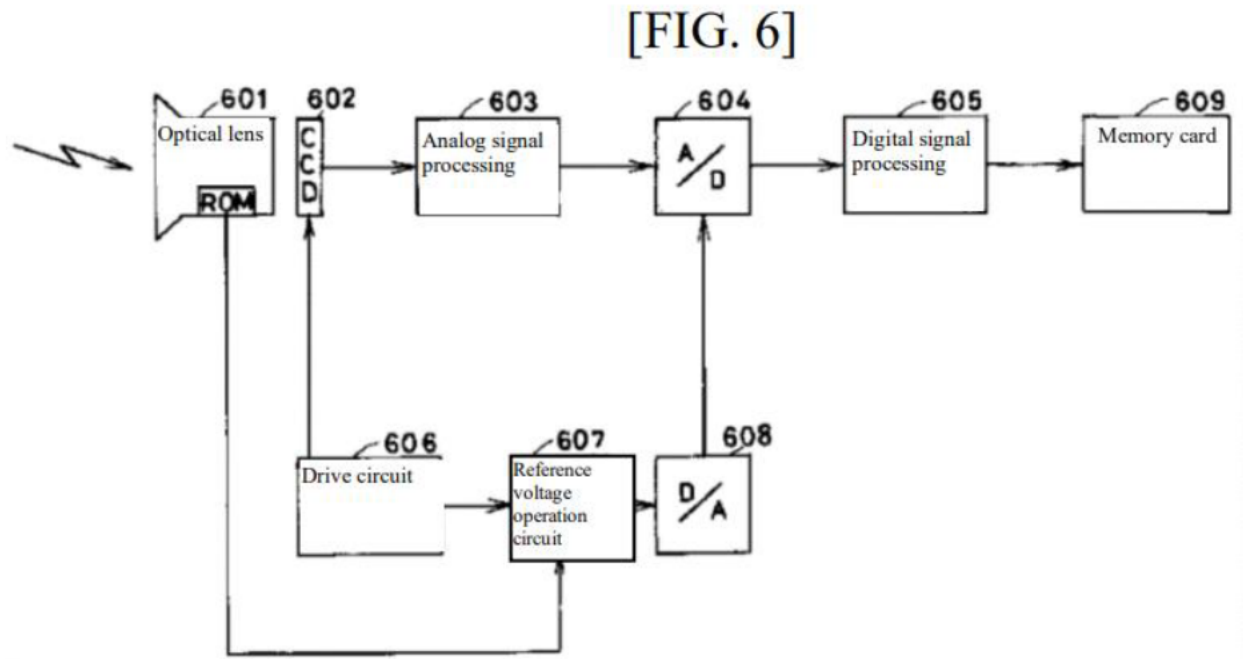
determining institution. Patent Owner reserves all rights regarding the correct constructions of terms/phrases in the '685 Patent.

#### IV. **GROUND 1: IWASAWA FAILS**

| Ground | Reference(s) | Claim(s)                   |
|--------|--------------|----------------------------|
| 1      | Iwasawa      | 1, 3, 6, 11-14, 17, and 19 |

##### A. SUMMARY OF IWASAWA

Iwasawa discloses a prior art image input device (“IID”) in FIG. 6. EX. 1005 at [0002].



EX. 1005, FIG. 6.

The prior art IID of FIG. 6 includes “an optical lens 601 storing a shading correction coefficient” and a CCD sensor 602. EX. 1005 at [0002], FIG. 6. The drive circuit 606 generates pulses for driving the CCD 602 and generates an

address signal. *See id.* The reference voltage operation circuit 607 reads the shading correction coefficient from the optical lens 601 and the address signal from the drive circuit 606 in order to calculate a digital reference voltage for each pixel. *See id.* The D/A converter 608 converts the digital output from the reference voltage operation circuit 607 to an analog amount and provides the analog reference voltage to the A/D converter 604. *See id.*

The analog signal processing circuit 603 performs correlated double sampling, signal amplification, etc. on the analog output from the CCD 602. *See id.* The A/D converter 604 converts the analog signal output from the analog signal processing circuit 603 into a digital value for each pixel. *See id.*

The digital signal processing circuit 605 synchronizes the different color information to obtain a video signal. *See id.*; *see also* EX. 1005 at [0024].

Thus, Iwasawa discloses prior art shading correction is performed by applying a calculated reference voltage for each pixel to the A/D converter. *See* EX. 1005 at [0003].<sup>5</sup>

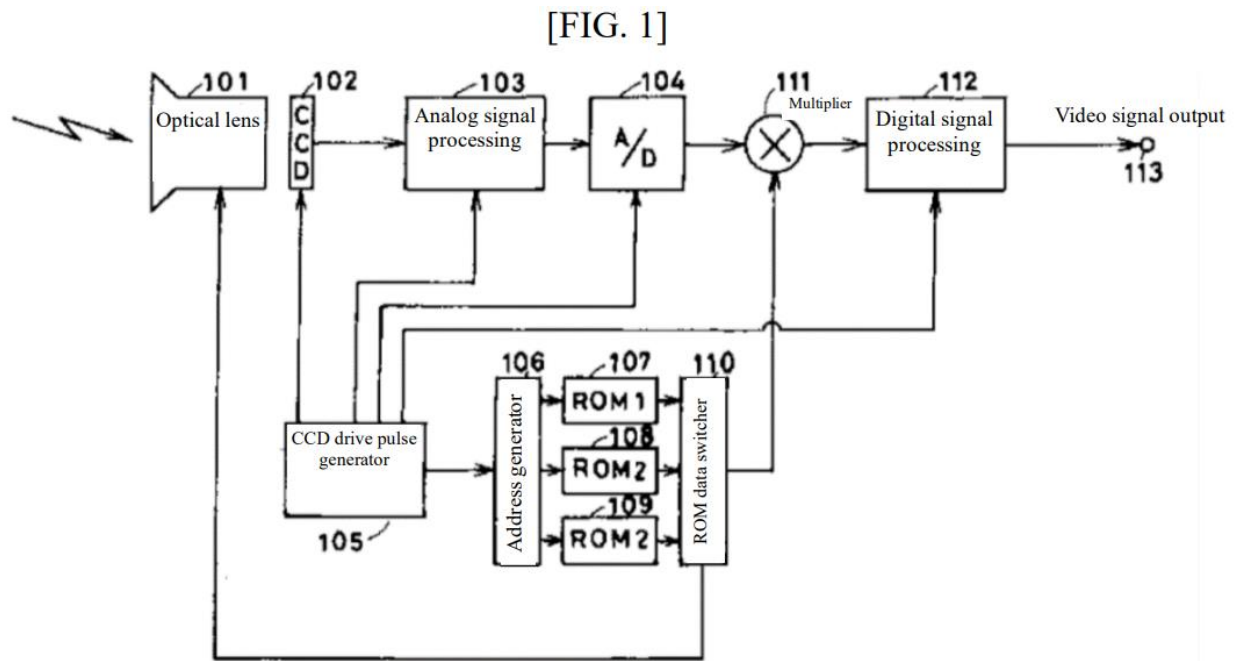
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<sup>5</sup> This disclosure is unusual in that a POSA would have understood that, typically, correlated double sampling is used to subtract the reference voltage of the pixel from the signal voltage of the pixel. Iwasawa discloses that analog signal processing circuit 603 performs correlated double sampling. However, Iwasawa

Unlike the prior art, Iwasawa discloses various embodiments of IIDs that will multiply the digital signal output of the A/D converter and the shading correction data. EX. 1005 at [0006].

### ***1. First Embodiment IID of FIG. 1***

The first embodiment IID of Iwasawa includes “an optical lens 101 capable of outputting one or more control signals of an aperture value, a zoom position, and a lens type” and a CCD sensor 102. EX. 1005 at [0015], FIG. 1.



discloses the analog reference voltage is provided to the A/D converter 604, not the analog signal processing circuit 603.

EX. 1005, FIG. 1.

The CCD drive pulse generator 105 generates pulses for driving the CCD 102. EX. 1005 at [0015], FIG. 1. The analog signal processing circuit 103 performs correlated doubling sampling, signal amplification, etc. on the analog output from the CCD 102. *See id.* The A/D converter 104 converts the analog signal output from the analog signal processing circuit 103. *See id.* The multiplier 111 performs a multiplication operation on the digital value for each pixel. *See id.*

To perform shading correction for each pixel, the address generator 106 generates an address synchronized with the pulse output from the CCD drive pulse generator 105. EX. 1005 at [0016].<sup>6</sup>

As shown in FIG. 1, the output from the address generator 106 is used to access shading correction data stored in ROMs 107-109. The output from the address generator 106 allows for “shading correction corresponding to the position of the screen” which a POSA would understand as permitting shading correction on a pixel-by-pixel basis. *See* EX. 1005 at Abstract.

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<sup>6</sup> Thus, CCD drive pulse generator 105 of FIG. 1 is different from the prior art drive circuit 606 of FIG. 6. Unlike the CCD drive pulse generator 105 of FIG. 1, the prior art drive circuit 606 of FIG. 6 also generates an address signal.

ROM 107, ROM 108, and ROM 109 store shading correction data “in advance” corresponding to the aperture value, the zoom position, and the lens type. EX. 1005 at [0016], [0017]. The ROM data switcher is a switching means to switch among ROMs 107-109. *See, e.g.*, EX. 1005 at claim 1, [0016].

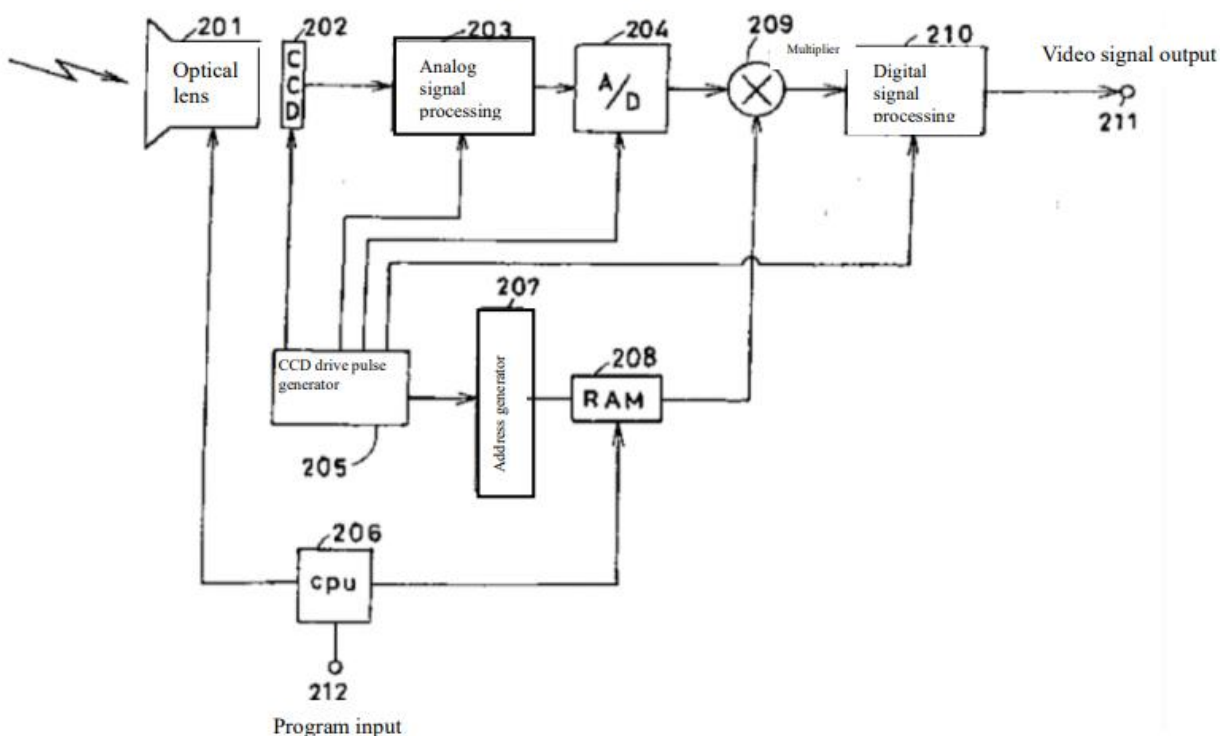
The ROM data switcher 110 uses the control signal to select the “optimal shading correction data”. EX. 1005 at [0016], FIG. 1. The optimal shading correction data is input to the multiplier 111. EX. 1005 at [0016]. The multiplier 111 multiplies the optimal shading correction data and the digital signal output from the A/D converter 104. EX. 1005 at [0016], [0017].

The digital signal processing circuit 112 is not involved in shading correction; rather, the digital signal processing circuit 112 synchronizes the digital signal output for each different color signal and obtains a video signal. EX. 1005 at claim 1, [0015].

## ***2. Second Embodiment IID of FIG. 2***

The second embodiment of Iwasawa differs from the first embodiment of Iwasawa. The second embodiment replaces ROMs 107-109 and ROM data switcher 110 with RAM 208 and CPU 206. EX. 1005 at [0019].

[FIG. 2]



EX. 1005, FIG. 2.

As disclosed in Iwasawa, the CPU 206 calculates shading correction data using a control signal from the optical lens 201 and writes the calculated shading correction data to RAM 208. EX. 1005 at [0019]. RAM 208 is a rewritable recording means. EX. 1005 at [0019].

The calculated shading correction data is read out from the RAM 208 and used by the multiplier 209 to multiply the calculated data and the digital signal output from the A/D converter 204. EX. 1005 at [0020].

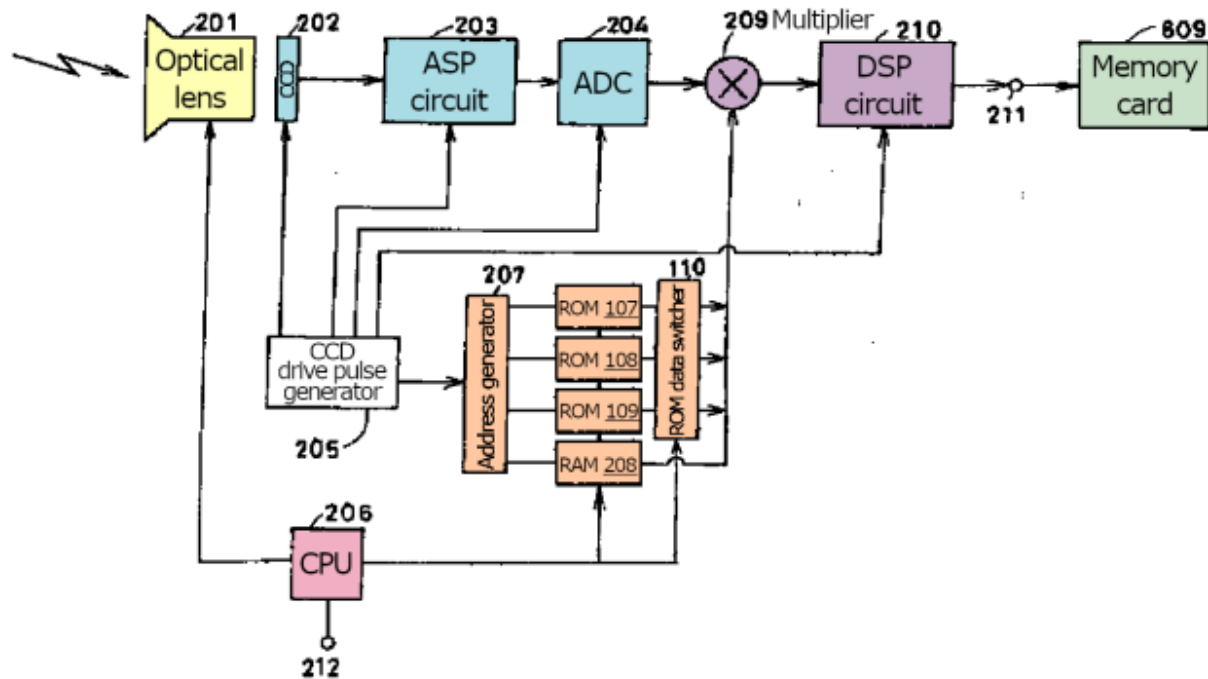
The digital signal processing circuit 210 is not involved in shading correction; rather, the digital signal processing circuit 210 synchronizes the digital

signal output for each different color signal and obtains a video signal. See EX.

1005 at [0021].

## B. PETITIONERS' PROPOSED COMBINED IID IS REplete WITH HINDSIGHT BIAS

Petitioners' analysis relies on their proposed "Combined IID". Petitioners' proposed Combined IID primarily relies on the second embodiment IID of Iwasawa and adds (i) ROMs 107-109 of the first embodiment IID, (ii) ROM data switcher 110 of the first embodiment IID, and (iii) memory card 609 of the prior art IID. Petition at 5-6.



Combined IID.

Petition at 6.

Petitioners’ proposed Combined IID is replete with hindsight bias and uses the claims of the ‘685 Patent as a roadmap. For at least this reason, institution should be denied. *See Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) (“[W]e cannot allow hindsight bias to be the thread that stitches together prior art patches into something that is the claimed invention.”); *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1351 (Fed. Cir. 2014) (criticizing use of the challenged patent as a “roadmap” for putting what the expert referred to as “pieces of a ‘jigsaw puzzle’” together).

**C. A POSA WOULD NOT HAVE BEEN MOTIVATED TO MAKE THE COMBINED IID AS PROPOSED BY PETITIONERS**

***1. A POSA would not have been motivated to add ROMs 107-109 to the second embodiment IID.***

Petitioners argue that “Iwasawa expressly discloses that the IID of Figure 2 could be modified to include ROMs 107-109, with or without the ROM data switcher 110.” Petition at 7-8 (citing EX. 1005 at [0019]). There is nothing in paragraph 19 of Iwasawa to support Petitioners’ argument for adding ROMs 107-109, let alone adding ROMs 107-109 with or without the ROM data switcher 110.

Because the second embodiment IID already includes RAM 208, a POSA would not have been motivated to also add ROMs 107-109. A POSA would not have been motivated to include more circuits at least because it would have been an inefficient use of limited real-estate in the camera and an unnecessary expense.

A POSA also would have understood that using more circuits uses more power. Therefore, a POSA would not have been motivated to add ROMs 107-109 to the second embodiment IID at least because it would have been an inefficient use of space and of limited power/battery life in the camera.

A POSA also would have understood that including a plurality of ROMs means storing a large amount of correction data, which also results in larger circuit size, more circuits, and higher costs. As such, a POSA would not have been motivated to add ROMs 107-109 to the second embodiment IID.

Petitioners argue that “the use of prestored correction data” for existing lenses stored in ROMs 107-109 would have been advantageous in the second embodiment IID. *See* Petition at 8-9. However, the prestored programs in CPU 206 for calculating shading correction data correspond to existing lenses. The CPU 206 calculates the shading correction data and writes the data to RAM 208. If a new lens is used, the *programs* in CPU 206 would need to be updated. EX. 1005 at [0021].

The second embodiment IID of Iwasawa highlights one of the problems the ‘685 Patent was designed to avoid. The prior art was heavily dependent on CPU-intensive processes that require more processing power. Instead, the claimed inventions of the ‘685 Patent efficiently distribute the workload among the claimed components and use, *inter alia*, an updatable database including a plurality of

optical image aberration corrections.<sup>7</sup> The ‘685 Patent explains that the updatable database is a “particularly important” feature to both the manufacturer and the user when, for example, a new lens is used. EX. 1001 at 29:22-26.

ROMs 107-109 are not updatable and a POSA would not have been motivated to add ROMs 107-109 to the second embodiment IID of Iwasawa. As discussed, *infra*, Iwasawa does not disclose any way to determine whether to use RAM 208 versus ROMs 107-109. A POSA would not be motivated to require such a determination given that the prestored programs in CPU 206 and the prestored data in ROMs 107-109 both correspond to existing lenses.

***2. RAM 208 is not a means that can be selected using the control signal output from the optical lens 201.***

Petitioners argue that “Iwasawa also states that the RAM 208 is a means that can be selected using the control signal output from the optical lens 201.” Petition at 25 (citing EX. 1005 at [0019]). There is nothing in paragraph 19 of Iwasawa to

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<sup>7</sup> In IPR2024-00923, Patent Owner made clear that the claimed “database” in the ‘685 Patent is updatable which amounts to prosecution history disclaimer. EX. 2005 at 36-37; *CUPP Computing AS v. Trend Micro Inc.*, 53 F.4th 1376, 1383 (Fed. Cir. 2022)(“To be clear, a disclaimer in an IPR proceeding is binding in later proceedings, whether before the PTO or in court.”).

support Petitioners' argument. Paragraph 19 of Iwasawa describes the second embodiment IID of FIG. 2. This disclosure makes clear that CPU 206 stores programs for existing lenses, uses the control signal to calculate the shading correction data, and writes this data to RAM 208. There is no selection of RAM 208 using the control signal.

***3. A POSA would not have been motivated to store correction data “in advance” in RAM 208.***

Regarding the first embodiment IID of FIG. 1, Iwasawa discloses correction data is stored “in advance” in ROMs 107-109. EX. 1005 at [0016]. Petitioners' expert agrees that ROM refers to read-only memory. EX. 1003 at ¶63. A POSA would have understood that ROM is non-volatile and thus retains data without power. A POSA also would have understood RAM is temporary memory storage that is volatile, meaning that data is lost without power. As such, given the differences between ROM and RAM, a POSA would not have been motivated to store correction data “in advance” in RAM 208 of the second embodiment IID. Instead, consistent with the disclosure of the second embodiment IID, the CPU 206 calculates shading correction data and temporarily stores this data in RAM 208. Data is easily rewritten to RAM 208 for different calculations.

Moreover, adding correction data for a manufacturer's existing lens types in a portion of RAM 208 would have to be done each time the camera starts up,

which increases the amount of time for start-up and photographing. This would also require significant processing power for the CPU to perform calculations for each aperture value, zoom position, and existing lens type. Therefore, a POSA would not have been motivated to store correction data “in advance” in a portion of RAM 208. *Contra* Petition at 8.

***4. A POSA would not have been motivated to switch among RAM 208 and ROMs 107-109 to read out correction data.***

The first embodiment IID includes ROM data switcher 110 to switch among ROMs 107-109 to select “optimal shading correction data”. EX. 1005 at [0016].

The second embodiment IID includes CPU 206 which calculates the shading correction data and writes the data to RAM 208.

In Petitioners’ proposed Combined IID, the CPU 206 would still calculate the shading correction data based on the control signal. Petitioners argue that the CPU 206 could calculate correction data “as necessary” (Petition at 8), but Petitioners do not describe how Iwasawa’s system would be modified to accomplish doing so.

Iwasawa discloses “CPU 206 has a program for calculating shading correction data in response to a control signal from the optical lens 201.” EX. 1005 at [0019]. The petition does not address how that program would be modified or

what factors would determine whether the CPU 206 performs its own calculation or uses prestored correction data in ROMs 107-109.

Additionally, because the second embodiment IID includes CPU 206 and RAM 208, the second embodiment IID provides “high-speed and accurate shading correction”. EX. 1005 at [0010]. A POSA would have been motivated to use the second embodiment CPU 206 and RAM 208 to calculate, store, and input shading correction data to the multiplier 209. There is no reason for a POSA to include ROMs 107-109 for prestored shading correction data. Doing so would have required larger circuit size, more circuits, and increased costs.

Moreover, because CPU 206 calculates the shading correction data and writes the calculated data to RAM 208, there is no need for a ROM data switcher 110 to select the optimal shading correction data. The calculated shading correction data stored in RAM 208 is the optimal shading correction data. Therefore, a POSA would not have been motivated to include ROM data switcher 110 in the second embodiment IID.

Also, there would have been no motivation to incorporate the functionality of ROM data switcher 110 into CPU 206. There is nothing in Iwasawa to suggest that ROM data switcher 110 would determine whether to switch among ROMs 107-109 and RAM 208. The petition does not explain otherwise. Petitioners simply argue that CPU 206 embodying the functionality of ROM data switcher 110

would allow CPU 206 to access ROMs 107-109 (Petition at 9-10). However, Petitioners do not explain how CPU 206 embodying the functionality of ROM data switcher 110 would inform any determination as to using ROMs 107-109 versus RAM 208. As discussed above, the second embodiment IID does not require this determination because the calculated shading correction data stored in RAM 208 is the optimal shading correction data.

***5. There is no need for a POSA to modify the second embodiment IID in order to support both new and existing lenses.***

Petitioners argue that the Combined IID is advantageous because it is “provides the advantages of both allowing fast access to correction data for a set of known lenses and efficient calculation of correction data when a new lens is adopted.” Petition at 9.

However, the second embodiment IID already provides this benefit. Therefore, there is no reason for a POSA to modify the second embodiment IID to achieve this benefit.

The CPU 206 has a program for calculating shading correction data in response to a control signal from the optical lens 201, and further has a program input 212 that can input a program from the outside. EX. 1005 at [0019]. Thus, CPU 206 of the second embodiment IID can calculate shading correction data for

existing lenses and receive updated program information to calculate shading correction data for new lenses. There is no reason to modify the second embodiment IID as proposed by Petitioners.

Also, as discussed above, it is the updated programs in CPU 206 that support new lenses. Iwasawa's heavy reliance on the CPU 206 in the second embodiment IID is contrary to the claimed inventions of the '685 Patent which instead use an updatable database to support new lenses.<sup>8</sup>

***6. Petitioners take Iwasawa's disclosure out of context.***

Petitioners argue that "Iwasawa discloses several elements in Figure 2's embodiment are 'the same as the first embodiment'... Iwasawa also refers to the first and second embodiments as operating in the same manner." Petition at 8.

Iwasawa expressly discloses that the first and second embodiments include different elements regarding ROMs107-109 / ROM data switcher 110 versus RAM 208/ CPU 206, respectively. EX. 1005 at [0019]. Just because the other elements of the IID may operate in a similar manner in the first and second embodiments, *e.g.*, the CCD, A/D converter, CCD drive pulse generator, address generator, multiplier, and digital signal processing circuit (EX. 1005 at [0021]), the functionality

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<sup>8</sup> As noted above, ROMs 107-109 are not updatable.

attributed to the different elements means that the first and second embodiments as a whole do not operate in the same manner. As conceded by Petitioners' expert, "the ROMs 107-109 and ROM data switcher 110 serve a different purpose as compared to CPU 206 and RAM 209 [sic – 208]." EX. 1003 at ¶ 77.

## **V. GROUND 2: IWASAWA + ENOMOTO FAILS**

| <b>Ground</b> | <b>Reference(s)</b> | <b>Claim(s)</b>                                |
|---------------|---------------------|------------------------------------------------|
| 2             | Iwasawa + Enomoto   | 1-3, 5-7, 10-15, 17-19, 23, 24, 27, 28, and 30 |

Petitioners rely on their analysis of their proposed Combined IID in Ground 1 in Ground 2. Petition at 49 (citing section 4.1.3). Petitioners only rely on Enomoto for its alleged disclosure of correcting a "plurality" of optical image aberrations. Petition at 46-49. For at least the reasons discussed above with respect to Ground 1, Ground 2 also fails.

Additionally, given the storage size, circuit size, and cost associated with Petitioners' proposed Combined IID, a POSA would not have been motivated to include additional correction methods taught by Enomoto. *Contra* Petition at 47.

Moreover, Petitioners argue that a POSA would have been motivated to add the aberration correction data used by characteristic correction unit 36 of Enomoto into the RAM 208 and/or ROMs 107-109 of Petitioners' proposed Combined IID for use by multiplier 209. Petition at 49; *see also* Petition at 48 (directly comparing

Enomoto's characteristic correction unit 36 and Iwasawa's multiplier 209).

Petitioners' argument fails for at least four reasons.

First, Enomoto does not disclose prestored "correction data" like Iwasawa. Enomoto discloses a correction *process* using characteristic correction unit 36. Petitioners do not explain how this *process* could be stored as data in RAM 208 and/or ROMs 107-109.

Second, there is no disclosure in Iwasawa that would suggest multiplier 209 would be capable of embodying the functionality of Enomoto's characteristic correction unit 36. Multiplier 209 simply performs a multiplication operation. The same is not true for Enomoto's characteristic correction unit 36.

Third, Petitioners do not explain how their proposed combination of Iwasawa and Enomoto would perform shading correction, chromatic aberration, and distortion aberration. Enomoto teaches that when performing separate corrections, "the calculation takes a long time and an interpolating calculation needs to be done a plurality of times so that there arises a problem that the image quality might be deteriorated." EX. 1006 at 4:51-57. For at least this reason, a POSA would not be motivated to combine Iwasawa and Enomoto as proposed.

Fourth, to avoid the aforementioned problems discussed directly above, Enomoto teaches methods that, *inter alia*, "calculate the deviation quantities  $\Delta r$  and  $\Delta b$  of the pixel values  $i_r$  and  $i_b$  of the R- and B- image data from the G-image data

ig,” “calculate the deviation quantity D of the input G-image data ig,” correct the R and B images with the G image as a basis, and perform interpolation. *See, e.g.*, EX. 1006 at 5:9-6:10. However, Petitioners do not address these methods. Petitioners do not propose, for example, incorporating Enomoto’s coordinate transformation processing unit 36a or Enomoto’s interpolation processing unit 36b in Petitioners’ proposed Combined IID. *See* EX. 1006, FIG. 2; Petition at 46-49. There is also nothing to suggest that Iwasawa’s multiplier 209 is capable of embodying the functionality of Enomoto’s coordination transformation processing unit 36a or Enomoto’s interpolation processing unit 36b.

Overall, Petitioners fail to explain *how* the methods taught by Enomoto actually work or *why* a POSITA would have been motivated to implement the specific methods in Petitioners’ proposed Combined IID. “[A] clear, evidence supported account of the contemplated workings of the combination is a prerequisite” to concluding “that a relevant skilled artisan would have been motivated to make the combination and reasonably expect success in doing so.” *Personal Web Techs., LLC v. Apple*, 848 F.3d 987, 994 (Fed. Cir. 2017).

## VI. ALL GROUNDS NECESSARILY FAIL

Because Grounds 1 and 2 are the only grounds addressing the independent claims, and because Grounds 1 and 2 fail for at least the reasons discussed above,

Grounds 3-10 addressing the dependent claims also fail. Patent Owner reserves all rights to fully address all arguments and all Grounds if this IPR is instituted.

**VII. CONCLUSION**

For at least the reasons set forth herein, Patent Owner respectfully requests that institution be denied.

Respectfully submitted,

Date: January 13, 2025

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**CERTIFICATE OF COMPLIANCE**

This Patent Owner Preliminary Response (“POPR”) consists of 4,735 words, which is no more than 14,000 words, excluding table of contents, table of authorities, certificate of service, this certificate, or table of exhibits. The POPR complies with the type-volume as mandated in 37 C.F.R. § 42.24. In preparing this certificate, counsel has relied on the word count of the word-processing system used to prepare the paper (Microsoft Word).

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**CERTIFICATE OF SERVICE**

Pursuant to 37 C.F.R. § 42.6(e), the undersigned hereby certifies the PATENT OWNER PRELIMINARY RESPONSE and all exhibits thereto were served on the undersigned date via email, as authorized by Petitioners, at the following email addresses:

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