

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.,
Petitioner,

v.

PICTIVA DISPLAYS INTERNATIONAL LTD.,
Patent Owner.

Case No. IPR2024-01222
Patent No. 6,949,389

**DECLARATION OF VIVEK SUBRAMANIAN, PH.D. IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 6,949,389**

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1. Dependent Claim 37: “The method as recited in claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing an organic layer through a shadow mask.” 117

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1. I, Vivek Subramanian, have been retained by counsel for Petitioner Samsung Display Co, Ltd. to provide my expert opinions concerning the patentability of certain claims of U.S. Patent No. 6,949,389 (“’389 patent”). For the reasons discussed below, it is my opinion that claims 34-37 and 40-46 of the ’389 patent would have been obvious to a person of ordinary skill in the art.

I. BACKGROUND AND QUALIFICATIONS

2. I summarize in this section my educational background, career history, publications, and other relevant qualifications. My full curriculum vitae is attached as Appendix A to this declaration.
3. I am currently a Professor of Electrical and Microengineering at Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland and director of the micromanufacturing science and engineering research center. I moved to EPFL in 2018. I was previously a professor at the University of California, Berkeley for almost 20 years, and am still maintaining an adjunct professorship appointment there while I graduate my remaining PhD students. I am also founder of Locix, Inc., of San Bruno, California, a privately held company that develops wireless sensors for industrial commercial applications. I also previously served as a founding technical advisor for Kovio, Inc. which developed thin film transistor technology for various applications, including RFID tags and displays.

4. I received a Ph.D. in electrical engineering from Stanford University in 1998. I received my MS in electrical engineering from Stanford in 1996, and my BS in electrical engineering from Louisiana State University, Baton Rouge, in 1994. My PhD thesis was specifically focused on the development of technology for displays. During my PhD, I was the recipient of an Eastman Kodak fellowship. As part of this award, I worked closely with Kodak on their OLED technology.
5. After completing my Ph.D., I held multiple jobs simultaneously. First, I was a founder and member of technical staff of Matrix Semiconductor (“Matrix”), which developed high density memory. We founded Matrix in 1997, and I maintained a full-time role through 2000, at which point I transitioned to an advisory role. Matrix was acquired by Sandisk in 2005, at which point my affiliation with Matrix ended. Between 1998 and 2000, I was also a visiting research engineer at the University of California, Berkeley, where I performed research on high-performance transistors and process technology. In that same period, I was also a consulting assistant professor at Stanford University, where I performed research on 3D integration of transistors, among other topics. In 2000, I was offered a professorship at Berkeley, and moved there full time. I received tenure in 2005, and became a full professor in 2011. In 2018, I was awarded with a Chancellor’s professorship. In 2018, I also accepted a position at

EPFL, and between 2018 and 2020, I maintained dual appointments at Berkeley and EPFL while I completed my move.

6. My professional career has been focused heavily on semiconductor and display technology, and I have been actively involved in the development of process technology for displays for a large part of my professional career, both in academia and in industry. I have specifically been involved in the development of thin film transistor technology for displays, development of materials and processes for OLEDs, and development of printing technology for display fabrication. I have also specifically worked on planarization technology and on encapsulation technology for organic display materials. Additionally, I have worked on both printing-based and vacuum-based selective deposition technologies for displays.
7. I have authored or co-authored more than 200 publications in journals and major international conference proceedings, many of which are specifically related to displays and the associated thin film technologies.

II. MATERIALS CONSIDERED

8. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the alleged invention.

9. In addition, I have considered the materials referenced herein, including each of the following:

Exhibit No.	Description
1001	U.S. Patent No. 6,949,389 (“389 patent”)
1002	Certified File History for U.S. Patent No. 6,949,389
1003	Declaration of Vivek Subramanian, Ph.D. (Yamazaki and Weaver grounds)
1004	Declaration of Vivek Subramanian, Ph.D. (Kijima grounds)
1005	U.S. Patent Application Publication No. 2003/0206332 (“Yamazaki”)
1006	U.S. Patent Application Publication No. 2001/0052752 (“Ghosh”)
1007	U.S. Patent Application Publication No. 2003/0011300 (“Palanisamy”)
1008	U.S. Patent Application Publication No. 2002/0140347 (“Weaver”)
1009	U.S. Patent No. 6,866,901 (“Burrows”)
1010	Japanese Published Application No. H09-245964, certified translation (“Kijima”)
1011	Japanese Published Application No. H09-245964, original document
1012	U.S. Patent No. 6,198,217 (“Suzuki”)
1013	U.S. Patent No. 6,087,196 (“Sturm”)
1014	Japanese Published Application No. H10-41069, certified translation (“Fujimori”)
1015	Japanese Published Application No. H10-41069, original document
1016	International Publication No. WO 2001/08242 (“Duthaler”)
1017	U.S. Patent No. 6,660,409 (“Komatsu”)
1018	J. Birnstock et al., <i>Screen-Printed Passive Matrix Displays Based on Light-Emitting Polymers</i> , 78 Appl. Phys. Lett. 3905 (2001) (“Birnstock”)
1019	Complaint, <i>Pictiva Displays Int’l Ltd. v. Samsung Elecs. Co., Ltd., et al.</i> , 2:23-cv-00495-JRG (E.D. Tex. Oct. 19, 2023)
1020	U.S. Patent Application Publication No. US 2003/0062186 (“Boroson”)
1021	U.S. Patent No. 6,770,502 (“Cok”)

Exhibit No.	Description
1022	U.S. Patent No. 6,214,631 (“Burrows-631”)
1023	Jun Hyung Souk, <i>Advances and New Challenges in LCD</i> , International Meeting on Information Display Digest, 24 (2002) (“Souk”)
1024	<i>OLED Fundamentals: Materials, Devices, and Processing of Organic Light-Emitting Diodes</i> (Daniel J. Gaspar & Evgueni Polikarpov eds., 1st ed. 2015) (excerpted) (“Gaspar”)
1025	Takashi Ohta, <i>Next Generation AMLCD Production Technologies for Large Substrate</i> , International Meeting on Information Display Digest, 3 (2001) (“Ohta”)

III. RELEVANT LEGAL STANDARDS

10. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to forming my opinions. I have applied the following understanding of the law:

11. Petitioner’s counsel has informed me that a patent claim is “anticipated” if each element of that claim is present either explicitly or inherently in a single prior art reference, with the elements arranged in the reference in the same manner as in the claim. Petitioner’s counsel has informed me that for a claimed limitation to be inherently present, the prior art need not expressly disclose the limitation, so long as the claimed limitation necessarily flows from a disclosure in the prior art.

12. Petitioner’s counsel has informed me that a patent claim is “obvious” if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a person of ordinary skill in the art at the time the application was filed. I have been informed whether a claim would have

been obvious involves consideration of (1) the level of ordinary skill in the art at the time the application was filed, (2) the scope and content of the prior art, (3) what differences, if any, existed between the claimed invention and the prior art, and (4) any secondary considerations of nonobviousness.

13. Petitioner's counsel has informed me that a single reference can render a patent claim obvious if any differences between that reference and the claim would have been obvious to a person of ordinary skill in the art. Alternatively, a claim can be rendered obvious where the teachings of two or more references may be combined in the same way as disclosed in the claim, if such a combination would have been obvious to one having ordinary skill in the art. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider, among other factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, and when combined, would yield predictable results;
- whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;

- whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent;
- whether the innovation would have been obvious to try, i.e., involving a choice from a finite number of identified, predictable solutions, with a reasonable expectation of success; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

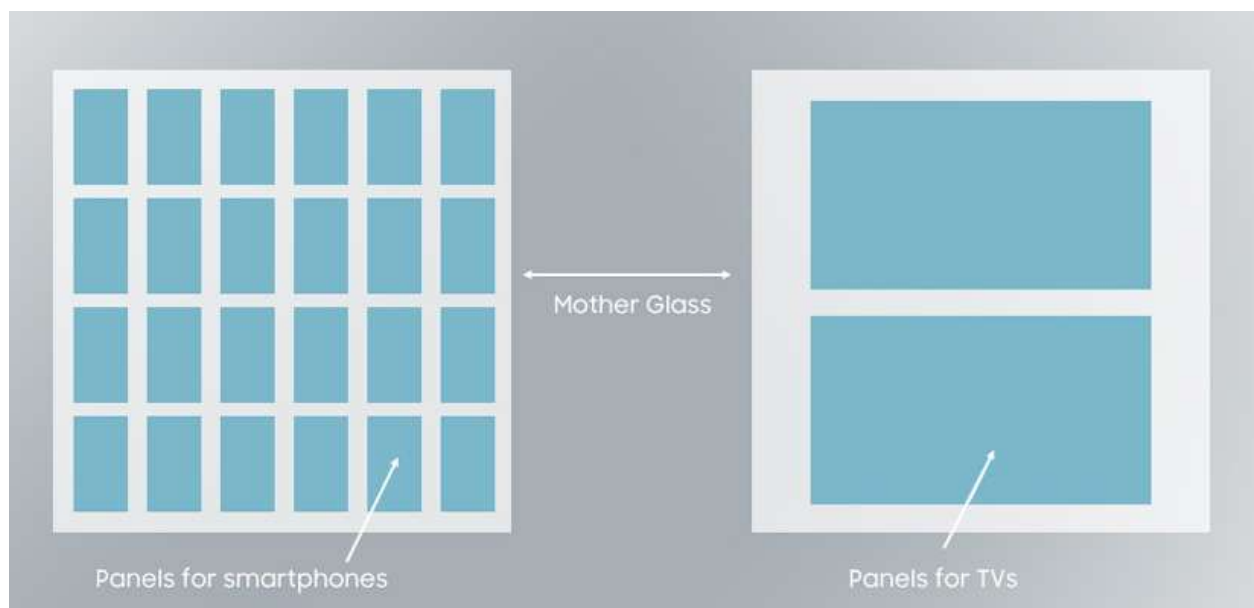
14. Petitioner's counsel has informed me that one of ordinary skill in the art has ordinary creativity and is not an automaton. Petitioner's counsel has informed me that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

15. Petitioner's counsel has informed me that secondary considerations of nonobviousness can include a long-felt but unmet need for the claimed invention, failure of others, copying, unexpected results, commercial success, skepticism, or industry praise. I understand that it is generally the patent owner's burden to present evidence of secondary considerations if the patent owner contends that any apply. I am not aware of any evidence of secondary considerations of nonobviousness that would apply to the claims at issue.

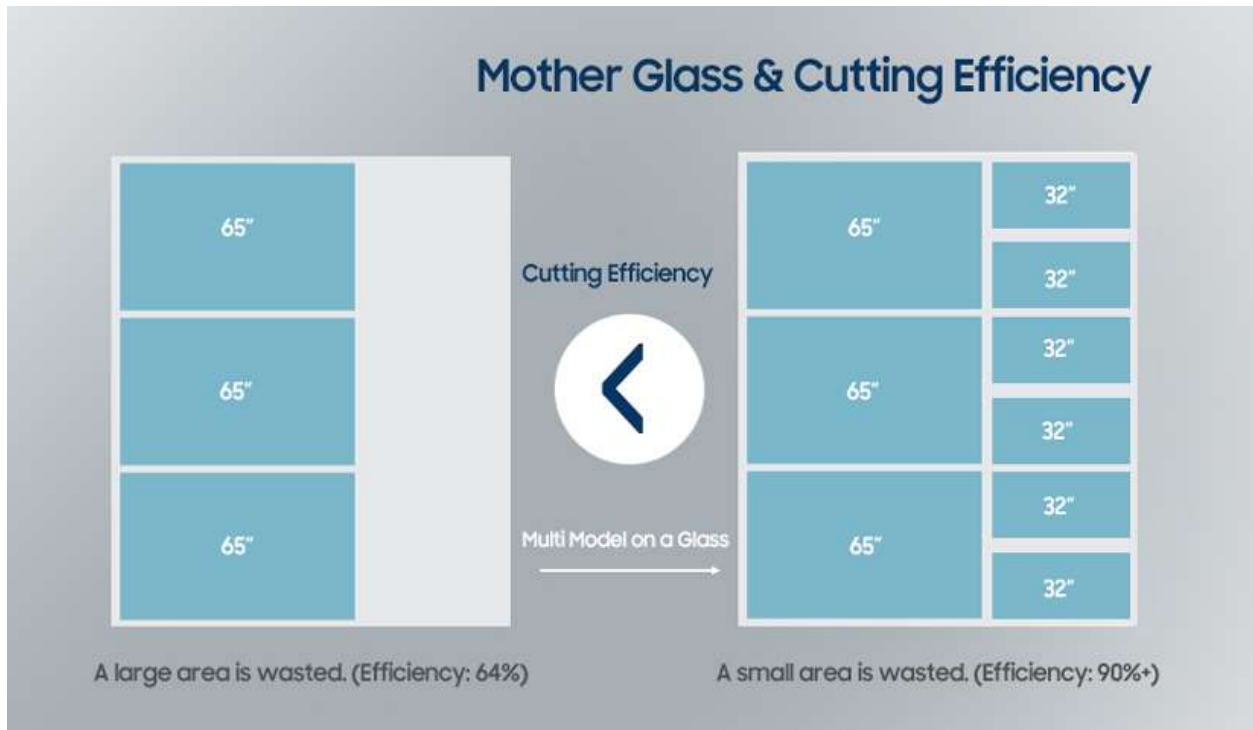
IV. TECHNOLOGY BACKGROUND

A. Batch Fabrication of OLED

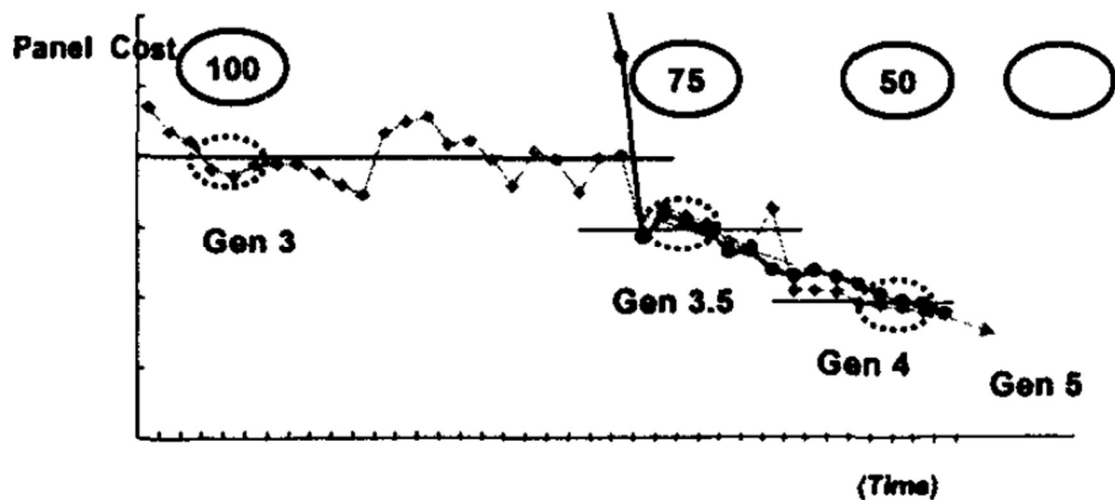
16. Organic light-emitting diodes (“OLEDs”) are fabricated by depositing organic and inorganic materials on a substrate. Various materials, such as glass and plastic, can be used in forming a substrate. Typically, multiple OLED displays are manufactured on a large sheet of substrate, known as a “mother glass.” For example, hundreds of smartphone displays can be made out of a single mother glass and cut into individual display panels as illustrated below:



17. This follows the traditional process for manufacturing Liquid Crystal Displays (LCDs). Traditionally, multiple LCDs have been manufactured on a mother glass to increase throughput and reduce manufacturing cost. As illustrated below, using a larger mother glass increases manufacturing efficiency by allowing more displays to be manufactured on a given substrate with less wasted areas:



18. Therefore, as illustrated below, using a larger mother glass reduces the cost of manufacturing each display panel:



Fig, 4 Mother glass size effect on panel cost

Souk (Ex.1023), 26. Similarly, OLEDs (which were developed later than the LCDs) have been manufactured on a mother glass to attain the known manufacturing efficiency, as well as take advantage of existing LCD process lines.

19. Over the years, the size of mother glasses used in the industry to manufacture LCDs and OLEDs have continued to increase. The main reason for the increased size is to produce display panels even more efficiently. Mother glasses are classified into different generations depending on their sizes. There is no universal standard for the size of the mother glass for each generation, so the exact size can vary for each generation by manufacturers. For example, Generation 1 mother glasses have dimensions of about 300 mm x 400 mm, and Generation 10 mother glasses have dimensions of about 2850 mm x 3050 mm:

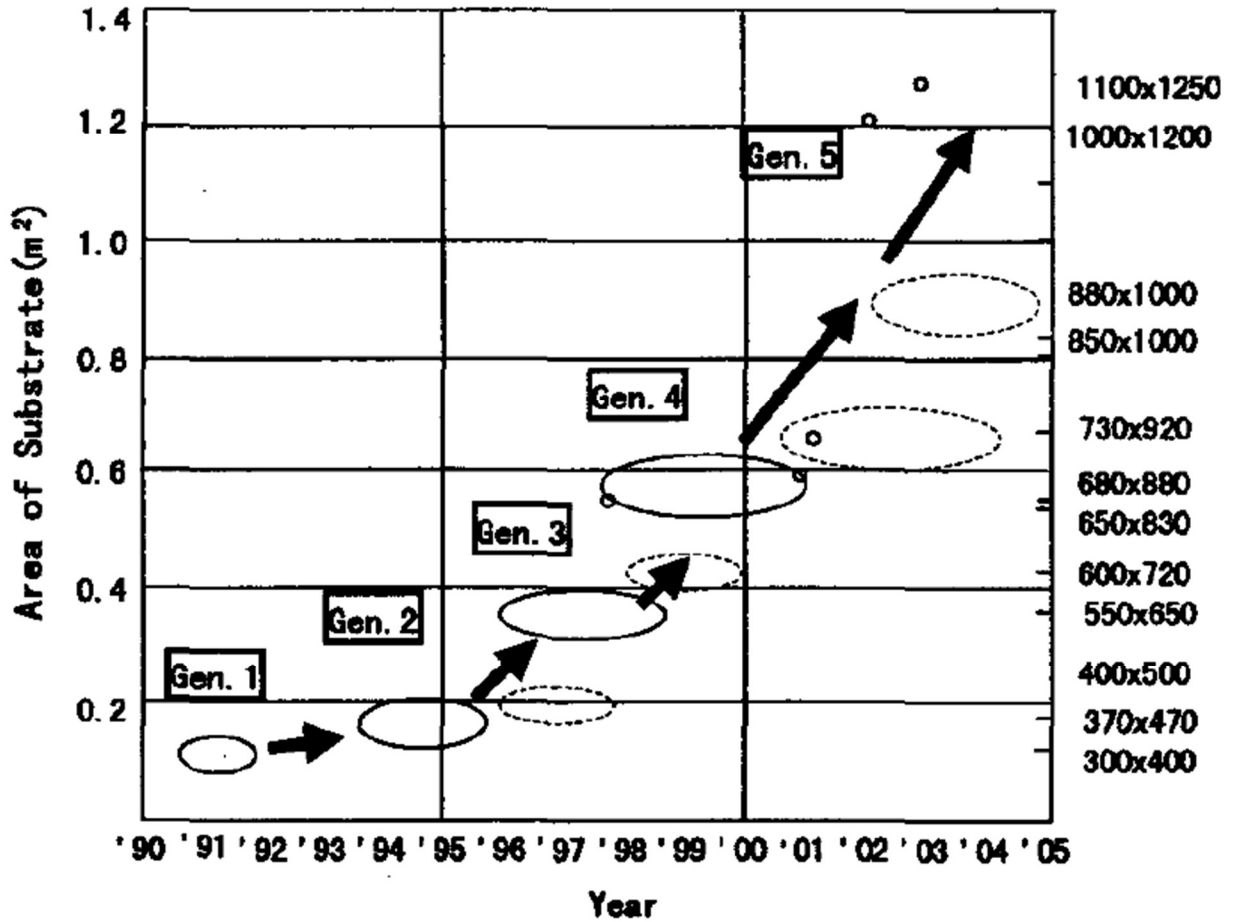
Table 14.2 Typical Glass Substrate Sizes for Different Generations of Displays

Generation	Dimensions	Area (m ²)	OLED Application
1	300 mm × 400 mm	0.12	Development
2	400 mm × 500 mm	0.20	Development
3	550 mm × 650 mm	0.36	
4	730 mm × 920 mm	0.67	Mobile displays/lighting
5	1100 mm × 1300 mm	1.43	Lighting/TVs
6	1500 mm × 1800 mm	2.70	
7	1900 mm × 2200 mm	4.18	
8	2200 mm × 2400 mm	5.28	Television
9	2400 mm × 2800 mm	6.72	
10	2850 mm × 3050 mm	8.69	

Gaspar (Ex.1024), 370.

20.By 2002, Generation 4 and 5 mother glasses were in use in the industry.

Fig.3 Trend of Substrate Size Expansion



Ohta (Ex.1025), 4. A Generation 5 mother glass was about ten times larger than a Generation 1 mother glass, allowing more display panels to be manufactured on a given substrate.

B. Selective Deposition Techniques

21.At the time of the invention, various methods of depositing a layer on a targeted area, known as selective deposition, were known. Selective deposition techniques

known and commonly used in 2002 included screen printing, inkjet printing, and using evaporation or vacuum deposition through shadow mask. *See* Palanisamy (Ex. 1007), [0021]-[0024]; '389 patent, 6:66-7:03. Inkjet printing deposits OLED ink through a nozzle on the desired location on the substrate. In screen printing, a material is deposited on the substrate by moving a device such as a squeegee to force the material to be printed through a screen having patterned openings. A shadow mask is a mask having apertures through which material is deposited onto a substrate. For example, a material that is evaporated can be applied through the shadow mask.

22. Different selective deposition techniques had their own benefits and considerations. For example, inkjet printing offers a high degree of control over precision printed patterns and is cost-efficient. Additionally, since the inkjet head does not come in contact with the substrate, it is often considered to have lower risk of contamination. Screen printing is inexpensive and allows high printing speed on large substrates. It is also a very mature technique in electronics manufacturing, and has been used in packaging of electronics and in production of electronic circuit boards for decades. Using a shadow mask allows good control of the positions on the substrate where the cover layers are formed and can be used together with other deposition techniques. Since it allows the use of

vacuum-based deposition techniques, it eliminates the need for the use of solvents to form inks.

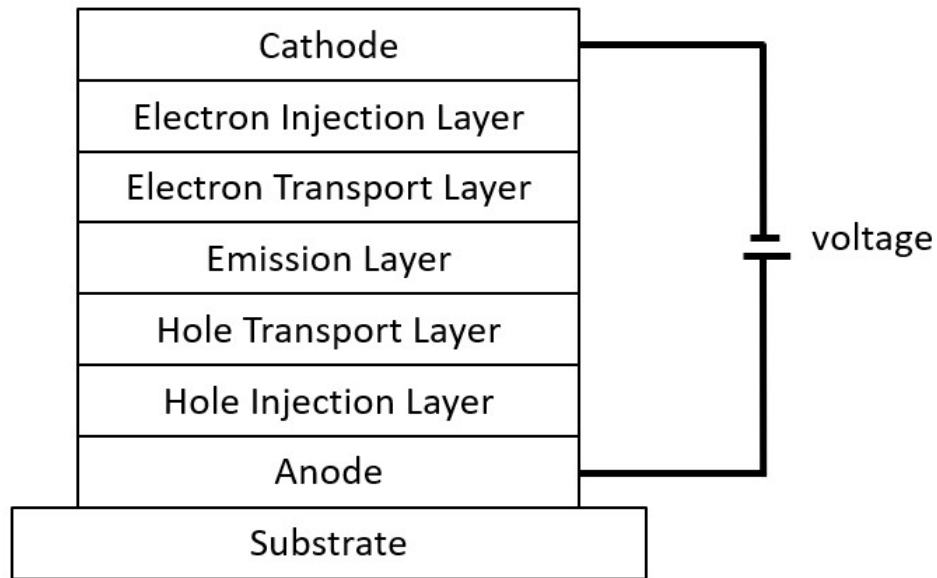
23. The above deposition techniques were known at the relevant time to be effective for selectively depositing layers for encapsulating an OLED device, as discussed in the next section. Such layers include may be comprised of organic material, which is a carbon-containing compound (including, for example, carbon-hydrogen or carbon-carbon comp). The encapsulating layers may also include inorganic material.

24. In addition, it was known at the relevant time that the above-mentioned selective deposition techniques were often interchangeable with one another. That is, for a given OLED encapsulation design that happened to inkjet printing as the means of selective deposition, as POSITA would have appreciated that it may have been suitable to substitute shadow masks or screen printing as the means to achieve the same selective deposition design.

C. Encapsulation of OLED Devices

25. OLEDs are used in display panels of various electronic products such as smartphones and TVs. A typical OLED is composed of at least a layer of organic material, also known as an electroluminescent (“EL”) layer, placed between two electrodes (a cathode and an anode). More specifically, OLEDs typically have thin multi-layers, which may include (1) a base substrate, (2) an anode, (3) a hole

injection layer, (4) a hole transport layer, (5) a light emitting layer, (6) electron transport layer, (7) electron injection layer, and (8) a cathode, as illustrated below.



This multi-layer structure for an OLED was used before 2002.

26. When electrical current flows from the cathode to the anode through the EL layer, the organic materials in the EL layer emit light.

27. The organic OLED materials are sensitive to moisture and oxygen. When exposed to moisture or oxygen, the organic materials oxidize and degrade, reducing light output. Therefore, OLED devices need to be encapsulated to protect them from moisture and oxygen. One approach of encapsulation is sealing the OLED devices with a metal or glass cap and epoxy glue. Another

encapsulation method is using thin-film barriers, such as a “polymer multilayer” (PML).

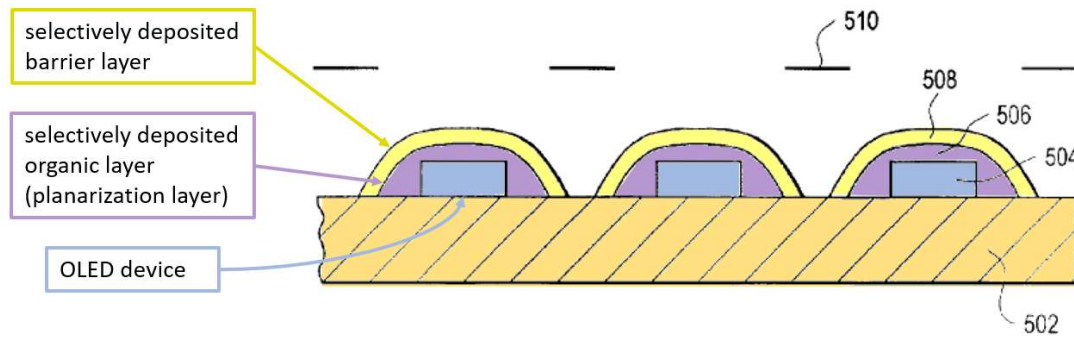
28. In a typical PML structure, a planarization layer is formed on top of the OLED structure. The planarization layer is commonly an organic layer and is provided to give a planar surface. The planarization layer is typically used to cover defects and make a smooth surface on the relatively irregular surface of the cathode. A barrier layer is formed on top of the planarization layer. The barrier layer is typically made of an inorganic material. By forming a barrier layer made of an inorganic material on the planarization layer, moisture and oxygen can be prevented from permeating into the planarization layer or the EL layer.

V. OVERVIEW OF U.S. PATENT NO. 6,948,349

A. Summary

29. The '389 patent relates to encapsulation of organic light emitting diode (“OLED”) devices. “Encapsulation is a way to protect the OLED device from the damaging environmental effects—primarily from oxygen and moisture.” '389 patent, 1:8-10.

30. In the embodiment of Figure 5 in the '389 patent, “organic layer 506 is deposited selectively,” “in a patterned fashion,” over an “OLED device 504 ... formed upon substrate 502,” *id.*, 6:53-58, and “barrier layer 508 may be selectively deposited” over the organic layer 506, *id.*, 7:3-6.



Id., Fig. 5 (annotated).

31.The patent states that “selectively depositing the organic layer ... may be accomplished in a variety of ways” (listing a number of conventional deposition techniques, and that “barrier layer 508 may be selectively deposited” “[i]n a similar fashion.” *Id.*, 6:66-7:6.

32.The '389 patent describes a prior method of encapsulation called “a ‘polymer multi-layer’ (PML) comprising alternating and repeating layers of an organic ... and a barrier layer,” as shown in Figure 1 below. *Id.*, 1:20-23.

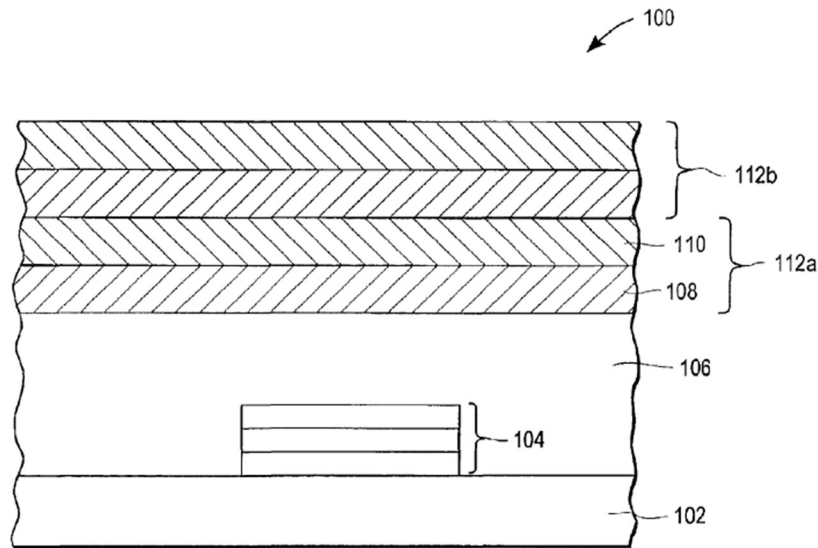


FIG. 1 (PRIOR ART)

Id., 1:23-24, Fig. 1.

33. The patent states that “[t]ypically, for PML structures, a planarization layer 106 is formed on top of OLED structure 104” and the “[p]lanarization layer 106 typically is an organic layer.” *Id.*, 1:30-34. “Barrier layer 108 typically comprises a sputtered metal, metal-oxide or a dielectric layer” and “provides the necessary environmental isolation from the corrosive effects of oxygen and moisture.” *Id.*, 1:37-40.

34. The ’389 patent also discusses a prior art method of “batch fabrication of many OLED devices upon a single large sheet of glass—such as shown as a top view in FIG. 2”:

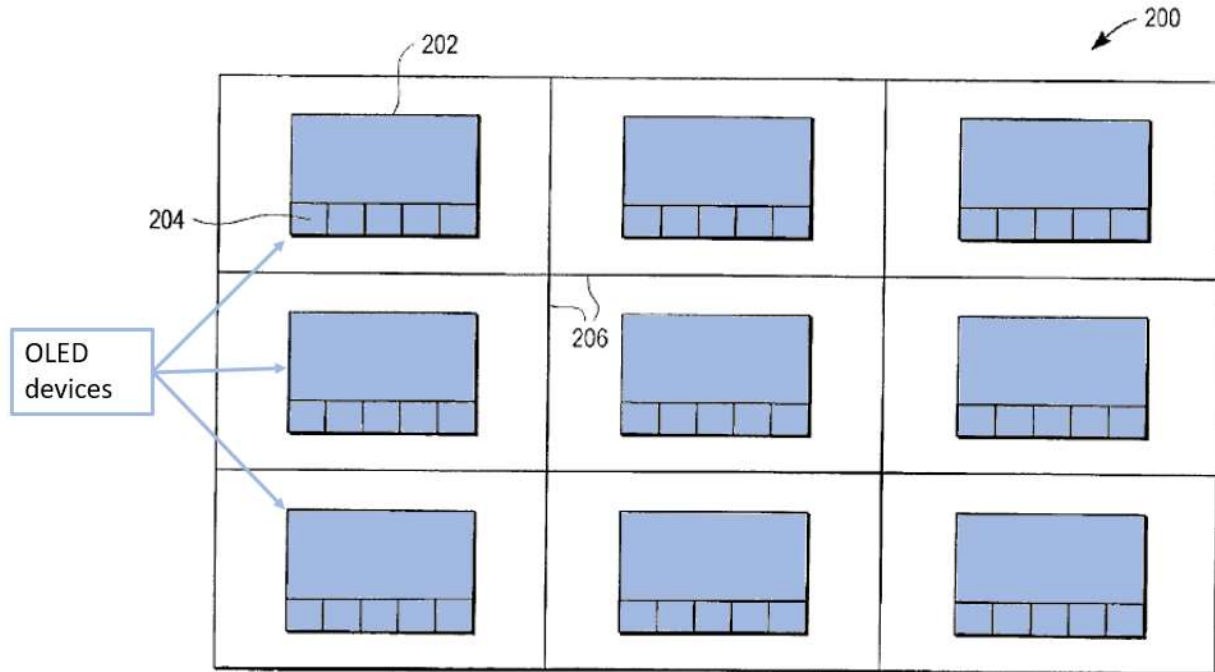


FIG. 2 (PRIOR ART)

Id., 1:63-65, Fig. 2 (annotated).

35. The patent states that “the PML structure is deposited ... over the entire glass sheet containing the multiple OLED devices.” *Id.*, 2:5-8. The patent further states that “[a]fter encapsulation, singulation is performed ... so that individual OLED devices 202 may be separated and further processed.” *Id.*, 2:12-16.

36. The patent states that the “problem with this PML technique” is that the PML layer is deposited over unwanted areas such as the electrical contact pads, scribe lines, break lines, and glue lines, whereas “the only part of the device that requires encapsulation is the OLED layer.” *Id.*, 2:17-28.

37. As discussed above, the '389 patent addresses this problem by selectively depositing the planarization layer and the barrier layer on each OLED device.

B. The Claims at Issue

38. Independent claim 34 recites:

A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

selectively depositing at least one planarization layer upon said devices; and

selectively depositing at least one barrier layer over said planarization layer.

39. Dependent claims 35-40 recite specific techniques for “selectively depositing” the “planarization layer” or the “barrier layer.”

40. Independent claim 41 recites:

A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing a mask on top of said substrate, such that mask openings are placed on top of said devices;

depositing at least one planarization layer upon said mask and said plurality of devices;

removing said mask from said substrate; and selectively depositing at least one barrier layer over said planarization layer.

41. Dependent claims 42-46 recite specific techniques for “depositing said mask” or “depositing at least one planarization layer.”

C. Level of Ordinary Skill in the Art

42. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

43. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '389 patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to understand the '389 patent. Finally, I placed myself back in the relevant

periods of time, and considered the state of the art and the level of skill of the engineers working in this field in those times.

44. It is my opinion that a POSITA for the '389 patent would have had a bachelor's degree in Electrical Engineering, Materials Science, or a related field, and at least one year of experience in display technologies. Additional education might compensate for a deficiency in experience, and vice-versa.

D. Claim Construction

1. “depositing by shadow mask, sputtering, ink jet deposition, screen printing evaporation”

45. The list of deposition processes in dependent claim 40 omits a connective term (i.e., either an “and” or “or”). I have been instructed to interpret dependent claim 40 as including an “or” as inserted below:

The method as recited in claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by shadow mask, sputtering, ink jet deposition, screen printing [*or*] evaporation.

46. As initially filed, the claim 40 read:

40. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises one of a group, said group comprising: depositing by shadow mask, sputtering, ink jet deposition, screen printing and evaporation.

'389 File History (Ex.1002), 399.

47.The Examiner subsequently amended the claim as follows:

In claim 40, at lines 2-3, **delete** "one of a group, said group comprising :'" and at line 4, **replace** "and" with -- or --.

Id., 418.

48.Although the "or" does not appear in the as-issued claim, it is my understanding that the Examiner's amendment shows that the claim was meant to include this coordinating conjunction.

2. "non-sucking to OLED substrate"

49.Claim 44 requires a "mask comprising a material non-sucking to OLED substrate." I understand that the file history indicates that this reflects a typographical error in the as-issued patent. The claim during prosecution instead used the term "non-sticking" as shown below:

44. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising a material substantially **non-sticking** to OLED substrate over the areas in between the active areas.

'389 File History (Ex. 1002), 400 (highlighted).

50.Accordingly, I have been instructed to address the claim under the assumption that "non-sucking to OLED substrate" should be interpreted as "non-sticking to

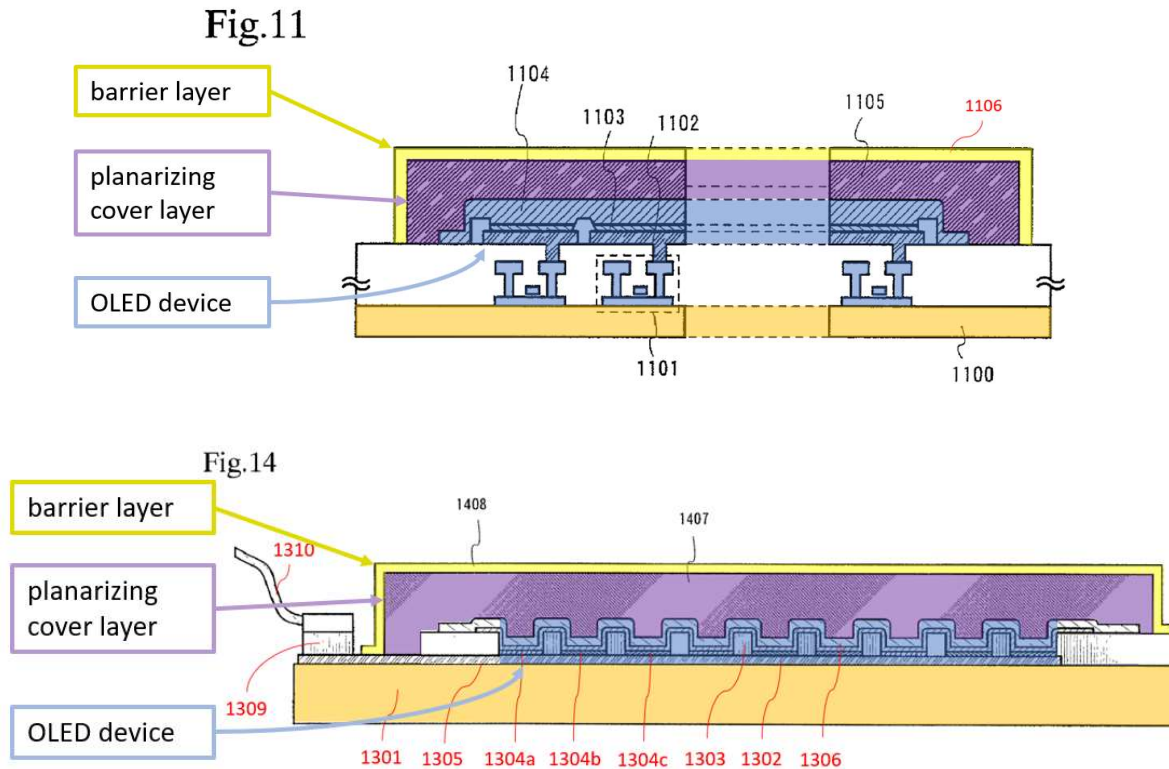
OLED substrate,” as well as under the alternative scenario in which the claim is applied as written.

VI. OVERVIEW OF THE PRIOR ART REFERECES

A. Yamazaki (Ex.1005)

51. Yamazaki teaches selective encapsulation for an OLED device, for use in a “self-light emitting device, i.e., a “display device.” Yamazaki, [0002]. It “has an object to provide a process of successively forming an EL layer, a cathode, a barrier layer, and a cover layer in the same multi-chamber.” *Id.*, [0009]. “By further forming a film made of an inorganic material (hereinafter referred to as a barrier layer) on the [organic] cover layer, moisture and oxygen can be prevented from permeating into the cover layer or the EL layer.” *Id.*, [0008].

52. As shown in Figures 11 and 14, which I have annotated below, Yamazaki discloses multiple embodiments in which OLED devices (blue) are encapsulated by forming a planarizing “cover layer ... made of an organic resin film evenly on the pixel portion” (purple), *id.*, [0177], as well as a “barrier layer ... to cover the cover layer” (yellow), *id.*, [0183].



Id., Figs. 11 and 14 (annotated). More specifically, Yamazaki illustrates that its cover layer forms a planar surface on which the barrier layer is formed, and explains that the layer is made from a “material that ... has planarity,” *id.*, [0178].

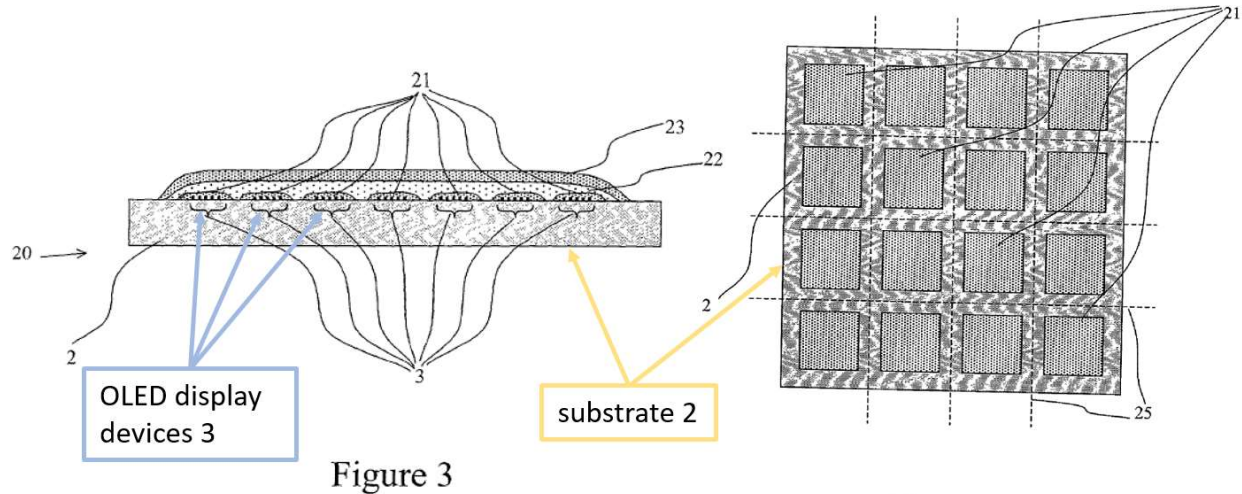
53. Like the '389 patent, Yamazaki teaches that these layers are selectively deposited using known selective deposition techniques. *See id.*, [0178] (“Because the cover layer 1105 is formed using the ink jet method, it can be selectively formed on the pixel portion.”), [0183] (“[T]he barrier layer 1106 is formed selectively using a shadow mask.”).

B. Ghosh (Ex.1006)

54. Ghosh teaches batch fabrication (and encapsulation) of OLED devices on a large substrate, consistent with the '389 patent's admissions on the prior art.

55. As I discussed above, OLED displays are typically manufactured in batch on a large sheet of substrate, known as a "mother glass." Indeed, the '389 patent admits that the "batch fabrication of many OLED devices upon a single large sheet of glass" was known, illustrating this process as "PRIOR ART" in Figure 2. '389 patent, 1:63-65. "As depicted [in Figure 2], "OLED devices 202 are typically laid down in rows and columns on a large sheet of glass 200," *id.*, 1:67-2:2, followed by a "thin film encapsulation step," *id.*, 2:5-12, so that "several tens (or even hundreds) of OLED devices 202 may be so fabricated" on a single sheet," *id.*, 1:65-67.

56. Ghosh likewise teaches batch fabrication (and encapsulation) of OLED devices on a large substrate. Ghosh teaches an encapsulation assembly "for a plurality of OLED display devices 3 on a substrate 2," as shown in the cross-sectional view (Fig. 3) and top-down view (Fig.5) below. Ghosh, [0031].



Id., Figs. 3, 5 (annotated).

57. The OLED display devices 3 are covered with a first encapsulation layer 21 that is selectively “patterned to leave exposed a portion of the substrate surface in between the individual OLED devices,” *id.*, [0032], and the “dashed lines 25 in FIG. 5 indicate where the substrate would be cut as part of the dicing operation following completion of the encapsulation assembly.” *Id.* That is, the devices are cut along these dashed lines to yield individual OLED displays. *See id.*

58. During prosecution of the '389 patent, the Examiner applied Ghosh in rejecting claim 34 (among others), explaining that Ghosh teaches a “method of encapsulating a plurality of devices fabricated upon a substrate,” the steps of said method comprising “fabricating a plurality of devices 13 (i.e. OLED) on a substrate 2 (Fig.3)”; depositing and patterning “at least one planarization layer 21”; and “selectively depositing at least one barrier layer 22 ... over the patterned

planarization layer.” ’389 File History (Ex.1002), 292. The applicants overcame this rejection, arguing that “[i]n *Ghosh*, the ‘second encapsulation layer 22’ (in the Office Action the Examiner refers to this layer as the ‘barrier layer’) is nonselectively deposited” *Id.*, 376. However, the applicants did not dispute that Ghosh teaches a method of encapsulating a plurality of OLED devices fabricated upon a substrate (or that Ghosh’s method comprises selectively depositing at least one planarization layer), *See id.*

C. Weaver (Ex.1008)

59. Weaver likewise discloses “structures that protect organic optoelectronic devices [e.g., OLEDs] from the surrounding environment,” Weaver, [0001], [0003], and methods for creating such protective structures, *see id.*, [0057]. For example, Figure 6 of Weaver, which I have annotated below, shows that an OLED 140 (blue) is protected (i.e., encapsulated) by a barrier region 150 comprising a series of organic “planarizing layers” 151a-c and “high-density layers” 152a-c:

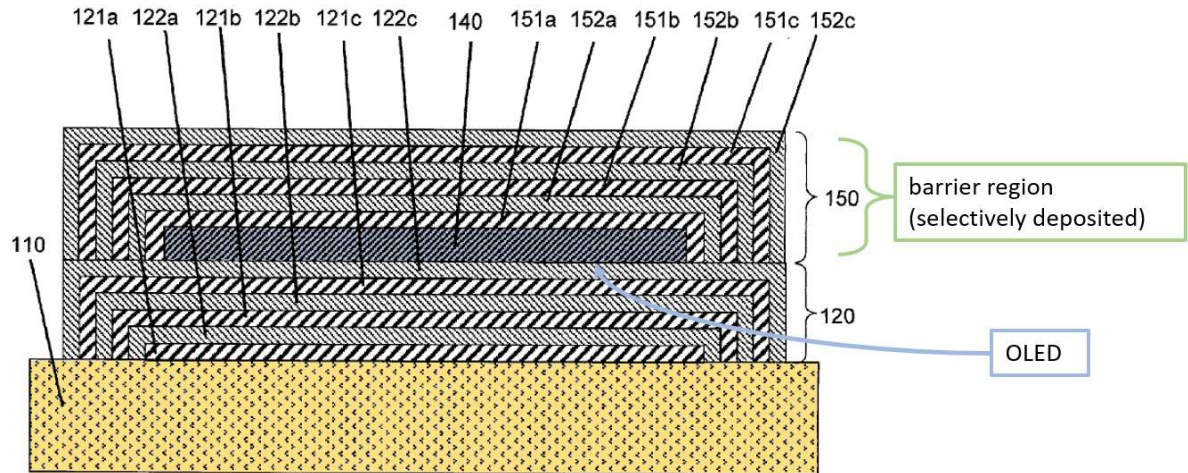


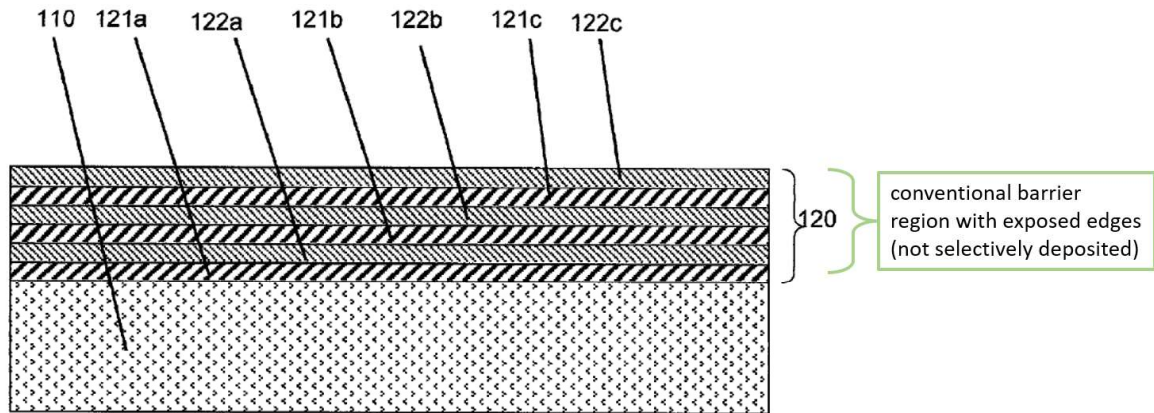
Fig. 6

Id., Fig. 6 (annotated).

60. These encapsulation layers are deposited selectively over the underlying device.

As I have shown in Figure 6, the planarizing layers 151a-c and high-density layers 152a-c surround the OLED 140 from the top and sides, but do not extend laterally over the entire surface of the substrate.

61. Like the '389 patent, Weaver teaches that such selective encapsulation is advantageous when manufacturing multiple OLED devices on “large sheets of material,” that “can be subsequently subdivided into sheet sizes appropriate for the final application (e.g., into sheets the size of a computer monitor screen.” *Id.*, [0038]. Weaver explains that under conventional (non-selective) approaches for multi-layer encapsulation, “cutting a large sheet produces a structure with exposed edges like that shown in FIG. 1a,” shown below. *Id.*, [0038].

**Fig. 1a**

Id., Fig. 1a (annotated). In contrast, “[t]his situation is improved by the structures of [Weaver’s] invention”—i.e., where selective encapsulation allows the barrier layers to “extend[] down the sides.” *Id.*, [0041]-[0042].

62. Weaver discloses that its “[d]eposition of progressively larger cooperative barrier layers can be achieved in a number of ways,” teaching further that “[p]referred techniques are continuous techniques such as web-based processing techniques,” *id.*, [0057]. Such an approach (which is sometimes described as a “roll-to-roll” process) is illustrated in the apparatus of Figure 8. This apparatus uses a series of “deposition sources” 221a-c and 222a-c in order to deposit the planarizing and high-density layers. As Weaver explains, “each deposition source is provided with an aperture that is larger than that of the adjacent upstream source ... such that the material being deposited from each source progressively covers a wider area as the substrate proceeds downstream (i.e., from left to right).” *Id.*, [0059],

Fig. 8. In other words, these deposition sources are configured to selectively deposit the encapsulating “planarizing layers” and “high-density layers” in specific areas.

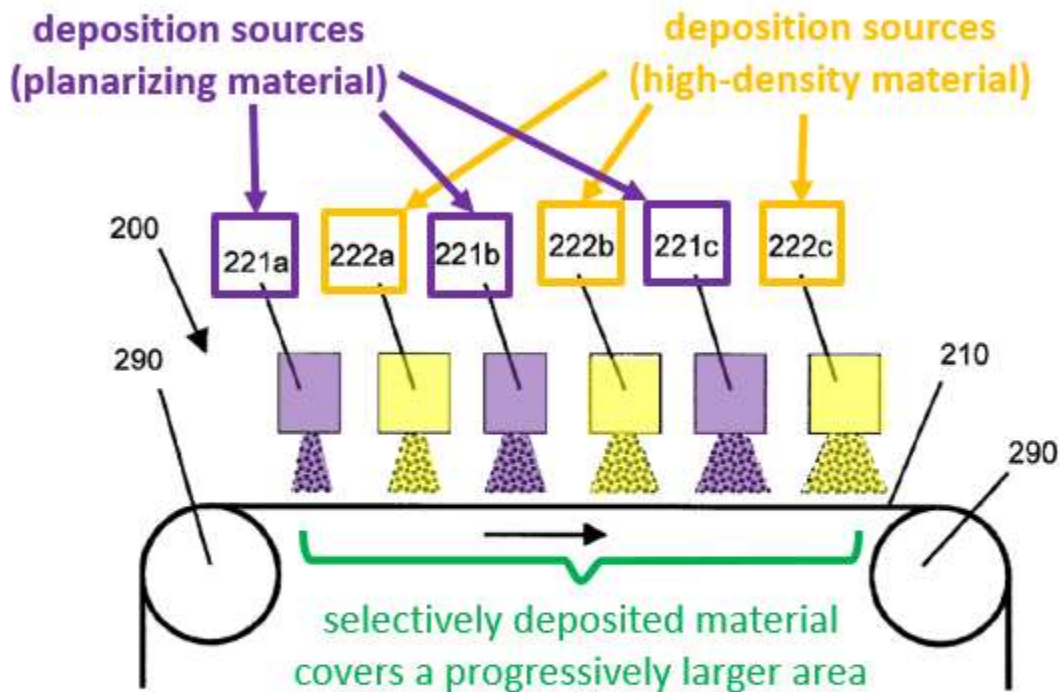


Fig. 8

Weaver, Fig. 8 (annotated).

D. Palanisamy (Ex.1007)

63.As I discussed above, the '389 patent explains that “selectively depositing the organic layer and the barrier layer may be accomplished in a variety of ways.” '389 patent, 6:66-7:03 (discussing use of a “shadow mask ... or by inkjet deposition or other screen printing techniques”). Consistent with this explanation,

Palanisamy discloses a number of techniques for “selectively applying an organic passivation material” for organic light emitting devices (OLEDs), Palanisamy, [Abstract]—including “an ink jet printer,” *id.*, [0021], “[a] mask,” *id.*, [0022], and “a screen printing technique,” *id.*, [0024].

64. Palanisamy explains that such passivation material is used to protect the OLED material from “moisture, oxygen, and common solvents”—i.e., to encapsulate the OLED material. Palanisamy, Abstract, [0001], [0003]. Palanisamy further teaches that “the passivation may be selectively applied to the areas coated by the OLED while excluding areas where passivation would be undesirable, such as the areas proximate to the contacts.” *Id.*, [0021].

65. Palanisamy discloses three specific selective deposition techniques. For example, “[o]ne selective, passivation deposition technique, shown in FIG. 3, involves an inkjet printer 44 to selectively apply passivation to areas 42.” Palanisamy, [0021].

I have annotated Figure 3 of Palanisamy below.

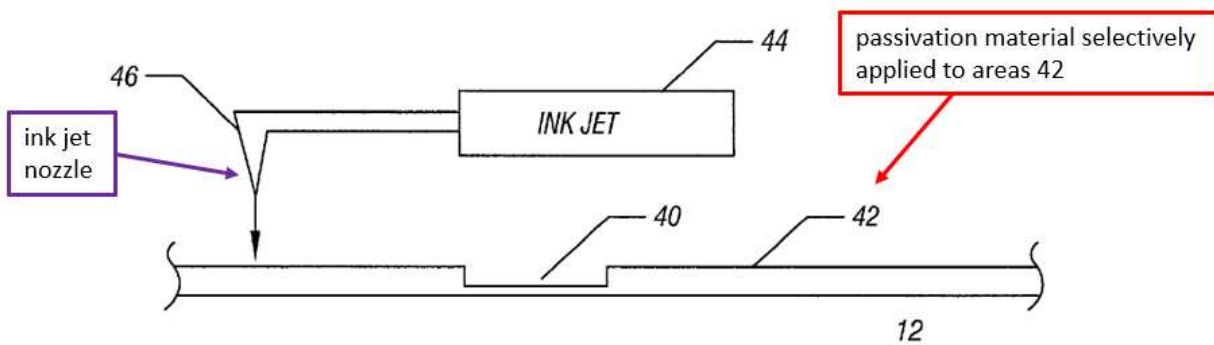


FIG. 3

Id., Fig. 3 (annotated).

66. “In accordance with another technique, a passivation sprayer 50 may be utilized ... as shown in FIG. 4. A mask 52 with openings 54 may be utilized to define the regions where passivation may be applied” *Id.*, [0022]. Figure 4 of Palanisamy is reproduced below.

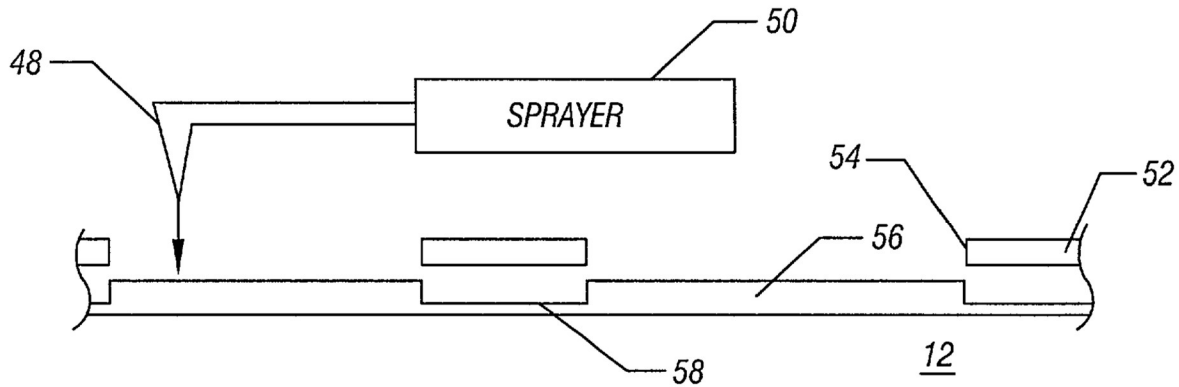
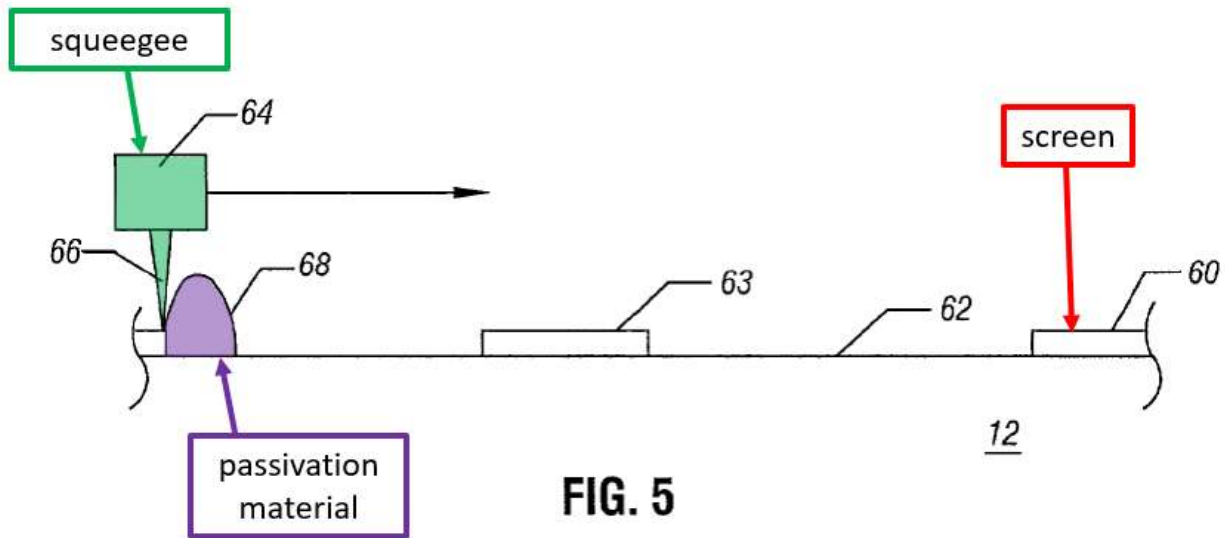


FIG. 4

Id., Fig. 4.

67. Finally, “[t]urning next to FIG. 5, a screen printing technique may be utilized to passivate selectively.... A squeegee 64 is passed across the surface of the screen 60 causing the material 68 to be pressed into the regions where the screen 60 is open” *Id.*, [0024]. I have annotated Figure 5 of Palanisamy below.



Id., Fig. 5 (annotated).

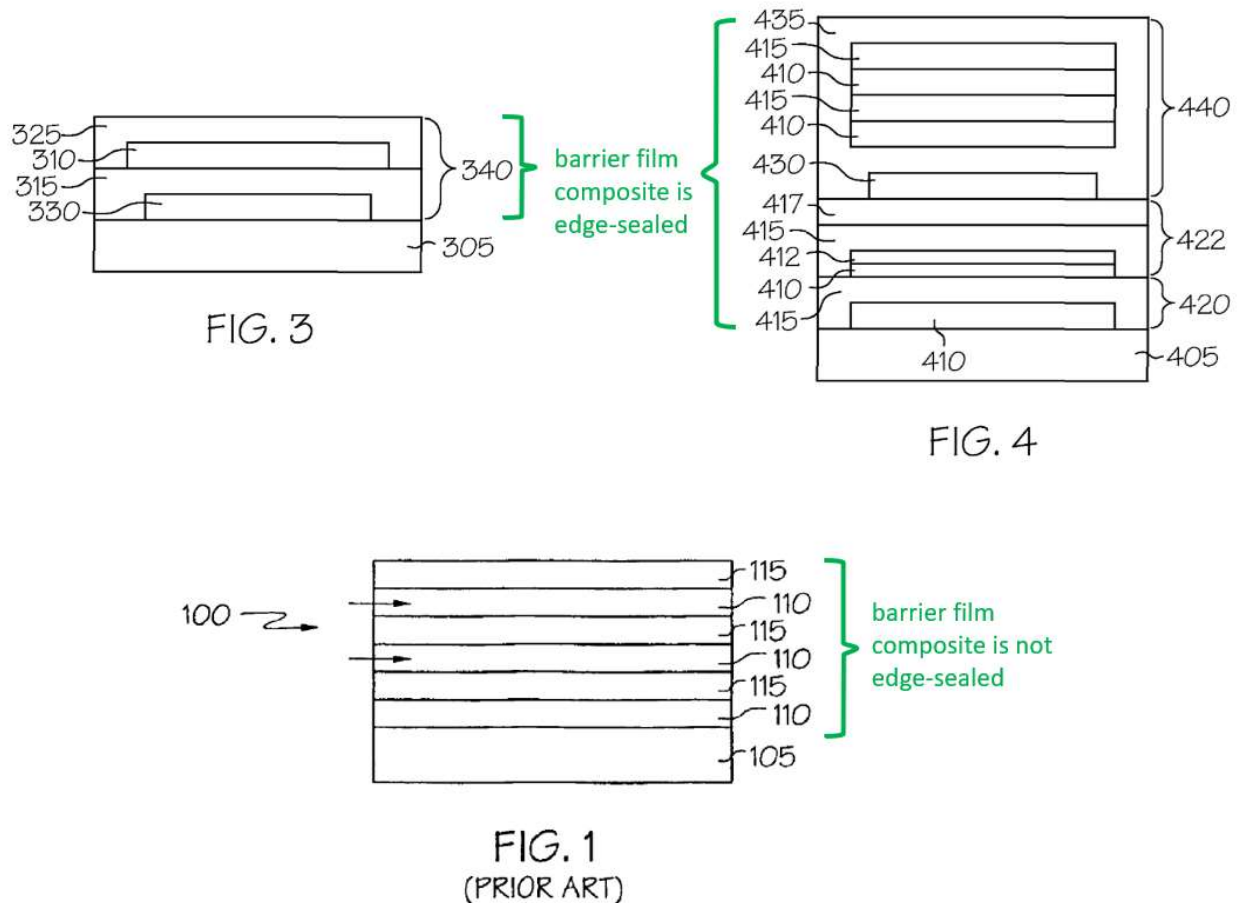
E. Fujimori (Ex. 1014)

68.Fujimori discloses an approach for manufacturing OLED display elements using a “mask attached to a substrate with magnetic force.” Fujimori, [0010], such that “adhesion between the mask and substrate is improved,” *id.*, [0029], and thereby allowing for “favorable pattern processing accuracy,” *id.*, [0009].

F. Burrows (Ex.1009)

69.Similar to Weaver, Burrows discloses techniques for encapsulating devices, such as OLED displays, “requiring protection from moisture, gas, or other contaminants.” Burrows, 5:22-30. Like Weaver, Burrows’s encapsulation technique results in the OLED device, and its encapsulating barrier film composites, being “edge-sealed.” *Id.*, Abstract, 1:47-57. This is shown for example in Figures 3 and 4 (which I have annotated below), compared to “PRIOR

ART” Figure 1 (also annotated below) in which the barrier film composite is not “edge-sealed:”



Id., Figs. 1, 3, 4 (annotated); 1:15-27, 5:10-21, 5:44-49.

70. Also similar to Weaver, Burrows’s encapsulation includes one or more “barrier stacks” (indicated as 340 and 440 in Figures 3 and 4 above, respectively), each including one or more decoupling layers (indicated as 310 and 410 in Figures 3 and 4 above, respectively) that “provide improved surface planarity,” *id.*, 7:8-18. A POSITA would have understood these decoupling layers to be “planarization

layers” as claimed in the ’389 patent. Further, like Weaver’s planarization layer, Burrows’s planarization (i.e., decoupling) layers are selectively deposited. This is reflected in Figures 3 and 4, where layers 310 and 410 are described as having an area that is, by comparison, smaller than the barrier layers in their respective stacks. *Id.*, 5:18-21 (“The barrier layers 315, 325 have an area greater than the area of the decoupling layer 310 so the decoupling layer 310 is sealed between the barrier layers 315, 325.”); 5:62-65 (“Barrier stack 440 also includes barrier layer 435 which has an area greater than the area of the decoupling layers 410 which seals the decoupling layers 410 within the area of barrier layer 435.”).

71. Burrows teaches that the selective deposition of its decoupling (i.e., planarization) layer can be achieved using shadow masks, as part of a continuous-roll process. As Burrows explains:

In order to encapsulate multiple small environmentally sensitive devices contained on a single large motherglass, **the decoupling material may be deposited through multiple openings in a single shadow mask, or through multiple shadow masks.** This allows the motherglass to be subsequently diced into individual environmentally sensitive devices, each of which is edge sealed.

For example, the mask may be in the form of a rectangle with the center removed (like a picture frame). **The decoupling material**

is then deposited through the opening in the mask. The layer of decoupling material formed in this way will cover an area less than the area covered by the layer of barrier material. **This type of mask can be used in** either a batch process or **a roll coating process operated in a step and repeat mode.**

Id., 7:59-8:10.

72. Burrows further discloses encapsulating **a plurality** of devices, using similar batch fabrication techniques as discussed in the '389 patent's discussion of the background art (*see* '389 patent, 1:63-2:02 and "PRIOR ART" Figure 2):

In order to encapsulate multiple small environmentally sensitive devices contained **on a single large motherglass**, the decoupling material may be deposited through multiple openings in a single shadow mask, or through multiple shadow masks. This allows **the motherglass to be subsequently diced into individual environmentally sensitive devices**, each of which is edge sealed.

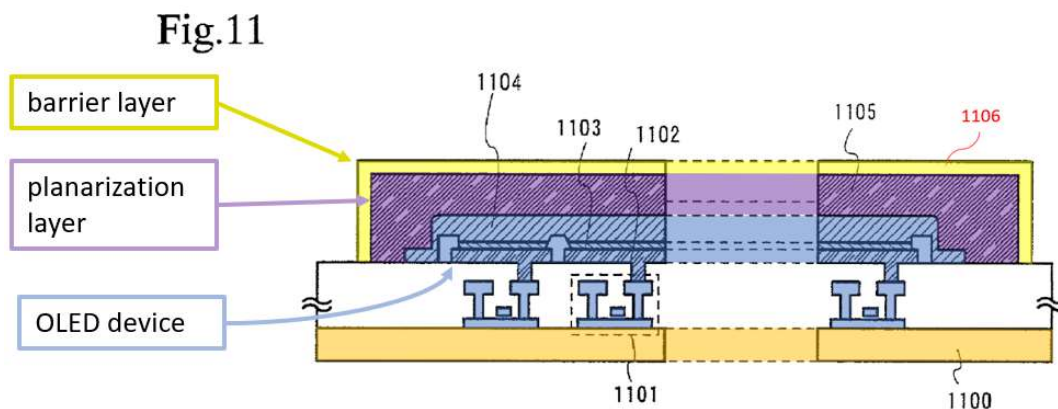
Id., 7:59-65.

VII. SPECIFIC GROUNDS OF CHALLENGE

A. Ground I: Claims 34, 35, 37, and 40 Are Obvious Over Yamazaki in View of AAPA/Ghosh

1. Independent Claim 34

73. In my opinion, Yamazaki discloses a method of encapsulating a device (specifically, an OLED display panel) fabricated upon a substrate by selectively depositing a planarization layer (Yamazaki's organic "cover layer") and selectively depositing a barrier layer (Yamazaki's "barrier layer"). This is shown for example in my below annotation of Figure 11.



Yamazaki, Fig. 11 (annotated).

74. Although Yamazaki does not expressly discuss encapsulating a *plurality* of such OLED display panel devices, in my opinion, it would be obvious to a POSITA that Yamazaki's approach would be implemented in a batch manufacturing process in which multiple display panels are being made simultaneously on a large substrate. Batch manufacturing was conventional for manufacturing OLED

displays, as the '389 patent itself admits. In addition, to the extent that a separate prior art reference disclosing batch manufacture of OLEDs would be necessary, Ghosh confirms that OLED display panels such as those in Yamazaki were routinely manufactured in batch, and that there were distinct benefits in doing so. Thus, Yamazaki renders obvious claims 34, 35, 37, and 40.

a. Element 34[Preamble]: “A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:”

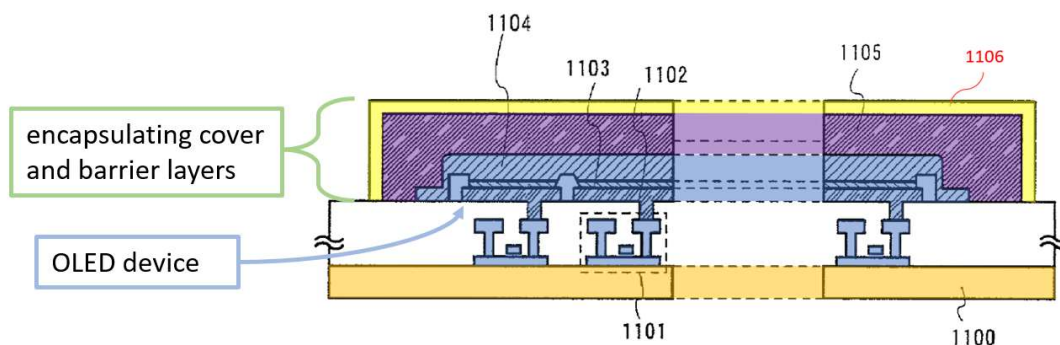
75. In my opinion, to the extent the preamble is limiting, it is obvious based on Yamazaki in view of the admitted prior art and/or Ghosh. At least two embodiments of Yamazaki independently disclose a *method of encapsulating* an OLED display panel *device fabricated upon a substrate*. Furthermore, it would have been obvious to apply these methods for *encapsulating a plurality* of such display devices during batch fabrication, as was known based on the admitted prior art and as further taught by Ghosh.

76. Yamazaki discloses methods for manufacturing active and passive matrix OLED display panels. Yamazaki explains that “[t]he present invention relates to ... a method of manufacturing an electric appliance having the self-light emitting device as a display unit [T]he above-mentioned self-light emitting device is also referred to as an OLED.” Yamazaki, [0002]; *see also id.* at [0006] (“There are two kinds of self-light emitting device: a passive type (simple matrix type)

and an active type (active matrix type).”). More particularly, Yamazaki teaches *methods of encapsulating* such devices using “a barrier layer and a cover layer.” *Id.*, [Abstract].

77.First, the embodiment of Figure 11 depicts “an active matrix type self-light emitting device,” Yamazaki, [0026], which includes a *device* (specifically, the active matrix OLED display panel) that is *fabricated upon a substrate* (“substrate 1100”), and *encapsulated* by a “cover layer 1105” and “barrier layer 1106.” Yamazaki, [0177], [0178], [0183]. I have shown this in my below annotation of Figure 11:

Fig.11

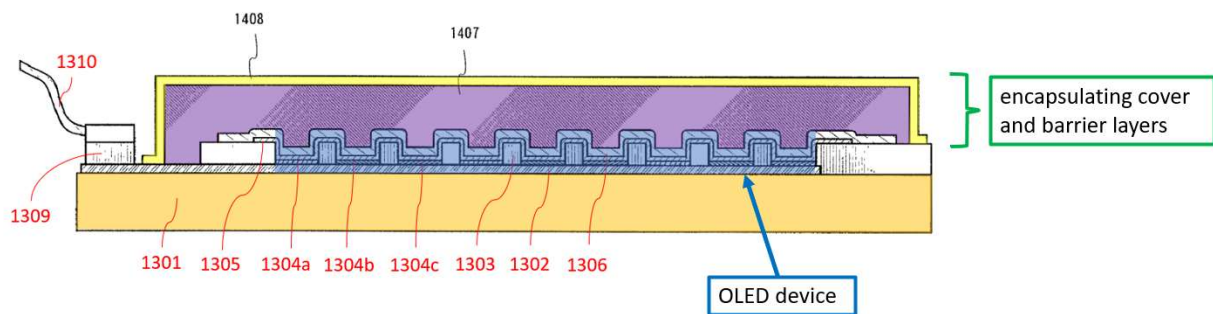


Yamazaki, Fig. 11 (annotated).

78.Yamazaki explains that “by forming the cover layer 1105 and the barrier layer 1106 on the active matrix substrate, the invasion of degrading factors to the EL [electroluminescent] element, such as moisture and oxygen, from the outside can be prevented.” *Id.*, [0184]. Thus, Yamazaki teaches a *method of encapsulating* the underlying device with this embodiment.

79. Second, the embodiment of Figure 14 depicts “a passive type self-light emitting device,” i.e., one that uses a “simple matrix” or “passive matrix” configuration. *Id.*, [0029]. It includes a *device* (passive matrix OLED display panel) that is *fabricated upon a substrate* (1301), and *encapsulated by* a “cover layer 1407” and “barrier layer 1408.” *Id.*, [0186]-[0203]. I have shown this in my below annotation of Figure 14:¹

Fig.14



Id., Fig. 14 (annotated).²

¹ I note that, as Yamazaki explains, the constitutions of these embodiments “may be implemented freely combining” with each other. Yamazaki, [0204]. Therefore, a POSITA would have understood that the teachings regarding Figure 11 are pertinent to those of Figure 14 and vice-versa.

² Figures 13 and 14 of Yamazaki depict two alternative configurations of its “passive type” (or “simple matrix”) display, which it describes as “Embodiment 4.” The configurations are the same except that in Figure 13 “the cover layer 1308 is formed

80. In my opinion, at the time of the alleged invention it would have been obvious to a POSITA to apply Yamazaki's methods for encapsulating a plurality of such devices in batch fabrication. While Yamazaki does not specifically discuss batch fabrication, for the reasons I explained above, a POSITA would have known that flat panel displays, such as the OLED panels in Yamazaki, were conventionally manufactured in bulk on a large sheet of substrate, which would be cut into smaller display sizes at the end of the manufacturing process. Compared to producing each display panel individually, producing multiple display panels from a large substrate was well-known to reduce costs, increase throughput, and increase yield. *See* Boroson, [0002] ("In manufacturing, electronic devices are typically produced by fabricating large substrates containing multiple electronic devices. ... The primary reason for fabricating multiple electronic devices on large individual substrates or a continuous roll substrate is to reduce manufacturing cost by decreasing handling, increasing throughput, and increasing yield.").

on the barrier 1307," whereas in Figure 14 (which I rely upon here) "barrier layer 1408 is formed after forming a cover layer 1407." Yamazaki, [0203]. Figure 14 omits labels for the structures that are identical between Figures 13 and 14. I have annotated Figure 14 to add the omitted labels.

81. Not surprisingly, the admitted prior art of the '389 patent confirms that such batch manufacture of OLED devices was routine and beneficial. The background of the patent describes a known problem that is "exacerbated during the batch fabrication of many OLED devices upon a single large sheet of glass—such as shown as a top view in FIG. 2." '389 patent, 1:63-65. Figure 2 of the '389 patent, labeled as "PRIOR ART"—and which I have annotated below—depicts this batch fabrication:

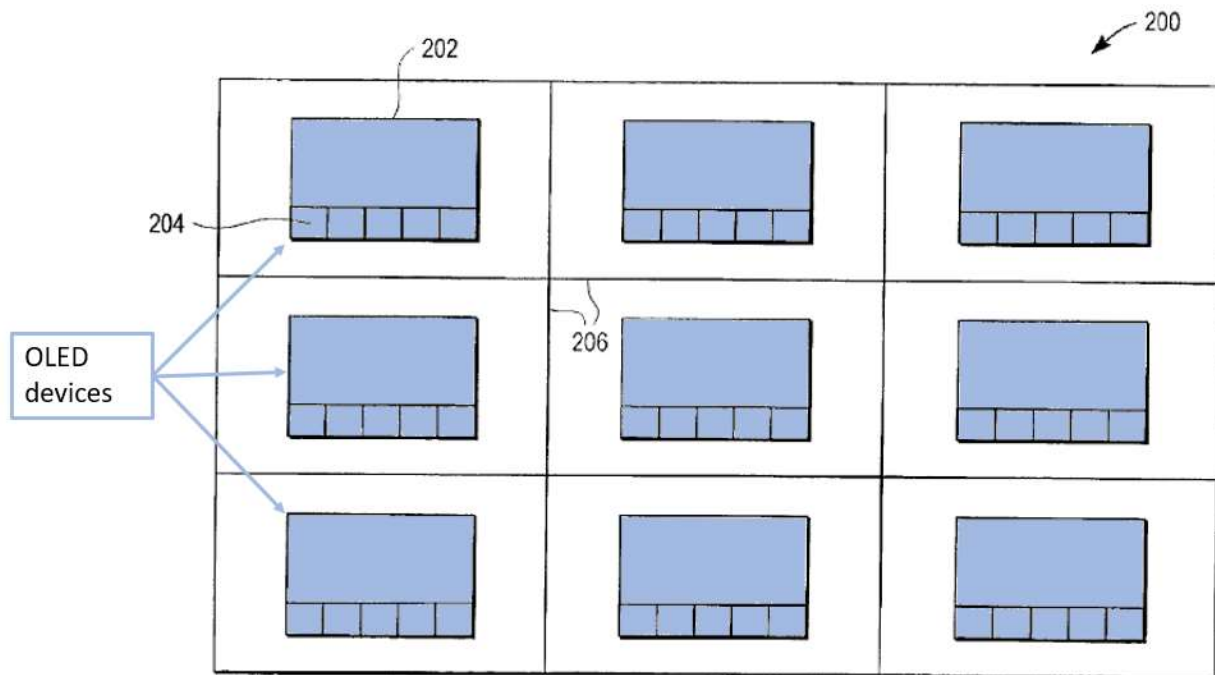
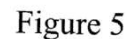


FIG. 2 (PRIOR ART)

'389 patent, Fig. 2 (annotated).

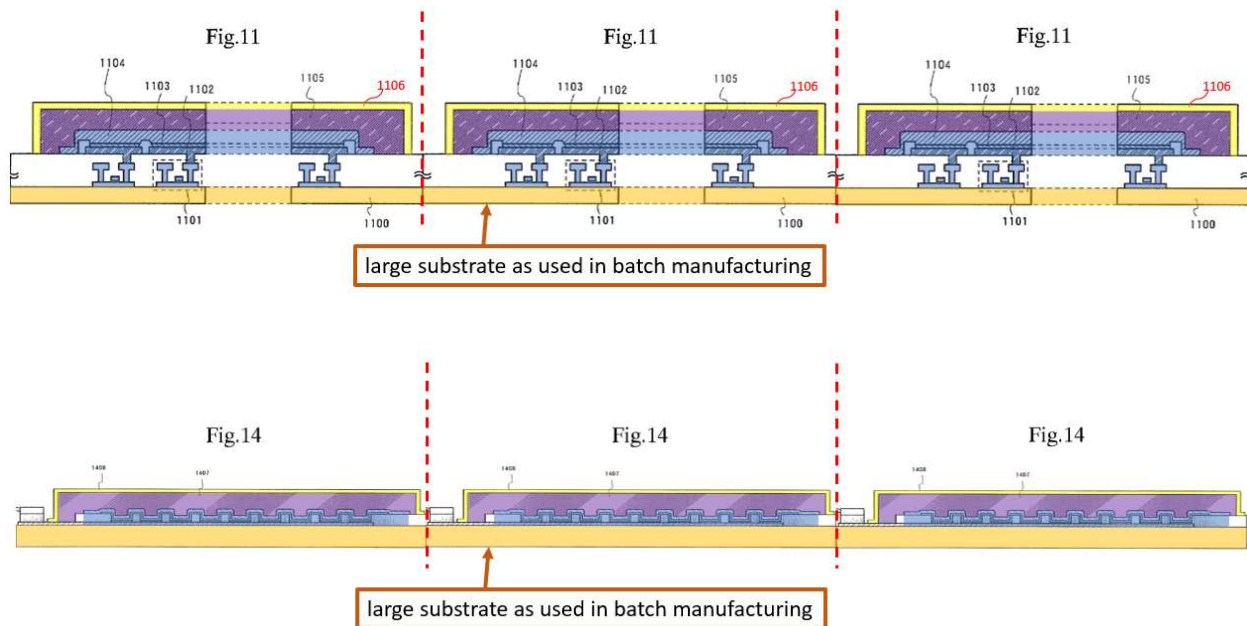
82. Referring to Figure 2, the '389 patent admits that "[a]s depicted, *OLED devices 202* are typically laid down in rows and columns on a large sheet of glass 200,"

83.To the extent that any separate reference is necessary to confirm that it was known to manufacture OLED devices such as those of Yamazaki in batch on a large sheet of substrate, the prior art Ghosh reference teaches precisely this. Specifically, Ghosh teaches batch fabrication (and encapsulation) of OLED devices, as it discloses an encapsulation assembly “for a plurality of OLED display devices 3 on a substrate 2” as shown in the cross-sectional view (Figure 3) and top-down view (Figure 5), as I have indicated below. Ghosh, [0031].



Id., Figs. 3, 5 (annotated). Ghosh explains that “[t]he dashed lines 25 in FIG. 5 indicate where the substrate would be cut as part of the dicing operation following completion of the encapsulation assembly.” *Id.*, [0032].

84. Accordingly, in my opinion, it would have been obvious to use Yamazaki’s encapsulation methods in batch fabrication—that is, to apply Yamazaki’s methods for *encapsulating a plurality* of OLED display panel devices on a large sheet of substrate. I have illustrated this in the following annotation, by laying multiple instances of Figure 11 side-by-side, and multiple instances of Figure 14 side-by-side, and (in both cases) included red vertical lines to indicate where the encapsulated devices would subsequently be separated (i.e. “singulated” or “diced”) into individual devices:



Yamazaki, Figs. 11 and 14 (replicated and annotated).

85. In my opinion, a POSITA would have been motivated to apply Yamazaki's encapsulation methods, as in the embodiments of Figures 11 and 14, for batch manufacturing multiple display panels on a large sheet of substrate, which was the conventional mode of manufacturing display panels for OLEDs. Specifically, a POSITA would have recognized that batch manufacture, by increasing the number of panels processed at one time, improves throughput, improves productivity, and reduces manufacturing costs.

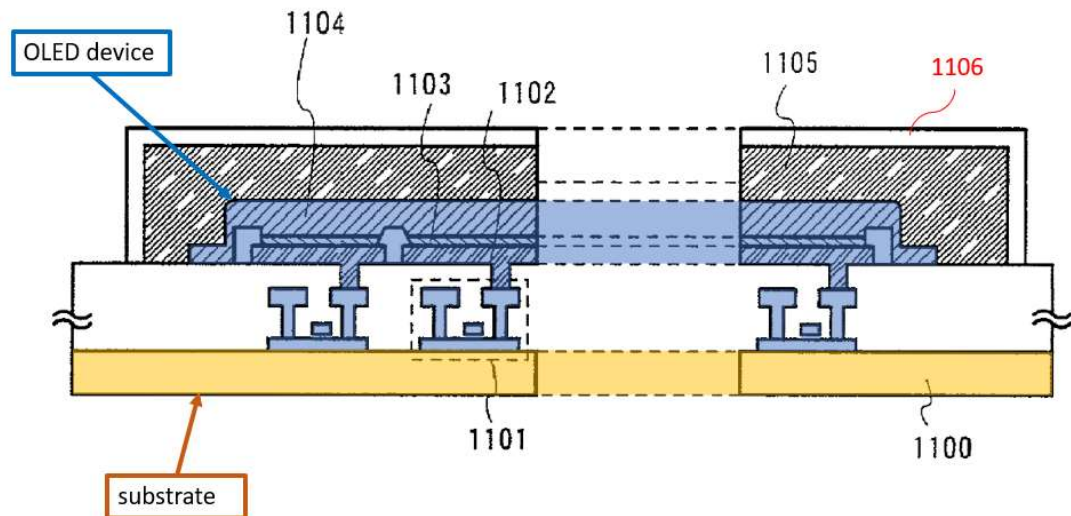
86. Further, in my opinion, a POSITA would have had a reasonable expectation of success in applying Yamazaki's encapsulation methods in batch manufacturing. As the '389 patent admits, in the prior art it was conventional to use batch fabrication to manufacture OLED display devices with thin-film encapsulation. *See* '389 patent, 1:63-2:12. Furthermore, Ghosh, like Yamazaki, is directed to encapsulation of an OLED display device with multiple thin-film layers, where at least the first encapsulation layer 21 is selectively deposited—in other words, “patterned to leave exposed a portion of the substrate surface in between the individual OLED devices.” Ghosh, [0032]. This amounts to the combination of familiar elements according to known methods, in order to yield predictable results.

b. Element 34[a]: “fabricating a plurality of devices on a substrate;”

87. In my opinion, applying Yamazaki’s methods to encapsulate a plurality of OLED display panels in batch manufacturing (in view of AAPA/Ghosh) would satisfy this element, because Yamazaki’s encapsulation methods entail *fabricating* an OLED display device *on a substrate*.

88. In the “active matrix” embodiment of Figure 11, the OLED display panel (*device*) comprises TFTs 1101, pixel electrodes 1102 electrically connected to the TFTs 1101, EL layers 1103, and cathodes 1104. *See* Yamazaki, [0176], [0177]. This device is *fabricated on a substrate* (substrate 1100). *See id.*, [0176] (explaining that manufacturing begins with “TFT 1101 formed on a substrate 1100”). I have demonstrated this my below annotation of Figure 11:

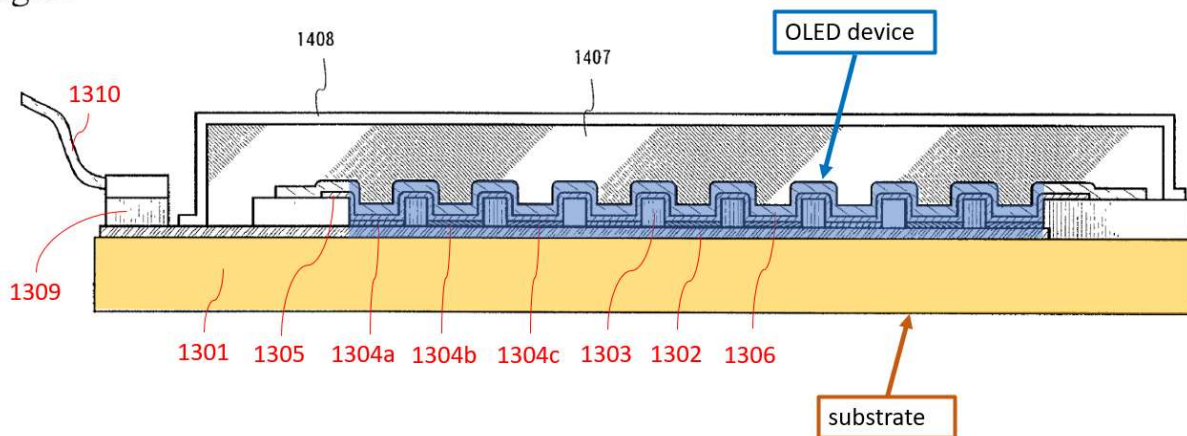
Fig.11



Yamazaki, Fig. 11 (annotated).

89. In the “passive matrix” embodiment of Figure 14, as illustrated below, the OLED display panel (*device*) comprises anode 1302, bank 1303, EL layers 1304a-c, cathode 1305, and protective electrode 1306. *See* Yamazaki, [0186]–[0188]. This device is *fabricated on a substrate* (substrate 1301). *See id.* [0200] (“EL element is ... formed on the substrate 1301”).³ I have demonstrated this in my below annotation of Figure 14.

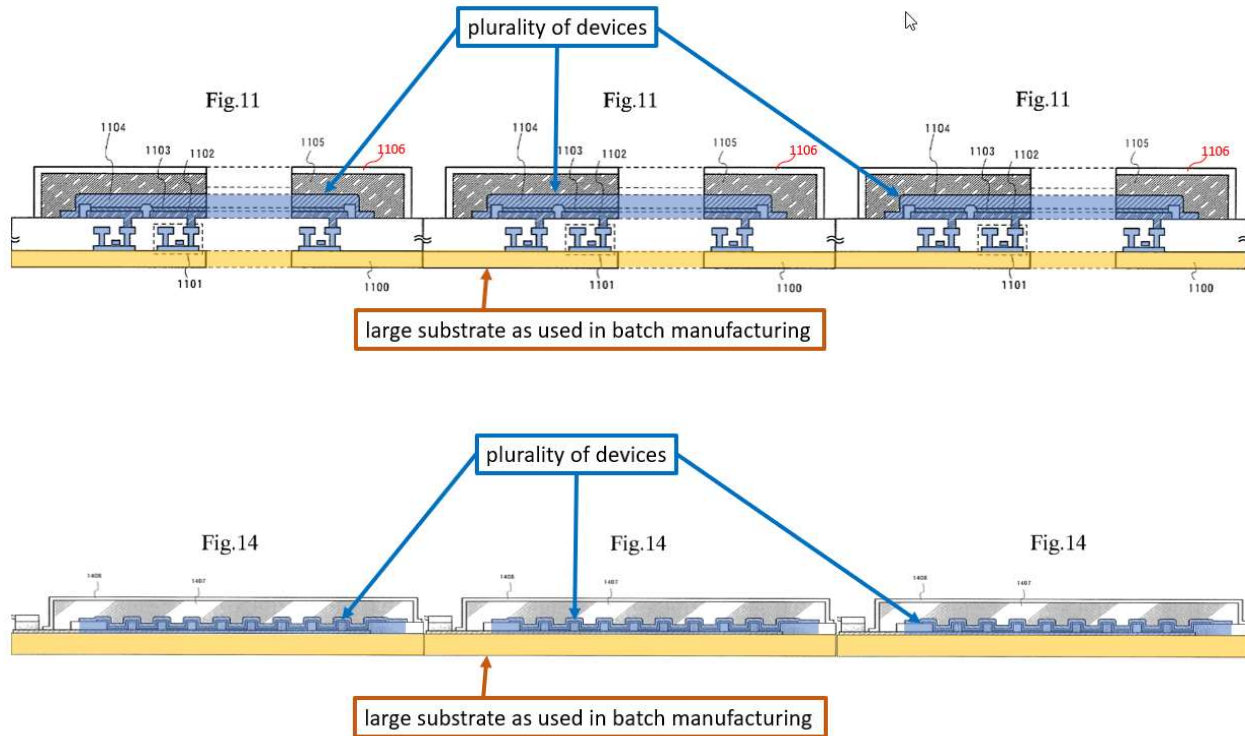
Fig.14



Yamazaki, Fig. 14 (annotated).

90. Thus, using Yamazaki’s methods in batch fabrication (as I discussed above for Element 34[Pre]) would entail *fabricating a plurality* of such OLED *devices* on a large sheet of *substrate* as I have shown in the following annotations:

³ As I discussed above in footnote 2, the embodiments of Figures 13 and 14 are the same except for the arrangement of the cover and barrier layers. Yamazaki’s disclosures for Figure 13 are otherwise equally applicable to Figure 14.



Yamazaki, Figs. 11 and 14 (replicated and annotated).

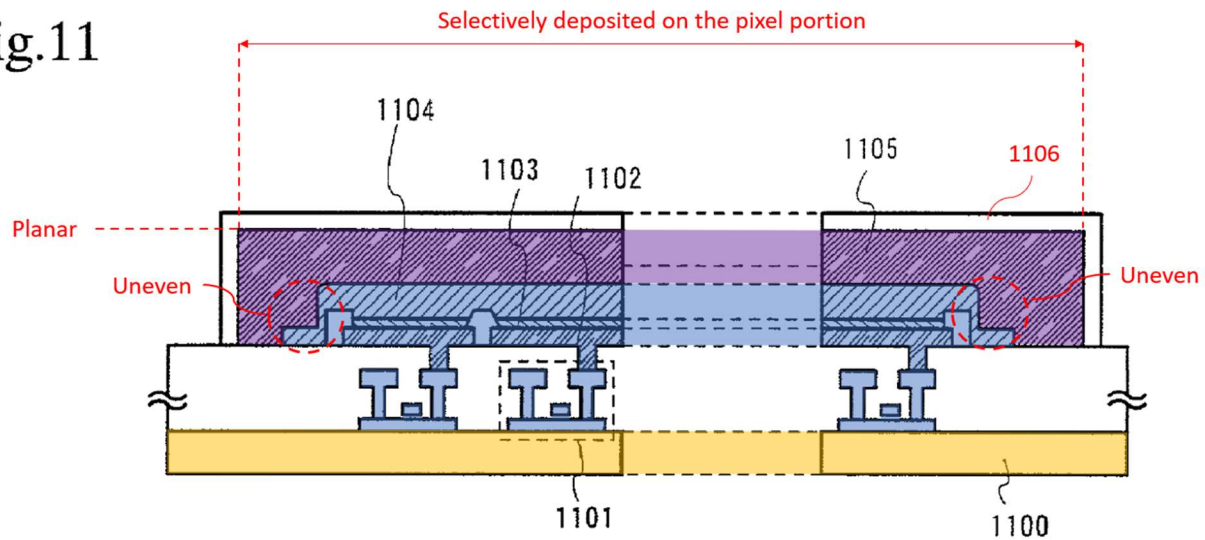
c. Element 34[b]: “selectively depositing at least one planarization layer upon said devices; and”

91. In my opinion, applying Yamazaki’s methods to encapsulate a plurality of OLED display panels in batch manufacturing would satisfy this element, because Yamazaki’s encapsulation methods entail *selectively depositing at least one planarization layer* (specifically, cover layer 1105/1407) *upon* its OLED display device.

92. In the “active matrix” embodiment of Figure 11, the cover layer 1105 (purple) is selectively deposited upon the OLED display panel (blue) as I have shown below. That is, “the ink jet method is ... used to form a cover layer 1105 made of an

organic resin film evenly on the pixel portion.” Yamazaki, [0177]. Ink jet is a “film deposition” method. *Id.*, [0007], Abstract.

Fig.11



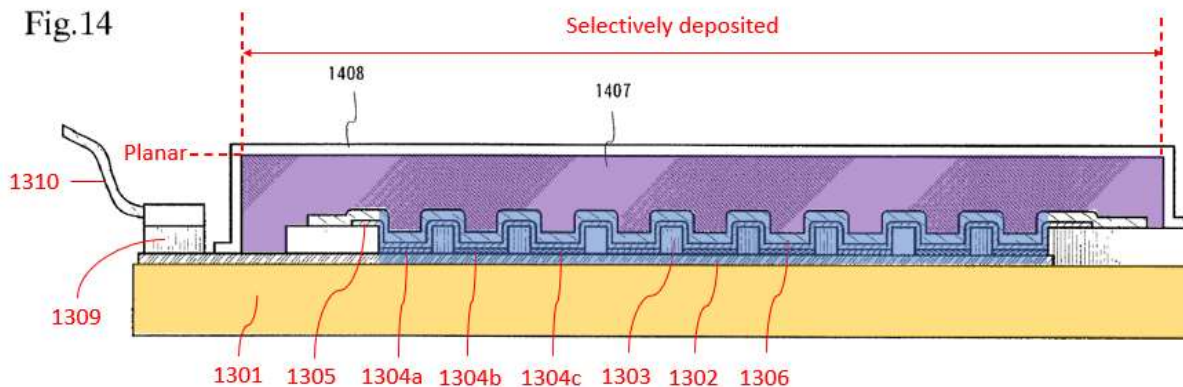
Id., Fig. 11 (annotated).

93. Yamazaki discloses *selectively depositing* the cover layer 1105 upon the display panel. “Because the cover layer 1105 is formed using the ink jet method, it can be *selectively formed* on the pixel portion.” *Id.*, [0178]. This selective deposition is also reflected in my above annotation of Figure 11, which shows that the cover layer is formed only on a certain portion of the underlying structure (specifically, the pixel portion), as opposed to extending laterally across the entire substrate.

94. Furthermore, Yamazaki’s cover layer 1105 constitutes a *planarization layer*. This is demonstrated by Yamazaki’s teaching that “[a]s a material for forming the cover layer 1105 made of an organic resin, it is appropriate to use a material that ... has *planarity*.” *Id.*, [0178]. And as evident in Figure 11, the top of the cover

layer 1105 is planar (in other words, flat), whereas the underlying cathode 1104 has uneven surfaces. Thus, Yamazaki teaches that the uneven surfaces are planarized (or flattened) by the cover layer. Accordingly, the addition of layer 1407 results in a planar surface topography. Further, other prior art references demonstrate the POSITA's knowledge that such an organic layer could be used to "make[] a smooth surface on the relatively irregular surface of the cathode" when forming OLED devices. Suzuki, 5:59-62.

95. Similarly, in the "passive matrix" embodiment of Figure 14, the cover layer 1407 (purple), which is planarizing, is selectively deposited upon the OLED display panel (blue) as I have shown below:



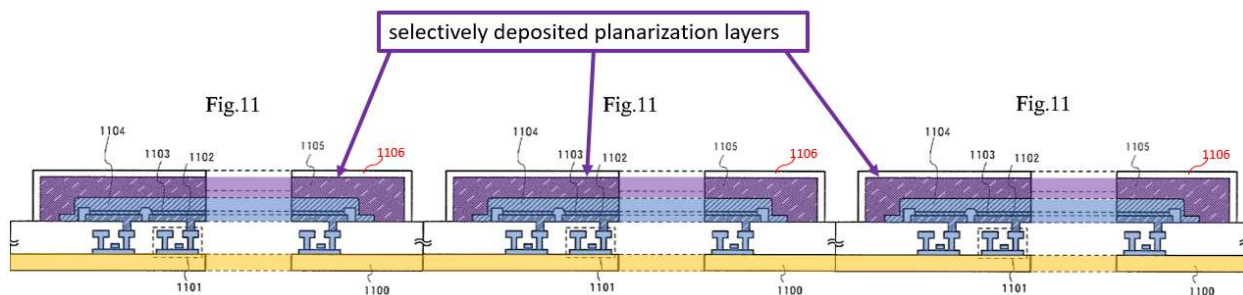
Yamazaki, Fig. 14 (annotated).

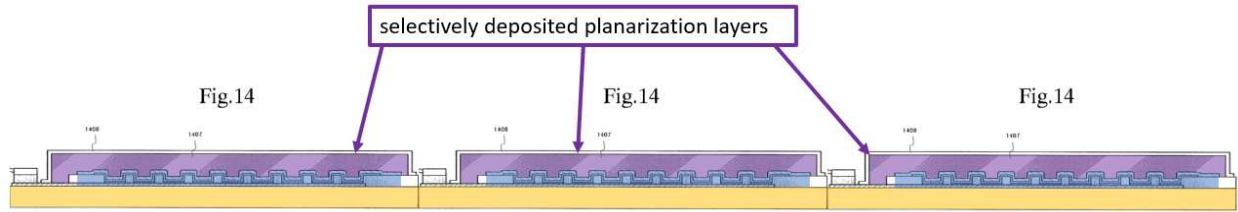
96. Again, Yamazaki discloses *selectively depositing* this cover layer 1407 upon the display panel. Figure 14 shows that the cover layer 1407 encapsulates only the light-emissive areas (specifically, pixels) and leaves exposed the FPC 1310, which would be attached to the contact pads. This is comparable to the selective

deposition described in the '389 patent. '389 patent, 6:2-4 (“[I]t might be desirable to encapsulate only the organic light-emissive areas (e.g. pixels) and leave the contact pads.”). Moreover, Yamazaki explains that “the application liquid for the EL layer can be *selectively* applied on to the desired position of the pixel,” Yamazaki, [0191] and the “cover layer 1308 ... is subsequently formed by the same method used for forming the EL layer,” *id.*, [0202]; *see also id.*, [0035] (“[T]he cover layer ... may be *selectively* formed only at the desired positions.”).

97. As with Figure 11, this cover layer 1407 of Figure 14 constitutes a *planarization layer*, because the top surface of cover layer 1407 is flat even though the underlying structure is uneven. *See id.*, [0178] (teaching that “it is appropriate to use a material that ... has *planarity*” for cover layer 1105 of Figure 11).

98. For all of the above reasons, using Yamazaki’s methods in batch fabrication would entail *selectively depositing at least one planarization layer* upon each of the *devices*, as I have shown in the following annotations:





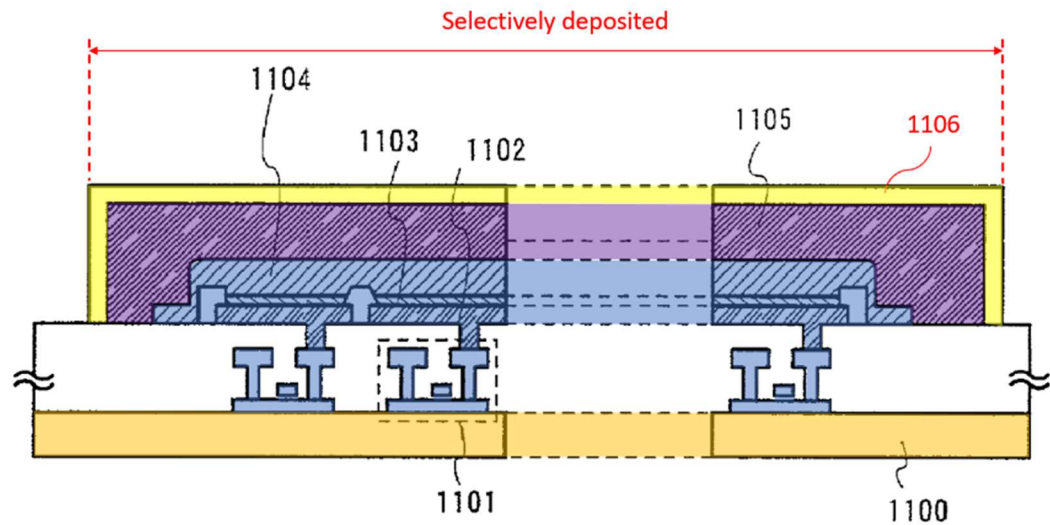
Yamazaki, Figs. 11 and 14 (replicated and annotated).

d. Element 34[c]: “selectively depositing at least one barrier layer over said planarization layer.”

99. In my opinion, applying Yamazaki’s methods to encapsulate a plurality of OLED display panels in batch manufacturing would satisfy this element, because Yamazaki’s encapsulation methods entail *selectively depositing at least one barrier layer* (specifically, either of barrier layers 1106 or 1408) *over said planarization layer* (i.e., either of its cover layers 1105 or 1407).

100. In the “active matrix” embodiment of Figure 11, which I have annotated below, a barrier layer 1106 (yellow) is selectively deposited over the cover layer 1105 (purple). That is, “after the formation of the cover layer 1105, a barrier layer 1106 is formed by sputtering to cover the cover layer 1105.” Yamazaki, [0183]. As a POSITA at the relevant time would have appreciated, sputtering is a deposition method.

Fig.11



Yamazaki, Fig. 11 (annotated).

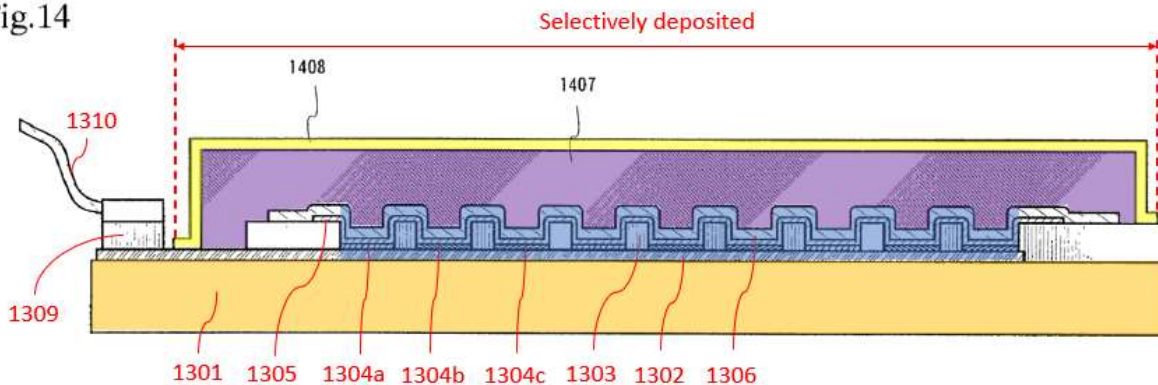
101. Yamazaki’s “barrier layer 1106” is a *barrier layer* under the ’389 patent, in that it is “provided for the purpose of preventing moisture and oxygen from penetrating into the EL layer.” Yamazaki, [0033]. This is quite like the ’389 patent’s barrier layer, which, according to the patent, “provides the necessary environmental isolation from the corrosive effects of oxygen and moisture.” ’389 patent, 1:38-41; *see also* Yamazaki, [0184] (“[B]y forming the cover layer 1105 and the barrier layer 1106 on the active matrix substrate, the invasion of degrading factors to the EL element, such as moisture and oxygen, from the outside can be prevented.”).

102. Yamazaki further discloses *selectively depositing* the barrier layer 1106 over the cover layer 1105 (i.e., *planarization layer*). Specifically, Yamazaki states, “[i]t is note[d] that the barrier layer 1106 is formed selectively using a shadow

mask.” *Id.*, [0183]. This selective deposition is also evident in Figure 11, which shows that the barrier layer is formed only on a certain portion of the underlying structure (specifically, over the cover layer 1105), as opposed to extending laterally across the entire substrate.

103. Similarly, in the “passive matrix” embodiment of Figure 14, the barrier layer 1408 (yellow) is selectively deposited over the cover layer 1407 (purple), as I have shown in the below annotation:

Fig.14



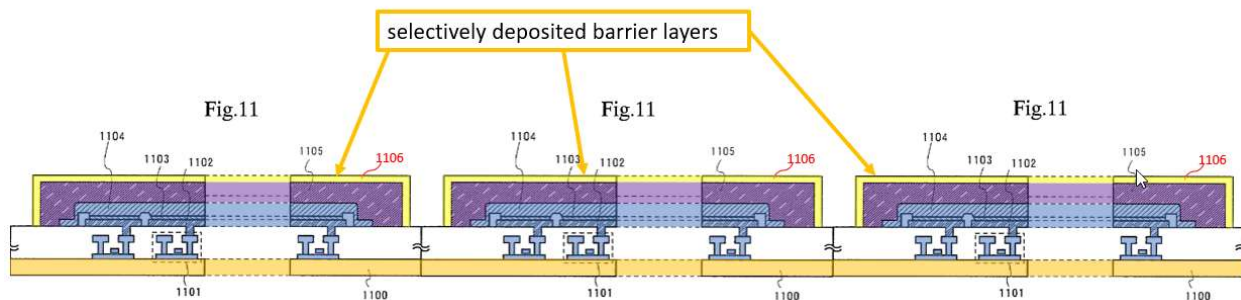
Id., Fig. 14 (annotated).

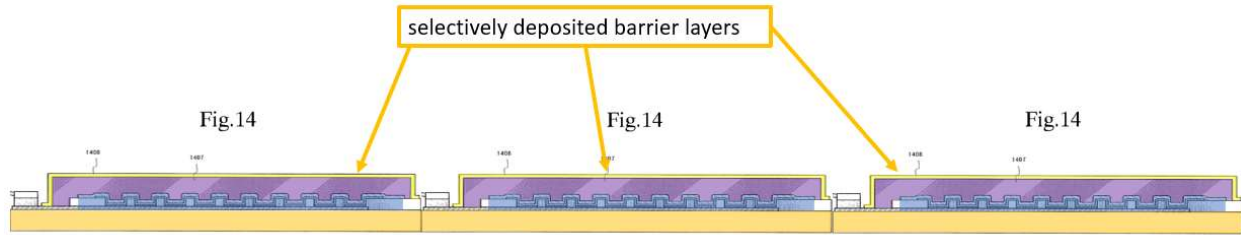
104. As with Figure 11, this barrier layer 1408 is provided for the same purpose as the *barrier layer* in the '389 patent. *See* Yamazaki, [0008] (“By further forming a film made of an inorganic material (hereinafter referred to as a barrier layer) on the cover layer, moisture and oxygen can be prevented from permeating into the cover layer or the EL layer.”), [0033] (“It is to be noted that the barrier layer is referred to as a passivation film provided for the purpose of preventing moisture

and oxygen from penetrating into the EL layer and formed of an inorganic material.”).

105. And once again, this barrier layer 1408 is *selectively deposited* over the cover layer 1407 (i.e., *planarization layer*). As shown in Figure 14, the barrier layer is formed only on a certain portion of the underlying structure (i.e., over the cover layer 1407), as opposed to extending laterally across the entire substrate. Figure 14 shows that the barrier layer 1408 encapsulates only the cover layer 1407 and leaves exposed the FPC 1310, which would be attached to the contact pads. This is just like the selective deposition described in the '389 patent, 6:2-4 (“[I]t might be desirable to encapsulate only the organic light-emissive areas (e.g. pixels) and leave the contact pads.”).

106. Accordingly, using Yamazaki’s methods in batch fabrication would entail *selectively depositing at least one barrier layer* over each *planarization layer*, as I have shown in the following annotations:





Yamazaki, Figs. 11 and 14 (replicated and annotated).

2. Dependent Claim 35: “The method as recited in claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by ink jet of an organic layer.”

107. In my opinion, Yamazaki satisfies the additional element of dependent claim 35. Specifically, as in the “active matrix” embodiment of Figure 11, Yamazaki teaches that the *planarization layer* of the Figure 11 embodiment (cover layer 1105) is formed by *depositing by ink jet of an organic layer*:

After forming the cathode 1104, the **ink jet** method is again used to form a cover layer 1105 made of an **organic resin film** evenly on the pixel portion.

Yamazaki, [0177]. Yamazaki’s other disclosures support this. *See id.* at [0011] (“The multi-chamber employed for the purpose of attaining the above object is a film deposition device which has an application chamber for forming the EL layer and the cover layer made of an organic material by the ink jet method”); [0034] (“[T]he cover layer is formed in the application chamber by means of the ink jet method, similar to the formation of the EL layer ...”).

3. Dependent Claim 37: “The method as recited in claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing an organic layer through a shadow mask.”

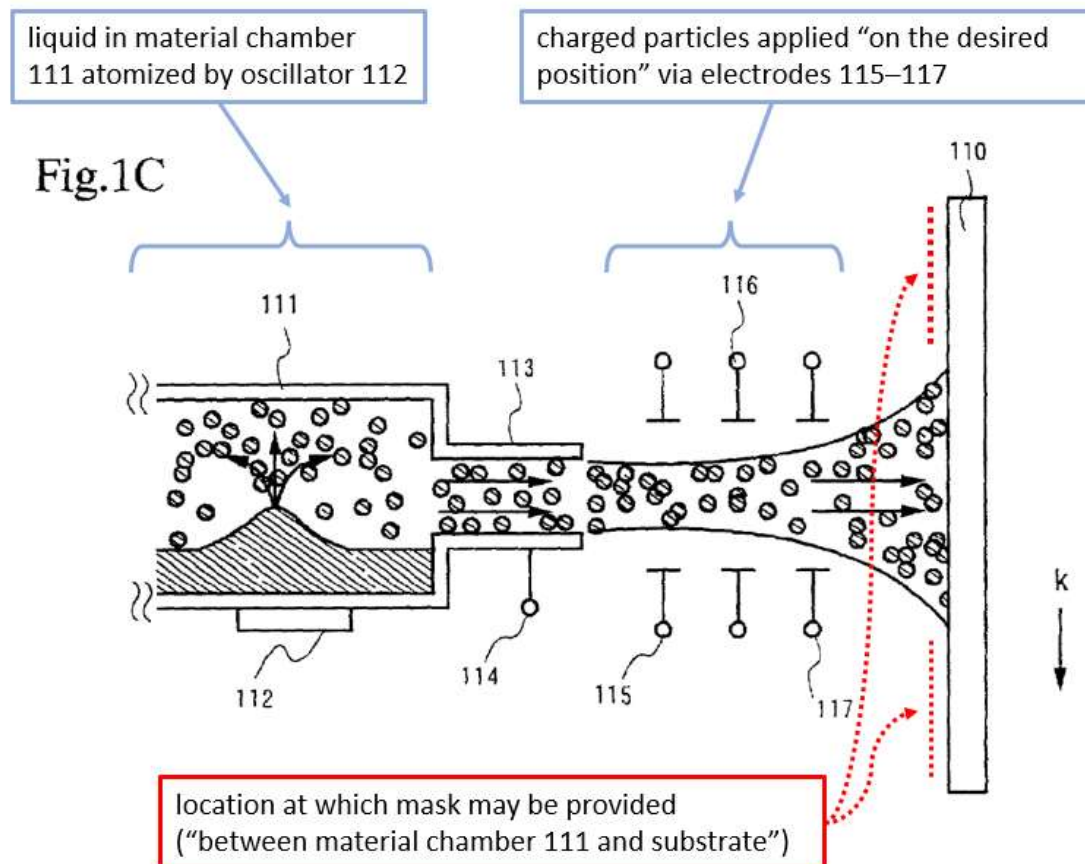
108. In my opinion, Yamazaki satisfies the additional element of dependent claim 37, because Yamazaki teaches that the *planarization layer* (cover layer) is formed by *depositing an organic layer through a shadow mask*. Additionally, this element is obvious in view of Ghosh’s teachings.

109. **First**, Yamazaki discloses that the cover layer in its embodiments is an *organic layer*, because is “made of organic material,” specifically an “organic resin film.” Yamazaki, [0011], [0177], [0178], [0202].

110. **Second**, Yamazaki teaches *depositing* this organic layer *through a shadow mask*. Yamazaki explains that the cover layer used in its self-emission device embodiments is “subsequently formed by the same method for forming the EL layer.” *Id.*, [0202]. Yamazaki further explains that the EL layer is “formed by using the electric field application method described in Embodiment 1.” *Id.*, [0188]. As to that embodiment, Yamazaki teaches that “a mask may be provided ... to thereby control the positions on the substrate” where the material is applied, *id.*, [0086].

111. Yamazaki discloses that the electric field application method uses the apparatus of Figure 1C to selectively apply the deposition material. As I have annotated in Figure 1C below, Yamazaki teaches that application liquid in a

“material chamber 111” is first “atomized by the ultrasonic oscillator 112”; then “become[s] charged particles through influence of an electric field”; and is thereafter “extracted,” “accelerated,” and “controlled” by electrodes 115–117 such that it is “applied on the desired position.” Yamazaki, [0082].



Id., [0082], Fig. 1C (annotated).

112. As to this method, Yamazaki additionally discloses that “a **mask** may be provided between the material chamber 111 and the substrate to thereby control the positions on the substrate at which the application liquid is [applied] via the mask.” *Id.*, [0086]. A POSITA would understand that this mask qualifies as a

shadow mask, because it prevents the deposition of the material in the areas where mask is present, but allow the deposition of the material in the areas of the mask openings. Other prior art references demonstrate this. *See* Burrows-631, 1:22-26 (“A ‘shadow’ mask is a mask having apertures through which material is deposited onto a substrate, as opposed to an optical mask, which is used to selectively expose photoresist on a substrate to radiation.”). I note that while this discussion is in relation to the embodiment of Figure 14, a POSITA would recognize that this approach could also be applied to other embodiments, including the active matrix embodiment of Figure 11.

113. **Third**, to the extent there is any question whether Yamazaki teaches or suggests shadow mask, it would nevertheless have been obvious to a POSITA to selectively deposit Yamazaki’s organic cover layer (i.e., *planarization layer*) through a shadow mask based on Ghosh, which discloses a method for depositing an organic encapsulation layer through a shadow mask. Ghosh, [0032].
114. Yamazaki teaches that its organic cover layer may be applied using alternative selective deposition methods. In particular, Yamazaki discusses use of a “film deposition device ... for forming the EL layer and the cover layer made of an organic material by the *ink jet method* or the *electric field application method*.” Yamazaki, [0011]. Yamazaki cites these as known “film deposition” methods in its “Description of the Related Art.” *Id.*, [0003]. In this regard, Yamazaki’s

disclosure is consistent with other prior art references, which teach that organic planarization layers can be selectively deposited using various methods. *See, e.g.*, Palanisamy, [0021]-[0025] (discussing that a “passivation [layer] may be selectively applied” using ink jet printer, shadow mask, or screen printing).

115. Depositing through a shadow mask was among these known selective deposition methods, as taught for example in Ghosh. In addition, the ’389 patent acknowledges that “[i]t will be appreciated that there are many manners of depositing this organic [planarization] layer upon the OLED device.” ’389 patent, 4:48-49, further explaining that “[t]he manner of selectively depositing the organic [planarization] layer ... may be accomplished in a variety of ways,” including “through a shadow mask.” *Id.*, 6:66-7:3. I note that the ’389 patent presumes that a POSITA would know how to employ a shadow mask to deposit the planarization layer, as demonstrated by the fact that the patent does not provide any detail on how to use the shadow mask. *Id.*, 6:66-7:20.

116. A POSITA would have recognized that a shadow mask could be used to selectively deposit Yamazaki’s cover layer. The prior art Ghosh reference discloses such a known technique, teaching that “patterning [of the first encapsulation layer] may be achieved by any well-known, conventional means, including *shadow masking* before layer formation.” Ghosh, [0032]. Ghosh demonstrates that this technique achieves selective deposition, explaining that the

layer “is patterned to leave exposed a portion of the substrate surface in between the individual OLED devices.” *Id.* Ghosh further explains that “the first encapsulation layer comprises a polymer, and more preferably, that polymer comprises a parylene,” which a POSITA would have recognized as an organic material. *Id.*, [0015]. As Burrows-631 demonstrates, “[t]he use of a shadow mask to deposit [] patterned thin films on the substrate is well known in the art.” Burrows-631, 1:20-22. In other words, a shadow mask was one of a finite number of identified, predictable solutions for achieving selective deposition of a planarization layer, such that a POSITA would have had reason to pursue for selectively depositing Yamazaki’s cover layer.

117. In my opinion, a POSITA would have been motivated to use the shadow mask disclosed in Ghosh to selectively deposit the cover layer in Yamazaki. Although other selective deposition techniques may have their own benefits, a POSITA would have recognized the benefits of using the shadow mask in certain circumstances, such as in connection with Yamazaki’s method. I understand that for analyzing obviousness, it is not required that the motivation be the best option, only that it be a suitable option from which the prior art did not teach away. Here, using a shadow mask allows for good control of the positions on the substrate where the planarizing layers are formed. Furthermore, a POSITA would have

appreciated that shadow masks can be used in conjunction with other processes for depositing a layer of liquid material, such as flash evaporation.

118. In my opinion, a POSITA also would have had a reasonable expectation of success of depositing the cover layer in Yamazaki through the shadow mask as disclosed in Ghosh. Like the cover layer in Yamazaki, the first encapsulation layer in Ghosh preferably comprises an organic polymer, such as a “parylene.” Ghosh, [0015]. A POSITA would have understood that parylene is a planarizing material. This is demonstrated, for example, by the Weaver reference. *See* Weaver, [0035] (“Preferred planarizing materials are polymers, such as ... parylenes.”). In fact, I see that during prosecution, the Applicant did not dispute that Ghosh’s first encapsulation layer is a planarization layer or that Ghosh’s first encapsulation layer is selectively deposited. Thus, a POSITA would have recognized that Ghosh’s disclosures for selectively depositing its first encapsulation layer are readily applicable to Yamazaki’s organic cover layer.

119. For all of the above reasons, claim 37 would have been obvious based on Yamazaki and Ghosh.

4. Dependent Claim 40: “The method as recited in claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by shadow mask, sputtering, ink jet deposition, screen printing evaporation.”

120. In my opinion, Yamazaki satisfies the additional element of dependent claim 40. Specifically Yamazaki discloses that the barrier layer is deposited using a

shadow mask, by *sputtering*, and by *evaporation*. By way of example, as for the embodiment of Figure 11:

[A] barrier layer 1106 is formed by **sputtering** to cover the cover layer 1105.... It is note[d] that the barrier layer 1106 is formed selectively using **a shadow mask**.

Yamazaki, [0183]. Likewise for Figure 14, “[t]he barrier layer can be formed by plasma CVD, *sputtering*, or *evaporation*.”). Yamazaki, [0201]. Yamazaki’s other disclosures support this conclusion. *See id.*, [0011] (“a **sputtering** chamber for forming the barrier layer”), [0034] (“Using **sputtering** or plasma CVD, the barrier layer is formed ...”), [0141] (“The barrier layer 353 is formed by employing **sputtering** ...”).

B. Ground II: Claims 41-46 Are Obvious Over Yamazaki in View of AAPA/Ghosh and Fujimori

121. In my opinion, Claims 41-46 would have been obvious based on Yamazaki in view of AAPA and/or Ghosh and further in view of Fujimori. As with claim 34, these claims likewise relate to a method of encapsulating a plurality of devices via at least one planarization layer and barrier layer, but unlike claim 34, these claims also specify particular requirements for using a mask when depositing the planarization layer.

122. As I describe further below, Fujimori discloses an approach for manufacturing OLED display elements using a “mask attached to a substrate with magnetic force.” Fujimori, [0010]. In particular, Fujimori teaches that its approach is advantageous over conventional masking techniques, for which “adhesion between the substrate and mask deteriorates due to warping and other factors,” *id.*, [0008], thereby “achiev[ing] favorable pattern processing accuracy,” *id.*, [0009]. In my opinion, and as I discuss below, it would have been obvious to use this magnetic masking approach for applying Yamazaki’s methods to encapsulate a plurality of OLED display panels in a batch manufacturing process.

1. Claim 41:

a. Element 41[Preamble]: “A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

123. In my opinion, to the extent the preamble is limiting, it is obvious based on Yamazaki in view of the admitted prior art and/or Ghosh for the same reasons I have set forth for Element 34 [preamble] in Ground I above, which is identical. More specifically, Yamazaki discloses a *method of encapsulating* an OLED display panel *device fabricated upon a substrate*, as shown in Figures 11 and 14 (which I have annotated below), and it would have been obvious to apply these methods for *encapsulating a plurality* of such display devices during batch

fabrication of multiple OLED devices, as was known based on the admitted prior art and as further taught by Ghosh.

Fig.11

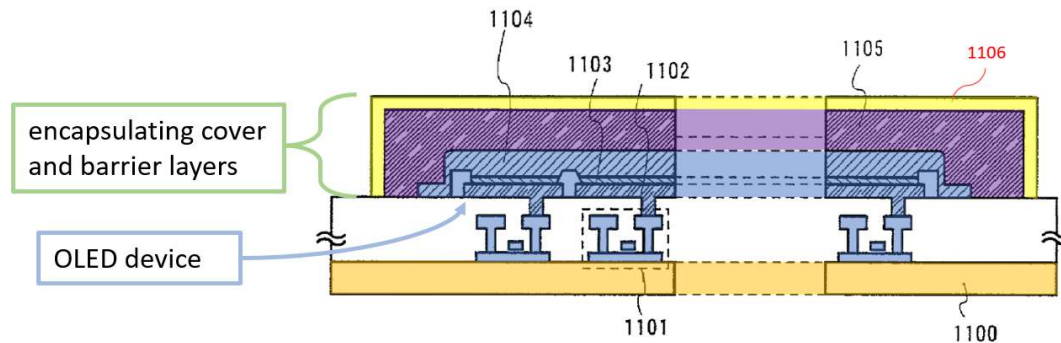
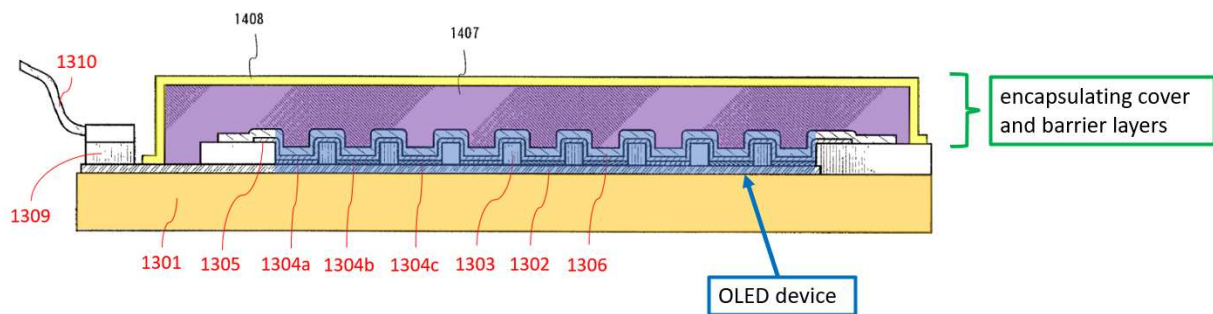


Fig.14



Yamazaki, Figs 11 and 14 (annotated).

b. Element 41[a]: “fabricating a plurality of devices on a substrate;”

124. In my opinion, applying Yamazaki’s methods to encapsulate a plurality of OLED display panels in batch fabrication would satisfy this element for the same reasons I have set forth above for Element 34[a] in Ground I above, which is identical. More specifically, Yamazaki’s encapsulation methods entail *fabricating* an OLED display device *on a substrate*, as I have annotated below in Figures 11 and 14.

Fig.11

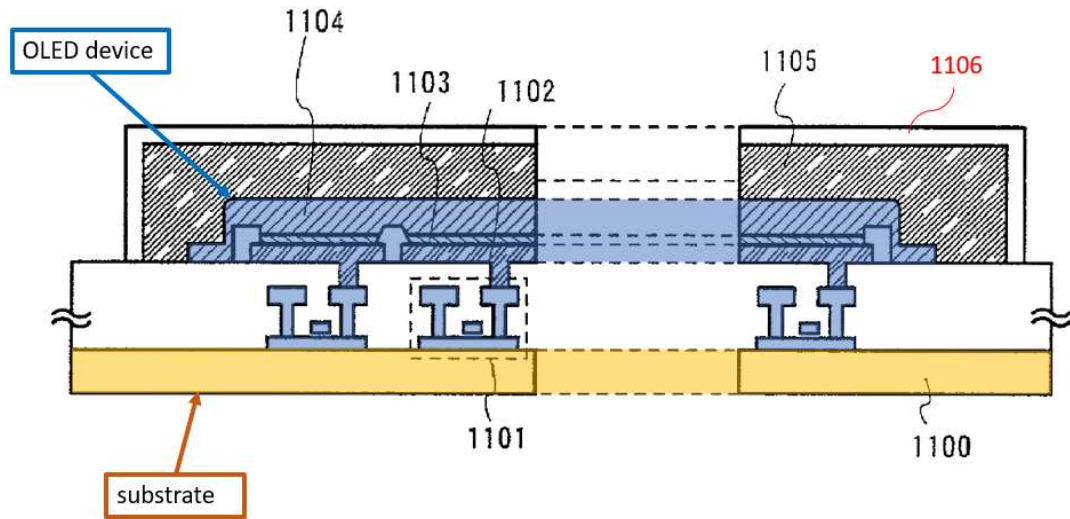
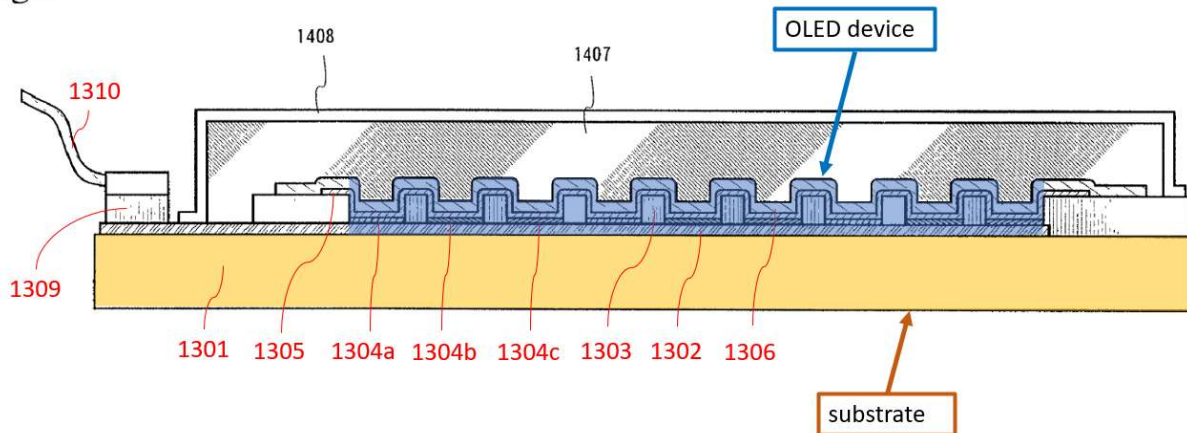


Fig.14



Yamazaki, Figs 11 and 14 (annotated).

- c. **Element 41[b]: “depositing a mask on top of said substrate, such that the mask openings are placed on top of said devices;”**

125. In my opinion, this element would have been obvious in view of the further teachings of Fujimori. As I explain below, it would have been obvious to use Fujimori’s magnetic masking approach for selectively depositing Yamazaki’s

planarizing “cover layer.” Further, doing so in batch manufacturing would entail *depositing a mask* (specifically, Fujimori’s magnetically held mask) *on top of said substrate* (Yamazaki’s substrate as I have identified for Element34[a] in Ground I above) *such that the mask openings are placed on top of said devices* (a plurality of OLED display devices as I have identified above).

126. As I have discussed for Claim 37 above, Yamazaki teaches that its organic cover layer may be applied using alternative selective deposition methods. Yamazaki specifically discusses use of a “film deposition device . . . for forming the EL layer and the cover layer made of an organic material by the *ink jet method or the electric field application method*.” Yamazaki, [0011]. Yamazaki cites these as known “film deposition” methods in its “Description of the Related Art.” *Id.*, [0003]. In addition, Yamazaki further notes that “a mask may be provided” in its electric field method to “control the positions on the substrate” where the material is deposited. *Id.*, [0086].

127. I note that Yamazaki’s disclosure is consistent with other prior art references, which teach that organic planarization layers can be selectively deposited using various methods. *See, e.g.,* Palanisamy, [0021]-[0025] (discussing that a “passivation [layer] may be selectively applied” using an ink jet printer, a shadow mask, or screen printing). Indeed, I note that the ’389 patent itself acknowledges that “[i]t will be appreciated that there are many manners of depositing this

organic [planarization] layer upon the OLED device. '389 patent, 4:48-55, further explaining that “[t]he manner of selectively depositing the organic [planarization] layer ... may be accomplished in a variety of ways,” including “through a shadow mask.” '389 patent, 6:66-7:3; *see also id.*, 7:3-5 (“In fact, generally any printing techniques suitable to deliver the desired planarization layer material can be used.”).

128. Likewise, the '389 patent acknowledges that “[i]t will be appreciated that a suitable mask might be formed in many possible manners.” 7:26-27.

129. To that end, Fujimori discloses a particular approach in which OLED elements are “formed through a mask attached to a substrate with magnetic force.” Fujimori, [0010]. According to Fujimori, this allows for increased precision:

An important feature of the present invention is that the adhesion between the mask and the substrate is improved by magnetic force. This effect reduces the proportion of the area where the deposited material or other material wraps around, i.e., the portion deposited from the mask opening that bleeds to the shadow portion of the mask, achieving fine pattern processing not conventionally possible.

Id., [0029].

130. According to Fujimori, with conventional masks, “adhesion between the substrate and mask deteriorates due to warping and other factors,” which “mak[es] it difficult to pattern the element with adequate accuracy. *Id.*, [0008]. However, the adhesion between Fujimori’s mask and the substrate is “improved [with] magnetic force,” thereby overcoming this problem. *Id.*, [0029].
131. Fujimori further explains that its magnetically held mask may be used for forming not only the OLED elements “involved in the light emission” but also for “non-light-emitting portions formed for the purpose of improving the contrast, pattern accuracy, and electrical insulation of the portions involved in light emission according to need, and therefore are not particularly limited.” *Id.*, [0023]. By way of example, its mask is suitable for organic light-emitting layers, *id.*, [0024]-[0025], electrodes, *id.*, [0026], and “non-light-emitting portions to be patterned ... [which] are not particularly limited,” *id.*, [0027].
132. Accordingly, in my opinion, a POSITA at the time of the alleged invention would have been motivated to use Fujimori’s magnetic masking approach for selectively depositing Yamazaki’s cover layer. While other techniques may have their own benefits, a POSITA would have recognized the benefits of using a magnetic masking approach as taught by Fujimori.
133. **First**, Yamazaki states that an “object of [its] invention is to form the cover layer *at a desirable position with good control.*” *Id.*, [0010]; *see also id.*, [0035]

(“the layers may be selectively formed *only at* the desired positions”). Indeed, a POSITA at the time of the alleged invention would have appreciated that insufficient control over the deposition may have undesirable effects, including unduly expanding the footprint of the cover layer beyond an intended area. Fujimori’s approach allows for improved accuracy. *See id.*, [Abstract].

134. **Second**, a POSITA at the time of the alleged invention would have appreciated that shadow masks and/or the underlying substrate are vulnerable to problems of warping or bending, which likewise adversely impact control over how the deposited layers are patterned. Fujimori recognizes that “adhesion between the substrate and mask deteriorates due to warping and other factors,” which “mak[es] it difficult to pattern the element with adequate accuracy. Fujimori, [0008]. Accordingly, in my opinion, a POSITA would have found additional motivation to employ Fujimori’s magnetically held mask to selectively deposit Yamazaki’s cover layer, to counter the adverse effects of warping, and to otherwise afford precision sufficient to achieve Yamazaki’s objective of “good control” and “desirable position[ing]” when depositing the cover layer.

135. **Third**, Fujimori’s magnetic masking approach would further Yamazaki’s provision that the “same method is used to form the EL layer and ... cover layer.” Yamazaki, [0008]. As noted above, Fujimori’s mask is suitable for organic light-emitting layers, Fujimori, [0024]-[0025], electrodes, *id.*, [0026], and “non-light-

emitting portions to be patterned ... [which] are not particularly limited,” *id.*, [0027].

136. In this regard, Fujimori’s magnetic masking approach would also be advantageous when forming Yamazaki’s OLED display, in order to “achieve favorable pattern processing accuracy”. Fujimori, [0009]. That is, Fujimori’s magnetic masking approach allows for advanced displays with fine pattern pitches (i.e., small pixel spacing, where the “pitch” is the distance between the centers of adjacent pixels). That is:

[W]ith conventional methods, the finer the pattern is, the more the position of the deposited material wrapping around the shadow of the mask cannot be ignored, making it difficult to pattern the element with adequate accuracy. This is a major problem that can cause a short in the elements and crosstalk due to increased leakage current.

Id., [0008]. According to Fujimori, its magnetic mask alleviates such issues, thereby “achieving fine pattern processing not conventionally possible.” *Id.*, [0029]. Accordingly, using Fujimori’s approach for Yamazaki’s EL and cover layers would permit the manufacturing of more advanced, higher resolution OLED displays.

137. In addition, a POSITA would have recognized that Fujimori’s magnetic masking approach may also may be used to selectively deposit Yamazaki’s

barrier layer, thus further simplifying the manufacturing process. Yamazaki already contemplates that “the barrier layer 1106 is formed selectively using a shadow mask.” Yamazaki, [0183]. Thus, Yamazaki’s masking approach is readily applicable to forming the barrier layer.

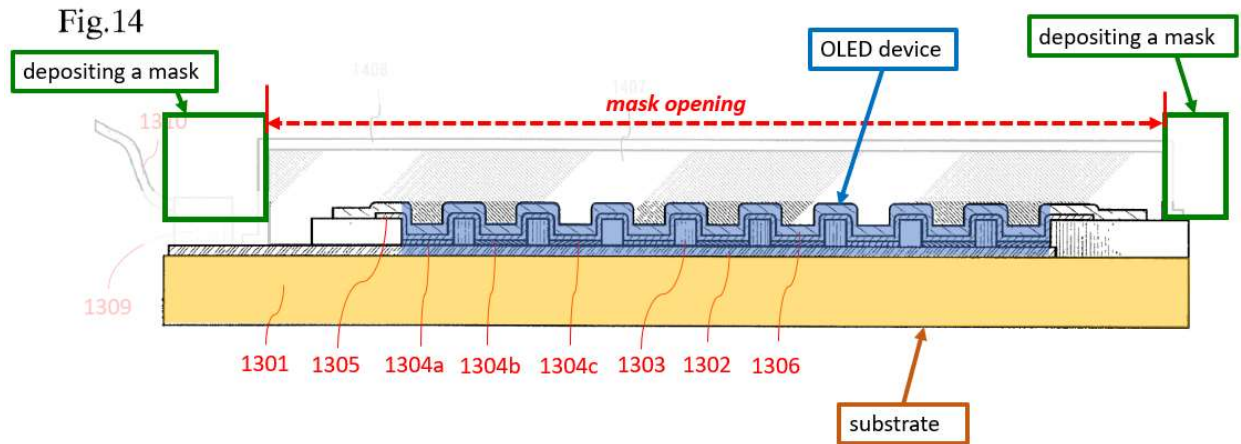
138. In addition, in my opinion, a POSITA would have reasonably expected success in using Fujimori’s magnetic masking approach to form the OLED device, cover layer, and barrier layer of Yamazaki’s embodiments. Yamazaki, like Fujimori, contemplates using the same method to selectively deposit both light-emitting layers (such as Yamazaki’s EL layer), and non-light emitting layers (such as Yamazaki’s cover layer). While Yamazaki’s approach involves selectively depositing these layers in an application chamber using ink jet or electric field, it does not foreclose using other techniques, it does not foreclose using other techniques, which the ’389 patent admits were known in the art.

139. In my opinion, combining the teachings of Fujimori with Yamazaki would have constituted nothing more than the application of known techniques (specifically, forming and encapsulating an OLED device using an magnetically held mask as taught by Fujimori’s) to a known method ready for improvement (here, Yamazaki’s encapsulation methods as illustrated in its Figure 11 and 14 embodiments), to yield predictable results (greater precision in forming OLED

* * *

Fig.11





Yamazaki, Figs. 11 and 14 (annotated). That is, the mask would be placed with openings where the cover layer is to be selectively deposited.⁴

⁴ I note that, as drafted, Figure 14 of Yamazaki appears to depict a “bank” that extends beyond the right side of the OLED device. This suggests that the surface to the right of the cover layer may be higher than the surface to the left of it. Further, I have greyed out the “anisotropic conductive film 1309” and “flexible printed circuit,” i.e., “FPC 1310,” as Yamazaki explains that those features are attached *after* the cover layer is deposited. See Yamazaki, [0157], [0202]. In my opinion, a POSITA would have appreciated, based on Fujimori’s disclosure, that improved adhesion may be obtained even with such an uneven surface, with proper “positional affixing” and ensuring that the “magnitude of the magnetic force” is “adequate.” Fujimori, [0030]. In any event, to the extent that an uneven surface would affect the proper adhesion of Fujimori’s mask, a POSITA would appreciate that this issue may

141. In my opinion, applying Fujimori’s magnetic mask would constitute *depositing a mask on top of said substrate*. Fujimori teaches that its mask is adhered to the underlying substrate by magnetic force, explaining that: “[W]hen the mask is affixed with mechanical contact, the magnetic force should be adequate to obtain the mask adhesiveness required, and if the mask is affixed with magnetic force, the magnetic force should be adequate for *mask adhesion and positional affixing*.” Fujimori, [0030]; *see also id.*, [Abstract] (“An organic electroluminescent element ... is formed through a mask *attached to a substrate* with magnetic force.”); [0009] (“[A]n object of the present invention” is “to provide a method to achieve adequate *adhesion between the mask and the substrate*.”); [0037] (“[I]t is advantageous to use a mask with high planarity in order to achieve uniform adhesion between the mask and the substrate.”)

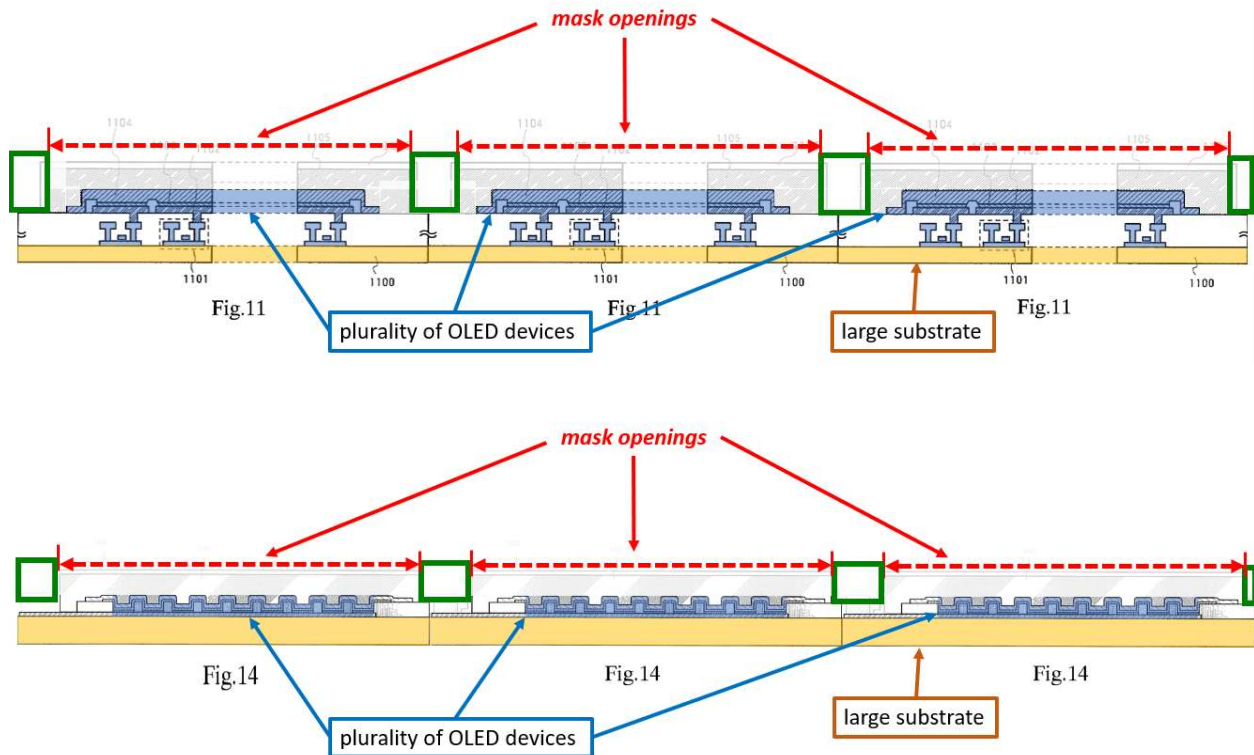
142. In my opinion, adhering the mask in this manner would constitute *depositing a mask* on top of said substrate within the meaning of the ’389 patent. Indeed, the ’389 patent explains that its mask 604 “could be made of magnetic material and

be readily alleviated by adjusting the geometry of Yamazaki’s device (for example, by having the bank symmetrically extend beyond both sides of the OLED, or neither) or Fujimori’s mask, so that the mask sufficiently follows the contours of the underlying surface.

thus held by magnetic forces,” in describing manners through which the “mask 604 is deposited.” ’389 patent, 7:47-49, 7:54-55. And dependent claim 42 specifies that the “step of depositing” recited in this Element 41[b] may “comprise[] ... depositing a ... magnetically held mask.” *Id.*, cl. 42.

143. In my opinion, using Fujimori’s magnetic masking approach for the cover layer 1105/1407 would further entail depositing the mask *such that mask openings are placed on top of said devices*. Fujimori explains the use of its mask as follows: “[o]rganic material or electrode material flying toward the substrate in vapor deposition or the like is deposited on the substrate through the mask opening placed in front of the substrate to achieve the [desired] patterning of the organic electroluminescence element corresponding to the mask opening shape.” Fujimori, [0028]. Accordingly, in my opinion, a POSITA would have appreciated using Fujimori’s magnetic masking approach to deposit Yamazaki’s cover layer would entail situating the mask openings to be *on top of said devices* (as identified above), in order to achieve the patterning (selective deposition) of the cover layer in the location shown in Yamazaki Figures 11 and 14.

144. Finally, using Fujimori’s masking technique to encapsulate a plurality of devices in batch fabrication would entail multiple *mask openings ... placed on top of said devices*, as I have shown in the below annotations.



Yamazaki, Figs. 11 and 14 (replicated and annotated).

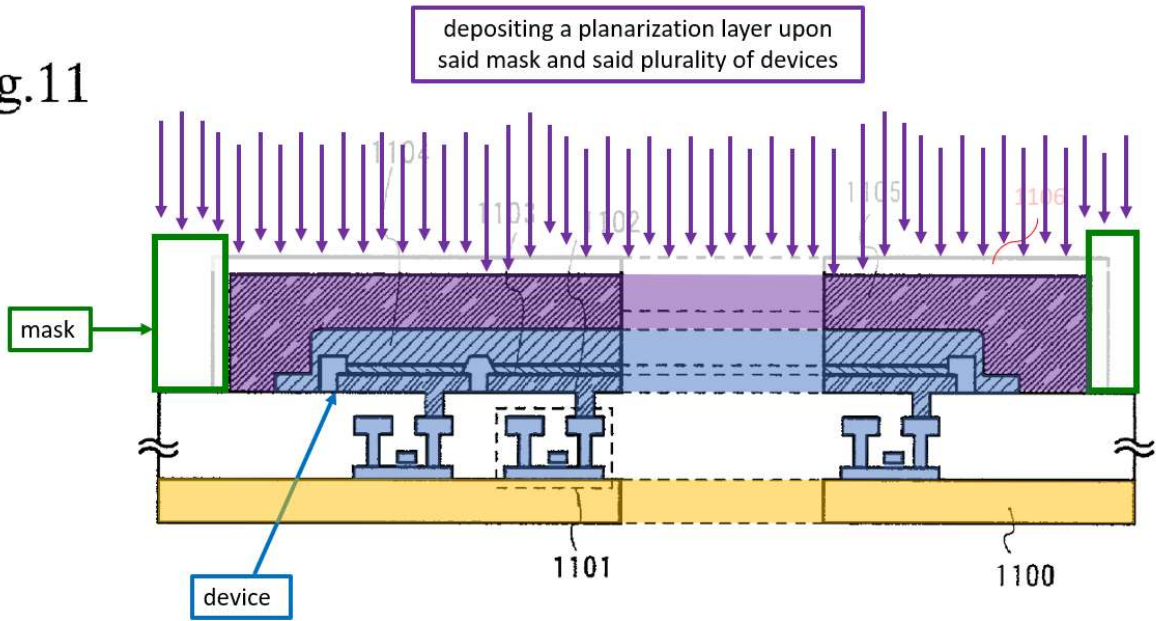
d. Element 41[c]: “depositing at least one planarization layer upon said mask and said plurality of devices;”

145. In my opinion, this element would have been satisfied or at least rendered obvious by Yamazaki’s encapsulation methods as modified to use Fujimori’s magnetically held mask.

146. Specifically, when Fujimori’s magnetically held mask is used with Yamazaki, the formation of the cover layer would entail *depositing at least one planarization layer* (i.e., Yamazaki’s cover layer 1105 or 1407) *upon said mask* (Fujimori’s mask) *and said plurality of devices* (a plurality of OLED display devices as I have

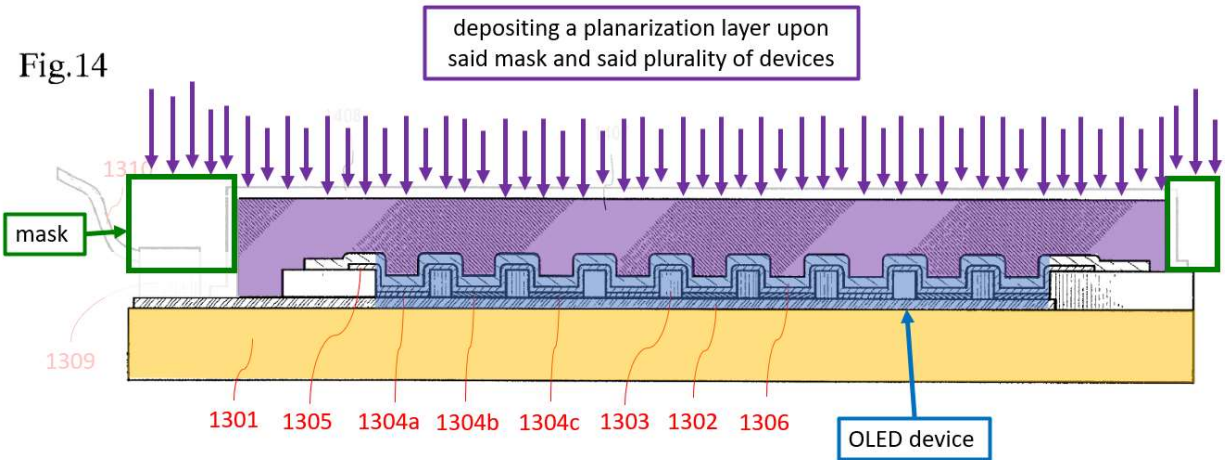
identified for Element 34[a] in Ground I above). I have illustrated this in Figures 11 and 14 below, with my annotations showing the deposition of the cover layers 1105 and 1407, respectively.

Fig.11



Yamazaki, Fig. 11 (annotated).

Fig.14



Yamazaki, Fig. 14 (annotated).

147. **First**, either of Yamazaki's cover layers (1105 or 1407) constitutes a *planarization layer* as I discussed for Element 34[b] in Ground **I** above.

148. **Second**, in my opinion, the formation of this layer using Fujimori's mask would entail *depositing* the planarization layer *upon said mask and said plurality of devices*. Fujimori explains the use of its mask as follows:

Organic material or electrode material **flying toward the substrate in vapor deposition** or the like is **deposited on the substrate through the mask opening** placed in front of the substrate to achieve the [desired] patterning of the organic electroluminescence element corresponding to the mask opening shape."

Fujimori, [0028].

149. As such, in my opinion, a POSITA would have appreciated that using Fujimori's magnetic masking method to deposit Yamazaki's cover layer would entail depositing a layer of "organic material," Yamazaki, [0008], *upon said mask and said plurality of devices*, in order for the material to become deposited through the mask openings, and in order to achieve the patterning (i.e., selective deposition) of the cover layer 1105 or 1407 in the respective locations shown in Figures 11 and 14.

e. Element 41[d]: “removing said mask from said substrate; and”

150. In my opinion, this element would have been satisfied or at least rendered obvious by Yamazaki’s encapsulation methods as modified to use Fujimori’s magnetically held mask.

151. Specifically, when Fujimori’s magnetically held mask is used with Yamazaki (whether Figure 11 or Figure 14), the method would entail *removing said mask from said substrate*, as the mask would need to be removed after forming the cover layer, in order to subsequently deposit the barrier layer. Yamazaki, [0008], [0183], [0203], Figs. 11, 14.

152. Indeed, a POSITA would have understood that deposition masks are removed after deposition is complete, as opposed to being part of the finished device. This understanding is supported by the prior art disclosures of Burrows and Fujimori. For example, Burrows (Ex. 1009) teaches that shadow masks may be used to deposit decoupling (i.e., planarization) layers which “will cover an area less than the area covered by the layer of barrier material,” Burrows, 7:59-8:10, but the masks are not part of Burrow’s completed, encapsulated devices. *See id.*, Figs. 3, 4. Similarly, Fujimori contemplates that its magnetic mask would be adhered only temporarily, as it explains that an “electromagnet,” which “can electrically control the switching of magnetic field”—i.e., turn it off and on—“is particularly suitable in the present invention.” Fujimori, [0033]. Similarly, Fujimori discusses

removing the mask before the next step in the process in its Embodiment 4.

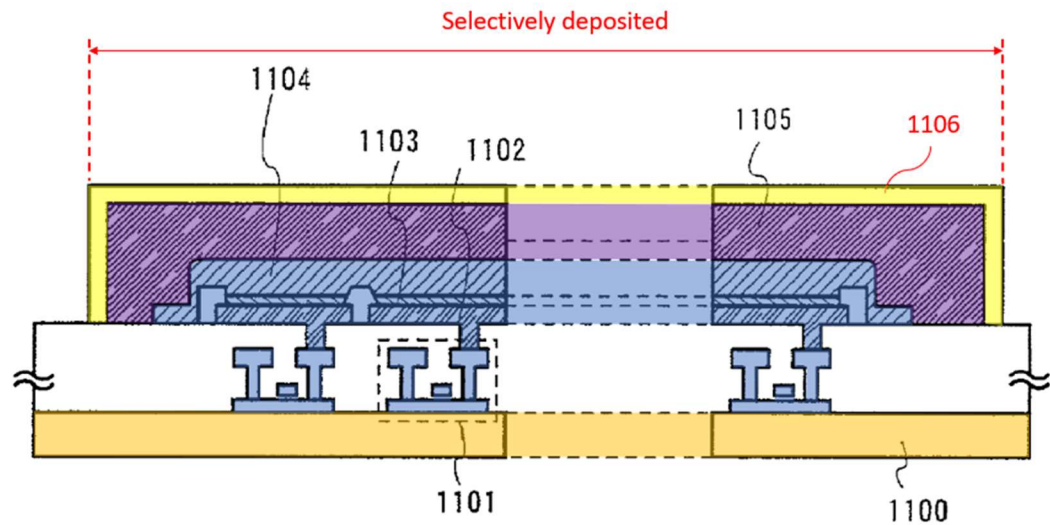
Fujimori, [0050] (“Subsequently, the mask for the light-emitting layers was removed and 20 nm of Alq3 was deposited on the entire surface of the substrate as a light-emitting layer covering layer 43.”).

153. Additionally, Yamazaki’s method entails depositing an additional larger layer over the cover layer 1005 or 1407—namely, the barrier layer 1106 or 1408. Yamazaki, [0183], [0203], Figs. 11, 14. Yamazaki shows the subsequently-deposited barrier layer as having an area that extends beyond the area of the cover layer, thereby covering the cover layer, thereby completely sealing the EL element from moisture, oxygen, and other degrading factors *see id.*, Figs. 11, 14, [0184]. Therefore, a POSITA would have understood that the mask would need to be *remov[ed] ... from said substrate* after cover layer 1105 or 1407 is formed, so that a separate magnetically held mask with corresponding larger openings could then be used to deposit the barrier layer.

f. Element 41[e]: “selectively depositing at least one barrier layer over said planarization layer.”

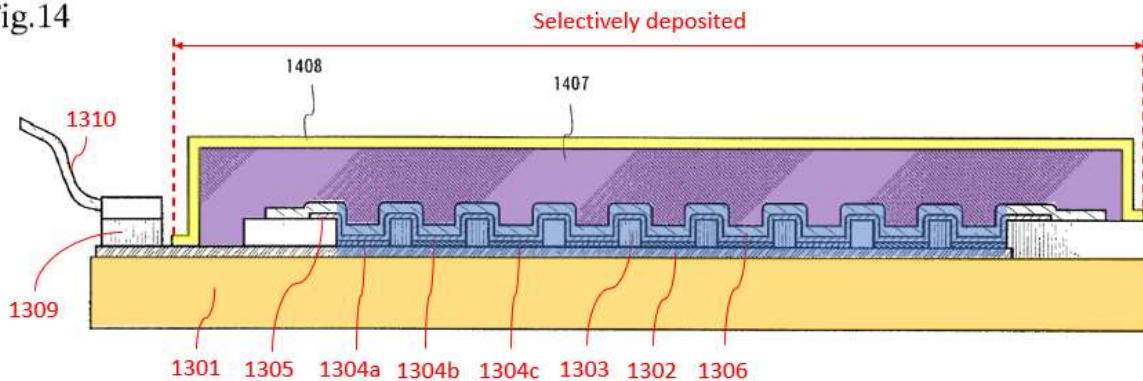
154. In my opinion, Yamazaki satisfies this element for the same reasons I have set forth above for Element 34[c] in Ground I above, which is identical. More specifically, Yamazaki’s encapsulation method entails *selectively depositing at least one barrier layer* (barrier layer 1106 or 1408) *over said planarization layer* (cover layer 1105 or 1407), as illustrated in Figures 11 and 14, respectively:

Fig.11



Yamazaki, Fig. 11 (annotated).

Fig.14



Id., Fig. 14 (annotated).

155. Yamazaki states that “barrier layer 1106 is formed selectively using a *shadow* mask,” Yamazaki, [0183]. Additionally, as noted for Element 41[b] above, Fujimori’s magnetic masking approach may be used for the barrier layer as well as the cover layer, thus further simplifying the manufacturing process. However, claim 41 does not recite any specific requirements as to the method used for selectively depositing the barrier layer.

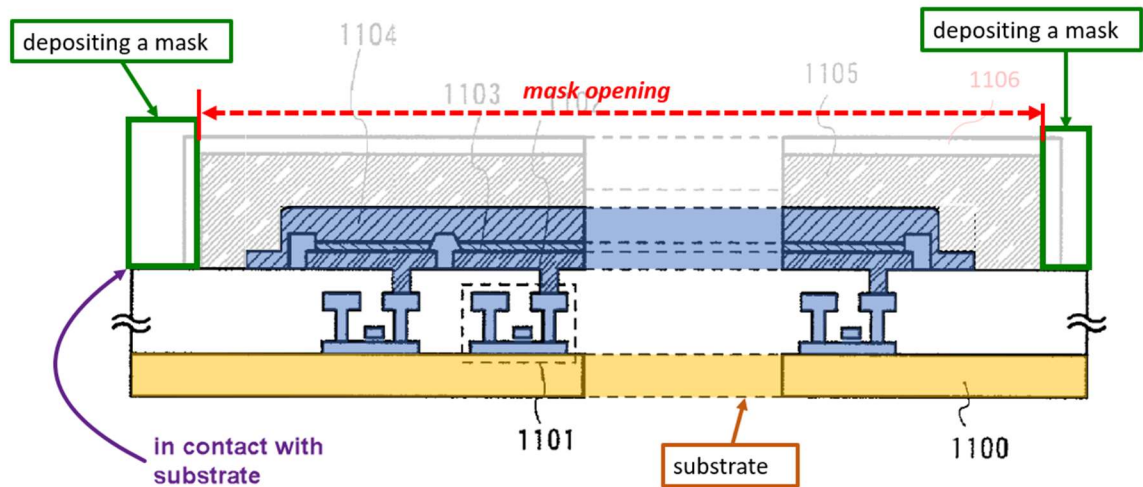
- 2. Dependent Claim 42: “The method as recited in claim 41 wherein the step of depositing said mask further comprises depositing a stamp mask, depositing a laminated film-mask, depositing a vacuum mask, or magnetically held mask.”**

156. In my opinion, Yamazaki’s encapsulation methods as modified to use Fujimori’s mask would satisfy the additional requirements of this claim. Specifically, the combination would entail *depositing a ... magnetically held mask*. As I discussed for Element 41[b] above, Fujimori teaches that its mask is adhered to the underlying substrate by magnetic force. *See* Fujimori, [Abstract], [0009], [0030], [0037].

- 3. Dependent Claim 43: “The method as recited in claim 41 wherein the step of depositing said mask further comprises depositing said mask such that said mask is in contact with said substrate.”**

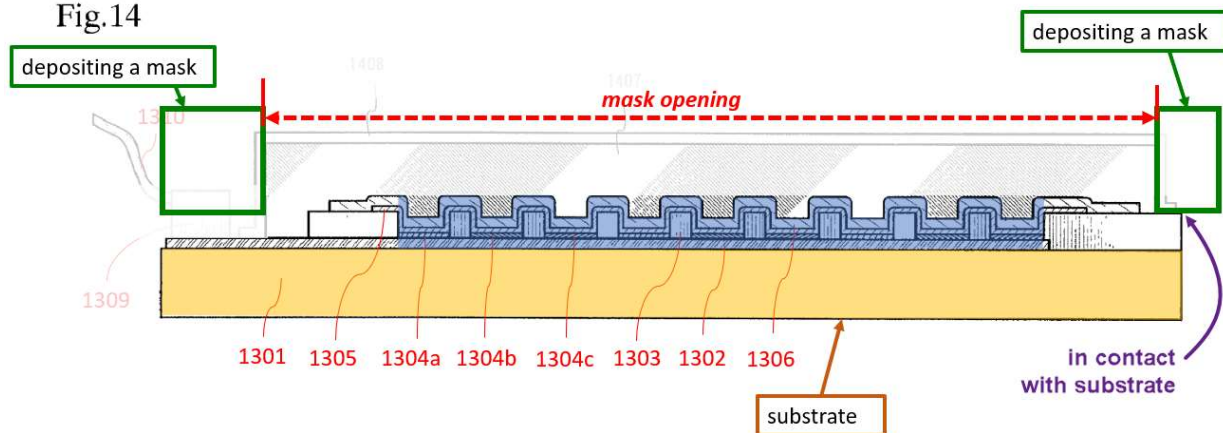
157. In my opinion, Yamazaki’s encapsulation methods as modified to use Fujimori’s magnetic masking approach would satisfy the additional requirements of dependent claim 43. Specifically, the combination entails *depositing said mask* (here, Fujimori’s magnetic mask) *such that said mask is in contact with said substrate*, as I have shown below.

Fig.11



Yamazaki, Fig. 11 (annotated).

Fig.14



Yamazaki, Fig. 14 (annotated).

158. As I have discussed for Element 41[b] above, Fujimori teaches that its mask is adhered to the underlying substrate by magnetic force. *See* Fujimori, [0030], [Abstract]. Fujimori explains that the mask is “*attached to a substrate* with magnetic force,” *id.*, [0010], and that an “object of the present invention” is “to provide a method to achieve adequate *adhesion between the mask and the*

substrate,” id., [0009]. In my opinion, these disclosures indicate that the mask is in contact with the underlying substrate. Indeed, Fujimori specifically discusses that the mask may be in “mechanical contact” with the substrate:

[W]hen the mask is **affixed with mechanical contact**, the magnetic force should be adequate to obtain the mask adhesiveness required, and if the mask is affixed with magnetic force, the magnetic force should be adequate for mask adhesion and positional affixing.

Fujimori, [0030].

159. In addition, Fujimori discloses that a spacer can be placed on the substrate “to prevent the mask from damaging the organic layer and the like deposited on the substrate when the manufacturing surface of the organic electroluminescent element and the mask are adhered to each other,” Fujimori, [0038], and that the “function of the spacer can also be achieved by ... coating the entire surface of the mask with a relatively flexible material such as a resin,” Fujimori, [0039]. These disclosures make clear that the mask is physically adhered to the underlying substrate, and that the resin-coated mask, for example, would be used to prevent damage when the mask is *in contact* with the substrate.

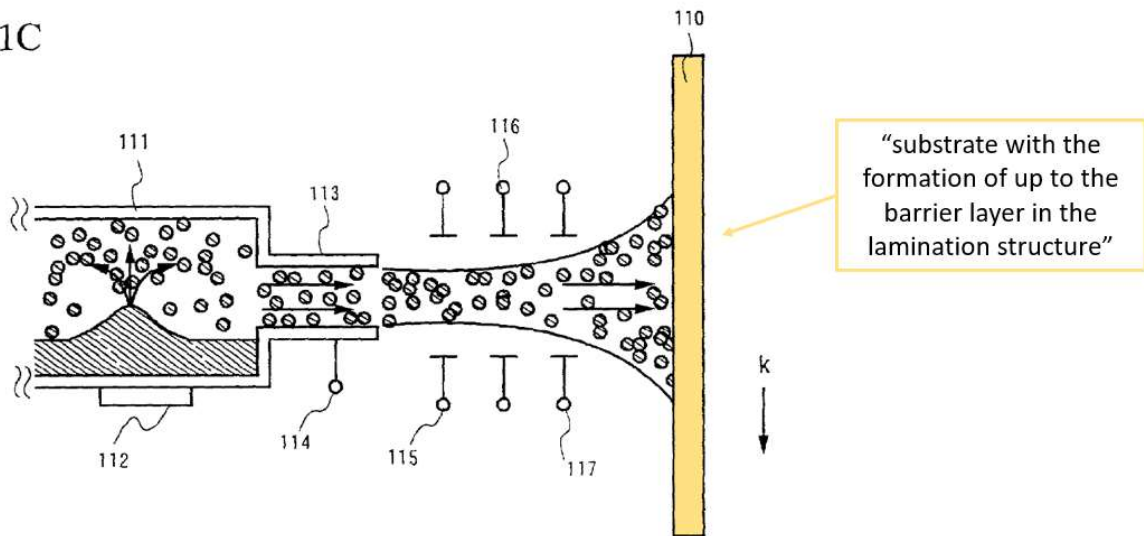
160. Further, I note that the mask is “in contact” with the Yamazaki substrate in a manner that is consistent with the ’389 patent’s disclosure. Specifically, even if

the mask is not in immediate contact with Yamazaki's bottom-most "substrate 1100" or "substrate 1301." The '389 patent distinguishes masks that are merely above (but not in physical contact with) the underlying layers (for example, Fig. 5 element 510), with masks that are deposited so as to be *in contact* with the underlying layers (for example, Fig. 6B element 604), and teaches the benefit of the latter approach:

The mask might be such that it could be brought into contact with the OLED sufficiently well so that the encapsulation organic is confined over the desired areas and does not seep under the areas where the encapsulation organic is not desired (e.g. contact pads).

'389 patent, 7:41-46. In my opinion, Fujimori's mask is "brought into contact with the OLED" in this same manner, as I have shown in the annotation above. Similarly, Yamazaki uses "substrate" to encompass not only the base layer but also a "substrate 110" (Yamazaki, [0041]) that "denotes the substrate with the formation of up to the barrier layer in the lamination structure" (*id.*, [0039]) as shown in Figure 1C, which I have annotated below. In other words, the "substrate" includes the entire "lamination structure" as placed in the deposition chamber.

Fig.1C



161. *Id.*, Fig. 1C (annotated). Thus, when Fujimori’s mask is used in Yamazaki’s method, the mask is *in contact with* Yamazaki’s substrate.

4. **Dependent Claim 44: “The method as recited in claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising a material substantially non-sucking [or non-sticking] to OLED substrate over the areas in between the active areas.”⁵**

162. In my opinion, Yamazaki’s encapsulation method as modified to use Fujimori’s magnetic masking approach would satisfy the additional requirements

⁵ As I have noted above in the claim construction section, I understand that the file history indicates that the claim language “non-sucking” reflects a typographical error. During prosecution, the pending claim instead used the term “non-sticking.” As such, I have analyzed the claim both under the assumption that “*non-sucking* to

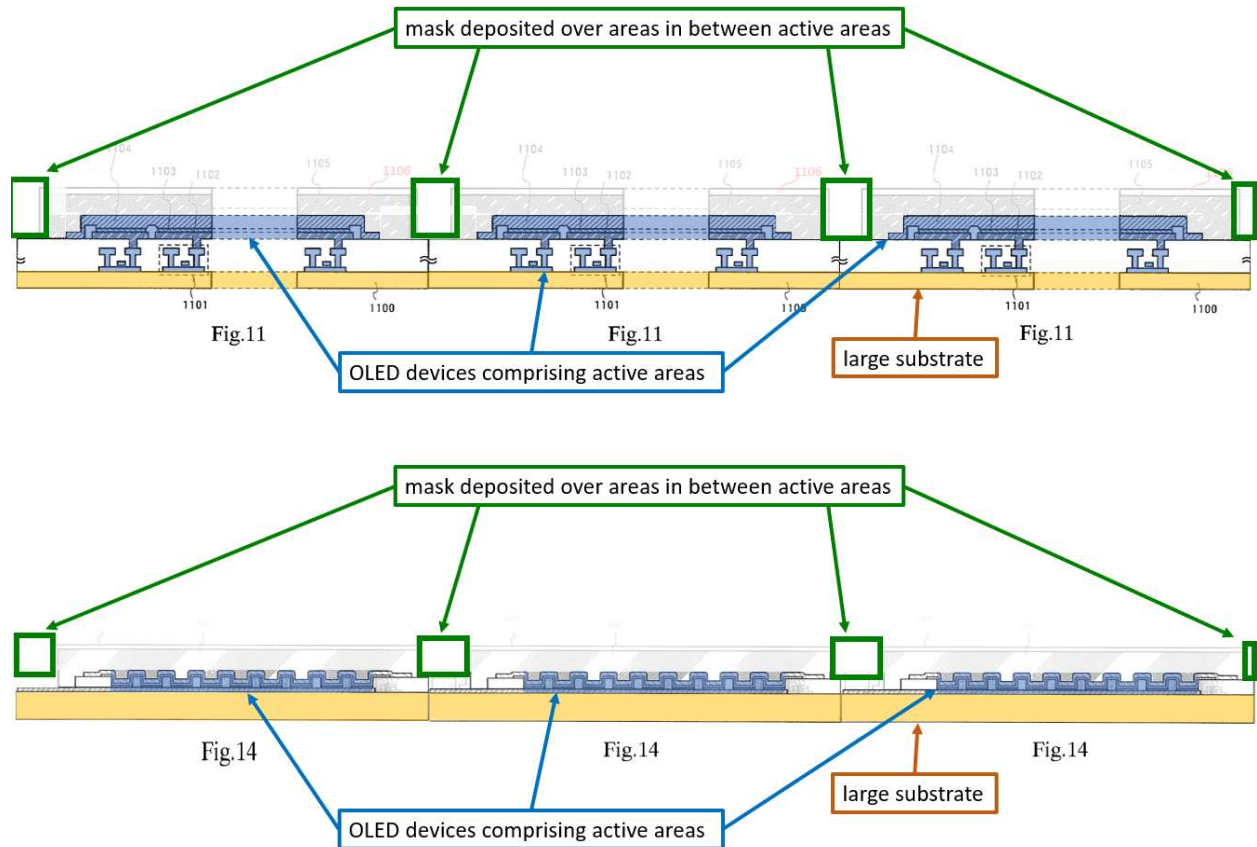
of dependent claim 44. Specifically, Fujimori teaches or suggests that the magnetic mask comprises *a material substantially non-sucking [or non-sticking] to OLED substrate over the areas in between the active areas.*

163. As an initial starting point, given that the mask needs to be removed from the substrate as for the reason I discussed for Element 41[d] above, in my opinion, it would have been obvious to use a mask whose material does not stick to the substrate, in order for it to be capable of being removed without damaging the substrate.

164. In addition, as I noted for Claim 43 above, Fujimori discloses that a spacer can be placed on the substrate “to prevent the mask from damaging the organic layer and the like deposited on the substrate when the manufacturing surface of the organic electroluminescent element and the mask are adhered to each other,” Fujimori, [0038], and that the “function of the spacer can also be achieved by ... coating the entire surface of the mask with a relatively flexible material such as a resin,” Fujimori, [0039]. Fujimori also explains that material of the mask itself may include “rubber or resin.” *Id.*, [0034].

OLED substrate” should be interpreted as “*non-sticking* to OLED substrate,” as well as under the alternative scenario in which the claim is applied as written.

165. In my opinion, a POSITA would have understood that in order for the flexible resin coating to “prevent the mask from damaging” the substrate, the resin should be a material that is *substantially non-sticking* to the substrate.
166. For the same reasons, in my opinion a POSITA would have appreciated that the resin would also be a material that is *substantially non-sucking* to the substrate. For context, as the '389 patent uses “suck” to refer to magnetic adhesion, *see* '389 patent, 7:48-49 (“magnet ... that ‘sucks’ the mask to the substrate”). A POSITA would have understood that a resin is not a material that is fixed by magnetic force, and thus does not “suck” in the manner described in the '389 patent.
167. Lastly, in my opinion, a POSITA would have understood that Yamazaki’s substrate would be an *OLED substrate* (as it is a substrate on which OLED devices are formed), and that the magnetically held mask would be *over the areas in between* the OLED devices comprising the *active areas* (e.g., areas that emit light), as I have shown in the illustration below. Therefore, in my opinion, a POSITA would have understood Fujimori to teach (or at least strongly suggest) that the mask comprises a material substantially non-sucking [non-sticking] *to OLED substrate over the areas in between the active areas*.



Yamazaki, Fig. 11 (replicated and annotated).

5. **Dependent Claim 45: “The method as recited in claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising a metal, a ceramic, a plastic, a polymer, PTFE, or poly-siloxane.”**

168. In my opinion, Yamazaki’s encapsulation method as modified to use Fujimori’s magnetic masking approach would satisfy the additional requirements of dependent claim 45. Specifically, Fujimori teaches that the magnetic mask *compris[es] a metal, a plastic, and/or a polymer.*

169. Fujimori teaches that the mask should include at least one magnetic metal (iron Fe, cobalt Co, or nickel Ni, all of which are metals), and/or rubber or resin:

[M]agnetic materials are ... suitable materials for the mask. It is favorable to fabricate the mask from these materials molded into thin sheets, but it is **also possible to use rubber or resin** mixed with magnetic powder and molded into a film shape, so the material composition of masks cannot be generally specified. In order to efficiently generate magnetic attraction, **the mask desirably contains** a total of at least 1% of at least one of the **magnetic elements Fe, Co, and Ni** (at least 1% if an element is used alone) and more desirably a total of least 20%. The mask itself may or may not be magnetized from the start, although the magnetic field will exert an attractive force on the fabricated mask. If necessary, the mask can be fabricated from magnetized material or magnetized after fabrication.

Fujimori, [0034].

170. In addition, as I have discussed for Claim 43 above, Fujimori discloses “coating the entire surface of the mask with a relatively flexible material such as ***a resin***.” Fujimori, [0039]. A POSITA would have appreciated that Fujimori thus discloses that the mask *compris[es] a metal* (e.g., Fe, Co, or Ni), *a plastic* (e.g., resin), and/or *a polymer* (e.g., rubber or resin).

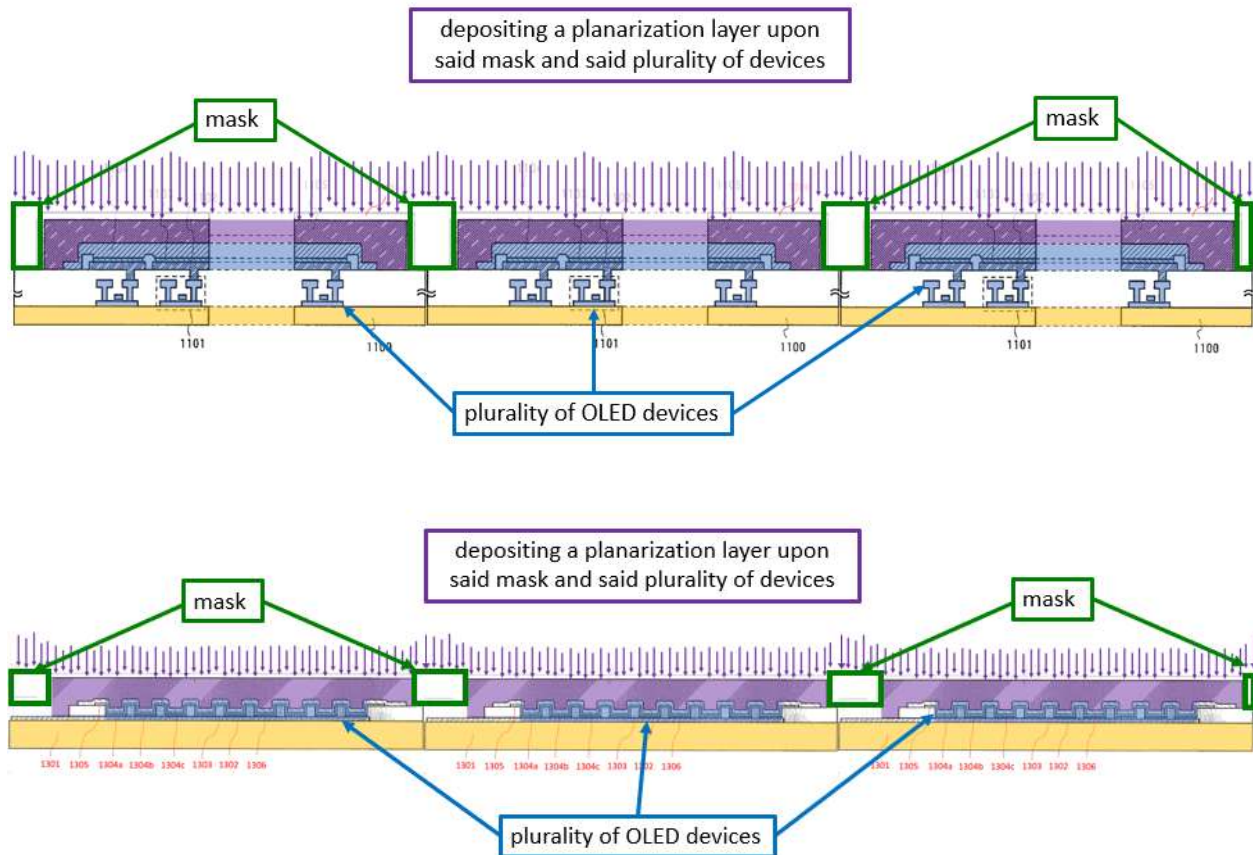
6. Dependent Claim 46: “The method as recited in claim 41 wherein the step of depositing at least one planarization layer further comprises depositing an organic layer over the entire mask.”

171. In my opinion, Yamazaki’s encapsulation method as modified to use Fujimori’s magnetic masking approach would satisfy the additional requirements of dependent claim 46. A POSITA would have understood that depositing the *planarization layer* (specifically, Yamazaki’s cover layer) entails *depositing an organic layer over the entire mask*.

172. *First*, as I have explained for dependent claim 37 in Ground I above, Yamazaki discloses that its cover layers (i.e., planarization layers) are “made of organic material,” specifically an “organic resin film.” Yamazaki, [0011], [0177], [0178], [0202].

173. *Second*, as I have explained for Element 41[c] above, when using Fujimori’s magnetic masking approach with Yamazaki, the organic material for the cover layer is deposited through the mask openings to the underlying OLED devices, as illustrated in the following annotations. *See* Fujimori, [0028] (“Organic material . . . **flying toward the substrate in vapor deposition** or the like is **deposited on the substrate through the mask opening** placed in front of the substrate to achieve the [desired] patterning of the organic electroluminescence element corresponding to the mask opening shape.”). In my opinion, a POSITA would have understood this to entail depositing an organic layer over the entire

mask (and at a minimum this would be obvious to a POSITA), as the layer would need to be deposited over the entire mask in order to ensure that the layer is formed for the OLED devices in each pixel of the display device.



Yamazaki, Figs. 11 and 14 (annotated).

C. Ground III: Claims 34 and 40 are Obvious Over Weaver

1. Independent Claim 34

- a. **Element 34[Preamble]: “A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:”**

174. In my opinion, to the extent the preamble is limiting, Weaver discloses it or at least renders it obvious. Specifically, the embodiment shown in my below

annotation of Figure 6 of Weaver shows a protective structure that serves to encapsulate an OLED device 140 (blue), which is fabricated upon a substrate (orange) (collectively, layer 110 and “barrier region” 120), where the device is encapsulated by “an additional barrier region” 150 comprising alternating “planarizing layers” 151a-c and a “high-density layers” 152a-c:

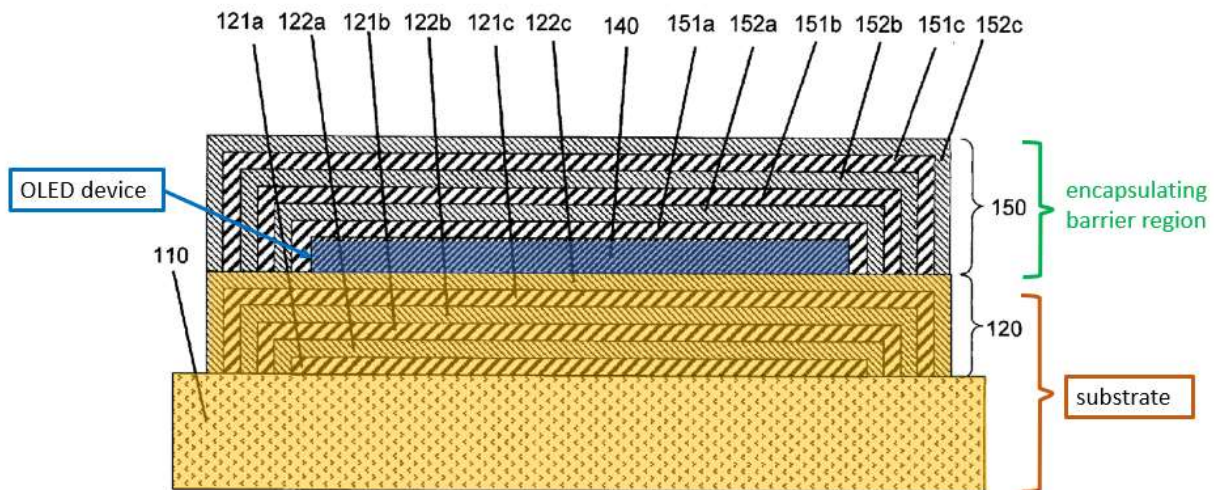


Fig. 6

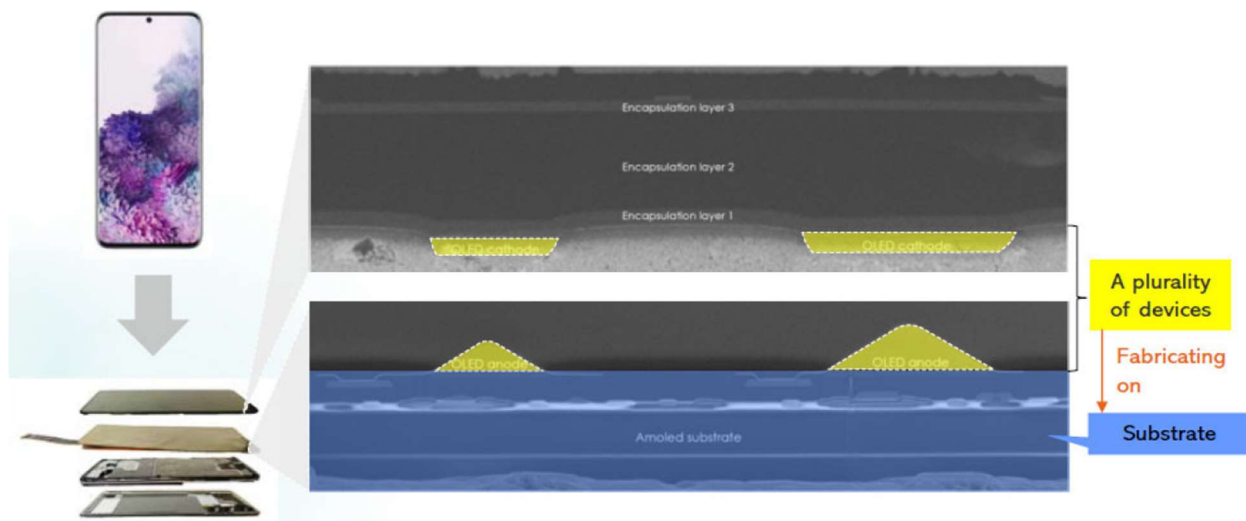
Weaver, Fig. 6 (annotated).

175. Further, the OLED device 140 is *fabricated upon a substrate*. For context, the '389 patent describes a “substrate” as encompassing a structure that “has formed upon its surface several OLED devices,” explaining that “this structure is to be construed very broadly.” '389 patent, 3:45-47. In addition, I understand that the Patent Owner has identified structures encompassing a series of layers as the

claimed substrate.⁶ Accordingly, under the Patent Owner’s understanding, which I have been instructed to adopt for purposes of my analysis, Weaver’s OLED 140 is fabricated upon a substrate comprising “substrate layer 110” and the first “barrier region 120”—which Weaver collectively refers to as a “covered substrate.” Weaver, [0056], [0028).

176. As I have shown above, Weaver’s encapsulation method is based on “[d]eposition of progressively larger cooperative barrier layers,” Weaver, [0057]. Weaver explains that its “[p]referred techniques are continuous techniques such as web-based processing techniques,” *id.*, and discloses specific approaches for

⁶ More specifically, I understand that in connection with its district court complaint (Ex. 1019, ¶ 34), Patent Owner asserts that a Galaxy S20 smartphone includes a “plurality of devices on a substrate,” by pointing to a substrate as shown below:



depositing the alternating planarizing and high-density layers using such continuous processing techniques. *See id.*, [0057]-[0060]; Figs. 8, 9. For example, as shown in Figure 8 (which I have annotated below), Weaver discloses a web-based approach for depositing the planarizing and high-density layers using “[a]n apparatus 200 containing various rolls,” in which “a web of substrate [] is passed under several deposition sources 221a-c and 222a-c.” *Id.*, [0057].

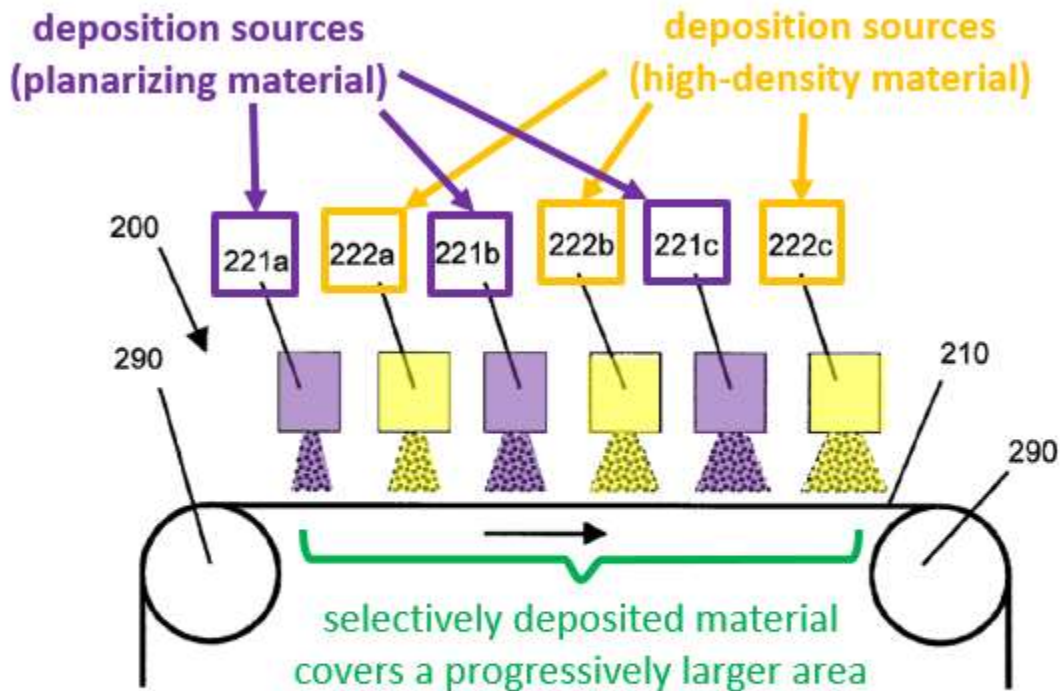


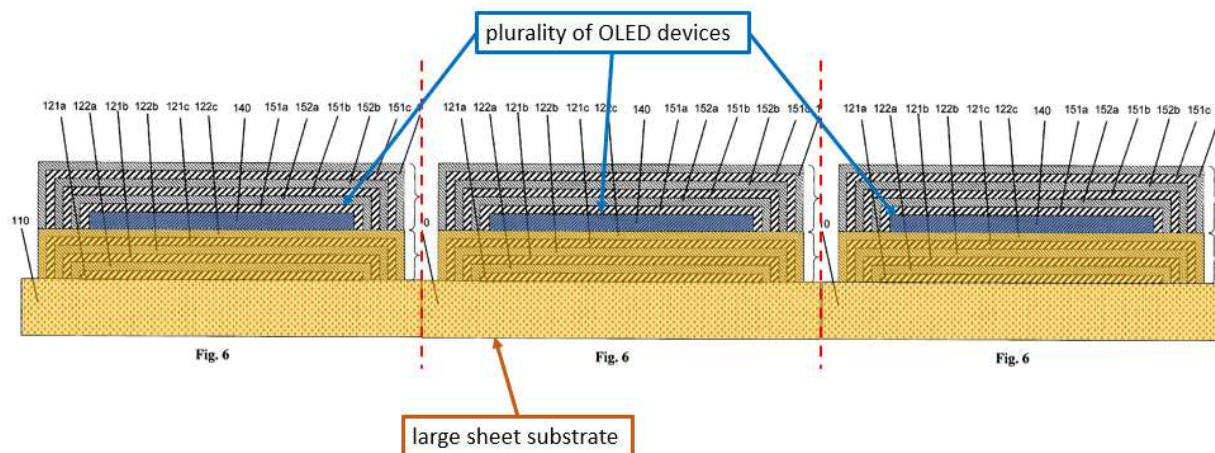
Fig. 8

Id., Fig. 8 (annotated).

177. In my opinion, a POSITA would have appreciated that Weaver’s method entails encapsulating a *plurality* of such OLED devices, particularly given that

Weaver explains that “[c]ontinuous processing techniques ... typically involve the *formation of large sheets of material*,” which “can be subsequently *subdivided into sheet sizes appropriate for the final application* (e.g., into sheets the size of a computer monitor screen).” *Id.*, [0038] (emphasis added). In addition, Weaver discloses a web-based processing technique where “a web of substrate [] is passed under several deposition sources,” and a POSITA would have understood that multiple OLED devices would be fabricated on such a web of substrate. *Id.*, [0057].

178. Accordingly, Weaver teaches or suggests that its method is used to encapsulate multiple devices on a large sheet of material, which are subsequently subdivided into individual devices. For the Figure 6 embodiment, this large sheet can be depicted by laying multiple instances of Figure 6 side-by-side:



Id., Fig. 6 (replicated and annotated).

179. Weaver's teachings regarding continuous processing on a large sheet are consistent with my above discussion regarding the knowledge of a POSITA, that flat panel displays were conventionally manufactured in bulk on a large "motherglass" which would be cut into smaller display sizes at the end of the manufacturing process. As I have explained for Ground I above, producing multiple display panels from a motherglass was well known to reduce costs, increase throughput, and increase yield compared to producing each display panel individually. Further, the '389 patent admits that this was known in the prior art. *See* '389 patent, 1:63-65, Fig. 2 (showing and describing "PRIOR ART" batch fabrication).

180. Indeed, Weaver explains that its structures are intended to address a problem with such sheet-based manufacturing, in that "cutting a large sheet produces a structure with exposed edges like that shown in FIG. 1a," which I have reproduced below. Weaver, [0038].

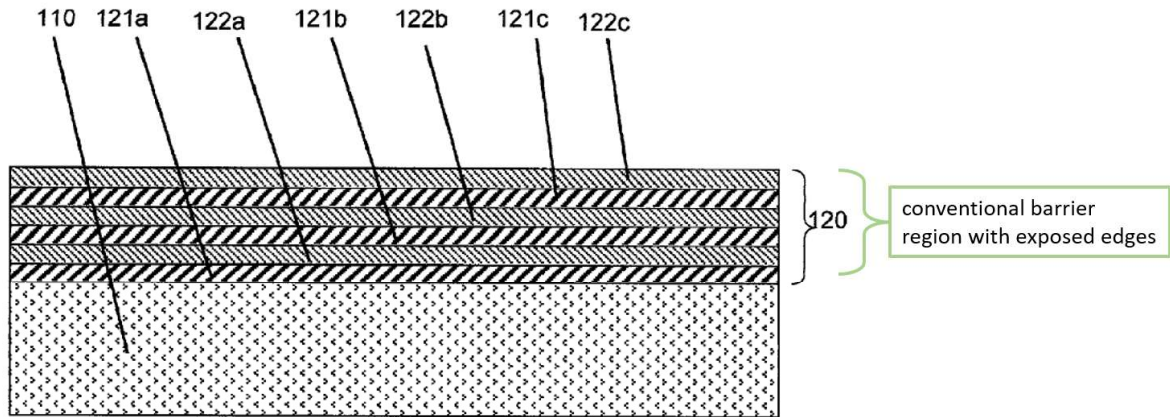


Fig. 1a

181. *Id.*, Fig. 1a (annotated). “Unfortunately, in exposing the edges of layers 121a-c and 122a-c in the barrier region 120, lateral diffusion of moisture and oxygen, as well as other species, becomes increasingly problematic.” *Id.* Weaver states that “[t]his situation is improved by the structures of the present invention.” *Id.*, [0041]. For example, in Figure 6, which I have annotated below, the OLED 140 is completely encapsulated by a barrier region 150 with no exposed edges (as shown below), leading to increased protection. *See id.* (“As a result, lateral diffusion of water and oxygen within the planarizing layers 121a-c is reduced ...”). This discussion underscores that Weaver’s method is used to encapsulate a plurality of devices on a large sheet of material.

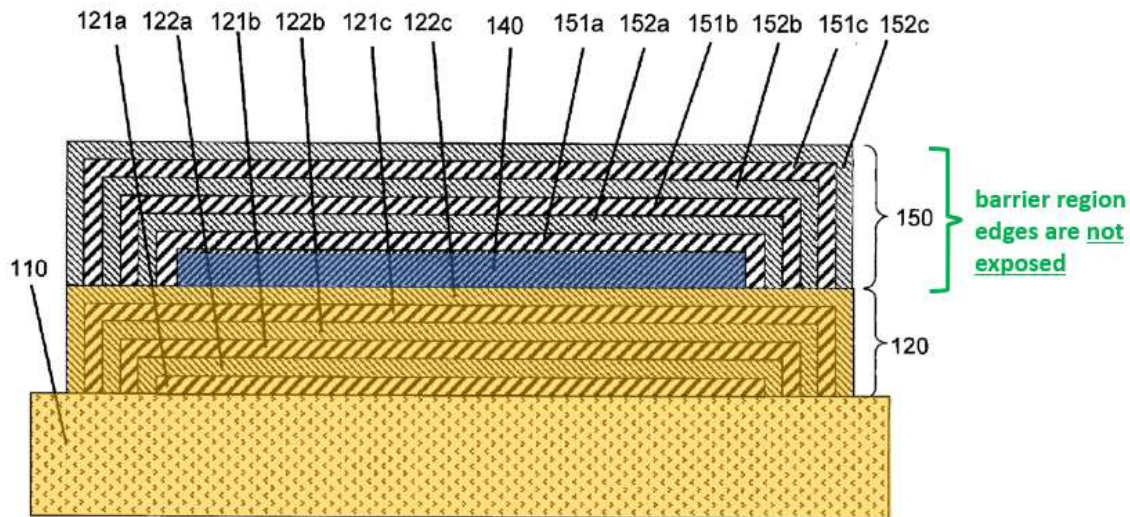


Fig. 6

Id., Fig. 6 (annotated).

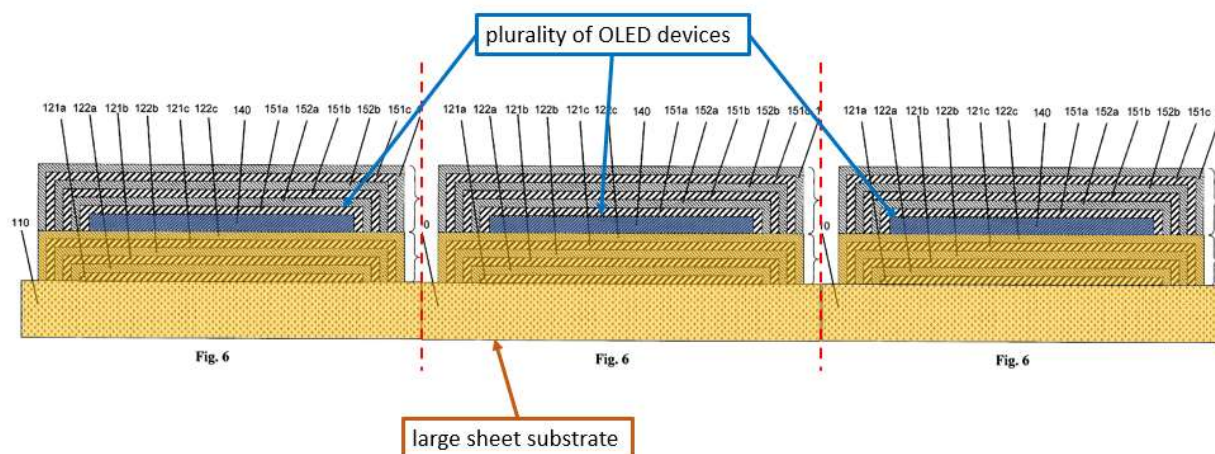
182. Weaver’s teachings regarding continuous or web-based processing on a large sheet are consistent with the knowledge of a POSITA that flat panel displays were conventionally manufactured in bulk, as I explained for Ground I above.

183. Accordingly, in my opinion, a POSITA would have been motivated to use Weaver’s continuous processing method for the Figure 6 embodiment to encapsulate a *plurality of devices*, in order to obtain the known benefits described above—i.e., reducing costs, increasing throughput, and increasing yield. *See, e.g.,* Boroson, [0002] (“In manufacturing, electronic devices are typically produced by fabricating large substrates containing multiple electronic devices The primary reason for fabricating multiple electronic devices on large

individual substrates or a continuous roll substrate is to reduce manufacturing cost by decreasing handling, increasing throughput, and increasing yield.”).

b. Element 34[a]: “fabricating a plurality of devices on a substrate;”

184. In my opinion, Weaver discloses or at least renders obvious this element. As I have discussed for Element 34[pre] above, Weaver teaches or suggests a method of encapsulating a plurality of OLED devices as part of a continuous processing technique. This entails *fabricating a device* (specifically, OLED 140) *on a substrate* (substrate 110 along with initial barrier region 120), as I have illustrated below.



Weaver, Fig. 6 (replicated and annotated).

185. As I explained above for Element 34[Preamble], under Pictiva’s understanding of the term “substrate,” which I have been instructed to adopt for purposes of my analysis, the entire set of layers underlying Weaver’s OLED

device 140—the substrate 110 along with the initial barrier region 120—collectively constitute a “substrate” on which the device is fabricated.

c. Element 34[b]: “selectively depositing at least one planarization layer upon said devices; and”

186. In my opinion, Weaver discloses this element or at least renders it obvious, as Weaver’s “planarizing layer” 151a is a *planarization layer* that is *selectively deposited upon said devices* (device 140) as I have shown in the following annotation.

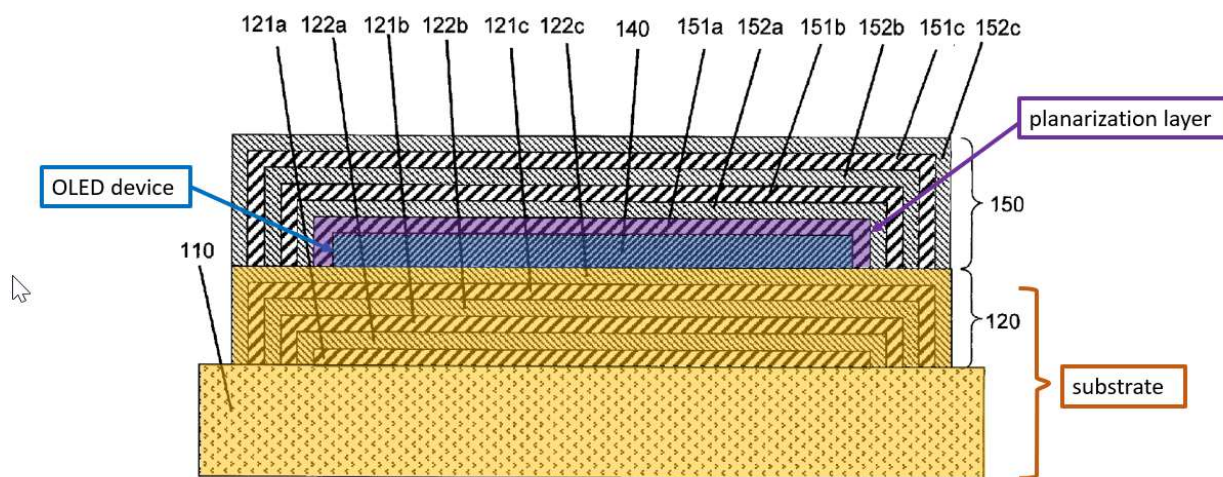


Fig. 6

Weaver, Fig. 6 (annotated); [0052].

187. Weaver teaches that this planarizing layer 151a constitutes a *planarization layer* as disclosed in the '389 patent. As Weaver explains:

By “planarizing material” is meant a material that **forms a smooth planar surface** upon application, rather than forming a surface that reflects irregular contours of the underlying surface.

Id., [0035] (emphasis added).

188. Weaver further teaches that planarizing layer 151a is *selectively deposited* upon the OLED 140. The selective deposition is evident from Figure 6, which shows the planarization layer as surrounding the OLED device from the top and sides, but not extending laterally over the entire surface of the substrate. *See also id.*, [0042] (describing, with respect to Figure 2, that successive planarizing and high-density layers each “completely cover[] an underlying ... layer (i.e., by covering the top of the underlying layer *and extending down the sides of the underlying layer to the substrate*)”, [0054] (similar discussion for Figure 4)).

189. Furthermore, Weaver specifically teaches the use of selective deposition to form such a planarizing layer, explaining that its web-based manufacturing approach utilizes “deposition sources” with “apertures.” Specifically, Weaver discloses a method for forming encapsulation based on the “[d]eposition of *progressively larger* cooperative barrier layers,” such as can be seen in layers 151a-c and 152a-c in Figure 6. *Id.*, [0057] (emphasis added). Weaver further teaches that in one embodiment, “a web of substrate 210 is passed under several deposition sources 221a-c and 222a-c within a web-coating apparatus,” wherein “[p]referred sources are thermal evaporation, sputtering, PECVD and electron beam sources for the high-density layers, and thermal evaporation, organic vapor phase deposition (OVPD), chemical vapor deposition (CVD), spraying and flash

evaporation sources for the planarization layers.” *Id.* As shown in Figure 8, which I have annotated below, Weaver teaches that “*each deposition source is provided with aperture* that is larger than that of the adjacent upstream source (i.e., the source to the left), such that the material being deposited from each source progressively covers a wider area as the substrate proceeds downstream (i.e., from left to right).” *Id.*, [0059].

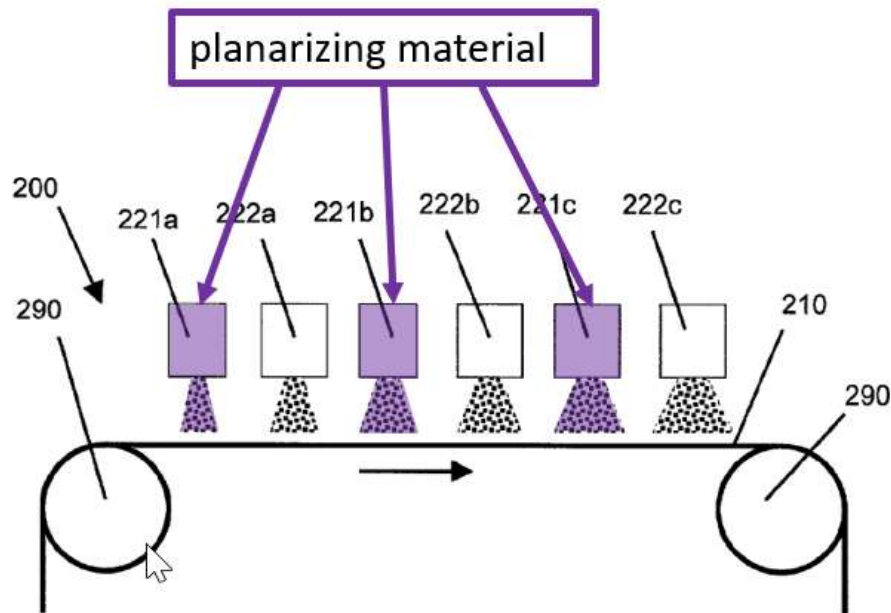


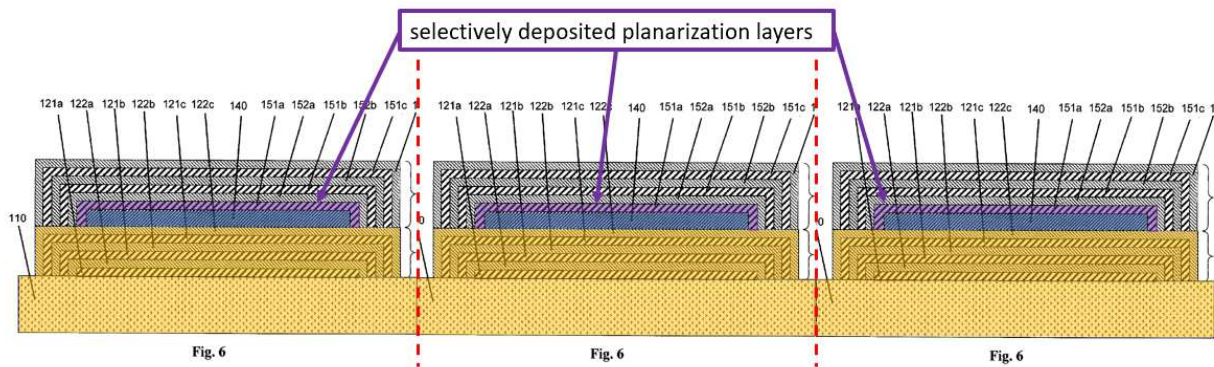
Fig. 8

Id., Fig. 8.

190. As I have annotated above, deposition sources 221a-c are taught as being used to deposit planarizing material layers and sources 222a-c are used to deposit high-

density layers, respectively. *Id.*, [0058].⁷ This achieves the *selective deposition* of planarization layer 151a in Figure 6 above.

191. Weaver’s continuous processing technique entails “selectively depositing at least one planarization layer (e.g., planarizing layer 151a) upon each of said plurality devices, as I have shown in the following annotation.



Weaver, Fig. 6 (replicated and annotated).

d. Element 34[c]: “selectively depositing at least one barrier layer over said planarization layer.”

192. In my opinion, Weaver discloses this element or at least renders it obvious.

As shown in Figure 6, which I have annotated below, Weaver’s encapsulation

⁷ Although paragraph [0058] of Weaver describes depositing planarizing layers 121a-c and high-density layers 122a-c, a POSITA would have appreciated that this description is equally applicable to the planarizing layers 151a-c and high-density layers 152a-c of the “additional barrier region 150,” which likewise constitute “progressively larger barrier layers.” Weaver, [0052], [0057].

method includes depositing “high-density layer” 152a (yellow)—a barrier layer—over the planarization layer 151a.

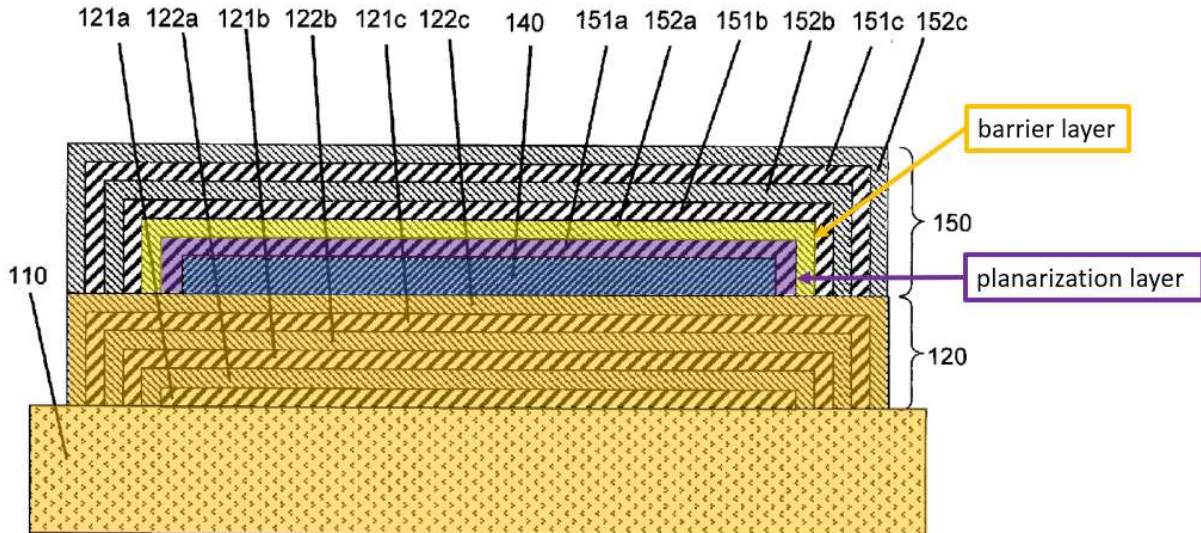


Fig. 6

Weaver, Fig. 6 (annotated).

193. In the context of the '389 patent, a “barrier layer” is a layer that “provides the necessary environmental isolation from the corrosive effects of oxygen and moisture.” '389 patent, 1:39-41. Weaver’s high-density layer 152a constitutes a “barrier layer” because, as Weaver explains, such a high-density layer is made by depositing “‘high-density material’ ... with sufficiently close atomic spacing such that diffusion of outside species, particularly water and oxygen, are

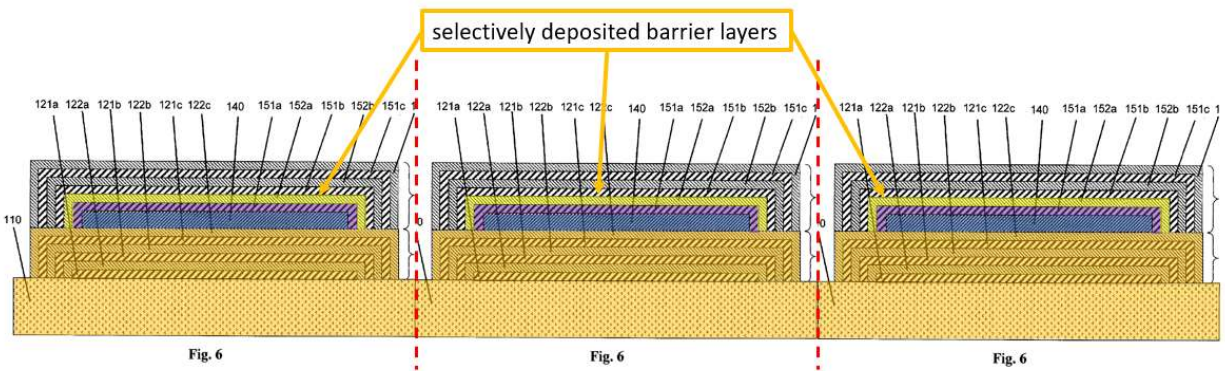
hindered.” *Id.*, [0036].⁸ This high-density layer 152a therefore “provides ... isolation from the corrosive effects of oxygen and moisture,” and is therefore a barrier layer as claimed in the ’389 patent.

194. Weaver further teaches that the high-density layer 152a is selectively deposited over the planarizing layer 151a (“planarization layer”). Again, this selective deposition is evident from Figure 6, which shows the high-density layer as surrounding the planarization layer from the top and sides, but not extending laterally over the entire surface of the substrate. Moreover, as I discussed with Element 34[b], Weaver specifically teaches the use of selective deposition to form the high-density layer, as part of its method for “[d]eposition of progressively larger cooperative barrier layers.” *Id.*, [0057]. This is illustrated in Figure 8, where deposition sources 222a-c are used to deposit high-density layers (such as high-density layer 152a of Figure 6), and where “each deposition source is provided with an aperture that is larger than that of the adjacent upstream source (in other words, the source to the left in Figure 8), such that the material

⁸ Although paragraph [0036] of Weaver references high-density layers 122a-c of Figure 2, a POSITA would have appreciated that this description is equally applicable to the high-density layers 152a-c of the “additional barrier region 150,” which likewise constitute “progressively larger barrier layers.” *Id.*, [0052], [0057].

being deposited from each source progressively covers a wider area as the substrate proceeds downstream (i.e., from left to right [in Figure 8]).” *Id.*, [0059].

195. Finally, Weaver’s continuous processing technique entails *selectively depositing at least one barrier layer* over each of the planarization layers, as I have shown in the following annotation:



Weaver, Fig. 6 (replicated and annotated).

2. **Dependent Claim 40:** “The method as recited in claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by shadow mask, sputtering, ink jet deposition, screen printing [or] evaporation.”

196. In my opinion, Weaver further satisfies the added requirements of dependent claim 40. As Weaver explains, its high-density layer 152a (i.e., the claimed “barrier layer”) is a layer that “can be applied using techniques known in the art such as *thermal evaporation*, *sputtering*, plasma-enhanced chemical vapor deposition (PECVD) methods and electron-beam techniques.” Weaver, [0036].

197. Additionally, as I have discussed for Elements 34[b] and 34[c] above, it would have been obvious at the time of the alleged invention to use Burrows's shadow masks, in connection with Weaver's continuous processing technique shown in Figure 8, in order to selectively deposit Weaver's "progressively larger cooperative barrier layers" of barrier region 150 (including barrier layer 152a). Weaver, [0057].

D. Ground IV: Claims 35 and 36 are Obvious Over Weaver in View of Palanisamy

1. Dependent Claim 35: "The method as recited in claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by ink jet of an organic layer."

198. In my opinion, dependent claim 35 is obvious based on Weaver in view of Palanisamy. Specifically, Weaver teaches that its *planarization layer* (planarizing layer 151a) is formed by *depositing ... an organic layer*, and it would have been obvious at the time of the alleged invention based on Palanisamy to use *ink jet* to deposit this layer when applying Weaver's methods as I have discussed for Claim 34 in Ground III above.

199. First, Weaver discloses that its planarization layers are made of organic materials. In particular, Weaver teaches that "[p]referred planarizing materials are polymers, such as fluorinated polymers, *parylenes*, cyclotenes and polyacrylates." Weaver, [0035]. A POSITA at the time of the alleged invention

would have appreciated that many polymers, including parylenes, are organic materials.

200. Second, Weaver discloses that its planarizing layers can be “provided using techniques known in the art, for example, by dipping, spin coating, sputtering, evaporative coating, spraying, flash evaporation, chemical vapor deposition and so forth.” Weaver, [0035]; *see also id.*, [0057] (explaining that “[d]eposition of progressively larger cooperative barrier layers *can be achieved in a number of ways*” (emphasis added)). In my opinion, a POSITA would have recognized that *depositing by ink-jet* could achieve Weaver’s planarizing layers. At the time of the alleged invention, ink-jet printing was a well-known selective deposition method, *see* Cok, 10:20-28 (“Patterned deposition can be achieved using ... inkjet method.”), and was one of a finite number of identified, predictable solutions that a POSITA would have had reason to pursue for depositing Weaver’s planarizing layer. Notably, the ’389 patent acknowledges that “[i]t will be appreciated” that “many manners” can be used for depositing its organic planarization layer, including “ink-jet printing.” ’389 patent, 4:48-55; *see also id.*, 7:1-5 (“In fact, generally any printing techniques suitable to deliver the desired planarization layer material can be used.”). The ’389 patent presumes that a POSITA would know how to employ ink jet technology to deposit the

planarization layer, as the patent does not provide any detail on how to use the ink jet technique. *Id.*, 4:53-55, 7:2-3, 7:14-17.

201. To that end, Palanisamy specifically teaches the use of “an ink jet printer,” Palanisamy, [0021], which may be used for “selectively applying an organic passivation material to the recently deposited organic light emitting material.” *Id.*, [Abstract]. Referring to Figure 3, which I have annotated below, Palanisamy describes this technique as follows:

One selective, passivation deposition technique, shown in FIG. 3, involves an inkjet printer 44 to selectively apply passivation to areas 42 while leaving areas 40 over the display panel 20 uncovered. The inkjet printer 44 is capable of applying the passivation material through a nozzle 46 at a very high rate. In this way, passivation may be selectively applied.

Id., [0021].

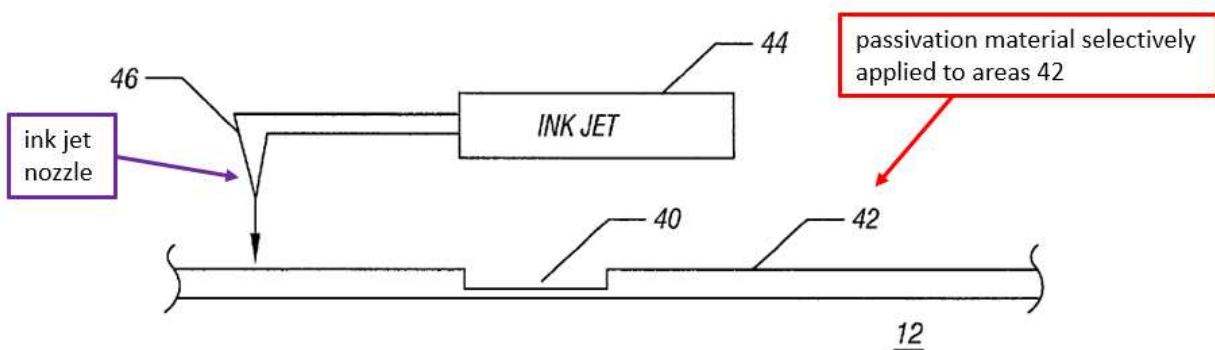


FIG. 3

Id., Fig. 3 (annotated).

202. Ink jet printing was known to provide specific advantages. For example, ink jet printing is a non-contact deposition technique, and thus minimizes risk of contamination. Ink jet printing is also a directed deposition technique, which is very material efficient and limits the amount of waste generated compared to other deposition techniques. Similarly, the technique is conducive to depositing multiple coats, allowing for the deposition of thicker layers. Finally, the technique is scalable, since large numbers of inkjet heads can be ganged together to rapidly print over large areas.
203. Accordingly, in my opinion, a POSITA would have been motivated to use *depositing by ink jet* as taught in Palanisamy to selectively deposit the *organic layer* that serves as the *planarization layer* in Weaver (Weaver’s “planarizing layer 151a”). Although other selective deposition techniques have their own benefits, a POSITA would have recognized the benefits of using the ink jet as taught by Palanisamy—including reduction of contamination risk, efficient use of deposition material, and scalability. At a minimum, a POSITA would have understood from Palanisamy that depositing by ink jet was one of a finite number of predictable solutions for “selectively applying an organic passivation material” for OLEDs, whose materials “are relatively sensitive to moisture, oxygen, and common solvents.” Palanisamy, [0001], [0003].

204. In addition, in my opinion, a POSITA also would have had a reasonable expectation of success in using ink jet printing as taught by Palanisamy to selectively deposit Weaver's organic planarizing layer. Indeed, Palanisamy identifies ink jet printing as a method by which an organic passivation layer "may be selectively applied to the areas coated by the OLED while excluding areas where passivation would be undesirable, such as the areas proximate to the contacts." *Id.*, [0021]. A POSITA would have appreciated that ink jet nozzles as shown in Figure 3 of Palanisamy could be used as the "deposition sources 221a-c" in Figure 8 of Weaver, in connection with a continuous processing technique, in order to selectively deposit Weaver's planarizing layers (including layer 151a). Weaver, [0059].

2. Dependent Claim 36: "The method as recited in claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by screen printing of an organic layer or depositing by gas nozzle."

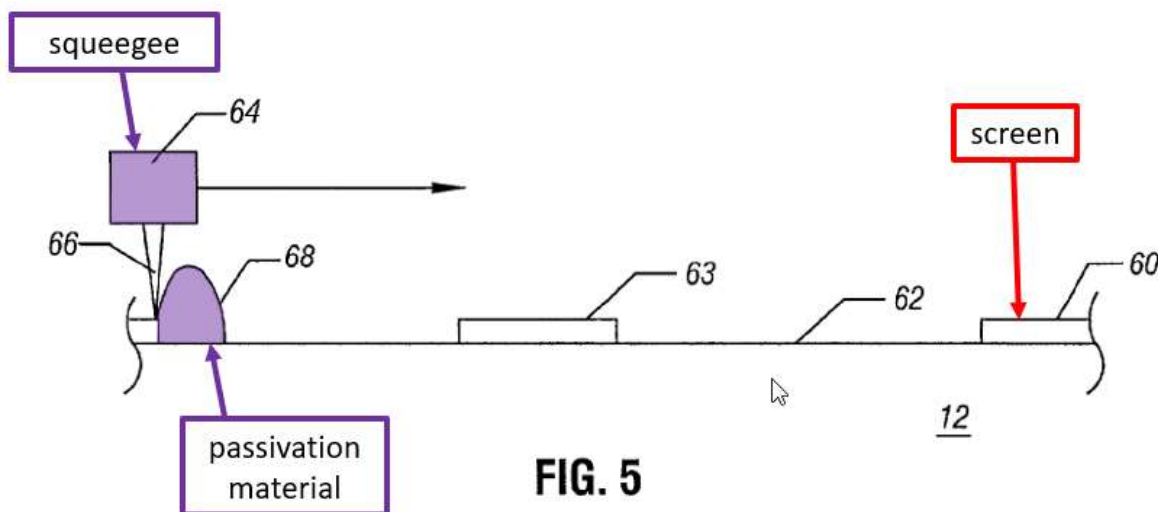
205. In my opinion, dependent claim 36 is obvious based on Weaver in view of Palanisamy. Specifically, Weaver teaches that its *planarization layer* (planarizing layer 151a) is formed by *depositing ... an organic layer*, and it would have been obvious at the time of the alleged invention based on Palanisamy to use *screen printing* to deposit this layer when applying Weaver's methods as I have discussed for Claim 34 in Ground III above.

206. First, Weaver discloses that its planarization layers are made of organic materials. Specifically, Weaver teaches that “[p]referred planarizing materials are polymers, such as fluorinated polymers, *parylenes*, cyclotenes and polyacrylates.” Weaver, [0035]. A POSITA would have appreciated that many polymers, including parylenes, are organic materials.

207. Second, Weaver discloses that its planarizing layers can be “provided using techniques known in the art, for example, by dipping, spin coating, sputtering, evaporative coating, spraying, flash evaporation, chemical vapor deposition and so forth.” Weaver, [0035]; *see also id.*, [0057] (explaining that “[d]eposition of progressively larger cooperative barrier layers *can be achieved in a number of ways*” (emphasis added)). In my opinion, a POSITA would have recognized that *depositing by screen printing* could achieve Weaver’s planarizing layers. At the time of the alleged invention, screen printing was a well-known selective deposition method, as evidenced for example by Birnstock (Ex. 1018), 3905 (discussing benefits of using screen printing to deposit layers, including an organic barrier layer, in passive matrix displays), and was one of a finite number of identified, predictable solutions that a POSITA would have had reason to pursue for depositing Yamazaki’s cover layer. In fact, the ’389 patent acknowledges that “[i]t will be appreciated” that “many manners” can be used for depositing its organic planarization layer, including “screen printing.” ’389

patent, 4:48-55; *see also id.*, 7:1-5. The '389 patent presumes that a POSITA would know how to employ screen printing to deposit the planarization layer, as the patent does not provide any detail on how to use the screen printing technique. *Id.*, 4:53-55, 7:1-3, 7:14-17.

208. To that end, Palanisamy teaches the use of “a screen printing technique,” Palanisamy, [0024], which may be used for “selectively applying an organic passivation material to ... recently deposited organic light emitting material,” Palanisamy, [Abstract], and which is illustrated in Figure 5 (which I have annotated below):



Id., Fig. 5 (annotated).

209. Palanisamy further teaches that its screen printing technique entails multiple benefits:

With screen printing processes, a range of passivation material viscosities may be utilized. Also, a screen printing process, with rapid ultraviolet curing at room temperature, makes for a very fast, low temperature, inline manufacturing process in one embodiment. The rapid processing time also limits the exposure of the organic light emitting material to air where moisture absorption can occur. The screen printing process is amenable to both liquid and paste passivation materials.

Id., [0025].

210. Accordingly, in my opinion, a POSITA would have been motivated to use *depositing by screen printing* as taught in Palanisamy to selectively deposit the *organic layer* that serves as the *planarization layer* in Weaver (Weaver’s “planarizing layer 151a”). Although other selective deposition techniques have their own benefits, a POSITA would have recognized the benefits of using the screen printing technique as taught by Palanisamy—including “rapid processing time” at lower temperatures, and enabling “a range of []material viscosities” to be used for Weaver’s planarizing layer 151a. Palanisamy, [0025]. At a minimum, a POSITA would have understood from Palanisamy that depositing by screen printing was one of a finite number of predictable solutions for “selectively applying an organic passivation material” for OLEDs, whose materials “are

relatively sensitive to moisture, oxygen, and common solvents.” *Id.*, [Abstract], [0003].

211. In addition, in my opinion, a POSITA also would have had a reasonable expectation of success in using screen printing as taught by Palanisamy to selectively deposit Weaver’s organic planarizing layer. Indeed, Palanisamy identifies screen printing as a method by which an organic passivation layer “may be selectively applied to the areas coated by the OLED while excluding areas where passivation would be undesirable, such as the areas proximate to the contacts.” *Id.*, [0021]. A POSITA would have appreciated that squeegees and screens as shown in Figure 5 of Palanisamy could be used in as the “deposition sources 221a-c” in Figure 8 of Weaver, in connection with a continuous processing technique, in order to selectively deposit Weaver’s planarizing layers (including layer 151a). Weaver, [0059].

E. Ground V: Claim 37 is Obvious Over Weaver in View of Burrows

1. Dependent Claim 37: “The method as recited in claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing an organic layer through a shadow mask.”

212. In my opinion, dependent claim 37 would have been obvious in view of Weaver and Burrows. Specifically, Weaver teaches that its *planarization layer* (i.e., planarizing layer 151a) is formed by *depositing ... an organic layer*, and in

my opinion, it would have been obvious to a POSITA based on Burrows to selectively deposit this layer *through a shadow mask*.

213. *First*, as I have explained for Element 34[b] in Ground III above, Weaver discloses that its planarizing layers (including planarizing layer 151a, which is the claimed *planarization layer*) are formed by *depositing an organic layer*. More specifically, Weaver teaches that “[p]referred planarizing materials are polymers, such as fluorinated polymers, parylenes, cyclotenes and polyacrylates.” Weaver, [0035]. A POSITA would have appreciated that many polymers, including parylenes, are organic materials.

214. *Second*, Weaver discloses an approach for selectively depositing its cooperative barrier layers (i.e., the planarizing and high-density layers), using a series of selective deposition sources, such that “each deposition source is provided with an aperture that is larger than that of the adjacent upstream source.” Weaver, [0059]; *see also* Ground III, Element 34[b] above. While Weaver does not describe these deposition sources in detail, in my opinion, its discussion of deposition “apertures” is at least suggestive of the shadow masking approach. *See* Burrows-631 (Ex. 1022), 1:22-26 (“A ‘shadow’ mask is a mask having apertures through which material is deposited onto a substrate, as opposed to an optical mask, which is used to selectively expose photoresist on a substrate to radiation.”). Weaver further states that its planarizing layers can be “provided

using techniques known in the art, for example, by dipping, spin coating, sputtering, evaporative coating, spraying, flash evaporation, chemical vapor deposition and so forth.” Weaver, [0035]. Weaver also explains that the “[d]eposition of progressively larger cooperative barrier layers can be achieved in a number of ways.” *Id.*, [0057].

215. *Third*, at the time of the alleged invention, *depositing ... through a shadow mask*, as taught for example in Burrows, was among the “techniques known in the art” for depositing such planarizing layers. The ’389 patent itself demonstrates this by acknowledging that “[i]t will be appreciated” that “many manners” can be used for depositing its organic planarization layer, including “deposit[ing] through a shadow mask.” ’389 patent, 4:48-55, 7:1-5; *see also* Burrows-631 (Ex. 1022), 1:20-22 (“The use of a shadow mask to deposit [] patterned thin films on the substrate is well known in the art.”).

216. For example, Burrows specifically teaches use of shadow masks for selectively depositing an organic planarization layer, in connection with encapsulation techniques that are very similar to those of Weaver. Burrows is directed to methods for making an “edge-sealed barrier film” for encapsulating “environmentally sensitive devices,” such as “organic light emitting devices”. Burrows, Abstract, 5:21-41, 2:27-34. As shown in Figure 4, which I have annotated below, Burrows discloses an approach in which the devices are

encapsulated with a series of planarizing “decoupling layers 410” (purple) and “barrier layers 415” (yellow). *Id.*, 5:58-65; *see also id.*, 7:13-16 (explaining that the decoupling layer is planarizing in that it “provid[es] a surface with significantly improved planarity”).

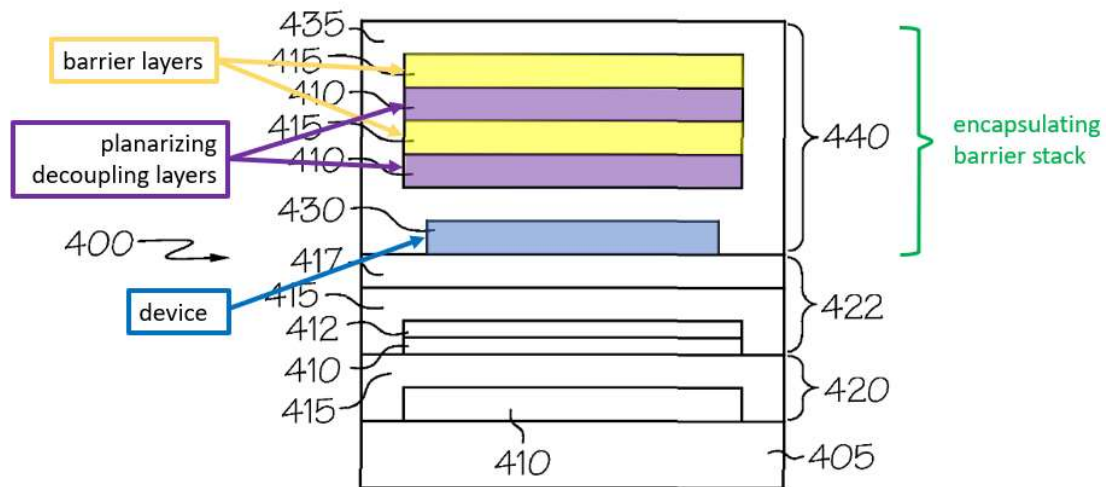
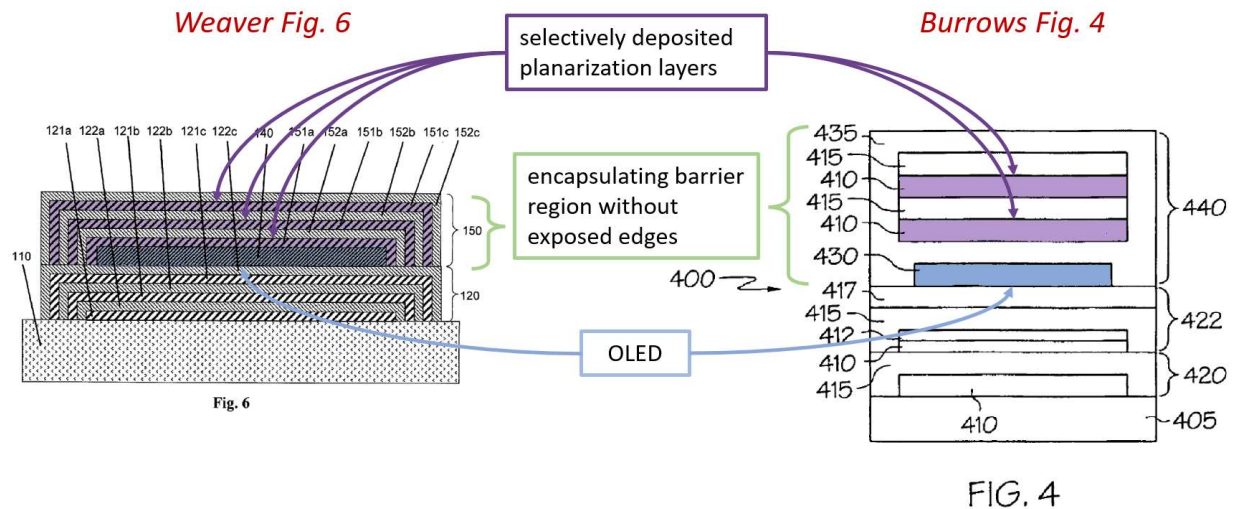


FIG. 4

Id., Fig. 4 (annotated). As seen above, an outer “third barrier layer” 435 seals the barrier stack 440 by surrounding it on the top and sides. *Id.*, 6:11-14. Accordingly, Burrows, like Weaver, discloses an approach for encapsulating an OLED device using a series of alternating planarization and barrier layers.

217. Furthermore, Burrows also teaches selectively depositing its planarizing decoupling layer, using a “mask ... [that] limits the deposition of the decoupling layer to an area which is smaller than, and contained within, the area covered by the barrier layer.” *Id.*, 7:62-65. As in Weaver, this selective deposition ensures

that the sides of the device are fully sealed by the barrier layer—and therefore avoids the problem of exposed edges, as I have illustrated in the following. comparison of embodiments in Weaver and Burrows.



Weaver, Fig. 6 (annotated); Burrows, Fig. 4 (annotated); *cf.* Burrows, 4:33-36 (“Because the [planarizing] decoupling layers 210 are sealed within the area covered by the barrier layers 215, ambient moisture, oxygen, and other contaminants cannot diffuse through the decoupling layers to the environmentally sensitive device.”); *with* Weaver, [0041] (“[E]ach planarizing layer 121a-c is separated from the outside environment by at least one high-density [barrier] layer 122a-c. As a result, lateral diffusion of water and oxygen within the planarizing layers 121a-c is reduced ...”).

218. Further, Burrows specifically teaches the use of “*shadow masks*” for depositing its planarizing decoupling layers, and discloses using this approach to

encapsulate a plurality of devices formed on a large substrate, as part of a batch or roll process. As Burrows explains:

In order to encapsulate **multiple small environmentally sensitive devices** contained on a single large motherglass, the decoupling material may be deposited through multiple openings in a single **shadow mask**, or through multiple **shadow masks**. This allows the motherglass to be subsequently diced into individual environmentally sensitive devices, each of which is edge sealed.

For example, the mask may be in the form of a rectangle with the center removed (like a picture frame). **The decoupling material is then deposited through the opening in the mask.** The layer of decoupling material formed in this way will cover an area less than the area covered by the layer of barrier material. **This type of mask can be used in either a batch process or a roll coating process** operated in a step and repeat mode.

Burrows, 7:59-8:10. Lastly, Burrows discloses that its “decoupling layer may be made ... [of] organic polymers.” *Id.*, 6:10-27; *see also id.*, 6:27-34 (listing examples of organic polymers).

219. Accordingly, in my opinion, it would have been obvious at the time of the alleged invention to use shadow masks (as taught in Burrows) to selectively deposit Weaver's cooperative barrier layers, including planarizing layer 151a (the claimed *planarization layer*). Shadow masks would have been a straightforward way to implement the "apertures" in Weaver's deposition sources.

220. In particular, Weaver teaches that its continuous processing technique may be achieved by the apparatus of Figure 8, which includes a series of deposition sources, each having an "aperture" that is progressively "larger than that of the adjacent upstream source." Weaver, [0059]. As I discussed above, a POSITA would have appreciated that a series of shadow masks (as taught by Burrows) may be used, such that the respective mask openings correspond to the "apertures" mentioned in Weaver. For example, Burrows teaches the use of shadow masks in a similar "roll coating process" that utilizes "one or more decoupling material deposition stations," *id.*, 8:33-34 and "one or more barrier deposition stations ... building up the number of layers desired," *id.*, 8:43-45. A POSITA would have understood that such masks could be used "step and repeat mode," as taught by Burrows, as part of Weaver's continuous processing technique for encapsulating a plurality of OLED devices as shown in Figure 8. A POSITA would have further appreciated that using shadow masks having

progressively larger “openings” or “apertures” would result in “the material being deposited from each source progressively cover[ing] a wide area as the substrate proceeds downstream” as taught in Weaver. *See* Weaver, [0059].

221. Doing so would have constituted the application of known techniques (specifically, encapsulating an OLED device using Burrow’s shadow masks, equipped with openings, in step-and-repeat mode) to a known device ready for improvement (e.g., Weaver’s Figure 8 apparatus for web-based processing of OLED devices, which already contemplates that each deposition source be “provided with an aperture that is larger than the of the upstream source”) in order to yield predictable results (selective “[d]eposition of progressively larger cooperative barrier layers”—which Weaver acknowledges “can be achieved in a number of ways”—and in turn, protection against lateral diffusion by moisture, oxygen, or other contaminants).

222. In my opinion, a POSITA would further be motivated to use this approach, as using a shadow mask allows a good control of the positions on the substrate where the planarizing layers are formed. Additionally, a shadow mask can be used in conjunction with other processes for depositing a layer of liquid material, such as flash evaporation.

223. The use of shadow masks in the Weaver-Burrows combination therefore entails depositing an organic planarization layer (e.g., layer 151a) through a shadow mask.

VIII. CONCLUSION

224. For the aforementioned reasons, in my opinion, claims 34-37 and 40-46 of the '389 patent would have been obvious to a POSITA.

225. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: August 12, 2024

Vivek Subramanian

Vivek Subramanian, Ph.D.

APPENDIX A

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Education

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**Ph.D. in Electrical Engineering, Stanford University
Stanford, California**

Honors earned: Graduate Fellowship, Eastman Kodak Company

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**MS in Electrical Engineering, Stanford University
Stanford, California**

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**BS in Electrical Engineering, Louisiana State University
Baton Rouge, Louisiana**

Honors earned: Summa cum laude, College Honors, Outstanding Senior, Junior and Sophomore, Honors College

Professional Experience

2018 - present

École polytechnique fédérale de Lausanne, Switzerland

2021 – present: Director, Micromanufacturing Science and Engineering Center (M2C)

2021 – present: Associate Director, Institute of Electrical and Micro Engineering (IEM)

2021 – present: Scientific Board, Swiss National Strategic Focus Area – Advanced Manufacturing (SFA-AM)

8/18 – present: Professor

2000 - present

**Department of Electrical Engineering & Computer Sciences, University of California
Berkeley, CA**

7/20 to date : Adjunct Professor

7/11 – 6/20: Professor

7/05 – 7/11: Associate Professor

7/00-7/05: Assistant Professor

Honors Earned:

2015 IEEE Kiyo Tomiyasu Award

Best in session and best in track awards, 2013 IMAPS Microelectronics Conference

Outstanding paper award, 2012 IMAPS Microelectronics Conference

2008 Printed Electronics Champion, Printed Electronics USA Conference

Outstanding Teaching Award, EECS Department, UC Berkeley, 2005

Best paper award, 2004 IEEE Device Research Conference

Nominated to MIT's Technology Review top 100 young innovators list (TR100), 2002

National Science Foundation Young Investigator (CAREER) Award, FY2002,

Nominated to National Academy of Engineering's Frontiers of Engineering, 2002

2002 Paul Rappaport Award for best paper in an IEEE EDS Journal

2009 - 2018

**Professor, World Class University Program, Sunchon National University
Sunchon, Korea**

Principal Investigator leading large research program focused on developing a new department in the area of printed electronics including 9 faculty covering multiple disciplines and 3 different countries

2000 - present

Independent Consultant

Consultant to the semiconductor industry and its associated fields in the following areas:

Memory technology and design

Silicon Process Technology

Display / Imager and Flexible Electronics Technology

RFID Technology

Intellectual Property Consulting

Technology Evaluation / Venture Capital due diligence

2014 – 2022	Founder and CTO, Locix Inc. San Bruno, CA Senior leadership role in venture-funded startup company working on wireless networking
2004 – 2013	Founding Scientific Advisor, Kovio, Inc. Sunnyvale, CA Scientific advising to printed electronics startup company
2008 – 2011	Chief Technical Advisor, QuSwami, Inc. San Francisco, CA Scientific advising to energy conversion device startup company
1998-2000	Consulting Assistant Professor, Electrical Engineering Department, Stanford University. Stanford, CA Advisory role for research group of Prof. Krishna C. Saraswat
1998-2000	Visiting Research Engineer, Electrical Engineering Department, University of California. Berkeley, CA Research into 25nm MOSFET technologies for giga-scale integration
1998 - 2000	Founder, Matrix Semiconductor, Inc. Santa Clara, CA Co-founder and technical advisor of startup company working on high-density memory technology Honors Earned: Nominated to Scientific American's SA50 List for Visionary Technology Finalist for 2003 World Technology Award for Information Technology Hardware Winner, 2005 EDN Innovation Award
1998	Co-instructor, Electrical Engineering Department, Stanford University. Stanford, CA Co-teaching of EE311, Advanced Integrated Circuit Fabrication Processes
1997	Intern, Advanced Product Research and Development Laboratory, Motorola Inc. Austin, TX Research into process development issues affecting SiGe SEMFET devices
1996	Head Teaching Assistant EE410: IC Fabrication Laboratory, Stanford University Stanford, CA Coordination and instruction of EE410, graduate level laboratory course.
1994-1998	Research Assistant, Electrical Engineering, Stanford University Stanford, CA Research into crystallization of amorphous Si and SiGe films using low thermal budget processes. Professional Affiliations and Activities Program Committee, IEEE Electronic Components and Technology Conference, 2014 to 2016 Chair, Scientific Board, iPACK, Royal Institute of Technology (KTH), Sweden, 2011 to 2016 Tampere Institute of Technology Faculty Search Committee, Finland, 2013 University of Oulu Faculty Search Committee, Finland, 2013 Served as external thesis committee member for several universities world-wide, including University of Cape Town (South Africa), Tampere Institute of Technology (Finland), Technical University of Eindhoven (Netherlands), Indian Institute of Science (India), Indian Institute of Technology (India), 2009 to date Associate Editor, IEEE Journal of Display Technology, 2008 to date Technical Program Chair, Large Area, Organic, and Printed Electronics Conference, 2012-2013 Scientific Committee, Large Area, Organic, and Printed Electronics Conference, 2009-2011 Scientific Committee, International Conference on Printed and Flexible Electronics, 2009-2013 IEEE Electron Devices Society Organic Electronics Committee, 2003 - 2005 Executive Committee, International Electron Device Meeting, 2003 to 2009 Technical Program Committee, International Electron Device Meeting, 2001-2002 Technical Program Committee member, Device Research Conference, 2000-2002 Technical Program Committee member, VLSI-TSA Conference, 2005 Member, Institute of Electrical and Electronic Engineers

List of Patents, Publications and Presentations

Patents

1. “Systems and methods for providing wireless asymmetric network architectures of wireless devices with power management features”, V Subramanian, E Alon, V Pavate, US Patent 11,924,757
2. “Systems and methods for precise radio frequency localization in the presence of multiple communication paths”, M Seth, L Kong, T Ylamurto, V Subramanian, US Patent 11,683,779
3. “Systems and methods for using radio frequency signals and sensors to monitor environments”, T. Bakhishev, V. Subramanian, V. Pavate, T. Ylamurto, US Patent 11,327,147
4. “Systems and methods for using radio frequency signals and sensors to monitor environments”, T. Bakhishev, V. Subramanian, V. Pavate, T. Ylamurto, US Patent 11,276,308
5. “Systems and methods for coarse and fine time of flight estimates for precise radio frequency localization in the presence of multiple communication paths”, M. Seth, L. Kong, T. Ylamurto, V. Subramanian, US Patent 11,228,999
6. “Systems and methods for using radio frequency signals and sensors to monitor environments”, T. Bakhishev, V. Subramanian, V. Pavate, T. Ylamurto, US Patent 11,030,902
7. “Systems and methods for precise radio frequency localization in the presence of multiple communication paths”, M. Seth, L. Kong, T. Ylamurto, V. Subramanian, US Patent 10,757,675
8. “Systems and methods for using ranging to determine locations of wireless sensor nodes based on radio frequency communications between the nodes and various RF-enabled devices”, T. Ylamurto, M. Seth, L. Kong, V. Subramanian, US Patent 10,551,479
9. “Systems and methods for providing communications within wireless sensor networks based on a periodic beacon signal”, T. Ylamurto, V. Pavate, E. Alon, V. Subramanian, US Patent 10,536,901
10. “Systems and methods for using radio frequency signals and sensors to monitor environments”, T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,514,704.
11. “Systems and methods for using radio frequency signals and sensors to monitor environments”, T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,504,364
12. “Systems and methods for coarse and fine time of flight estimates for precise radio frequency localization in the presence of multiple communication paths”, M. Seth, L. Kong, T. Ylamurto, V. Subramanian, US Patent 10,470,156
13. “Methods and apparatus for monitoring wound healing using impedance spectroscopy”, M. Maharbiz, V. Subramanian, A. C. Arias, S. Swisher, A. Liao, M. Lin, F. Pavinatto, Y. Khan, D. Cohen, E. Leeftang, S. Roy, M. Harrison, D. Young, US Patent 10,463,293
14. “Systems and methods for using radio frequency signals and sensors to monitor environments”, T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,156,852.
15. “Systems and methods for determining locations of wireless sensor nodes in a tree network architecture having mesh-based features”, L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 10,104,508.
16. “Systems and methods for providing wireless asymmetric network architectures of wireless devices with power management features”, V. Subramanian, E. Alon, V. Pavate, US Patent 10,028,220.
17. “Random delay generation for thin-film transistor based circuits”, V Subramanian, M Mao, Z Wang, US Patent 9,985,664
18. “Systems and methods for determining locations of wireless sensor nodes in a network architecture having mesh-based features for localization”, L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 9,846,220
19. “Systems and methods for determining locations of wireless sensor nodes in a tree network architecture having mesh-based features”, L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 9,763,054
20. “Through silicon vias and thermocompression bonding using inkjet-printed nanoparticles”, V. Subramanian and J. Sadie, US Patent 9,717,145
21. “Systems and methods for providing wireless asymmetric network architectures of wireless devices with anti-collision features”, V. Subramanian, E. Alon, V. Pavate, US Patent 9,706,489

22. "Systems and methods for determining locations of wireless sensor nodes in an asymmetric network architecture", V. Subramanian, E. Alon, V. Pavate, US Patent 9,529,076
23. "Systems and methods for providing wireless sensor networks with an asymmetric network architecture", V. Subramanian, E. Alon, V. Pavate, US Patent 9,380,531
24. "Transparent metal oxide nanoparticle compositions, methods of manufacture thereof and articles comprising the same", V. Subramanian, S. K. Volkman, US Patent 9,343,202
25. "Three-dimensional nonvolatile memory and method of fabrication", M. G. Johnson, T. H. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 9,214,243
26. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 9,171,857
27. "Print compatible designs and layout schemes for printed electronics", Z. Wang, V. Subramanian, L. Cleveland, US Patent 9,155,202
28. "Wireless devices including printed integrated circuitry and methods for manufacturing and using the same", P. Smith, C. Choi, V. Pavate, J. M. Cleeves, V. Subramanian, R. Young, V. Biviano, US Patent 9,004,366.
29. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, M. G. Johnson, P. M. Farmwald, I. Kouznetsov, US Patent, 8,981,457.
30. "High reliability surveillance and/or identification tag/devices and methods of making and using the same", V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, J. M. Cleeves, US Patent, 8,933,806.
31. "Surveillance devices with multiple capacitors", P. Smith, C. Choi, J. M. Cleeves, V. Subramanian, A. Kamath, S. Moles, US Patent, 8,912,890.
32. "Pillar-shaped nonvolatile memory and method of fabrication", M. G. Johnson, T. H. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 8,897,056
33. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 8,853,765
34. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 8,823,076
35. "Random delay generation for thin-film transistor based circuits", V. Subramanian, M. Mao, Z. Wang, US Patent 8,810,298
36. "Vertically stacked field programmable nonvolatile memory and method of fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 8,503,215
37. "Process-variation tolerant series-connected NMOS and PMOS diodes, and standard cells, tags, and sensors containing the same", V. Subramanian, P. Smith, US Patent 8,471,308
38. "Printed compatible designs and layout schemes for printed electronics", Z. Wang, V. Subramanian, L. Cleveland, US Patent 8,383,952
39. "Method for making surveillance devices with multiple capacitors", P. Smith, C. Choi, J. M. Cleeves, V. Subramanian, A. Kamath, S. Moles, US Patent 8,296,943
40. "High reliability surveillance and/or identification tag/devices and methods of making and using the same", V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, and J. M. Cleeves, US Patent 8,264,359
41. "High reliability surveillance and/or identification tag/devices and methods of making and using the same", V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, and J. M. Cleeves, US Patent 8,227,320
42. "Vertically stacked field programmable nonvolatile memory and method of fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 8,208,282
43. "Reliable tag deactivation", J. M. Cleeves, V. Subramanian, US Patent 8,138,921
44. "Combined static and dynamic frequency divider chains using thin film transistors", V. Subramanian, US Patent 8,085,068
45. "Process-variation tolerant diode, standard cells including the same, tags and sensors containing the same, and methods for manufacturing the same", V. Subramanian, P. Smith, US Patent 7,932,537

46. "Three terminal nonvolatile memory Device with vertical gated diode", T. H. Lee, V. Subramanian, J. M. Cleeves, M. G. Johnson, P. M. Farmwald, I. G. Kouznetsov, US Patent 7825455
47. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7816189
48. "Multi-mode tags and methods of making and using the same", P. Smith, J. M. Cleeves, V. Pavate, V. Subramanian, US Patent 7750792
49. "Method of manufacturing complementary diodes", V. Subramanian, P. Smith, US Patent 7528017
50. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7319053
51. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7265000
52. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7160761
53. "Vertically stacked field programmable nonvolatile memory and method of fabrication", V. Subramanian, J. M. Cleeves, US Patent 7157314
54. "Dense arrays and charge storage devices", T. H. Lee, V. Subramanian, J. M. Cleeves, A. J. Walker, C. Petti, I. Kouznetzov, M. G. Johnson, P. M. Farmwald, B. Herner, US Patent 7129538
55. "Patterning three dimensional structures", C. K. Li, J. N. Knall, M. A. Vyvoda, J. M. Cleeves, V. Subramanian, US Patent 7071565
56. "Monolithic three dimensional array of charge storage devices containing a planarized layer", T. H. Lee, V. Subramanian, J. M. Cleeves, A. J. Walker, C. J. Petti, I. G. Kouznetzov, M. G. Johnson, P. M. Farmwald, and B. Herner, US Patent 6881994
57. "Thermal processing for three dimensional circuits", V. Subramanian, J. M. Cleeves, J. N. Knall, C. K. Li, and M. A. Vyvoda, US Patent 6,770,939
58. "Vertically stacked field programmable nonvolatile memory and method of fabrication", M. G. Johnson, T. H. Lee, V. Subramanian, and P. M. Farmwald, US Patent 6780711
59. "Multigate semiconductor device with vertical channel current and method of fabrication", J. M. Cleeves and V. Subramanian, US Patent 6677204
60. "Thermal processing for three dimensional circuits", V. Subramanian, J. M. Cleeves, J. N. Knall, C. K. Li, and M. A. Vyvoda, US Patent 6624011
61. "Multigate semiconductor device with vertical channel current and method of fabrication", J. M. Cleeves and V. Subramanian, US Patent 6580124
62. "Patterning three dimensional structures", C. K. Li, J. N. Knall, M. A. Vyvoda, J. M. Cleeves, and V. Subramanian, US Patent 6627530
63. "Low cost three-dimensional memory array", M. Johnson, T. Lee, V. Subramanian, P. Farmwald, J. Knall, US Patent 6515888
64. "Integrated circuit structure including three-dimensional memory array", M. Johnson, T. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 6385074.
65. "FINFET transistor structures having double gate channel extending vertically from a substrate and methods of manufacture", C. Hu, T-J. King, V. Subramanian, L. Chang, X. Huang, Y-K. Choi, J. T. Kedzierski, N. Lindert, J. Bokor, W-C. Lee, US Patent 6413802
66. "Vertically stacked field programmable nonvolatile memory and method of fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6185122.
67. "Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6034882.
68. "Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication", M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6351406.

69. “Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleaves, US Patent 6483736.

Invited Magazine Articles, Books, Chapters, and Monographs

1. Chapter in “Inkjet Technology for Digital Fabrication”, Editors: Ian M. Hutchings, Graham D. Martin, Wiley, ISBN: 978-0470681985
2. Chapter in “Applications of Organic and Printed Electronics: A Technology-Enabled Revolution (Integrated Circuits and Systems), Editor: E. Cantatore, ISB: 978-1-461-43159-6
3. Chapter in “Inkjet-based Micromanufacturing”, Editors: Korvink, Smith, Shin, Wiley, ISBN: 978-3-527-31904-6
4. Chapter in “Organic Electronics II. More Materials and Applications”, Editor: H. Klauk, Wiley, ISBN: 978-3-527-32647-1
5. Chapter in “Transparent Electronics: From Synthesis to Applications”, Editors: A. Facchetti and T. Marks, Wiley, ISBN: 978-0-470-99077-3, 2010.
6. Chapter in “The chemistry of inkjet inks”, Editor: S. Magdassi, World Scientific Publishing Company, ISBN: 978-9812818218, 2009
7. Chapter in “Organic Field-Effect Transistors”, Editors: Z. Bao, and J. Locklin, CRC Press, ISBN: 978-0849380808, 2007
8. “Developments in printed RFID”, V. Subramanian, Pira Publishing, UK, 2006.
9. “3D Chips: Future Possibilities”, V. Subramanian, Silicon India, Feb 2003, pp. 24-25

Invited Conference Presentations

1. **Invited**, “Materials, Process, and Device Innovations for High-Performance Printed Electronics”, PRINSE’18 – The 5th Printed Intelligence Industry Seminar on Manufacturing Solutions for Customer Needs and Vision to the Future, Oulu, Finland, Jan 31-Feb 1, 2018.
2. **Invited**, “Highly scaled gravure printed organic transistors for high-performance printed organic electronics”, High-frequency printed and direct-written organic-hybrid integrated circuits (HEROIC) Workshop, Milan, Italy, Nov 8-10, 2017.
3. **Keynote**, “Printed Electronics: Innovations in Materials, Processes, and Devices”, Association of International Metallizers, Coaters, and Laminators (AIMCAL) R2R Conference USA 2017, Tampa, FL, Oct-15-18, 2017.
4. **Invited**, “High-performance gravure printed organic transistors”, 2017 European Materials Research Society Meeting, Strasbourg, France, May 22-26, 2017
5. **Invited**, “Printed Electronics: Innovations in Materials, Processes, and Devices”, 2017 International Thin Film Transistor Conference (ITC 2017), Austin, TX, February 23-24, 2017.
6. **Invited**, “High-speed Printing of Transistors: From Inks to Devices”, 2016 International Society of Coating Science and Technology Symposium (ISCST), Pittsburgh, PA, September 18-21, 2016.
7. **Keynote**, “Printed Electronics: Innovations in Materials, Processes, and Devices”, 2016 Canadian Printable Flexible Wearable electronics Symposium (CPES2016), April 19-20, Oakville, Canada
8. **Keynote**, “Printed Electronics: Innovations in Materials, Processes, and Device”, 2016 Society of Vacuum Coaters Techcon, Indianapolis, IN, May 10-13, 2016.
9. **Invited**, Subramanian, Vivek, Chung, Seungjun, Grau, Gerd and Scheideler, William J., “71-2: Invited Paper: Printed Transistors and MEMS for Large-Area Electronics”, 2016 Society for Information Display Symposium, San Francisco, May 20-27, 2016.
10. **Keynote**, “Printed Electronics: Innovations in Materials, Processes, and Devices”, 31st Philippine Chemistry Congress, Iloilo, Philippines, April 13-15, 2016.
11. **Keynote**, “Advanced Processes, Materials, and Devices for Emerging Printed Electronics Applications”, 3rd Swiss Conference on Printed Electronics and Functional Materials, Neuchatel, Switzerland, Oct 1-2, 2015.
12. **Invited**, “High-performance printed organic transistors: Materials, processes, and devices”, V. Subramanian, G. Grau, H. Kang, and R. Kitsomboonloha, 2015 American Chemical Society National Meeting and Exposition, Boston, MA, Aug 17th, 2015.

13. **Invited**, Subramanian, Vivek, Jaewon Jang, William Scheideler, and Sarah Swisher. "39.1: Invited Paper: Printed Inorganic Transistors Based on Transparent Oxides." In SID Symposium Digest of Technical Papers, vol. 46, no. 1, pp. 587-590. 2015.
14. **Plenary**, "Printed Electronics: Advanced Technologies Enabling New Applications", 2015 Flexible and Printed Electronics Conference, Monterey, CA, February 23-26, 2015.
15. **Invited**, "High-resolution gravure printing of organic thin film transistors for high-performance printed electronic systems", V. Subramanian, R. Kitsomboonloha, J. Cen, H. Kang, G. Grau, and W. J. Scheideler, Materials Research Society Fall Meeting, Boston, MA, Dec 3, 2014.
16. **Invited**, "Advanced printed electronics technologies for novel ubiquitous human interactive systems", 2014 CMOS Emerging Technologies Research Symposium, Grenoble, France, July 6-8, 2014.
17. **Invited**, "Printed Electronics: A pathway to functionally-rich systems", 64th annual IEEE Electronic Components and Technology Conference, Orlando, FL, May 27, 2014.
18. **Invited**, "Printed Electronics: The Confluence of Printing and Semiconductors", Canadian Printed Electronics Symposium, Montreal, Canada, April 9, 2013.
19. **Invited** "Modeling, scaling, and integration of gravure printing for fast switching Organic FETs", V. Subramanian, S. J. S. Morris, H. Kang, Materials Research Society Fall 2012 Meeting, Boston, MA, Nov 25-30, 2012
20. **Invited**, "Printed Nanoparticles as routes to high-performance printed conductors: Synthesis, Printing Processes, and Device Applications", V. Subramanian, H. Kang, R. Kitsomboonloha, and S. K. Volkman, The 2012 International Conference on Flexible and Printed Electronics ICFPE2012, Tokyo, Japan, September 6th - 8th, 2012
21. **Invited** "Advanced Printing Processes for High-Performance Printed Transistors", V. Subramanian, Flextech Workshop on Printing Electronics - Ink and Substrate Interactions, Kalamazoo, MI, August 1-2, 2012
22. **Invited** "High-performance Printed Transistors: Materials, Processes, and Devices", V. Subramanian, 2nd CPEM International Symposium "Organic Semiconductors and Printed Electronics", Gyeonggi, South Korea, May 10th, 2012.
23. **Invited** "Highly-Scaled Gravure and Inkjet Printed Organic Transistors: Tools, Processes, and Devices", Hongki Kang & Vivek Subramanian, 2012 Flextech Flexible Electronics and Display Conference, Phoenix, AZ, Feb 5-9, 2012.
24. **Plenary** "Nanomaterials for printed electronics: synthesis, design, and applications", V. Subramanian, International Conference on Nano Science and Nano Technology, Sunchon, Korea, November 11th, 2011.
25. **Invited** "Advances in scaling of printed transistors", V. Subramanian, International Seminar on Printed Electronics, Seoul, Korea, June 8th, 2011.
26. **Invited** "High-Performance Fully Printed Transistors: Materials, Processes, and Device Characteristics", V. Subramanian, H. Tseng, R. Kitsomboonloha, and A. de la Fuente Vornbrock, 2011 Electrochemical Society Meeting, Montreal, Canada, May 2011
27. **Invited** "From Droplets to Devices: Printed Transistor Processes, Integration, and Characteristics", Vivek Subramanian, Daniel Soltman, Huai-Yuan Tseng, Rungrot Kitsomboonloha and Alejandro de la Fuente Vornbrock, Materials Research Society Spring Meeting, San Francisco, CA, April 2011
28. **Keynote** "Printed electronics: Innovations in tools, materials, devices, and applications", V. Subramanian, 2011 Korea Printed Electronics Association (KoPeA) meeting, Seoul, Korea, March 2011
29. **Keynote** "Printed RF tags and sensors: the confluence of printing and semiconductors", V. Subramanian, F. Liao, and H-Y. Tseng, The European Microwave Integrated Circuits Conference 2010, Paris, France, September 2010.
30. **Invited** "Droplet-on-demand direct patterning of active materials: materials, modeling, and integration", V. Subramanian, The 2010 IEEE Lithography Workshop, Kuai, Hawaii, November 2010
31. **Plenary** "Printed electronics: where are we, and where are we going", V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.
32. **Keynote** "Printed RFID: Technology Trends and Outlook", V. Subramanian, IEEE International Conference on RFID 2010, Orlando, Florida, April 2010.
33. **Invited** "Mechanistic studies on sintering of nanoparticles for formation of solution-processed thin films", 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.

34. **Invited** “Printed Electronics: the confluence of printing and semiconductors”, Vivek Subramanian, 2009 International Conference on Flexible and Printing Electronics, Jeju Island, Korea, Nov 2009.
35. **Invited** “Organic Transistor Vapor and Biosensors – Technology Status and Implementation Issues”, Vivek Subramanian, Frank Liao, Lakshmi Jagannathan, Electrochemical Society Meeting, Vienna, Austria, October 2009.
36. **Invited** “Printed transistors for low-cost electronics: the confluence of printing and printable electronic materials”, Vivek Subramanian, Alejandro de la Fuente Vornbrock, Steven Molesa, Daniel Soltman, Huai-Yuan Tseng, and Steven K. Volkman, SPIE Optics + Photonics, August 2-6, 2009, San Diego, CA
37. **Invited** “Printed Zinc Oxide Based Electronics: Materials, Devices, and Outlook”, V. Subramanian, S. K. Volkman, and D. R. Redinger, LOPE-C, June 23-25, 2009, Frankfurt, Germany
38. **Invited** “Printed Devices for Low-Cost Electronics: Technology Status and Outlook”, V. Subramanian, PETEC Inaugural Event, March 17, 2009, Durham, United Kingdom
39. **invited** “Printed Electronic Tags and Sensors for Smart Packaging Applications”, Vivek Subramanian, Josephine Chang, Lakshmi Jagannathan, Frank Liao, Steve Molesa, David Redinger, Daniel Soltman, Huai-Yuan Tseng, Steve Volkman, Shong Yin, 2009 Flexible Electronics and Display Conference, Phoenix, AZ, Feb 2-5, 2009.
40. **invited** “Electronic Nose Sensors for Consumer Packaging”, V. Subramanian, IDTechEx Printed Electronics USA, San Jose, CA, Dec 2-5, 2008.
41. **invited** “Solution-Processed Transparent Transistors for Low-Cost, Flexible Displays”, V. Subramanian, S. K. Volkman, and D. R. Redinger, LEOS 2008: The 21st Annual Meeting of the IEEE Lasers and Electro-Optics Society, Newport Beach, CA, 9-13 November, 2008.
42. **invited** “Organic chemical and biosensors for smart packages”, V. Subramanian, IDTechEx Printed Electronics Asia, Tokyo, Japan, Oct 8-9, 2008.
43. **invited** “Printed Electronics for Low-Cost Tags, Displays, and Sensors”, V. Subramanian, 1st International Conference on R2R Printed Electronics, Seoul, Korea, April 30-May 2, 2008.
44. **invited** “Printed organic RFID tags: technology, roadmaps, and challenges”, V. Subramanian, 1st Plastic Electronics Asia Conference and Showcase, Seoul, Korea, June 24-26, 2008
45. **invited** “Power supply considerations and solutions for printed electronic tags and sensors”, V. Subramanian, IDTechEx Printed Electronics Europe, Dresden, Germany, April 8-9, 2008
46. **invited** “Printed Chemical and Biosensors: Technology, Design and Challenges”, GOSPEL Workshop on Plastic Chemical Sensors, Dresden, Germany, April 9, 2008
47. **Plenary** “Printed Electronics For Low-Cost Electronic Systems: Technology Status and Application Development”, Vivek Subramanian, Josephine B. Chang, Alejandro de la Fuente Vornbrock, Daniel C. Huang, Lakshmi Jagannathan, Frank Liao, Brian Mattis, Steven Molesa, David R. Redinger, Daniel Soltman, Steven K. Volkman, Qintao Zhang, 38th European Solid State Device Research Conference, Edinburgh, Scotland, September 15-19, 2008
48. **invited** “Printed Organic Transistors for Low-cost Tags, Displays, and Sensors: Technology, Modeling and Challenges”, Vivek Subramanian, Alejandro de la Fuente Vornbrock, Huai-Yuan Tseng and Shong Yin, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008.
49. **invited** “Printed Electronics for Low-Cost Tags and Sensors”, Vivek Subramanian, Sixth Annual Workshop on Microelectronics and Electron Devices, April 18, 2008.
50. **invited** “Printed organic RF tags, chemical sensors and biosensors”, Vivek Subramanian, International Symposium for Flexible Electronics and Display, Hsinchu, Taiwan, Nov 18, 2007.
51. **invited** “Printed Tags and Sensors for RFID: Opportunities and Challenges”, Vivek Subramanian, Printed Electronics USA 2007, San Francisco, CA, Nov 14, 2007.
52. **invited** “Printed RFID Tags: Materials, Processes, and Devices”, Vivek Subramanian, Daniel Soltman, Daniel Huang, Steven Molesa, 2007 AiChE Annual Meeting, Salt Lake City, UT, Nov. 8, 2007.
53. **invited** “Printed organic RFID tags: technology, roadmaps, and challenges”, Vivek Subramanian, 3rd Global Plastic Electronics Conference and Showcase, Frankfurt, Germany, Oct 30, 2007.
54. **invited** “Printed organic transistors: technology, characteristics, and modeling”, Vivek Subramanian, Alejandro de la Fuente Vornbrock, Daniel Soltman, Huai-Yuan Tseng, and Steve Molesa, 212th meeting of the Electrochemical Society, Washington, DC, Oct 8, 2007.

55. **invited** "Printed electronic tags and sensors - device, materials, and circuit issues", Vivek Subramanian, 2007 Organic Electronics Conference and Exhibition, Frankfurt, Germany, Sept 25, 2007.
56. **invited** "Inkjet printing of transistors, diodes, and passive components for smart tags", Vivek Subramanian, Innovations in Inkjet: 3rd DPI Inkjet Workshop, Eindhoven Institute of Technology, Netherlands, June 28-29, 2007.
57. **invited** "Printed organic transistors", A. de la Fuente and V. Subramanian, Industry Forum on Printed Electronics, Chicago, IL, April 23-24, 2007
58. **invited** "From Materials to Circuits: Implications of printed materials on printed RFID", V. Subramanian, 2007 Pira printed RFID conference, Frankfurt, Germany, June 4-6, 2007.
59. **keynote** "Droplet on demand lithography: An enabling technology for low-cost electronics", V. Subramanian, A. de la Fuente Vornbrock, S. Moles, D. Redinger, Q. Zhang, and S. K. Volkman, SPIE Advanced lithography, 27th February, 2007
60. **invited** "Printed RFID tags: performance needs and technology trends", V. Subramanian, 2007 IDTechEx Smart labels USA, Boston, MA, February 20-23, 2007.
61. **keynote** "Printed Organic Transistors for low-cost tagging and sensing applications", V. Subramanian, J. Chang, A. de la Fuente Vornbrock, S. Moles, D. Soltman, and Q. Zhang. 6th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics, Tokyo, January 15th-18th, 2007.
62. **invited** "Nano Inks for Printed RFID", V. Subramanian, Pira Nanoscale Inks and Pigment Technologies Conference, Chicago, IL, Sept 27-28, 2006.
63. **invited** "Toward Printed RFID: Materials, Processes, and Devices", V. Subramanian, 5th Annual Printed Electronics and Displays Conference and Trade Fair, Las Vegas, Oct 11-13, 2006.
64. **invited** "Inkjetted Organic Transistors for Smart Tagging Applications", Vivek Subramanian, Jean M. J. Frechet, Steven Moles, Josephine Chang, Amanda R. Murphy, Alejandro de la Fuente Vornbrock, Steven Volkman, 2006 AiChE Annual Meeting, Nov 17th, 2006
65. **invited focal paper** "All-printed electronics: Materials, Devices, and Circuit Implications", V. Subramanian, J. Chang, S. Moles, D. Redinger, and S. Volkman, Digital Fabrication 2006, Denver, CO, Sept 17-22, 2006.
66. **invited** "Printed transistors and passive components for low-cost electronics applications", V. Subramanian, J. B. Chang, S. E. Moles, S. K. Volkman, and D. R. Redinger, International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA) April, 2006, pp. 68-9.
67. **invited** "Advanced printed materials and devices for RFID applications", V. Subramanian, IDTechEx Printed Electronics Europe, April 19-21, 2006.
68. **invited** "Printed Electronic Nose Vapor Sensors for Consumer Product Monitoring", V. Subramanian, J. Lee, V. Liu, S. Moles, IEEE International Solid State Circuits Conference, Paper 15.3, February, 2006.
69. **invited** "Nanotechnology in Printed Electronics: Nanoparticles, Nanorods, and Nanowhy", V. Subramanian, Pira Pack Electronics Conference, January 25-26, 2006.
70. **invited** "All-printed RFID Tags: Materials, Devices, and Circuit Implications", Vivek Subramanian, Paul C. Chang, Daniel Huang, Josephine B. Lee, Steven E. Moles, David R. Redinger, and Steven K. Volkman, VLSI Design, 2006, Hyderabad India, Jan 2006.
71. **invited** "Printed organic transistors: materials and technology", Vivek Subramanian, Pacificchem 2005: American Chemical Society Pacific Basin meeting, December 15-20, 2005, Honolulu, HI,
72. **invited** "Low-cost arrayed gas sensors for environmental monitoring". Vivek Subramanian, Josephine Lee and Vincent Liu, Materials Research Society Fall Symposium, Paper S2.1, Boston, MA, December 2005.
73. **invited** "Prospects for All-printed RFID: Materials, Devices, Circuits", V. Subramanian, International Workshop on Radio Frequency Identification (RFID) and Wireless Sensors, 11-13 November, 2005, Kanpur, India.
74. **invited** "Printed electronics for low-cost tagging applications", V. Subramanian, 2005 International Symposium on Flexible Electronics and Display, Hsinchu, Taiwan, October 2005.
75. **invited** "Printed electronic nose gas sensors", Vivek Subramanian, Plastic Electronics 2005, Frankfurt, Germany, Oct 4-5, 2005

76. **invited** "Uses of nanotechnology in printed electronics", Vivek Subramanian, Printed Electronics 205, Pira International, Thistle Marble Arch, London, UK, Sept 14-15, 2005
77. **invited** "Printed organic transistors for low-cost RFID applications", Vivek Subramanian, Proceedings of SPIE-The International Society for Optical Engineering vol. 5940, (594013/1-594013/9) , pp. 170-178, 2005.
78. **invited** "Advanced printed materials and devices for ultra-low-cost RFID", Vivek Subramanian, Printed RFID: Achieving low cost tags through printed electronics – Pira International, Gatwick, Surrey, UK, May 10-11, 2005.
79. **Plenary session invited talk** "Printed Organic Transistors for Ultra-low-cost RFID Applications", Vivek Subramanian, Paul C. Chang, Josephine B. Lee, Steven E. Molesa, and Steven K. Volkman, Polytronic 2004: 4th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics, Portland, Oregon, USA, 12 September 2004.
80. **invited** "Materials, Device, and Circuits Issues for low-cost printed RFID", V. Subramanian, 2nd Cintelliq Organic Semiconductor Conference, 2004 (OSC-2004), Cambridge, England, October 2004.
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Conference Presentations

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2. B. Mazinani, V. Subramanian, "Synthesis and characterization of highly durable P2O5-ZnO-Na2O/CaO-Fe2O3 glasses for low-temperature sealing applications", 2023 European Materials Research Society Spring Meeting, Strasbourg, France, May 29-June 2, 2023
3. M. Fadlelmula, V. Subramanian, "A Sol-gel inkjet printable PZT ink for additively fabricated mechanical transducers for energy harvesting, sensing, and mechanical actuation", 2023 European Materials Research Society Spring Meeting, Strasbourg, France, May 29-June 2, 2023
4. A. Hodaiei, V. Subramanian, "All-Additively-Fabricated Microsupercapacitors: Fine-Tuning Chemistry to Maximize Performance", 2023 European Materials Research Society Spring Meeting, Strasbourg, France, May 29-June 2, 2023
5. M. Deng, V. Subramanian, "Understanding and insight of paste formulation and curing behavior with sub-100-nanometer Ag-Cu core-shell nanoparticles", 10th Metallization and Interconnection Workshop, Genk, Belgium, Nov 14-15, 2022.
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7. R. Kumar, E. Kedzie, B. D. McCloskey, and V. Subramanian, "Characterizing Zn Corrosion in Printed Zn-Air batteries Via Operando Dens, XRD, and XAS", Electrochemical Conference on Energy and the Environment: Bioelectrochemistry and Energy Storage, MA2019-04 July 21-26, 2019, Glasgow, Scotland

8. Carlos Biao, Matt McPhail, Vivek Subramanian and Oscar Dubon, "Comprehensive Multifactorial Studies on the Degradation of Perovskite Solar Cells in Operation", 2019 Spring Materials Research Society Meeting, Phoenix, AZ, April 22-26, 2019.
9. Rajan Kumar, Jessica E. Nichols, Bryan D. McCloskey, and Vivek Subramanian, "Low-Temperature-Processing of Printed Cathodes for Aqueous Metal-Air Batteries", ECS AiMES 2018 Meeting, September 30, 2018 - October 4, 2018, Cancun, Mexico
10. N. Deka and V. Subramanian, "First demonstration of vacuum-sealed fully integrated BEOL-compatible field emission devices for Si integrated high voltage applications," 2018 76th Device Research Conference (DRC), Santa Barbara, CA, 2018, pp. 1-2.
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13. "Morphological Control of Gravure Printed Perovskite Films", M. McPhail and V. Subramanian, 2017 Materials Research Society Fall meeting, Boston, MA, Nov 29, 2017.
14. "Improving high-speed nanomaterial printing with sub-process-decoupled gravure printer design", W. Scheideler, V. Subramanian, ASME 2017 Conference on Smart Materials, Adaptive Structures, and Intelligent Systems, Snowbird, UT, Sept 18-20, 2017
15. "Development of a printed cathode and catalyst layer for printed zinc-air batteries, R. Kumar, N. Williams, and V. Subramanian, 232nd ECS Meeting, National Harbor, MD, Oct 1-5, 2017.
16. "UV-annealing-enhanced stability in high-performance printed InOx transistors, W. Scheideler, V. Subramanian, 2017 IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Toyama, Japan, Feb 28-Mar 2, 2017.
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37. "Through silicon vias and thermocompression bonding using inkjet-printed gold nanoparticles for heterogeneous MEMS Integration", N. Quack, J. Sadie, V. Subramanian, and M. C. Wu, The 17th International Conference on Solid-State Sensors, Actuators and Microsystems, Barcelona, Spain, June 16-20, 2013.
38. "Micro-relay reliability improvement by inkjet-printed microshell encapsulation", Yenhao Chen, Eung Seok Park, I-Ru Chen, Louis Hutin, Vivek Subramanian, Tsu-Jae King Liu, The 17th International Conference on Solid-State Sensors, Actuators and Microsystems, Barcelona, Spain, June 16-20, 2013.
39. "Understanding the Enhanced Mobility of Transparent Metal-Oxide Semiconductor Thin-Film Transistors Utilizing High-k Dielectrics" Andre Zeumault, Jaewon Jang, Vivek Subramanian, 2013 Large Area, Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, June 11-13, 2013.
40. "High Performance Solution-Processed Thin-Film Transistors Based on In₂O₃ Nanocrystals: Investigating Effects of Annealing Conditions and Gate Dielectric", Sarah L. Swisher, Steve Volkman, and Vivek Subramanian, 2013 Large Area, Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, June 11-13, 2013.
41. "Printed Transistors on Paper: Towards Smart Consumer Product Packaging", Gerd Grau, Rungrot Kitsomboonloha, Sarah Swisher, Hongki Kang and Vivek Subramanian, 2013 Large Area, Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, June 11-13, 2013.
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44. "Experimental study of the residue film in direct gravure printing of electronics", Rungrot Kitsomboonloha, Umut Ceyhan, SJS Morris, Vivek Subramanian, 65th Annual Meeting of the APS Division of Fluid Dynamics, Volume 57, Number 17, San Diego, California, November 18-20, 2012

45. "Lubrication analysis of the nanometric coating film deposited during gravure printing", Umut Ceyhan, Rungrot Kitsomboonloha, SJS Morris, Vivek Subramanian, 65th Annual Meeting of the APS Division of Fluid Dynamics, Volume 57, Number 17, San Diego, California, November 18–20, 2012
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52. "Resistance Switching Memory Device with Ag₂Se Nano-particle Aqueous Ink", Jaewon Jang, Feng Pan, Kyle Braam and Vivek Subramanian, 2012 Spring Materials Research Meeting.
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54. "Inkjet-Printed Microshell Encapsulation: A New Zero-Level Packaging Technology", Eung Seok Park, Jaeseok Jeon, Vivek Subramanian, and Tsu-Jae King Liu, The 25th International Conference on Micro Electro Mechanical Systems, Paris, France, January 29 – February 2, pp. 257-230, 2012.
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