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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Karl Pichler
Application No.:	10/137,163
Filing Date:	May 2, 2002
Group Art Unit:	2823
Examiner:	Lee, Hsien Ming
Title:	Improved Encapsulation for Organic Light Emitting Diodes Devices
Attorney Docket No.:	2002P03156US

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Alexandria, VA 22313-1450

Dear Sir:

RESPONSE PURSUANT TO 37 C.F.R. § 1.111

In response to the Office Action mailed June 19, 2003, please amend the above-identified application as follows:

AMENDMENTS TO THE SPECIFICATION begin on page 2 of this paper.

AMENDMENTS TO THE CLAIMS begin on page 3 of this paper.

REMARKS/ARGUMENTS begin on page 12 of this paper.

AMENDMENTS TO THE SPECIFICATION:

Please delete the Abstract.

Please insert the following Abstract:

An embodiment of an encapsulated OLED device is described. This embodiment of the encapsulated OLED device is formed by: fabricating multiple OLED devices on a substrate; depositing at least one planarization layer on the OLED devices; hardening the at least one planarization layer in a patterned manner such that the hardened region substantially covers the OLED device; removing areas of the at least one planarization layer that are not hardened; and selectively depositing at least one barrier layer over the hardened region.

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AMENDMENTS TO THE CLAIMS:

1. (original): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices;

hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said device;

removing areas of the at least one planarization layer that are not hardened; and

selectively depositing at least one barrier layer over said hardened region.

2. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises spin coating.

3. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises flash evaporation.

4. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises evaporation.

5. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises blade coating.

6. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises roll coating.

7. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises dip coating.

8. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises spray-coating.

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9. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises one among a group, said group comprising: screen printing and ink jet printing.

10. (original): The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises one of a group, said group comprising flood-exposure of UV light through a mask and scanning a line-source of UV light through a mask.

11. (original): The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises exposure by UV light comprising an optical patterning system.

12. (original): The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises exposure by UV light comprising a UV-beam scanning system.

13. (original): The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer further comprises one of a group, said group comprising: cross-linking, patterned heat transfer system, patterned IR source, masked IR source, scanned IR source, patterned e-beam, masked e-beam and scanned e-beam.

14. (currently amended): The method as recited in Claim 1 wherein the step of removing areas of the at least one ~~organic~~ planarization layer that are not ~~cross-linked~~ hardened comprises removing by thermal evaporation.

15. (original): The method as recited in Claim 14 wherein the step of removing by thermal evaporation further comprises applying a short high temperature pulse.

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16. (currently amended): The method as recited in Claim 15 wherein the step of applying a short high temperature pulse further comprises placing the ~~OLED plate~~ plurality of devices onto a hotplate.

17. (original): The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises removing by pumping in a vacuum.

18. (original): The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises removing by thermal evaporation and pumping in a vacuum.

19. (original): The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises one of a group, said group comprising: washing, blowing away, rinsing, sonicing, and plasma.

20. (original): The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises a barrier layer comprising one of a group, said group comprising a dielectric, a metal, a metal-oxide and an alloy.

21. (original): The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing said barrier layer through a mask.

22. (original): The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing the barrier layer in a larger area than the planarization layer.

23. (original): The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing one of a group, said

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group comprising: metal-oxide, dielectric layer, SiOx, SiNx , SiOxNy, AlOx, AlNx, ITO, ZnOx, Al-doped ZnOx, metal film, and alloy film.

24. (currently amended): The method as recited in Claim 1 wherein said plurality of devices are a plurality of OLED displays and substantially only [the] light emissive areas of said plurality of OLED displays are covered by the planarization layer and the barrier layer.

25. (original): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices wherein said planarization layer is deposited as an unpatterned liquid film;

selectively depositing at least one barrier layer over said planarization layer; and

removing said areas of unwanted planarization layer.

26. (original): The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises curing an organic layer selectively over the substrate.

27. (original): The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises curing an organic layer over the entire substrate.

28. (original): The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises evaporating a plurality of reactive organic molecules, said reactive organic molecules comprising a condensed conformal film on the substrate.

29. (original): The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises one of a group, said group comprising a

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Parylene coating of said organic layer over the substrate, and a plasma-assisted organic material deposition.

30. (original): The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises etching an organic layer.

31. (original): The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises etching an organic layer with a chemical etch process.

32. (original): The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises one of a group, said group comprising etching an organic layer with a plasma-assisted etching process, oxygen plasma, reactive ion-etch, anisotropic etch, laser assisted/based removal and laser ablation.

33. (original): The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises removing said organic layer.

34. (original): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

selectively depositing at least one planarization layer upon said devices; and

selectively depositing at least one barrier layer over said planarization layer.

35. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by ink jet of an organic layer.

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36. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by one of a group, said group comprising: screen printing of an organic layer and depositing by gas nozzle.

37. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing an organic layer through a shadow mask .

38. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by ink jet of said barrier layer.

39. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by screen printing of said barrier layer.

40. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises one of a group, said group comprising: depositing by shadow mask, sputtering, ink jet deposition, screen printing and evaporation.

41. (currently amended): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing a mask on top of said substrate, such that mask openings are placed on top of said devices;

depositing at least one planarization layer upon said mask and said plurality of devices;

removing said mask from said substrate; and

selectively depositing at least one barrier layer over said planarization layer.

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42. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises one of group, said group comprising: depositing a stamp mask, depositing a laminated film-mask, depositing a vacuum mask, magnetically held mask.

43. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing said mask such that said mask is in contact with said substrate.

44. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising a material substantially non-sticking to OLED substrate over the areas in between the active areas.

45. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising one of a group, said group comprising a metal, a ceramic, a plastic, a polymer, PTFE, and poly-siloxane.

46. (original): The method as recited in Claim 41 wherein the step of depositing at least one planarization layer further comprises depositing an organic layer over the entire mask.

47. (original): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices; and

depositing at least one barrier layer over planarization layer wherein at least one said step is accomplished in an inert atmosphere.

48. (original): The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is the step of depositing at least one planarization layer.

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49. (original): The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is the step of depositing at least one barrier layer.

50. (original): The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is both the step of depositing at least one planarization layer and the step of depositing at least one barrier layer.

51. (original): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices;

depositing at least one barrier layer over planarization layer; and

depositing a secondary encapsulation layer over said barrier layer.

52. (original): The method as recited in Claim 51 wherein the step of depositing a secondary encapsulation layer further comprises depositing one of a group, said group comprising: a plastic, a metal, a metal plus plastic foil, a polymer, and glass.

53. (currently amended): The method as recited in Claim 51 wherein the step of depositing a secondary encapsulation layer further comprises singulating the devices before the deposition of said secondary ~~encapuslation~~ encapsulation.

54. (original): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices; and

depositing at least one barrier layer over planarization layer wherein at least one said deposition step is accomplished by gas nozzle deposition.

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55. (original): The method as recited in Claim 54 wherein one said deposition step is accomplished by gas nozzle deposition further comprises depositing a layer over a plurality of devices with an array of nozzles positioned above said substrate.

56. (original): The method as recited in Claim 55 wherein the step of depositing a layer over a plurality of devices further comprises moving said array and said substrate in relative motion.

57. (original): An electronic device, said device comprising:

a substrate;

a plurality of active areas disposed upon said substrate;

a plurality of planarization layers disposed on said substrate whereby said planarization layer cover substantially only said active areas; and

a plurality of barrier layers disposed on said substrate whereby said barrier layers cover substantially only said planarization layers.

58. (original): The electronic device as recited in Claim 57 wherein said electronic device is one of a group, said group comprising an OLED, an organic electronic cir*Cuit*, an organic detector, an organic solar cell.

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REMARKS/ARGUMENTS

Claims 1-58 were considered by the Examiner. In the First Office Action, claims 1-58 were rejected. Objections were made to claims 14, 16, and 56. For the reasons set forth below, Applicants respectfully request reconsideration and allowance of all rejected and objected to claims.

Objection to Specification

The Examiner objected to the Abstract because claim phrases were used.

The original Abstract has been replaced with a new Abstract that does not use any claim phrases.

Since the original Abstract has been replaced, Applicants respectfully request reconsideration and withdrawal of this objection.

Objection to the Claims

The Examiner objects to claims 14, 16, and 56.

Applicants have amended claim 14 so that it is consistent with the terms used in claim 1.

Similarly, Applicants have amended claim 16 so that it is consistent with the terms used in claim 1.

Applicants have not amended claim 56 as specified by the Examiner because "depositing a layer" includes "depositing at least one planarization layer" and/or "depositing at least one barrier layer". "Depositing a layer" should not be limited to "depositing the at least one planarization layer" but rather includes depositing one or more planarization layers and/or barrier layers because claim 54 states that "at least one deposition step [i.e., this step is the "depositing at least one planarization layer" step and/or the "depositing at least one barrier layer" step] is accomplished by gas nozzle deposition" (brackets added). Therefore, Applicants respectfully submit that claim 56 is proper as originally written and does not have to be amended.

Applicants respectfully request reconsideration and withdrawal of the objections to the claims.

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Section 112 Rejection

Claim 24 is rejected under 35 U.S.C. §112, ¶2 for insufficient antecedent basis. Claim 24 has been amended such that "the" is removed from the term "the light emissive areas"; thus, this claim has been amended to remove the improper antecedent basis. Support for amended claim 24 is provided at, for example, page 9, lines 24-26 of the patent application.

Since claim 24 has been amended to remove the improper antecedent basis, Applicants respectfully request reconsideration and withdrawal of this rejection.

Section 102 Rejections

Section 102(b) Rejections

Claims 1, 10-12, 19-21, 25-27, and 34:

Claims 1, 10-12, 19-21, 25-27, 34 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,703,433 by *Fujii* et al. ("*Fujii*"). Applicants traverse this rejection for the reasons discussed below.

Applicants submit that *Fujii* does not disclose the method of encapsulating devices claimed in claim 1 or claim 25. More specifically, with respect to claim 1, Applicants submit that *Fujii* does not disclose "depositing at least one planarization layer upon said devices". In *Fujii*, the photoresist 4 is deposited on barrier ribs 2. See column 4, lines 30-33. The barrier ribs 2 are not devices but rather, the barrier ribs 2 are insulating separators that separate plasma pixels. The electrode 9 and the fluorescent substance 3 together may comprise a device, however, the barrier ribs 2 are not devices. In Applicant's specification at, for example, page 6, lines 29-31, devices are described as, for example, active areas on a substrate; in addition, on page 7, lines 3-5, devices are described as, e.g., an OLED display, an organic detector, or an organic solar cell. Since the photoresist 4 is deposited on the barrier ribs 2, *Fujii* does not disclose "depositing at least one planarization layer upon said devices" (underline added) as recited in claim 1.

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In addition, Applicants submit that *Fujii* does not disclose "selectively depositing at least one barrier layer over said hardened region" as recited in claim 1. At page 4 of the Office Action, the Examiner asserts that the fluorescent substance 3 is a barrier layer. However, the fluorescent substance 3 does not adequately prevent oxygen and moisture from permeating through it and therefore is not a barrier layer. In *Fujii*, the purpose of the fluorescent substance 3 is to emit light and not to inhibit the permeation of oxygen and moisture. The fluorescent substance 3 is not a barrier layer and, therefore, *Fujii* does not disclose depositing a "barrier layer" as recited in claim 1.

Also, *Fujii* does not disclose "depositing at least one barrier layer over said hardened region" (underline added) as recited in claim 1; the hardened regions is the hardened portions of the planarization layer. In *Fujii*, the fluorescent substance 3 is deposited over the substrate 1 rather than over the sandblasting mask 7 (i.e., the sandblasting mask 7 is the hardened portions of the photoresist 4; see column 4, lines 30-35). Therefore, *Fujii* does not disclose "depositing at least one barrier layer over said hardened region" (underline added) as recited in claim 1.

For at least these reasons, Applicants respectfully request reconsideration and allowance of claim 1. Claims 10-12, 19-21 depend from claim 1. Accordingly, they are patentable over *Fujii* at least for the reasons set forth above with respect to claim 1.

With respect to claim 25, Applicants submit that *Fujii* does not disclose "depositing at least one planarization layer upon said devices wherein said planarization layer is deposited as an unpatterned liquid film". As explained earlier with respect to claim 25, *Fujii* discloses depositing the photoresist 4 on barrier ribs 2 rather than on devices. Also, *Fujii* discloses depositing the photoresist 4 as a dry film rather than a "liquid film" as recited in claim 25. See *Fujii*, column 4, line 31. Therefore, *Fujii* does not disclose "depositing at least one planarization layer upon said devices wherein said planarization layer is deposited as an unpatterned liquid film" as recited in claim 25. In addition, *Fujii* does not disclose "selectively depositing at least one barrier layer over said planarization layer" (underline added) as recited in claim 25. In *Fujii*, the fluorescent substance 3 is deposited over the substrate 1 rather than over the sandblasting mask 7 (i.e., the sandblasting mask 7 is the hardened portions of the photoresist 4; see column 4,

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lines 30-35). Therefore, *Fujii* does not disclose "selectively depositing at least one barrier layer over said planarization layer" (underline added) as recited in claim 25.

For at least these reasons, Applicants respectfully request reconsideration and allowance of claim 25. Claims 26-27, and 34 depend from claim 25. Accordingly, they are patentable over *Fujii* at least for the reasons set forth above with respect to claim 25.

Claims 47-50:

Claims 47-50 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,072,227 by *Yau* et al. (*"Yau"*). Applicants traverse this rejection for the reasons discussed below.

Applicants submit that *Yau* does not disclose the method of encapsulating devices in claim 47. More specifically, with respect to claim 47, Applicants submit that *Yau* does not disclose "depositing at least one planarization layer upon said devices". In *Yau*, the "PECVD gap filling layer" 302 is deposited on the "PECVD lining layer" 300 which cover the metal lines 306, 308, 310. The "PECVD lining layer" 300 and the metal lines 306, 308, 310 together do not form devices. In Applicant's specification at, for example, page 6, lines 29-31, devices are described as, for example, active areas on a substrate; in addition, on page 7, lines 3-5, devices are described as, e.g., an OLED display, an organic detector, or an organic solar cell. The metal lines 306, 308, 310 themselves are not active areas and are not part of a device such as an OLED display or an organic detector. Since the "PECVD gap filling layer" is deposited on the metal lines/lining layer, *Yau* does not disclose "depositing at least one planarization layer upon said devices" (underline added) as recited in claim 47.

Moreover, the "PECVD gap filling layer" 302 cannot be used as a planarization layer because the "PECVD gap filling layer" 302 needs to be cured in order to remove water from this layer. See, e.g., *Yau*, column 12, lines 26-28. The curing process results in water being released onto the underlying object (e.g., device) and thus use of the "PECVD gap filling layer" 302 as the planarization layer defeats the purpose of a planarization layer which is to prevent water from reaching the object.

In addition, for claim 47, *Yau* does not disclose "wherein at least one said step is accomplished in an inert atmosphere". In *Yau*, the process gasses that form the "PECVD

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gap filling layer" 302 are carried to the intended destination (e.g., the PECVD lining layer 300) using an inert carrier gas. See e.g., *Yau*, column 12, lines 13-16. In *Yau*, the inert gas is used to carry the process gasses, however, *Yau* does not disclose that either the "PECVD gap filling layer" 302 or the "cap layer" 312 is deposited in an "inert atmosphere.

For at least these reasons, Applicants respectfully request reconsideration and allowance of claim 47. Claims 48-50 depend from claim 47. Accordingly, they are patentable over *Yau* at least for the reasons set forth above with respect to claim 47.

Section 102(e) Rejections

Claims 41, 43, 44-45:

Claims 41, 43, 44-45 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,271,135 by *Palmans* et al. (*"Palmans"*). Applicants traverse this rejection for the reasons discussed below.

Applicants submit that *Palmans* does not disclose the method of encapsulating devices in claim 41. More specifically, with respect to claim 41, Applicants submit that *Palmans* does not disclose "depositing at least one planarization layer upon said mask and said plurality of devices." In *Palmans*, the metal studs 5 (on page 5 of the Office Action, the Examiner asserts that the metal studs 5 are planarization layers) are deposited on the conductive pattern 2 (on page 5 of the Office Action, the Examiner asserts that the conductive pattern 2 are devices). The conductive pattern 2 are not devices as defined at, for example, page 6 and page 7 of Applicant's specification.

Moreover, the metal studs 5 cannot be used as a planarization layer because the metal studs 5 do not provide a flat surface. The metal studs 5 are formed by depositing a copper containing metal. See *Palmans*, column 4, lines 56-57. Metals, and copper in particular, that are evaporated onto a layer do not cover-up the imperfections of the underlying layer, but rather, the metals reproduce the topography of the underlying layer. Therefore, metals cannot be used as a planarization layer.

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For at least these reasons, Applicants respectfully request reconsideration and allowance of claim 41. Claims 43, 44-45 depend from claim 41. Accordingly, they are patentable over *Palmans* at least for the reasons set forth above with respect to claim 41.

Claims 51-55, and 57:

Claims 51-55 and 57 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,387,802 by *Marsh* (*"Marsh"*). Applicants traverse this rejection for the reasons discussed below.

In *Marsh*, the word line 124 that is made of the layers 130/132/134 is not a device, but rather the word line 124 is a control line used to control a capacitor having a lower electrode made of the platinum layer 152. Thus, in *Marsh*, the insulating layer 142/148 is not deposited upon a device and, therefore, *Marsh* does not disclose "depositing at least one planarization layer upon said devices" as recited in claim 51 and claim 54.

For at least this reason, Applicants respectfully request reconsideration and allowance of claim 51 and claim 54. Claims 52-53 depend from claim 51, and claim 55 depends from claim 54. Accordingly, they are patentable over *Marsh* at least for the reasons set forth above with respect to claims 51 and 54.

With respect to claim 57, *Marsh* does not disclose "a plurality of active areas disposed upon said substrate" as recited in that claim. The "layers 130/132/134" (on page 6 of the Office Action, the Examiner asserts that the "layer 130/132/134" are devices) are not active areas of a device, but rather these layers make up a word line that is a control line used to control the capacitor. In addition, *Marsh* does not disclose "a plurality of planarization layers disposed on said substrate whereby said planarization layers cover substantially only said active areas" as recited in claim 57. In *Marsh*, the "layers 142, 146" (on page 6 of the Office Action, the Examiner asserts that the "layers 142/146" are planarization layers) extend past the "layers 130, 132, 134" such that the "layers 142, 146" also cover, for example, the active layer 118, the nitride layer 140, and the sidewall insulating spacer 138. Moreover, *Marsh* does not disclose "a plurality of barrier layers disposed on said substrate whereby said barrier layers cover substantially only said planarization layers" as recited in claim 57. In *Marsh*, the barrier layer 157

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extends past the "layers 142, 146" to cover, for example, the nitride layer 140 and the sidewall insulating spacer 138.

For at least these reasons, Applicants respectfully request reconsideration and allowance of claim 57.

Section 103 Rejections

Claims 13-15:

Claims 13-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Fujii* in view of U.S. Patent No. 6,524,937 by *Cheng* et al. ("*Cheng*") ("the proposed combination").

With respect to claims 13-15, Applicants submit that the proposed combination does not disclose "depositing at least one planarization layer upon said devices". In *Fujii* and *Cheng*, layers are not deposited on devices, but rather, the layers are deposited on metal lines on a substrate. In addition, for claim 14, the proposed combination does not disclose "removing areas of the at least one organic layer that are not cross-linked comprises removing by thermal evaporation." The proposed combination discloses removing areas by spraying an aqueous solution. See, *Fujii*, column 4, lines 41-42. Moreover, for claim 15, the proposed combination does not disclose "wherein the step of removing by thermal evaporation further comprises applying a short high temperature pulse."

In addition, Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Fujii* and *Cheng* references. The Examiner has the burden of showing that the cited references provide a suggestion to combine them. *See* MPEP 2142. In *Fujii*, the photoresist layer is patterned to form sandblasting masks so that the fluorescent substance of a plasma display can be sandblasted such that it's wider towards a front plate. In *Cheng*, the photoresist layer forms a portion of a T-shaped gate of a field effect transistor. In the two references, the photoresist layers are used for different purposes and for different devices, and there is no explicit or implicit suggestion in the references to combine them.

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For at least these reasons, Applicants respectfully request reconsideration and allowance of claims 13-15.

Claims 2-4, 6-9, 22-23, 30-31, 33, 35-36, 38-40:

Claims 2-4, 6-9, 22-23, 30-31, 33, 35-36, 38-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Fujii* in view of U.S. Patent No. 6,498,114 by *Amundson* et al. ("*Amundson*") ("the proposed combination").

With respect to claims 2-4, 6-9, 22-23, 30-31, 33, 35-36, 38-40, Applicants submit that the proposed combination does not disclose "depositing at least one planarization layer upon said devices" as recited in claim 1. In *Fujii* and *Amundson*, the layers (i.e., the photoresist layer 4 of *Fujii* and the organic semiconductor layer 20 of *Amundson*) are not deposited on devices, but rather, the layers are deposited on metal lines (*Fujii*) or on a dielectric 30 ("*Amundson*"). In *Amundson*, the organic semiconductor film 20 is an active layer of the transistor rather than a planarization layer that is used to encapsulate the device.

In addition, Applicants submit that the proposed combination does not disclose "selectively depositing at least one barrier layer over said hardened region" (claim 1) or "selectively depositing at least one barrier layer over said planarization layer" (claims 25, 34). The proposed combination does not disclose a barrier layer and does not disclose that the barrier layer is selectively deposited over a hardened region or over a planarization layer (for more details, please refer to the earlier discussion for claim 1).

For claim 22, the proposed combination does not disclose "depositing the barrier layer in a larger area than the planarization layer" since the fluorescent substance 3 is not an adequate barrier layer (for more details, please refer to the earlier discussion for claim 1). Moreover, for claim 23, the proposed combination does not disclose the listed barrier materials. Also, for claims 38-40, the proposed combination does not disclose depositing the barrier layer using the methods listed in those claims.

In addition, Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Fujii* and the *Amundson* references. The Examiner has the burden of showing that the cited references provide a suggestion to combine them. *See* MPEP

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2142. In *Fujii*, the photoresist layer 4 are patterned to form sandblasting masks so that the fluorescent substance 3 is wider toward a front plate. In *Amundson*, the semiconductor layer 20 is not a photoresist layer but rather the active material of a transistor. In the two references, the photoresist layer 4 of *Fujii* and the semiconductor layer 20 of *Amundson* perform different functions, are used for different purposes, are used for different devices, and there is no explicit or implicit suggestion in the references to combine them.

For at least these reasons, Applicants respectfully request reconsideration and allowance of claims 2-4, 6-9, 22-23, 30-31, 33, 35-36, 38-40.

Claim 5:

Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Fujii* in view of U.S. Patent Publication No. 2002/0155661 by *Massingill* et al. ("*Massingill*") ("the proposed combination").

With respect to claim 5, Applicants submit that the proposed combination does not disclose "selectively depositing at least one barrier layer over said hardened region" as recited in claim 1. Neither *Fujii* nor *Massingill* discloses depositing a barrier layer over the planarization layer (i.e., the hardened region). Also, neither *Fujii* nor *Massingill* discloses "depositing at least one barrier layer over said hardened region" (underline added) as recited in claim 1. In *Fujii*, the fluorescent substance 3 (in the earlier Office Action, the Examiner asserted that the fluorescent substance is the barrier layer) is deposited over the substrate rather than over the sandblasting mask 7 (in the earlier Office Action, the Examiner asserted that the sandblasting mask 7 is the planarization layer). In *Massingill*, a separate barrier layer is not disclosed nor suggested.

In addition, Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Fujii* and the *Massingill* references. The Examiner has the burden of showing that the cited references provide a suggestion to combine them. *See* MPEP 2142. In *Fujii*, the photoresist layer 4 are patterned to form sandblasting masks so that the fluorescent substance 3 of a plasma display can be sandblasted so that it's wider toward a front plate. In *Massingill*, the photoresist layer covers the capacitors. In the two

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references, the photoresist layer 4 of *Fujii* and the photoresist layer of *Massingill* perform different functions, are used for different purposes, are used for different devices, and there is no explicit or implicit suggestion in the references to combine them.

For at least these reasons, Applicants respectfully request reconsideration and allowance of claim 5.

Claims 17-18:

Claims 17-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Fujii* in view of U.S. Patent No. 5,369,151 by *Fujibayasni* et al. ("*Fujibayasni*") ("the proposed combination").

Applicants submit that proposed combination does not disclose "depositing at least one planarization layer upon said devices" as recited in claim 1. In *Fujii*, the layer is not deposited on devices, but rather, the layer is deposited on metal lines. *Fujibayasni* does not disclose use of a planarization layer; in *Fujibayasni*, it is disclosed to use an organic solvent to remove a predetermined amount of reaction product water but the organic solvent is not used to form a planarization layer. *See Fujibayasni*, column 8, lines 42-47. In addition, Applicants submit that the proposed combination does not disclose "selectively depositing at least one barrier layer over said hardened region". The fluorescent substance 3 of *Fujii* is not a barrier layer, and *Fujibayasni* does not disclose use of a barrier layer. Moreover, the proposed combination does not disclose "depositing at least one barrier layer over said hardened region" (underline added) as recited in claim 1. In *Fujii*, the fluorescent substance 3 is deposited over the substrate 1 rather than over the sandblasting mask 7, and *Fujibayasni* does not disclose use of a barrier layer.

In addition, Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Fujii* and the *Fujibayasni* references. The Examiner has the burden of showing that the cited references provide a suggestion to combine them. *See* MPEP 2142. In *Fujii*, the photoresist layer 4 is patterned to form sandblasting masks so that the fluorescent substance 3 is wider toward a front plate. In *Fujibayasni*, a planarization layer is not disclosed or suggested, therefore, this reference does not disclose or suggest removing the planarization layer by vacuum. Because *Fujibayasni* does not even

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disclose or suggest a planarization layer, there is no suggestion to combine these two references to show that the planarization layer can be removed using a vacuum.

For at least these reasons, Applicants respectfully request reconsideration and allowance of claims 17-18.

Claims 16 and 24:

Claims 16 and 24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Fujii* in view of U.S. Patent No. 6,498,114 by *Amundson* et al. ("*Amundson*"), and further in view of U.S. Patent No. 6,500,604 by *Dimitrakopoulos* et al. ("*Dimitrakopoulos*") ("the proposed combination").

Applicants submit that the proposed combination does not disclose "depositing at least one planarization layer upon said devices" as recited in claim 1. For the reasons stated earlier, the proposed combination does not disclose depositing the planarization layer upon the devices, but rather discloses depositing the layer on metal lines (*Fujii*), on the organic layer (*Dimitrakopoulos*), and on a dielectric 30 (*Amundson*). In addition, with respect to claim 16, the proposed combination does not disclose or suggest "placing the OLED plate onto a hotplate." With respect to claim 24, the proposed combination does not disclose or suggest that "substantially only the light emissive areas are covered by the planarization layer and the barrier layer."

In addition, Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine *Fujii*, *Dimitrakopoulos*, and *Amundson*. The Examiner has the burden of showing that the cited references provide a suggestion to combine them. *See* MPEP 2142. These references cannot be combined because, as explained earlier, the purported planarization layer in these references perform different functions, are deposited for different purposes, and there is no explicit or implicit suggestion in the references to combine them.

For at least these reasons, Applicants respectfully request reconsideration and allowance of claims 16 and 24.

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Claim 37:

Claim 37 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Fujii* in view of U.S. Patent No. 6,146,715 by *Kim* et al. ("*Kim*") ("the proposed combination").

Applicants submit that the proposed combination does not disclose "selectively depositing at least one planarization layer upon said devices" as recited in claim 34. For the reasons stated earlier, the proposed combination does not disclose depositing the planarization layer upon the devices, but rather discloses depositing the layer on metal lines (*Fujii*). In *Kim*, the use of a planarization layer is not disclosed or suggested at all. In addition, the proposed combination does not disclose "selectively depositing at least one barrier layer over said planarization layer" as recited in claim 34.

In addition, Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine *Fujii* and *Kim*. The Examiner has the burden of showing that the cited references provide a suggestion to combine them. *See* MPEP 2142. These references cannot be combined because *Kim* teaches away from the use of shadow mask. In the Abstract section of *Kim*, it states that the organic EL display is pixilated "without using a shadow mask". In the "Background" section of *Kim*, the disadvantages of shadow masks are listed including: "difficulties in making the shadow mask itself and difficulties in aligning the shadow mask"; the invention of *Kim* provides an alternative to using shadow masks. In addition, *Kim* uses the shadow masks to deposit the organic electroluminescent material rather than a planarization layer. For these reasons, there is no suggestion to combine these two references.

For at least these reasons, Applicants respectfully request reconsideration and allowance of claim 37.

Claims 42 and 46:

Claims 42 and 46 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Palmans* in view of U.S. Patent No. 6,103,456 by *Tobben* et al. ("*Tobben*") ("the proposed combination").

Applicants submit that the proposed combination does not disclose or suggest "depositing at least one planarization layer upon said mask and said plurality of devices"

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as recited in claim 41. In *Palmans*, the metal studs 5 are deposited on the conductive pattern 2 rather than on the devices. In *Tobben*, the organic layer 24 is the active layer of the device and a photoresist layer 25 is deposited on the organic layer 24. The photoresist layer 25 is not deposited on a device, but rather the photoresist layers 25 is deposited on the organic layer 24.

For at least these reasons, Applicants respectfully request reconsideration and allowance of claim 41.

Claims 56 and 58:

Claims 56 and 58 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Marsh* in view of U.S. Patent No. 6,148,764 by *Cui* et al. ("*Cui*") ("the proposed combination").

The proposed combination does not disclose or suggest "depositing at least one planarization layer upon said devices" as recited in claim 54, or "whereby said planarization layer cover substantially only said active areas" as recited in claim 57. In *Marsh*, the word line 124 that is made of the layers 130/132/134 is not a device, but rather the word line 124 is a control line used to control a capacitor having a lower electrode made of the platinum layer 152. *Cui* does not disclose or suggest using a planarization layer or a barrier layer.

In addition, Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine *Marsh* and *Cui*. The Examiner has the burden of showing that the cited references provide a suggestion to combine them. *See* MPEP 2142. These references cannot be combined because *Marsh* discloses depositing material using gas deposition but *Cui* discloses depositing material using jet vapor deposition. These two deposition techniques are different since gas deposition uses a high vacuum and the gas phase mean free path is large, but jet vapor deposition uses a low vacuum and the gas phase mean free path is small. See *Cui*, column 1, lines 34-46. Moreover, Cui does not disclose or suggest the planarization layer or the barrier layer and therefore there is no implicit or explicit suggestion to deposit the planarization layer or the barrier layer using nozzles where the nozzles and the substrate are moved relative to each other. These two

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deposition techniques are different from each other, and no implicit or explicit suggestion is provided in the references to combine them.

With respect to claim 58, the Examiner relies on the common knowledge of those skilled in the art to assert that this claim is obvious. However, if the Examiner is going to rely on the knowledge of those skilled in the art, then Applicants request that the Examiner provide evidence that the information is known to those skilled in the art as is required. *See, for example, In re Sang-Su Lee*, 277 F.3d at 1344.

For at least this reason, Applicants respectfully request reconsideration and allowance of claim 56 and claim 58.

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CONCLUSION

Applicants have made an earnest attempt to place this case in condition for allowance. For the foregoing reasons, and for other reasons clearly apparent, Applicants respectfully request allowance of all pending claims.

If the Examiner feels that a telephone conference or an interview would advance prosecution of this Application in any manner, the undersigned attorney for Applicants stands ready to conduct such a conference at the convenience of the Examiner.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayments to Deposit Account No. 19-2179 of Siemens Corp.

Date: Nov. 18, 2003

Respectfully requested,

SIEMENS CORPORATION
Intellectual Property Department
170 Wood Avenue South
Iselin, New Jersey 08830
ATTENTION: Elsa Keller, IP Department
Telephone: (732) 321-3026

By: Thomas George
Thomas George
Registration No. 45,740
Attorney for Applicants
Tel: 650-694-5191
Fax: 650-968-4517

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Attorney Docket Number: 2002P03156US

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Karl Pichler
Application No.:	10/137,163
Filing Date:	May 2, 2002
Group Art Unit:	2823
Examiner:	Lee, Hsien Ming
Title:	Improved Encapsulation for Organic Light Emitting Diodes Devices
Attorney Docket No.:	2002P03156US

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PETITION FOR EXTENSION OF TIME

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant(s) hereby petition(s) for a two month extension of time to respond to the Office Action with the mailing date of June 19, 2003. This two month extension will extend the due date from September 19, 2003 to November 19, 2003.

11/26/2003 CNGUYEN 00000138 192179 10137163
01 FC:1252 420.00 DA

Please charge the extension fee of $420.00 to Deposit Account No. 19-2179. A duplicate copy of this sheet is enclosed.

Date: Nov. 18, 2003

Respectfully requested,

SIEMENS CORPORATION
Intellectual Property Department
170 Wood Avenue South
Iselin, New Jersey 08830
ATTENTION: Elsa Keller, IP Department
Telephone: (732) 321-3026

By: Thomas George

Thomas George
Registration No. 45,740
Attorney for Applicants
Tel: 650-694-5191
Fax: 650-968-4517

PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10137163	05/02/2002	428	26	1775	H. LEE

953

**APPLICANTS: Pichler Karl; Firschknecht Kyle; 438 1745 2822

**CONTINUING DATA VERIFIED: Lee NONE

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** FOREIGN APPLICATIONS VERIFIED: Lee NONE

PG-PUB DO NOT PUBLISH ☐ RESCIND ☐

Foreign priority claimed	☐ yes ☒ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☒ no	2002P03156US
Verified and Acknowledged Examiners's intials	Lee	

TITLE : Encapsulation for organic light emitting diodes devices

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G.
ISSUE FEE: Amount Due / Date Paid		DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
TERMINAL DISCLAIMER	Primary Examiner	Application Examiner
	PREPARED FOR ISSUE	

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	28	6/11	
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	48		
	55		
	531		
	624		
	627		
	641		
257	900	"	"
	53		
	21		
	59		
	414		
	431		
	701		
	760		

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.

SEARCH NOTES

(List databas s searched. Attach search strategy inside.)

	Date	Exmr.
EAST attached	6/4/03	Lee
CUSPAT; USPG;	6/11/03	
EPO; JPO; IBM;	6/12/03	
Derwent)		

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INTERNATIONAL CLASSIFICATION			
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/			
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/			∧ Continued on Issue Slip Inside File Jacket

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INDEX OF CLAIMS

✓ .... Rejected	– (Through numeral) ... Canceled	N .... Non-elected	A .... Appeal
= .... Allowed	+ .... Restricted	I .... Interference	O .... Objected

Claim Final	Claim Original	Date 6/12/03	Claim Final	Claim Original	Date 6/12/03	Claim Final	Claim Original	Date
	1	✓		51	✓		101	
	2	✓		52	✓		102	
	3	✓		53	✓		103	
	4	✓		54	✓		104	
	5	✓		55	✓		105	
	6	✓		56	✓		106	
	7	✓		57	✓		107	
	8	✓		58	✓		108	
	9	✓		59			109	
	10	✓		60			110	
	11	✓		61			111	
	12	✓		62			112	
	13	✓		63			113	
	14	✓		64			114	
	15	✓		65			115	
	16	✓		66			116	
	17	✓		67			117	
	18	✓		68			118	
	19	✓		69			119	
	20	✓		70			120	
	21	✓		71			121	
	22	✓		72			122	
	23	✓		73			123	
	24	✓		74			124	
	25	✓		75			125	
	26	✓		76			126	
	27	✓		77			127	
	28	✓		78			128	
	29	✓		79			129	
	30	✓		80			130	
	31	✓		81			131	
	32	✓		82			132	
	33	✓		83			133	
	34	✓		84			134	
	35	✓		85			135	
	36	✓		86			136	
	37	✓		87			137	
	38	✓		88			138	
	39	✓		89			139	
	40	✓		90			140	
	41	✓		91			141	
	42	✓		92			142	
	43	✓		93			143	
	44	✓		94			144	
	45	✓		95			145	
	46	✓		96			146	
	47	✓		97			147	
	48	✓		98			148	
	49	✓		99			149	
	50	✓		100			150	

826 6/13/02 BB 9/13/02

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05-03-02 A

Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

PATENT APPLICATION
Attorney Docket No. : 2002P03156US
Express Mail Label No. EV 048645610US
Date of Deposit : May 2, 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

THE ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

TRANSMITTAL LETTER FOR NEW APPLICATION

Sir:

Transmitted herewith for filing is a(n) [X]Original patent application.
[X] Utility [ ] Design [ ]Continuation-in-part application

INVENTOR(S): Karl Pichler and Kyle D. Firschknecht

TITLE: IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

Enclosed with this Transmittal (submitted in duplicate) are:

[X] Twenty-four (24) page specification.
[X] Eight (8) sheets of drawings [ ] formal [X] informal drawings (one set)
[X] The Declaration and Power of Attorney [] signed [X] unsigned
[X] Filing fee has been calculated as shown below (other than small entity):

For	Number Filed	Number Extra	Rate	Additional Fees
Total Claims	58 - 20	= 38	x $ 18	$684.00
Indep. Claims	8 - 3	= 5	x $ 84	$420.00
[ ] First Presentation of a Multiple Dependent Claim			+ $260	$ -0-
		Basic filing Fee		$ 740.00
			Total	$1,844.00

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PLEASE MAIL CORRESPONDENCE TO:
Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

Respectfully submitted,
Stuart P. Kaler
Stuart P. Kaler, Reg. No. 35,913
Attorney(s) for Applicant(s)
Date: May 2, 2002
Telephone: 650-694-5191

J1131 U.S. PTO 05/02/02
Jc986 U.S. PTO 10/137163 05/02/02
10137163 050202

05-03-02 A

Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

PATENT APPLICATION
Attorney Docket No. : 2002P03156US
Express Mail Label No. EV 048645610US
Date of Deposit : May 2, 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

THE ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

TRANSMITTAL LETTER FOR NEW APPLICATION

Sir:

Transmitted herewith for filing is a(n) [X]Original patent application.
[X] Utility [ ] Design [ ]Continuation-in-part application

INVENTOR(S): Karl Pichler and Kyle D. Firschknecht

TITLE: IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

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Total Claims	58 - 20	= 38	x $ 18	$684.00
Indep. Claims	8 - 3	= 5	x $ 84	$420.00
[ ] First Presentation of a Multiple Dependent Claim			+ $260	$ -0-
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			Total	$1,844.00

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Respectfully submitted,
Stuart P. Kaler
Stuart P. Kaler, Reg. No. 35,913
Attorney(s) for Applicant(s)
Date: May 2, 2002
Telephone: 650-694-5191

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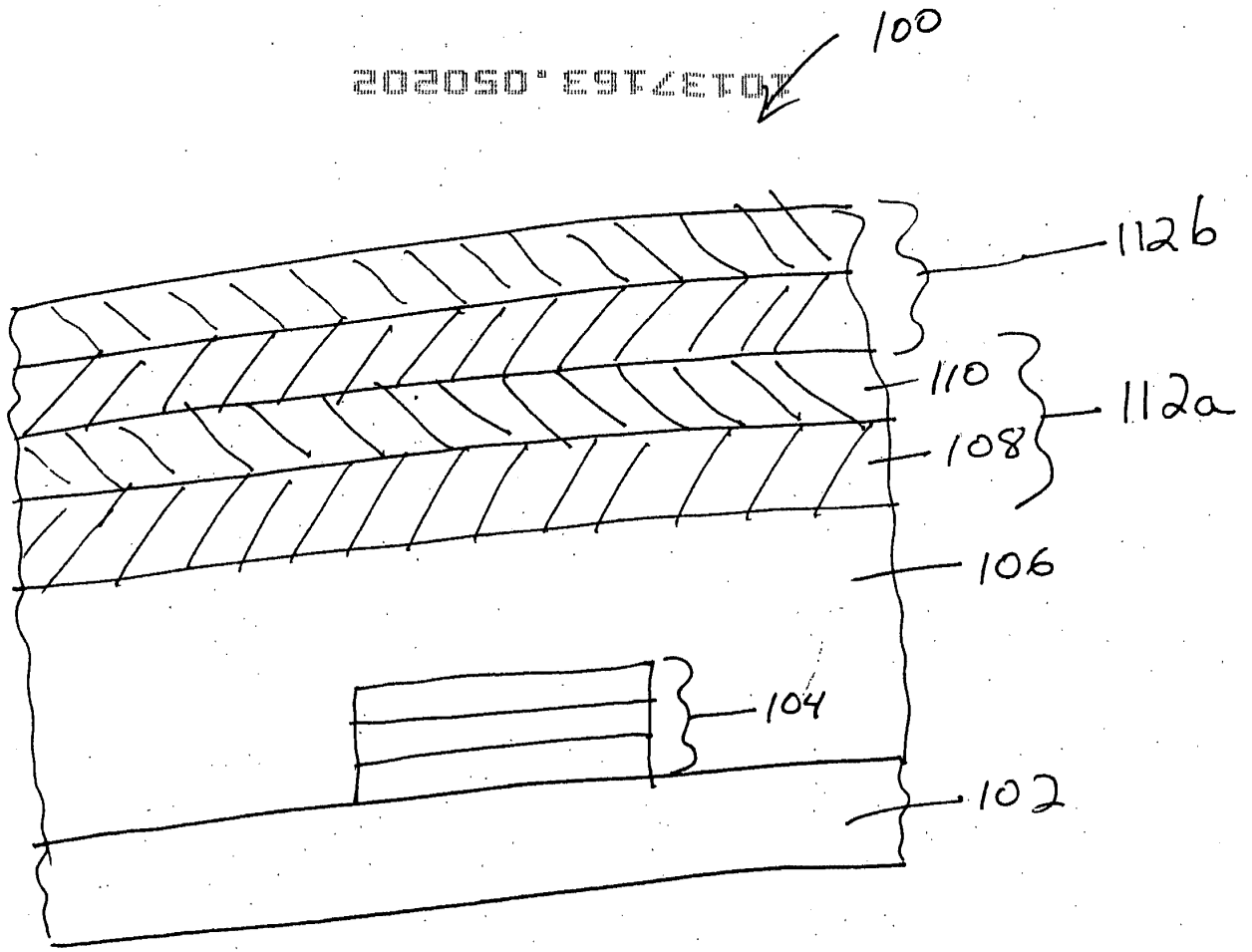
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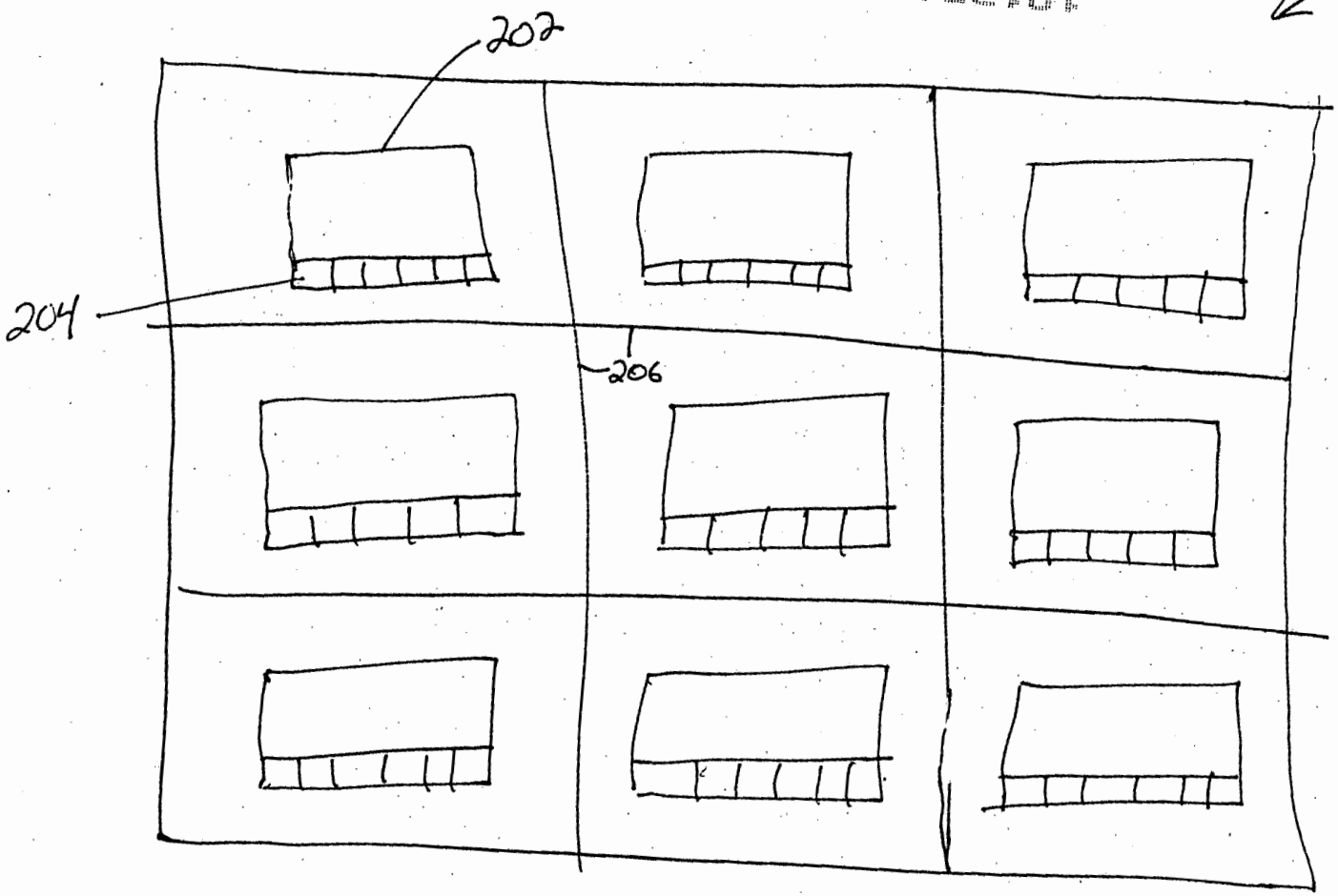
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(PRIOR ART)

FIGURE 1

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(PRIOR ART)

FIGURE 2

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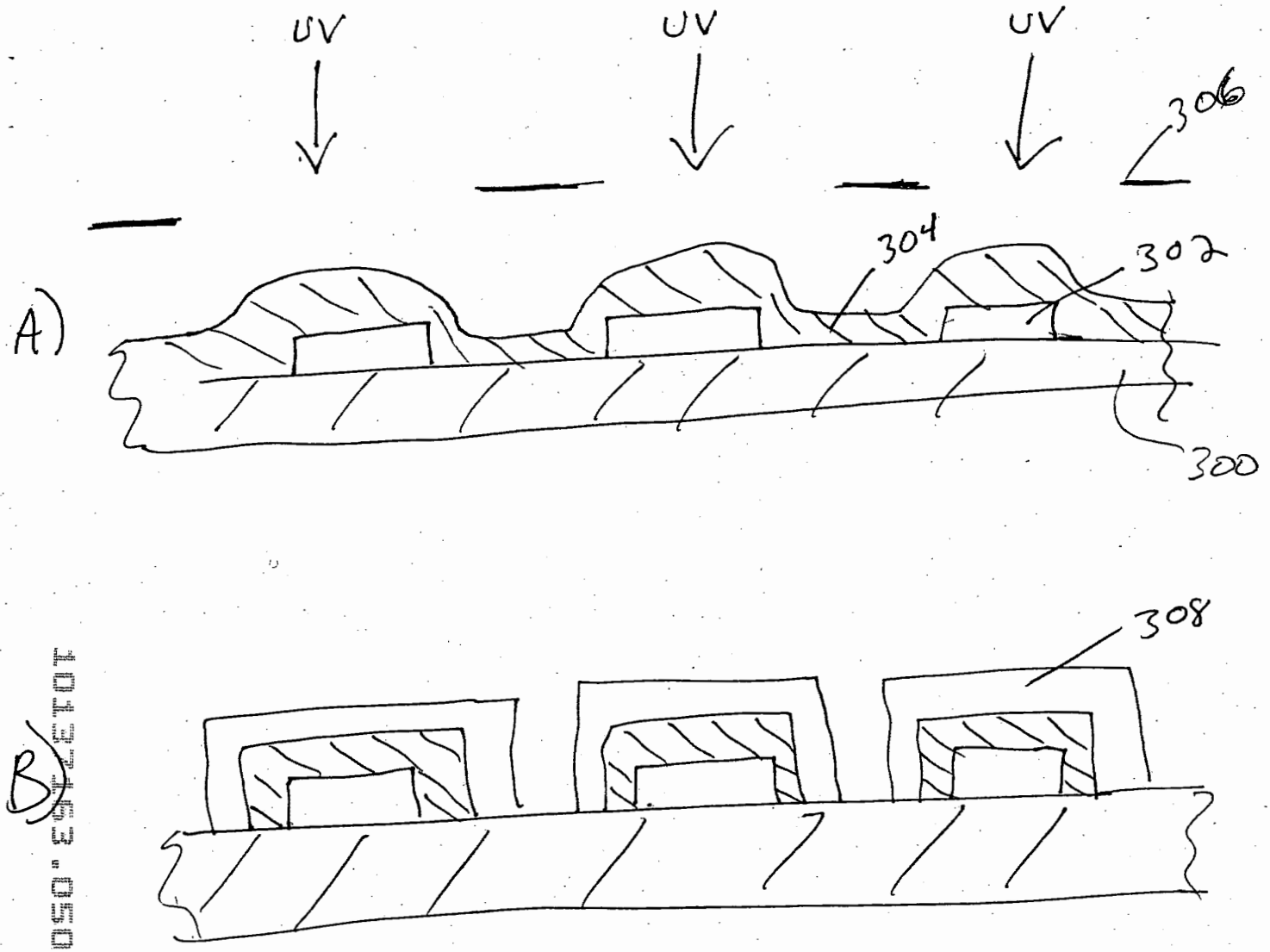


FIGURE 3

20050913.SET.OUT

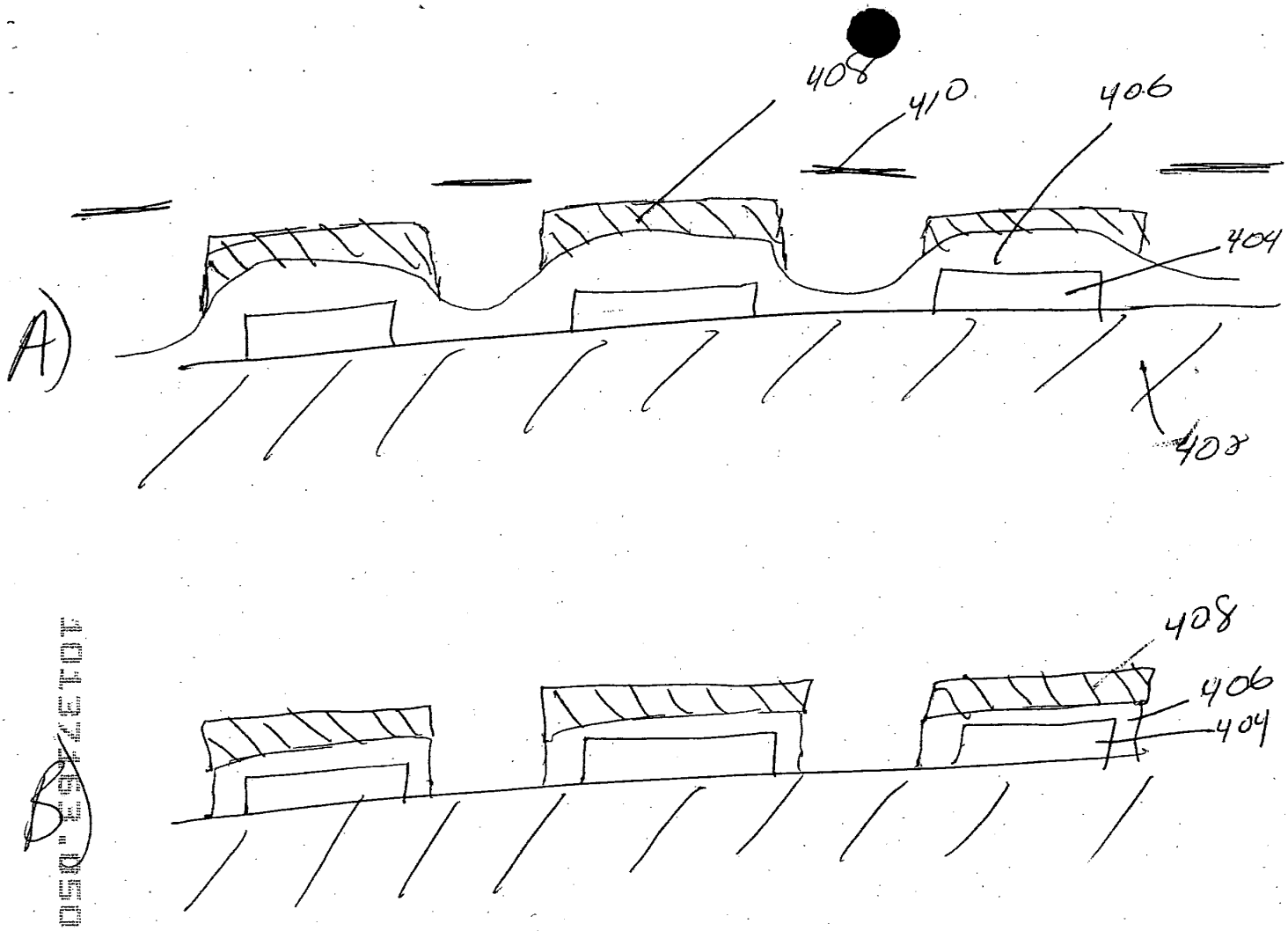


FIGURE 4

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20020504.1634.04

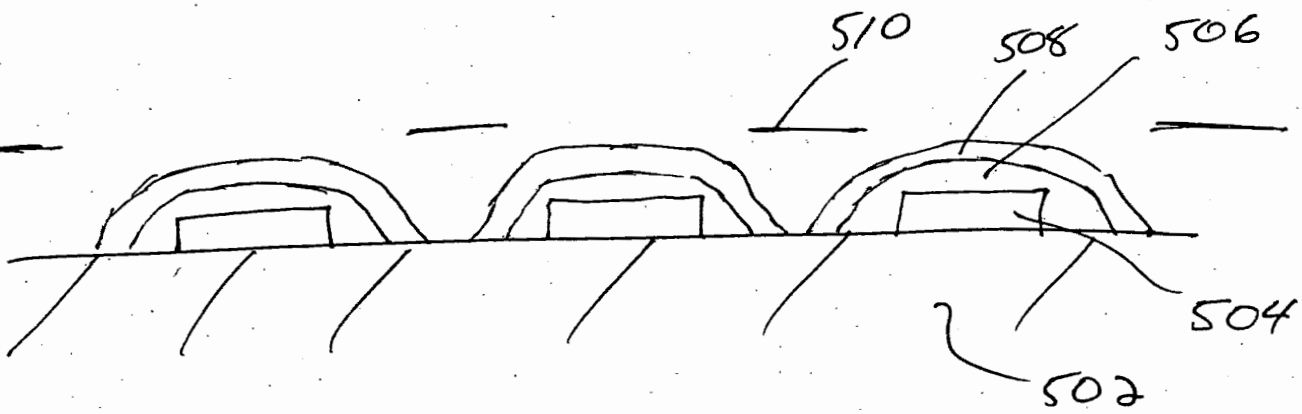


FIGURE 5

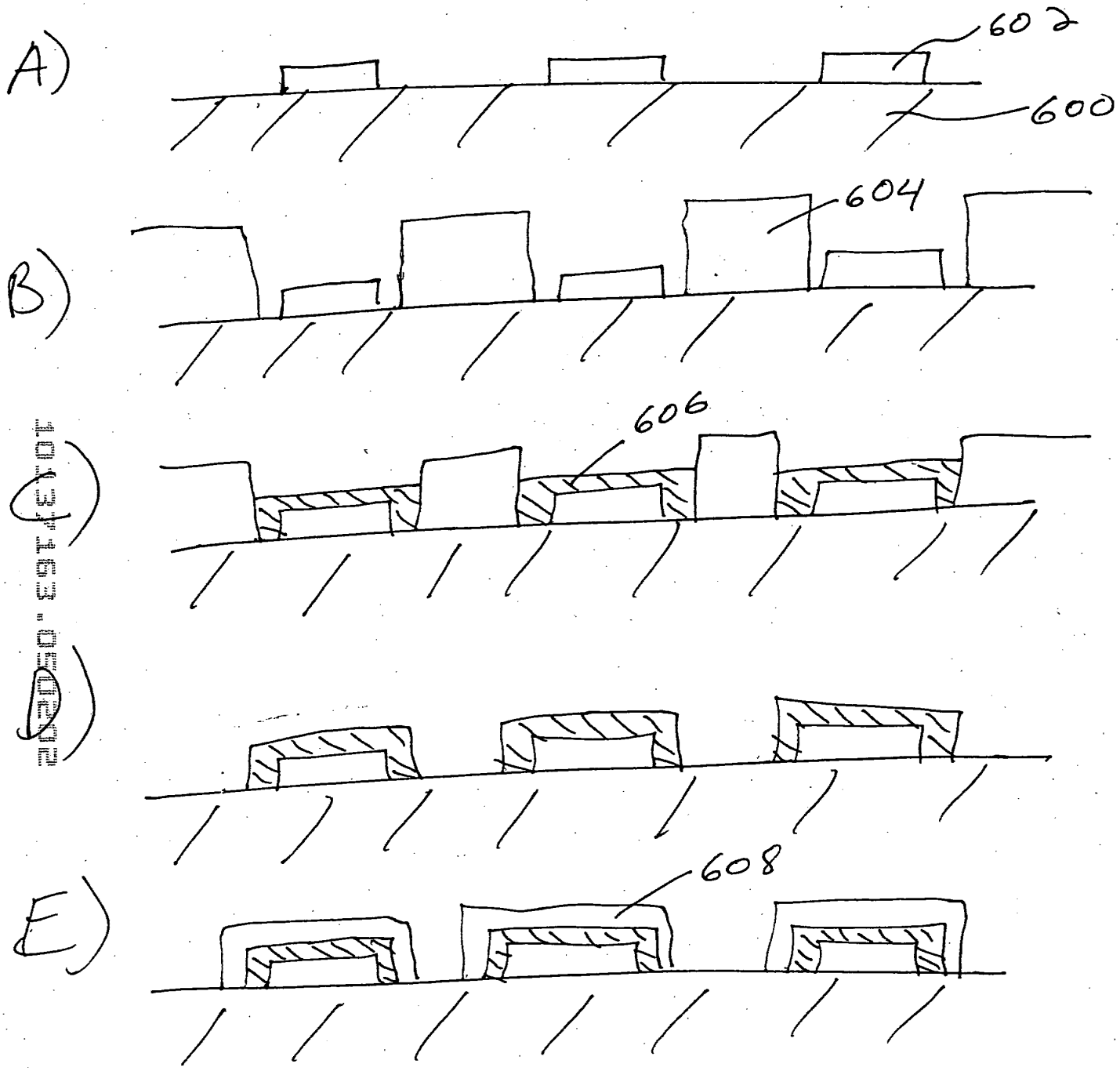


FIGURE 6

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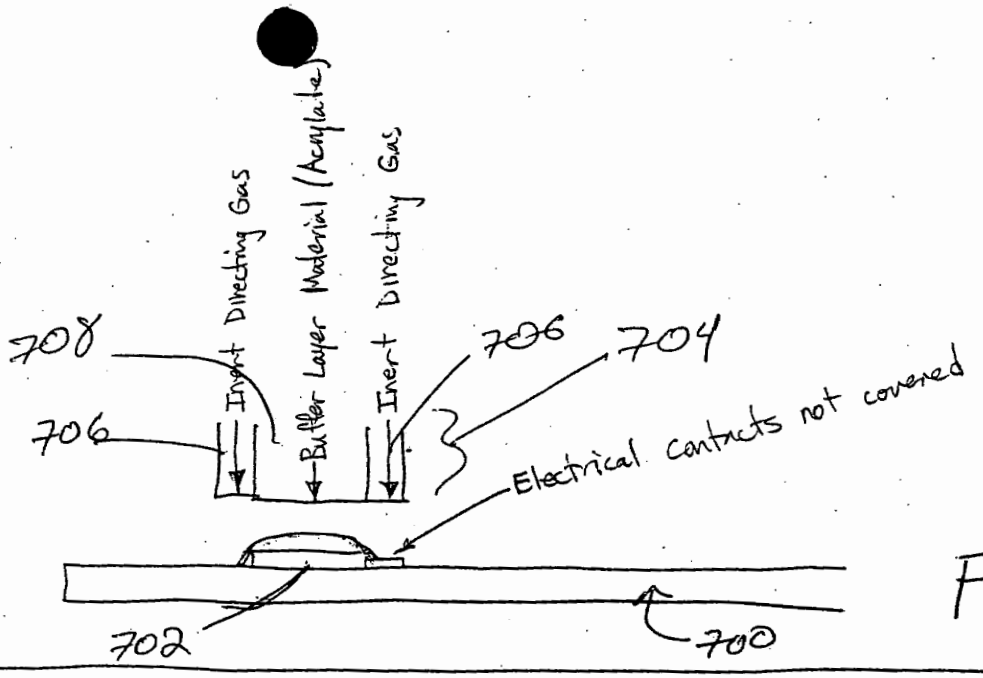


FIG 7A

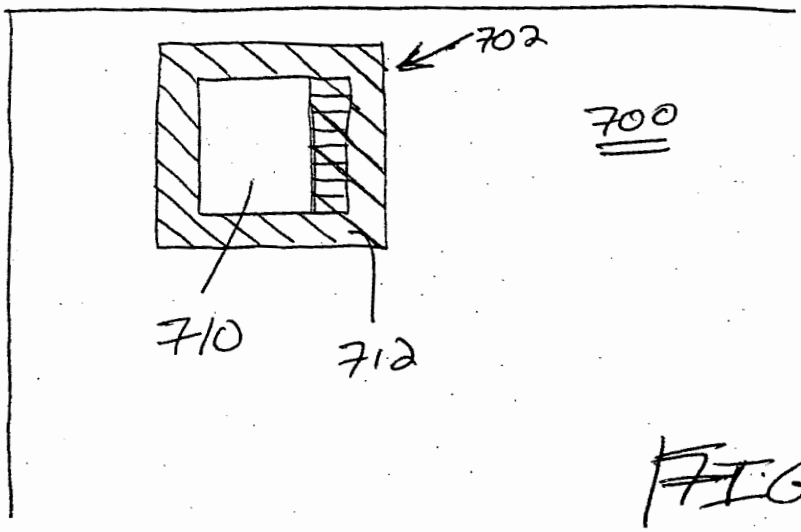


FIG 7B

20220504 EFT/FTOT

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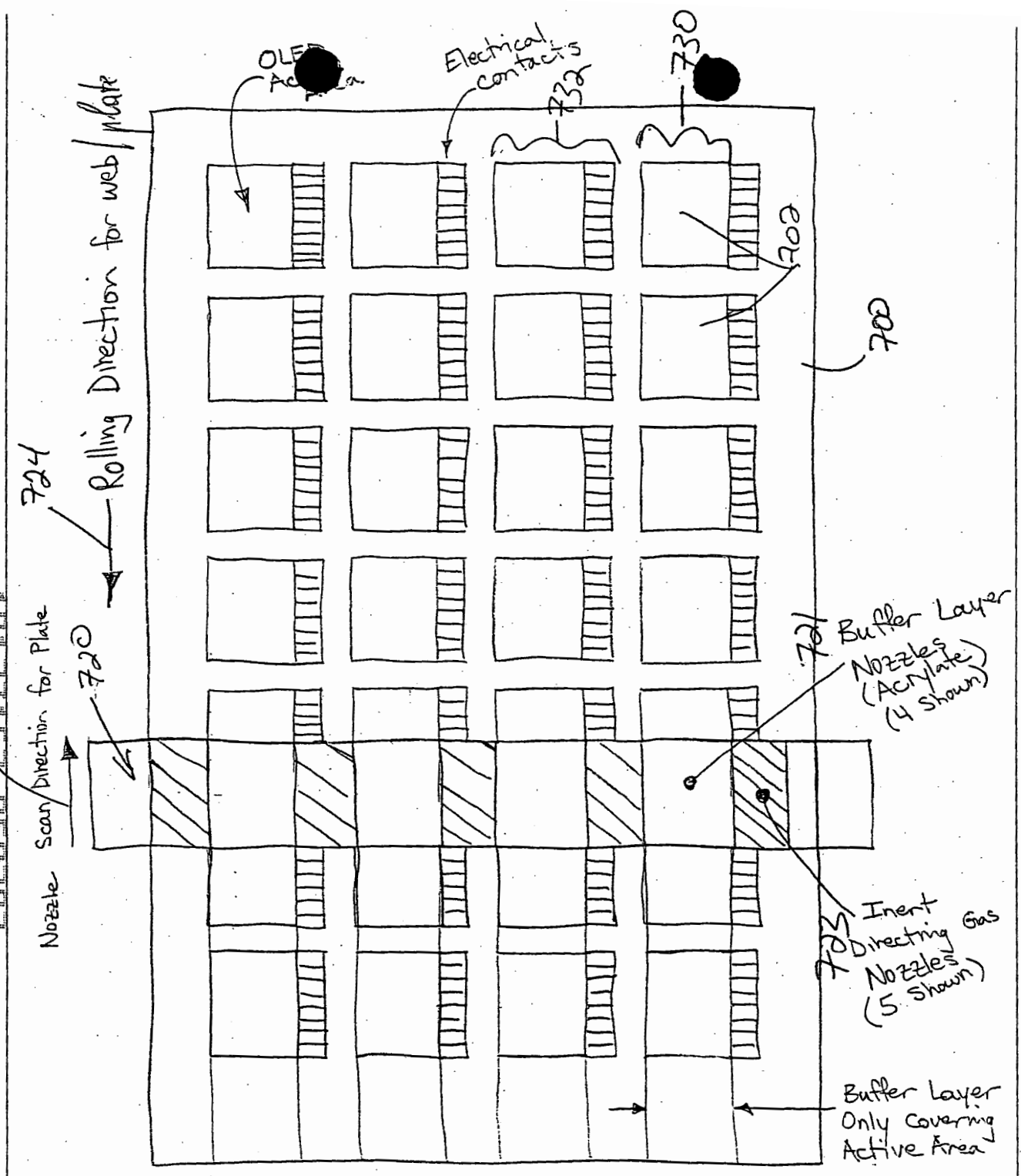

OLED Active Area
Electrical contacts
732
730
700
702
Rolling Direction for web/plate
724
Scan Direction for Plate
720
Nozzle
722
Buffer Layer Nozzles (Acrylate) (4 shown)
704
Inert Gas Directing Nozzles (5 shown)
706
Buffer Layer Only Covering Active Area

Fig 7C

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UNITED STATES PATENT APPLICATION

FOR:

IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

20020503 "0137463"

Inventors:

Karl Pichler
Kyle Frischknecht

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Background of the Invention

One of the last manufacturing steps in the construction of an organic light emitting diode ("OLED") is encapsulation. Encapsulation is a way to protect the OLED device from the damaging environmental effects – primarily from oxygen and moisture. It is well known in the art to encapsulate an OLED device by physically mating a top glass (or other suitable material) layer over, but usually not touching, the OLED device with an epoxy border. The glass, together with its epoxy border, typically is an effective, tried-and-true way to provide the necessary environmental protection required for long-lived OLED usage.

Of late, there has been some discussion in the art to provide a cheaper and better manner of encapsulation, called "direct thin-film" encapsulation. In this manner, thin film encapsulation is typically described as a "polymer multi-layer" (PML) comprising alternating and repeating layers of an organic (usually acrylate or the like) and a barrier layer. **Figure 1** depicts a typical PML structure 100 as is currently known in the art. A glass (or other suitable material) substrate 102 provides the support structure for OLED structure 104 formed on top of substrate 102 in any manner known in the art. Layers 102 and 104 form typically the structure that requires encapsulation – either by known techniques or by the encapsulation techniques of the present invention.

Typically, for PML structures, a planarization layer 106 is formed on top of OLED structure 104. Planarization layer 106 typically is an organic layer (e.g. acrylate or the like) and is provided to give a planar surface for the deposition of the PML structure 112a. PML structure 112a typically comprises barrier layer 108 and another planarization layer 110.

Barrier layer 108 typically comprises a sputtered metal, metal-oxide or a dielectric layer. Barrier layer 108 provides the necessary environmental isolation from the corrosive effects of oxygen and moisture. Planarization layer 110 may again comprise an organic layer (e.g. acrylate or the like) and is typically laid down to provide a planar surface for deposition of the barrier layer 108. This entire PML structure 112a may be repeated (e.g. PML structure 112b) -- possibly several times -- for additional encapsulation of the entire OLED device.

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The advantages of direct thin-film encapsulation over the prior art are primarily cost reduction and improved reliability. Using direct thin-film encapsulation, the package may also be thinner and/or lighter and/or mechanically more flexible. Several structures and steps of the prior art may be excluded with this process. For example, there is no need for a separate glass plate, no need for an epoxy seal, no need for a getter (which is typical in the prior art).

One of the problems of the direct thin film encapsulation occurs with the barrier layer. The barrier layer should ideally not contain any point defects (i.e. pin holes) in its surface --- otherwise its usefulness as a barrier layer is severely compromised. That is primarily the reason that a planar organic layer is typically used as a substrate upon which the barrier layer is deposited.

This problem is exacerbated during the batch fabrication of many OLED devices upon a single large sheet of glass – such as shown as a top view in **Figure 2**. Upon such a single glass sheet 200, several tens (or even hundreds) of OLED devices 202 may be so fabricated. As depicted, OLED devices 202 are typically laid down in rows and columns on a large sheet of glass 200. Typically, each OLED 202 comprises an electrical contact area 204 for electrically mating the OLED device to a driver circuit.

At the thin film encapsulation step, the PML structure is deposited where at least one UV-curable organic liquid material is deposited over the entire glass sheet containing the multiple OLED devices. This organic layer is subsequently cured – followed by a deposition of a barrier layer (e.g. sputtered metal-oxide or dielectric). Such a process may be repeated to form a PML structure – primarily to avoid external particle/dirt-induced pinhole defects. After encapsulation, singulation is performed, for example by forming scribe and break lines 206 upon the entire structure so that individual OLED devices 202 may be separated and further processed.

The problem with this PML technique is that the only part of the device that requires encapsulation is the OLED structure itself – and not, e.g., the electrical contact pads. In fact, the contact pad must typically be exposed for electrical mating with external driver circuitry. So, at a minimum, additional processing must be performed for the removal of the PML structure over these areas.

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Another potential problem with the current PML techniques is that by having the PML layer over the scribe and break lines and/or the glue lines the integrity of the sealed package may be deteriorated, for example by delamination of the PML layer over these areas.

Approaches other than PML are known in the prior art that use combination of organic planarizing layers together with inorganic barrier layers to achieve some degree of thin-film direct encapsulation. Organic planarization layers that do not require special cure may be used as well as layers that are electron-beam or thermally cured, in vacuum or gas atmosphere, preferably inert gas. Such organic layers may also be deposited in non-liquid form, e.g. be evaporated or plasma-deposited (e.g. Parylene).

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Summary of the Invention

In one embodiment, herein is described a method of encapsulating a plurality of OLED devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of OLED devices on a substrate;

depositing at least one planarization layer upon said OLED devices;

hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said OLED device;

removing areas of the at least one planarization layer that are not hardened; and

selectively depositing at least one barrier layer over said hardened region.

In yet another embodiment, herein is described a method of encapsulating a plurality of OLED devices fabricated upon a substrate, the steps of said method comprising

fabricating a plurality of OLED devices on a substrate;

depositing at least one planarization layer upon said OLED devices wherein said planarization layer is deposited as an unpatterned liquid film;

selectively depositing at least one barrier layer over said planarization layer; and

removing said areas of unwanted planarization layer.

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In yet another embodiment, herein is described a method of encapsulating a plurality of OLED devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of OLED devices on a substrate;

selectively depositing at least one planarization layer upon said OLED devices; and

selectively depositing at least one barrier layer over said planarization layer.

In yet another embodiment, herein is described a method of encapsulating a plurality of OLED devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of OLED devices on a substrate;

depositing a mask on top of said substrate, such that mask openings are placed on top of said OLED devices;

depositing at least one planarization layer upon said mask;

removing said mask from said substrate; and

selectively depositing at least one barrier layer over said planarization layer.

PCT/US2004/035202

Brief Description of the Drawings

Figure 1 is side view of a typical PML encapsulation structure formed over an OLED device.

Figure 2 is a top view of an array of mass-produced OLED structures upon a large glass substrate.

Figures 3A and 3B are a set of side view diagrams showing the processing steps of one embodiment of the encapsulation techniques as made in accordance with the principles of the present invention.

Figures 4A and 4B are a set of side view diagrams showing another embodiment of the present invention.

Figure 5 is a side view of yet another embodiment of the present invention.

Figures 6A through 6E are a set of side view diagrams showing still yet another embodiment of the present invention.

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Figures 7A through 7C are a set of diagrams depicting a gas nozzle deposition system made in accordance with the principles of the present invention.

Detailed Description of the Invention

Turning attention to **Figures 3A – 3B**, there is shown a series of side views of OLED devices being encapsulated in accordance with the principles of the present invention. In **Figure 3A**, substrate 300 has formed upon its surface several OLED devices 302. For the purposes of the present invention, this structure is to be construed very broadly. For example, substrate 300 could be comprised of glass (possibly with ITO as a first electrode), quartz, plastic foils, metal, metal foils, silicon wafers or any other potential substrate material that encompasses very broad classes of OLED devices. Broadly, the OLED device could be bottom-emitting or top-emitting. The device could have the bottom electrode as anode or cathode respectively – in either a top or bottom emitting configuration.

Additionally, the encapsulation techniques and structures of the present invention could be used for any number of applications – e.g. active matrix, passive matrix, segmented, alpha-numeric, or backlight OLED displays or any combination thereof. It will be appreciated that any of these OLED devices could be some that have structures patterned on the OLED substrate that are much higher than the OLED stack itself -- e.g. several micron high row separators (e.g. mushrooms) or an ink-confinement well / bank such as used in ink-jet-printed OLEDs. It is intended that the scope of the present invention includes encapsulating over these structures that are within the active areas of the display.

Additionally, it should be appreciated that the scope of the present invention also includes other displays and any electronic or other devices that require encapsulation – e.g. general organic electronic devices such as organic transistors, detectors, solar-cells, etc. (particular OLEDS) and also includes displays for lighting such as OLED-based light sources and backlights.

It should be appreciated that the present invention also comprises a myriad of electronic devices, said devices comprising: a substrate; a plurality of active areas disposed upon said substrate; a plurality of planarization layers disposed on said

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substrate whereby said planarization layer cover substantially only said active areas; and a plurality of barrier layers disposed on said substrate whereby said barrier layers cover substantially only said planarization layers. In particular, the present invention comprises electronic devices such as an OLED, an organic electronic circuit, an organic detector, an organic solar cell.

A UV-curable organic layer 304 is substantially deposited over the entire display glass comprise a plurality of OLED devices. Such suitable organic layer could be a liquid comprising acrylate, together with a photo initiator for selective curing – or other materials such as generally known in the PML and UV or otherwise curable organic planarization layer technology / prior art..

It should be appreciated that layer 304 could also be any suitable planarization layer. For example, an inorganic or hybrid planarization layer might also suffice as a buffer layer that has desirable planarizing and/or protecting properties from the barrier layer deposition process.

Additionally, a wet-processable and post-processing curable organo-metallic compounds such as spin-on glasses might suffice. Such an organic layer might provide a planar structure on which to deposit a barrier layer and to substantially cover point defects (e.g. dirt particles) in lower layers. It is generally desirable that the organic layer be deposited in sufficient quantity so that any such layer is no longer "conformal" to the point defect – i.e. any point defects are not geometrically projected upwards into layers deposited above. Such a first organic layer might also serve to protect the underlying OLED from potential damage due to the deposition of the first barrier layer.

In yet other embodiments, non-PML approaches could be used within the scope and principles of the present invention. For example, a non-liquid evaporated organic – e.g. polysiloxane as might be applied to later Figures.

It will be appreciated that there are many manners of depositing this organic layer upon the OLED device. For example, the layer could be either evaporated or flash evaporated. Alternatively, a liquid organic layer could be spun coated, dip coated, roll coated, spray-coated or blade coated – as is well known in the art. Additionally, other suitable printing technology could be employed, in particular, screen-printing or ink-jet printing.

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Once the organic layer is deposited upon the OLED devices, UV-light is used to selectively cure the layer over the OLED devices to produce the desired cross-linking. This step could be accomplished by a mask 306 which blocks the UV light from areas where it is desired that the organic layer be removed. Alternatively, the cross-linking could be accomplished by using a UV light having an optical patterning system, such as a projection exposure system. In another embodiment, the cross-linking could be accomplished by selectively scanning the UV beam across the plate. In yet another embodiment, the layer need not necessarily have to be UV-cured. Instead, it could be thermally cured -- e.g. using a heat source that has a temperature profile, an IR laser, a stencil/stamp, or e-beam cured. Other methods might include: cross-linking, patterned heat transfer system, patterned IR source, masked IR source, scanned IR source, patterned e-beam, masked e-beam and scanned e-beam.

Once the organic layer has been selectively cross-linked, the remaining uncross-linked layer should be removed. This removal may be accomplished by thermal evaporation (e.g. by heating the substrate) or by using short higher temperature pulses (e.g. placing the OLED plate onto a hotplate). Other removal methods are also possible – e.g. pumping in a vacuum to remove the liquid organic layer. A combination of techniques is also possible – applying thermal energy while pumping in a vacuum.

Still other methods of removal are possible – immersion in a rinse tank, spray-rinsing, ultra-sonicing (either dry or wet), or some combination of techniques (e.g. dry ultra-sonic or mega-sonic in a vacuum). Plasma etching techniques could also be employed to aid the removal process. Additionally, laser-assisted methods such as laser ablation or providing heat via laser might suffice.

Once the residual organic layer has been removed, then a barrier layer is selectively deposited on the OLED plate. **Figure 3B** shows that barrier layer 308 is selectively deposited over the OLED devices where the organic layer has been also deposited. Barrier layer 308 comprises any material that is suitable to protect the OLED device from the environmental effects of oxygen and moisture – and, as such, should be relatively impervious to them. Such barrier layer material might comprise a metal-oxide or a dielectric layer, e.g. SiOx (e.g. SiO2), SiNx (e.g. Si2N3), SiOxNy, AlOx (e.g. Al2O3), AlNx, ITO, ZnOx, Al-doped ZnOx, or any high barrier dielectrics or conductive

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oxides. Generally, any inorganic materials known in the prior art that give good oxygen and water barrier properties would suffice for purposes of the present invention. In the case of a bottom emitting display, the encapsulation does not have to be transparent, then metal or alloy films (e.g. Al or alloys, Cr, Cu or alloys, etc.) or non-transparent or colored dielectric films are potentially suitable, both evaporated or sputtered.

The deposition of the barrier layer can be any suitable method known in the art to deposit dielectric layers, metal-oxides, metals or alloys. For example, sputtering or reactive sputtering (DC, AC, pulsed, or a combination thereof) would suffice. Additionally, evaporation of such dielectrics (resistive heating or electron beam) or metal films is possible. Further, ion-beam assisted or other plasma-enhanced deposition methods are also possible.

It should be appreciated that other embodiments are possible. For example, the patterned UV cure described herein could be done such that the thickness of the planarization layer gradually decreases from the value over the active area to zero or near zero somewhere outside the active area. This may facilitate a nice smooth encapsulation of the OLED (or other structures) plus the planarization layer from the active area out to where there is no encapsulation (e.g. scribe / break line and/or contacts). It might be desirable to have the barrier layer slightly larger in area to cover the planarization layer because the planarization layer might not have such a sharp step and such a barrier layer coverage might provide adequate side step coverage. This embodiment applies also to the embodiments discussed herein, as they may be tuned to provide such a smooth transition of the buffer layer by way of re-flow or evaporation or printing or partial pre-cure and the like of the planarization layer at the edges prior to barrier layer deposition. In yet another embodiment, it might be desirable to encapsulate only the organic light-emissive areas (e.g. pixels) and leave the contact pads, auxiliary encapsulation areas, scribe/break areas free of the organic and barrier layers.

Figures 4A and 4B depict another embodiment of the present invention and particularly a different manner of encapsulating OLED devices. **Figure 4A** shows a step in the processing of present invention in which OLED devices 404 are formed on top of substrate 402. Organic layer 406 is deposited over the entire substrate, covering OLED devices 404. Then, barrier layer 408 is selectively deposited in a manner known in the art

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– e.g. through a mask or screen 410 – situated on top of the OLED devices. **Figure 4B** shows the next step in the processing after that portion of the unwanted organic layer 406 is removed by methods known in the art.

It will be appreciated that organic layer 406 may or may not be cured in its entirety and may or may not be cured selectively through a mask or screen. Likewise, it might be desirable not to cure the organic layer at all. In several embodiments, the organic may be either fully cured before patterned barrier layer deposition, partly cured or completely non-cured and that after the barrier layer deposition, there may be another cure step to ensure that the underlying organic is cured to the intended level, if it wasn't already before the barrier layer deposition. If the unwanted organic layer is etched away (by any number of etching methods known – e.g. chemical (dry or wet) etch, plasma-assisted (with or without oxygen), reactive-ion etching, anisotropic reactive-ion etching, etc.) then barrier layer 408 might act as an effective etch stop as well as laser assisted/based removal (e.g. laser ablation).

In addition, the organic layer could be deposited in any manner previously described (e.g. evaporation of a plurality of reactive organic molecules to form a condensed conformal layer on the substrate) or by well-known Parylene coating methods.

In one embodiment, it may be the case that the edges of the active areas are exposed; however, even if the planarization layer is only a few microns thick and the planarization + barrier layer perimeter around the active device is tens or even over 100 microns wide, then permeation of e.g. water through this thin planarization layer along the 10's or >100 microns should be slow. Alternatively, a second barrier layer may be larger than the area of the planarization layer so that the exposed planarization layer edge is covered with barrier layer also. This could also be achieved by making a potential second planarization layer + barrier layer stack wider than the first and so on. This can naturally already be done in previous embodiments by making the barrier layer mask wider.

Figure 5 depicts another embodiment of encapsulation techniques in accordance with the present invention. In this embodiment, OLED device 504 is again formed upon substrate 502. Organic layer 506 is deposited in a patterned fashion as well as barrier layer 508. As organic layer 506 is deposited selectively; there may be no need to cure the

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layer. It should be appreciated that the cure and patterning aspects could be independent; -- relating to the type of material and deposition technique of for the planarization layer. For example, if UV (or other)-curable liquids such as for PML or screen- or ink-jet print are used, then it is possible to cure. Alternatively, if evaporation of an organic through a mask is the relevant step, there may be no need to cure.

The manner of selectively depositing the organic layer and the barrier layer may be accomplished in a variety of ways. For example, organic layer may be selectively deposited though a shadow mask (as depicted as mask 510) or by ink jet deposition or other screen printing techniques. In fact, generally any printing techniques suitable to deliver the desired planarization layer material can be used. In similar fashion, barrier layer 508 may be selectively deposited. For alternative embodiments, it is possible to employ all options for selective deposition: same mask, different masks and also same mask with different substrate to mask distances (e.g. smaller distance for planarizing layer and then larger distance for barrier such that the barrier coverage is wider – because of slight non-directionality of and differences in the materials deposition).

In the case of printing, screen-printing, ink-jet-printing, the masks can either be not required (ink-jet) or possibly different from that used for a patterned sputter-deposited barrier layer deposition. For other embodiments, it may also be possible to partially cure the planarization layer, deposit the barrier layer and then complete the cure of the planarization layer, if necessary.

Figures 6A through 6E depict yet another embodiment of encapsulation techniques in accordance with the principles of the present invention. First, OLED device 602 is formed on substrate 600. Then, mask 604 is formed onto substrate 600 with mask openings for OLED devices 602.

It will be appreciated that a suitable mask might be formed in many possible manners. For example, such a mask might be a film laminated to the OLED or a mask pressed or pushed or clamped to the OLED. Additionally, such mask might be a multi-use mask or a one-off that then gets removed. Such mask might comprise a metal, ceramic, or plastic foil or sheet; it could also comprise a PTFE (Teflon) or a poly-siloxane type material (e.g. polydimethylsiloxane) or generally any material that does not stick to the OLED (which might cause damage or delamination when the mask is

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removed) and/or a material to which the encapsulation organic does not stick so well so that the mask's removal after encapsulation organic deposition and cure (complete or partial) does not remove the organic.

The mask might be such that it could be brought into contact with the OLED sufficiently well so that the encapsulation organic is confined over the desired areas and does not seep under the areas where the encapsulation organic is not desired (e.g. contact pads). Such a mask might comprise a "stamp" mask. Such a mask could be pressed on, clamped on, or the mask could be made of magnetic material and thus held by magnetic forces (e.g. with sheet magnet behind substrate that 'sucks' the mask to substrate). Additionally, the mask could be multi-use mask or one-off use. Vacuum-suction masks may also suffice. Additionally, a laminated film-mask could also suffice.

Once mask 604 is deposited, organic layer 606 is deposited in any suitable manner. For example, organic layer could be dispensed, squashed, rolled, printed, blade-coated, dropped into, sprayed onto the mask openings. Once deposited, then the organic layer may or may not be cured – either partially or completely prior to the removal of mask 604. The mask could be removed by any means known in the art --e.g. by peeling it off; mechanical removal if a stencil, and the like.

It will be appreciated that the edges of the planarization layer may or may not re-flow such that the subsequently deposited barrier gives better barrier edge coverage.

After the mask is removed, then barrier layer 608 is selectively deposited over the planarization layers covering the OLED devices. Any known technique for such selective deposition is suitable for purposes of the present invention. For various alternative embodiments, it is possible to either fully cure then remove mask; partly cure then remove mask; no cure then remove mask. These variations may also be in combination with potentially another cure after the barrier layer deposition. Specifically, it might be possible to slightly cure then remove mask then e.g. heat to reflow to smoothen the edges – then continue with full cure / barrier layer deposition.

In yet another embodiment, it is also possible to deposit both the planarization and barrier layer(s) before the removal of the mask.

In yet other embodiments, all encapsulation process steps could be accomplished in an inert atmosphere (i.e. with reduced oxygen, ozone, other reactive gases and in

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particular moisture). Alternatively, only the first organic layer and first barrier layer ("dyad") could be done in an inert atmosphere. Alternatively, only the first organic layer could be done in an inert atmosphere.

Other embodiments might include encapsulation with a secondary encapsulation layer for additional protection. This might be accomplished by laminating, glueing or otherwise depositing a plastic, metal, metal plus plastic foil, thin glass, thick glass or metal sheet over said OLED display sheet. Said secondary encapsulation may include a getter material (e.g. zeolite, reactive metal, reactive metal-oxide, metal-sulfide, etc.; in film, powder, paste, tablet, etc. form) in the package to absorb water, oxygen or other reactive gases. Singulation could be accomplished either before or after secondary encapsulation.

Figures 7A through 7C depict a novel gas nozzle deposition system for the deposition of several layers, including the planarization layer. **Figure 7A** shows one gas nozzle 704 as it is depositing a layer onto a device 702 upon a substrate 700. Nozzle 704 comprises at least a nozzle 706 that directs a gas, preferably inert, ~~to the layer being deposited~~ and a nozzle 708 that directs the material to be deposited – e.g. acrylate – onto the device. The gas directs the depositing material away from areas that should be free of deposition. **Figure 7B** shows the device 702 after having been covered with the layer by the gas nozzle system. More precisely, area 710 has been covered with the layer – while area 712 is left free of the deposit. Such an area 712 might represent electrical contacts, scribe lines, or other areas that are desired to be free of such deposit.

Figure 7C depicts the action of an array of such gas nozzles 720 that effects a deposition over a plate 700 of devices 702. Array 720 would comprise a plurality of planarization layer nozzles 721 and inert gas nozzles 723 that are advantageously disposed above the plate of devices so that the layer being deposited is done in only those areas desired. Area 730 is such a desired area for deposition, out of a total area 732 for the device. Array 720 and plate 700 could be placed into relative motion in order to effect an efficient deposition upon a plurality of devices. Direction 722 depicts a possible motion of the array over the plate; while direction 724 depicts a possible motion of the plate under the array – any combination of the two motions are also possible.

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It has now been shown several embodiments of advanced encapsulation techniques performed in accordance with the principles of the present invention. It will be appreciated that the present invention is meant to cover any and all obvious variations as described herein.

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CLAIMS:

1. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices;

hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said device;

removing areas of the at least one planarization layer that are not hardened; and

selectively depositing at least one barrier layer over said hardened region.

2. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises spin coating.

3. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises flash evaporation.

4. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises evaporation.

5. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises blade coating.

6. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises roll coating.

7. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises dip coating.

8. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises spray-coating.

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9. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises one among a group, said group comprising: screen printing and ink jet printing.

10. The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises one of a group, said group comprising flood-exposure of UV light through a mask and scanning a line-source of UV light through a mask.

11. The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises exposure by UV light comprising an optical patterning system.

12. The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises exposure by UV light comprising a UV-beam scanning system.

13. The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer further comprises one of a group, said group comprising: cross-linking, patterned heat transfer system, patterned IR source, masked IR source, scanned IR source, patterned e-beam, masked e-beam and scanned e-beam.

14. The method as recited in Claim 1 wherein the step of removing areas of the at least one organic layer that are not cross-linked comprises removing by thermal evaporation.

15. The method as recited in Claim 14 wherein the step of removing by thermal evaporation further comprises applying a short high temperature pulse.

16. The method as recited in Claim 15 wherein the step of applying a short high temperature pulse further comprises placing the OLED plate onto a hotplate.

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SDC EX. 1002 - 62/544

17. The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises removing by pumping in a vacuum.

18. The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises removing by thermal evaporation and pumping in a vacuum.

19. The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises one of a group, said group comprising: washing, blowing away, rinsing, sonicing, and plasma.

20. The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises a barrier layer comprising one of a group, said group comprising a dielectric, a metal, a metal-oxide and an alloy.

21. The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing said barrier layer through a mask.

22. The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing the barrier layer in a larger area than the planarization layer.

23. The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing one of a group, said group comprising: metal-oxide, dielectric layer, SiOx, SiNx , SiOxNy, AlOx, AlNx, ITO, ZnOx, Al-doped ZnOx, metal film, and alloy film.

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24. The method as recited in Claim 1 wherein substantially only the light emissive areas are covered by the planarization layer and the barrier layer.

25. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices wherein said planarization layer is deposited as an unpatterned liquid film;

selectively depositing at least one barrier layer over said planarization layer; and

removing said areas of unwanted planarization layer.

26. The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises curing an organic layer selectively over the substrate.

27. The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises curing an organic layer over the entire substrate.

28. The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises evaporating a plurality of reactive organic molecules, said reactive organic molecules comprising a condensed conformal film on the substrate.

29. The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises one of a group, said group comprising a Parylene coating of said organic layer over the substrate, and a plasma-assisted organic material deposition.

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30. The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises etching an organic layer.

31. The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises etching an organic layer with a chemical etch process.

32. The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises one of a group, said group comprising etching an organic layer with a plasma-assisted etching process, oxygen plasma, reactive ion-etch, anisotropic etch, laser assisted/based removal and laser ablation.

33. The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises removing said organic layer.

34. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

selectively depositing at least one planarization layer upon said devices; and

selectively depositing at least one barrier layer over said planarization layer.

35. The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by ink jet of an organic layer.

36. The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by one of a group, said group comprising: screen printing of an organic layer and depositing by gas nozzle.

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37. The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing an organic layer through a shadow mask .

38. The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by ink jet of said barrier layer.

39. The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by screen printing of said barrier layer.

40. The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises one of a group, said group comprising: depositing by shadow mask, sputtering, ink jet deposition, screen printing and evaporation.

41. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing a mask on top of said substrate, such that mask openings are placed on top of said devices;

depositing at least one planarization layer upon said mask;

removing said mask from said substrate; and

selectively depositing at least one barrier layer over said planarization layer.

42. The method as recited in Claim 41 wherein the step of depositing said mask further comprises one of group, said group comprising: depositing a stamp mask, depositing a laminated film-mask, depositing a vacuum mask, magnetically held mask.

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43. The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing said mask such that said mask is in contact with said substrate.

44. The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising a material substantially non-sticking to OLED substrate over the areas in between the active areas.

45. The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising one of a group, said group comprising a metal, a ceramic, a plastic, a polymer, PTFE, and poly-siloxane.

46. The method as recited in Claim 41 wherein the step of depositing at least one planarization layer further comprises depositing an organic layer over the entire mask.

47. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices; and

depositing at least one barrier layer over planarization layer wherein at least one said step is accomplished in an inert atmosphere.

48. The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is the step of depositing at least one planarization layer.

49. The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is the step of depositing at least one barrier layer.

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50. The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is both the step of depositing at least one planarization layer and the step of depositing at least one barrier layer.

51. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices;

depositing at least one barrier layer over planarization layer; and

depositing a secondary encapsulation layer over said barrier layer.

52. The method as recited in Claim 51 wherein the step of depositing a secondary encapsulation layer further comprises depositing one of a group, said group comprising: a plastic, a metal, a metal plus plastic foil, a polymer, and glass.

53. The method as recited in Claim 51 wherein the step of depositing a secondary encapsulation layer further comprises singulating the devices before the deposition of said secondary encapuslation.

54. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices; and

depositing at least one barrier layer over planarization layer wherein at least one said deposition step is accomplished by gas nozzle deposition.

55. The method as recited in Claim 54 wherein one said deposition step is accomplished by gas nozzle deposition further comprises depositing a layer over a plurality of devices with an array of nozzles positioned above said substrate.

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56. The method as recited in Claim 55 wherein the step of depositing a layer over a plurality of devices further comprises moving said array and said substrate in relative motion.

57. An electronic device, said device comprising:

a substrate;

a plurality of active areas disposed upon said substrate;

a plurality of planarization layers disposed on said substrate whereby said planarization layer cover substantially only said active areas; and

a plurality of barrier layers disposed on said substrate whereby said barrier layers cover substantially only said planarization layers.

58. The electronic device as recited in Claim 57 wherein said electronic device is one of a group, said group comprising an OLED, an organic electronic circuit, an organic detector, an organic solar cell.

Attorney Docket No. 20050202

SDC EX. 1002 - 69/544

ABSTRACT

A method of encapsulating a plurality of OLED devices fabricated upon a substrate is described, the steps of said method comprising: fabricating a plurality of OLED devices on a substrate; depositing at least one planarization layer upon said OLED devices; hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said OLED device; removing areas of the at least one planarization layer that are not hardened; and selectively depositing at least one barrier layer over said hardened region.

Express Mail No. EV 325 705 025 US

SDC EX. 1002 - 70/544

DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:
IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

the specification of which (check one)
__is attached hereto.
___ was filed on as Application Serial No.
and was amended on _____ (if applicable)

List of Inventors: Karl Pichler AND Kyle D. Firschknecht

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Codes, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			Priority claimed	
(Number)	(Country)	(Day/month/year filed)	Yes	No
(Number)	(Country)	(Day/month/year filed)	Yes	No

application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

EV 340754505 US

(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)
(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application listed below:

(Application Serial No.)	(Filing date)	(Status)

Power of Attorney: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

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Elsa Keller
Legal Administrator (908) 321-3026

I hereby declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

10/745,950 - 05/20/2005

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Inventor's signature:	
Date:	
Residence:	Livermore, CA
Citizenship:	USA
Post Office Address:	566 Shelley Street, Livermore, CA 94550

PATENT - 05/05/2005

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

05/06/2002 GWORDOF1 00000007 192179 10137163

01 FC:101 740.00 CH
02 FC:102 420.00 CH
03 FC:103 684.00 CH

PTO-1556
(5/87)

*U.S. Government Printing Office: 2001 — 481-697/59173

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number: 10137163

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	58	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	58 minus 20=	* 38
INDEPENDENT CLAIMS	8 minus 3 =	* 5
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ OR OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	684
X42=		OR	X84=	420
+140=		OR	+280=	
TOTAL		OR	TOTAL	1844

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY OR OTHER THAN SMALL ENTITY

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

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AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If th "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If th "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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CLAIMS ONLY

SERIAL NO. 10137163 | FILING DATE 05-06-02

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1	1					
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TOTAL IND.	8	⇩		⇩		⇩
TOTAL DEP.	50					
TOTAL CLAIMS	58					

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	IND.	DEP.	IND.	DEP.	IND.	DEP.
51	1					
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TOTAL DEP.						
TOTAL CLAIMS						

* *MAY BE USED FOR ADDITIONAL CLAIMS OR ADMENDMENTS*

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L Number	Hits	Search Text	DB	Time stamp
1	107	(light adj emitting adj diodes) same (encapsulation or encapsulating)	USPAT; US-PGPUB	2003/06/07 16:04
2	64	((light adj emitting adj diodes) same (encapsulation or encapsulating)) and plurality and @ad<=20020502	USPAT; US-PGPUB	2003/06/07 16:05
3	554	(led or oled) same (encapsulation or encapsulating)	USPAT; US-PGPUB	2003/06/07 15:57
4	274	((led or oled) same (encapsulation or encapsulating)) and plurality and @ad<=20020502	USPAT; US-PGPUB	2003/06/07 15:57
5	258	(((led or oled) same (encapsulation or encapsulating)) and plurality and @ad<=20020502) not (((light adj emitting adj diodes) same (encapsulation or encapsulating)) and plurality and @ad<=20020502)	USPAT; US-PGPUB	2003/06/07 15:49
8	2	((led or oled) same (encapsulation or encapsulating)) and plurality	EPO; JPO; DERWENT; IBM_TDB	2003/06/07 15:58
6	142	(led or oled) same (encapsulation or encapsulating)	EPO; JPO; DERWENT; IBM_TDB	2003/06/07 16:03
9	25	((light adj emitting adj diodes) same (encapsulation or encapsulating)) and (harden or hardening or uv)	USPAT; US-PGPUB	2003/06/07 16:07
11	24	(((light adj emitting adj diodes) same (encapsulation or encapsulating)) and (harden or hardening or uv)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/07 16:05
12	321	(light adj emitting adj diodes) and (encapsulation or encapsulating) and (harden or hardening or uv)	USPAT; US-PGPUB	2003/06/07 16:08
13	297	((light adj emitting adj diodes) and (encapsulation or encapsulating) and (harden or hardening or uv)) not ((((light adj emitting adj diodes) same (encapsulation or encapsulating)) and (harden or hardening or uv)) and @ad<=20020502)	USPAT; US-PGPUB	2003/06/07 16:08
14	258	(((light adj emitting adj diodes) and (encapsulation or encapsulating) and (harden or hardening or uv)) not ((((light adj emitting adj diodes) same (encapsulation or encapsulating)) and (harden or hardening or uv)) and @ad<=20020502)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/07 16:09
16	193	((((light adj emitting adj diodes) and (encapsulation or encapsulating) and (harden or hardening or uv)) not ((((light adj emitting adj diodes) same (encapsulation or encapsulating)) and (harden or hardening or uv)) and @ad<=20020502)) and @ad<=20020502) and plurality	USPAT; US-PGPUB	2003/06/07 16:10

L=5

	U	1 [1]	Document ID	Issu Date	Pages	Title	Curr nt OR
1	☐	☒	US 20030094691 A1	20030522	12	ENCAPSULATION OF ELECTRONIC DEVICES	257/704
2	☐	☒	US 20030062527 A1	20030403	10	Barrier stack	257/79
3	☐	☒	US 20030062186 A1	20030403	19	Sealing structure for highly moisture-sensitive electronic device element and method for fabrication	174/52.2
4	☐	☒	US 20020003403 A1	20020110	11	Thin film encapsulation of organic light emitting diode devices	313/512
5	☐	☒	US 6410942 B1	20020625	17	Enhanced light extraction through the use of micro-LED arrays	257/88

	Current XR f	Retrieval Classif	Inv ntor	S	C	P	2	3	4	5
1	257/710		Auch, Mark et al.	☒	☐	☐	☐	☐	☐	☐
2			Kumar, Senthil et al.	☒	☐	☐	☐	☐	☐	☐
3	174/52.3		Boroson, Michael L. et al.	☒	☐	☐	☐	☐	☐	☐
4	257/E51.02		Ghosh, Amalkumar P. et al.	☒	☐	☐	☐	☐	☐	☐
5	257/91; 257/93; 257/98; 257/E25.02; 257/E33.012; 257/E33.068		Thibeault, Brian et al.	☒	☐	☐	☐	☐	☐	☐

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	U	1 [1]	Document ID	Issu Date	Pages	Titl	Current OR
1	☐	☒	WO 3005774 A1	20030116	20	CONTAINER FOR ENCAPSULATING OLED AND MANUFACTURING METHOD THEREOF	
2	☐	☒	WO 2071506 A1	20020912	31	THIN FILM ENCAPSULATION OF ORGANIC LIGHT EMITTING DIODE DEVICES	
3	☐	☒	US 20010052752 A	20011101	11	Organic light emitting diode display device has encapsulation assembly having first encapsulation layer of dielectric oxide in direct contact with substrate, and second encapsulation layer covering first encapsulation layer	

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1	257/E51.02		HUH, JIN WOO et al.	☒	☐	☐	☐	☐	☐	☐
2	257/E51.02		GHOSH, AMALKUJAR P et al.	☒	☐	☐	☐	☐	☐	☐
3			GHOSH, A P et al.	☒	☐	☐	☐	☐	☐	☐

L=16

	U	1 [1]	Document ID	Issu Date	Pages	Title	Current OR
1	☐	☒	US 6410942 B1	20020625	17	Enhanced light extraction through the use of micro-LED arrays	257/88
2	☐	☒	US 6146715 A	20001114	25	Method of fabricating organic electroluminescent display panel	427/555

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1	257/91; 257/93; 257/98; 257/E25.02; 257/E33.012; 257/E33.068		Thibeault, Brian et al.	☒	☐	☐	☐	☐	☐	☐
2	216/17; 216/18; 216/94; 257/E27.119; 427/556; 427/64; 427/68; 430/293; 430/317; 430/319		Kim, Chang Nam et al.	☒	☐	☐	☐	☐	☐	☐

#2

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UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/137,163	05/02/2002	Karl Pichler	2002P03156US

CONFIRMATION NO. 1705

Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

FORMALITIES LETTER

OC000000008284291

Date Mailed: 06/13/2002

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(l) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Substitute drawings in compliance with 37 CFR 1.84 because:
    - drawing sheets do not have the appropriate margin(s) (see 37 CFR 1.84(g)). Each sheet must include a top margin of at least 2.5 cm. (1 inch), a left side margin of at least 2.5 cm. (1 inch), a right side margin of at least 1.5 cm. (5/8 inch), and a bottom margin of at least 1.0 cm. (3/8 inch);

Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$130** for a Large Entity

- **$130** Late oath or declaration Surcharge.

A copy of this notice <u>MUST</u> be returned with the reply.

Tsehaie H

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US-PAT-NO: 6498114

DOCUMENT-IDENTIFIER: US 6498114 B1

TITLE: Method for forming a patterned semiconductor film

2, 4, 6, 7, 8

---------- KWIC ---------

Brief Summary Text - BSTX (5):
Organic semiconductor materials or dispersions of inorganic semiconducting particles lend themselves to relatively simple and inexpensive deposition methods. Possible methods include thermal **evaporation** in a vacuum chamber or wet processing such as **spin** coating using an appropriate solvent or by other coating techniques known to yield thin films.

Detailed Description Text - DETX (14):
Gross changes in portions of the organic semiconductor 20 can be caused by other materials as the destructive agent 100. For example, chemical reactions through use of, for example, an oxidizing agent can cause portions of the organic semiconductor film 20 to convert to an insulator. Other destructive agents, for example electromagnetic radiation such as **UV** applied through a contact mask and e-beam applied without a mask, can convert exposed portions of the organic semiconductor film 20 into insulator.

Detailed Description Text - DETX (30):
The mask in some embodiments is formed through use of a solvent-based polymer. The solvent-based polymer can be deposited, for example, by a printing process followed by **evaporation** of the solvent.

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In another embodiment, a polymer is deposited and then cured to form the mask 70'.

Detailed Description Text - DETX (34):

In a preferred embodiment, an encapsulated electrophoretic display assembly is manufactured with use of printing or coating steps on a wide variety of flexible substrates. As used herein, the term "printing" includes all forms of printing and coating, including, but not limited to, pre-metered coatings such as patch die coating, slot or extrusion coating, slide or cascade coating, and curtain coating; **roll** coating such as knife over **roll** coating, forward and reverse **roll** coating, gravure coating, **dip** coating, **spray** coating, meniscus coating, **spin** coating, brush coating, air knife coating, silk screen printing processes, electrostatic printing processes, thermal printing processes, ink jet printing processes and other similar techniques. Thus, the resulting display can be flexible. Further, because the display medium can be printed (using a variety of methods), the display itself can be made inexpensively.

Detailed Description Text - DETX (55):

Chemical processes such as dispersion polymerization, mini- or micro-emulsion polymerization, suspension polymerization precipitation, phase separation, solvent **evaporation,** in situ polymerization, seeded emulsion polymerization, or any process which falls under the general category of microencapsulation may be used. A typical process of this type is a phase separation process wherein a dissolved polymeric material is precipitated out of solution onto a dispersed pigment surface through solvent dilution, **evaporation,** or a thermal change. Other processes include

chemical means for staining polymeric latices, for example with metal oxides or dyes.

Detailed Description Text - DETX (61):
The fluid must be capable of being formed into small droplets prior to a capsule being formed. Processes for forming small droplets include flow-through jets, membranes, nozzles, or orifices, as well as shear-based emulsifying schemes. The formation of small drops may be assisted by electrical or sonic fields. Surfactants and polymers can be used to aid in the stabilization and emulsification of the droplets in the case of an emulsion type **encapsulation**. A preferred surfactant for use in displays of the invention is sodium dodecylsulfate.

Detailed Description Text - DETX (73):
D. **Encapsulation**

Detailed Description Text - DETX (74):
There is a long and rich history to **encapsulation**, with numerous processes and polymers having proven useful in creating capsules. **Encapsulation** of the internal phase may be accomplished in a number of different ways. Numerous suitable procedures for microencapsulation are detailed in both Microencapsulation, Processes and Applications, (I. E. Vandegaer, ed.), Plenum Press, New York, N.Y. (1974) and Gutcho, Microcapsules and Mircroencapsulation Techniques, Nuyes Data Corp., Park Ridge, N.J. (1976). The processes fall into several general categories, all of which can be applied to the present invention: interfacial polymerization, in situ polymerization, physical processes, such as coextrusion and other phase separation processes, in-liquid

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curing, and simple/complex coacervation.

Detailed Description Text - DETX (77):
In the context of the present invention, one skilled in the art will select an **encapsulation** procedure and wall material based on the desired capsule properties. These properties include the distribution of capsule radii; electrical, mechanical, diffusion, and optical properties of the capsule wall; and chemical compatibility with the internal phase of the capsule.

Detailed Description Text - DETX (78):
The capsule wall generally has a high electrical resistivity. Although it is possible to use walls with relatively low resistivities, this may limit performance in requiring relatively higher addressing voltages. The capsule wall should also be mechanically strong (although if the finished capsule powder is to be dispersed in a curable polymeric binder for coating, mechanical strength is not as critical). The capsule wall should generally not be porous. If, however, it is desired to use an **encapsulation** procedure that produces porous capsules, these can be overcoated in a post-processing step (i.e., a second **encapsulation**). Moreover, if the capsules are to be dispersed in a curable binder, the binder will serve to close the pores. The capsule walls should be optically clear. The wall material may, however, be chosen to match the refractive index of the internal phase of the capsule (i.e., the suspending fluid) or a binder in which the capsules are to be dispersed. For some applications (e.g., interposition between two fixed electrodes), monodispersed capsule radii are desirable.

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Detailed Description Text - DETX (79):

An **encapsulation** procedure involves a polymerization between urea and formaldehyde in an aqueous phase of an oil/water emulsion in the presence of a negatively charged, carboxyl-substituted, linear hydrocarbon polyelectrolyte material. The resulting capsule wall is a urea/formaldehyde copolymer, which discretely encloses the internal phase. The capsule is clear, mechanically strong, and has good resistivity properties.

Detailed Description Text - DETX (84):

Surface tension modifiers can be added to adjust the air/ink interfacial tension. Polysiloxanes are typically used in such an application to improve surface leveling while minimizing other defects within the coating. Surface tension modifiers include, but are not limited to, fluorinated surfactants, such as, for example, the Zonyl.RTM. series from DuPont (Wilmington, Del.), the Fluorod.RTM. series from 3M (St. Paul, Minn.), and the fluoroakyl series from Autochem (Glen Rock, N.J.); siloxanes, such as, for example, Silwet.RTM. from Union Carbide (Danbury, Conn.); and polyethoxy and polypropoxy alcohols. Antifoams, such as silicone and silicone-free polymeric materials, may be added to enhance the movement of air from within the ink to the surface and to facilitate the rupture of bubbles at the coating surface. Other useful antifoams include, but are not limited to, glyceryl esters, polyhydric alcohols, compounded antifoams, such as oil solutions of alkyl benzenes, natural fats, fatty acids, and metallic soaps, and silicone antifoaming agents made from the combination of dimethyl siloxane polymers and silica. Stabilizers such as **uv**-absorbers and antioxidants may also be added to improve the lifetime of the ink.

Detailed Description Text - DETX (85):
Other additives to control properties like coating viscosity and foaming can also be used in the coating fluid. Stabilizers (**UV**-absorbers, antioxidants) and other additives which could prove useful in practical materials.

Detailed Description Text - DETX (91):
The thermoset systems are exemplified by the family of epoxies. These binary systems can vary greatly in viscosity, and the reactivity of the pair determines the "pot life" of the mixture. If the pot life is long enough to allow a coating operation, capsules may be coated in an ordered arrangement in a coating process prior to the resin curing and **hardening**.

L Number	Hits	Search Text	DB	Time stamp
1	23	(encapsulation or encapsulating) same (planarization or planarizing) same (spin or flash or evaporation or roll or blade or dip or spray)	USPAT; US-PGPUB	2003/06/09 10:40
2	2	((encapsulation or encapsulating) same (planarization or planarizing) same (spin or flash or evaporation or roll or blade or dip or spray)) and hardening	USPAT; US-PGPUB	2003/06/09 10:40
3	139	(encapsulation or encapsulating) and ((planarization or planarizing) same (spin or flash or evaporation or roll or blade or dip or spray))	USPAT; US-PGPUB	2003/06/09 10:41
4	10	((encapsulation or encapsulating) and ((planarization or planarizing) same (spin or flash or evaporation or roll or blade or dip or spray))) and hardening	USPAT; US-PGPUB	2003/06/09 10:42
5	8	(((encapsulation or encapsulating) and ((planarization or planarizing) same (spin or flash or evaporation or roll or blade or dip or spray))) and hardening) not (((encapsulation or encapsulating) same (planarization or planarizing) same (spin or flash or evaporation or roll or blade or dip or spray)) and hardening)	USPAT; US-PGPUB	2003/06/09 10:40
6	28806	(encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)	USPAT; US-PGPUB	2003/06/09 11:36
7	1913	((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening	USPAT; US-PGPUB	2003/06/09 11:13
8	925	(((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and plurality	USPAT; US-PGPUB	2003/06/09 11:02
9	239	((((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and plurality) and uv	USPAT; US-PGPUB	2003/06/09 10:43
10	221	(((((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and plurality) and uv) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 11:03
11	199	(((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and (plurality with (device or elements))	USPAT; US-PGPUB	2003/06/09 11:03
12	193	((((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and (plurality with (device or elements))) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 11:41
13	151	(((((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and (plurality with (device or elements))) and @ad<=20020502) not ((((((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and plurality) and uv) and @ad<=20020502)	USPAT; US-PGPUB	2003/06/09 11:04
14	855	(encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)	EPO; JPO; DERWENT; IBM_TDB	2003/06/09 11:13
15	14	((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening	EPO; JPO; DERWENT; IBM_TDB	2003/06/09 11:13
16	621	(hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))	USPAT; US-PGPUB	2003/06/09 11:40

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17	347	((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and (removing or etching)	USPAT; US-PGPUB	2003/06/09 11:51
18	72	((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and ((removing or etching) with (hardening or hardened))	USPAT; US-PGPUB	2003/06/09 11:41
19	61	(((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and ((removing or etching) with (hardening or hardened))) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 11:46
20	10	((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and ((removing or etching) with (hardening or hardened))) and @ad<=20020502) and barrier	USPAT; US-PGPUB	2003/06/09 11:46
21	312	(((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and (removing or etching)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 11:54
22	59	((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and (removing or etching)) and @ad<=20020502) and barrier	USPAT; US-PGPUB	2003/06/09 11:46
23	49	(((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and (removing or etching)) and @ad<=20020502) and barrier) not (((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and ((removing or etching) with (hardening or hardened))) and @ad<=20020502) and barrier)	USPAT; US-PGPUB	2003/06/09 11:46
24	197	438/106-110,124,126,127.ccls. and hardening and (removing or etching)	USPAT; US-PGPUB	2003/06/09 12:14
25	160	(438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality	USPAT; US-PGPUB	2003/06/09 11:57
26	147	((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 11:57
27	31	(((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier	USPAT; US-PGPUB	2003/06/09 11:57
28	678	438/106-110,124,126,127.ccls. and harden$3	USPAT; US-PGPUB	2003/06/09 12:14
29	527	(438/106-110,124,126,127.ccls. and harden$3) and plurality	USPAT; US-PGPUB	2003/06/09 11:57
30	87	((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier	USPAT; US-PGPUB	2003/06/09 12:03
31	82	(((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 15:32
32	51	((((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier) and @ad<=20020502) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier)	USPAT; US-PGPUB	2003/06/09 11:57
33	21	((438/106-110,124,126,127.ccls. and harden$3) and plurality) and ((removing or etching) with (hardened or unwanted))	USPAT; US-PGPUB	2003/06/09 13:50

34	420	(438/106-110,124,126,127.ccls. and harden$3) and (removing or etching)	USPAT; US-PGPUB	2003/06/09 12:15
35	387	((438/106-110,124,126,127.ccls. and harden$3) and (removing or etching)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 13:50
36	358	(((438/106-110,124,126,127.ccls. and harden$3) and (removing or etching)) and @ad<=20020502) not (((((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier) and @ad<=20020502) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier))	USPAT; US-PGPUB	2003/06/09 12:16
37	327	((((438/106-110,124,126,127.ccls. and harden$3) and (removing or etching)) and @ad<=20020502) not (((((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier) and @ad<=20020502) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier))) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier)	USPAT; US-PGPUB	2003/06/09 12:16
38	327	(((((438/106-110,124,126,127.ccls. and harden$3) and (removing or etching)) and @ad<=20020502) not (((((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier) and @ad<=20020502) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier))) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier)) not ((((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and (removing or etching)) and @ad<=20020502) and barrier) not (((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and ((removing or etching) with (hardening or hardened))) and @ad<=20020502) and barrier))	USPAT; US-PGPUB	2003/06/09 12:17

39	321	((((((438/106-110,124,126,127.ccls. and harden$3) and (removing or etching)) and @ad<=20020502) not (((((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier) and @ad<=20020502) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier))) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier)) not ((((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and (removing or etching)) and @ad<=20020502) and barrier) not (((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and ((removing or etching) with (hardening or hardened))) and @ad<=20020502) and barrier))) not ((((((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and (plurality with (device or elements))) and @ad<=20020502) not ((((((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and plurality) and uv) and @ad<=20020502))	USPAT; US-PGPUB	2003/06/09 13:38
40	188	(organic with hardening) and (encapsulat$3)	USPAT; US-PGPUB	2003/06/09 13:55
41	185	((organic with hardening) and (encapsulat$3)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 13:53
42	81	(((organic with hardening) and (encapsulat$3)) and @ad<=20020502) and (removing or etching)	USPAT; US-PGPUB	2003/06/09 13:52
43	356	(organic same hardening) and (encapsulat$3)	USPAT; US-PGPUB	2003/06/09 13:52
44	145	((organic same hardening) and (encapsulat$3)) and (removing or etching)	USPAT; US-PGPUB	2003/06/09 13:52
45	140	(((organic same hardening) and (encapsulat$3)) and (removing or etching)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 13:57
46	59	((((organic same hardening) and (encapsulat$3)) and (removing or etching)) and @ad<=20020502) not ((((organic with hardening) and (encapsulat$3)) and @ad<=20020502) and (removing or etching))	USPAT; US-PGPUB	2003/06/09 13:53
47	81	hardening and encapsulat$3 and (planarization or planarizing or planarized)	USPAT; US-PGPUB	2003/06/09 13:57
48	79	(hardening and encapsulat$3 and (planarization or planarizing or planarized)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 14:06
49	58	((hardening and encapsulat$3 and (planarization or planarizing or planarized)) and @ad<=20020502) and plurality	USPAT; US-PGPUB	2003/06/09 14:06
50	576	(hardening with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)	USPAT; US-PGPUB	2003/06/09 14:14
51	252	((hardening with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality	USPAT; US-PGPUB	2003/06/09 14:15

52	240	(((hardening with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 14:15
53	108	((((hardening with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and @ad<=20020502) and (etching or removing)	USPAT; US-PGPUB	2003/06/09 14:15
54	1508	(UV with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)	USPAT; US-PGPUB	2003/06/09 14:15
55	681	((UV with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality	USPAT; US-PGPUB	2003/06/09 14:15
56	407	(((UV with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and (etching or removing)	USPAT; US-PGPUB	2003/06/09 14:15
57	368	((((UV with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and (etching or removing)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 14:15
58	354	(((((UV with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and (etching or removing)) and @ad<=20020502) not (((((hardening with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and @ad<=20020502) and (etching or removing))	USPAT; US-PGPUB	2003/06/09 14:16
59	354	((((((UV with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and (etching or removing)) and @ad<=20020502) not (((((hardening with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and @ad<=20020502) and (etching or removing))) not (((organic with hardening) and (encapsulat$3)) and @ad<=20020502)	USPAT; US-PGPUB	2003/06/09 15:31
60	6291	(photoresist or photomask) with negative	USPAT; US-PGPUB	2003/06/09 15:43
61	143	((photoresist or photomask) with negative) and (hardening with (uv or light))	USPAT; US-PGPUB	2003/06/09 15:43
62	138	(((photoresist or photomask) with negative) and (hardening with (uv or light))) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 15:33
63	2037	(photoresist or photomask) with negative	EPO; JPO; DERWENT; IBM_TDB	2003/06/09 15:43
64	9	((photoresist or photomask) with negative) and (hardening with (uv or light))	EPO; JPO; DERWENT; IBM_TDB	2003/06/09 15:44

L Number	Hits	Search Text	DB	Time stamp
1	225	(photoresist or photomask) with (hardening same (light or UV))	USPAT; US-PGPUB	2003/06/11 11:05
2	209	((photoresist or photomask) with (hardening same (light or UV))) and (removing or etching or patterning)	USPAT; US-PGPUB	2003/06/11 11:07
3	46	(((photoresist or photomask) with (hardening same (light or UV))) and (removing or etching or patterning)) and barrier	USPAT; US-PGPUB	2003/06/11 10:23
4	43	((((photoresist or photomask) with (hardening same (light or UV))) and (removing or etching or patterning)) and barrier) and @ad<=20020502	USPAT; US-PGPUB	2003/06/11 11:08
5	88	(photoresist or photomask) with (hardening same (light or UV))	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 10:29
6	25	((photoresist or photomask) with (hardening same (light or UV))) and (removing or etching or patterning)	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 10:29
7	1	("6498114").PN.	USPAT; US-PGPUB	2003/06/11 11:04
8	27759	(photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)	USPAT; US-PGPUB	2003/06/11 11:24
9	17677	((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor	USPAT; US-PGPUB	2003/06/11 11:24
10	16363	(((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and substrate	USPAT; US-PGPUB	2003/06/11 11:07
11	15122	((((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and substrate) and (removing or etching or patterning)	USPAT; US-PGPUB	2003/06/11 11:24
12	8738	(((((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and substrate) and (removing or etching or patterning)) and plurality	USPAT; US-PGPUB	2003/06/11 11:25
13	978	((((((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and substrate) and (removing or etching or patterning)) and plurality) and (led or oled)	USPAT; US-PGPUB	2003/06/11 11:09
15	44	(((((((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and substrate) and (removing or etching or patterning)) and plurality) and (led or oled)) and hardening	USPAT; US-PGPUB	2003/06/11 11:26
16	4003	(photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 11:24
17	1233	((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 11:24
18	411	(((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and (removing or etching or patterning)	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 11:25

19	8	((((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and (removing or etching or patterning)) and plurality	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 11:25
25	0	((pichler near2 kari) or (firschknecht near2 kyle))	USPAT; US-PGPUB	2003/06/11 11:30
26	0	((pichler near2 kari) or (firschknecht near2 kyle))	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 11:30

L=15

	U	1 [1]	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R trieval Classif
1	☐	☒	US 20020052062 A1	20020502	24	Method of manufacturing circuit device	438/110	438/107; 438/113	
2	☐	☒	US 20020045028 A1	20020418	17	Microstructure array, mold for forming a microstructure array, and method of fabricating the same	428/156	427/248.1; 427/402; 427/58; 428/161; 428/163	
3	☐	☒	US 20020044163 A1	20020418	52	Head unit, display device panel manufacturing apparatus for manufacturing panel for display device using the head unit, manufacturing method thereof, manufacturing method of liquid crystal display device having color filter, and device having the liquid crystal display device	347/1		
4	☐	☒	US 20010003384 A1	20010614	19	Method for manufacturing a molding tool used for substrate molding	264/219	425/192R	
5	☐	☒	US 6207247 B1	20010327	17	Method for manufacturing a molding tool used for sustrate molding	428/64.1	369/275.1; 369/288; 428/457; 428/64.2; 428/64.4; 428/913; 430/270.11; 430/495.1; 430/913	

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	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
1	Sakamoto, Noriaki et al.	☒	☐	☐	☐	☐	☐	☐	US 20020052062	☐
2	Teshima, Takayuki et al.	☒	☐	☐	☐	☐	☐	☐	US 20020045028	☐
3	Shigemura, Yoshihiro	☒	☐	☐	☐	☐	☐	☐	US 20020044163	☐
4	Morita, Seiji	☒	☐	☐	☐	☐	☐	☐	US 20010003384	☐
5	Morita, Shiji	☒	☐	☐	☐	☐	☐	☐	US 6207247	☐

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L Number	Hits	Search Text	DB	Time stamp
1	612	(selectively with depositi$3) same mask	EPO; JPO; DERWENT; IBM_TDB	2003/06/12 12:44
2	26	((selectively with depositi$3) same mask) and barrier	EPO; JPO; DERWENT; IBM_TDB	2003/06/12 13:22
3	1536	(selectively with depositi$3) same mask	USPAT; US-PGPUB	2003/06/12 12:44
4	418	((selectively with depositi$3) same mask) and barrier	USPAT; US-PGPUB	2003/06/12 12:44
5	398	(((selectively with depositi$3) same mask) and barrier) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 13:23
10	148	(laminated with mask) same opening	USPAT; US-PGPUB	2003/06/12 13:32
11	38	(laminated near3 mask) same opening	USPAT; US-PGPUB	2003/06/12 13:24
12	36	((laminated near3 mask) same opening) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 13:34
13	0	(laminated adj mask) same organic	USPAT; US-PGPUB	2003/06/12 13:33
14	0	(laminated adj film adj mask) same organic	USPAT; US-PGPUB	2003/06/12 13:33
15	0	(multiple adj film adj mask) same organic	USPAT; US-PGPUB	2003/06/12 13:34
16	0	(multiple adj layer adj mask) same organic	USPAT; US-PGPUB	2003/06/12 13:34
17	30	(multiple with layer with mask) same organic	USPAT; US-PGPUB	2003/06/12 13:34
18	27	((multiple with layer with mask) same organic) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 14:02
19	1	(plurality near3 devices) and planarization and barrier and (depositing with inert)	USPAT; US-PGPUB	2003/06/12 13:58
20	0	(plurality near3 devices) and planarization and barrier and (depositing with inert with (ambient or atmosphere))	USPAT; US-PGPUB	2003/06/12 13:58
21	8	planarization and barrier and (depositing with inert with (ambient or atmosphere))	USPAT; US-PGPUB	2003/06/12 14:01
22	13	(planarized near3 (layer or film)) and barrier and (depositing with inert with (ambient or atmosphere))	USPAT; US-PGPUB	2003/06/12 14:02
23	13	((planarized near3 (layer or film)) and barrier and (depositing with inert with (ambient or atmosphere))) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 14:07
24	1	("5886410").PN.	USPAT; US-PGPUB	2003/06/12 14:06
25	76	mosfet and planarization and (inert with (ambient or atmosphere))	USPAT; US-PGPUB	2003/06/12 14:14
26	30	(mosfet and planarization and (inert with (ambient or atmosphere))) and barrier	USPAT; US-PGPUB	2003/06/12 14:14
27	27	((mosfet and planarization and (inert with (ambient or atmosphere))) and barrier) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 14:10
28	1	mosfet and planarization and (depositing with inert with (ambient or atmosphere))	USPAT; US-PGPUB	2003/06/12 14:09
29	0	mosfet and (depositing with planarization) and (depositing with inert with (ambient or atmosphere))	USPAT; US-PGPUB	2003/06/12 14:32
30	10	mosfet and (depositing with inert with (ambient or atmosphere)) and barrier	USPAT; US-PGPUB	2003/06/12 14:15
31	10	(mosfet and (depositing with inert with (ambient or atmosphere)) and barrier) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 14:15
32	271	interconnect and planarization and (inert with (ambient or atmosphere))	USPAT; US-PGPUB	2003/06/12 14:14
33	168	(interconnect and planarization and (inert with (ambient or atmosphere))) and barrier	USPAT; US-PGPUB	2003/06/12 14:38

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① dep are stretching for majority
② spent 3 days
v. exhausted search

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34	6	((interconnect and planarization and (inert with (ambient or atmosphere))) and barrier) and (depositing with inert with (ambient or atmosphere)) and barrier	USPAT; US-PGPUB	2003/06/12 14:15
35	6	(((interconnect and planarization and (inert with (ambient or atmosphere))) and barrier) and (depositing with inert with (ambient or atmosphere)) and barrier) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 14:33
36	21	depositing with dielectric with inert with (ambient or atmosphere)	USPAT; US-PGPUB	2003/06/12 14:37
38	0	((laminated adj film adj mask) same organic) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 14:38
37	14	(depositing with dielectric with inert with (ambient or atmosphere)) and barrier	USPAT; US-PGPUB	2003/06/12 14:36
39	375	depositing with inert with (ambient or atmosphere)	USPAT; US-PGPUB	2003/06/12 14:37
40	827	depositing same (inert with (ambient or atmosphere))	USPAT; US-PGPUB	2003/06/12 14:37
41	284	(depositing same (inert with (ambient or atmosphere))) and barrier	USPAT; US-PGPUB	2003/06/12 14:38
42	275	((depositing same (inert with (ambient or atmosphere))) and barrier) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 15:00
43	275	(((depositing same (inert with (ambient or atmosphere))) and barrier) and @ad<=20020502) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 14:46
44	803	(depositing same (inert with (ambient or atmosphere))) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 15:01
45	528	((depositing same (inert with (ambient or atmosphere))) and @ad<=20020502) not ((depositing same (inert with (ambient or atmosphere))) and barrier)	USPAT; US-PGPUB	2003/06/12 14:47
46	0	gas adj nozzle adj deposition	USPAT; US-PGPUB	2003/06/12 15:00
47	583	gas with nozzle with deposition	USPAT; US-PGPUB	2003/06/12 15:01
48	558	(gas with nozzle with deposition) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 15:27
49	120	((gas with nozzle with deposition) and @ad<=20020502) and barrier	USPAT; US-PGPUB	2003/06/12 15:03
50	0	(((gas with nozzle with deposition) and @ad<=20020502) and barrier) and Oled	USPAT; US-PGPUB	2003/06/12 15:03
51	0	(((gas with nozzle with deposition) and @ad<=20020502) and barrier) and oled	USPAT; US-PGPUB	2003/06/12 15:03
52	16	(((gas with nozzle with deposition) and @ad<=20020502) and barrier) and led	USPAT; US-PGPUB	2003/06/12 15:03
53	60	((gas with nozzle with deposition) and @ad<=20020502) and (moving with substrate)	USPAT; US-PGPUB	2003/06/12 15:32

	Typ	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
28	BRS	107	(light adj emitting adj diodes) same (encapsulation or encapsulating)	USPAT; US-PGPUB	2003/06/07 16:04		
29	BRS	64	((light adj emitting adj diodes) same (encapsulation or encapsulating)) and plurality and @ad<=20020502	USPAT; US-PGPUB	2003/06/07 16:05		
30	BRS	554	(led or oled) same (encapsulation or encapsulating)	USPAT; US-PGPUB	2003/06/07 15:57		
31	BRS	274	((led or oled) same (encapsulation or encapsulating)) and plurality and @ad<=20020502	USPAT; US-PGPUB	2003/06/07 15:57		
32	BRS	258	(((led or oled) same (encapsulation or encapsulating)) and plurality and @ad<=20020502) not (((light adj emitting adj diodes) same (encapsulation or encapsulating)) and plurality and @ad<=20020502)	USPAT; US-PGPUB	2003/06/07 15:49		
33	BRS	2	((led or oled) same (encapsulation or encapsulating)) and plurality	EPO; JPO; DERWENT; IBM_TDB	2003/06/07 15:58		
34	BRS	142	(led or oled) same (encapsulation or encapsulating)	EPO; JPO; DERWENT; IBM_TDB	2003/06/07 16:03		
35	BRS	25	((light adj emitting adj diodes) same (encapsulation or encapsulating)) and (harden or hardening or uv)	USPAT; US-PGPUB	2003/06/07 16:07		
36	BRS	24	(((light adj emitting adj diodes) same (encapsulation or encapsulating)) and (harden or hardening or uv)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/07 16:05		

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	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error D finition
37	BRS	321	(light adj emitting adj diodes) and (encapsulation or encapsulating) and (harden or hardening or uv)	USPAT; US-PGPUB	2003/06/07 16:08		
38	BRS	297	((light adj emitting adj diodes) and (encapsulation or encapsulating) and (harden or hardening or uv)) not ((((light adj emitting adj diodes) same (encapsulation or encapsulating)) and (harden or hardening or uv)) and @ad<=20020502)	USPAT; US-PGPUB	2003/06/07 16:08		
39	BRS	258	(((light adj emitting adj diodes) and (encapsulation or encapsulating) and (harden or hardening or uv)) not ((((light adj emitting adj diodes) same (encapsulation or encapsulating)) and (harden or hardening or uv)) and @ad<=20020502)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/07 16:09		
40	BRS	193	((((light adj emitting adj diodes) and (encapsulation or encapsulating) and (harden or hardening or uv)) not ((((light adj emitting adj diodes) same (encapsulation or encapsulating)) and (harden or hardening or uv)) and @ad<=20020502)) and @ad<=20020502) and plurality	USPAT; US-PGPUB	2003/06/09 09:39		
41	BRS	23	(encapsulation or encapsulating) same (planarization or planarizing) same (spin or flash or evaporation or roll or blade or dip or spray)	USPAT; US-PGPUB	2003/06/09 10:40		

SDC EX. 1002 - 107/544

	Type	Hits	Search T xt	DBs	Time Stamp	Comments	Error Definition
42	BRS	2	((encapsulation or encapsulating) same (planarization or planarizing) same (spin or flash or evaporation or roll or blade or dip or spray)) and hardening	USPAT; US-PGPUB	2003/06/09 10:40		
43	BRS	139	(encapsulation or encapsulating) and ((planarization or planarizing) same (spin or flash or evaporation or roll or blade or dip or spray))	USPAT; US-PGPUB	2003/06/09 10:41		
44	BRS	10	((encapsulation or encapsulating) and ((planarization or planarizing) same (spin or flash or evaporation or roll or blade or dip or spray))) and hardening	USPAT; US-PGPUB	2003/06/09 10:42		
45	BRS	8	(((encapsulation or encapsulating) and ((planarization or planarizing) same (spin or flash or evaporation or roll or blade or dip or spray))) and hardening) not (((encapsulation or encapsulating) same (planarization or planarizing) same (spin or flash or evaporation or roll or blade or dip or spray)) and hardening)	USPAT; US-PGPUB	2003/06/09 10:40		
46	BRS	28806	(encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)	USPAT; US-PGPUB	2003/06/09 11:36		

SDC EX. 1002 - 108/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
47	BRS	1913	((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening	USPAT; US-PGPUB	2003/06/09 11:13		
48	BRS	925	(((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and plurality	USPAT; US-PGPUB	2003/06/09 11:02		
49	BRS	239	((((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and plurality) and uv	USPAT; US-PGPUB	2003/06/09 10:43		
50	BRS	221	(((((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and plurality) and uv) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 11:03		
51	BRS	199	(((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and (plurality with (device or elements))	USPAT; US-PGPUB	2003/06/09 11:03		
52	BRS	193	((((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and (plurality with (device or elements))) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 11:41		

SDC EX. 1002 - 109/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
53	BRS	151	(((((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and (plurality with (device or elements))) and @ad<=20020502) not ((((((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening) and plurality) and uv) and @ad<=20020502)	USPAT; US-PGPUB	2003/06/09 11:04		
54	BRS	855	(encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)	EPO; JPO; DERWENT; IBM_TDB	2003/06/09 11:13		
55	BRS	14	((encapsulation or encapsulating) and (spin or flash or evaporation or roll or blade or dip or spray)) and hardening	EPO; JPO; DERWENT; IBM_TDB	2003/06/09 11:13		
56	BRS	621	(hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))	USPAT; US-PGPUB	2003/06/09 11:40		
57	BRS	347	((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and (removing or etching)	USPAT; US-PGPUB	2003/06/09 11:51		
58	BRS	72	((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and ((removing or etching) with (hardening or hardened))	USPAT; US-PGPUB	2003/06/09 11:41		

SDC EX. 1002 - 110/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
59	BRS	61	(((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and ((removing or etching) with (hardening or hardened))) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 11:46		
60	BRS	10	((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and ((removing or etching) with (hardening or hardened))) and @ad<=20020502) and barrier	USPAT; US-PGPUB	2003/06/09 11:46		
61	BRS	312	(((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and (removing or etching)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 11:54		
62	BRS	59	((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and (removing or etching)) and @ad<=20020502) and barrier	USPAT; US-PGPUB	2003/06/09 11:46		

SDC EX. 1002 - 111/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
63	BRS	49	((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and (removing or etching)) and @ad<=20020502) and barrier) not ((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and ((removing or etching) with (hardening or hardened))) and @ad<=20020502) and barrier)	USPAT; US-PGPUB	2003/06/09 11:46		
64	BRS	197	438/106-110,124,126,127.ccls. and hardening and (removing or etching)	USPAT; US-PGPUB	2003/06/09 12:14		
65	BRS	160	(438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality	USPAT; US-PGPUB	2003/06/09 11:57		
66	BRS	147	((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 11:57		
67	BRS	31	(((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier	USPAT; US-PGPUB	2003/06/09 11:57		
68	BRS	678	438/106-110,124,126,127.ccls. and harden$3	USPAT; US-PGPUB	2003/06/09 12:14		
69	BRS	527	(438/106-110,124,126,127.ccls. and harden$3) and plurality	USPAT; US-PGPUB	2003/06/09 11:57		
70	BRS	87	((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier	USPAT; US-PGPUB	2003/06/09 12:03		

SDC EX. 1002 - 112/544

	Type	Hits	Search T xt	DBs	Time Stamp	Comments	Error Definition
71	BRS	82	(((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 15:32		
72	BRS	51	((((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier) and @ad<=20020502) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier)	USPAT; US-PGPUB	2003/06/09 11:57		
73	BRS	21	((438/106-110,124,126,127.ccls. and harden$3) and plurality) and ((removing or etching) with (hardened or unwanted))	USPAT; US-PGPUB	2003/06/09 13:50		
74	BRS	420	(438/106-110,124,126,127.ccls. and harden$3) and (removing or etching)	USPAT; US-PGPUB	2003/06/09 12:15		
75	BRS	387	((438/106-110,124,126,127.ccls. and harden$3) and (removing or etching)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 13:50		
76	BRS	358	(((438/106-110,124,126,127.ccls. and harden$3) and (removing or etching)) and @ad<=20020502) not (((((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier) and @ad<=20020502) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier))	USPAT; US-PGPUB	2003/06/09 12:16		

SDC EX. 1002 - 113/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
77	BRS	327	((((438/106-110,124,126,127.ccls. and harden$3) and (removing or etching)) and @ad<=20020502) not (((((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier) and @ad<=20020502) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier))) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier)	USPAT; US-PGPUB	2003/06/09 12:16		

SDC EX. 1002 - 114/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
78	BRS	327	(((((438/106-110,124,126,127.ccls. and harden$3) and (removing or etching)) and @ad<=20020502) not (((((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier) and @ad<=20020502) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier))) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier)) not ((((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and (removing or etching)) and @ad<=20020502) and barrier) not (((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and ((removing or etching) with (hardening or hardened))) and	USPAT; US-PGPUB	2003/06/09 12:17		

SDC EX. 1002 - 115/544

	Type	Hits	Search Text	DBs	Tim Stamp	Comments	Error Definition
79	BRS	321	((((((438/106-110,124,126,127.ccls. and harden$3) and (removing or etching)) and @ad<=20020502) not (((((438/106-110,124,126,127.ccls. and harden$3) and plurality) and barrier) and @ad<=20020502) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier))) not ((((438/106-110,124,126,127.ccls. and hardening and (removing or etching)) and plurality) and @ad<=20020502) and barrier)) not ((((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and (removing or etching)) and @ad<=20020502) and barrier) not ((((hardening with (dielectric or insulative or insulating or insulator or layer)) and (plurality with (devices or elements))) and ((removing or etching) with (hardening or hardened))) and	USPAT; US-PGPUB	2003/06/09 13:38		
80	BRS	188	(organic with hardening) and (encapsulat$3)	USPAT; US-PGPUB	2003/06/09 13:55		
81	BRS	185	((organic with hardening) and (encapsulat$3)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 13:53		

SDC EX. 1002 - 116/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
82	BRS	81	(((organic with hardening) and (encapsulat$3)) and @ad<=20020502) and (removing or etching)	USPAT; US-PGPUB	2003/06/09 13:52		
83	BRS	356	(organic same hardening) and (encapsulat$3)	USPAT; US-PGPUB	2003/06/09 13:52		
84	BRS	145	((organic same hardening) and (encapsulat$3)) and (removing or etching)	USPAT; US-PGPUB	2003/06/09 13:52		
85	BRS	140	(((organic same hardening) and (encapsulat$3)) and (removing or etching)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 13:57		
86	BRS	59	((((organic same hardening) and (encapsulat$3)) and (removing or etching)) and @ad<=20020502) not ((((organic with hardening) and (encapsulat$3)) and @ad<=20020502) and (removing or etching))	USPAT; US-PGPUB	2003/06/09 13:53		
87	BRS	81	hardening and encapsulat$3 and (planarization or planarizing or planarized)	USPAT; US-PGPUB	2003/06/09 13:57		
88	BRS	79	(hardening and encapsulat$3 and (planarization or planarizing or planarized)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 14:06		
89	BRS	58	((hardening and encapsulat$3 and (planarization or planarizing or planarized)) and @ad<=20020502) and plurality	USPAT; US-PGPUB	2003/06/09 14:06		
90	BRS	576	(hardening with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)	USPAT; US-PGPUB	2003/06/09 14:14		

SDC EX. 1002 - 117/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
91	BRS	252	((hardening with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality	USPAT; US-PGPUB	2003/06/09 14:15		
92	BRS	240	(((hardening with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 14:15		
93	BRS	108	((((hardening with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and @ad<=20020502) and (etching or removing)	USPAT; US-PGPUB	2003/06/09 14:15		
94	BRS	1508	(UV with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)	USPAT; US-PGPUB	2003/06/09 14:15		
95	BRS	681	((UV with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality	USPAT; US-PGPUB	2003/06/09 14:15		
96	BRS	407	(((UV with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and (etching or removing)	USPAT; US-PGPUB	2003/06/09 14:15		
97	BRS	368	((((UV with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and (etching or removing)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 14:15		

SDC EX. 1002 - 118/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
98	BRS	354	(((((UV with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and (etching or removing)) and @ad<=20020502) not (((((hardening with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and @ad<=20020502) and (etching or removing))	USPAT; US-PGPUB	2003/06/09 14:16		
99	BRS	354	((((((UV with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and (etching or removing)) and @ad<=20020502) not (((((hardening with (organic or polymer or dielectric or insulating or insulative or insulator)) and (encapsulat$3)) and plurality) and @ad<=20020502) and (etching or removing))) not (((organic with hardening) and (encapsulat$3)) and @ad<=20020502)	USPAT; US-PGPUB	2003/06/09 15:31		
100	BRS	6291	(photoresist or photomask) with negative	USPAT; US-PGPUB	2003/06/09 15:43		
101	BRS	143	((photoresist or photomask) with negative) and (hardening with (uv or light))	USPAT; US-PGPUB	2003/06/09 15:43		
102	BRS	138	(((photoresist or photomask) with negative) and (hardening with (uv or light))) and @ad<=20020502	USPAT; US-PGPUB	2003/06/09 15:33		

SDC EX. 1002 - 119/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
103	BRS	2037	(photoresist or photomask) with negative	EPO; JPO; DERWENT; IBM_TDB	2003/06/09 15:43		
104	BRS	9	((photoresist or photomask) with negative) and (hardening with (uv or light))	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 10:21		
105	BRS	225	(photoresist or photomask) with (hardening same (light or UV))	USPAT; US-PGPUB	2003/06/11 11:05		
106	BRS	209	((photoresist or photomask) with (hardening same (light or UV))) and (removing or etching or patterning)	USPAT; US-PGPUB	2003/06/11 11:07		
107	BRS	46	(((photoresist or photomask) with (hardening same (light or UV))) and (removing or etching or patterning)) and barrier	USPAT; US-PGPUB	2003/06/11 10:23		
108	BRS	43	((((photoresist or photomask) with (hardening same (light or UV))) and (removing or etching or patterning)) and barrier) and @ad<=20020502	USPAT; US-PGPUB	2003/06/11 12:56		
109	BRS	88	(photoresist or photomask) with (hardening same (light or UV))	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 10:29		
110	BRS	25	((photoresist or photomask) with (hardening same (light or UV))) and (removing or etching or patterning)	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 10:29		
111	IS&R	1	("6498114").PN.	USPAT; US-PGPUB	2003/06/11 11:04		
112	BRS	27759	(photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)	USPAT; US-PGPUB	2003/06/11 12:52		
113	BRS	17677	((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor	USPAT; US-PGPUB	2003/06/11 11:24		

SDC EX. 1002 - 120/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
114	BRS	16363	(((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and substrate	USPAT; US-PGPUB	2003/06/11 11:07		
115	BRS	15122	((((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and substrate) and (removing or etching or patterning)	USPAT; US-PGPUB	2003/06/11 11:24		
116	BRS	8738	(((((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and substrate) and (removing or etching or patterning)) and plurality	USPAT; US-PGPUB	2003/06/11 11:25		
117	BRS	978	((((((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and substrate) and (removing or etching or patterning)) and plurality) and (led or oled)	USPAT; US-PGPUB	2003/06/11 11:09		
118	BRS	44	(((((((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and substrate) and (removing or etching or patterning)) and plurality) and (led or oled)) and hardening	USPAT; US-PGPUB	2003/06/11 11:26		

SDC EX. 1002 - 121/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
119	BRS	4003	(photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 11:24		
120	BRS	1233	((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 11:24		
121	BRS	411	(((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and (removing or etching or patterning)	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 11:25		
122	BRS	8	((((photoresist or photomask) and (spinor flash or evaporation or blade or roll or dip or spray or screen or jet)) and semiconductor) and (removing or etching or patterning)) and plurality	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 11:25		
123	BRS	0	((pichler near2 kari) or (firschknecht near2 kyle))	USPAT; US-PGPUB	2003/06/11 11:30		
124	BRS	0	((pichler near2 kari) or (firschknecht near2 kyle))	EPO; JPO; DERWENT; IBM_TDB	2003/06/11 11:47		
125	IS&R	1	("6498114").PN.	USPAT; US-PGPUB	2003/06/11 12:54		
126	BRS	1007	(photoresist or photomask) same (flash or blade)	USPAT; US-PGPUB	2003/06/11 12:55		
127	BRS	243	(photoresist or photomask) same ((flash with evaporation) or blade)	USPAT; US-PGPUB	2003/06/11 12:49		
128	BRS	0	(photoresist or photomask) same (flash with evaporation) same blade	USPAT; US-PGPUB	2003/06/11 12:50		
129	BRS	13	(photoresist or photomask) same (flash with evaporation)	USPAT; US-PGPUB	2003/06/11 12:51		

SDC EX. 1002 - 122/544

	Type	Hits	Search Text	DBs	Tim Stamp	Comments	Error Definition
130	BRS	4437	blade adj coating	USPAT; US-PGPUB	2003/06/11 12:56		
131	BRS	789	(blade adj coating) and semiconductor	USPAT; US-PGPUB	2003/06/11 12:55		
132	BRS	90	((blade adj coating) and semiconductor) and (photoresist or photomask)	USPAT; US-PGPUB	2003/06/11 12:56		
133	BRS	89	(((blade adj coating) and semiconductor) and (photoresist or photomask)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/11 13:17		
134	BRS	0	((((blade adj coating) and semiconductor) and (photoresist or photomask)) and @ad<=20020502) and (flash adj evaporation)	USPAT; US-PGPUB	2003/06/11 12:56		
135	BRS	7	((((blade adj coating) and semiconductor) and (photoresist or photomask)) and @ad<=20020502) and flash	USPAT; US-PGPUB	2003/06/11 13:44		
136	BRS	0	optical adj patterning adj system	USPAT; US-PGPUB	2003/06/11 13:17		
137	BRS	77	optical adj patterning	USPAT; US-PGPUB	2003/06/11 13:17		
138	BRS	32	(optical adj patterning) and UV	USPAT; US-PGPUB	2003/06/11 13:17		
139	BRS	32	((optical adj patterning) and UV) and @ad<=20020502	USPAT; US-PGPUB	2003/06/11 14:39		
140	BRS	0	((thermal adj evaporation) with vacuum) with removing	USPAT; US-PGPUB	2003/06/11 13:46		
141	BRS	487	((thermal adj evaporation) with vacuum)	USPAT; US-PGPUB	2003/06/11 13:51		
142	BRS	112	(((thermal adj evaporation) with vacuum)) and removing	USPAT; US-PGPUB	2003/06/11 13:51		
143	BRS	40	((((thermal adj evaporation) with vacuum)) and removing) and photoresist	USPAT; US-PGPUB	2003/06/11 13:46		

SDC EX. 1002 - 123/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
144	BRS	39	(((((thermal adj evaporation) with vacuum)) and removing) and photoresist) and @ad<=20020502	USPAT; US-PGPUB	2003/06/11 13:46		
145	BRS	14	(((thermal adj evaporation) with vacuum)) and hardening	USPAT; US-PGPUB	2003/06/11 13:52		
146	BRS	5	((((thermal adj evaporation) with vacuum)) and hardening) and removing	USPAT; US-PGPUB	2003/06/11 13:50		
147	BRS	0	((thermal adj evaporation) with vacuum) same removing	USPAT; US-PGPUB	2003/06/11 13:52		
148	BRS	0	((thermal adj evaporation) with vacuum) same removing	EPO	2003/06/11 13:52		
149	BRS	9	(evaporation with vacuum) same removing	EPO	2003/06/11 13:52		
150	BRS	911	(evaporation with vacuum) same removing	USPAT; US-PGPUB	2003/06/11 13:52		
151	BRS	505	(evaporation with vacuum) with removing	USPAT; US-PGPUB	2003/06/11 13:52		
152	BRS	11	((evaporation with vacuum) with removing) and hardening	USPAT; US-PGPUB	2003/06/11 14:25		
153	IS&R	1	("6498114").PN.	USPAT; US-PGPUB	2003/06/11 14:37		
154	BRS	16	parylene same plasma same (deposition or depositing) same (photoresist or resist or photomask)	USPAT; US-PGPUB	2003/06/11 15:02		
155	BRS	16	(parylene same plasma same (deposition or depositing) same (photoresist or resist or photomask)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/11 14:53		
156	BRS	280	parylene same (deposition or depositing) same (photoresist or resist or photomask or dielectric)	USPAT; US-PGPUB	2003/06/11 14:59		
157	BRS	71	(parylene same (deposition or depositing) same (photoresist or resist or photomask or dielectric)) same plasma	USPAT; US-PGPUB	2003/06/11 14:57		

SDC EX. 1002 - 124/544

	Type	Hits	Search Text	DBs	Tim Stamp	Comments	Error Definition
158	BRS	54	((parylene same (deposition or depositing) same (photoresist or resist or photomask or dielectric)) same plasma) and semiconductor	USPAT; US-PGPUB	2003/06/11 14:57		
159	BRS	54	(((parylene same (deposition or depositing) same (photoresist or resist or photomask or dielectric)) same plasma) and semiconductor) and @ad<=20020502	USPAT; US-PGPUB	2003/06/11 14:57		
160	BRS	64	parylene same (deposition or depositing) same (photoresist or resist or photomask)	USPAT; US-PGPUB	2003/06/11 14:57		
161	BRS	16	(parylene same (deposition or depositing) same (photoresist or resist or photomask)) same plasma	USPAT; US-PGPUB	2003/06/11 15:03		
162	BRS	16	((parylene same (deposition or depositing) same (photoresist or resist or photomask)) same plasma) and @ad<=20020502	USPAT; US-PGPUB	2003/06/11 15:00		
163	BRS	6	(((parylene same (deposition or depositing) same (photoresist or resist or photomask)) same plasma) and @ad<=20020502) and semiconductor	USPAT; US-PGPUB	2003/06/11 14:58		
164	BRS	179	parylene same (deposition or depositing) same plasma	USPAT; US-PGPUB	2003/06/11 14:59		
165	BRS	95	(parylene same (deposition or depositing) same plasma) and semiconductor	USPAT; US-PGPUB	2003/06/11 15:00		
166	BRS	92	((parylene same (deposition or depositing) same plasma) and semiconductor) and @ad<=20020502	USPAT; US-PGPUB	2003/06/11 15:02		

SDC EX. 1002 - 125/544

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
167	BRS	214	parylene same (photoresist or resist or photomask)	USPAT; US-PGPUB	2003/06/11 15:02		
168	BRS	201	(parylene same (photoresist or resist or photomask)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/11 15:02		
169	BRS	65	((parylene same (photoresist or resist or photomask)) and @ad<=20020502) and (plasma with (depositing or deposition))	USPAT; US-PGPUB	2003/06/12 10:38		
170	IS&R	1	("5703433").PN.	USPAT; US-PGPUB	2003/06/11 16:17		
171	BRS	445	(selective adj deposition) same mask	USPAT; US-PGPUB	2003/06/12 11:06		
172	BRS	231	((selective adj deposition) same mask) and opening	USPAT; US-PGPUB	2003/06/12 10:56		
173	BRS	76	(((selective adj deposition) same mask) and opening) and barrier	USPAT; US-PGPUB	2003/06/12 11:06		
174	BRS	155	(((selective adj deposition) same mask) and opening) not ((((selective adj deposition) same mask) and opening) and barrier)	USPAT; US-PGPUB	2003/06/12 10:56		
175	BRS	153	((((selective adj deposition) same mask) and opening) not ((((selective adj deposition) same mask) and opening) and barrier)) and @ad<=20020502	USPAT; US-PGPUB	2003/06/12 10:57		
176	BRS	90	(selective adj deposition) same mask	EPO; JPO; DERWENT; IBM_TDB	2003/06/12 12:40		

SDC EX. 1002 - 126/544

1700 INTERNAL TRANSFER REQUEST FOR S.N.: 10/137/163

FROM (print name/AU): Cathy Lam **DATE:** 10-2-02

FORWARD TO:		REASON(S):	
Art Unit:	1753	You had Parent S.N.:	
Class:	136	See Specification page(s):	
Subclass:	244	See Claims:	

REASONS:

Claims are directed to an organic solar cell device.

ACCEPTED BY (print name/AU): _____ **DATE:** _____

DECLINED BY (print name/AU): Nguyen **DATE:** _____

FORWARD TO:		REASON(S):	
Art Unit:	1775	You had Parent S.N.:	
Class:	428	See Specification page(s):	
Subclass:		See Claims:	

REASONS:

Claim directed to electronic device; try class 257

BEST AVAILABLE COPY

ACCEPTED BY (print name/AU): _____ **DATE:** _____

DECLINED BY (print name/AU): _____ **DATE:** _____

FORWARD TO: 1709 1745	REASON(S):	
1700 CLASSIFICATION UNIT	See Specification page(s):	
	See Claims:	

REASONS:

See the last claim, it is directed to a solar cell device.

DISPOSITION BY 1700 CLASSIFICATION UNIT

FORWARD TO:		REASON(S):	
Art Unit:		You had Parent S.N.:	
Class:		See Specification page(s):	
Subclass:		See Claims:	

REASONS:

BY CLASSIFIER (print name): _____ **DATE:** _____

Form PTO-447A (Rev. 7-98) | Staple to face of Application | U.S. DEPARTMENT OF COMMERCE PATENT & TRADEMARK OFFICE

APPLICATION TRANSFER REQUEST FOR S.N. 10137163

Section I. TRANSFER REQUEST BY Name **JONES, DEBORAH D** Date **12/6/2002**

TO: Art Unit ~~2811~~ 2823 Class/sub ~~257~~/438 **FROM:** A.U. **1775** Class _____

REASON:
See last claim - to solar cell device

Gatekeeper concurrence _____

Section IIa. DISPOSITION BY RECEIVING TC **By:** _____ **A.U.** _____ **Date** _____

NOT ACCEPTED ☐ Forward to receiving TC Post Classifier

REASON:

Section IIb. DISPOSITION BY RECEIVING TC POST CLASSIFIER

☐ This dispute was resolved. Forward to TC/AU _____ Class/Sub _____/_____ Post Classifier _____ Date _____

Concurring _____

☐ This dispute was not resolved, forward to DISPUTE RESOLUTION PANEL

Post Classifier Assessment:

Gatekeeper concurrence _____ Post Classifier _____ Date _____

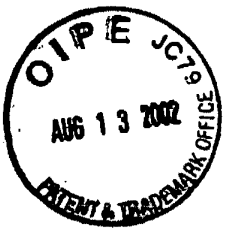
Section III. DISPOSITION BY DISPUTE RESOLUTION PANEL Date _____

Panel Decision: Forward To Technology Center/Art Unit _____ Class/sub _____/_____

REASON:

Panel Member _____ Concurring Panel Member _____

SDC EX. 1002 - 128/544



PATENT
Atty. Docket No.: 2002P03156US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Karl Pichler et al.

Application No.: 10/137,163

Filed: May 2, 2002

For: IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

Examiner: Unassigned
Group: Unassigned

I hereby certify that this correspondence is being deposited on this date with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: The Assistant Commissioner of Patents, Washington D.C. 20231 on the below date:

Date: August 9, 2002.
By: Jeanette L. Taplin

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

This is in response to the Notice to File Corrected Application Papers in that the drawings did not have the appropriate margins. Enclosed herewith are the Formal Drawings consisting of eight (8) sheets.

We believe there is no fee due for this response, however, if the Assistant Commissioner does not agree, please charge Deposit Account No. **19-2179** for any fees or credit to any overpayments. A duplicate copy of this sheet is enclosed.

Respectfully requested,

By: Tom George

Tom George
Registration No. 45,740
Attorney for Applicants
Tel: 650-694-5191
Fax: 650-968-4517

SIEMENS CORPORATION
Intellectual Property Department
186 Wood Avenue South
Iselin, New Jersey 08830
ATTENTION: Elsa Keller, IP Department
Telephone: (732) 321-3026

SDC EX. 1002 - 129/544

OIPE JC79
AUG 13 2002
PATENT & TRADEMARK OFFICE

#3

PATENT

Atty. Docket No.: 2002P03156US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Karl Pichler et al.

Application No.: 10/137,163

Filed: May 2, 2002

For: IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

Examiner: Unassigned
Group: Unassigned

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Date: August 9, 2002

By: Jeanette L. Taplin

RESPONSE TO NOTICE TO FILE MISSING PARTS

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

This is in response to the Notice to File Missing Parts mailed June 13, 2002, a copy of which is enclosed. Submitted herewith is the executed Declaration and Power of Attorney. An Assignment is being concurrently submitted to the Assignment Branch under separate cover.

Please charge the $130.00 surcharge for this response to our Deposit Account No. 19-2179. The Assistant Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment, to this deposit account. A duplicate copy of this sheet is enclosed.

Respectfully requested,

By: Tom George

Tom George
Registration No. 45,740
Attorney for Applicants
Tel: 650-694-5191
Fax: 650-968-4517

SIEMENS CORPORATION
Intellectual Property Department
186 Wood Avenue South
Iselin, New Jersey 08830
ATTENTION: Elsa Keller, IP Department
Telephone: (732) 321-3026

SDC EX. 1002 - 130/544

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/137,163	05/02/2002	Karl Pichler	2002P03156US

CONFIRMATION NO. 1705

Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

OIPE JC79 AUG 13 2002 PATENT & TRADEMARK OFFICE

FORMALITIES LETTER

OC000000008284291

Date Mailed: 06/13/2002

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

10137163 081502

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(l) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Substitute drawings in compliance with 37 CFR 1.84 because:
    - drawing sheets do not have the appropriate margin(s) (see 37 CFR 1.84(g)). Each sheet must include a top margin of at least 2.5 cm. (1 inch), a left side margin of at least 2.5 cm. (1 inch), a right side margin of at least 1.5 cm. (5/8 inch), and a bottom margin of at least 1.0 cm. (3/8 inch);

Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

SUMMARY OF FEES DUE:

08/15/2002 MBELETE1 00000050 192179 10137163
01 FC:105 130.00 CH

Total additional fee(s) required for this application is **$130** for a Large Entity

- **$130** Late oath or declaration Surcharge.

A copy of this notice <u>MUST</u> be returned with the reply.

Tsehai H

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

ACTION CLOSED

OIPE JC19
AUG 13 2002
PATENT & TRADEMARK OFFICE

PATENT
Atty. Docket No.: 2002P03156US

#4/IDS
Rcvd
8/6/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Karl Pichler et al.

Application No.: 10/137,163

Filed: May 2, 2002

For: IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

Examiner: Unassigned
Group: Unassigned

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Date: August 9, 2002
By: Jeanette L. Taplin

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

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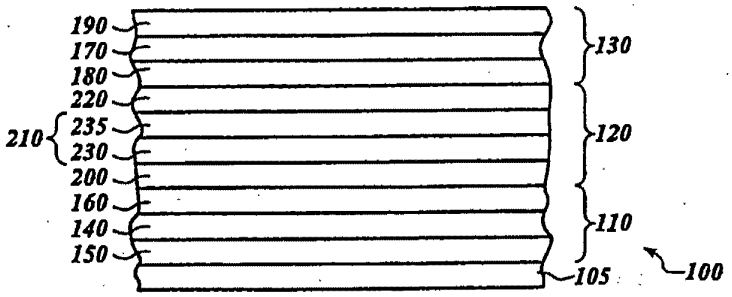
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(54) Title: ENVIRONMENTAL BARRIER MATERIAL FOR ORGANIC LIGHT EMITTING DEVICE AND METHOD OF MAKING



(57) Abstract

An encapsulated organic light emitting device. The device includes a first barrier stack (110) comprising at least one first barrier layer (140) and at least one first polymer layer (150, 160). There is an organic light emitting layer stack (120) adjacent to the first barrier stack. A second barrier stack (130) is adjacent to the organic light emitting layer stack. The second barrier stack has at least one second barrier layer (170) and at least one second polymer layer (180, 190). A method of making the encapsulated organic light emitting device is also provided.

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ENVIRONMENTAL BARRIER MATERIAL FOR ORGANIC LIGHT EMITTING DEVICE AND METHOD OF MAKING

BACKGROUND OF THE INVENTION

The present invention relates to organic light emitting devices (OLEDs), and more particularly to OLEDs encapsulated in barrier stacks.

There is a need for versatile visual displays for electronic products of many different types. Light emitting diodes (LEDs) and liquid crystal displays (LCDs) have found many useful applications, but they are not adequate for all situations. OLEDs are a relatively new type of visual display which has shown great promise. An OLED basically includes an organic electroluminescent substance placed between two electrodes. When an electric potential is applied across the electrodes, the electroluminescent substance emits visible light. Typically, one of the electrodes is transparent, allowing the light to shine through. U.S. Patent Nos. 5,629,389 (Roitman et al.), 5,747,182 (Friend et al.), 5,844,363 (Gu et al.), 5,872,355 (Hueschen), 5,902,688 (Antoniadis et al.), and 5,948,552 (Antoniadis et al.), which are incorporated herein by reference, disclose various OLED structures.

The use of OLEDs in flat panel displays and other information display formats is limited by the poor environmental stability of the devices. G.Gustafson, Y.Cao, G.M.Treacy, F.Klavetter, N.Colaneri, and A.J.Heeger, Nature, Vol. 35, 11 June 1992, pages 477-479. Humidity and oxygen significantly reduce the useful life of most OLEDs. As a result, these devices are typically fabricated on glass substrates with glass covers laminated on top of the OLED and with the edges sealed to exclude water and oxygen from the active layers. U.S. Patent No. 5,872,355 discloses the use of a polymer such as saran to seal the device. The water vapor permeation rates (WVTR) required to provide sufficient lifetime for OLEDs is calculated to be approximately 10^{-6} $g/m^2/day$. The best polymer films (such as saran) have WVTR values that are 5 orders of magnitude too high to be considered for OLED encapsulation.

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Furthermore, saran cannot be deposited using flash evaporation, condensation, and in situ polymerization within a vacuum chamber.

Thus, there is a need for an improved lightweight, barrier construction which can be used to encapsulate the OLED and prevent the deterioration caused by permeation of oxygen and water vapor and for a method of making such an encapsulated OLED.

SUMMARY OF THE INVENTION

These needs are met by the present invention, which is an encapsulated organic light emitting device (OLED). The device includes a first barrier stack comprising at least one first barrier layer and at least one first polymer layer. There is an organic light emitting layer stack adjacent to the first barrier stack. A second barrier stack is adjacent to the organic light emitting layer stack. The second barrier stack has at least one second barrier layer and at least one second polymer layer. The device optionally includes at least one first intermediate barrier stack located between the substrate and the first barrier stack, and/or at least one second intermediate barrier stack located between the organic light emitting layer stack and either the first or second barrier stacks. The first and second intermediate barrier stacks include at least one polymer layer and at least one barrier layer.

Preferably, either one or both of the first and second barrier layers of the first and second barrier stacks is substantially transparent. At least one of the first and second barrier layers preferably comprises a material selected from metal oxides, metal nitrides, metal carbides, metal oxynitrides, and combinations thereof. The metal oxides are preferably selected from silica, alumina, titania, indium oxide, tin oxide, indium tin oxide, and combinations thereof, the metal nitrides are preferably selected from aluminum nitride, silicon nitride, and combinations thereof, the metal carbide is preferably silicon carbide, and the metal oxynitride is preferably silicon oxynitride.

The encapsulated OLED can also include a substrate adjacent to the first barrier stack on a side opposite to the organic light emitting layer stack. The

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substrate can be either a flexible substrate or a rigid substrate. It is preferably a flexible substrate material, which can be polymers, metals, paper, fabric, and combinations thereof. The rigid substrate is preferably glass, metal, or silicon. If a rigid substrate is used, it can be removed prior to use if desired.

The polymer layers of the first and second barrier stacks and the polymer layers in the first and second intermediate barrier stacks are preferably acrylate-containing polymers (as used herein, the term acrylate-containing polymer includes acrylate-containing polymers, methacrylate-containing polymers, and combinations thereof). The polymer layers in the first and/or the second barrier stacks can be the same or different.

The organic light emitting layer stack preferably comprises a first electrode, an electroluminescent layer, and a second electrode. The electroluminescent layer preferably includes a hole transporting layer, and an electron transporting layer, as is known in the art and shown in the patents whose disclosures have been specifically incorporated herein.

The invention also involves a method of making the encapsulated organic light emitting device. The method includes forming a first barrier stack comprising at least one first barrier layer and at least one first polymer layer, forming an organic light emitting layer stack, forming a second barrier stack comprising at least one second barrier layer and at least one second polymer layer, and combining the first barrier stack, the organic light emitting layer stack, and the second barrier stack to form the encapsulated organic light emitting device. Intermediate barrier stacks can optionally be formed. The layers are preferably formed by vacuum deposition.

The organic light emitting layer stack can be combined with the first barrier stack and/or the second barrier stack by laminating them together. Alternatively, they can be combined simultaneously with forming by depositing one layer on the other.

In an alternative embodiment, the invention involves an encapsulated organic light emitting device having a substrate, an organic light emitting layer stack adjacent to the substrate, and a barrier stack comprising at least one barrier layer and at least one polymer layer, the barrier stack adjacent to the

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organic light emitting layer stack. The invention also involves methods of making the encapsulated organic light emitting device. One method includes providing a substrate having an organic light emitting layer stack thereon, and laminating a barrier stack comprising at least one barrier layer and at least one polymer layer over the organic light emitting layer stack to encapsulate the organic light emitting barrier layer stack. The barrier stack is preferably laminated (edge sealed) using an adhesive, but other methods can be used including heat.

Another method involves vacuum depositing the barrier stack on a substrate having an organic light emitting layer stack thereon. Still another method involves providing a substrate with an organic light emitting layer stack thereon, vacuum depositing at least one barrier layer on the organic light emitting layer stack, and depositing at least one first polymer layer on the at least one barrier layer. At least one second polymer layer can be deposited on the organic light emitting layer stack before the barrier layer is deposited.

Accordingly, it is an object of the present invention to provide an encapsulated OLED, and to provide a method of making such a device.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-section of one embodiment of the encapsulated OLED of the present invention.

Fig. 2 is a cross-section of an alternate embodiment of the encapsulated OLED of the present invention.

Fig. 3 is a cross-section of an embodiment of an encapsulated OLED of the present invention.

DESCRIPTION OF THE INVENTION

One embodiment of the present invention is an encapsulated OLED 100 as shown in Fig. 1. The encapsulated OLED 100 includes substrate 105, a first barrier stack 110, an organic light emitting layer stack 120, and a second barrier stack 130. The first barrier stack 110 has a first barrier layer 140 and two

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polymer layers 150, 160. The second encapsulation layer 130 includes a second barrier layer 170 and two polymer layers 180, 190.

Although the Figures show barrier stacks with a single polymer layer on both sides of a single barrier layer, the barrier stacks can have one or more polymer layers and one or more barrier layers. There could be one polymer layer and one barrier layer, there could be multiple polymer layers on one side of one or more barrier layers, or there could be one or more polymer layers on both sides of one or more barrier layers. The important feature is that the barrier stack have at least one polymer layer and at least one barrier layer.

The organic light emitting layer stack 120 includes a first electrode layer 200, an electroluminescent layer 210, and a second electrode 220. The electroluminscent layer 210 can include a hole transport layer 230, and an electron transport layer 235. The exact form and composition of the organic light emitting layer stack is not critical. The organic light emitting layer stack includes first and second electrode layers on opposite sides of one or more active layers. The electrode layers are connected to a power source. At least one of the electrodes is transparent. The electroluminescent layer may be multiple layers as shown, or a single layer. The electroluminescent layer typically includes a hole injection layer, a hole transport layer, an electron transport layer, and an emissive layer, and combinations thereof. Additional layers may also be present, including dielectric layers. The organic light emitting layer stack can be made using known techniques, such as those described in U.S. Patent Nos. 5,629,389 (Roitman et al.), 5,844,363 (Gu et al.), 5,872,355 (Hueschen), 5,902,688 (Antoniadis et al.), and 5,948,552 (Antoniadis et al.), which have been incorporated herein by reference.

The present invention is compatible with organic light emitting layer stacks made with light emitting polymers and small molecules.

In the alternate embodiment shown in Fig. 2, the encapsulated OLED 300 also includes a first intermediate barrier stack 240 and a second intermediate barrier stack 270. The first intermediate barrier stack is located between the substrate 105 and the first barrier stack 110, and it includes a polymer layer 250 and a barrier layer 260. The second intermediate barrier stack 270 includes a

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polymer layer 280 and a barrier layer 290. The second intermediate barrier stack 270 is located between the organic light emitting layer stack 120 and the second barrier stack 130. Alternatively, the second intermediate layer could be located between the first barrier layer and the organic light emitting layer stack. In addition, there could be multiple first intermediate barrier stacks on top of one another to provide enhanced barrier protection. Similarly, there could be multiple second intermediate barrier stacks on top of one another. The order of the barrier and polymer layers in the intermediate barrier stacks is not critical. It depends on where the intermediate barrier stack is located and what layers are next to them.

The encapsulated OLED can be made by forming the first barrier stack 110, the organic light emitting layer stack 120, and the second barrier stack 130. The stacks are combined to form the encapsulated OLED.

Preferably, the stacks are combined by forming them using vacuum deposition. In this method, one layer is vacuum deposited on the previous layer, thereby combining the layers simultaneously with forming them. Alternatively, the organic light emitting layer stack can be combined with the first and second barrier stacks by laminating it between the first and second barrier stacks and sealing it along the edges with adhesive, glue, or the like, or by heating. The first and second barrier stacks include at least one barrier layer and at least one polymer layer. If a polymer/barrier/polymer structure is desired, it can be preferably formed as follows. These barrier stacks can be formed by depositing a layer of polymer, for example an acrylate-containing polymer, onto a substrate or previous layer. Preferably, an acrylate-containing monomer, oligomer or resin (as used herein, the term acrylate-containing monomer, oligomer, or resin includes acrylate-containing monomers, oligomers, and resins, methacrylate-containing monomers, oligomers, and resins, and combinations thereof) is deposited and then polymerized *in situ* to form the polymer layer. The acrylate-containing polymer layer is then coated with a barrier layer. Another polymer layer is deposited onto the barrier layer. U.S. Patent Nos. 5,440,446 and 5,725,909, which are incorporated herein by reference, describe methods of depositing thin film, barrier stacks.

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The barrier stacks are preferably vacuum deposited. Vacuum deposition includes flash evaporation of acrylate-containing monomer, oligomer, or resin with *in situ* polymerization under vacuum, plasma deposition and polymerization of acrylate-containing monomers, oligomer, or resin, as well as vacuum deposition of the barrier layers by sputtering, chemical vapor deposition, plasma enhanced chemical vapor deposition, evaporation, sublimation, electron cyclotron resonance-plasma enhanced vapor deposition (ECR-PECVD), and combinations thereof.

It is critical to protect the integrity of the barrier layer to avoid the formation of defects and/or microcracks in the deposited layer. The encapsulated OLED is preferably manufactured so that the barrier layers are not directly contacted by any equipment, such as rollers in a web coating system, to avoid defects that may be caused by abrasion over a roll or roller. This can be accomplished by designing the deposition system such that a set of layers of polymer/barrier/polymer are deposited prior to contacting or touching any handling equipment.

The substrate can be flexible or rigid. The flexible substrate may be any flexible material, including, but not limited to, polymers, for example polyethlyene terephthalate (PET), polyethylene naphthalate (PEN), or high temperature polymers such as polyether sulfone (PES), polyimides, or Transphan™ (a high Tg cyclic olefin polymer available from Lofo High Tech Film, GMBH of Weil am Rhein, Germany), metal, paper, fabric, and combinations thereof. The rigid substrate is preferably glass, metal, or silicon. If a flexible, encapsulated OLED is desired and a rigid substrate was used during manufacture, the rigid substrate is preferably removed prior to use.

The polymer layers of the first and second barrier stacks and the polymer layers of the first and second intermediate barrier stacks are preferably acrylate-containing monomer, oligomer or resin, and combinations thereof. The polymer layers of the first and second barrier stacks and first and second intermediate stacks can be the same or they can be different. In addition, the polymer layers within the each barrier stack can be the same or different.

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The barrier layers in the barrier stacks and the intermediate barrier stacks may be any barrier material. The barrier materials in the first and second barrier stacks and first and second intermediate barrier stacks can be the same or different. In addition, multiple layers of the same or different barrier layers can be used in a stack. Preferred transparent barrier materials include, but are not limited to, metal oxides, metal nitrides, metal carbides, metal oxynitrides, and combinations thereof. The metal oxides are preferably selected from silica, alumina, titania, indium oxide, tin oxide, indium tin oxide, and combinations thereof, the metal nitrides are preferably selected from aluminum nitride, silicon nitride, and combinations thereof, the metal carbide is preferably silicon carbide, and the metal oxynitride is preferably silicon oxynitride.

Since only one side of the device must be transparent, only one of the barrier layers must be transparent. In this situation, the barrier layer on the opposite side could be an opaque barrier material, including, but not limited to, metal, ceramic or polymer.

An alternate encapsulated OLED is shown in Fig. 3. The encapsulated OLED 400 has a substrate 105 on which is fabricated an organic light emitting layer stack 120. A barrier stack 130 is deposited conformally over the organic light emitting layer stack 120, encapsulating it. The polymer layers in the barrier stack can be deposited in vacuum or by using atmospheric processes such as spin coating and/or spraying. A preferred method of forming the barrier stack is flash evaporating acrylate-containing monomers, oligomers or resins, condensing on the OLED layer stack, and polymerizing in-situ in a vacuum chamber. The barrier layer is then deposited on the polymer layer using conventional vacuum processes such as evaporation, sputtering, CVD, PECVD or ECR-PECVD. A second polymer layer is then deposited on the barrier layer using the process described above.

Alternatively, the OLED device could also be encapsulated by laminating a lid structure, containing the barrier stack, to the substrate over the organic light emitting layer structure. The lamination can be performed using either adhesive, or glue, or the like, or by heating. The encapsulated OLED could also include an

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intermediate barrier stack 270 as shown. If the substrate is transparent, then the barrier material could be opaque, or vice versa, as discussed above.

A single pass, roll-to-roll, vacuum deposition of a three layer combination on a PET substrate, i.e., PET substrate/polymer layer/barrier layer/polymer layer, can be more than five orders of magnitude less permeable to oxygen and water vapor than a single oxide layer on PET alone. See J.D.Affinito, M.E.Gross, C.A.Coronado, G.L.Graff, E.N.Greenwell, and P.M.Martin, Polymer-Oxide Transparent Barrier Layers Produced Using PML Process, 39th Annual Technical Conference Proceedings of the Society of Vacuum Coaters, Vacuum Web Coating Session, 1996, pages 392-397; J.D.Affinito, S.Eufinger, M.E.Gross, G.L.Graff, and P.M.Martin, PML/Oxide/PML Barrier Layer Performance Differences Arising From Use of UV or Electron Beam Polymerization of the PML Layers, Thin Solid Films, Vol.308, 1997, pages 19-25. This is in spite of the fact that the effect on the permeation rate of the polymer multilayers (PML) layers alone, without the barrier layer (oxide, metal, nitride, oxynitride) layer, is barely measurable. It is believed that the improvement in barrier properties is due to two factors. First, permeation rates in the roll-to-roll coated oxide-only layers were found to be conductance limited by defects in the oxide layer that arose during deposition and when the coated substrate was wound up over system idlers/rollers. Asperities (high points) in the underlying substrate are replicated in the deposited inorganic barrier layer. These features are subject to mechanical damage during web handling/take-up, and can lead to the formation of defects in the deposited film. These defects seriously limit the ultimate barrier performance of the films. In the single pass, polymer/barrier/polymer process, the first acrylic layer planarizes the substrate and provides an ideal surface for subsequent deposition of the inorganic barrier thin film. The second polymer layer provides a robust "protective" film that minimizes damage to the barrier layer and also planarizes the structure for subsequent barrier layer (or organic light emitting layer stack) deposition. The intermediate polymer layers also decouple defects that exist in adjacent inorganic barrier layers, thus creating a tortuous path for gas diffusion. The permeability of the barrier stacks used in the present invention is shown below.

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Table 1

Sample	Oxygen Permeation Rate ($cc/m^2/day$)		Water vapor Permeation ($g/m^2/day$)+
	23°C*	38°C+	38°C+
1-barrier stack	<0.005	<0.005	0.46
2- barier stacks	<0.005	<0.005	<0.005
5-barrier stacks	<0.005	<0.005	<0.005

* 38°C, 90% RH, 100% O_2
+ 38°C, 100% RH

NOTE: Permeation rates of <0.005 are below the detection limits of current instrumentation (Mocon OxTran 2/20L).

As can be seen from the data in Table 1, the barrier stacks used in the present invention provide exceptional environmental protection, which was previously unavailable with polymers.

We have also compared the performance of OLED devices (fabricated on glass and silicon) before and after encapsulation using the barrier stacks of the present invention. After encapsulation, the current density-versus-voltage and brightness-versus-current density characteristics were identical (within experimental error) to the measured behavior of the pristine (unencapsulated) devices. This shows that the barrier stacks and deposition methods are compatible with OLED device manufacturing.

Thus, the present invention provides a barrier stack with the exceptional barrier properties necessary for hermetic sealing of an OLED. It permits the production of an encapsulated OLED.

While certain representative embodiments and details have been shown for purposes of illustrating the invention, it will be apparent to those skilled in the art that various changes in the compositions and methods disclosed herein may be made without departing from the scope of the invention, which is defined in the appended claims.

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What is claimed is:

1. An encapsulated organic light emitting device comprising:

a first barrier stack comprising at least one first barrier layer and at least one first polymer layer;

an organic light emitting layer stack adjacent to the first barrier stack; and

a second barrier stack comprising at least one second barrier layer and at least one second polymer layer, the second barrier stack adjacent to the organic light emitting layer stack.

2. The encapsulated organic light emitting device of claim 1 further comprising a substrate adjacent to the first barrier stack on a side opposite to the organic light emitting layer stack.

3. The encapsulated organic light emitting device of claim 2 further comprising at least one first intermediate barrier stack located between the substrate and the first barrier stack, the first intermediate barrier stack comprising at least one third polymer layer and at least one third barrier layer.

4. The encapsulated organic light emitting device of claim 1 further comprising at least one second intermediate barrier stack located between the organic light emitting layer stack and either the first or second barrier stacks, the second intermediate barrier stack comprising at least one fourth polymer layer and at least one fourth barrier layer.

5. The encapsulated organic light emitting device of claim 1 wherein the at least one first barrier layer is substantially transparent.

6. The encapsulated organic light emitting device of claim 1 wherein the at least one second barrier layer is substantially transparent.

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7. The encapsulated organic light emitting device of claim 1 wherein at least one of the at least one first and second barrier layers comprise a material selected from metal oxides, metal nitrides, metal carbides, metal oxynitrides, and combinations thereof.

8. The encapsulated organic light emitting device of claim 7 wherein the metal oxides are selected from silica, alumina, titania, indium oxide, tin oxide, indium tin oxide, and combinations thereof.

9. The encapsulated organic light emitting device of claim 7 wherein the metal nitrides are selected from aluminum nitride, silicon nitride, and combinations thereof.

10. The encapsulated organic light emitting device of claim 1 wherein the at least one first barrier layer is substantially opaque.

11. The encapsulated organic light emitting device of claim 1 wherein the at least one second barrier layer is substantially opaque.

12. The encapsulated organic light emitting device of claim 1 wherein at least one of the at least one first and second barrier layers is selected from opaque metals, opaque polymers, and opaque ceramics.

13. The encapsulated organic light emitting device of claim 2 wherein the substrate comprises a flexible substrate material.

14. The encapsulated organic light emitting device of claim 13 wherein the flexible substrate material is selected from polymers, metals, paper, fabric, and combinations thereof.

15. The encapsulated organic light emitting device of claim 2 wherein the substrate comprises a rigid substrate material.

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16. The encapsulated organic light emitting device of claim 15 wherein the rigid substrate material is selected from glass, metal, and silicon.

17. The encapsulated organic light emitting device of claim 1 wherein at least one of the at least one first polymer layers comprises an acrylate-containing polymer.

18. The encapsulated organic light emitting device of claim 1 wherein at least one of the at least one second polymer layers comprises an acrylate-containing polymer.

19. The encapsulated organic light emitting device of claim 3 wherein at least one of the at least one third polymer layers comprises an acrylate-containing polymer.

20. The encapsulated organic light emitting device of claim 4 wherein at least one of the at least one fourth polymer layers comprises an acrylate-containing polymer.

21. The encapsulated organic light emitting device of claim 1 wherein the organic light emitting layer stack comprises a first electrode, an electroluminescent layer, and a second electrode.

22. The encapsulated organic light emitting device of claim 21 wherein the electroluminescent layer comprises a hole transporting layer, and an electron transporting layer.

23. A method of making an encapsulated organic light emitting device comprising:

forming a first barrier stack comprising at least one first barrier layer and at least one first polymer layer;

forming an organic light emitting layer stack;

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forming a second barrier stack comprising at least one second barrier layer and at least one second polymer layer; and

combining the first barrier stack, the organic light emitting layer stack adjacent to the first barrier stack, and the second barrier stack adjacent to the organic light emitting layer stack to form the encapsulated organic light emitting device.

24. The method of claim 23 further comprising providing a substrate and forming the first barrier stack on the substrate.

25. The method of claim 24 further comprising placing at least one first intermediate barrier stack comprising at least one third polymer layer and at least one third barrier layer between the substrate and the first barrier stack.

26. The method of claim 23 further comprising placing at least one second intermediate barrier stack comprising at least one fourth polymer layer and at least one fourth barrier layer between the organic light emitting layer stack and either the first or second barrier stacks.

27. The method of claim 23 wherein the organic light emitting layer stack is combined with the first barrier stack by laminating the organic light emitting layer stack to the first barrier stack.

28. The method of claim 23 wherein the organic light emitting layer stack is combined with the first barrier stack simultaneously with forming by depositing the organic light emitting layer stack on the first barrier stack.

29. The method of claim 23 wherein the second barrier stack is combined with the organic light emitting layer stack by laminating the second barrier stack over the organic light emitting layer stack.

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30. The method of claim 23 wherein the second barrier stack is combined with the organic light emitting layer stack simultaneously with forming by depositing the second barrier stack on the organic light emitting layer stack.

31. The method of claim 24 wherein the substrate comprises a flexible material.

32. The method of claim 24 wherein the substrate comprises a rigid material.

33. The method of claim 24 wherein the substrate is removed from the encapsulated organic light emitting device.

34. The method of claim 23 wherein the first barrier stack is formed by vacuum deposition.

35. The method of claim 23 wherein the organic light emitting layer stack is formed by vacuum deposition.

36. The method of claim 23 wherein the second barrier stack is formed by vacuum deposition.

37. The method of claim 23 wherein at least one of the at least one first and second barrier layers is substantially transparent.

38. The method of claim 23 wherein at least one of the first and second barrier layers comprises a material selected from metal oxides, metal nitrides, metal carbides, metal oxynitrides, and combinations thereof.

39. The method of claim 38 wherein the metal oxides are selected from silica, alumina, titania, indium oxide, tin oxide, indium tin oxide, and combinations thereof.

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40. The method of claim 38 wherein the metal nitrides are selected from aluminum nitride, silicon nitride, and combinations thereof.

41. The method of claim 23 wherein at least one of the at least one first and second barrier layers is substantially opaque.

42. The method of claim 23 wherein at least one of the at least one first and second barrier layers is selected from opaque metals, opaque polymers, and opaque ceramics.

43. The method of claim 31 wherein the flexible substrate material is selected from polymers, metals, paper, fabric, and combinations thereof.

44. The method of claim 32 wherein the rigid substrate material is selected from glass, metal, and silicon.

45. The method of claim 23 wherein at least one of the at least one first and second pairs of polymer layers comprises an acrylate-containing polymer.

46. The method of claim 25 wherein the third polymer layer comprises an acrylate-containing polymer.

47. The method of claim 26 wherein the fourth polymer layer comprises an acrylate-containing polymer.

48. An encapsulated organic light emitting device comprising:

a first intermediate barrier stack comprising at least one polymer layer and at least one barrier layer ;

a first barrier stack comprising at least one first barrier layer and at least one first polymer layer adjacent to the first intermediate barrier stack;

an organic light emitting layer stack adjacent to the first barrier stack;

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a second intermediate barrier stack comprising at least one polymer layer and at least one barrier layer, the second intermediate barrier stack adjacent to the organic light emitting layer stack; and

a second barrier stack comprising at least one second barrier layer and at least one second polymer layer, the second barrier stack adjacent to the second intermediate barrier stack.

49. The encapsulated organic light emitting device of claim 48 further comprising a substrate adjacent to the first intermediate barrier stack on a side opposite to the first barrier stack.

50. A method of making an encapsulated organic light emitting device comprising:

forming a first intermediate barrier stack comprising at least one polymer layer and at least one barrier layer;

forming a first barrier stack comprising at least one first barrier layer and at least one first polymer layer adjacent to the first intermediate barrier stack;

forming an organic light emitting layer stack adjacent to the first barrier stack;

forming a second intermediate barrier stack comprising at least one polymer layer and at least one barrier layer adjacent to the organic light emitting layer stack; and

forming a second barrier stack comprising at least one second barrier layer and at least one second polymer layer adjacent to the second intermediate barrier stack; and

combining the first intermediate barrier stack, the first barrier stack, the organic light emitting layer stack, the second intermediate barrier stack, and the second barrier stack to form the encapsulated organic light emitting device.

51. The method of claim 50 wherein the first intermediate barrier stack is formed by vacuum deposition.

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52. The method of claim 50 wherein the first barrier stack is formed by vacuum deposition.

53. The method of claim 50 wherein the organic light emitting layer stack is formed by vacuum deposition.

54. The method of claim 50 wherein the second intermediate barrier stack is formed by vacuum deposition.

55. The method of claim 50 wherein the second barrier stack is formed by vacuum deposition.

56. An encapsulated organic light emitting device comprising:

a substrate;

an organic light emitting layer stack adjacent to the substrate;

a barrier stack comprising at least one barrier layer and at least one polymer layer, the barrier stack adjacent to the organic light emitting layer stack.

57. The encapsulated organic light emitting device of claim 56 further comprising an intermediate barrier stack located between the organic light emitting layer stack and the barrier stack, the intermediate barrier stack comprising at least one polymer layer and at least one barrier layer.

58. The encapsulated organic light emitting device of claim 56 wherein the at least one barrier stack is substantially transparent.

59. The encapsulated organic light emitting device of claim 56 wherein the at least one barrier layer comprises a material selected from metal oxides, metal nitrides, metal carbides, metal oxynitrides, and combinations thereof.

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60. The encapsulated organic light emitting device of claim 59 wherein the metal oxides are selected from silica, alumina, titania, indium oxide, tin oxide, indium tin oxide, and combinations thereof.

61. The encapsulated organic light emitting device of claim 59 wherein the metal nitrides are selected from aluminum nitride, silicon nitride, and combinations thereof.

62. The encapsulated organic light emitting device of claim 56 wherein the at least one barrier layer is substantially opaque.

63. The encapsulated organic light emitting device of claim 56 wherein the at least one barrier layer is selected from opaque metals, opaque polymers, and opaque ceramics.

64. The encapsulated organic light emitting device of claim 56 wherein at least one of the at least one polymer layers comprises an acrylate-containing polymer.

65. The encapsulated organic light emitting device of claim 56 wherein the substrate comprises a rigid substrate material.

66. The encapsulated organic light emitting device of claim 65 wherein the rigid substrate material is selected from glass, metal, and silicon.

67. The encapsulated organic light emitting device of claim 56 wherein the substrate comprises a flexible substrate material.

68. The encapsulated organic light emitting device of claim 67 wherein the flexible substrate material is selected from polymers, metals, paper, fabric, and combinations thereof.

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69. A method of making an encapsulated organic light emitting device comprising:

providing a substrate having an organic light emitting layer stack thereon; and

vacuum depositing a barrier stack comprising at least one barrier layer and at least one polymer layer over the organic light emitting layer stack to encapsulate the organic light emitting layer stack.

70. The method of claim 69 further comprising depositing an intermediate barrier layer stack comprising at least one polymer layer and at least one barrier layer on the organic light emitting layer stack prior to vacuum depositing the barrier stack.

71. A method of making an encapsulated organic light emitting device comprising:

providing a substrate having an organic light emitting layer stack thereon;

vacuum depositing at least one barrier layer over theorganic light emitting layer stack;

depositing at least one first polymer layer over the at least one barrier layer.

72. The method of claim 71 further comprising depositing at least one second polymer layer over the organic light emitting layer stack prior to vacuum depositing the at least one barrier layer.

73. The method of claim 71 further comprising depositing an intermediate barrier layer stack comprising at least one polymer layer and at least one barrier layer on the organic light emitting layer stack prior to depositing the at least one barrier layer.

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74. The method of claim 71 wherein at least one of the at least one first polymer layers is deposited using a process at atmospheric pressure.

75. The method of claim 74 wherein the process at atmospheric pressure is selected from spin coating and spraying.

76. The process of 71 wherein at least one of the at least one first polymer layers is deposited using a vacuum process.

77. The method of claim 72 wherein at least one of the at least one second polymer layers is deposited using a process at atmospheric pressure.

78. A method of making an encapsulated organic light emitting device comprising:

providing a substrate having an organic light emitting layer stack thereon; and

laminating a barrier stack comprising at least one barrier layer and at least one polymer layer over the organic light emitting layer stack to encapsulate the organic light emitting layer stack.

79. The method of claim 78 wherein the barrier stack is laminated using an adhesive.

80. The method of claim 78 wherein the barrier stack is laminated using heat.

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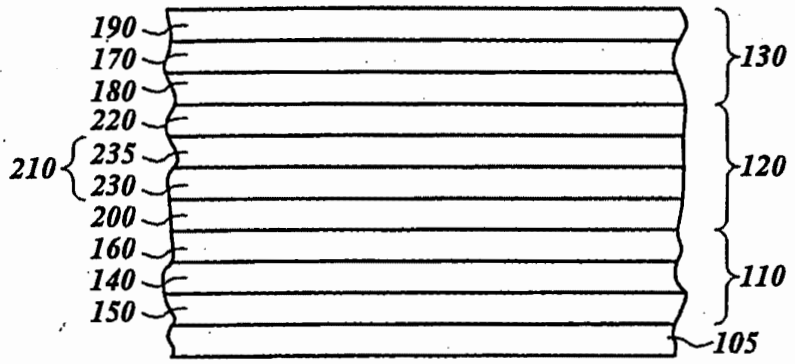


Fig. 1

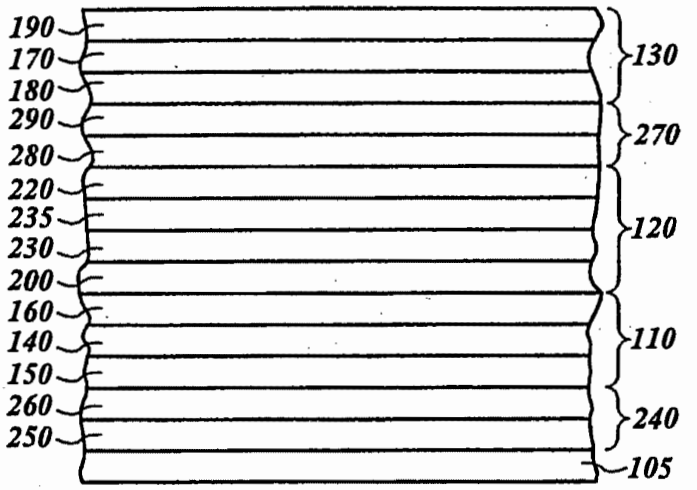


Fig. 2

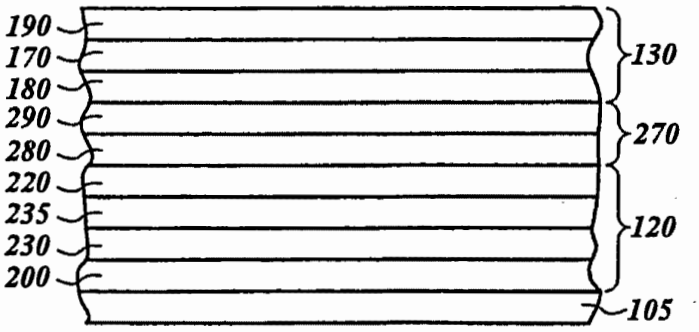


Fig. 3

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INTERNATIONAL SEARCH REPORT

ternational Application No
PCT/US 99/29853

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L51/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 757 126 A (HARVEY III THOMAS B ET AL) 26 May 1998 (1998-05-26) the whole document	1-5,7-9, 11-14, 21-26, 28,30, 31,34, 35, 37-43, 48-53, 56,57, 62,63, 67,68
Y		1-9, 11-14, 21-31, 34,35, 37-43, 48-53, 56-63,

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
22 February 2000	03/03/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	De Laere, A

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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A		67,68, 78-80 10, 17-20, 36, 45-47, 54,55, 64,69-77
X	DE 196 03 746 A (BOSCH GMBH ROBERT) 24 April 1997 (1997-04-24) the whole document	56, 58-63, 67,68, 78-80
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A		10,36, 55,69, 71,72, 74-77
A	AFFINITO J D ET AL: "PML/oxide/PML barrier layer performance differences arising from use of UV or electron beam polymerization of the PML layers" THIN SOLID FILMS,CH,ELSEVIER-SEQUOIA S.A. LAUSANNE, vol. 308-309, no. 1-4, 31 October 1997 (1997-10-31), pages 19-25, XP004110238 ISSN: 0040-6090 cited in the application the whole document	1,5,7,8, 13,14, 17,23, 24,31, 34, 37-39, 43, 48-50, 52,56, 58-60, 64, 67-69, 71,72, 76,78

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INTERNATIONAL SEARCH REPORT

ternational Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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E	EP 0 977 469 A (HEWLETT PACKARD CO) 2 February 2000 (2000-02-02) the whole document	1,2,5-9, 13,14, 17,18, 21-24, 28,30, 31, 34-40, 43,45, 56, 58-61, 64, 67-69, 71,72,76

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 99/29853

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DEUTSCHES PATENTAMT

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20.10.95 DE 195390504

(71) Anmelder:
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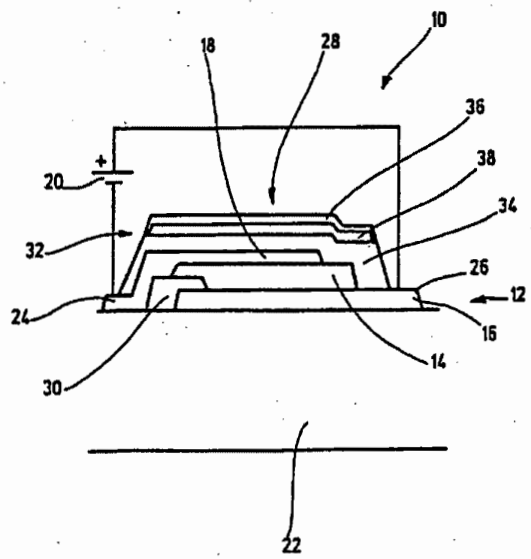
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JP 07014675 A (Engl. Abstract);
JP 07169567 A (Engl. Abstract);
JP 07147189 A (Engl. Abstract);
JP 07153571 A (Engl. Abstract);

Prüfungsantrag gem. § 44 PatG ist gestellt

(54) Elektrolumineszierendes Schichtsystem

(57) Die Erfindung betrifft eine elektrolumineszierende Vorrichtung mit einem elektrolumineszierenden Schichtsystem aus einem zwischen zwei mit einer Gleichspannungsquelle verbindbaren Elektroden angeordneten lichtemittierenden organischen Material, wobei eine erste Elektrode eine löcherinjizierende Elektrode (Anode) und eine zweite Elektrode eine elektroneninjizierende Elektrode (Kathode) ist, und einer Kapselung.
Es ist vorgesehen, daß die Kapselung (28, 28') aus einem Mehrschichtsystem (32) besteht.



DE 196 03 746 A1

Die folgenden Angaben sind den vom Anmelder eingereichten Unterlagen entnommen

BUNDESDRUCKEREI 02. 97 702 017/455

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Beschreibung

Die Erfindung betrifft ein elektrolumineszierendes Schichtsystem nach dem Oberbegriff des Anspruchs 1.

Stand der Technik

Elektrolumineszierende Schichtsysteme sind bekannt. Bei diesen werden entweder anorganische oder organische Substanzen verwendet, die mittels einer elektrischen Spannung zum Aussenden von Lichtstrahlen anregbar sind. Die lichtemittierenden Substanzen sind hierbei beispielsweise zwischen flächenhaften Elektroden angeordnet, wobei eine erste Elektrode als löcherinjizierende Elektrode (Anode) und eine zweite Elektrode als elektroneninjizierende Elektrode (Kathode) ausgebildet ist. Wird die lichtemittierende Substanz von einem organischen Material gebildet, kann die Anregung über eine Gleichspannungsquelle erfolgen. Hierbei ist die Anode mit dem Pluspol der Gleichspannungsquelle und die Kathode mit dem Minuspol der Gleichspannungsquelle verbunden.

Da bekanntermaßen die Grenzflächen zwischen den Elektroden und dem lichtemittierenden organischen Material beziehungsweise das organische Material selbst unter dem Einfluß von Sauerstoff und/oder Wasser degradieren, ist es notwendig, zur Langzeitstabilisierung des elektrolumineszierenden Schichtsystems einen entsprechenden Schutz vorzusehen.

Hierzu ist beispielsweise aus der EP 0 468 440 B1 bekannt, die Kathode mit einer Abdeckschicht zu versehen. Die Abdeckschicht, die beispielsweise aus reinen Metallen, aus codeponierten Metallkompositen oder aus codeponierten Kompositen, die metallische und organischen Bestandteile aufweisen, besteht, hat den Nachteil, das beispielsweise bei strukturierten Kathoden zur Erzeugung bestimmter Lichteffekte, die zwischen den Kathoden vorhandenen Bereiche nicht mit der Abdeckschicht geschützt sind.

Weiterhin ist aus Appl. Phys. Lett. 65 (1994) Seite 2922–2924 bekannt, die elektrolumineszierenden Schichtsysteme mittels einer Glasplatte zu kapseln, die beidseitig das elektrolumineszierende Schichtsystem schützt und an den Kanten verklebt ist. Hierbei ist nachteilig, daß die Kapselung unter einem Inertgas durchgeführt werden muß, damit der Raum zwischen der Rückseite der Kathode und der Glasplatte frei von Sauerstoff und Wasserstoff ist. Weiterhin ist nachteilig, daß die Glasplatte nicht flexibel ist und somit keine flexiblen elektrolumineszierenden Schichtsysteme herstellbar sind.

Vorteile der Erfindung

Die erfindungsgemäße elektrolumineszierende Vorrichtung mit den im Anspruch 1 genannten Merkmalen bietet demgegenüber den Vorteil, daß einerseits ein effizienter Schutz, der zwischen den Elektroden und dem organischen Material bestehenden Grenzschichten und des organischen Materials selbst gegen Sauerstoff und Wasser besteht, und das elektrolumineszierende Schichtsystem insgesamt flexibel hergestellt werden kann. Dadurch, daß die Kapselung aus einem Mehrschichtsystem besteht, wobei die Schichten des Mehrschichtsystems vorzugsweise flexibel sind und sich der Geometrie des eletrolumineszierenden Schichtsystems anpassen, ist es vorteilhaft möglich, ein insgesamt flächiges elektrolumineszierendes Schichtsystem zu schaffen, das einen flexiblen Aufbau und eine äußerst geringe Permeation von Sauerstoff und Wasser aufweist.

In bevorzugter Ausgestaltung der Erfindung ist vorgesehen, daß eine erste aus Kunststoff bestehende Schicht vorgesehen ist, die von einer zweiten, aus Metall, einer Metallegierung oder einem Metalloxid bestehenden Schicht überdeckt ist. Hierdurch kann eine Kapselung sehr vorteilhaft durch die Kombination von Kunststoffschicht und Metall- oder Metalloxidschicht vorgenommen werden. Die Metallschicht besteht bevorzugt aus einem Metall, das eine stabile Passivierungsschicht an der Oberfläche ausbildet, so daß auch eine Langzeitstabilität des elektrolumineszierenden Schichtsystems gegeben ist.

Weiterhin ist bevorzugt, wenn zwischen der Kunststoffschicht und der Metallschicht eine zusätzliche sogenannte Getterschicht vorgesehen ist. Hierdurch wird sehr vorteilhaft erreicht, daß durch die Getterschicht eventuell auftretende Reste an Sauerstoff oder Wasser gebunden werden können, so daß diese nicht zu einer Degradierung des organischen Materials beitragen können.

In weiterer bevorzugter Ausgestaltung der Erfindung ist vorgesehen, daß die Getterschicht zwischen zwei Kunststoffschichten eingebettet ist und eine äußere Kunststoffschicht vorzugsweise die Metallschicht trägt. Hierdurch wird sehr vorteilhaft erreicht, daß die Stabilität der Kapselung bei gleichzeitiger Wahrung ihrer Flexibilität erhöht werden kann.

Ferner ist eine Ausführungsform der Erfindung bevorzugt, bei der das elektrolumineszierende Schichtsystem auf einem flexiblen Trägersubstrat angeordnet ist und das Trägersubstrat vorzugsweise ebenfalls mit einer Kapselung aus einem Mehrschichtsystem versehen ist. Das Mehrschichtsystem zur Kapselung des Trägersubstrates besitzt vorzugsweise den gleichen Aufbau wie die Kapselung des elektrolumineszierenden Schichtsystems. Sowohl die Trägerschicht als auch die Kapselung der Trägerschicht sind vorzugsweise transparent oder semitransparent ausgebildet, so daß das von dem elektrolumineszierenden Schichtsystem erzeugte Licht abgestrahlt werden kann. Somit wird eine allseitige Kapselung des elektrolumineszierenden Schichtsystems erreicht, die insgesamt flexibel ausgebildet ist und eine äußerst geringe Permeation von Sauerstoff und Wasser aufweist.

In weiterer vorteilhafter Ausgestaltung der Erfindung ist vorgesehen, daß die Kapselung oder zumindest Teile der Kapselung aus einer separaten, die einzelnen Schichten der Kapselung aufweisenden Verbundfolie besteht, die anschließend auf das elektrolumineszierende Schichtsystem aufgebracht wird. Somit kann die Fertigung des elektrolumineszierenden Schichtsystems und die Fertigung der Kapselung separat durchgeführt werden, und es ist lediglich nur noch das Aufbringen der Verbundfolie auf das elektrolumineszierende Schichtsystem notwendig. Eine mechanische und/oder thermische Beanspruchung des elektrolumineszierenden Schichtsystems kann hierdurch während der Fertigung verringert werden.

Weitere vorteilhafte Ausgestaltungen der Erfindung ergeben sich aus den übrigen, in den Unteransprüchen genannten Merkmalen.

Zeichnung

Die Erfindung wird nachfolgend in Ausführungsbeispielen anhand der zugehörigen Zeichnungen näher er-

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läutert. Es zeigen:

Fig. 1 eine schematische Schnittdarstellung durch eine elektrolumineszierende Vorrichtung in einer ersten Ausführungsvariante;

Fig. 2 eine schematische Schnittdarstellung durch eine elektrolumineszierende Vorrichtung in einer zweiten Ausführungsvariante und

Fig. 3 eine schematische Schnittdarstellung durch eine elektrolumineszierende Vorrichtung nach einer dritten Ausführungsvariante.

Beschreibung der Ausführungsbeispiele

Die Fig. 1 zeigt eine allgemein mit 10 bezeichnete elektrolumineszierende Vorrichtung. Die Vorrichtung 10 weist ein elektrolumineszierendes Schichtsystem 12 auf, das von einem lichtemittierenden organischen Material 14, einer ersten Elektrode 16 und einer zweiten Elektrode 18 gebildet wird. Die Elektroden 16 und 18 sowie das organische Material 14 sind flächenhaft ausgebildet. Die Elektroden 16 und 18 sind mit einer Spannungsquelle 20, beispielsweise einer Gleichspannungsquelle, verbunden. Die Elektrode 16 ist hierbei mit dem Pluspol der Spannungsquelle 20 und die Elektrode 18 mit dem Minuspol der Spannungsquelle 20 verbunden.

Die Elektrode 16 besteht aus einem Material mit hoher Elektronenaustrittsarbeit. Die Elektrode 16 kann beispielsweise aus einem Metall oder einer metallischen Legierung oder einem Metalloxid, beispielsweise Indium-Zinnoxid (ITO), bestehen. Durch Verbinden der Elektrode 16 mit dem Pluspol der Spannungsquelle 20 ist diese als Anode geschaltet, wobei auf Grund der hohen Elektronenaustrittsarbeit, die beispielsweise größer als 4,5 eV ist, diese Löcher injiziert, die als Ladungsträger in das organische Material 14 transportiert werden.

Die zweite Elektrode 18 besteht aus einem Material mit niedriger Elektronenaustrittsarbeit, die beispielsweise kleiner als 4,5 eV ist. Die Elektrode 18 besteht aus einem elektrisch leitfähigen Material, beispielsweise aus einem Metall, einer Metallegierung oder einem Metalloxid. Die Elektrode 18 kann beispielsweise aus Aluminium, Indium, Magnesium, Kalzium, einer Magnesium-Silber-Legierung oder einer Magnesium-Indium-Legierung bestehen. Durch das Verbinden der Elektrode 18 mit dem Minuspol der Spannungsquelle 20 und gleichzeitigem Verbinden der Elektrode 16 mit dem Pluspol der Spannungsquelle, wirkt diese als Kathode und injiziert Elektronen in das lichtemittierende organische Material 14. Hierdurch kommt es in dem lichtemittierenden Material 14 zu einem Stromfluß zwischen den Elektroden 16 und 18, so daß die organischen Substanzen in dem Material 14 zum Erzeugen von Lichtquanten angeregt werden. Das elektrolumineszierende Schichtsystem 12 kann somit als Leuchtquelle verwendet werden.

Das verwendete lichtemittierende organische Material 14 enthält hierzu mindestens eine organische Verbindung, die unter Anlegen der Spannung in der Lage ist, Licht zu emittieren. Die Farbe des emittierten Lichtes wird hierbei durch die chemische Struktur der verwendeten organischen Substanz bestimmt. Als lichtemittierende organische Materialien 14 kommen beispielsweise Polymere, niedermolekulare organische Verbindungen, Monomere oder molekulardotierte Polymere in Betracht. Zwischen den Elektroden 16 und 18 können weitere — hier nicht dargestellte — Schichten angeordnet sein, die ebenfalls zur Lichtemission oder zu einem Ladungsträgertransport zu dem lichtemittierenden organischen Material 14 dienen.

Das elektrolumineszierende Schichtsystem 12 ist auf einen Träger 22 aufgebracht. Sowohl die als Anode geschaltete Elektrode 16 als auch der Träger 20 sind hierbei optisch transparent oder semitransparent, so daß das von dem lichtemittierenden organischen Material 14 erzeugte Licht von der gesamten Vorrichtung 10 nach außen abgestrahlt werden kann.

Wie der Darstellung in der Fig. 1 zu entnehmen ist, sind die Elektroden 16 und 18 sowie die das organische Material 14 ergebenden Schichten teilweise überlappend auf dem Träger 22 angeordnet, so daß die Anschlußbereiche 24 beziehungsweise 26 der Elektroden 18 beziehungsweise 16 auf dem Träger 22 aufliegen und seitlich aus einer noch zu erläuternden Kapselung 28 herausgeführt sind. Zwischen den Elektroden 16 und 18 ist hierbei ein Isolator 30 angeordnet, der beispielsweise aus Aluminiumoxid bestehen kann.

Die Kapselung 28 besteht aus einem Mehrschichtsystem 32, das eine erste Schicht 34 aus einem Kunststoff und eine zweite Schicht 36 aus einem Metall, einer Metallegierung oder einem Metalloxid aufweist. Die Kunststoffschicht 34 kann beispielsweise aus einem Acrylharz, Alkydharz, Epoxidharz, Polyurethanharz, EVOH, Polyester, PVC, PVDC, Polypropylen, PMMA oder anderen Polymeren und Lacken bestehen. Diese Kunststoffschicht wird auf das elektrolumineszierende Schichtsystem 12 beispielsweise durch Gießen, Aufschleudern, Aufdrucken oder Aufextrudieren aufgebracht. Darüber hinaus kann das elektrolumineszierende Schichtsystem 12 in ein entsprechendes Bad eingetaucht werden, so daß eine Tauchbeschichtung mit der Kunststoffschicht 34 erfolgt. Durch die Art des Aufbringens der Kunststoffschicht 34 ergibt sich, daß sich diese der Kontur des elektrolumineszierenden Schichtsystems 12 anpaßt und dieses somit allseitig — mit Ausnahme der Anschlußbereiche 26 und 24 — umgibt und somit einschließt. Die Kunststoffschicht 34 wird anschließend thermisch, chemisch oder strahlungsindiziert ausgehärtet beziehungsweise vernetzt, so daß sich eine stabile, jedoch flexible Haube ergibt.

Zwischen der Kunststoffschicht 34 und der Metallschicht 36 ist eine Getterschicht 38 aufgebracht. Die Getterschicht 38 besteht aus einem Material, das für Sauerstoff und Wasser eine bindende Wirkung entfaltet. Die Getterschicht 38 besteht beispielsweise aus einem Metall, das eine niedrigere oder ähnlichere Elektronenaustrittsarbeit als das Material der als Kathode geschalteten Elektrode 18 aufweist. Besteht die Elektrode 18 beispielsweise aus Magnesium, kann als Material für die Getterschicht 38 beispielsweise Kalzium, Lithium oder Strontium eingesetzt werden. Als Material für die Getterschicht 38 können Alkali-Metalle, Erdalkali-Metalle oder Seltene Erden Verwendung finden.

Nach weiteren Ausführungsbeispielen kann die Getterschicht 38 beispielsweise aus einem hygroskopischen Polymer, einer Mischung eines Binderpolymers und einer pulverförmigen hygroskopischen Substanz, beispielsweise Silica-Gel oder Kieselgel oder Zeolithen bestehen. Bei dieser Materialwahl kann die Getterschicht 38 beispielsweise mittels Gießen, Spin-Coating, Dip-Coating, Cap-Coating, Sieb-Druck oder Rakeln deponiert werden. Ferner kann die Getterschicht 38 beispielsweise aus aufgedampften hygroskopischen Materialien beziehungsweise Verbindungen, beispielweise Zinksulfid, Kupfersulfid, Lithiumchlorid bestehen, die als dünne Schicht auf die Kunststoffschicht 34 aufge-

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bracht werden.

Auf die Getterschicht 38 wird die zweite Schicht 36 aufgebracht. Die Schicht 36 ist hier so ausgewählt, daß die Getterschicht 38 vollkommen umschlossen wird, so daß diese keinerlei Kontakt nach außen aufweist. Die zweite Schicht 36 besteht beispielsweise aus einem Metall, zum Beispiel Aluminium, Kupfer, Nickel, Chrom, Zinn oder Tantal, einer Metallegierung, zum Beispiel Nickel-Chrom oder einem Metalloxid, zum Beispiel Aluminiumoxid oder Siliciumoxid, oder einer Nitridschicht, zum Beispiel Aluminiumnitrid oder Siliciumnitrid. Die Schicht 36 kann vorzugsweise auf die zuvor aufgebrachte Kunststoffschicht 34 und die Getterschicht 36 aufgesputtert oder aufgedampft werden. Durch die Schicht 36, die den äußeren Abschluß der Kapselung 28 bildet, wird eine stabile Passivierung der gesamten Vorrichtung 10 erzielt, so daß diese gegenüber äußeren Einflüssen langzeitstabil ist. Die Metallschicht 36 kann zusätzlich mit einer in Fig. 1 nicht dargestellten weiteren Schicht passiviert werden. Hierzu kann beispielsweise eine Polymer-, eine Lack- oder eine organisch modifizierte Keramikschicht aufgebracht werden.

Etwa auftretende Reste beziehungsweise infolge von Leckage auftretendes Sauerstoff oder Wasser werden durch die Getterschicht 38 quasi aufgesogen, so daß diese nicht an die Grenzschichten zwischen den Elektroden 16 und 18 mit dem organischen Material 14 beziehungsweise direkt an das organische Material 14 kommen können. Das Mehrschichtsystem 32 besitzt somit eine äußerst geringe Permeation für Sauerstoff und Wasser.

Da das Mehrschichtsystem aus wenigstens zwei Schichten, nämlich der Kunststoffschicht 34 und der metallischen Deckschicht 36 oder bei zusätzlicher Anordnung der Getterschicht 38 aus drei Schichten von jeweils dünn aufgetragenden Materialien besteht, wird insgesamt die Flexibilität der Vorrichtung 10 im wesentlichen nicht beeinträchtigt. Somit ist es also möglich, trotz Anordnung der Kapselung 28 die elektrolumineszierende Vorrichtung nach der Herstellung, das heißt nach dem Aufbau der Schichtsysteme, den entsprechenden Anwendungen anzupassen.

In den Fig. 2 und 3 sind weitere Ausführungsvarianten der elektrolumineszierenden Vorrichtung 10 gezeigt, bei denen die Kapselung 38 einen modifizierten Aufbau besitzt. Gleiche Teile wie in Fig. 1 sind mit gleichen Bezugszeichen versehen und nicht nochmals erläutert.

Bei dem in Fig. 2 gezeigten Ausführungsbeispiel ist oberhalb der Getterschicht 38 eine weitere Kunststoffschicht 40 angeordnet. Die Kunststoffschicht 40 umschließt die Getterschicht 38 allseitig, mit Ausnahme der Berührungsfläche der Getterschicht 38 mit der Kunststoffschicht 34. Diese Kunststoffschicht 40 besitzt eine isolierende Wirkung und weist gleichzeitig eine ausreichende Flexibilität auf. Anstelle eines Kunststoffmaterials kann auch ein anderes geeignetes Material mit diesen Eigenschaften gewählt werden. Die Kunststoffschicht 40 besteht beispielsweise aus dem gleichen Material wie die bereits zu Fig. 1 ausführlich erläuterte Kunststoffschicht 34.

Auf die Metallschicht 36 kann bei der Verwendung bestimmter Metalle eine weitere Passivierungsschicht 42 aufgebracht sein. Diese Schicht 42 kann beispielsweise aus einem Polymer, einem Lack oder einer organisch modifizierten Keramik bestehen.

Insgesamt ist somit über dem elektrolumineszierenden Schichtsystem eine Kapselung 28 aus insgesamt fünf Teilschichten 34, 38, 40, 36 und 42 aufgebracht. Diese Teilschichten sind so ausgebildet, daß insgesamt eine Flexibilität der Kapselung 28 erhalten bleibt. Durch die Abfolge der Teilschichten wird gewährleistet, daß keinerlei Reste von Sauerstoff und/oder Wasser zu dem elektrolumineszierenden Schichtsystem 12, insbesondere zu dem organischen Material 14, gelangen können. Hierdurch wird eine Degradierung des organischen Materials 14 verhindert, so daß die elektrolumineszierende Vorrichtung 10 insgesamt eine Langzeitstabilität aufweist.

Bei der in Fig. 3 gezeigten Ausführungsvariante der elektrolumineszierenden Vorrichtung 10 ist zusätzlich auf Seiten des Trägers 22 eine weitere Kapselung 28' vorgesehen. Der Träger 22 besteht beispielsweise aus einem flexiblen Substrat, das eine gewisse Permeation von Wasser und Sauerstoff aufweist. Verwendung kann beispielsweise eine PET-Folie mit einer Stärke von ca. 100 µm finden. Die auf dem Träger 22 angeordnete Kapselung 28' besitzt im wesentlichen den gleichen Aufbau wie die Kapselung 28. An den Träger 22 schließt sich eine Getterschicht 44 an, die von einer Kunststoffschicht 46 überdeckt ist. Die Kunststoffschicht 46 dient der Stabilisierung der Getterschicht 44. Als Materialien für die Getterschicht 44 und die Kunststoffschicht 46 kommen die bereits erwähnten Materialien für die Getterschicht 38 beziehungsweise die Kunststoffschichten 34 und 40 in Betracht. Auf der Getterschicht 46 ist eine Schicht 48 aufgebracht, die impermeabel für Sauerstoff und Wasser ist. Die Schicht 48 besteht beispielsweise aus sehr dünn aufgetragenem Aluminium, Kupfer, Nikkel, Chrom, Zinn, Tantal, Gold oder einer Metallegierung. Ferner kann diese aus einer dünnen Oxidschicht, beispielsweise Siliziumoxid, Aluminiumoxid, Titanoxid, Tantaloxid oder Wismutoxid mit geeigneter Modifikation zum Erreichen der Impermeabilität für Wasser und Sauerstoff bestehen. Durch die Materialauswahl und das Auftragen in einer entsprechend geringen Dicke der Schicht 48, der Kunststoffschicht 46 und der Getterschicht 44 wird die optische Transparenz beziehungsweise Semitransparenz zum Abstrahlen des mittels des elektrolumineszierenden Schichtsystems 12 emittierten Lichtes gewährleistet. Mittels entsprechender Materialwahl kann sehr vorteilhaft gleichzeitig über die Kapselung 28' eine Entspiegelung der elektrolumineszierenden Vorrichtung 10 erreicht werden.

Allen drei Ausführungsbeispielen ist gemeinsam, daß die Kapselung 28 beziehungsweise 28' jeweils aus einem Schichtsystem 32 besteht. Die einzelnen Schichten des Schichtsystems 32 sind so gewählt, daß diese eine Flexibilität besitzen. Für eine Herstellung der mit der erfindungsgemäßen Kapselung 28 beziehungsweise 28' versehenen elektrolumineszierenden Vorrichtung 10 kann es vorteilhaft sein, wenn das gesamte Schichtsystem 32 oder auch nur Teilschichten des Schichtsystems 32, beispielsweise die Kunststoffschichten 34 und 40, mit der dazwischen angeordneten Getterschicht 38 separat als Verbundfolie vorgefertigt werden. Diese vorgefertigte Verbundfolie kann in einfacher Weise auf das elektrolumineszierende Schichtsystem 12 aufgebracht, beispielsweise aufgeklebt werden. Das Verkleben kann hierzu beispielsweise mit Heißsiegelklebstoffen, UV-härtenden Klebstoffen thermisch oder chemisch härtenden Klebstoffen erfolgen.

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Patentansprüche

1. Elektrolumineszierende Vorrichtung mit einem elektrolumineszierenden Schichtsystem aus einem zwischen zwei mit einer Gleichspannungsquelle verbindbaren Elektroden angeordneten lichtemittierenden organischen Material, wobei eine erste Elektrode eine löcherinjizierende Elektrode (Anode) und eine zweite Elektrode eine elektroneninjizierende Elektrode (Kathode) ist, und einer Kapselung, **dadurch gekennzeichnet**, daß die Kapselung (28, 28') aus einem Mehrschichtsystem (32) besteht.

2. Elektrolumineszierende Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, das das Mehrschichtsystem (32) flexible Schichten (34, 36, 38, 40, 42, 44, 46, 48) aufweist.

3. Elektrolumineszierende Vorrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß das Mehrschichtsystem (32) eine der Geometrie des elektrolumineszierenden Schichtsystems (12) angepaßte Kontur aufweist.

4. Elektrolumineszierende Vorrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß das Mehrschichtsystem (32) einseitig auf das Schichtsystem (12) aufgebracht ist und die Elektroden (16, 18) und das organische Material (14) umschließt.

5. Elektrolumineszierende Vorrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß das Mehrschichtsystem (32) aus wenigstens einer aus Kunststoff bestehenden Schicht (34, 40) und einer metallhaltigen Schicht (36) besteht.

6. Elektrolumineszierende Vorrichtung nach Anspruch 5, dadurch gekennzeichnet, daß die metallhaltige Schicht (36) aus einem Metall, einer Metalllegierung, einem Metalloxid oder einem Metallnitrid besteht.

7. Elektrolumineszierende Vorrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß zwischen der Kunststoffschicht (34) und der Schicht (36) eine zusätzliche Getterschicht (38) vorgesehen ist.

8. Elektrolumineszierende Vorrichtung nach Anspruch 7, dadurch gekennzeichnet, daß die Getterschicht (38) von der Schicht (36) außer an den Kontaktbereichen mit der Schicht (34) vollständig umschlossen wird.

9. Elektrolumineszierende Vorrichtung nach Anspruch 5 bis Anspruch 7, dadurch gekennzeichnet, daß zwischen der Metallschicht (36) und der Getterschicht (38) eine weitere Kunststoffschicht (40) vorgesehen ist.

10. Elekrolumineszierende Vorrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die Schichten (34, 40) aus Kunststoff aufgeschleudert, aufgedruckt, gegossen, aufextrudiert oder durch Tauchbeschichtung aufgebracht sind.

11. Elekrolumineszierende Vorrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die metallische Schicht (36) aufgedampft oder aufgesputtert ist.

12. Elekrolumineszierende Vorrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß auf die Schicht (36) eine Passivierungsschicht (42) aufgebracht ist.

13. Elekrolumineszierende Vorrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die Kapselung (28') aus optisch transparenten oder semitransparenten Materialien besteht.

14. Elekrolumineszierende Vorrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß das Mehrschichtsystem (32) oder wenigstens zwei Teilschichten (34, 36, 38, 40, 42, 44, 46, 48) des Mehrschichtsystems (32) aus einer separat vorgefertigten Verbundfolie bestehen, die zur Herstellung der Kapselung (28, 28') auf das elektrolumineszierende Schichtsystem (12) aufgebracht wird.

Hierzu 2 Seite(n) Zeichnungen

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– Leerseite –

Numm r: DE 196 03 748 A1
Int. Cl.[6]: H 05 B 33/04
Offenlegungstag: 24. April 1997

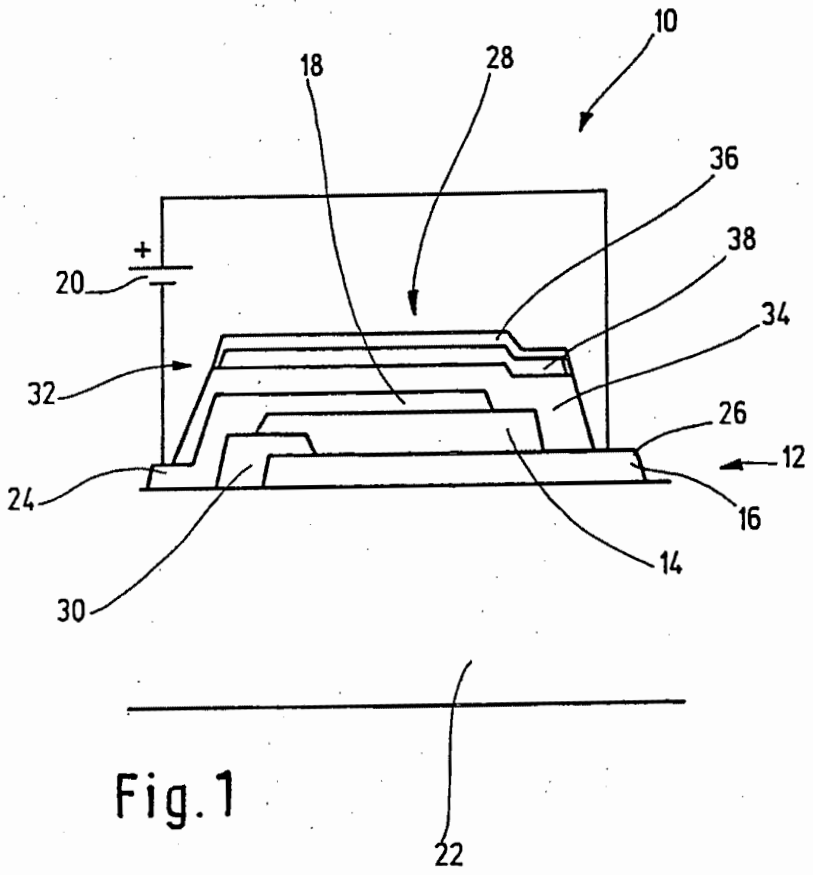


Fig. 1

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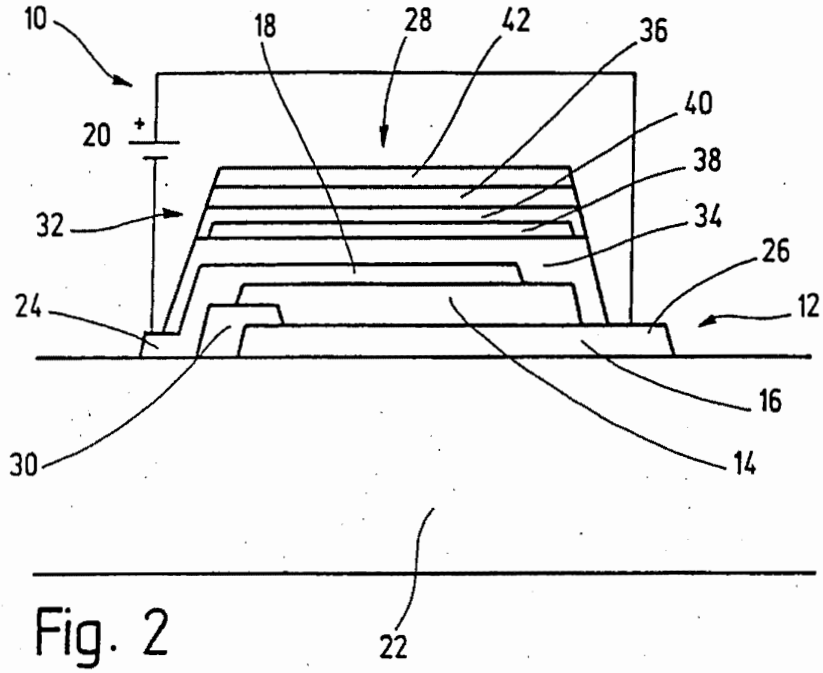


Fig. 2

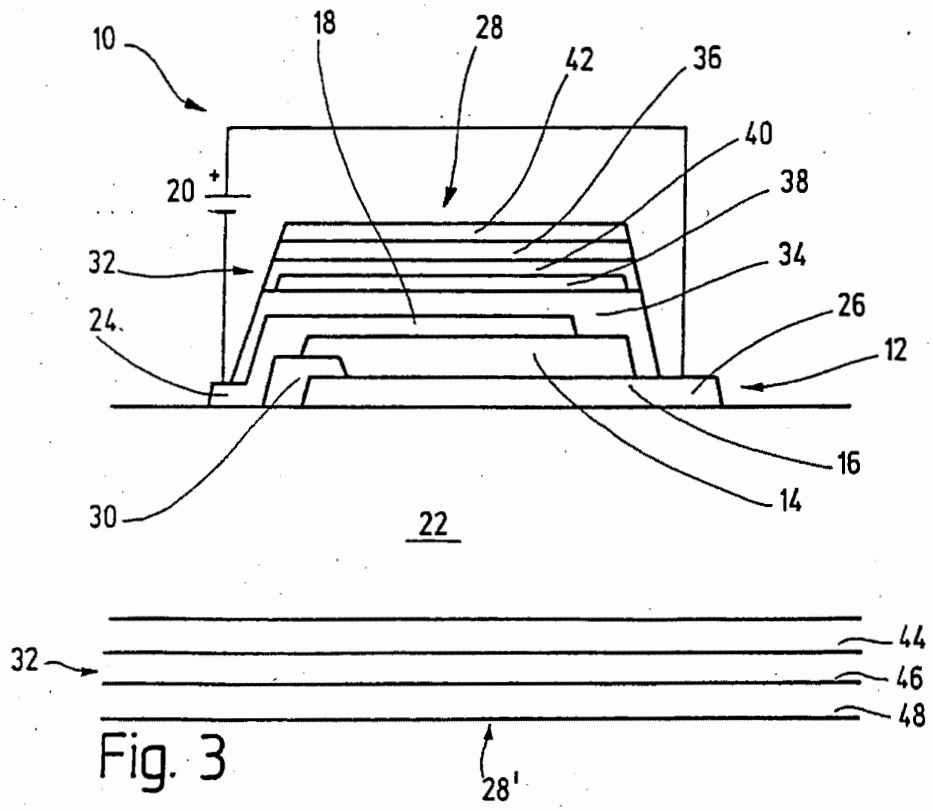


Fig. 3

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Low-cost display assembly and interconnect using ink-jet printing technology

Donald J. Hayes
W. Royall Cox
Michael E. Grove

Abstract — Ink-jet printing methods may be utilized for efficient micro-deposition of solder bumps, spacer balls, and adhesive sealant/bond lines, as well as liquid-crystal and color-filter droplets, in the manufacture of display panels. Advantages realized by this approach include data-driven low-cost high-speed non-contact environmentally friendly processing.

Keywords — Ink-jet printing, solder, spacers, liquid crystals, phosphors, color filters.

1 Introduction

Manufacturing technologies are being driven toward further automation, miniaturization, and reductions in costs, cycle times, and environmental impact. Thus, ink-jet printing methods are becoming increasingly attractive material micro-dispensing alternatives in a wide variety of applications. Advantages offered by the ink-jet printing method include low cost, precise control of dispensed volumes, data driven, *in-situ*, processing, and environmental friendliness. As a non-contact deposition method, this technology may also be employed to print on non-planar and curved surfaces.

Two differing approaches are utilized for piezoelectric (verses thermal) micro-jet printing of materials for manufacturing applications. As explained in Ref. 1, a stream of fluid ejected from the orifice of a pressurized fluid chamber is broken up into droplets by the application of pulses to a transducer bonded to the chamber. The droplets are electrostatically charged and deflected as needed to hit or bypass a moving-target substrate. This method offers advantages when high-speed coverages of relatively large areas are required, since droplets up to 0.5 mm in diameter may be produced at rates up to 1 MHz. A more widely utilized approach for smaller-droplet (20–100 μm) lower-frequency (to 10 kHz) dispensing applications is the drop-on-demand (DOD) technology.[2] In this type of ink-jet printing system, a droplet is only ejected from the device orifice when a voltage pulse is applied to a transducer coupled to the fluid at ambient pressure. The inherent temporal and spatial stability of the DOD micro-drop formation process is clearly illustrated in the 1-sec exposure shown in Fig. 1, where the stroboscopically illuminated image of an ejected droplet is actually the superposition of 2000 droplets.

Materials dispensed by DOD ink-jet printing processes have included (a) solder for placing bumps for flip-chip and ball-grid-array[3-5] and towers (vias) for chip-scale packages[6], (b) epoxy for micro-optics fabrication[7], (c) adhesive patterns for component bond-line patterns,[8] (d) dielectrics for component over coating and conformal capacitor fabrication, and (e) a variety of filled polymer systems for the printing of components such as resistors, micro-optical detector elements and organic polymer light-emitting diodes (PLED).[9,10]

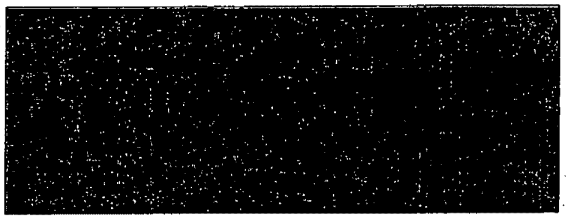


FIGURE 1 — Generation of 50-μm droplets by DOD microjet at 2 kHz.

2 Objectives

The overall objective of this work is to develop ink-jet/micro-jet processes and platforms for use in the fabrication of displays – both active elements (organic light-emitting polymers and phosphors) and passive elements (spacers, sealants, and electrical interconnects). This paper will focus primarily on passive-element printing, including solder bumps for IC driver electrical connection, polymer spacers, and adhesive bond/sealant lines.

For solder bump printing, the technical development objectives are now focused on increasing speed and placement accuracy. In addition to speed and accuracy objectives, spacer bump and adhesive bond/seal line printing also involve the challenges of optimizing the fluid formulations for meeting the applications requirements, while keeping within the rheological constraints imposed by the DOD

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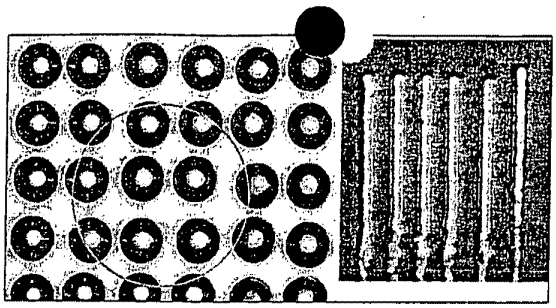


FIGURE 2 — Printed array of 24-μm-diameter solder bumps (left) and 25-μm-wide 400-μm-high solder towers (right).

micro-jetting process. For example, printed and cured polymer spacer bumps in LCDs must exhibit height uniformity to better than a micron, along with high levels of compressive strength and thermal stability. Likewise, printed and cured polymer sealant lines must be highly adherent to the bond surfaces and thermally stable against out-gassing or leaking at elevated processing temperatures.

3 Results

3.1 Solder bumping

Of the three micro-jet printing applications for panel display manufacturing addressed here, only the "Solder-Jet" technology has advanced to the point of commercialization. Tin/lead (63/37) solders have been printed at 220°C in both the continuous and drop-on-demand mode, and as both step-and-repeat and fire-on-the-fly processes. The size and shape of a printed solder bump depend on the number and diameter of the droplets deposited at the target site and on the temperature of the substrate. For Sn/Pb solder, no flux is needed to achieve good adhesion to gold or clean copper substrates, and adhesion to aluminum has been demonstrated with a doped Sn/Pb formulation. Indium-based solders have also been used for printing patterns of bumps directly onto ITO substrates.

In the DOD mode of solder-jetting, the diameter of a droplet formed by a device of a given orifice size may be modulated over a two-fold range by adjusting the device-driving waveform. By reducing the print-head device orifice size, solder bumps as small as 24 μm have been printed, and

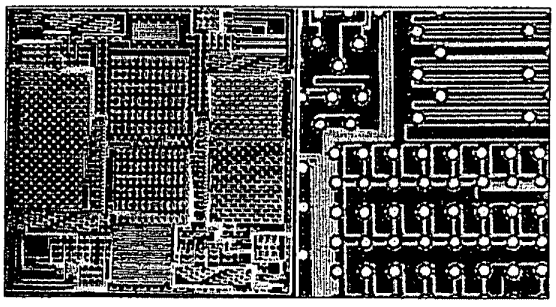


FIGURE 3 — Portions of microprocessor test vehicle with 1440 pads printed with 60-μm solder droplets at 100% yield.

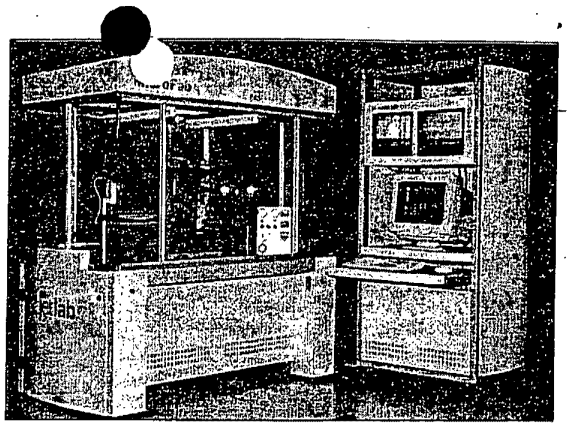


FIGURE 4 — MicroFab JetLab® solder and polymer high-temperature printing platform.

3D towers-vias fabricated, as shown in Fig. 2, with a step-and-print printing process. The use of this process in microelectronics manufacturing is illustrated in the photographs of Fig. 3, where 1440 microprocessor test vehicle pads were bumped at 100% yield utilizing the solder printing platform shown in Fig. 4. In the print-on-the-fly process, the substrate stages raster back and forth in the two horizontal-plane directions without stopping, while the print head ejects droplets continuously, but in the drop-on-demand mode. Data on target pad locations are entered *via* a CAD file, and the machine-vision system automatically registers the file with substrate fiducials. With this system wafer and chip pad bumping speeds in excess of 400 bumps/sec have been demonstrated.

3.2 Polymer spacer printing

The high-temperature DOD dispensing process for printing UV-curing polymer elements for applications such as dis-

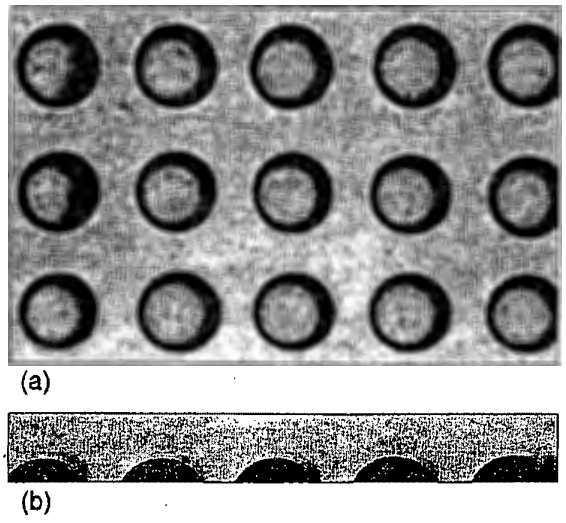


FIGURE 5 — (a) Array of 95-μm-diameter 34-μm-high printed polymer microlenses/spacer bumps, shown in the substrate plane. (b) Array of 95-μm-diameter microlenses/spacer bumps of (a) shown in profile.

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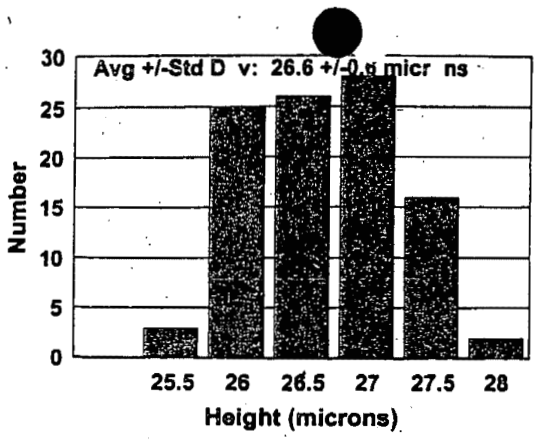


FIGURE 6 — Height distribution for an array of 80-μm-diameter printed polymer bumps.

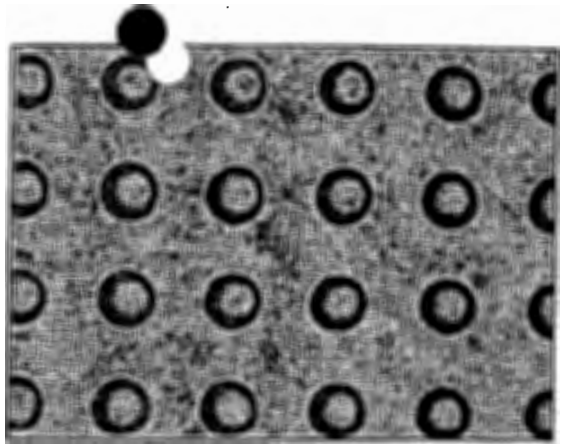


FIGURE 8 — Array of 100-μm-diameter droplets of liquid-crystal fluid printed at room temperature onto glass.

play spacers is very similar to that for solder bumping, so the same platform, with multiple print heads for different materials, may be used for both steps. UV-curing optical epoxies which are currently being used for printing microlens arrays, such as that pictured in Fig. 5, would meet the physical and thermal (in excess of 200°C) durability requirements for panel-display spacers. For spacer printing, the key parameter to control is the height of the deposited droplets, which is determined by droplet volume and the degree of spreading which occurs on the substrate prior to solidification and curing. The DOD printing process produces droplets of diameter close to that of the print head orifice and provides volumetric control over dispensed droplets to better than 2%. The spreading of deposited material may also be precisely controlled by the use of low-wetting coatings on the target substrates to provide specific contact angles and, additionally, by varying substrate temperature to adjust fluid viscosity prior to solidification. The distribution in the heights of printed spacer bumps currently achievable is exemplified by the data in Fig. 6 for an array of 80-μm-diameter epoxy bumps. Arrays of hemispherical microlenses as small as 25 μm in diameter and 8 μm in height, have been printed in our laboratory. This is within the usable size range for the manufacture of low-cost displays, and could contribute to further cost reductions.

Finally, the printing of microlenses such as those pictured in Fig. 5 has been discussed for enhancing pixel brightness by focusing the light in back-lighted displays.

3.3 Sealant/bond line printing

The ink-jet printing of adhesives for the sealing and bonding of various components has been used in applications such as optical component assembly and could be employed for the sealing of LCD cells. For materials requiring dispensing at temperatures less than 140°C, either single-jet or array-type print heads may be used, depending on throughput requirements. In all cases the line patterns would be printed from data files and aligned to substrate fiducials. The width and

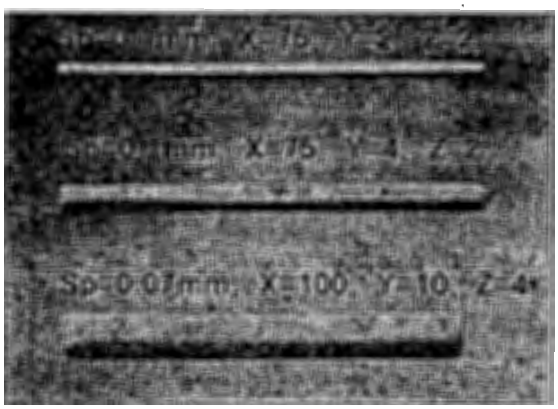


FIGURE 7 — Printed bond lines (top is 300 μm wide) made by deposition at 125°C of 60 μm droplets of thermoset epoxy, where site spacings (Sp), number of sites in the horizontal (*x*) and vertical (*y*) directions in the substrate plane, and number of droplets per site (*z*) are as indicated.

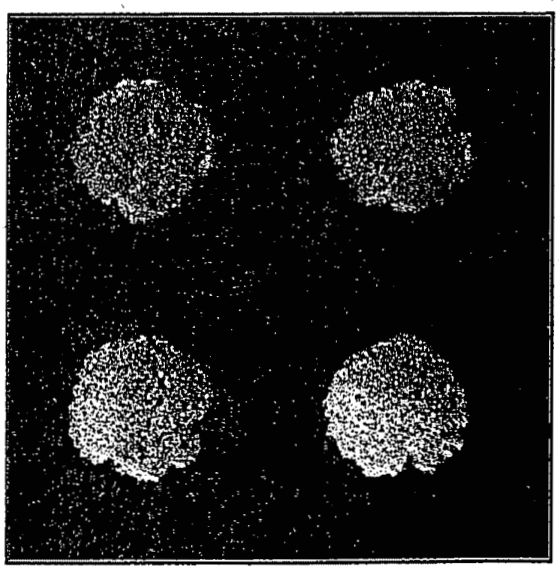


FIGURE 9 — SEM photograph of Zn_2SiO_4:Mn phosphor powder dots with 90-μm diameters ink-jet printed onto glass (at MicroFab Laboratories). (Micropowders and photograph courtesy of superior micropowders, see Ref. 11.)

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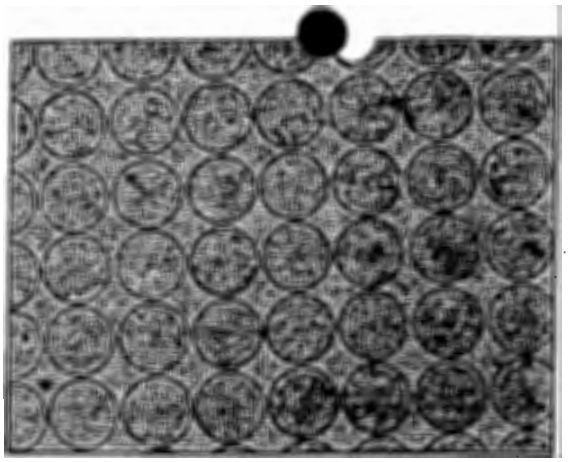


FIGURE 10 — 130-μm-diameter drops of pigment printed at 40°C onto 100°C glass.

height of the cross section of each printed line is determined by the specified spacings of the deposition sites and the number of droplets deposited per site, as seen in Fig. 7, as well as by the wetability of the substrate surface by the adhesive fluid.

3.4 Active element and color-filter printing

Arrays of printed droplets of liquid crystal and phosphor[11] elements are shown in Figs. 8 and 9, respectively. The print-on-the-fly microjet printing method may be utilized for printing such arrays at rates up to 200 elements per second. Being a high-speed additive process, ink-jet printing offers an economy in the manufacture of liquid-crystal and phosphor screens that conventional slurry photolithography, or even screen-printing methods, cannot match, even with recovery. This advantage of economy may also be realized in the ink-jet printing of arrays of pigment-doped optical epoxy spots, as illustrated in Fig. 10, for the fabrication of color-filter elements. In these cases, three print heads are utilized, one for each color to maximize throughput rates.

4 Conclusions

We have developed the basic technologies for the ink-jet printing of metals, polymers, phosphor dispersions, and liquid crystals for potential use in flat-panel-display manufacturing *via* automated deposition of solder and spacer bumps, LCD cell sealant/bond lines, active elements, and microlenses. High-speed production printing stations are currently available for solder and polymer printing. The industrial impact of the use of ink-jet printing technology on the fabrication of color flat (or curved) panel displays could be substantial. Cost advantages accruing from this approach could result from (a) digital control of dispensing which may be site-specific and (b) additive processing, which conserves expensive optically active materials and reduces environmental impact.

Acknowledgments

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W. Royall Cox has A.B. and Ph.D. degrees in physics from Duke University and the University of Texas, respectively. As Principal Scientist at MicroFab Technologies, Inc., he has managed the development of micro-optics printing and micromachining technologies and has contributed to the development of high-temperature microjet printing devices. Dr. Cox, a member of SPIE and IEEE, has numerous publications and patents on micro-optics printing technology.

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Mike E. Grove [illegible] and M.S. degrees in chemistry from the University of Texas and the Illinois Institute of Technology, respectively. He has 27 years experience in formulating materials such as conductive and photo-active polymers for both inks and coatings for ink-jet printing and other applications. At MicroFab he has developed original thermoplastic and UV-curing optical material formulations for micro-jet printing.

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Progress and Trends in Ink-jet Printing Technology

Part 4

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Ink Chemistry. The most critical component of ink-jet printing is probably the ink. Ink chemistry and formulations not only dictate the quality of the printed image, but they also determine the drop ejection characteristics and the reliability of the printing system. Many different types of inks have been developed and used in ink-jet applications. Figure 26 illustrates a technology map of different types of ink-jet inks.

Aqueous- or water-based inks are commonly used in home and small-office ink-jet printers such as in the Hewlett-Packard DeskJet series, Canon BJC series, and Epson Color Stylus series ink-jet printers. In the case of thermal ink-jet, due to the basic vapor bubble formation process, water seems the material of choice for the method. Typical composition of a water-based ink for ink-jet printing is presented in Table II Viscosity of water-based ink-jet inks range from 2 to 8 cps.

Figure 27 illustrates the behavior of a water-based ink droplet when it lands on the surface of an uncoated media such as bond, copy, or plain papers. The ink tends to spread along the paper fibers and penetrate into the bulk of the paper. The water-based ink actually depends on penetration and absorption for its drying mechanism. Some evaporation of water is taking place, but this drying mechanism is often very slow. Such ink behavior lowers color density and spot resolution on paper. It has been known for some time that pape or other media with a coated water-receiving layer can greatly improve both color density and resolution by controlling the ink spreading and penetration at the coated layer. However, just within the past few years the market for the specialty-coated ink-jet media has exploded, especially in the home photo quality and large-format ink-jet printing areas.[32] Recent availability of printhead technologies with high resolution (such as 1440 dpi Epson Color Stylus 800, 1200 x 1200 dpi Lexmark 7000, 10 pL drop Hewlett-Packard DeskJe 890C), multilevel dye load gray-scale (such as in photo pens from Epson, Canon, and Hewlett-Packard) and multilevel dot volume gray-scale capability (such as in Hewlett-Packard DeskJet 720C and 890C certainly have made a positive impact on this trend.

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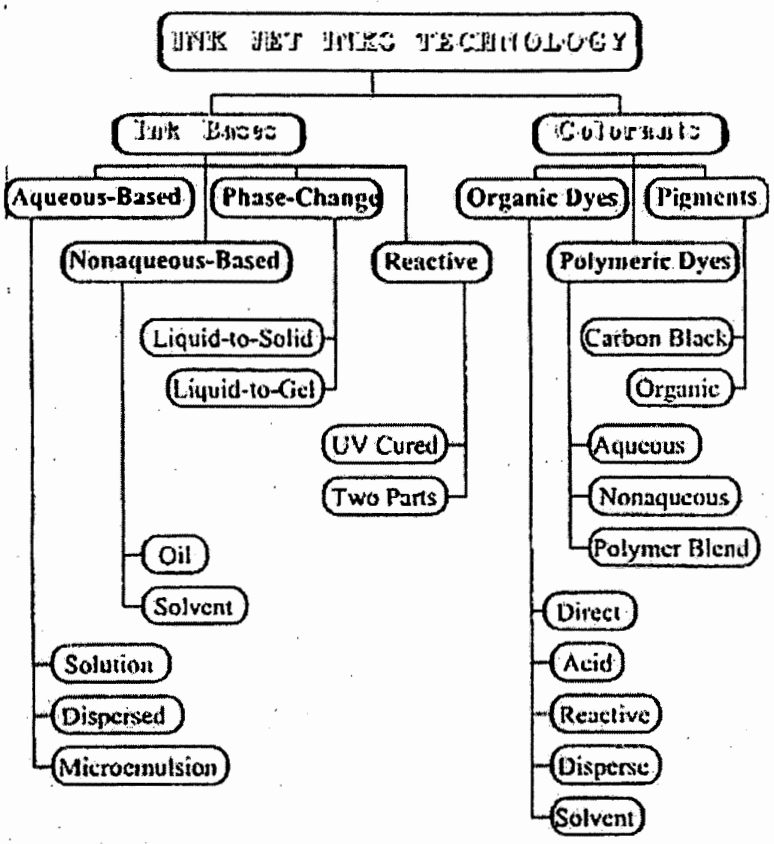


Figure 26. An ink-jet ink technologies map.

Table II. Water-Based Ink-Jet Ink Composition

Component	Function	Concent
Deionized water	Aqueous carrier medium	60 - 90
Water soluble solvent	Humectant, viscosity control	5 - 30
Dye or pigment	Provides color	1 - 10
Surfactant	Wetting, penetrating	0.1 - 10
Biocide	Prevents biological growth	0.05 - 1
Buffer	Controls the pH of ink	0.1 - 0.5
Other additives	Chelating agent, defoamer, solublizer etc.	> 1

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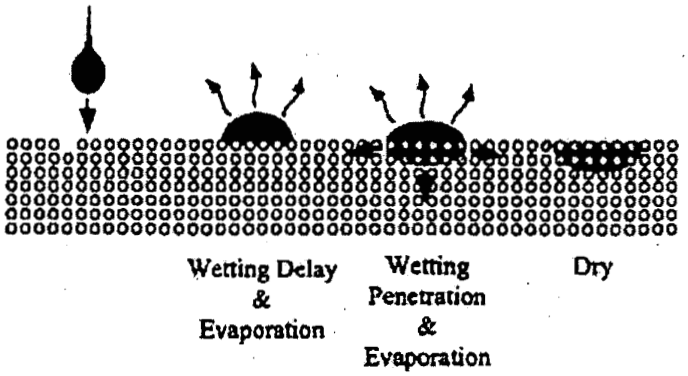


Figure 27. Drying mechanisms of a water-based ink-jet drop on a plain paper.

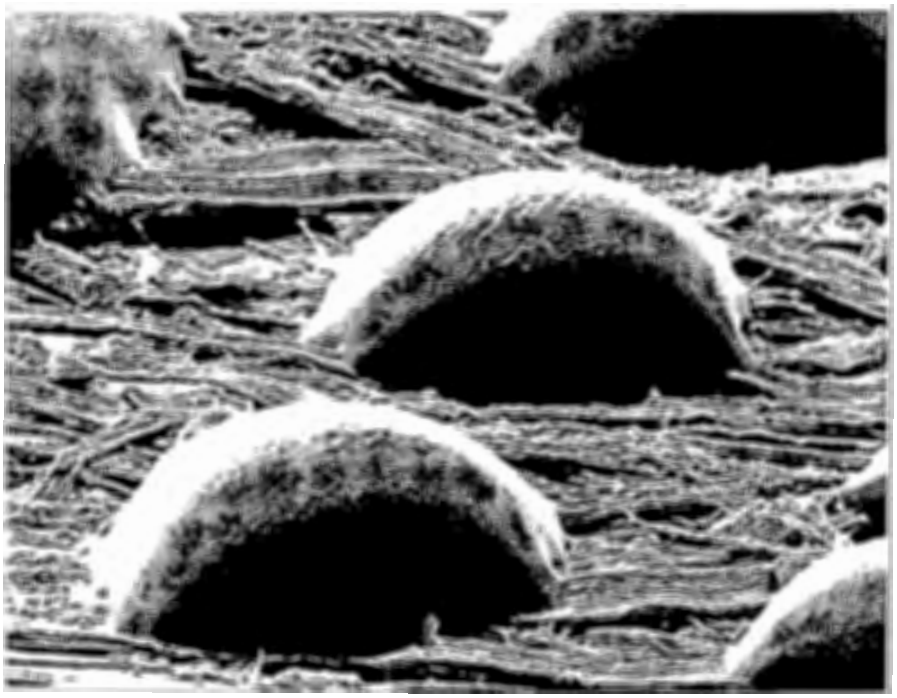


Figure 28. A SEM photograph of phase-change ink drops on the surface of a bond paper.

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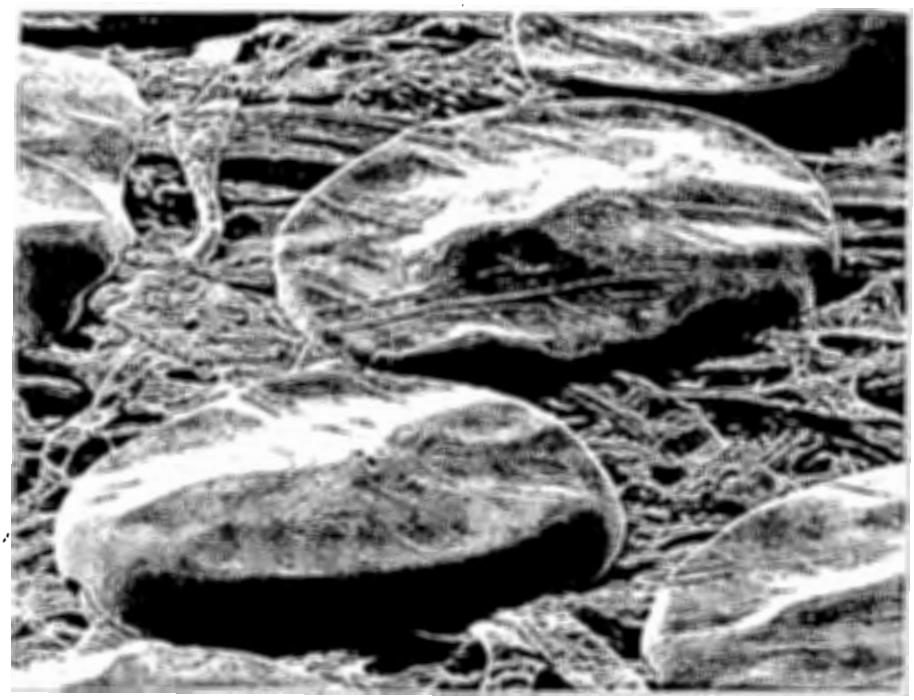


Figure 29. A SEM photograph of phase-change ink drops after fuse by cold pressure rollers.

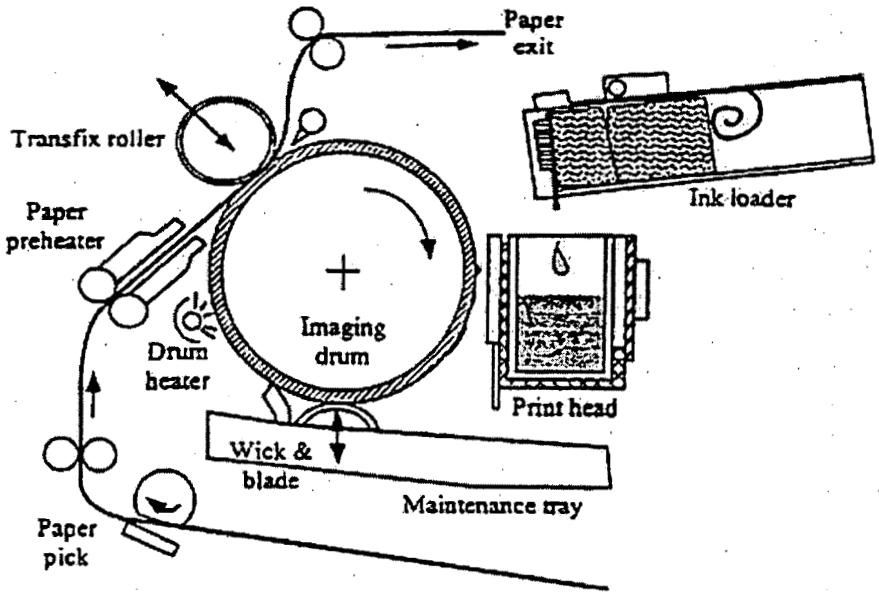


Figure 30. The basic configuration of the Tektronix's Phaser 350 offset drum transfer ink-jet printer.

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Figure 31. A SEM photograph of a phase-change ink drop on the surface of aluminum substrate.

Phase-change ink is also called hot melt or solid ink which is solid at room temperature. The ink is jetted ou from the printhead as a molten liquid. Upon hitting a recording surface, the molten ink drop solidifies immediately, thus preventing the ink from spreading or penetrating the printed media. The quick solidification feature ensures that image quality is good on a wide variety of recording media. Figure 28 shows a SEM photograph of phase-change ink drops printed on the surface of a Xerox 4024 bond paper Notice that the ink drops maintain their hemisphere shape with little or no evidence of ink spreading, even along rough paper fiber structures. Tektronix currently implements phase-change ink-jet technology in the Phaser 300 ink-jet printer. However, in practice, the solidified ink drops need to be fused on top of paper to increase ink adhesion and prevent light scattering owing to the lens effect of the hemisphere shaped ink dot.[33] Figure 29 shows a SEM photograph of several Tektronix Phaser 300 phase-change ink drops afte being fused by a cold pressure fusing roller.

Another successful implementation of phase-change ink-jet technology is in the Tektronix Phaser 350 offse trans fer printing architecture. Figure 30 describes major components of a Tektronix Phaser 350 color ink-je printer. Basically, the printing process starts with coating a thin silicon oil film onto a warm rotating aluminum drum. Ink is then jetted onto this intermediate drum. Once an entire image is printed, it is then transferred from the drum onto a preheated media via a pressure nip. It is very critical for the drum to be heated at a temperature above the glass transition temperature and below the ink melting point so that the phase-change-ink material is soft enough to fuse into paper with moderate pressure, but still strong enough to prevent the ink from cohesive failure when exiting the pressure nip.[35]

A SEM photograph of a phase-change ink drop on an aluminum surface is shown in Fig. 31. A SEM photograph of an offset-transferred phase-change-ink dot on an aluminum surface onto a bond paper is showed in Fig. 32. Because of its ability to print good color quality images on a variety of bond and plain papers at speeds of up to 6 ppm, Tektronix's Phaser 350 phase-change ink-jet printer has been very successful in the office network printer market. Other companies that actively develop and commercialize the phase-change ink-jet-printing method are Spectra[36] and Dataproducts.[13]

Table III describes a typical composition for a phase-change ink formulation. Operating temperatures fo phase-change inks range from 120 to 140C. Viscosity at the operating temperatures are from 8 to 15 cps.

Solvent-based inks are commonly used in industrial marking or coating applications where the printing is done on a nonporous substrate such as plastic, metal, or glass. Because no absorption or penetration occurs, the printed image relies on quick evaporation of the ink solvent to be fixed onto the substrate.

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Figure 32. A SEM of a fused phase-change ink drop on a paper that results from a offset drum transfer process.

Table III. Phase-change Ink Composition

Component	Function	Concentration, %
Solid wax mixture	Ink vehicle	40 to 70
Viscosity modifier	Lowers viscosity	5 to 20
Tackifier	Imparts adhesion	1 to 15
Plasticizer	Provides flexibility	1 to 15
Dye or pigment	Provides color	1 to 10
Antioxidant	Heat stability	0.05 to 2

Another type of nonaqueous-based ink is oil-based. This type of ink was recently used in several large-format ink-jet printers including the Raster Graphics PiezoPrint 5000 and the Xerox ColorgrafX. Both of these printers utilize Nu-Kote piezo shear-mode printheads. This printhead requires its ink to be compatible with the PZT electrode that is located on the walls of its ink chambers. The use of nonpolar oil-based ink minimizes the effect of electrical fields on ink and printhead materials. However, the ink manufacturer (Zeneca) for the Nu-Kote shear-mode ink-jet printhead also claims that the advantages of oil-based inks, when compared with water-based are faster drying time and the absence of cockle on paper substrates.[37] With the proper paper coating design, the above claim can be realized.

Image quality and durability for water-based, phase-change, and oil-based ink-jet inks are generally acceptable when they are printed on ink-jet papers or coated substrates. However, when printing on nonabsorbent substrates such as metal, glass, and plastic, the above ink systems are not adequate to produce durable and sharp images. To solve this problem, the idea of using a UV curable ink system fo ink-jet printing has been discussed for a long time. However, many factors (such as ink-jet printhead capability, photoinitiator and low-toxicity monomer availability, and market needs) have hindered the progress of UV curable ink-jet ink development. Today ink-jet printheads are more capable and available UV photoinitiators, monomers, and oligomers are readily available at economic scale; and market needs are strong. Successful development of UV curable inks for ink-jet applications are predicted in the near future.

Drying mechanisms for various ink-jet ink systems are summarized in Table IV.

Another major development in the ink-jet printing industry is the successful implementation and commercialization of pigment-based inks in color printing applications. Many companies including 3M Dupont, and Kodak have already had pigmented ink-jet ink products on the market. With such focus by the industry, the color quality, image durability, and jetting reliability of the inks will be improved. In addition severe competition for market share will likely result in significantly reduced cost for pigmented ink-jet inks.

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Table IV. Drying Mechanisms for Different Ink-Jet Inks

Ink	Printhead	Drying M chanism
Aqueous	Thermal/Piezo	Continuous Absorption/ Penetration Evaporation
Oil	Piezo continuous	Absorption/Penetration
Solvent	Continuous piezo	Evaporation
Hot melt	Piezo	Solidification
UV curable-based	Piezo continuous	Polymerization
Reactive-based	Piezo Continuous	Oxidation Polymerization

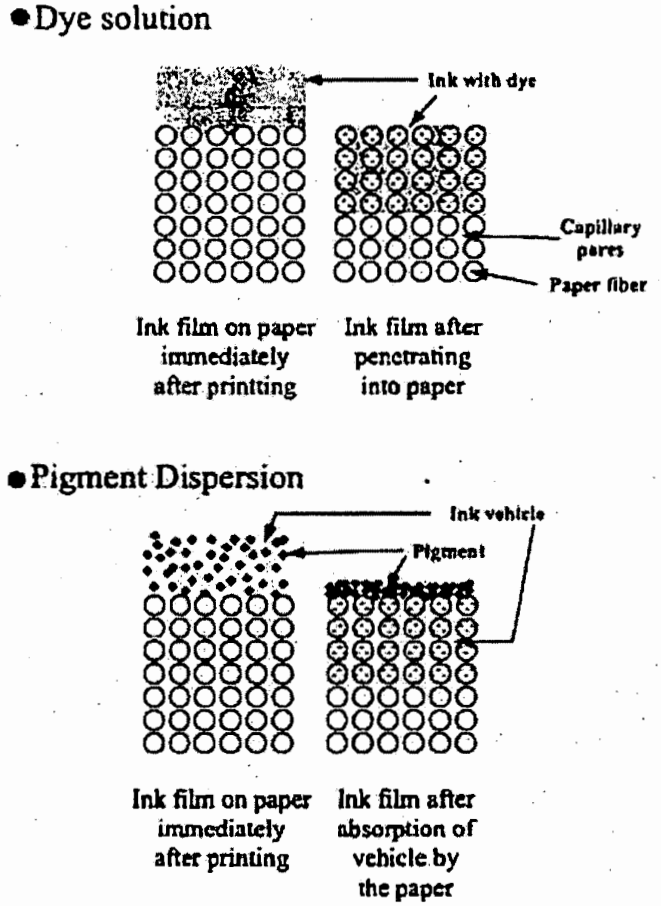


Figure 33. Comparison between dye solution and pigment dispersion behaviors on paper.

Figure 33 compares the ink and paper interactions between dye solution and pigment dispersion. Dye molecules are dissolved into an ink base that tends to penetrate or absorb into a paper or coating substrate. Pigment particles are dispersed into the ink base. While the ink base penetrates into the bulk of the paper substrate, pigment particles tend to remain on the surface of the paper. Figure 34 is a cross section light microscope photograph showing the behavior of pigmented black and cyan dye ink-jet inks throughout the thickness of a bond paper.

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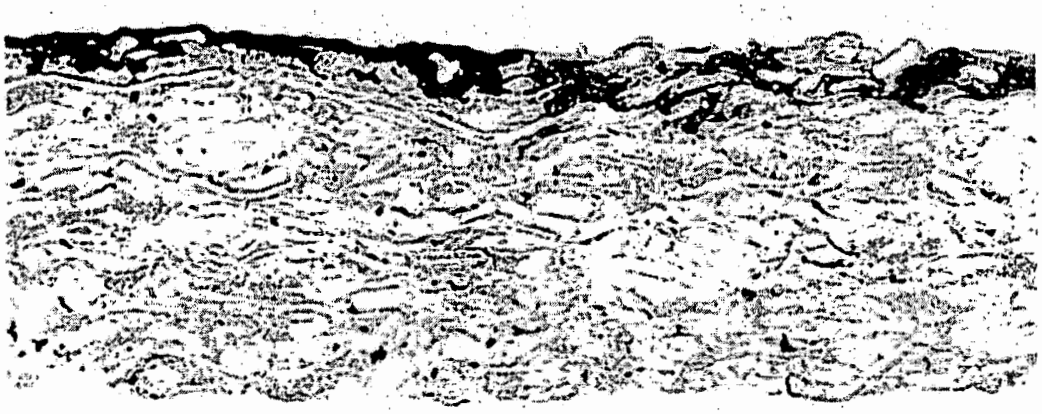


Figure 34. A cross section light microscope of pigment-based (on the left) and dye-based (on the right) inks on paper.

One significant advantage of pigment-based as compared to dye-based ink is its color durability when exposed to light or outdoor weather conditions. This feature is definitely critical to applications such as billboards or other large-format displays. However, as compared to dye base, pigment-based ink-jet ink has the inherent disadvantage of particle dispersion instability that may lead to nozzle clogging. Even though the pigment dispersion chemistry and process of making ink-jet ink has improved significantly in the past few years,[37–40] the trend in the ink-jet industry is toward smaller nozzle diameter for high resolution and a highe number of jets for print speed. The reliability issue should be a part of the decision process when it comes to the pigment or dye-base question.

Another recent development in the ink-jet ink area is the introduction of the Canon BJC-7000 ink-jet printer This new printer implemented a new process called Plain Paper Optimized Printing (P-POP). The black printhead contains black ink and a precoat fluid applied to the paper surface a few microseconds before dye-based ink drops hit the paper. The precoat fluid is clear and believed to contain a compound that wil aggregate with the dye, thus fixing it instantly on the surface of paper.[41] This unique approach is proven to provide excellent waterfastness. The P-POP process not only improved waterfastness of the printed image but fixed the ink on the top surface of the paper, making a plain paper perform like a coated media. If this approach does not impact the overall reliability of the system in any way, the P-POP process will become one of Canon's significant technological breakthroughs.

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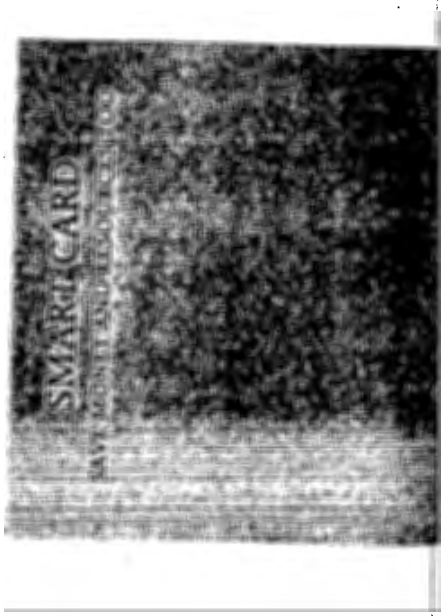
- UV curable ink.
- High resistance to solvents.
- Excellent light fastness.
- Excellent end user properties.
- Recommended for applications printing onto materials including:
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  - LDPE
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  - Stainless Steel
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- Heart resist ink : Up to 1300 °C after printing.
- UV curable ink.

Ink Specifications

Variety of Ink realized to print on a various base.

Name of Ink	Color	Solvent Base	Drying time at 20°C	Ink Characteristics and Primary Applications	Applicable Nozzle Size 65µm	40µm
JP-K67	Black	MEK	1-5(s)	General purpose ink. Good adhesion for various materials and high tolerance for sunshine. :Paper,Steel,Plastics,Food,Drinks,Cosmetics,Medicine,Electric parts,Electronic parts,Mechanic parts,etc.	O	O
JP-K27E	Black				O	O
JP-R27	Red				O	-
JP-G27	Green				O	-
JP-B27	Blue				O	-
JP-K26	Black	MEK	1-5(s)	Alkali-soluble :Recyclable containers.	O	-
JP-K28	Black	MEK	1-5(s)	Plastic and can(surface with wax)	O	-
JP-K31A	Black	MEK	1-5(s)	Coping resist :Plastic,etc, Steam resist :Cans,etc	O	-
JP-K60	Black	Ethanol	3-10(s)	Ethanol based general-purpose ink. :Foods,Medicine,etc.	O	-
JP-K61	Black	MEK	1-5(s)	Available for PP film.	O	-
JP-K62	Black	MEK	1-5(s)	Resist for sweating on the glass surface. :Glass bottles,etc.	O	-
JP-F63	Radiate Blue by UV light	MEK	20-40(s)	The print message appears in UV light radiation. For quality control in production line.	O	-
JP-T64	Brown(20C)	MEK	1-5(s)	Heart resist ink :Ceramics,Metals,etc	O	-
JP-K65	Black	MEK	Depends on the curing condition	UV curable ink :Printed circuit board, Electric and electronic parts,etc.	O	-

[Note MEK:Methyl-Ethyl-Ketone]

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Acknowledgements

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Spin-dependent exciton formation in π-conjugated compounds

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The efficiency of light-emitting diodes (LEDs) made from organic semiconductors is determined by the fraction of injected electrons and holes that recombine to form emissive spin-singlet states rather than non-emissive spin-triplet states. If the process by which these states form is spin-independent, the maximum efficiency of organic LEDs will be limited to 25 per cent[1]. But recent reports have indicated fractions of emissive singlet states ranging from 22 to 63 per cent[2–5], and the reason for this variation remains unclear. Here we determine the absolute fraction of singlet states generated in a platinum-containing conjugated polymer and its corresponding monomer. The spin-orbit coupling introduced by the platinum atom allows triplet-state emission, so optically and electrically generated luminescence from both singlet and triplet states can be compared directly. We find an average singlet generation fraction of 22 ± 1 per cent for the monomer, but 57 ± 4 per cent for the polymer. This suggests that recombination is spin-independent for the monomer, but that a spin-dependent process, favouring singlet formation, is effective in the polymer. We suggest that this process is a consequence of the exchange interaction, which will operate on overlapping electron and hole wavefunctions on the same polymer chain at their capture radius.

Several sophisticated methods have been used to determine the singlet generation fraction in organic LEDs, but these are often complicated by the fact that triplet states are generally non-emissive in conjugated organic compounds. As a result it has previously only been possible to place a lower limit on the singlet generation fraction in polymer LEDs. We have circumvented the problem of a non-emissive triplet state by investigating a Pt-containing polymer and its corresponding monomer (Fig. 1). The heavy Pt atom introduces spin-orbit coupling which allows the spin of the electron to flip or rephase and transitions between the singlet and triplet manifolds become possible[6]. Conjugation is preserved through the Pt atom by mixing of the frontier orbitals of the Pt and the ligand[7]. Direct emission from the triplet state is therefore observed for both optical and electrical excitation of LEDs made from these materials and this allows a straightforward calculation of the absolute singlet generation fraction.

The photoluminescence and electroluminescence spectra of the polymer and monomer (Fig. 2) both show two characteristic emission bands, and the relative contribution of each band to the total emission is indicated as a percentage. The high and low energy bands are due to singlet and triplet excited states S_1 and T_1,

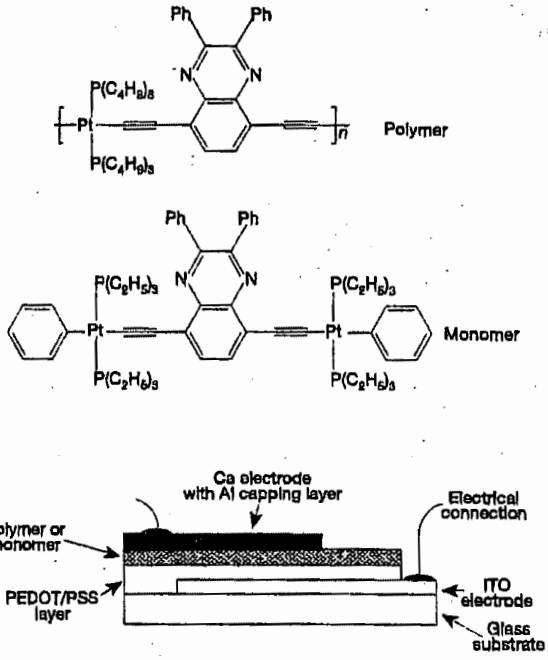


Figure 1 The chemical structures of the platinum-containing polymer and monomer investigated. A schematic of the simple light-emitting diode structure used is also given. PEDOT, poly(3,4-ethylenedioxythiophene); PSS, poly(styrenesulphonate); ITO, indium-tin oxide.

respectively. The triplet-state emission of this polymer and monomer and that of other similar materials has been well characterized previously by lifetime and photoinduced absorption measurements[8–11]. The triplet emission is observed at around 0.7 eV below the singlet in this and other conjugated polymers[9,10,12–14] and this finite exchange energy implies an excited state which is self-localized.

We note that although the spin-orbit coupling induced by the heavy Pt atom has been shown to produce close to 100% intersystem crossing[8] from the S_1 state to T_1, there is still more emission observed from S_1 than from T_1 in photoluminescence at 290 K. This is because, despite the T_1–S_0 transition being partially allowed in this polymer and monomer, the radiative decay rates from the triplet states are still only of the order of $10^3\ s^{-1}$ in comparison with non-radiative decay rates of 10^6–$10^5\ s^{-1}$, so only one in 1,000 of the triplets generated emits[15]. The non-radiative decay rate increases exponentially with decreasing T_1–S_0 gap and is controlled by multi-phonon emission[15].

In order to compare electroluminescence and photoluminescence spectra we measured both in LED structures. For electrical excitation we observe a greater percentage of the photons to be from the triplet state than with optical excitation, but in other respects the spectra are very similar (Fig. 2). In order to use the emission spectra to calculate the fraction of excited states generated in the singlet spin state, χ_S, we model the processes of photoluminescence and electroluminescence as shown in Fig. 3. In photoluminescence a number I of excitons are originally all created in the singlet S_1 state, and from there they decay radiatively (with a decay rate $k_{R(S)}$) or non-radiatively (with a decay rate $k_{NR(S)}$) to the singlet ground state S_0, or undergo intersystem crossing to the triplet manifold (with a rate k_{ISC}). Both radiative and non-radiative decay occurs from the triplet state T_1 to the ground state S_0. For electroluminescence the processes are exactly the same as in photoluminescence, with the important exception that it is also possible to create a fraction χ_T of triplet excitons directly. We define the quantum yields

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Φ for radiative triplet (TR) and singlet (SR) emission and for intersystem crossing (ISC):

$$\Phi_{SR} = \frac{k_{R(S)}}{[k_{ISC} + k_{R(S)} + k_{NR(S)}]} \qquad \Phi_{TR} = \frac{k_{R(T)}}{[k_{R(T)} + k_{NR(T)}]}$$

$$\Phi_{ISC} = \frac{k_{ISC}}{[k_{ISC} + k_{R(S)} + k_{NR(S)}]}$$

The number of photons emitted from the triplet and singlet states are denoted N_T and N_S respectively, and the ratio of these is labelled R. For photoluminescence:

$$N_{S,PL} = I\Phi_{SR,PL}$$

$$N_{T,PL} = I\Phi_{ISC,PL}\Phi_{TR,PL}$$

$$R_{PL} = \frac{N_{T,PL}}{N_{S,PL}} = \frac{\Phi_{ISC,PL}\Phi_{TR,PL}}{\Phi_{SR,PL}}$$

For electroluminescence:

$$N_{S,EL} = I\chi_S\Phi_{SR,EL}$$

$$N_{T,EL} = I\chi_S\Phi_{ISC,EL}\Phi_{TR,EL} + I\chi_T\Phi_{TR,EL}$$

$$R_{EL} = \frac{N_{T,EL}}{N_{S,EL}} = \frac{\chi_S\Phi_{ISC,EL}\Phi_{TR,EL} + \chi_T\Phi_{TR,EL}}{\chi_S\Phi_{SR,EL}}$$

Comparing photoluminescence and electroluminescence gives:

$$\frac{R_{PL}}{R_{EL}} = \left(\frac{\chi_S\Phi_{ISC,PL}}{\chi_S\Phi_{ISC,EL} + \chi_T}\right)\left(\frac{\Phi_{TR,PL}}{\Phi_{TR,EL}}\right)\left(\frac{\Phi_{SR,EL}}{\Phi_{SR,PL}}\right) \qquad (1)$$

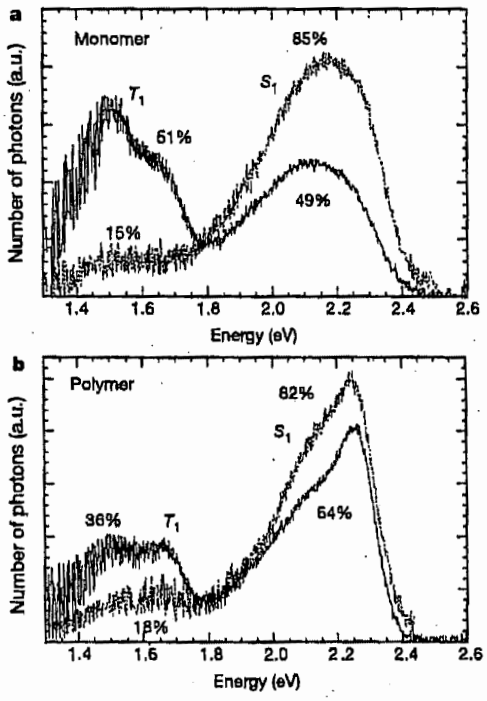


Figure 2 Comparison of the photoluminescence and electroluminescence spectra of light-emitting diodes of the platinum-containing polymer and monomer at 290 K. **a**, The photoluminescence (dotted line) and electroluminescence (solid line) spectra of a monomer LED. **b**, The photoluminescence and electroluminescence spectra of a polymer LED. The triplet emission is denoted by T_1 and the singlet emission by S_1. The spectra have been plotted in terms of number of photons and the fraction of the total emission that the singlet and triplet emission represent are given as percentages.

If we assume that the decay rates are the same for electroluminescence and photoluminescence we obtain $\Phi_{PL} = \Phi_{EL}$, and because $\chi_S + \chi_T = 1$, equation (1) becomes:

$$\frac{R_{PL}}{R_{EL}} = \left(\frac{\chi_S\Phi_{ISC,PL}}{\chi_S\Phi_{ISC,EL} + (1 - \chi_S)}\right) \qquad (2)$$

For these materials Φ_{ISC} is known to be close to one[8] so we approximate equation (2) by:

$$\frac{R_{PL}}{R_{EL}} = \chi_S \qquad (3)$$

Therefore, simply by dividing the spectrally integrated triplet emission by that of singlet emission for electroluminescence and photoluminescence in spectra such as those in Fig. 2, it is possible to obtain an absolute value for the singlet generation fraction, χ_S, with the advantage that many factors involved cancel out. For example for the data shown in Fig. 2b, $R_{PL} = 18/82$, and $R_{EL} = 36/64$ which gives $\chi_S = 0.39$.

The only assumption that has been made is that there is no difference in the decay rates for excited states whether they are created optically or electrically and we now examine this more closely. If electroluminescence and photoluminescence originate from different positions in the device relative to the electrodes, they may experience different quenching[16,17]. To check this we measured the dependency of χ_S on film thickness (Fig. 4a) and also the lifetimes (and therefore decay rates[6]) of triplet emission for both optical and electrical excitation. We find no significant variations in χ_S down to devices where the emitting layer was only around 20 nm thick and we observe the same lifetimes in photoluminescence and electroluminescence. For the monomer the room-temperature triplet lifetime is 10 ± 2 μs for optical excitation and 11.8 ± 0.5 μs for electrical excitation. For the polymer the room temperature lifetime is shorter and therefore more difficult to measure, but at around 100 K optical excitation gives a triplet lifetime of 2.8 ± 0.8 μs and electrical excitation gives 3 ± 1 μs. The decay rates of the triplet are therefore the same for both optical and electrical excitation.

In order to elucidate which parameters control the generation of singlet and triplet excited states in organic LEDs we studied the dependence of the singlet generation fraction on electric field and temperature. The temperature may affect carrier mobilities and processes with an activation energy, and the electric field could also influence exciton formation[18]. However, it can be seen from Fig. 4b and c that we observe no significant variation in χ_S with temperature or electric field over the working range of the devices. We note that the room-temperature values for χ_S are slightly lower than the values below 200 K, but we cannot rule out a systematic error here as

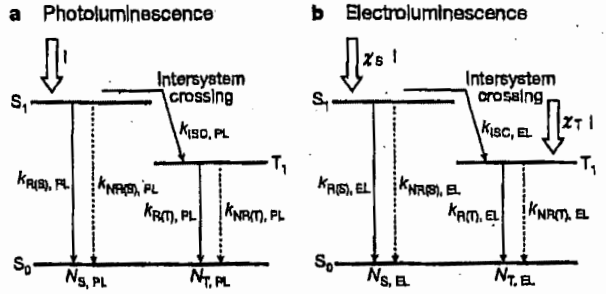


Figure 3 A simple model for the emission spectra in photoluminescence (**a**) and electroluminescence (**b**). I represents an initial number of excitons. k_{NR}, k_R and k_{ISC} represent non-radiative, radiative and intersystem crossing rates respectively, and N_S and N_T represent the number of singlet and triplet photons that would be expected to be emitted. χ_S and χ_T are the singlet and triplet generation fractions, respectively. S_0 is the singlet ground state.

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there is very little triplet emission in photoluminescence at 290 K.

To summarize, we find different values of the singlet generation fraction χ_S for the polymer and monomer of the same material that reconcile the different values available in the literature. The average values of χ_S we obtain for the monomer and polymer at room temperature are 0.15 ± 0.01 and 0.40 ± 0.03 respectively, and averaging over all temperatures gives 0.22 ± 0.01 and 0.57 ± 0.04 respectively. For the monomer this is close to the 0.25 expected from simple spin statistics and in agreement with the value of 0.22 ± 0.03 measured[2] for the small molecule Alq_3. For the polymer the average value of χ_S is more than double the value expected from simple spin statistics and is above the lower limit for the singlet generation fraction of 0.35–0.5 measured for PPV derivative polymers[3,4]. The 290 K value also agrees with the χ_S value of 0.4 predicted[5] for a polymer with a bandgap between 2.3 and 2.5 eV. Clearly the fact that we observe χ_S to be largely independent of temperature and applied electric field means these parameters do not significantly influence the probability of forming either a singlet or triplet spin state.

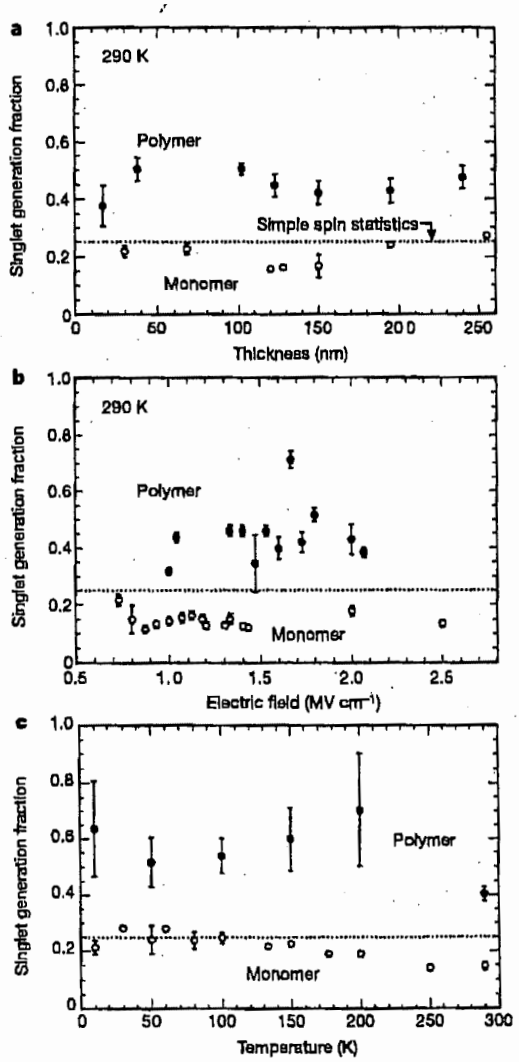


Figure 4 The singlet generation fraction χ_S for the platinum-containing polymer and monomer under different device conditions. **a**, χ_S plotted as a function of device thickness for polymer (solid circles) and monomer (open circles) LEDs. **b**, χ_S plotted as a function of applied electric field. **c**, χ_S plotted as a function of temperature. The error bars on each point represent the statistical error obtained by measuring a large number of devices. The dotted line represents the fraction (0.25) expected from simple spin statistics.

The marked difference we find in χ_S for polymer and monomer LEDs implies different processes of singlet and triplet formation via electron–hole capture and we now consider why these may occur. Organic LEDs operate by injection of electrons and holes from opposite electrodes, and transport by hopping from one molecular site (or polymer chain) to another. Electron and hole capture one another when they are held within their mutually attractive potential, and this process is usually described using the Langevin model[19,20]. Typical capture radii are about 10 nm. The distinction between molecular semiconductors and conjugated polymers is that this distance is considerably greater than a molecular dimension, but comparable to the delocalization lengths for electron and hole wavefunctions on polymer chains. Therefore, for molecular materials, electron–hole capture is achieved at a range where only the Coulomb interaction is effective, and the process is independent of the final spin state of the exciton (even though the rates for the final step of exciton formation may be spin-dependent). In contrast, for the polymers, when electron and hole are present on the same chain at the capture range, the interaction between them results also from direct overlap of electron and hole wavefunctions, and is therefore spin-dependent (through the exchange interaction). Thus, the probability of electron–hole capture is now spin-dependent. Our results demonstrate that singlets are favoured over triplets, and there are a number of processes which might be responsible for this[5,18,21–23]. These include the greater spatial extension along the polymer chain of the singlet exciton, giving a stronger longer-range attraction[14]; or the closer energy match between the electron–hole and the singlet exciton compared to the triplet exciton[18]. Spin-dependent interactions at this point of electron–hole capture give spin-dependent singlet–triplet generation fractions because the probability of forming the exciton over electron and hole moving apart is spin-dependent.

Thus, direct observation of triplet emission has allowed us to demonstrate that there is a different quantum-mechanical process of electron–hole capture in operation in organic compounds with an extended conjugated system as compared to small conjugated molecules. In particular, the process of electron–hole capture in conjugated polymers is dependent on the final spin state. The high singlet generation fractions found in conjugated polymers[3–5] suggest that it may not be necessary to harvest triplets in these materials in order to create efficient LEDs. □

Methods

Single-layer light-emitting diodes of the platinum-containing polymer and monomer were fabricated according to the structure shown in Fig. 1 by spin-coating and subsequent thermal evaporation of the metal electrodes. Measurements of photoluminescence and electroluminescence were made with the LEDs in a continuous-flow helium cryostat. For photoluminescence, excitation was provided by the 457-nm line of a continuous wave argon ion laser, incident almost perpendicular to the indium-tin oxide (ITO) side of the devices. Measurements of electroluminescence spectra were made with the devices in exactly the same configuration as for photoluminescence and with a constant voltage supplied by a Keithley 230 voltage source. The photoluminescence and electroluminescence emission spectra were recorded perpendicular to the devices by using a spectrograph with an optical fibre input coupled to a cooled charge-coupled device (CCD) array (Oriel Instaspec IV). For the photoluminescence lifetime measurements, the tripled output from a Q-switched YAG laser was used (355 nm, ~15 ns pulses). For the electroluminescence lifetime measurements, square wave electrical pulses (15–30 V, 500 μs pulses) were applied to the devices. In both cases the transient emission was recorded by using a photomultiplier tube and a digital oscilloscope. Lifetimes were calculated by fitting the decay curves to an exponential. All measurements were made under vacuum or in a He atmosphere of 10 mbar.

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Superconductivity in single crystals of the fullerene C_{70}

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The observation of superconductivity in doped C_{60} has attracted much attention[1–3], as these materials represent an entirely new class of superconductors. A maximum transition temperature (T_c) of 40 K has been reported[4] for electron-doped C_{60} crystals, while a T_c of 52 K has been seen[5] in hole-doped crystals; only the copper oxide superconductors have higher transition temperatures. The results for C_{60} raise the intriguing questions of whether conventional electron–phonon coupling alone[1] can produce such high transition temperatures, and whether even higher transition temperatures might be observed in ther fullerenes[6–8]. There have, however, been no confirmed reports of superconductivity in other fullerenes, though it has recently been observed in carbon nanotubes[9]. Here we report the observation of superconductivity in single crystals of electric-field-doped C_{70}. The maximum transition temperature of about 7 K is achieved when the sample is doped to approximately four electrons per C_{70} molecule, which corresponds to a half-filled conduction band. We anticipate superconductivity in smaller fullerenes at temperatures even higher than in C_{60} if the right charge density can be induced.

Metallic behaviour is expected for KC_{70} and K_4C_{70} owing to the half-filling of the lowest unoccupied molecular orbital bands in K-intercalated C_{70}. An initial transport study on K-intercalated C_{70} found a maximum conductivity of ~2 S cm^{-1} (ref. 10). Theory and experiment showed that K_4C_{70} exhibits a larger conductivity because of its higher density of states[11–13]. Pure C_{70} and alkali-metal-doped C_{70} show non-zero resistance down to 1.8 K. The absence of superconductivity in these experiments is not well understood, and might be related to disorder and structural defects in the K_4C_{70} thin films. A weak electron–phonon interaction[11,14] and a reduced density of states at the Fermi level[15] have also been invoked as reasons for the apparent lack of superconductivity. We note, however, that most experiments have been performed on polycrystalline material, and phase-pure alkali-doped C_{70} analogues of A_3C_{60} have not been reported. In addition, various crystallographic structures of C_{70} have been observed[16]. Here we have chosen a different approach to induce electric charge in C_{70} crystals. We have recently demonstrated that the electrical properties of organic materials can be investigated over a wide range of charge density using field-effect doping, without inducing additional disorder[5,17–19], leading to gate-induced superconductivity in a variety of molecular organic crystals[5,17,18]. This method therefore seems to be well suited to our investigation of the reasons for the absence of superconductivity in the higher fullerenes—is it related to intrinsic properties, or to difficulties in chemical doping? Here we apply this technique to investigate the possibility of superconductivity in high-quality C_{70} single crystals.

We grew single crystals of C_{70} (smaller than 1 mm^3) from the vapour phase in a stream of hydrogen; the experimental conditions were similar to those used to grow C_{60} (ref. 5). The crystals were annealed in a xenon atmosphere, but we detected no incorporation of the inert gas into the crystals. We performed an X-ray structural analysis of the C_{70} single crystals, which showed them to be hexagonal closed packed (h.c.p.) C_{70}, with lattice parameters a = 10.602(9) Å and c = 17.263(13) Å. Previous studies of hexagonal C_{70} gave lattice parameters of a = 10.104 Å and c = 18.584 Å, with a wide mosaic spread of the order of a few degrees[20]—furthermore, these crystals showed diffuse rods typical of stacking faults[21]. In contrast, our crystals show a much narrower mosaic of the order of 0.4°. In addition, the c/a ratio for our crystals is close to the ideal value of 1.63 for sphere packing, in contrast to the reported value of 1.84. To first order, it is possible to approximate the ellipsoidal C_{70} molecule by a hollow sphere with radius r = 3.78 Å, and we obtained a residual of R = 0.065 for 118 independent reflections measured. As stacking faults were expected to be present, we looked for diffuse rods of intensity. Instead, we found well developed superstructure reflections with a mosaic spread of the order of 0.4° consistent with 6H polytypes, leading to a tripling of the c axis ($3c$ = 51.79 Å). Different 6H stacking sequences are expected, producing twinning at room temperature. On average, five layers are stacked coherently, with the sixth in either the h.c.p. or the cubic close packed (c.c.p.) position. Low-temperature X-ray diffraction revealed a further lowering of symmetry, but the crystals clearly undergo multiple twinning upon cooling. This lowering of the symmetry is indicative of a transition to a phase in which the C_{70} molecules no longer rotate freely. However, we do not expect that the orientational order of the molecules will be complete, similar to the phase transition observed for C_{60} upon cooling[22]. Further structural studies at low temperature are under way.

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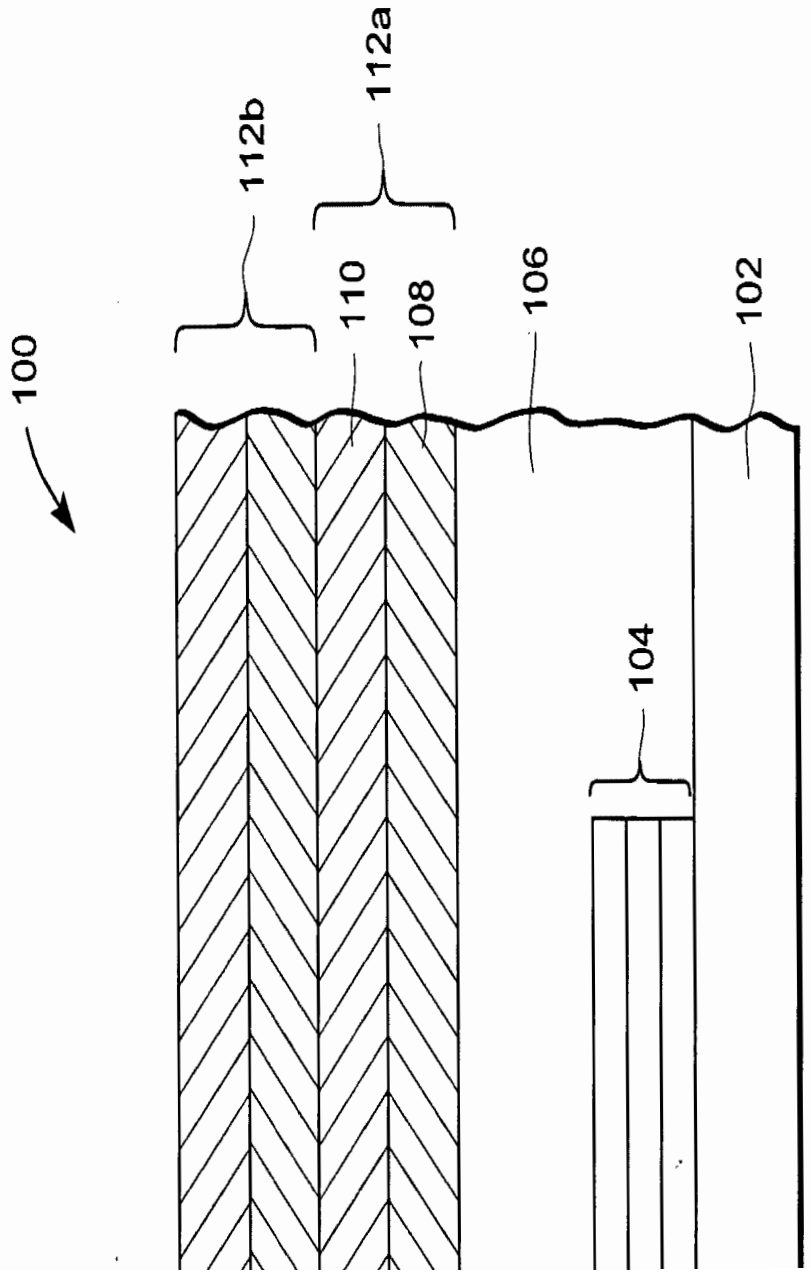


FIG. 1 (PRIOR ART)

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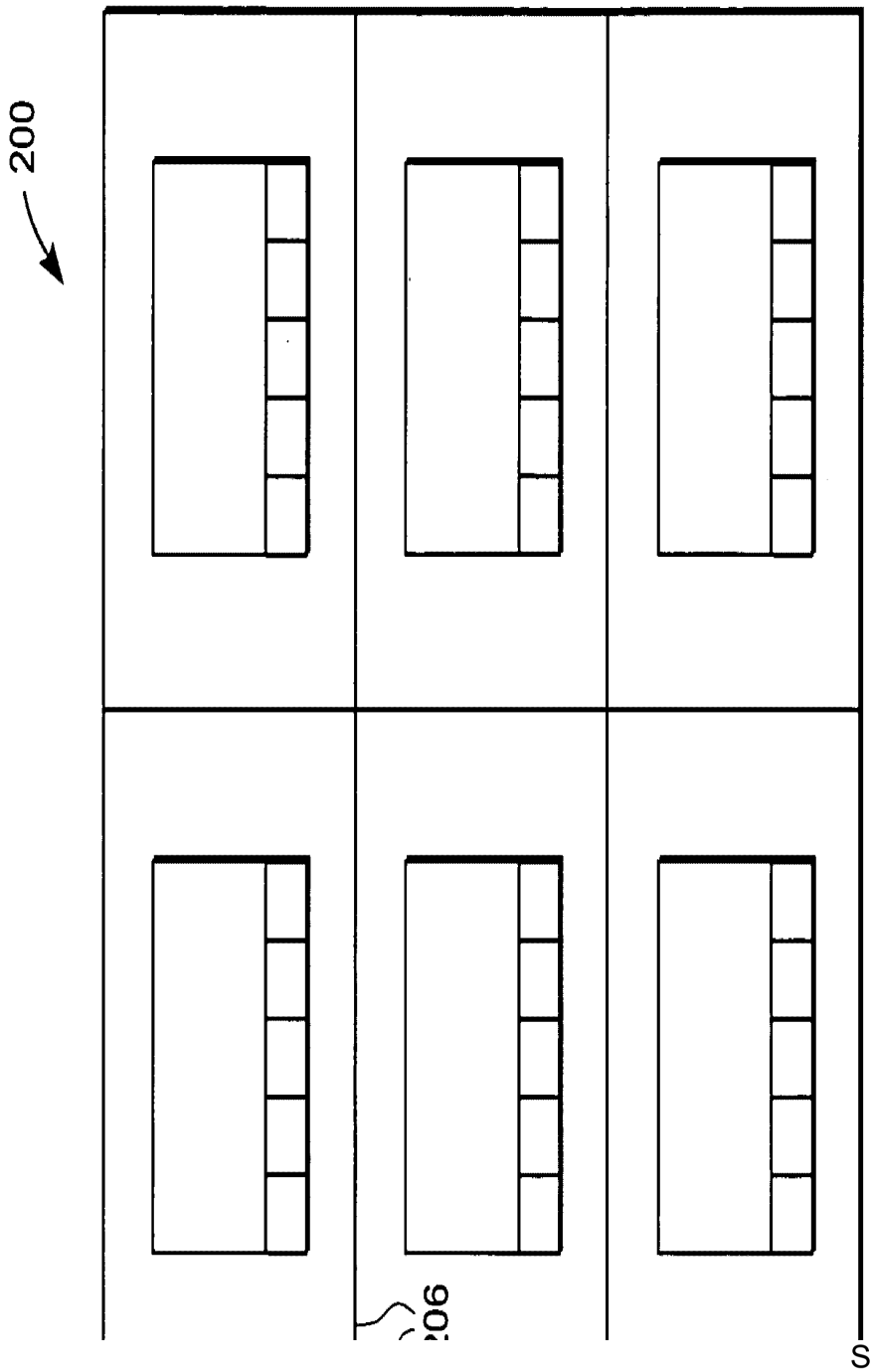


FIG. 2 (PRIOR ART)

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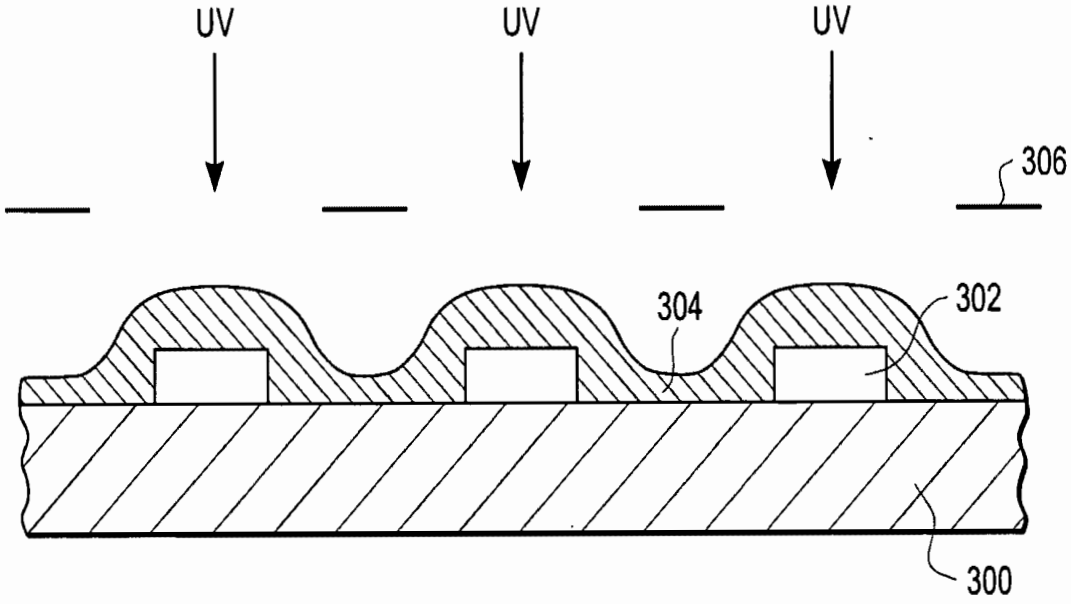


FIG. 3A

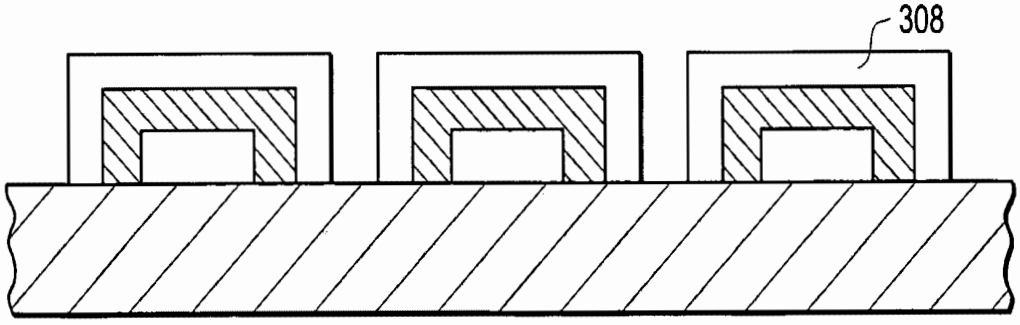


FIG. 3B

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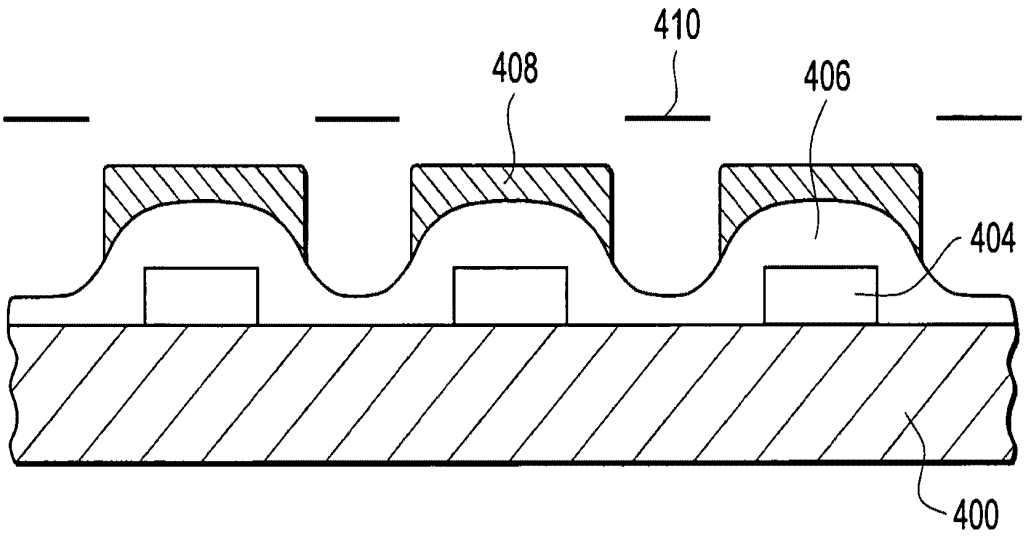
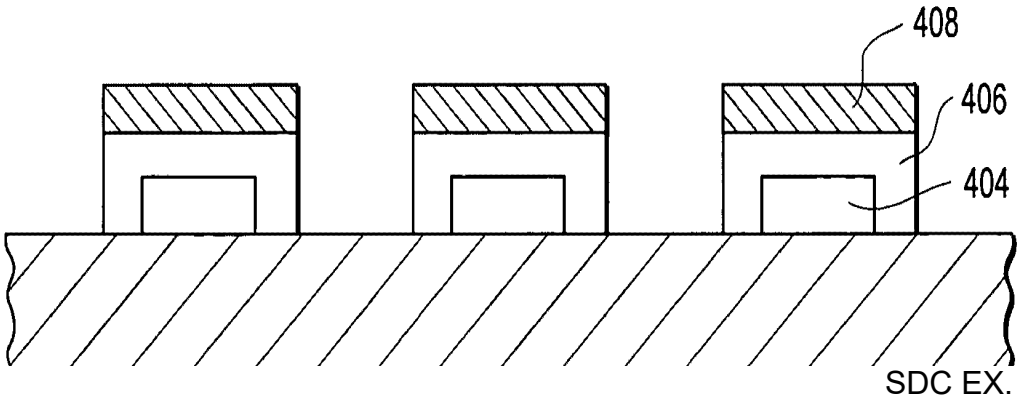


FIG. 4A



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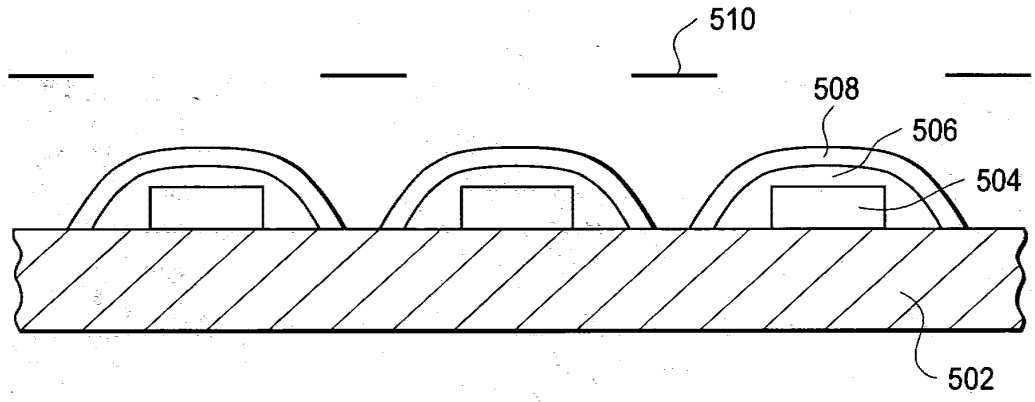


FIG. 5

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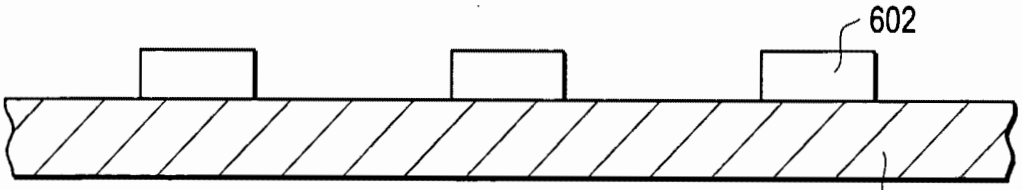


FIG. 6A

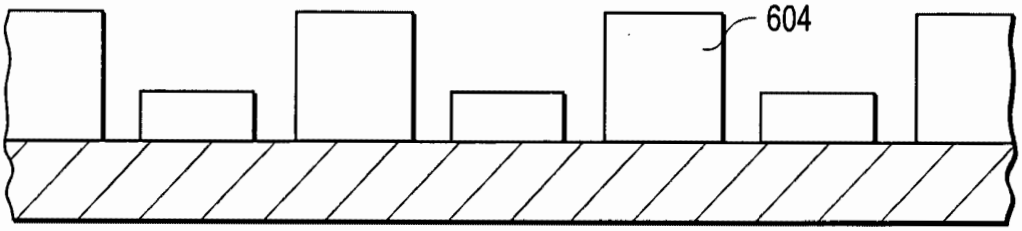


FIG. 6B

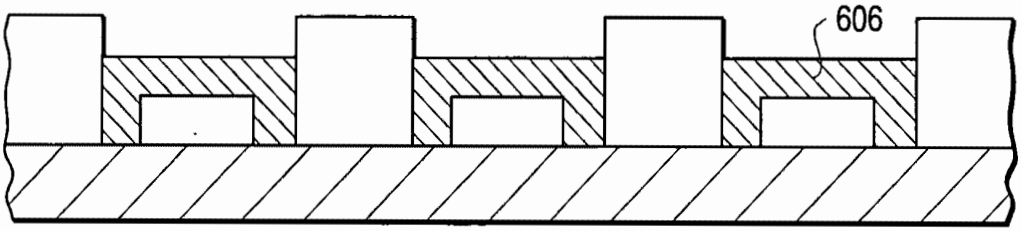


FIG. 6C

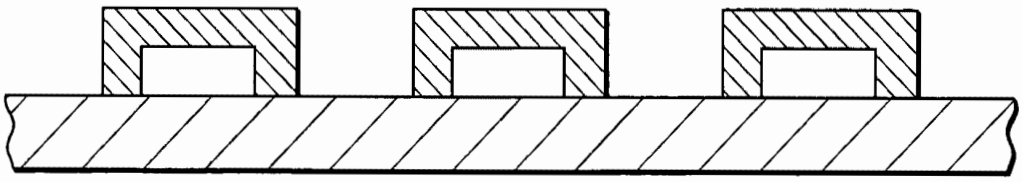
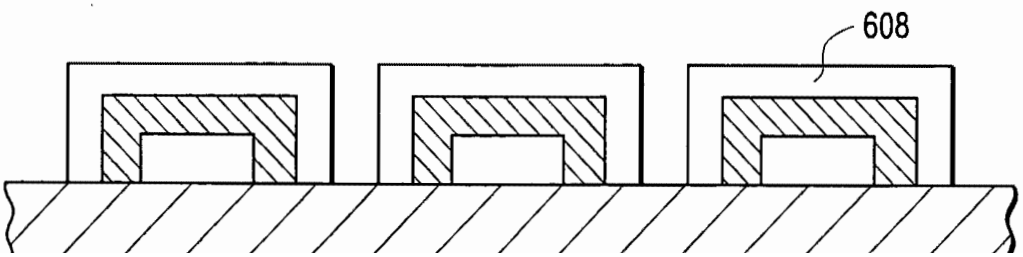


FIG. 6D



DEFENDANT'S EXHIBIT

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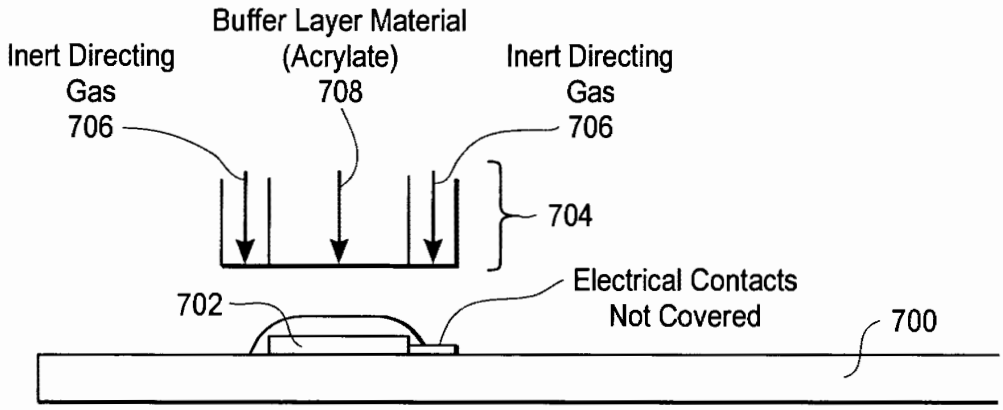


FIG. 7A

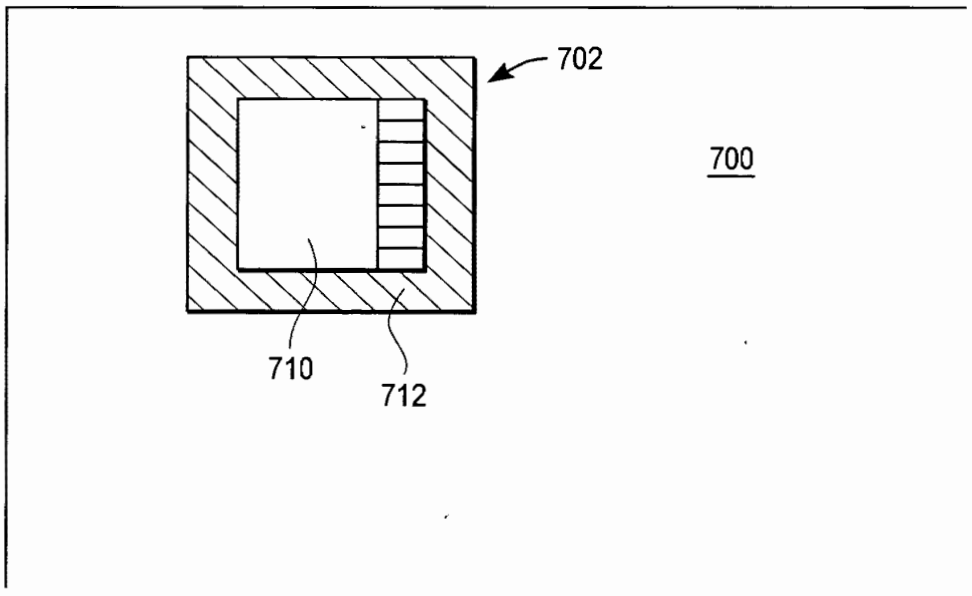


FIG. 7B

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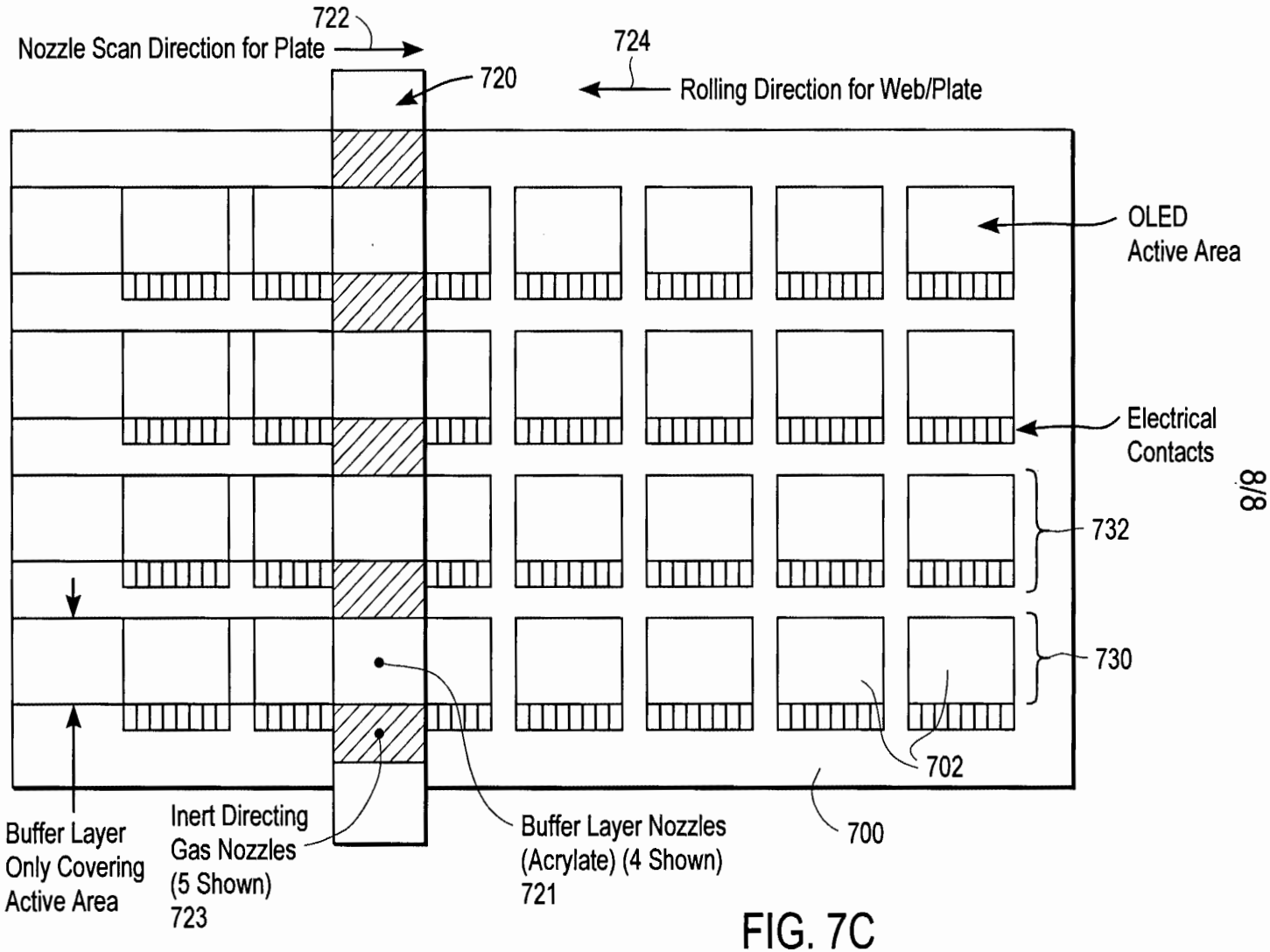


FIG. 7C

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/137,163	05/02/2002	Karl Pichler	2002P03156US	1705

7590 06/19/2003

Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

EXAMINER
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/137,163	PICHLER ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-58 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-58 is/are rejected.

7)☒ Claim(s) 14,16 and 56 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 May 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

SDC EX. 1002 - 208/544

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The **abstract** should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and **"said," should be avoided**. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

Claim Objections

2. Claim 14 is objected to because of the following informalities: in-consistent terminologies. Claim 14 recites " the at least one organic layer that are not cross-linked", whereas its base claim 1 recites " the at least one planarization layer that are not hardened."

Claim 16, at line 31," **the** OLED plate" lacks an antecedent basis.

Claim 56, at lines 1-2, " depositing a layer over a plurality of devices" should be -- depositing **the at least one planarization** layer over a plurality of devices --. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 24 recites the limitation "the light emissive areas" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 10-12, 19-21, 25-27, 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujii et al. (US 5,703,433).

In re claims 1, 10, 20, 21, 25-27, 34, Fujii et al., in Fig. 1A-1F and related text, teach a method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

- fabricating a plurality of devices 2 on a substrate 1 (Fig.1A);
- depositing at least one planarization layer 4 (a photoresist layer, which is known to the ordinary skilled in the art be an organic layer) as an unpatterned liquid film upon said devices 2 (Fig.1B);
- hardening or curing said at least one planarization layer 4 by UV light 6 in a patterned manner through a mask 5 such that the hardened region (i.e. exposed area) substantially covers said device 2 (Fig.1C);
- removing unwanted areas of the at least one planarization layer that are not hardened (i.e. the un-exposed areas) (Fig.1D); and

- selectively depositing at least one barrier layer 3 (i.e. a dielectric, fluorescent paste, col. 4, line 27) over said hardened region, i.e. selectively the barrier layer 3 on the sidewalls of the hardened region and the device 2 (Fig.1F).

In re claims 11 and 12, Fujii et al. also inherently teach that the step of hardening said at least one plananzation layer in a patterned manner comprises exposure by UV light comprising an optical patterning system or an UV-beam scanning system, wherein the system comprises the UV light 6 and the mask 5.

In re claim 19, Fujii et al. further teach that the step of removing areas of the at least one planarization layer that are not hardened comprises rinsing, i.e. rinsing by spraying in an aqueous solution of sodium carbonate anhydride (col.4, lines 40-43).

7. Claims 47-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Yau et al. (US 6,072227).

Yau et al. teach the claimed method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

- fabricating a plurality of devices 310/300 on a substrate 304 (Fig. 6A);
- depositing at least one planarization layer 302 upon said devices 310/300 (Fig.6B); and
- depositing at least one barrier layer 312 over planarization layer 302 wherein at least one said step is accomplished in an inert atmosphere, i.e. accomplished in an inert atmosphere is the step of depositing the planarization layer or the step of depositing the barrier layer or both the step of depositing the planarization layer and the step of depositing the barrier layer (col. 9, lines 55-58, col.11, lines 54-57).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 41, 43, 44, 45 are rejected under 35 U.S.C. 102(e) as being anticipated by Palmans et al. (US 6,271,135).

In re claim 41, 43 and 45, Palmans et al. teach the claimed method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

- fabricating a plurality of devices 2 on a substrate 1 (Fig,1A);
- depositing a mask 3 on top of said substrate 1, such that mask openings 4 are placed on top of said devices 2 and in contact with said substrate 1 (Fig.1B), wherein said mask 3 is a polymer (col. 5, lines 27-29);
- depositing at least one planarization layer 5 upon said mask 3 (Fig.1C);
- removing said mask 3 from said substrate 1 (Fig.1D); and
- selectively depositing at least one barrier layer 6 over said planarization layer 5 (Fig.1E and col. 6, line 67 through col.7, line 4).

In re claim 44, Palmans et al. also inherently teach depositing a mask 3, said mask 3 comprising a material substantially non-sticking to the substrate 1 over the areas in between the

active areas because the mask can be easily removed from the substrate 1, i.e. non-sticking to the substrate 1.

10. Claims 51-55 and 57 are rejected under 35 U.S.C. 102(e) as being anticipated by Marsh (US 6,387,802).

In re claims 51-54, Marsh teaches the claimed method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

- fabricating a plurality of devices 130/132/134 on a substrate 112 (Fig.4);
- depositing at least one planarization layer 142/148 upon said devices 103/132/134 (Figs. 5-9);
- depositing at least one barrier layer 157 over planarization layer 142/148 (Fig.9); and
- depositing a secondary encapsulation layer 152 over said barrier layer 157 (Fig.10), wherein the secondary encapsulation layer 152 comprises depositing a metal (Pt); and wherein at least one said deposition step is accomplished by gas nozzle deposition (col. 4, lines 20-21).

In re claim 55, Marsh also teaches depositing a layer over a plurality of devices with an array of nozzles 28 positioned above said substrate 26 as shown in Fig.2.

In re claim 57, Marsh also teaches the claimed electronic device, said device comprising:

- a substrate 112;
- a plurality of active areas 130/132/134 disposed upon said substrate 112 (Fig.8);
- a plurality of planarization layers 142 and 146 disposed on said substrate 112 whereby said planarization layer 142 and 146 cover substantially only said active areas 103/132/134 (Fig.8); and

- a plurality of barrier layers 148 and 157 disposed on said substrate 112, whereby said barrier layers 148 and 157 cover substantially only said planarization layers 142 and 146 (Fig.9).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. (US '433) in view of Cheng et al. (US 6,524,937).

Fujii et al. do not expressly teach hardening the planarization layer by cross-linking (claim 13); and removing areas of the organic layer that are not cross-linked by thermal evaporation (claim 14) or by applying a short high temperature pulse (claim 15).

However, as the photoresist layer (i.e. the organic layer) is exposed to the UV light it would form cross-linking compound, as evidenced by Cheng et al. (col. 5, lines 30-31). Cheng et al. teach that the cross-linking of the photoresist layer can be achieved by exposing to a high temperature (col. 5,lines 63-67), which would cause thermal evaporation of solvent in the photoresist layer.

Therefore, it would have been obvious to one of the ordinary skilled in the art, at the time the invention was made, to utilize the methods of Cheng et al in the method of Fujii et al. to form cross-linking since by doing so it would form the planarization layer (i.e. the photoresist layer) with etch selectivity, which, in turn, is beneficial to the subsequent patterning step.

13. Claims 2-4, 6-9, 22-23, 30, 31, 33, 35, 36, 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. (US '433) in view of Amundson et al. (US 6,498,114).

In re claims 2-4, 6-9, 35, 36, 38-40, Fujii et al. do not teach depositing at least one planarization layer (the photoresist layer) by spin coating (claim 2) or evaporation (claims 3 and 4) or roll coating (claim 6) or dip coating (claim 7) or spray coating (claim 8) or screen printing (claims 9 and 36); and depositing an organic layer using ink jet processing (claim 35) or depositing the barrier layer using ink jet processing or screen printing (claims 38-40).

However, the aforementioned methods have been widely used for depositing the photoresist layer or an organic layer, as evidenced by Amundson et al.. Amundson et al., in col. 4, lines 56-62 and col. 7, lines 17-32, teach forming the planarization layer 20 (the photoresist layer) over a substrate 10 (Fig.1) using spin coating, evaporation, roll coating, dip coating, spray coating, screen printing, and ink jet printing process.

Therefore, it would have been obvious to one of the ordinary skilled in the art, at the time the invention was made, to utilize methods of spin coating, evaporation, roll coating, dip coating, spray coating, screen printing and ink jet processing as taught by Amundson et al for depositing the planarization layer or the organic layer or the barrier layer of Fujii et al. since these methods are good candidates for forming the aforementioned layers.

In re claims 22 and 23, one of the ordinary skilled in the art would have been motivated to select a desired material as the barrier layer of Fujii et al. and in a larger area than the planarization layer for a reasonable expectation of success, i.e. to obtain a satisfactory patterned layer over the plurality of devices.

In re claims 30, 31 and 33, Fujii et al. in view of Amundson et al also teach that removing said areas of unwanted planarization layer further comprises etching an organic layer since the planarization layer 4 (i.e. the photoresist layer) of Fujii et al. is usually an organic layer; and the unwanted portion (i.e. un-exposed portion) of the planarization layer 4 is etched away as shown in Fig.1D.

14. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. (US '433) in view of Massingill et al. (US 2002/0155661).

Fujii et al. do not teach depositing the planarization layer (the photoresist layer) by blade coating.

However, the aforementioned method has been widely used for depositing the photoresist layer, as evidenced by Massingill et al. in paragraph [0134], wherein they teach forming the photoresist layer comprising blade coating, roll coating, spray coating and screen printing.

Therefore, it would have been obvious to one of the ordinary skilled in the art, at the time the invention was made, to utilize the blade coating of Massingill et al for depositing the photoresist layer (i.e. the planarization layer) of Fujii et al. since the method is a good candidate for forming the planarization layer.

15. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. (US '433) in view of Fujibayasni et al. (US 5,369,151).

Fujii et al. do not teach removing areas of the planarization layer that are not hardened by pumping in a vacuum or by thermal evaporation and pumping in a vacuum.

However, removing the planarization layer by the thermal evaporation in a vacuum system has been widely used in the art, as evidenced by Fujibayasni et al. in col. 8, lines 42-47.

Therefore, it would have been obvious to one of the ordinary skilled in the art, at the time the invention was made, to utilize methods of Fujibayasni et al. for removing the unwanted planarization layer since by doing so it would satisfactory provide a patterned layer over the plurality of the devices.

16. Claims 28, 29 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. (US '433) in view of Dimitrakopoulos et al. (US 6,500,604).

In re claim 28 and 29, Fujii et al. do not teach depositing the planarization layer by evaporating a plurality of reactive organic molecules, said reactive organic molecules comprising a condensed conformal film on the substrate; and the planarization layer comprises one of a group, said group comprising a Parylene coating of said organic layer over the substrate, and a plasma-assisted organic material deposition.

However, Dimitrakopoulos et al. teach forming a planarization layer (i.e. a protective material layer) comprising a Parylene coating of said organic layer over the substrate, and a plasma-assisted deposition (col. 4, lines 16-17 and 45-46).

Therefore, it would have been obvious to one of the ordinary skilled in the art, at the time the invention was made, to utilize the plasma-assisted depositing methods of Dimitrakopoulos et al. in the method of Fujii et al. since by doing so it would satisfactory form the planarization layer comprising Parylene.

In re claim 32, Fujii et al. do not teach removing said areas of unwanted planarization layer by one of a group, said group comprising etching an organic layer with a plasma-assisted etching process, oxygen plasma, reactive ion-etch, anisotropic etch, laser assisted/based removal and laser ablation.

However, utilizing the aforementioned methods for patterning the planarization layer has been widely used in the art, as evidenced by Dimitrakopoulos et al. in col. 5, lines 40-45, wherein the reactive ion-etch and plasma-assisted etching are used.

Therefore, it would have been obvious to one of the ordinary skilled in the art, at the time the invention was made, to utilize the removing methods of Dimitrakopoulos et al. in the method of Fujii et al. since by doing so it would satisfactory remove the unwanted portion of the planarization layer.

17. Claims 16 and 24 rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. in view of Amundson et al. as applied to claims 1 and 14-15 above, and further in view of Dimitrakopoulos et al. (US '604).

In re claims 16 and 24, one of the ordinary skilled in the art would have been motivated to apply Fujii's teachings to any situation that requires encapsulating layer formed over the devices such as OLED, in light of teachings of Dimitrakopoulos et al. since Fujii's teachings is illustrative rather than restrictive. Dimitrakopoulos et al. teach forming planarization layer 16 in the processing of forming the OLED (col.1, lines 11-16).

18. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. (US '433) in view of Kim et al. (US 6,146,715).

Fujii et al. do not teach selectively depositing the planarization layer through a shadow mask.

However, by utilizing the shadow mask for selectively deposition has been widely used in the art for the advantage of simplicity, as evidenced by Kim et al (col. 1, line 64 through col.2,

line 1), wherein Kim et al. teach selectively depositing a layer 4 over the substrate 1 by through the shadow mask 5 (Fig.2).

Therefore, one of the ordinary skilled in the art would have been motivated to apply the selective deposition method of Kim et al. for depositing the planarization layer of Fujii et al. since it would provide a simple means for depositing the desired layer in selective areas.

19. Claims 42 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palmans et al. (US '135) in view of Tobben et al. (US 6,103,456).

In re claims 42 and 46, Palmans et al. do not teach depositing a laminated-film mask (claim 42), wherein the laminated-film mask is formed by depositing an organic layer over the entire mask (claim 46).

However, Tobben et al., in an analogous art of patterning, teach depositing a laminated-film mask 24/25 by depositing one organic layer 25 over the entire mask 24 (Fig.1B) for the purpose of avoiding light reflection during patterning (col.1, lines 52-56).

Therefore, one of the ordinary skilled in the art would have been motivated to substitute the single mask of Palmans et al with the laminated-film mask of Tobben et al. for the purpose of improving patterning accuracy.

20. Claims 56 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marsh (US '802) in view of Cui et al. (US 6,148,764).

In re claim 56, Marsh does not teach that the step of depositing a layer over a plurality of devices comprises moving said array and said substrate in relative motion.

However, Cui et al., in a gas nozzle deposition processing, teach utilizing an array of nozzle (i.e. multiple jets) with moving the array of nozzles in relative to the substrate (col. 2, lines 21-40) for the purposes of improving film uniformity and covering larger area.

Therefore, one of the ordinary skilled in the art would have been motivated to combine the method of Cui et al. with the method of Marsh since by doing so it would improve film uniformity.

In re claim 58, one of the ordinary skilled in the art would have been motivated to apply the method of Marsh to provide the electronic device having OLED or organic electronic circuit, or organic detector or organic solar cell without departing the spirit and scope of Marsh (col.8, lines 35-46) since the teachings of Marsh is illustrative rather than restrictive.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien-Ming Lee
Examiner
Art Unit 2823

June 12, 2003

Notice of References Cited	Application/Control No. 10/137,163	Applicant(s)/Patent Under Reexamination PICHLER ET AL.	
	Examiner Hsien-Ming Lee	Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,703,433	12-1997	Fujii et al.	313/484
	B	US-6,072,227	06-2000	Yau et al.	257/642
	C	US-6,271,135	08-2001	Palmans et al.	438/687
	D	US-6,387,802	05-2002	Marsh	438/680
	E	US-6,524,937	02-2003	Cheng et al.	438/574
	F	US-6,498,114	12-2002	Amundson et al.	438/780
	G	US-2002/0155661	10-2002	Massingill et al.	438/244
	H	US-5,369,151	11-1994	Fujibayashi et al.	523/414
	I	US-6,500,604	12-2002	Dimitrakopoulos et al.	430/322
	J	US-6,146,715	11-2000	Kim et al.	427/555
	K	US-6,103,456	08-2000	Tobben et al.	430/317
	L	US-6,148,764	11-2000	Cui et al.	118/723 ME
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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	P					
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US 20020155661A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2002/0155661 A1

Massingill et al. (43) Pub. Date: Oct. 24, 2002

(54) MULTI-CHIP MODULE AND METHOD FOR FORMING AND METHOD FOR DEPLATING DEFECTIVE CAPACITORS

(76) Inventors: Thomas J. Massingill, Scotts Valley, CA (US); Mark Thomas McCormack, Livermore, CA (US); Wen-Chou Vincent Wang, Cupertino, CA (US)

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Third Floor
600 Beach Street
San Francisco, CA 94109 (US)

(21) Appl. No.: 09/997,589

(22) Filed: Nov. 29, 2001

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/429,854, filed on Oct. 28, 1999. Continuation-in-part of application No. 09/956,605, filed on Sep. 18, 2001.

Publication Classification

(51) Int. Cl.[7] G03F 7/00; H01L 21/8242

(52) U.S. Cl. 438/244; 430/311; 430/313

(57) ABSTRACT

A method for deplating defective capacitors comprising forming a plurality of capacitors on a semiconductor substrate, forming a plurality of metal contacts on the plurality of capacitors, and depositing a layer of photoresist on the semiconductor substrate. The photoresist layer is patterned so that the plurality of metal contacts are exposed, which are then contacted with an electrically conductive solution. The metal contacts, which are disposed over defective capacitors, are subsequently deplated. A method for forming a multi-chip module comprising forming a thin-film polymeric interconnect structure having a pair of sides, one of which is disposed on a silicon substrate having active or passive devices and the other of which has a computer chip mounted thereon. A multi-chip module formed by the method.

Following a planarization step, another conformal polymer layer is deposited upon which fuurther circuit buildup may take place. An optional ground layer may be deposited prior to second layer buildup for dimensional stability and/or electrical performance.

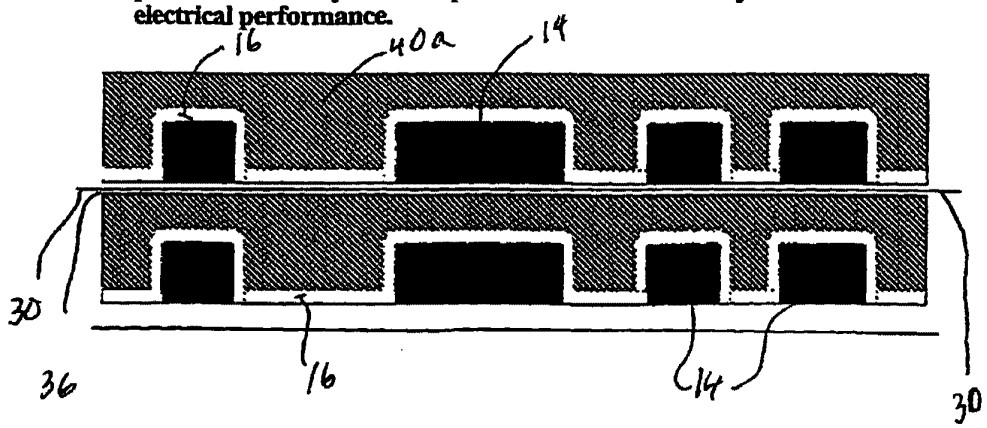


Figure 1: Conf rmal Polymer Layer(s) on Substrate/Conductors/Previous Layers (Ground metallization over conformal coating is optional)

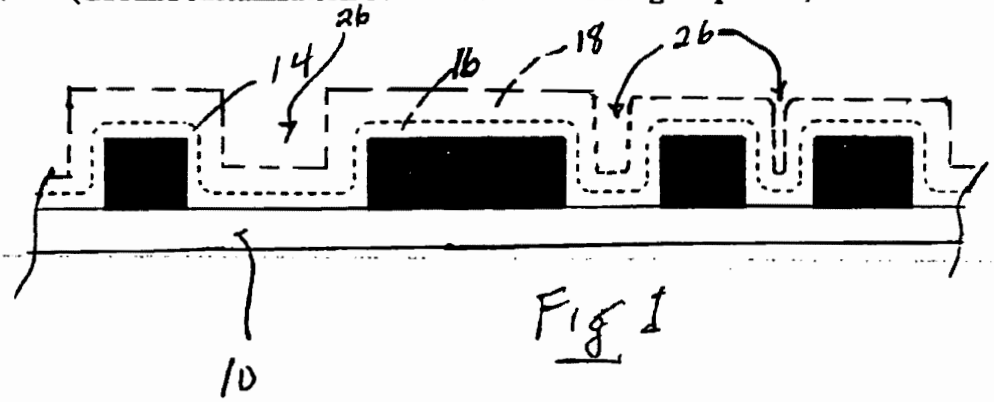


Fig 1

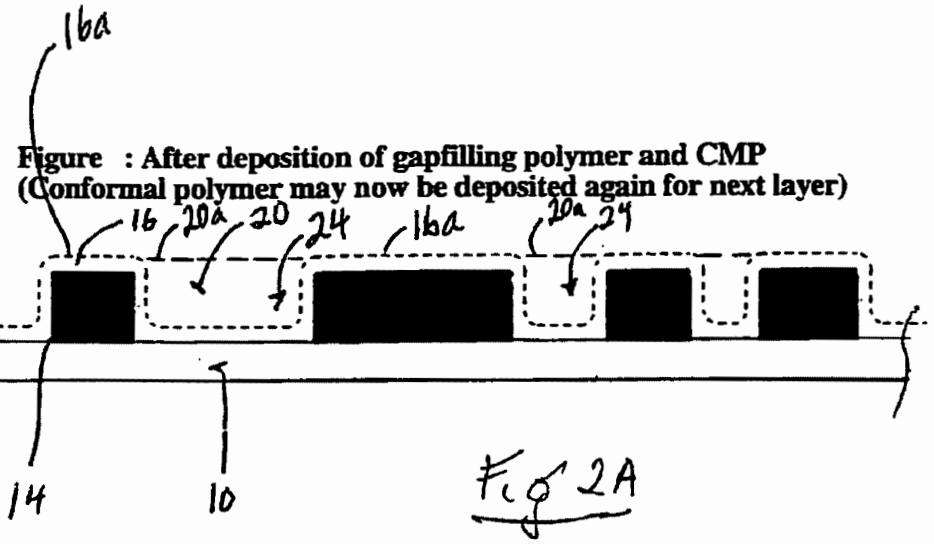


Figure : After deposition of gapfilling polymer and CMP (Conformal polymer may now be deposited again for next layer)

Fig 2A

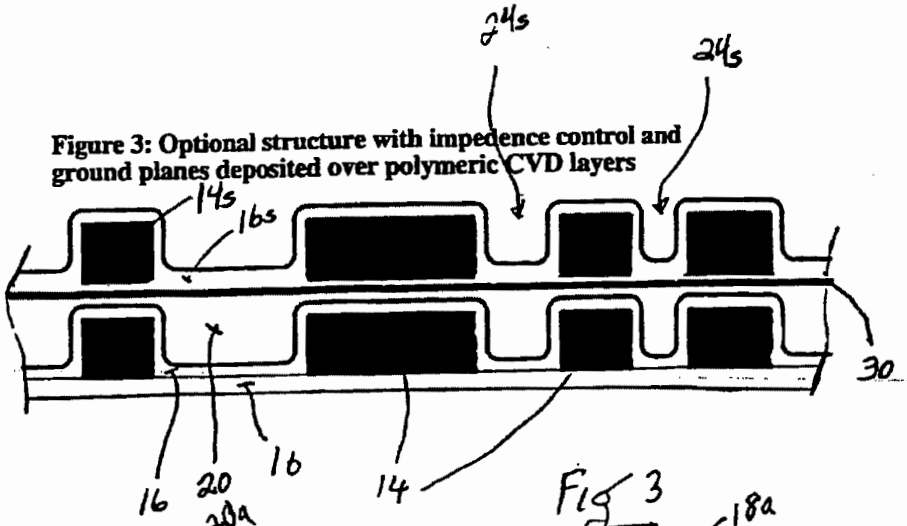


Figure 3: Optional structure with impedence control and ground planes deposited over polymeric CVD layers

Fig 3

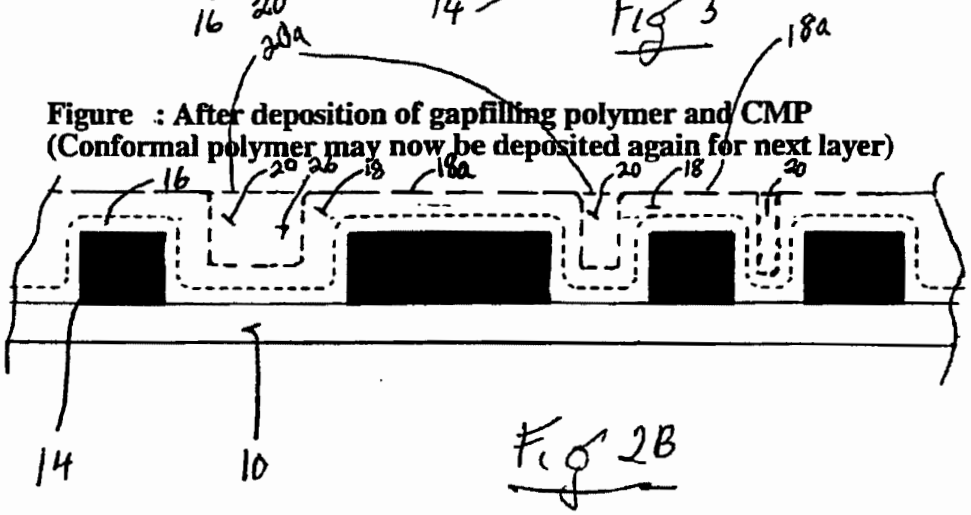


Figure : After deposition of gapfilling polymer and CMP (Conformal polymer may now be deposited again for next layer)

Fig 2B

Figure 1: a) Circuit on substrate with Conformal Polymer Layer(s) on Substrate/Conductors/Previous Layers.
b) Masking can be used to make polymer layer discontinuous from conductor to conductor.

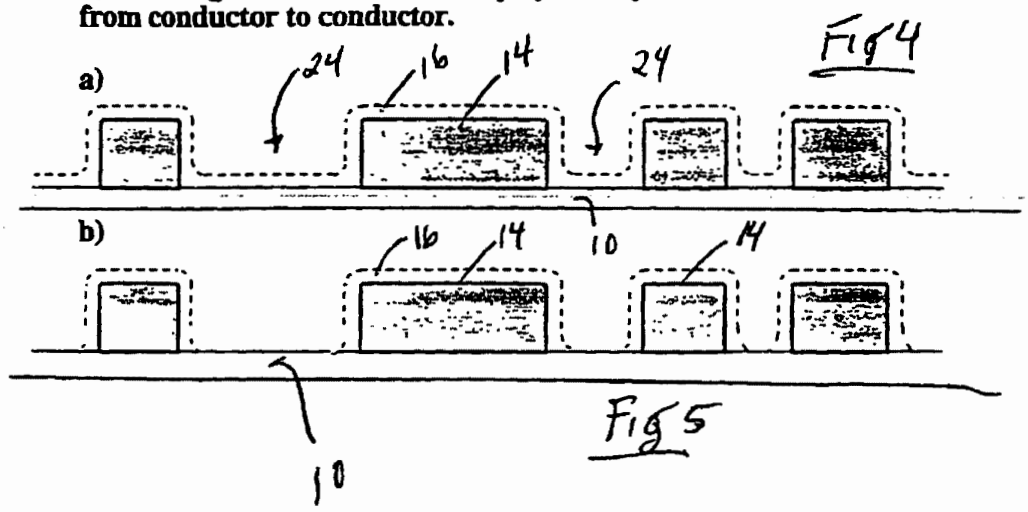


Figure 2: Organic or Inorganic gap filling layer is provided. This layer may be continuous or discontinuous (foam or full of voids/cracks. Previous conformal layer serves as adhesion promoter, and diffusion barrier.

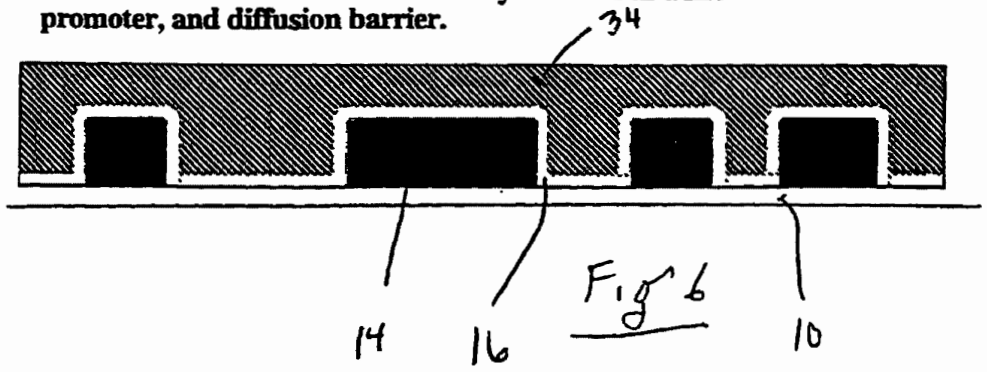


Fig 7

Figure 3: Planarizing Layer(s) to act as compliant sealant layers, facilitate CMP and further buildup

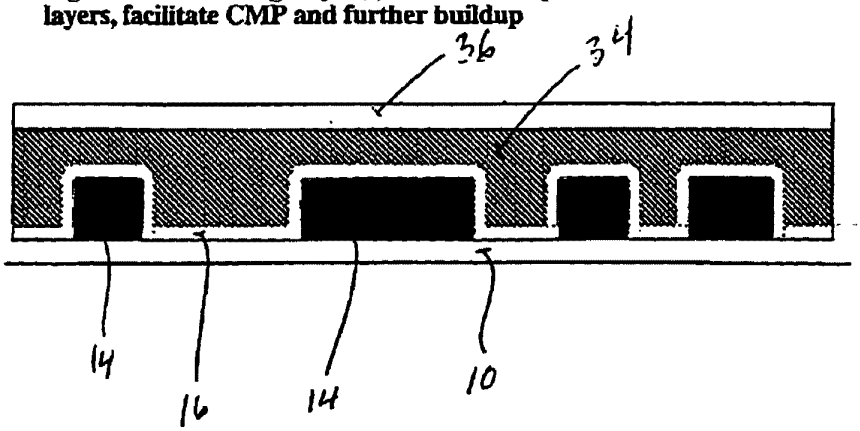


Fig 8

Figure 4:
Shown with subsequent build up of successive layer.

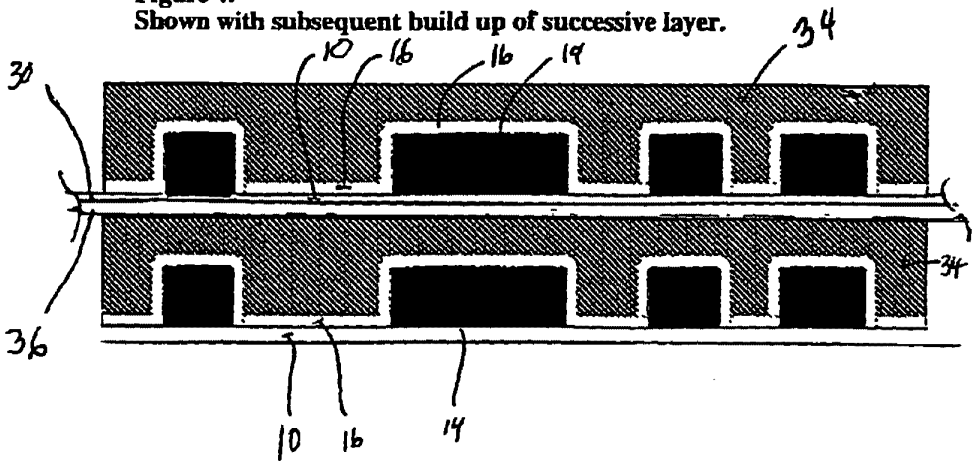
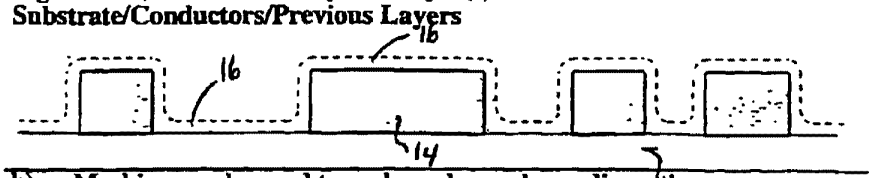


Fig 9

Figure 1: a) Conformal Polymer Layer(s) on Substrate/Conductors/Previous Layers



b) or Masking can be used to make polymer layer discontinuous from conductor to conductor.

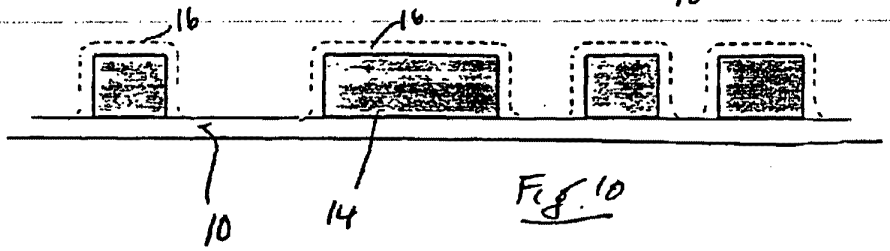


Fig 10

Figure 2: Application of Low Dielectric Constant Thermoplastic Particulates.

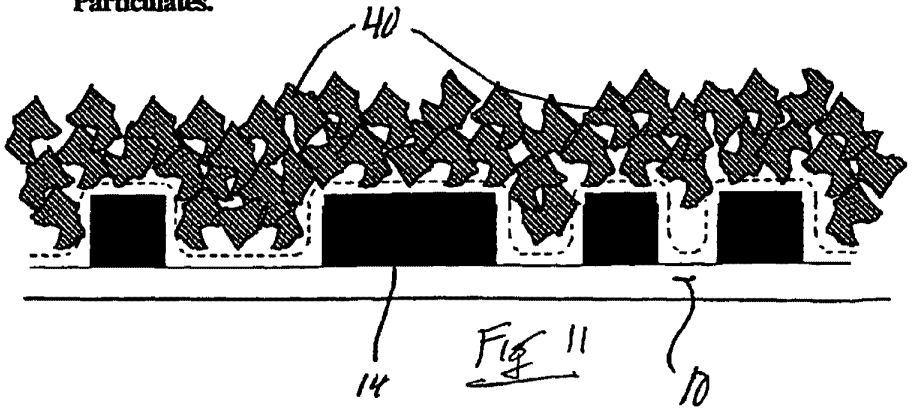


Fig 11

Figure 3: Foll wing Thermal Treatment (e.g., autoclave or lamination). Possible Voids may be retained in thermoplastic region.

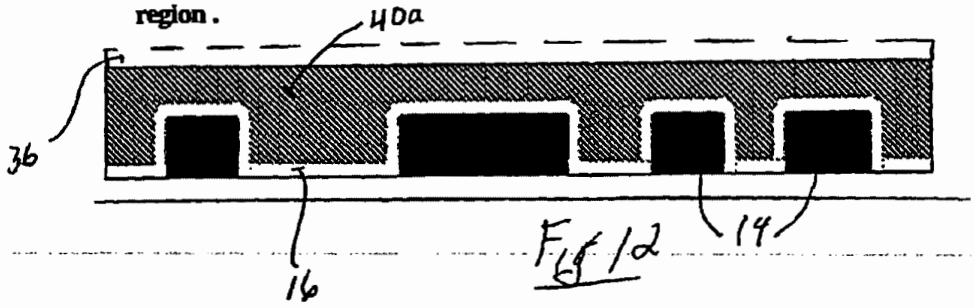


Fig 12

Figure 4: Following a planarization step, another conformal polymer layer is deposited upon which fuurther circuit buildup may take place. An optional ground layer may be deposited prior to second layer buildup for dimensional stability and/or electrical performance.

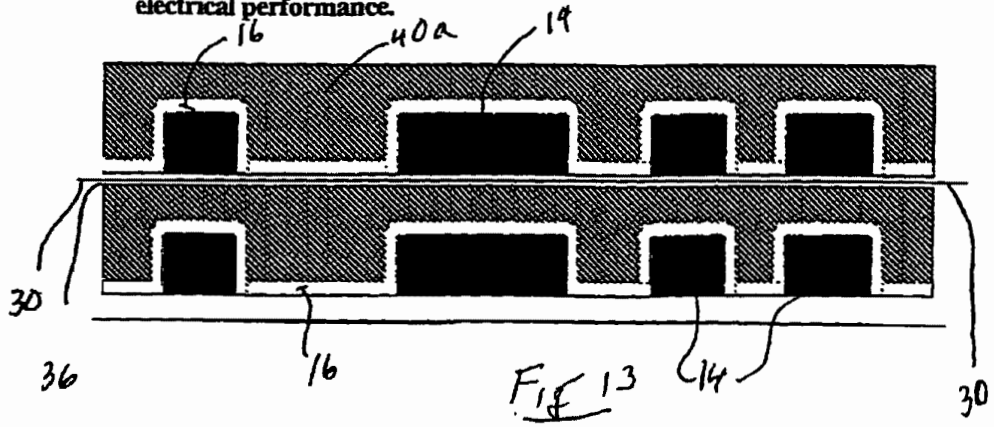
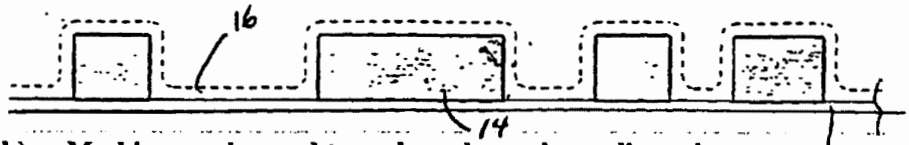


Fig 13

Fig 14

Figure 1: a) Conformal Polymer Layer(s) on Substrate/Conductors/Previous Layers



b) or Masking can be used to make polymer layer discontinuous from conductor to conductor.

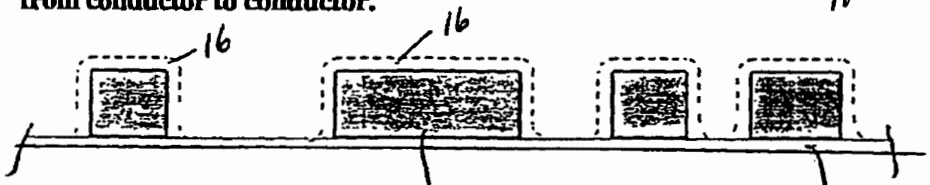


Fig 15

Figure 2: Application of Composite Low Dielectric Constant Polymer Particulates within another planarizing Low Dielectric Constant Polymer. Particulates may be co-sprayed with the fluid, pressed into fluid or the fluid may be spun on lightly compressed (and/or partially sintered) particulates. Alternatively the particulates may be precipitated out of solution. After Curing an additional CMP step may be performed.

Fig 16

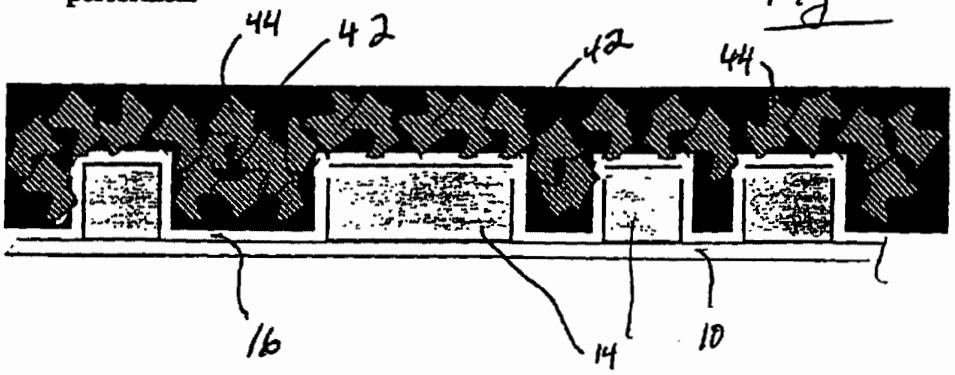


Figure 3: Another conformal polymer layer is optionally deposited upon which further circuit buildup may take place. An optional ground layer may be deposited prior to second layer buildup for dimensional stability and/or electrical performance.

Fig 17

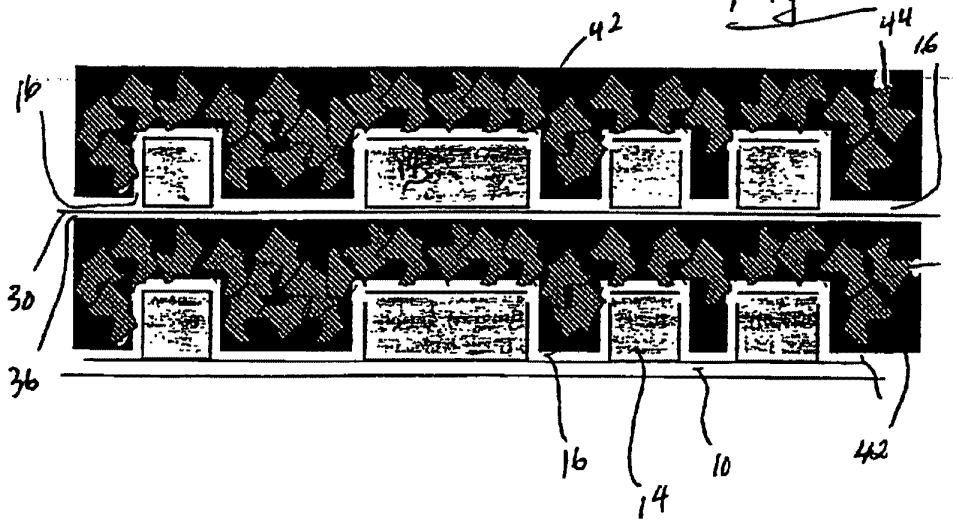
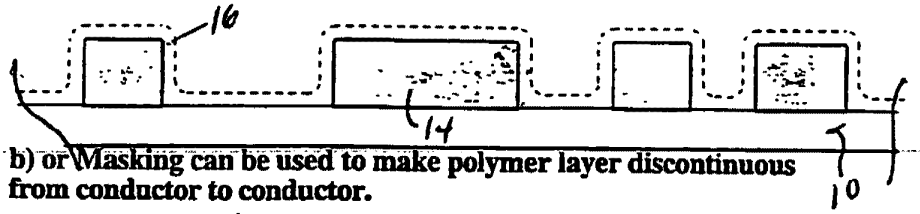


Figure 1: a) Conformal Polymer Layer(s) on Substrate/Conductors/Previous Layers

Fig 18



b) or Masking can be used to make polymer layer discontinuous from conductor to conductor.

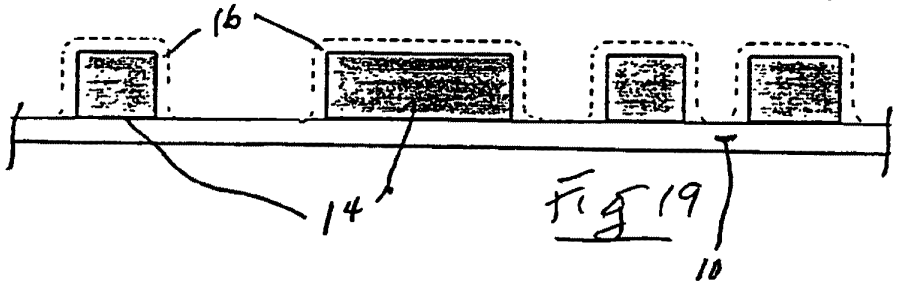


Fig 19

Figure 2: Thermoplastic Low Dielectric Constant Polymer Film is placed on top of circuitry.

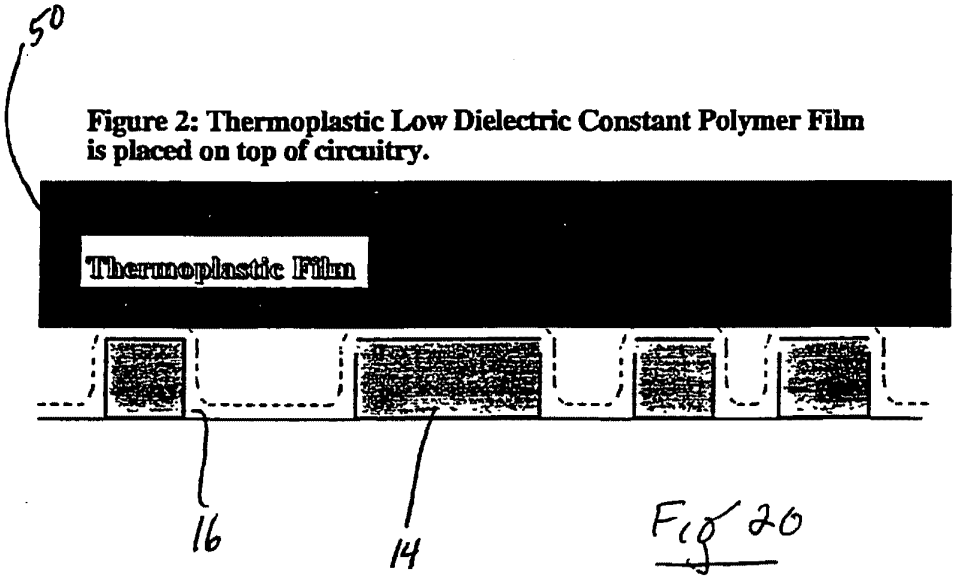


Fig 20

Figure 3:
Thermal Application of Therm plastic Low Dielectric Constant Polymer Film. Film may be laminated or autoclaved. Another conformal polymer layer is optionally deposited upon which further circuit buildup may take place. Another option is to combine a planarizing layer deposited over the surface to facilitate CMP. An optional ground layer may be deposited prior to second layer buildup for dimensional stability and/or electrical performance.

Fig 21

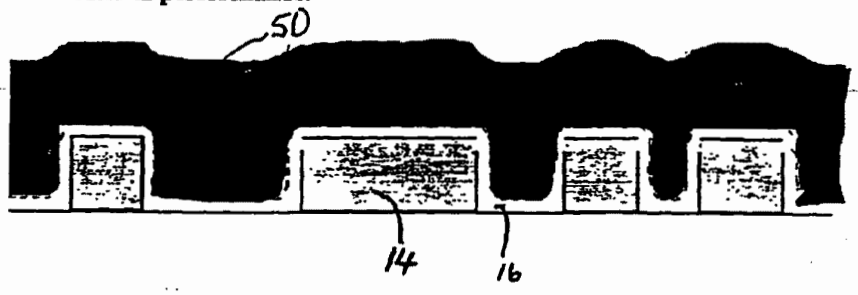
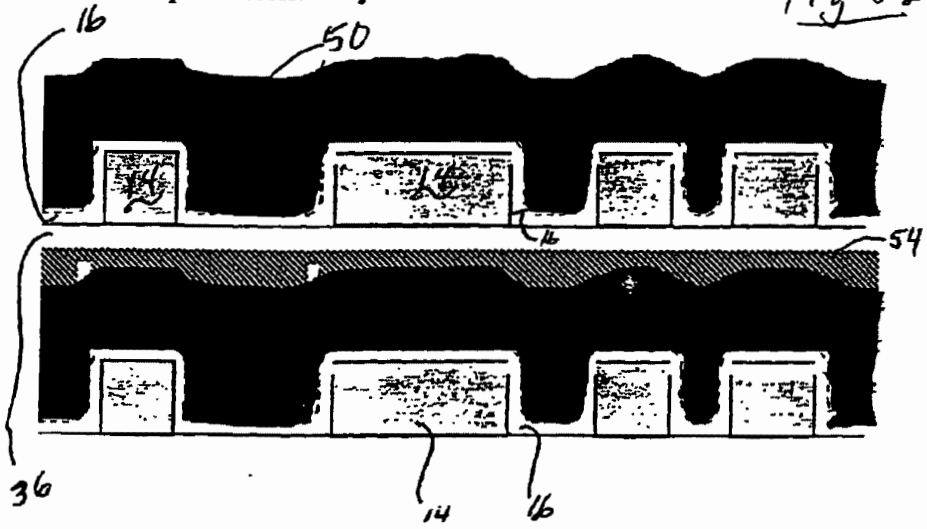


Figure 4:
Shown with the optional planarizing layer and subsequent build up of successive layer.

Fig 22



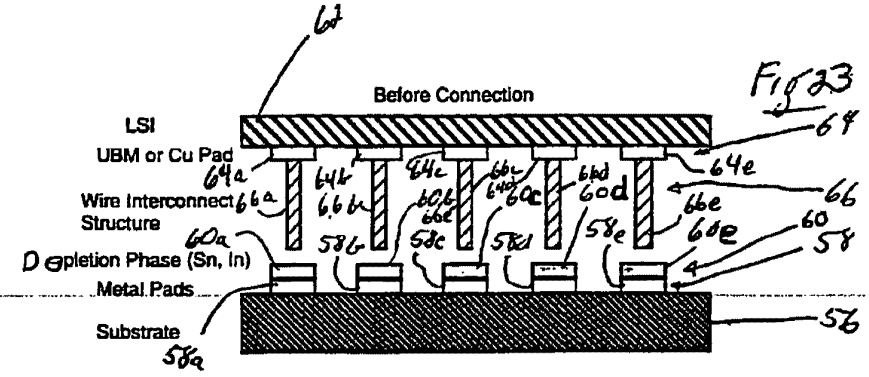


Fig 23

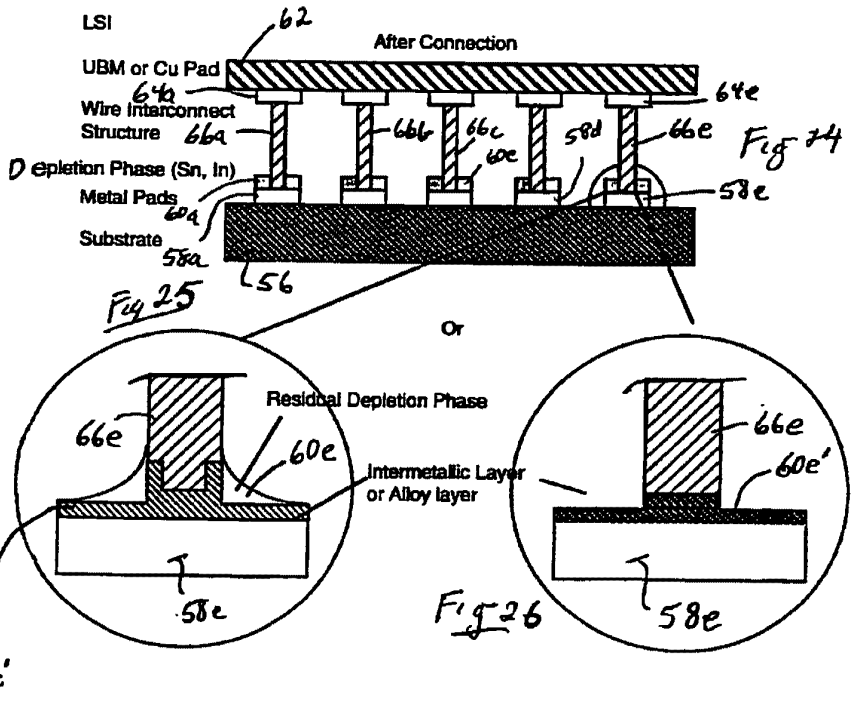


Fig 24

Fig 25

Fig 26

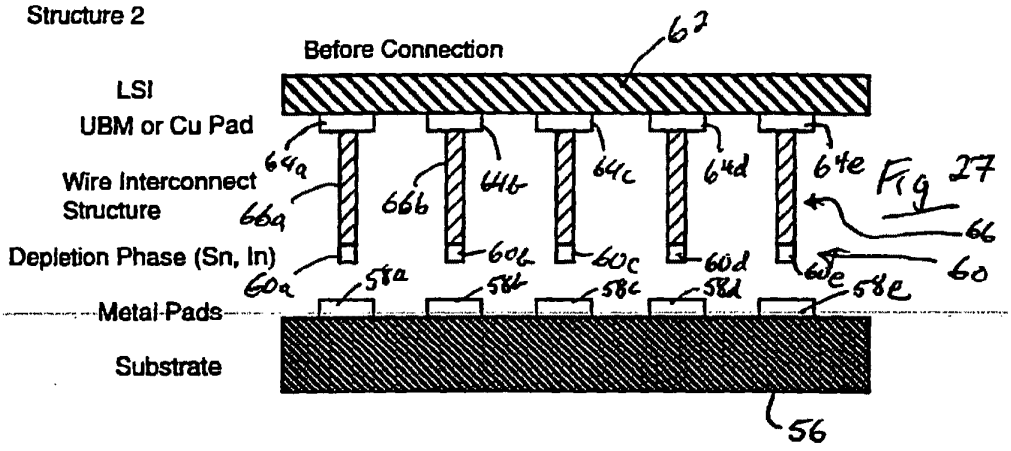


Fig 27

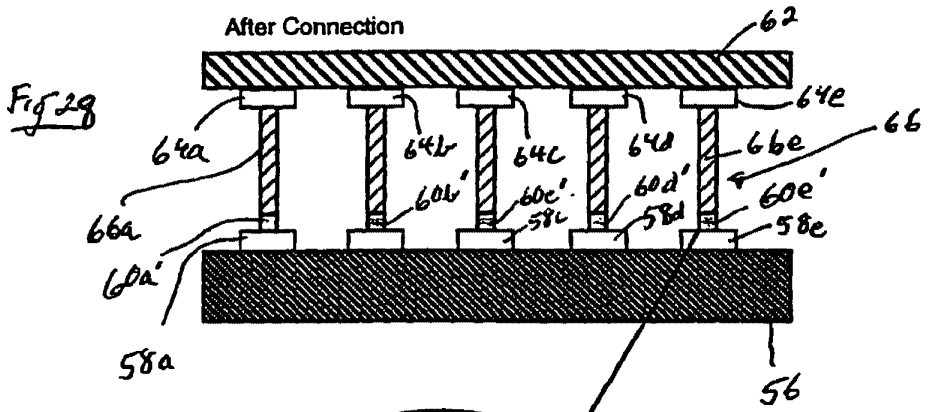


Fig 28

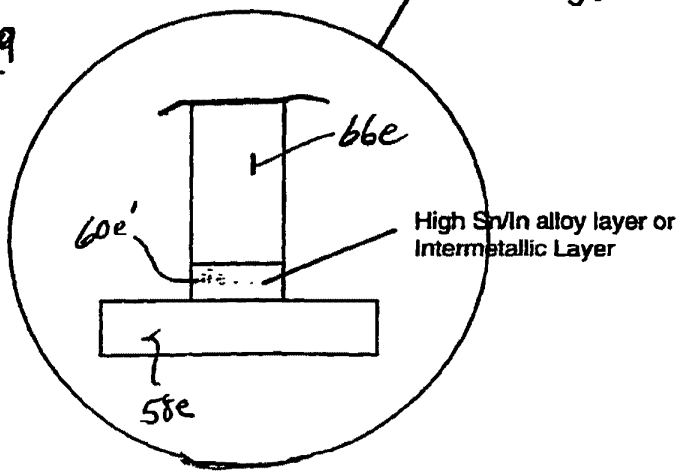


Fig 29

Structure 3

Fig 30

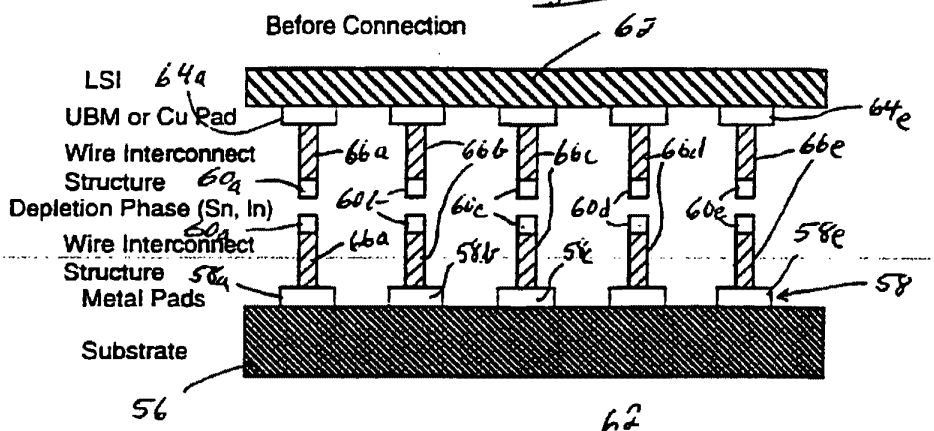


Fig 31

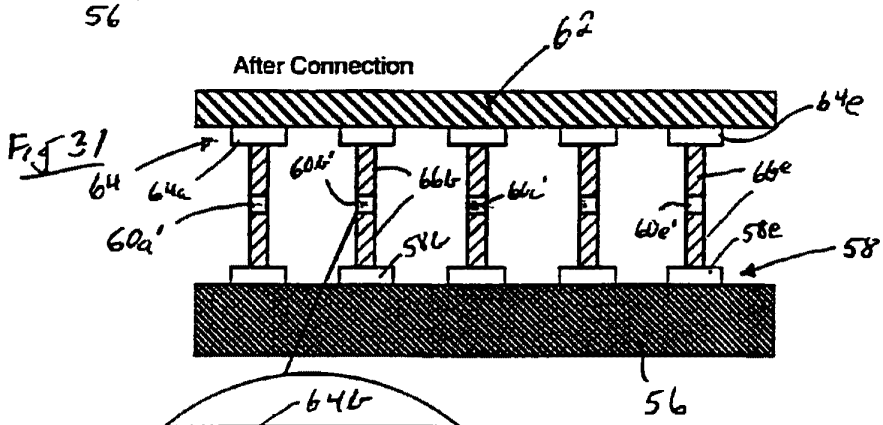
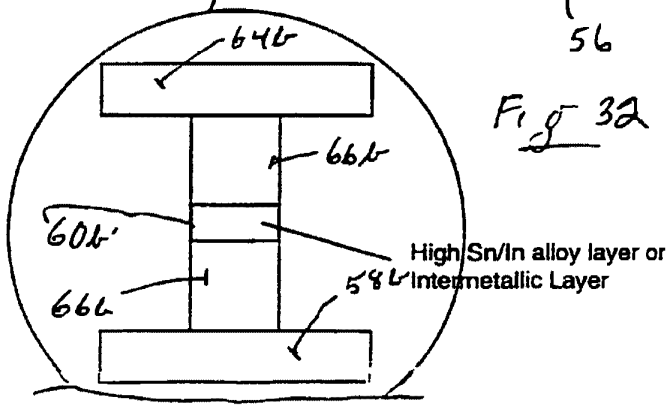
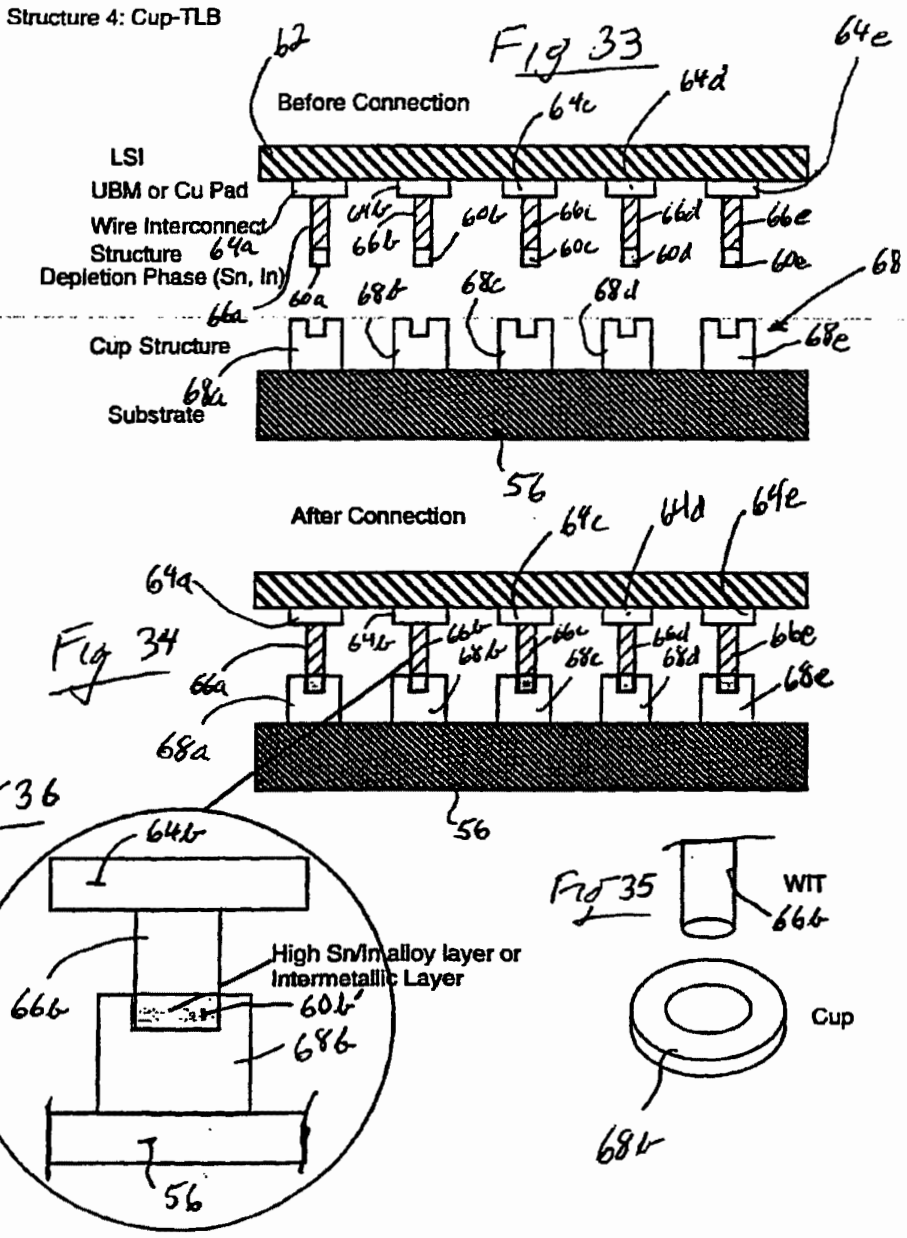


Fig 32




Structure 4: Cup-TLB
Fig 33
Before Connection
LSI
UBM or Cu Pad
Wire Interconnect Structure
Depletion Phase (Sn, In)
Cup Structure
Substrate
After Connection
Fig 34
Fig 36
High Sn/In alloy layer or Intermetallic Layer
Fig 35
WIT
Cup

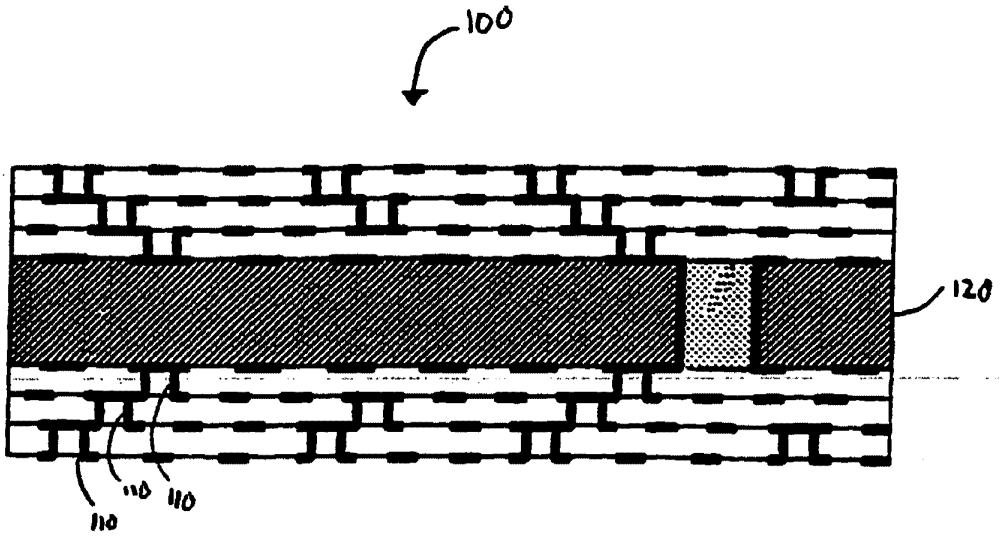


FIG. 37

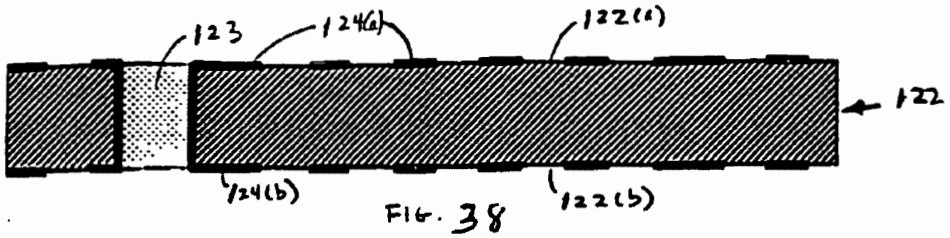


FIG. 38

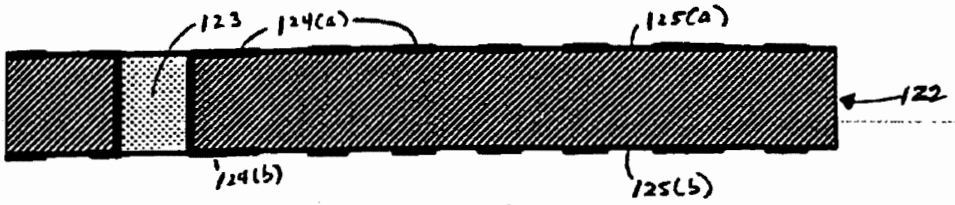


FIG. 39

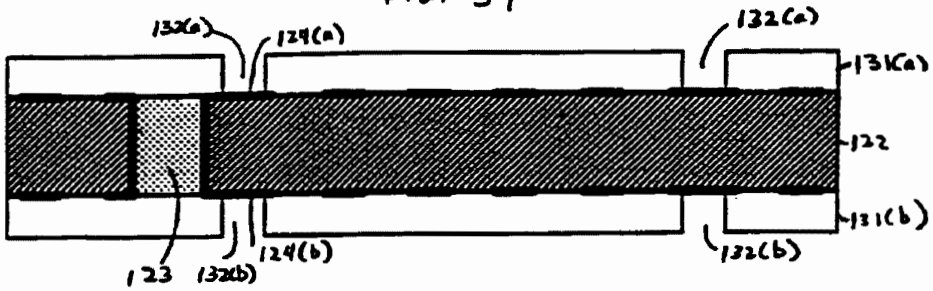


FIG. 40

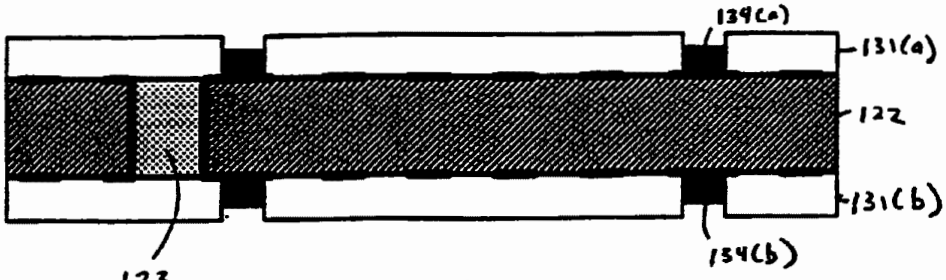


FIG. 41



FIG. 42

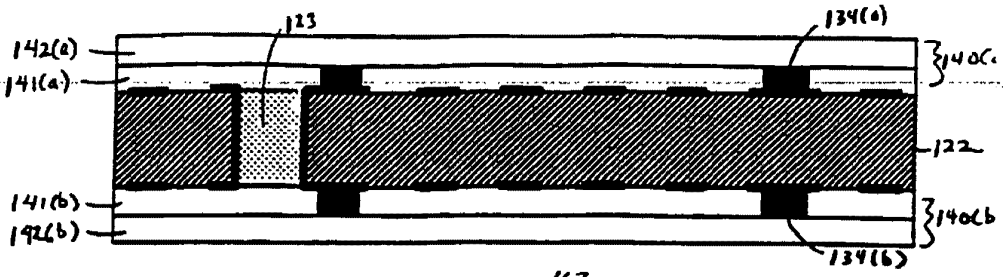


FIG. 43

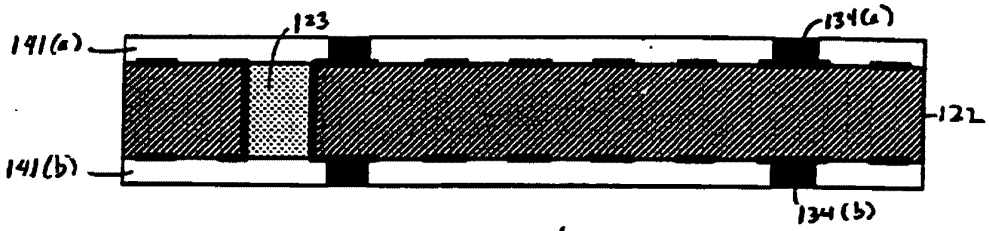


FIG. 44

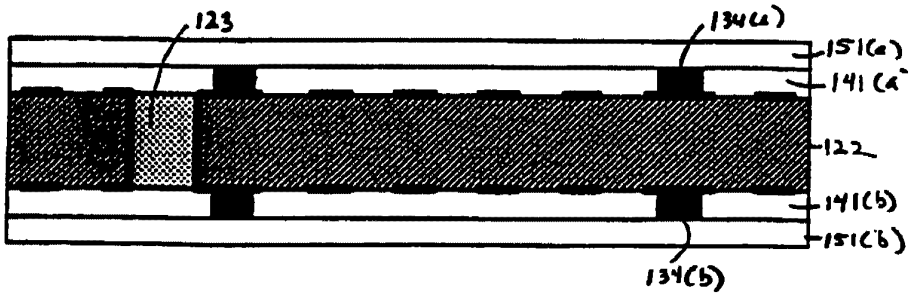


FIG. 45

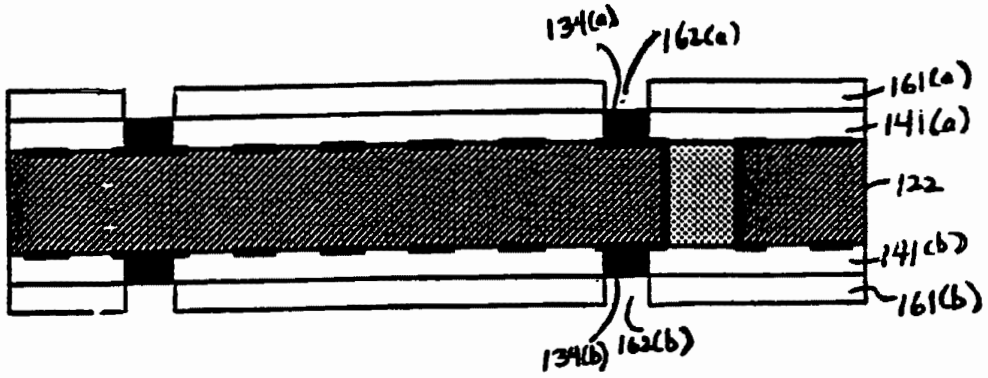


FIG. 46

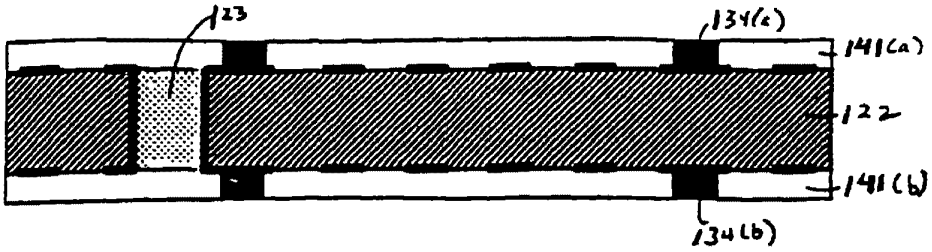


FIG. 47

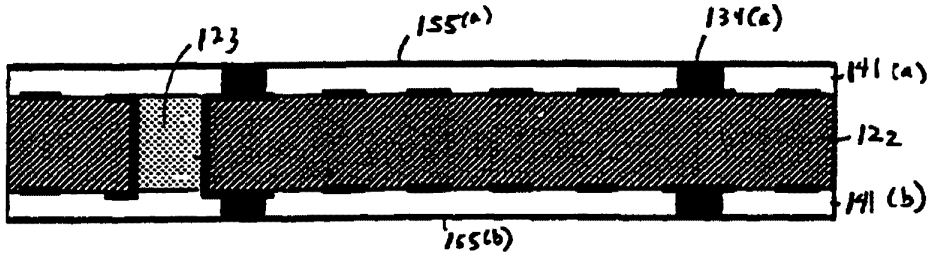


FIG. 48

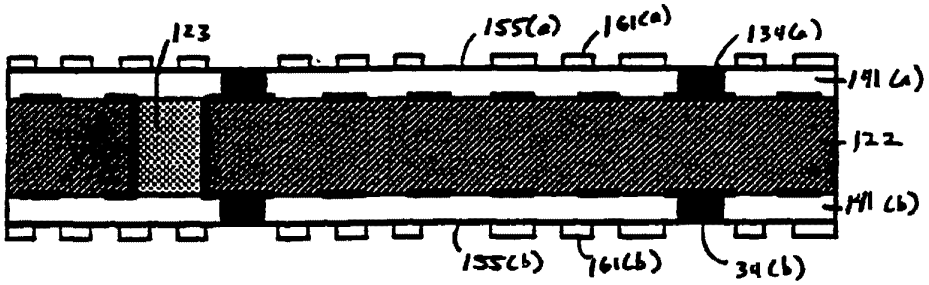


FIG. 49

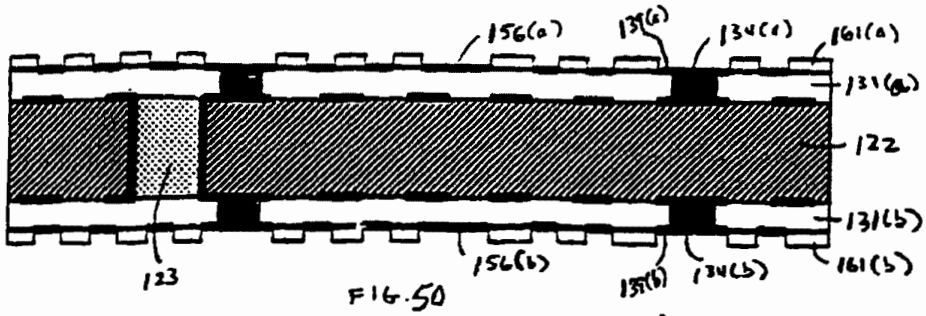


FIG. 50

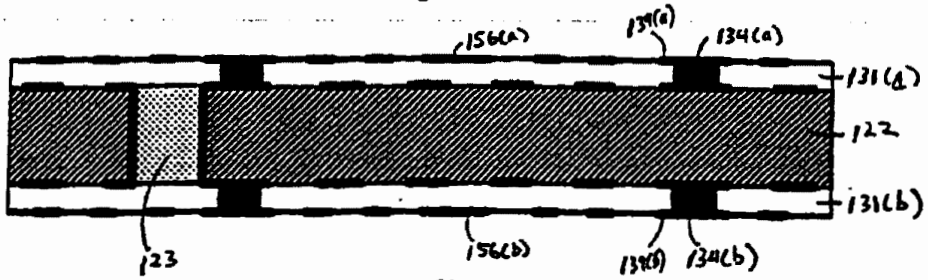


FIG 51

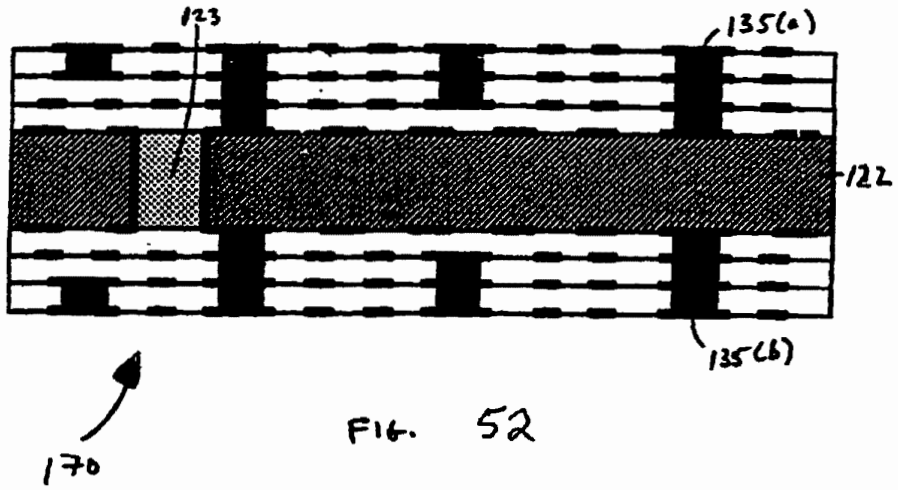


FIG. 52

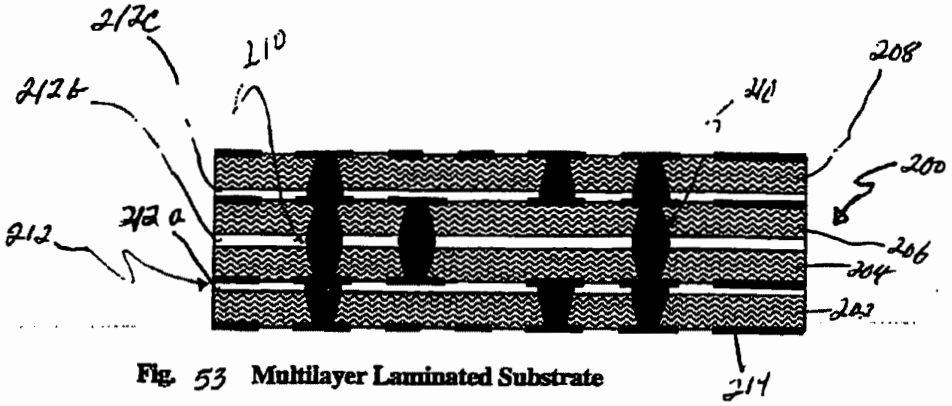


Fig. 53 Multilayer Laminated Substrate

Fabrication Flow – Subtractive



Fig. 54 Start from single side laminate



Fig. 55 Laser blind via

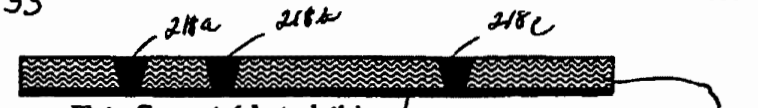


Fig. 56 Plate Cu post (electrolytic)

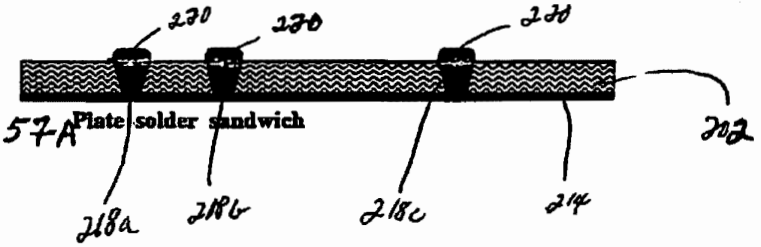
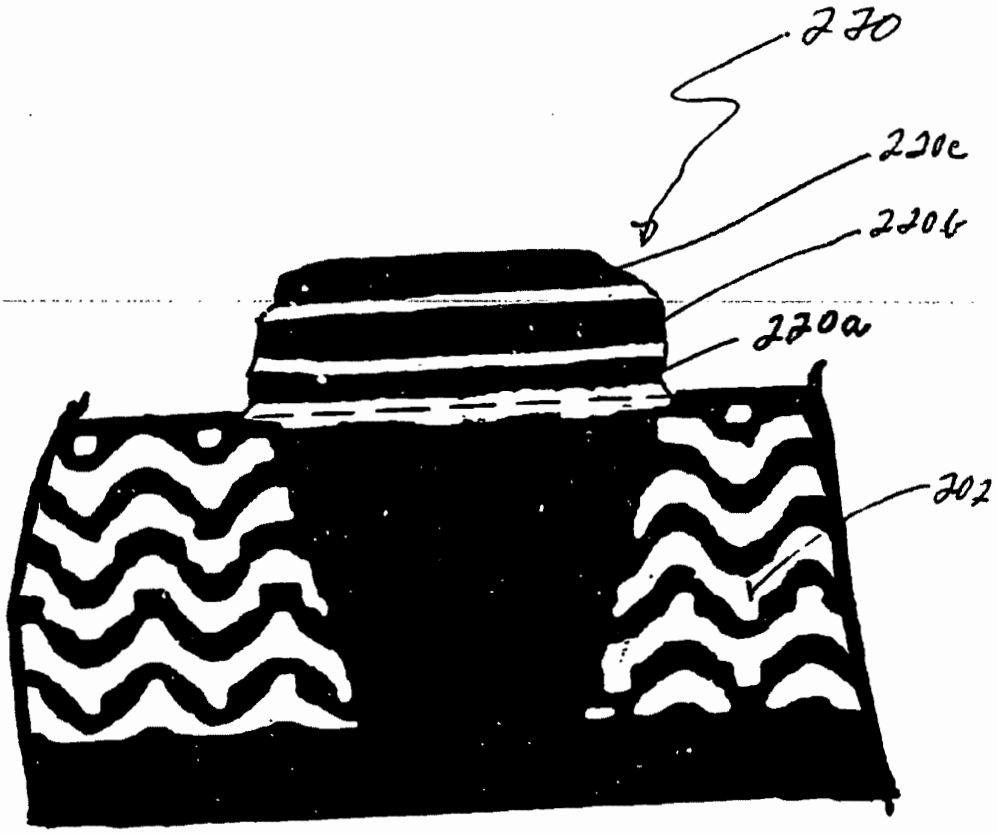
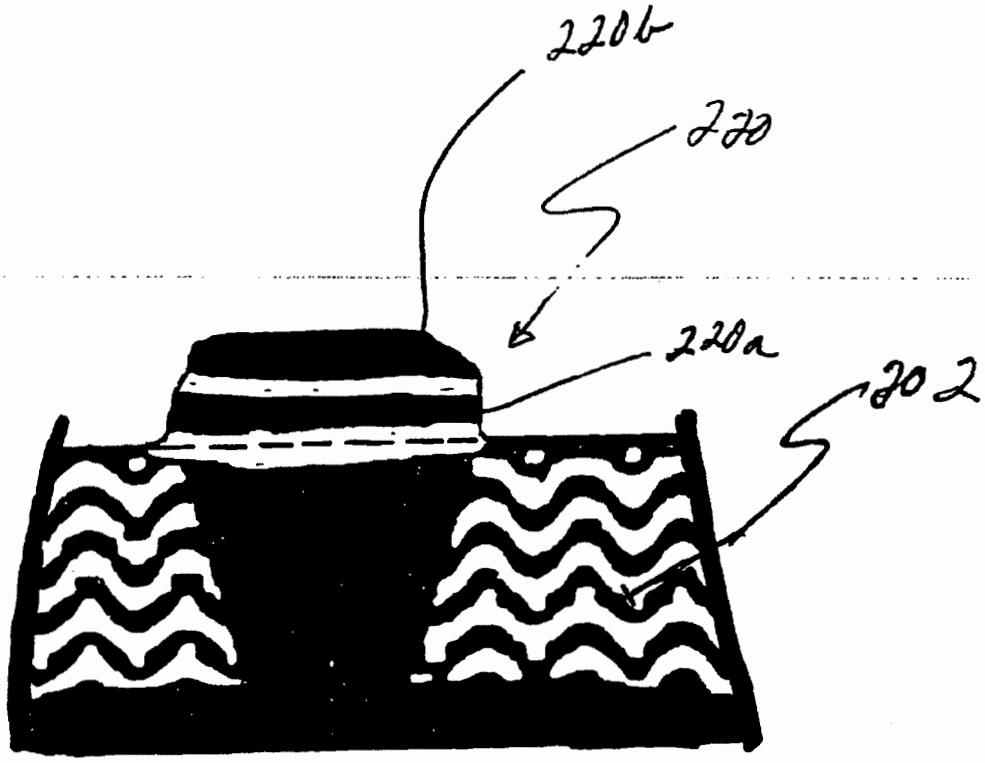


Fig. 57A Plate solder sandwich



57B



57C

Option A:

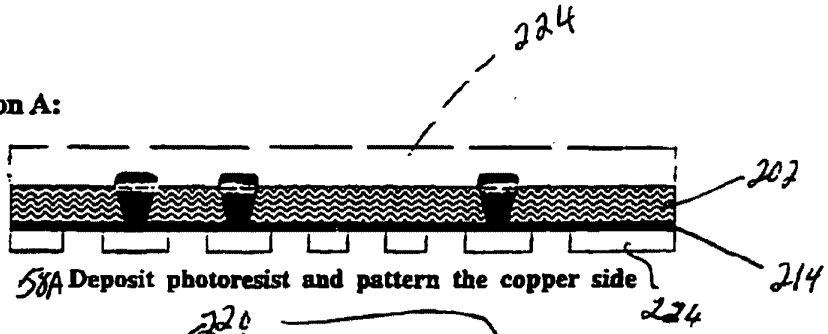


Fig. 58A Deposit photoresist and pattern the copper side

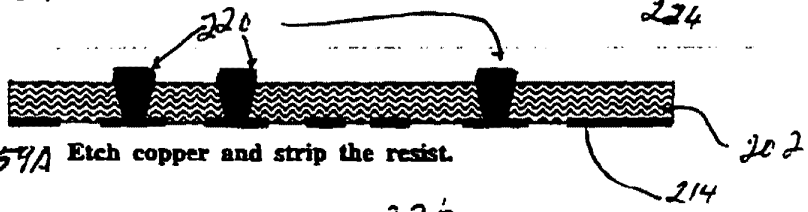


Fig. 59A Etch copper and strip the resist.

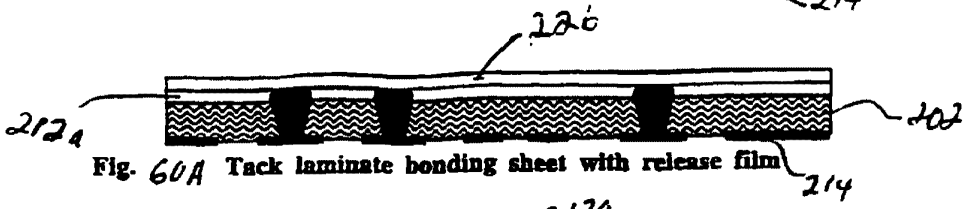


Fig. 60A Tack laminate bonding sheet with release film

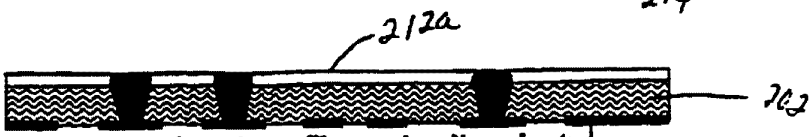


Fig. 61A Remove the release film on bonding sheet

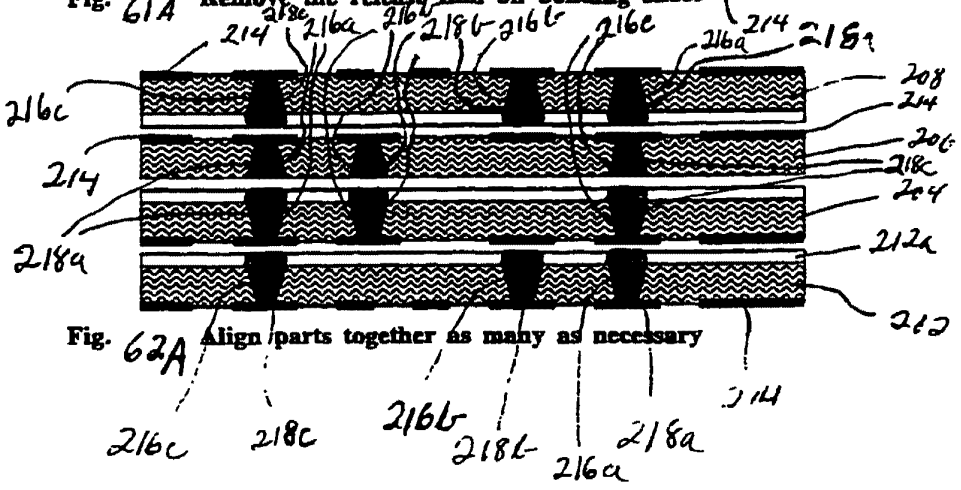


Fig. 62A Align parts together as many as necessary

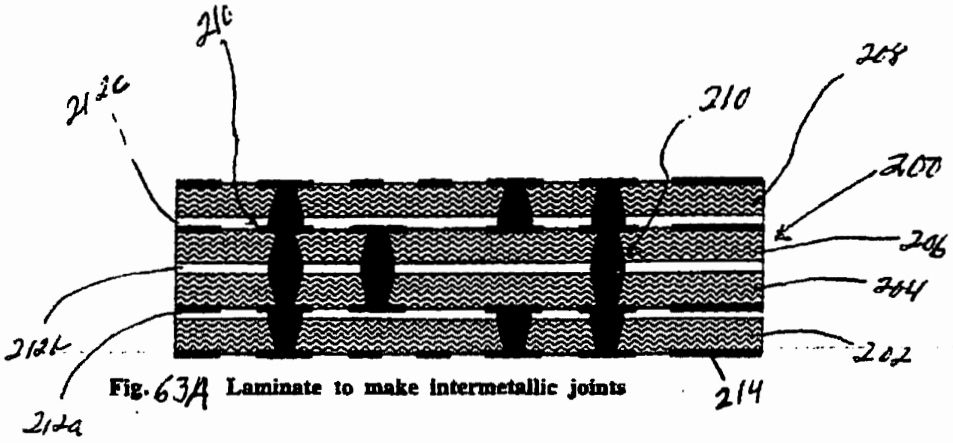


Fig. 63A Laminate to make intermetallic joints

Option B:

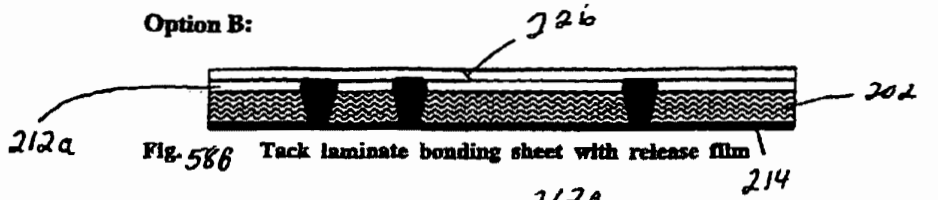


Fig. 58B Tack laminate bonding sheet with release film

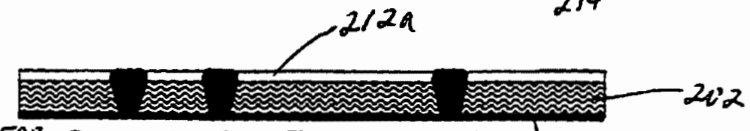


Fig. 59B Remove the release film on bonding sheet

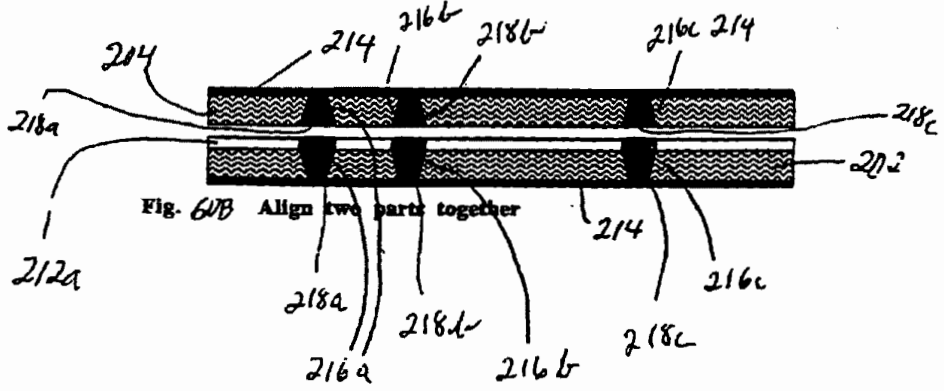


Fig. 60B Align two parts together

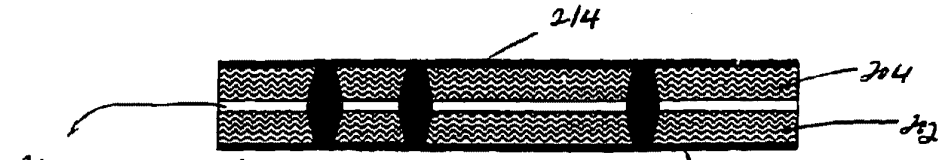


Fig. 61B Laminate to make intermetallic joints

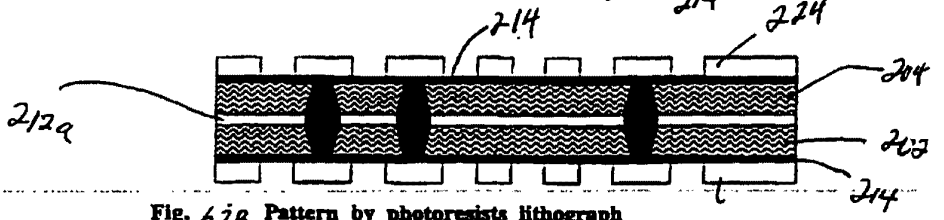


Fig. 62B Pattern by photoresists lithograph

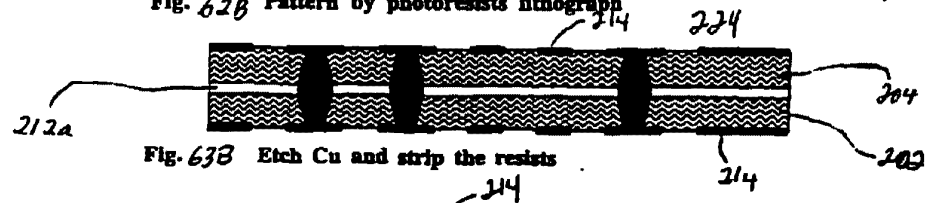


Fig. 63B Etch Cu and strip the resists

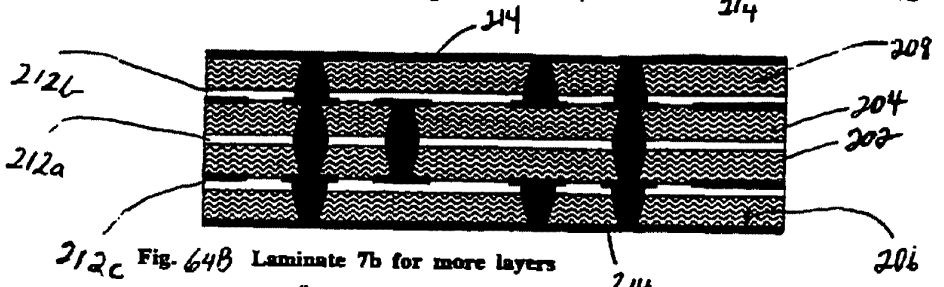


Fig. 64B Laminate 7b for more layers

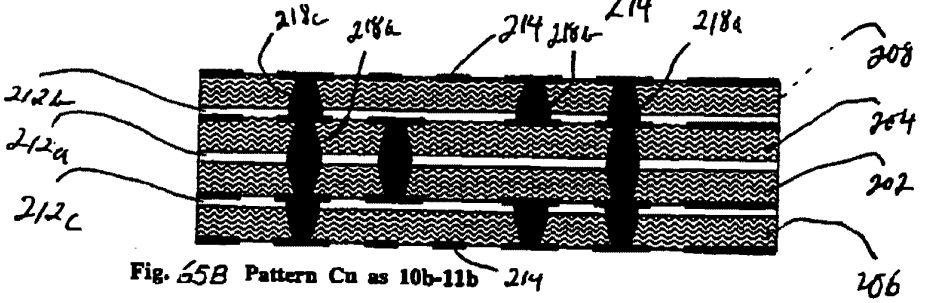


Fig. 65B Pattern Cu as 10b-11b

De-plate pads to capacitors with shorts

Process: Use a de-plating process to remove M2 pads connected to defective capacitors with shorts (or high leakage) to the substrate. M2 is copper. Mask design opens resists over the entire M2 capacitor pads, or only the trace leading to the pad. Breaking the capacitor into many small capacitors, allows the isolation (de-plating) of defects without large reductions in capacitance

Fig 66

- process completed thru Metal 2.	
- spin resist	
- de-plate (MASK 6)	Mask design opens resists over all M2 capacitor pads
- de-plate delective capacitors	Place wafer in plating fixture and put in plating solution. The plating bias is the reverse that used to plate copper, negative voltage to back of wafer and positive voltage to solution. Plating solution can be copper sulfate, sulfuric acid, and additives. Contact to the back of the wafer can be from therontside ; M2 pads to metal 1 to the silicon.
- wet etch	with resist on, follow deplate with short Cu etch to remove residue. The adhesion layer etch, to remove any exposed adhesion layer.
- strip resist	

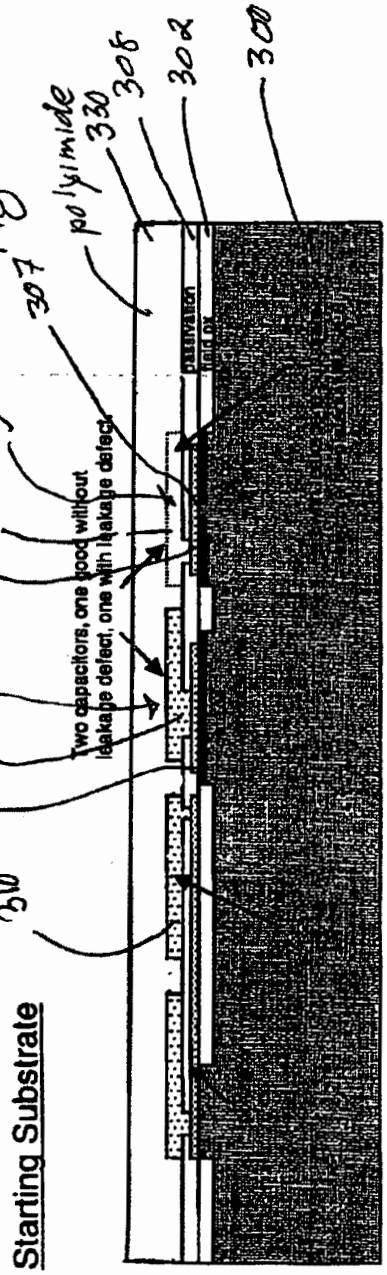


Fig 67

Semiconuctor process:
- nitride deposition
- field oxide (MASK 1)
- nitride etch, field oxidation(1um), nitride stripe, gate oxidation(10nm)
- contact mask (MASK 2)
- oxide etch, polysilicon deposit, metal deposit
- metal 1 mask (MASK 3)
- aluminum etch, polysicon etch, passivation deposition
- pad mask (MASK 4)
- passivation etch, TiCu deposition
- metal 2 mask (MASK 5)
- M2 pattern
- de-plate (MASK 6)
- de-plate defective capacitors
- polyimide coat

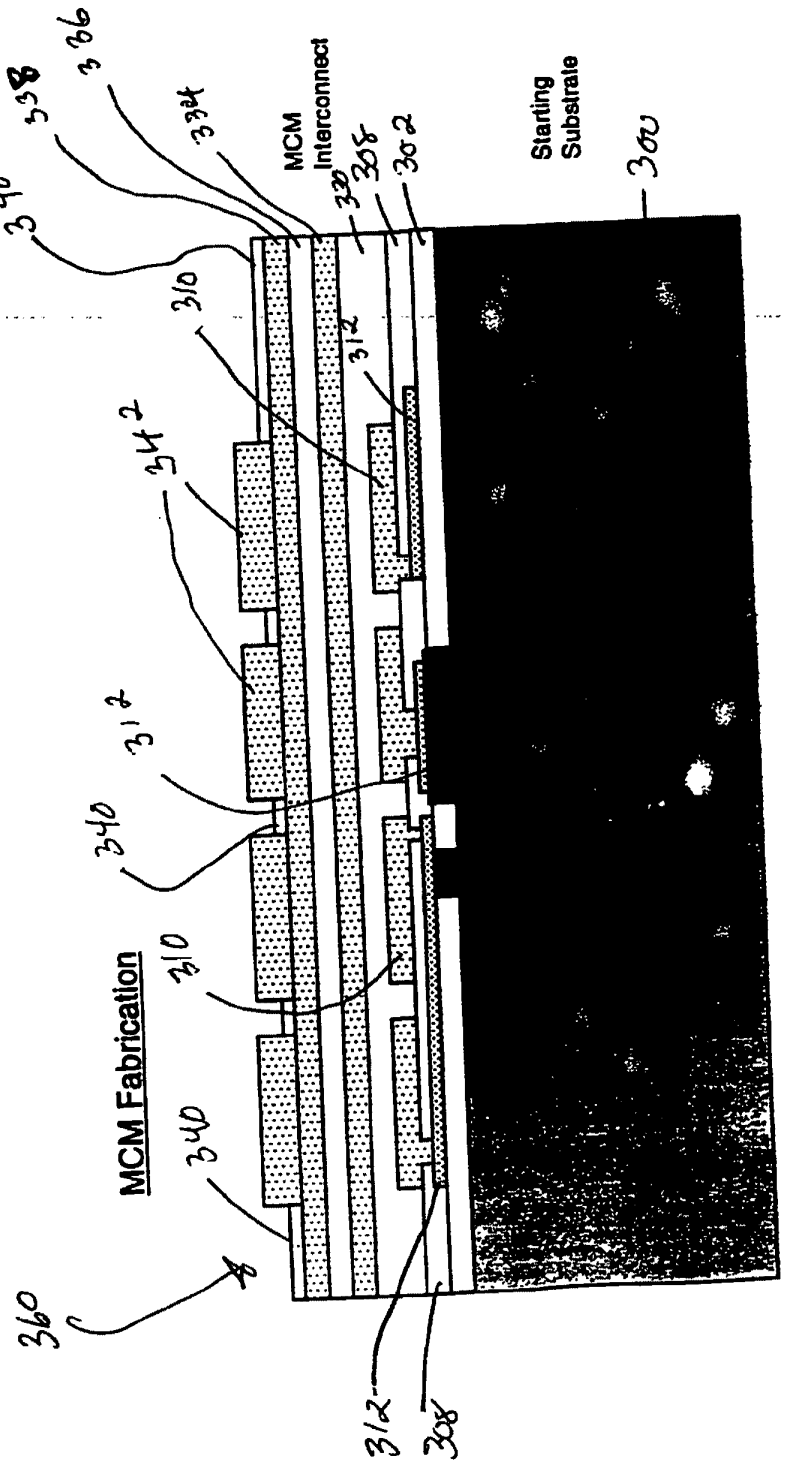

MCM Fabrication
MCM Interconnect
Starting Substrate
360
340
310
312
342
338
336
334
330
308
302
300

Fig 6E

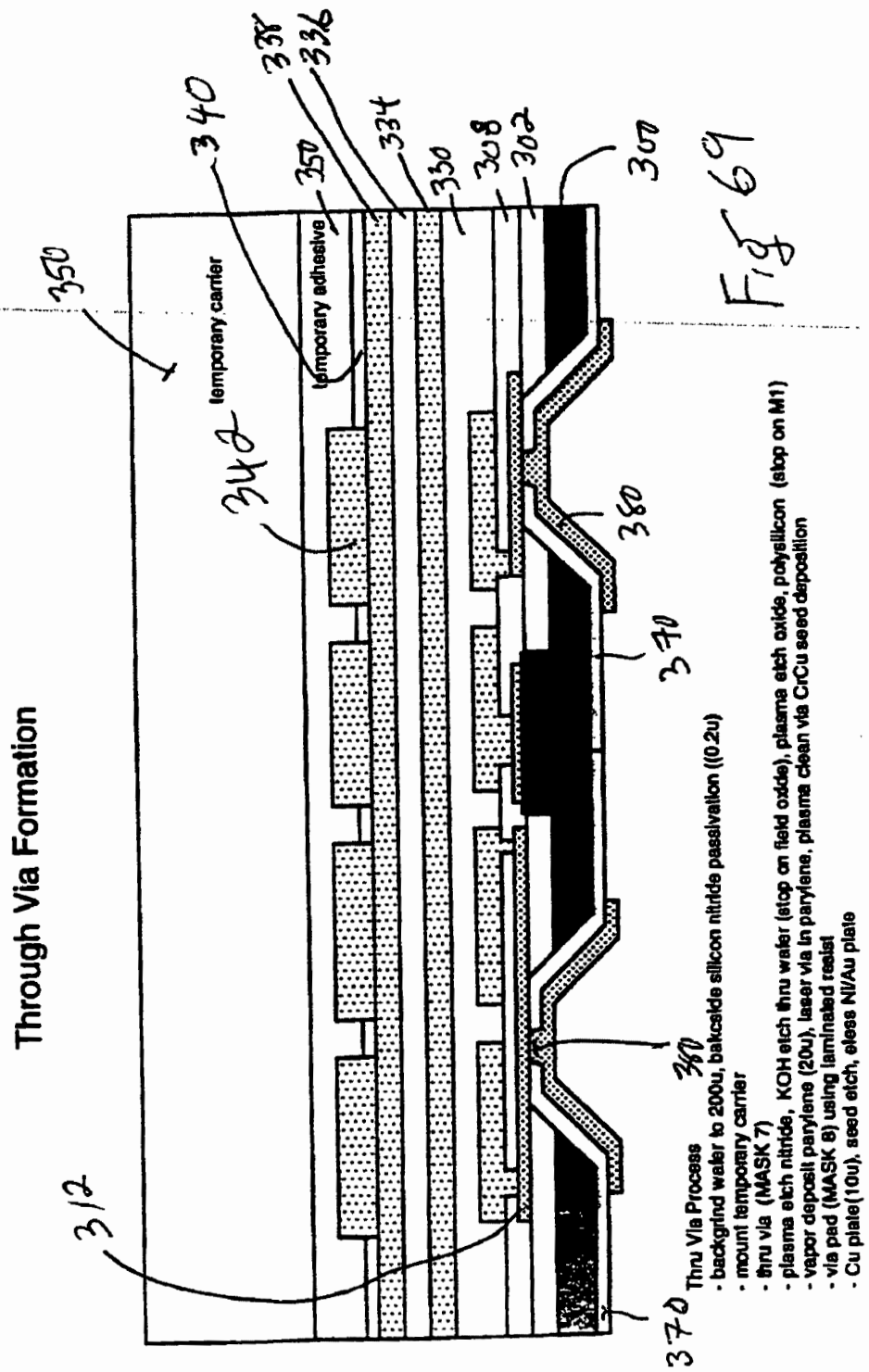

Through Via Formation
temporary carrier
temporary adhesive
350
340
342
338
336
334
330
308
302
307
380
370
360
312
370
Thru Via Process
- backgrind wafer to 200u, backside silicon nitride passivation ((0.2u)
- mount temporary carrier
- thru via (MASK 7)
- plasma etch nitride, KOH etch thru wafer (stop on field oxide), plasma etch oxide, polysilicon (stop on M1)
- vapor deposit parylene (20u), laser via in parylene, plasma clean via CrCu seed deposition
- via pad (MASK 8) using laminated resist
- Cu plate(10u), seed etch, eless Ni/Au plate

Fig 6C

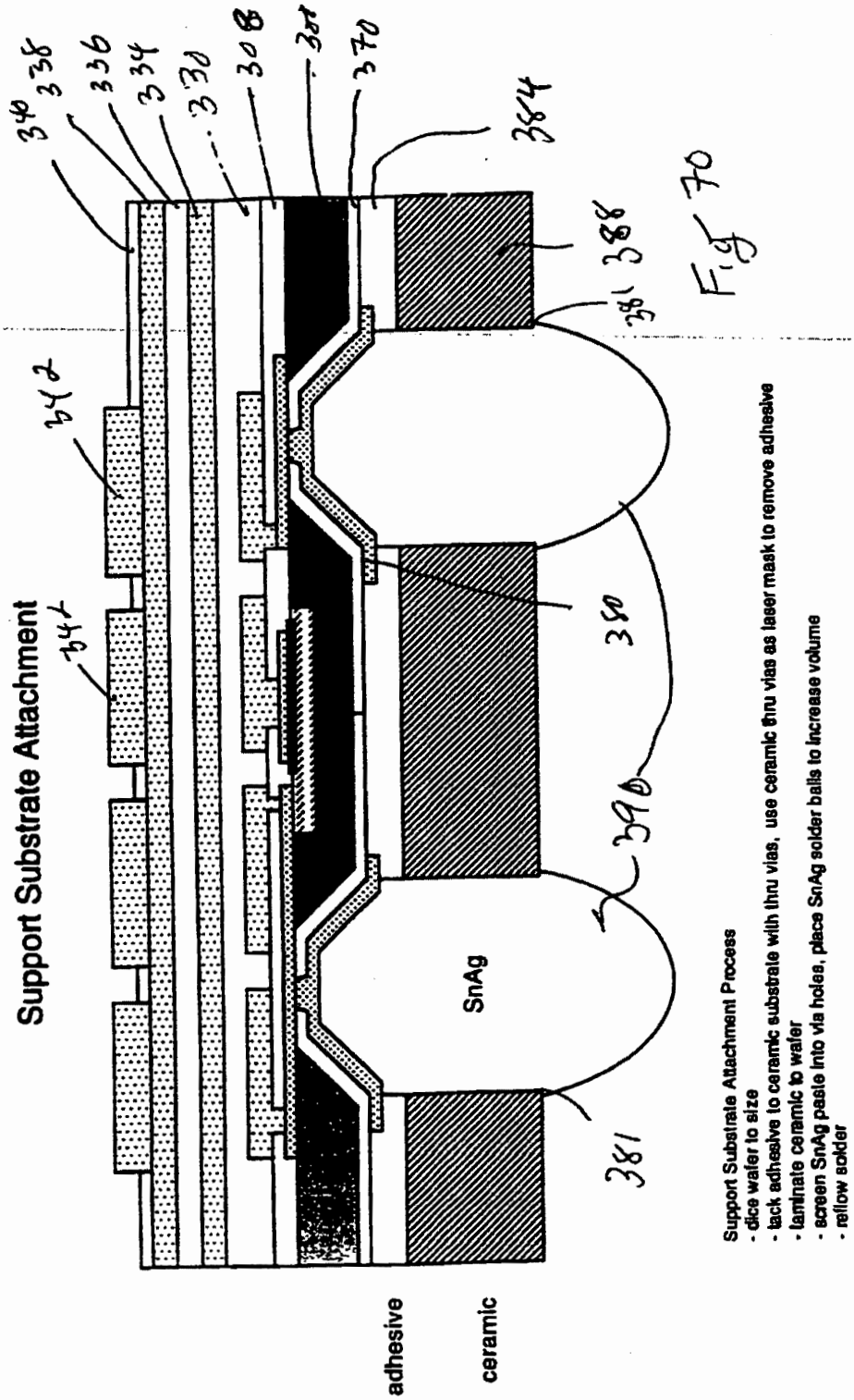

340
338
336
334
330
308
302
370
384
388
381
342
347
350
390
381
Support Substrate Attachment
SnAg
adhesive
ceramic
Support Substrate Attachment Process
- dice wafer to size
- tack adhesive to ceramic substrate with thru vias, use ceramic thru vias as laser mask to remove adhesive
- laminate ceramic to wafer
- screen SnAg paste into via holes, place SnAg solder balls to increase volume
- reflow solder

Fig 70

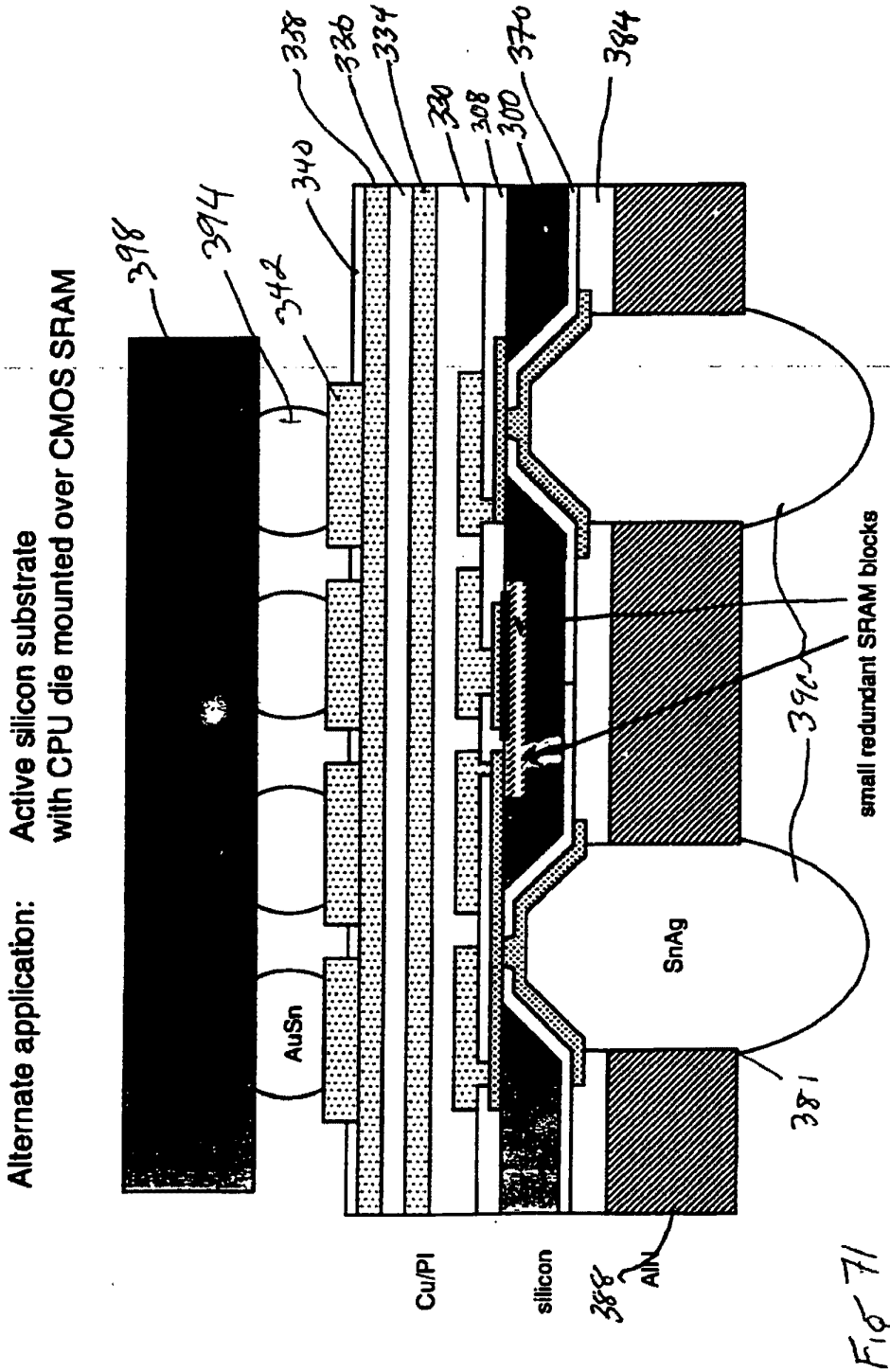

Alternate application:
Active silicon substrate
with CPU die mounted over CMOS SRAM
398
394
342
340
338
336
334
330
308
300
370
384
AuSn
SnAg
small redundant SRAM blocks
391
381
Cu/PI
silicon
388
AlN

Fig 71

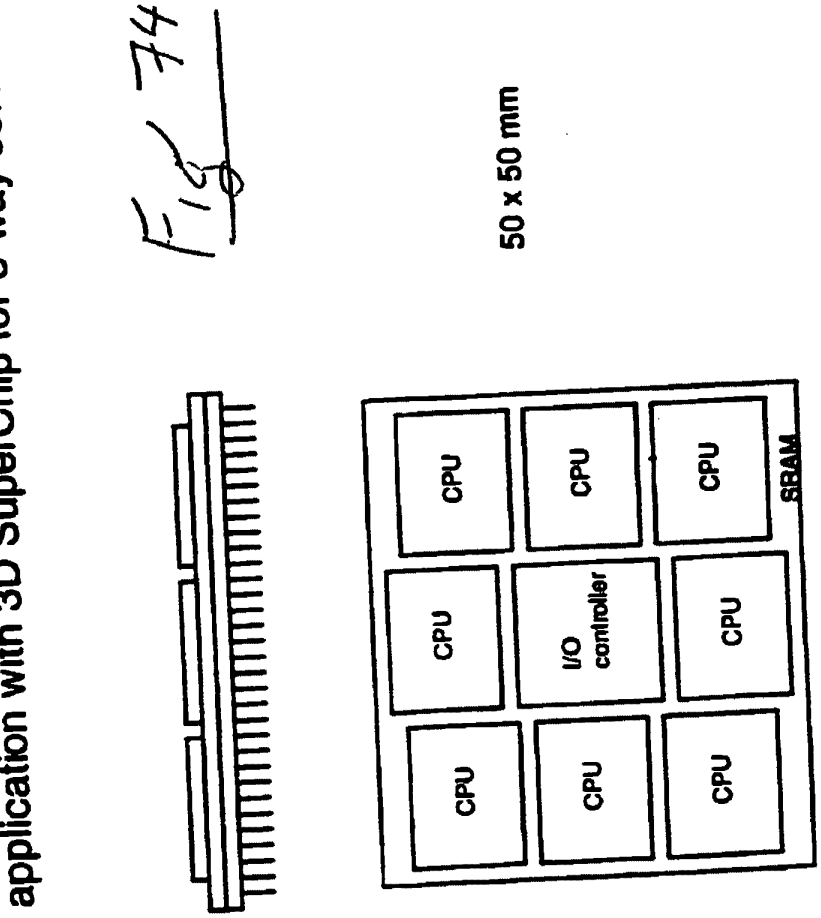
Alternate application with 3D SuperChip for high performance MCM

Fig 72

Fig 73

Fig 75

Fig 74


Alternate application with 3D SuperChip for 8-way server
50 x 50 mm
CPU
CPU
CPU
CPU
I/O controller
CPU
CPU
CPU
CPU
SRAM

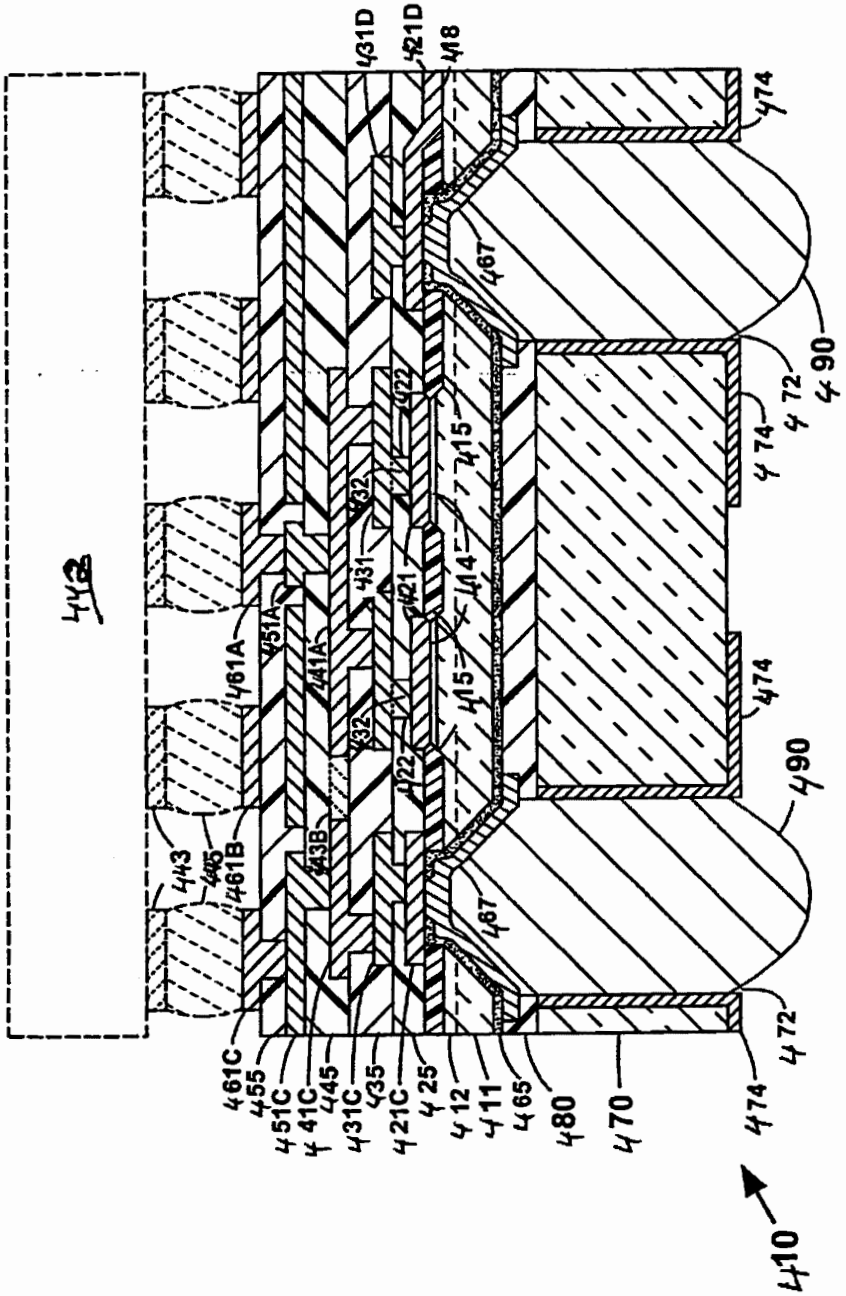

431D
421D
418
474
467
490
472
474
415
422
432
414
431
421
451A
441A
461A
415
474
490
432
422
443
445
461B
443B
467
472
461C
455
451C
441C
445
431C
435
421C
425
412
411
465
480
470
474
410

FIG. 76

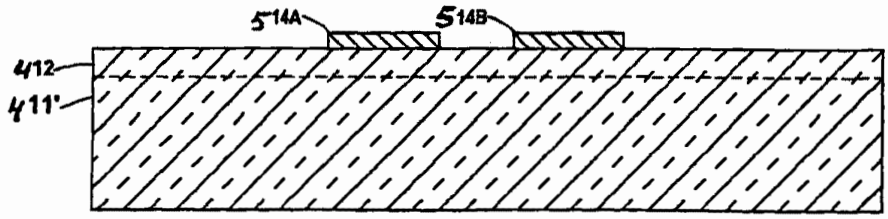


FIG. 77

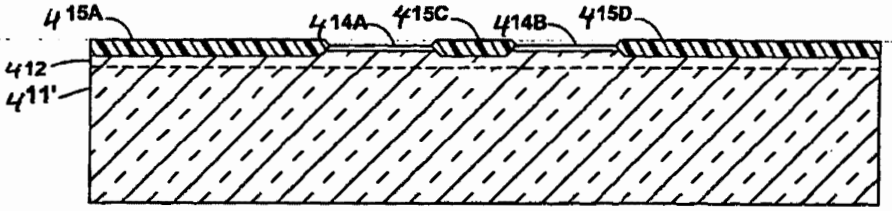


FIG. 78

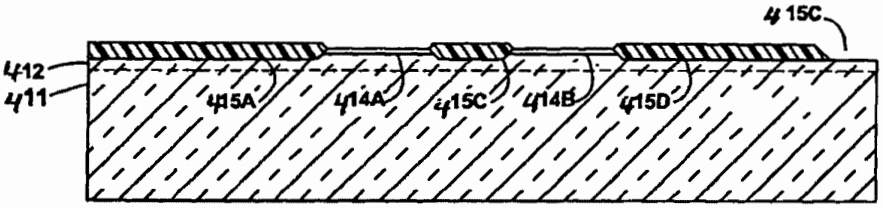


FIG. 79

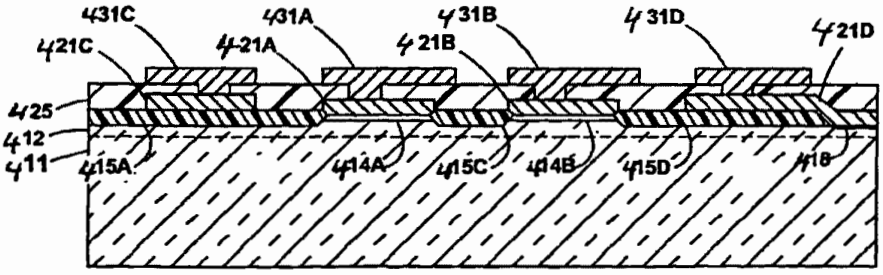


FIG. 80

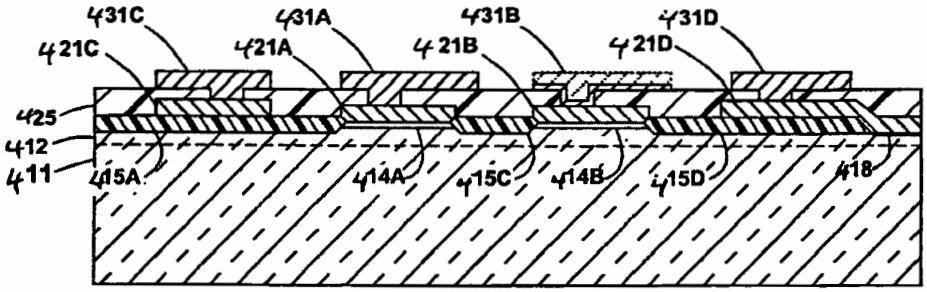


FIG. 81

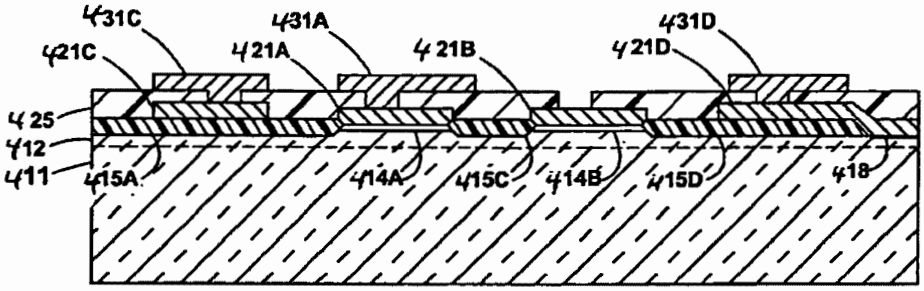


FIG. 82

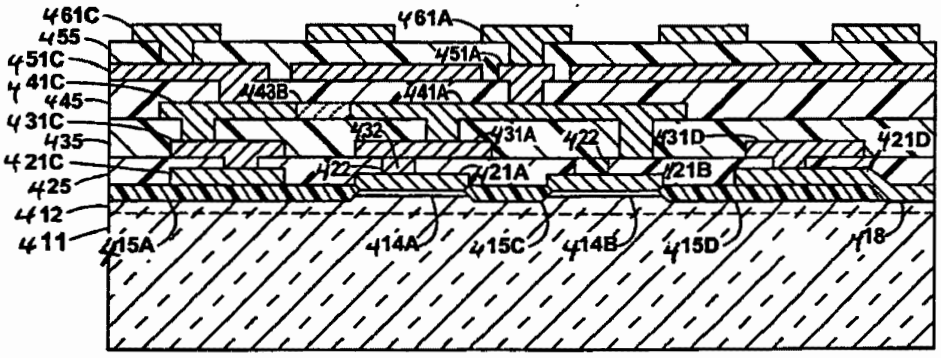


FIG. 83

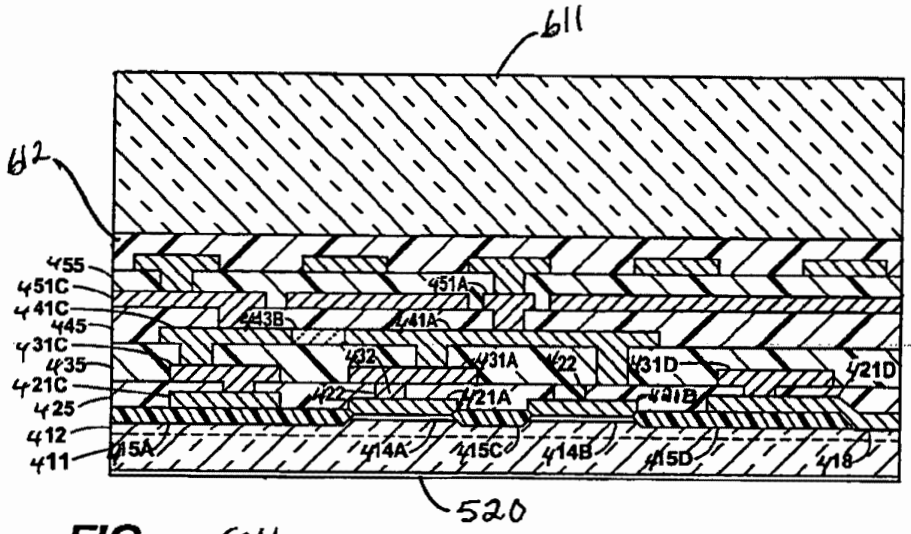

611
612
455
451C
441C
445
431C
435
421C
425
412
411
415A
451A
443B
441A
432
431A
422
431D
421D
421A
421B
414A
415C
414B
415D
418
520

FIG. 84

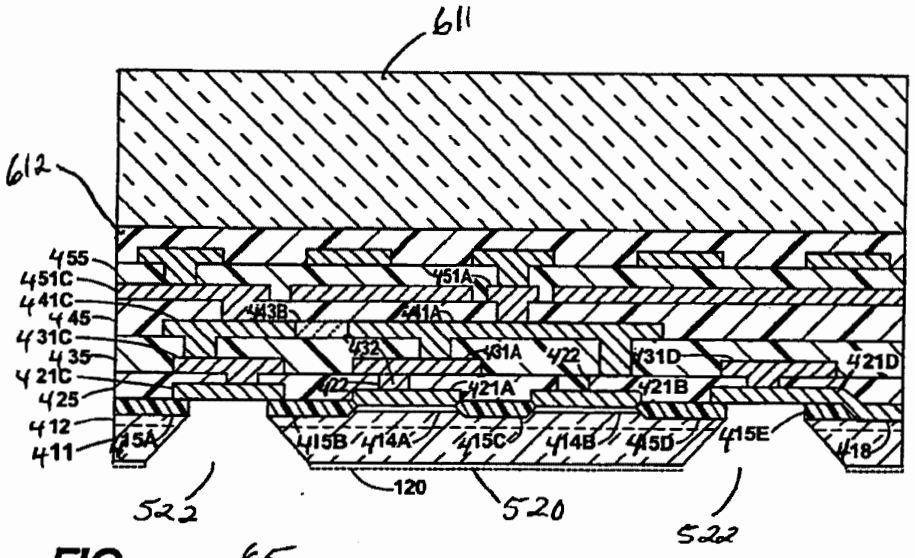

611
612
455
451C
441C
445
431C
435
421C
425
412
411
415A
451A
443B
441A
432
431A
422
431D
421D
421A
421B
415B
414A
415C
414B
415D
415E
418
120
522
520
522

FIG. 85

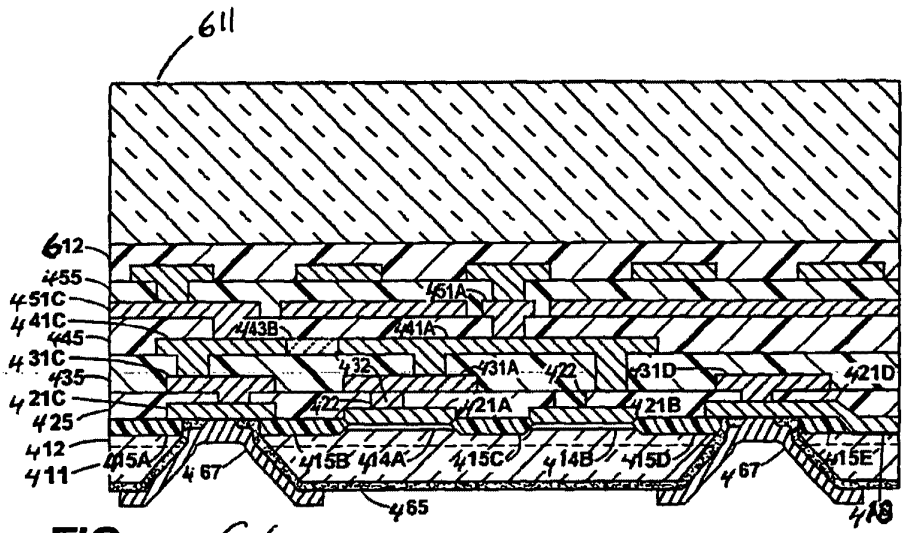

611
612
455
451C
441C
445
431C
435
421C
425
412
411
415A
467
415B
414A
415C
414B
415D
467
415E
465
451A
443B
441A
432
431A
422
431D
421D
422
421A
421B

FIG. 86

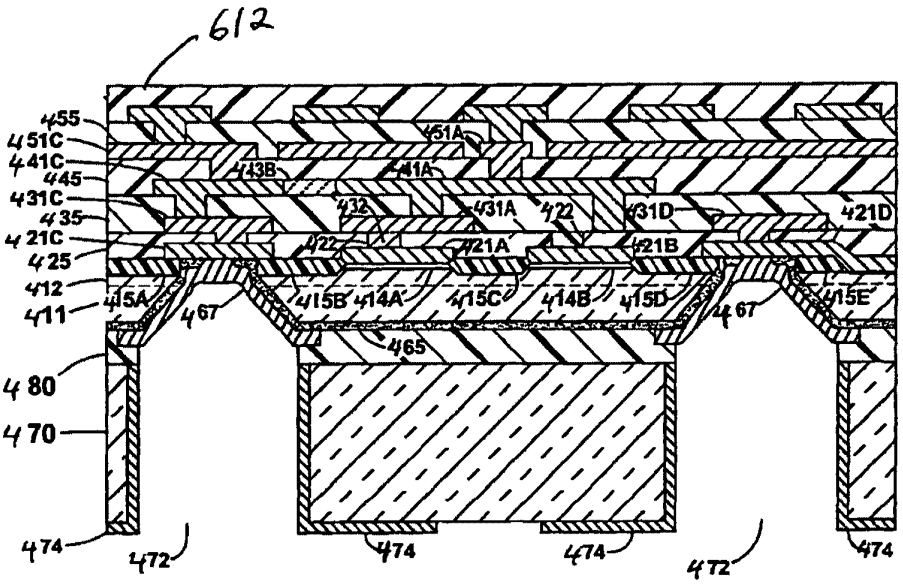

612
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414B
415D
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415E
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480
470
474
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474
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472
474
451A
443B
441A
432
431A
422
431D
421D
422
421A
421B

FIG. 87

MULTI-CHIP MODULE AND METHOD FOR FORMING AND METHOD FOR DEPLATING DEFECTIVE CAPACITORS

[0001] This is a continuation-in-part patent application of patent applications having Ser. No. 09/429,854, filed Oct. 28, 1999, and Ser. No. 09/956,605, filed Sep. 18, 2001. Benefit of the earlier filing dates is claimed for all common subject matter.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention is related to multichip modules (MCMs). More specifically, the present invention provides MCM substrates, as well as to a method for making multichip module substrates and to a method for deplating defective capacitors.

[0004] 2. Description of the Prior Art

[0005] Multilayer circuit structures can be used to electrically communicate two or more electrical devices such as two or more computer chips. Multilayer circuit structures typically contain multiple conductive layers separated by one or more dielectric layers. Via structures disposed in apertures in the dielectric layers provide conductive paths so that electrical signals can pass from one conductive layer to another conductive layer. Multiple via structures in successive dielectric layers can be used to form a conductive path from an inner region to an outer region of a multilayer circuit structure.

[0006] Multichip module (MCM) packages require off-module connections to receive input signal, to provide output signals, and to receive power and ground voltages. In low-cost, low performance MCM modules, these off-module connections are usually around the periphery edges of the MCM's substrate. In higher-cost, higher performance MCM modules, the off-module connections are formed through the MCM's substrate which usually comprises a multilayer ceramic material.

[0007] Discrete surface-mount or chip capacitors are often added to the surface of a MCM substrate to remove (e.g., de-couple) noise between the power lines and the ground lines. However, as the operating frequency of MCMs has increased, the effectiveness of these surface mount and chip capacitors has decreased to marginal and unacceptable levels.

[0008] The via structures in successive dielectric layers can be staggered in a multilayer circuit structure. For example, as shown in **FIG. 37**, a plurality of staggered via structures **110** are in electrical communication with each other. The staggered conductive path formed by the via structures **110** can provide communication between a core structure **120** and an outer surface of the multilayer circuit structure **100**. Each of the via structures **110** shown in **FIG. 37** is in the form of a conductive coating on an aperture wall in a dielectric layer. Unfortunately, staggering the via structures can consume valuable area in a multilayer circuit structure and can increase the signal run length. This can decrease the density of the circuitry in a multilayer circuit structure. Moreover, the metal coating of via structures of the type shown in **FIG. 37** is thin. Open circuits can form if the coating is not thick enough or is not uniform.

[0009] A patentability investigation was conducted and the following U.S. Patents were discovered: U.S. Pat. No. 3,867,272 to Rust et al.; U.S. Pat. No. 4,729,970 to Nath et al.; U.S. Pat. No. 4,749,454 to Arya et al.; U.S. Pat. No. 4,782,028 to Farrier et al.; U.S. Pat. No. 4,984,358 to Nelson; U.S. Pat. No. 5,202,018 to Horántl et al.; U.S. Pat. No. 5,543,585 to Booth et al.; U.S. Pat. No. 5,591,678 to Bendik et al.; U.S. Pat. No. 5,656,548 to Zavracky et al.; U.S. Pat. No. 5,656,552 to Hudak et al.; U.S. Pat. No. 5,716,881 to Liang et al.; U.S. Pat. No. 5,770,487 to Maas et al.; U.S. Pat. No. 5,784,261 to Pedder; U.S. Pat. No. 5,807,783 to Gaul et al.; U.S. Pat. No. 5,811,879 to Akram; U.S. Pat. No. 5,838,545 to Clocher et al.; U.S. Pat. No. 5,843,806 to Tsai; U.S. Pat. No. 5,851,845 to Wood et al.; U.S. Pat. No. 5,856,937 to Chu et al.; U.S. Pat. No. 5,859,397 to Ichinose et al.; U.S. Pat. No. 5,863,412 to Ichinose et al.; U.S. Pat. No. 5,863,829 to Nakayoshi et al.; U.S. Pat. No. 5,866,441 to Pace; U.S. Pat. No. 5,872,025 to Cronin et al.; U.S. Pat. No. 5,872,700 to Collander; and U.S. Pat. No. 5,877,034 to Ramm et al.

[0010] U.S. Pat. No. 3,867,272 discloses microelectric devices and circuits, such as those found in semiconductor and hybrid microelectrics. Microelectric devices are rendered unrecognizable and may be destroyed by means of an electrochemical reaction comprising an electro-chemical or chemical etching and/or de-plating process.

[0011] U.S. Pat. No. 4,729,970 discloses an electronic device of the type including a thin film body having a superposed electrode and further including short circuit defects therein passivated by conversion process in which the electrical resistivity of the electrode material is increased proximate the defect regions. Conversion is accomplished by exposing the electrode material to a conversion reagent and activating the reagent proximate the defect regions. The process may be utilized for a variety of differently configured devices, and may be readily adapted for use in a roll-to-roll device fabrication process.

[0012] U.S. Pat. No. 4,749,454 discloses a method of removing electrical shorts and shunts from a thin-film semiconductor device having pairs of electrodes with exposed contact surfaces wherein each pair of electrodes is separated by a semiconductor film. The disclosed method comprises the steps of coating the exposed contact surfaces with an ionic solution and successively applying a reverse-bias voltage between the exposed contact surfaces of each pair of electrodes. The ionic solution has an etching rate that increases with increased temperature so that the leakage current flowing through shorts and shunts located between each respective pair of electrodes in response to the reverse-bias voltage will create a local temperature increase at the shorts and shunts and selectively etch or oxidize the shorts and shunts, rendering them substantially nonconductive. The exposed contact surfaces can be coated using a sponge application or spray apparatus. The preferred ionic solution comprises an acid mixture diluted to one part in at least five parts water.

[0013] U.S. Pat. No. 4,782,028 discloses a method for forming a detector device, such as thinned bulk silicon blocked impurity transducer infrared detector, by thinning a semiconductor substrate and processing the thinned region on two sides to form the detector device. The semiconductor substrate is thinned to form a cavity in the substrate. Further

processing on both sides of the thinned region is performed while the thinned region is still connected to the thicker substrate. The thinned region is then separated from the substrate upon completion of the given processing steps. The device may then be mounted to a readout device.

[0014] U.S. Pat. No. 4,984,358 discloses integrated circuit dies which, while still in wafer form, are prepared for stacking without requiring packaging. Holes are made through a wafer having a plurality of integrated circuit dies and are placed between the dies and adjacent the die pads. A layer of insulating material is placed on the wafer and in the outer periphery of the holes. An electrically conductive connection is made between the top of each pad and the inside of the insulating material in an adjacent hole. The insulating layer and the electrically conductive layer can be further extended to the backside of the dies if desired. The dies are separated from each other and can be assembled in a stack and/or surface mounted to a substrate.

[0015] U.S. Pat. No. 5,202,018 discloses the invention relating to the electrochemical dissolution of semiconductors by alternating applications of anodic and cathodic direct currents to an electrode formed by contacting a semiconductor material with an electrolyte.

[0016] U.S. Pat. No. 5,543,585 discloses a simple process for card assembly by direct chip attachment using electrically conductive adhesives. Methods are disclosed which create the same intermediate wafer product with a layer of insulative thermoplastic and conductive thermoplastic bumps. After sawing or dicing the wafer to form the chips, the chips are adhered to chip carriers with conductive pads which match the conductive thermoplastic bumps, using heat and pressure. Chips may be easily removed and replaced using heat.

[0017] U.S. Pat. No. 5,591,678 discloses a microelectric device, which is fabricated by furnishing a first substrate having a silicon etchable layer, a silicon dioxide etch-stop layer overlying the silicon layer, and a single-crystal silicon wafer overlying the etch-stop layer. The wafer has a front surface not contacting the etch stop layer. A microelectronic circuit element is formed in the single-crystal silicon wafer. The method further includes attaching the front surface of the single-crystal silicon wafer to a second substrate, and etching away the silicon layer of the first substrate down to the etch-stop layer. The second substrate may also have a microelectronic circuit element therein that can be electrically interconnected to the microelectronic circuit element.

[0018] U.S. Pat. No. 5,656,548 discloses a multi-layered structure fabricated in which a microprocessor is configured in different layers and interconnected vertically through insulating layers which separate each circuit layer of the structure. Each circuit layer can be fabricated in separate wafer or thin film material and then transferred onto the layered structure and subsequently interconnected.

[0019] U.S. Pat. No. 5,656,552 discloses a method of making a multi-chip module by thinning individual integrated circuit die or an integrated circuit wafer containing multiple integrated circuits, bonding thinned dice or a thinned wafer to a mylar, polyimide, semiconductor, or a ceramic substrate, and depositing at least one interconnect material over the wafer, where the first interconnect layer is deposited directly over the wafer. A dielectric layer is disclosed as being deposited over each of the interconnect layers. Vias are opened in the dielectric layers in order to interconnect the dice and multip-chip module as required, and the substrate is removed to form a thin, conformal, and high-yielding multi-chip module.

[0020] U.S. Pat. No. 5,716,881 discloses a fabrication process for integrating stacked capacitor DRAM devices, and thin film transistor SRAM devices. The fabrication process includes combing key operations used to create transfer gate transistor structures, and access transistor structures for the DRAM and SRAM devices.

[0021] U.S. Pat. No. 5,770,487 discloses a method of manufacturing a device whereby a layer structure with semiconductor elements and conductor tracks is formed on a first side of a semiconductor wafer which is provided with a layer of semiconductor material disposed on an insulating layer. The semiconductor wafer is subsequently fastened with the first side to a support wafer by means of a glue layer. The support wafer is provided with a metallization. Material is then removed from the semiconductor wafer from the second side of the semiconductor wafer until the insulating layer is exposed. Contact windows are provided in the insulating layer from the first side of the semiconductor wafer before the latter is refastened on the support wafer. These windows are filled with a material which can be removed selectively relative to the insulating layer. The contact windows are opened from the second side of the semiconductor wafer after the latter has been fastened on the support wafer and after the insulating layer has been exposed.

[0022] U.S. Pat. No. 5,784,261 discloses formation of low profile microchip module assemblies by first mounting one or more active semiconductor integrated circuit chips on a multilayer metallization and dielectric structure disposed on a substrate by wire bonding or flip-chip solder bonding, and then inverting the substrate and mounting it on a printed circuit board by means of solder bump connections. The solder bump connections are sufficiently high for the chips to be held clear of the printed circuit board.

[0023] U.S. Pat. No. 5,807,783 discloses a bonded wafer having a first handle wafer, a device layer, an interconnected layer, and a number of vias filled with conductive material that extends between surfaces of the device layer. The interconnect layer has conductors that connect internal device contacts to the conductive vias. A second handle wafer of glass is bonded to the interconnect layer and the first handle wafer is removed. Bottom, external contacts are formed on a surface of device layer.

[0024] U.S. Pat. No. 5,811,879 discloses a multi-chip module (MCM) and method of manufacturing same which provides for attachment of semiconductor dice to both sides of the MCM printed circuit boards (PCB). Semiconductor dice, attached to the top surface of the PCB, may be attached by conventional wire bonding, TAB or flip chip methods. Those semiconductor dice attached to the bottom surface of the PCB are wire bonded or TAB connected to the top surface through openings in the PCB. The openings provide a lead-over chip (LOC) arrangement for those semiconductor dice attached to the bottom surface. The bottom surface of the PCB may be provided with die recesses into which the openings extend, to receive the dice and bring their active surfaces even closer to the top surface of the PCB for wire bonding.

[0025] U.S. Pat. No. 5,838,545 discloses a high performance, low cost multi-chip module package using a heatsink as a substrate with thin film wiring techniques or multilayered wiring techniques for interconnection of the chips on the surface of the module and a solder column grid array or solder ball grid array for interconnection to the next level of packaging (printed circuit board). The columns or balls create a space between the board and module with the chips being in the space and provide the required interconnect density.

[0026] U.S. Pat. No. 5,843,806 discloses methods for packaging TAB-BGA integrated circuits which include providing a double-sided polyimide,. forming first dry film layers, sequentially performing a multi-layer electroplating operation of electro-coppering, electronickelling, gold plating and electronickelling again (or electronickelling and gold plating, or electro-coppering and electronickelling), and removing the first dry film layers. A lower second dry film layer serves as a mask for etching a bottom thin copper layer to define a plurality of predetermined openings, and the bottom thin copper layer serves as a mask for applying a laser etching operation to the polymide substrate to define holes without totally penetrating the polymide substrate. An electrolytic plating operation is applied to the holes for forming protruding contacts, and the exposed top thin copper layer is etched or removed. A chip installation hole and a plurality of through holes are respectively defined by performing a laser drilling operation, and a chip is attached to the two electroplated multi-layer (or double-layer) protrusions beside the chip installation hole by using a single point bond method.

[0027] U.S. Pat. No. 5,851,845 discloses a method for packaging semiconductor dice. The package includes a thinned die mounted on a compliant adhesive layer disposed on a substrate. The package is formed by providing a wafer containing a plurality of dice, thinning a backside of the wafer by etching or polishing, attaching the thinned wafer to the substrate, and then dicing the wafer. The semiconductor package may be mounted to a supporting substrate such as a printed circuit board in a chip-on-board configuration. The compliant adhesive layer and substrate of the package eliminate stresses and cracking of the die caused by a thermal mismatch between the die and supporting substrate. In addition, the semiconductor package can be mounted in a flip chip configuration with the substrate for the package protecting a backside of the die from radiation.

[0028] U.S. Pat. No. 5,856,937 discloses a processor module having a cache of SRAM chips mounted on both a back and front surface, and de-coupling capacities mounted on only the back surface. Each de-coupling capacitor is for suppressing current spikes from a pair of SRAM chips. The pair of SRAM chips includes a first SRAM chip on the same surface as the capacitor and a second SRAM chip opposite the first SRAM chip on the front surface of the module. The first SRAM chip belongs to a first bank while the second SRAM chip belongs to a second bank. Two chip-enable signals control access to the two banks. Only one bank and only one SRAM chip in the pair of SRAM chips creates a current spike at any time. Thus, a capacitor can be shared between the two SRAM chips in the pair. The shared capacitor may be mounted next to or under one of the SRAM chips, or formed within the multi-layer substrate itself.

[0029] U.S. Pat. No. 5,859,397 discloses a process for producing a photovoltaic element by the steps of: providing a photovoltaic element comprising a lower electrode layer having a metallic layer comprising aluminum or an aluminum compound and a transparent and electrically conductive layer, a photoelectric conversion semiconductor layer, and a transparent electrode layer stacked on an electrically conductive surface of a substrate, and immersing the photovoltaic element in an electrolyte solution to passivate a short-circuited current path defect present in the photovoltaic element by the action of an electric field.

[0030] U.S. Pat. No. 5,863,412 discloses a method for etching an object having a portion to be etched on the surface thereof. The method comprises the steps of: immersing the object in an electrolyte solution such that the object serves as a negative electrode, arranging a counter electrode having a pattern corresponding to a desired etching pattern to be formed at the portion to be etched of the object in the electrolyte solution so as to maintain a predetermined interval between the counter electrode and the object, and applying a direct current or a pulse current between the object and the counter electrode to etch the portion to be etched of the object into a pattern corresponding to the pattern of the counter electrode.

[0031] U.S. Pat. No. 5,863,829 discloses a process for fabricating an SOI substrate with no peripheral scratches and with enhanced fabrication efficiency. The present process includes bonding a semiconductor wafer of an active substrate onto a semiconductor base wafer to form a bonded wafer. The active substrate is surface-grounded and then spin etched.

[0032] U.S. Pat. No. 5,866,441 discloses an electronic packaging module for inverted bonding of semiconductor devices, integrated circuits, and/or application specific integrated circuits and having protuberances on the conductive pattern of the substrate. The protuberances are ductile metal which is capable of being metallurgically bonded to the input/output pads of semiconductor devices. The input/output pads of the semiconductor devices are simulataneously bonded to the protuberances of the packaging module.

[0033] U.S. Pat. No. 5,872,025 discloses stacked three-dimensional devices prepared by stacking wafers as an alternative to stacking individual devices. Chip regions are formed on several wafers with each chip region being surrounded by a separation region, such as an insulator filled trench. The wafers are subsequently stacked with the chip regions in alignment. Aligning the wafers may be facilitated using notched regions in the periphery of the wafers. The wafers are subsequently joined together by lamination. After laminating the stacks of wafers, stacks of chips are separated by etching, dicing or other processes, which separate out stacked chip devices from the stacked wafer at the chip separation regions.

[0034] U.S. Pat. No. 5,872,700 discloses microcircuit packaging techniques, and more particularly packaging of a structure compiled of several microcircuits. Unpackaged components are mounted on a substrate, and to the substrate there is attached a tape. Solder bumps are formed on a side of the tape so that the whole structure can be mounted to a circuit board by applying conventional surface-mounting techniques. The connections between the solder bumps and

the I/O lines of the substrate are realised by conductive patterns formed on the tape, and by leads provided at the edges of the tape.

[0035] U.S. Pat. No. 5,877,034 discloses a method of making a three-dimensional integrated circuit by the steps of: transferring fully processed devices from a device layer of first substrate to an auxiliary substrate, separating the auxiliary substrate and the devices thereon into individual chips, testing the chips for their functionality and mounting functioning chips on a carrier substrate in a side-by-side arrangement to form a device layer therein, and thereafter mounting a further device layer on the device layer of the carrier substrate.

[0036] Accordingly, there is a need in the art to provide a capacitance to the MCM module substrate which is capable of operating at higher frequencies. More specifically, there is a need for a method for efficiently producing a reliable high-density multilayer circuit structure in a cost effective manner.

SUMMARY OF THE INVENTION

[0037] The present invention provides a method for deplating defective capacitors comprising forming a plurality of capacitors on a semiconductor substrate, forming a plurality of metal contacts on the plurality of capacitors, and depositing a layer of photoresist on the semiconductor substrate. The method for deplating defective capacitor additionally comprises patterning the photoresist layer so that the plurality of metal contacts are exposed, contacting the exposed metal contacts with an electrically conductive solution, and deplating metal contacts which are disposed over defectively capacitors (e.g. capacitors having at least one short circuit). Also provided is a method for forming a multi-chip module comprising forming a thin-film polymeric interconnect structure having a first side and a second side disposed on a silicon substrate having active or passive devices, and mounting a computer chip on the first side of the thin-film interconnect structure. The method for forming a multi-chip module may further comprise reducing the thickness of the semiconductor substrate to form a thin semiconductor layer, and subsequently forming an aperture through the thin semiconductor layer. A ceramic carrier may be disposed on the semiconductor layer on a side opposite the interconnect structure. A further aspect of embodiments of the present invention is a multi-chip module comprising a thin-film polymeric interconnect structure having a first side and a second side, a chip disposed on the first side, and semiconductor layer disposed directly on the second side and having active or passive devices. The active devices may comprise SRAMS, and the passive devices may comprise chip capacitors. The semiconductor layer further comprises an aperture extending through the layer and filled with a solder material.

[0038] The present invention further provides a multichip module substrate capacitor structure comprising a substrate having a top surface and a bottom surface, a doped region of the substrate located at the substrate's top surface, an ohmic contact located on the top surface of the substrate, and a first dielectric layer disposed over the doped region. A first conductive layer includes a top surface and a bottom surface and is disposed over the first dielectric layer with its bottom surface adjacent to the first dielectric layer. The first conductive layer has at least a sub-layer of a first conductive material disposed at its top surface. A second dielectric layer is disposed over the first conductive layer, and an aperture is formed in the second dielectric layer over the first conductive layer to expose a portion thereof. A conductive via is formed through the aperture and is disposed against a portion of the first conductive layer and includes a second conductive material disposed adjacent to the sub-layer of the first conductive material of the first conductive layer. A second conductive layer is disposed over the second dielectric layer with its bottom surface adjacent to the second dielectric layer. The second conductive layer includes a portion therefor disposed over the conductive via.

[0039] Embodiments of the invention are also directed to methods for forming multilayer circuit structures, particularly high density multilayer circuit structures, having stacked via structures. The via structures are preferably stacked conductive posts.

[0040] One embodiment of the invention may be directed to a method for forming a multilayer circuit structure. The method comprises: forming a first plurality of conductive posts on first and second sides of a circuitized core structure, each conductive post having an end proximate to the core structure and an end distal to the core structure; depositing a first dielectric layer on the first side of the core structure; depositing a second dielectric layer on the second side of the core structure; removing dielectric layer material from the distal ends of the first plurality of conductive posts; and forming a second plurality of conductive posts on the distal ends of the first plurality of conductive posts.

[0041] Another embodiment is directed a method comprising: forming a first plurality of conductive posts on a side of a circuitized core structure, each conductive post having an end proximate to the core structure and an end distal to the core structure; laminating a dielectric layer on the core structure; depositing a protective layer on the dielectric layer; removing dielectric layer material from the distal ends of the first plurality of conductive posts through the protective layer; and forming a second plurality of conductive posts on the distal ends of the first plurality of conductive posts.

[0042] The present invention also provides a method for forming a solder bump on a metal comprising providing a metallic support; depositing a first solder layer on the metallic support; and depositing a second solder layer on the first solder layer. A third solder layer may be disposed on the second solder layer. The first solder layer comprises a first solder composition and the second layer comprises a second solder composition which is generally different than the first solder composition. The third solder layer comprises a third solder composition, which may be generally different than the second solder composition. In one preferred embodiment of the invention, the third solder composition is generally equal to the first solder composition. In another preferred embodiment of the invention the first solder composition and the third solder composition each comprise a major proportion of tin and a minor proportion of lead, and the second solder composition comprises a major proportion of lead and a minor proportion of tin. The metallic support may be a metal-filled via in a laminated substrate. Preferably, the metal-filled via comprises a blind via having a generally frusto-conical shape in vertical cross section. In another

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embodiment of the invention, a bonding sheet may be disposed on the substrate and the solder layers may be disposed in an opening in the bonding sheet.

[0043] The present invention further provides a method for forming a multilayered packaging assembly comprising forming a first metallic support on a first substrate; forming a second metallic support on a second substrate; depositing a first solder layer on the first metallic support; depositing a second solder layer on the first solder layer; and coupling the second solder layer to the second metallic support on the second substrate. The method additionally comprises rotating the second substrate 180 degrees prior to the coupling of the second solder layer to the second metallic support on the second substrate. The method further additionally comprises heating the first solder layer to a temperature higher than its melting point temperature but below a melting point temperature of the second solder layer. A third solder layer may be deposited on the second solder layer. In an alternative preferred embodiment of the invention, the method additionally comprises heating the first substrate to a temperature higher than a melting temperature of the first and third solder layers but below a melting point temperature of the second solder layer. A bonding sheet is preferably supported by the first substrate. An opening may be formed in the bonding sheet and one or more of the solder layers may be positioned in the opening. In another embodiment of the invention, the first substrate is subsequently heated to a temperature greater than the melting point temperature of the second solder layer, and the first substrate is then preferably cooled to a temperature which approximates a curing temperature of the bonding sheet.

[0044] The present invention also provides a substrate assembly and a multilayered packaging assembly. The substrate assembly comprises a substrate having a metallic member, a first solder layer disposed on the metallic member, and a second solder layer disposed on the first solder layer. The multilayered packaging assembly comprises a first substrate having a first metallic support, a first solder layer disposed on the first metallic support, a second solder layer disposed on the first solder layer, a third solder layer disposed on the second solder layer, and a second substrate having a second metallic support and coupled to the first substrate.

[0045] These provisions together with the various ancillary provisions and features which will become apparent to those skilled in the art as the following description proceeds, are attained by the methods and multilayered circuit structures of the present invention, preferred embodiments thereof being shown with reference to the accompanying drawings, by way of example only, wherein:

BRIEF DESCRIPTION OF THE DRAWINGS

[0046] **FIG. 1** is a side elevational view of conformal polymer layer(s) disposed on a substrate assembly and over conductor pads;

[0047] **FIG. 2** is a side elevational view of the substrate assembly of **FIG. 1** after deposition of gap-filling polymer;

[0048] **FIG. 3** is a side elevational view of an alternative substrate assembly with impedance control and ground planes deposited over polymeric CVD layers;

[0049] **FIG. 4** is a side elevational view of the substrate assembly of **FIG. 3** after deposition of gap-filling polymer;

[0050] **FIG. 5** is a side elevational view of a substrate assembly with conformal polymer layer(s) on a substrate assembly and over conductor(s) and previously deposited layers;

[0051] **FIG. 6** is a side elevational view of the substrate assembly of **FIG. 1** after deposition of an organic or inorganic gap-filling layer;

[0052] **FIG. 7** is a side elevational view of the substrate assembly of **FIG. 6** after depositing a planarizing layer(s) to provide a compliant sealant layer, to facilitate chemical mechanical polishing and further build-up;

[0053] **FIG. 8** is a side elevational view of the substrate assembly of **FIG. 7** after subsequent build-up;

[0054] **FIG. 9** is a side elevational view of part of the substrate assembly of **FIG. 5**;

[0055] **FIG. 10** is a side elevational view another part of the substrate assembly of **FIG. 5**;

[0056] **FIG. 11** is a side elevational view of the substrate assembly of **FIG. 1** after low dielectric constant thermoplastic particulates were deposited;

[0057] **FIG. 12** is a side elevational view of the substrate assembly of **FIG. 11** after thermal treatment;

[0058] **FIG. 13** is a side elevational view of the substrate assembly of **FIG. 12** after build-up with another substrate assembly;

[0059] **FIG. 14** is a side elevational view of part of the substrate assembly of **FIG. 5**;

[0060] **FIG. 15** is a side elevational view of another part of the substrate assembly of **FIG. 5**;

[0061] **FIG. 16** is a side elevational view of the substrate assembly of **FIG. 14** after depositing a composite of low dielectric constant polymer particulates within another planarizing low dielectric constant polymer;

[0062] **FIG. 17** is a side elevational view of the substrate assembly of **FIG. 16** after build-up with another substrate assembly;

[0063] **FIG. 18** is a side elevational view of part of the substrate assembly of **FIG. 5**;

[0064] **FIG. 19** is a side elevational view of another part of the substrate assembly of **FIG. 5**;

[0065] **FIG. 20** is a side elevational view of the substrate assembly of **FIG. 18** after disposing a thermoplastic low dielectric constant polymer film on top thereof;

[0066] **FIG. 21** is a side elevational view of the substrate assembly of **FIG. 20** after thermal treatment;

[0067] **FIG. 22** is a side elevational view of the substrate assembly of **FIG. 20** after disposing an optional planarizing layer and subsequent build-up of successive layers;

[0068] **FIG. 23** is a side elevational view of an LSI substrate assembly separated from a substrate supporting metal pads;

[0069] **FIG. 24** is a side elevational view of the LSI substrate assembly after being coupled to the pad-supporting substrate;

[0070] **FIG. 25** is a partial enlarged sectional view of one embodiment of a post in **FIG. 24** coupled to a metal pad;

[0071] **FIG. 26** is a partial enlarged sectional view of another embodiment of a post in **FIG. 24** coupled to a metal pad;

[0072] **FIG. 27** is a side elevational view of another embodiment of the two assemblies of **FIG. 23**;

[0073] **FIG. 28** is a side elevational view of the two assemblies of **FIG. 27** coupled together;

[0074] **FIG. 29** is a partial enlarged elevational view of one embodiment of a post in **FIG. 28** coupled to a metal pad;

[0075] **FIG. 30** is a side elevational view of another embodiment of the two assemblies of **FIG. 23**;

[0076] **FIG. 31** is a side elevational view of the two assemblies of **FIG. 30** coupled together;

[0077] **FIG. 32** is an enlarged elevational view of two posts in **FIG. 31** coupled together;

[0078] **FIG. 33** is a side elevational view of another embodiment of the two assemblies of **FIG. 23**;

[0079] **FIG. 34** is a side elevational view of the two assemblies of **FIG. 33** coupled together;

[0080] **FIG. 35** is an enlarged elevational view of a post in **FIG. 34** coupled to a cup member;

[0081] **FIG. 36** is a partial perspective view of a wire interconnect structure (e.g., a WIT) spaced from a cup member;

[0082] **FIG. 37** shows a cross section of a multilayer circuit structure with staggered via structures;

[0083] FIGS. **38** to **51** show cross sections of multilayer circuit structure precursors used to form a multilayer circuit structure with stacked conductive posts;

[0084] **FIG. 52** shows a cross section of a multilayer circuit structure with stacked conductive posts;

[0085] **FIG. 53** shows a cross section of another embodiment of a multilayer circuit structure assembly;

[0086] FIGS. **54** to **57A** illustrates the fabrication process for forming a substrate having a plurality of metal-filled vias with each via supporting an embodiment of the solder bump(s) of the present invention;

[0087] **FIG. 57B** is an enlarged sectional view of one embodiment of the solder bump;

[0088] **FIG. 57C** is an enlarged sectional view of another embodiment of the solder bump;

[0089] **FIGS. 58A** to **63A** illustrate one embodiment of process flow steps for forming the multilayer circuit structure assembly of **FIG. 53**;

[0090] **FIGS. 58B** to **65B** illustrate another embodiment of process flow steps for forming the multilayer circuit structure assembly of **FIG. 53**;

[0091] **FIG. 66** is a side elevational view of a semiconductor substrate assembly supporting a good capacitor and a defective capacitor with a short circuit;

[0092] **FIG. 67** is a side elevational view of the substrate assembly of **FIG. 66** after depleting the defective capacitor and removing the photoresist, and after depositing a dielectric layer (e.g. a polyimide coat);

[0093] **FIG. 68** is a side elevational view of a MCM substrate assembly;

[0094] **FIG. 69** is a side elevational view of the MCM substrate assembly of **FIG. 68** after formation of a through via;

[0095] **FIG. 70** is a side elevational view of the MCM substrate assembly of **FIG. 69** after coupling a ceramic (e.g. Al N) substrate thereto and after depositing SnAg paste or solder balls into the via holes;

[0096] **FIG. 71** is a side elevational view of the MCM substrate assembly of **FIG. 70** after coupling a silicon substrate thereto;

[0097] **FIG. 72** is a side elevational view of a 3D superchip for a high performance MCM substrate assembly;

[0098] **FIG. 73** is a top plan view of the substrate assembly of **FIG. 72**;

[0099] **FIG. 74** is a side elevational view of an alternative assembly with 3D superclip for 8-way server;

[0100] **FIG. 75** is a top plan view of the substrate assembly of **FIG. 74**;

[0101] **FIG. 76** is another cross-sectional view of the embodiment of a multichip module substrate according to the present invention;

[0102] FIGS. **77-83** illustrate a primary substrate according to the present invention at various stages of processing to form de-coupling capacitors according to the present invention; and

[0103] FIGS. **84-87** illustrate a primary substrate according to the present invention at various stages of processing to form de-coupling capacitors according to embodiments of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[0104] Referring in detail now to the drawings, there is seen in FIGS. **1-22** various embodiments of a structure and method for making a low dielectric constant MCM. Structures and methods of the type illustrated in FIGS. **1-22** are of priority of future generation MCM's as they will enable gigahertz speed products without huge losses, noise, and delays. The advantages of a low dielectric constant MCM of the various embodiments of the present invention are: (1) higher performance MCMs may be made with lower dielectric constants; (2) reduces amount of chemical mechanical polishing (CMP) required by using only conformal dielectric coatings in the MCMs; (3) enables better dielectric-layer adhesion than possible with only one type of dielectric polymer because of using two or more dielectric polymers; and (4) enables controlled impedance structures. A dielectric constant is a value serving as an index of the ability of the dielectric material(s) (e.g., polymers) to resist the transmission of an electrostatic force from one charged body to another. The dielectric materials utilized in various embodiments of the present invention for producing low dielectric

constant MCMs have a low dielectric constant, such as a dielectric constant less than about 3.8 at 20° C. In a preferred embodiment of the invention, the dielectric constant at 20° C. for the dielectric materials ranges from about 1.2 to about 3.4; preferably from about 1.4 to about 3.0; more preferably from about 1.6 to about 2.8; most preferably from about 1.8 to about 2.7; such as from about 2.0 to about 2.6 including from about 2.1 to about 2.5.

[0105] Suitable dielectric material(s) include B-stage polymeric compounds, such as polyimides, epoxy resins, polyurethanes or silicons, provided that these compounds are produced with a low dielectric constant at 20° C. Additional suitable materials could include thermosetting materials, such as high glass transition anhydride-cured epoxy composition possessing a low dielectric constant at 20° C. More particular suitable thermoset materials include, but are not limited to, one or more compounds produced with a low dielectric constant at 20° C. and selected from group consisting of epoxies and modified epoxies, melamine-formaldehydes, urea formaldehydes, phelonic resins, poly(bis-maleimides), acetylene-terminated BPA resins, IPN polymers, triazine resins, and mixtures thereof. Further additional suitable materials include high temperature thermoplastic materials, such as liquid crystal polyesters (e.g., Xydar™ or Vectra™), poly-(ether ether ketones), or the poly(aryl ether ketones), provided that these thermoplastic materials are produced such as to possess the low dielectric constant at 20° C. Additional suitable thermoplastic materials include, by way of example only, ABS-containing resinous materials (ABS/PC, ABS/polysulfone, ABS/PVC), acetals acrylics, alkyds, allylic ethers, benzocyclobutenes, cellulosic esters, chlorinated polyalkylene ethers, cyanate, cyanamides, furans, parylene amorphous fluoropolymers, polyalkylene ethers, polyamides (Nylons), polyarylene ethers, perfluoroalkoxy polymeric resins, fluoroethylenepropylene polymers, polybutadienes, polycarbonates, polyesters, polyfluorocarbons, polyimides, polyphenylenes, polyphenylene sulfides, polypropylenes, polystyrenes, polysulfones, polyurethanes, polyvinyl acetates, polyvinyl chlorides, polyvinyl chloride/vinylidine chlorides, polyetherimides, and the like, and mixtures of any of the foregoing, provided that the materials are manufactured to have a low dielectric constant at 20° C.

[0106] In another preferred embodiment of the invention the low dielectric constant material comprises a polymer having the repeat structure $(—CH_2C_6H_4CH_2—)_n$ wherein n is an integer having a value ranging from about 2,000 to about 8,000; more preferably from about 3,000 to about 7,000; most preferably from about 4,000 to about 6,000, such as from about 4,500 to about 5,500 including from about 4,800 to about 5,200. In a further embodiment of the invention the low dielectric constant material comprises the repeat structure $(—CF_2—CF_2—)_n$ wherein n is an integer having a value ranging from about 3,000 to about 16,000; more preferably from about 4,000 to about 14,000; most preferably from about 8,000 to about 12,000.

[0107] Referring now to FIGS. **1-3**, a thin conformal coating of one low dielectric constant layer of material **16** is first deposited over the conductor traces **14** (i.e., Cu) supported by substrate **10**. A conformal coating is a coating which has sufficient viscosity to generally conform to an underneath supporting surface as shown in **FIG. 1**. A conformal coating is also a coating which deposits in a generally uniform thickness as shown in **FIG. 1**. A conformal coating is furthermore a coating which does not have to be polished (e.g., such as by CMP) after deposition. Conductor traces **14** (or pads or regions) may be plated and/or sputtered onto substrate **10**. This layer of material **16** provides good adhesion to the conductor traces **14**, and may be deposited by any suitable manner, such as chemical vapor deposition (CVD), sprayed on, or spun on. Optionally, a second low dielectric constant layer of material **18**, preferably a conformal layer of material **18**, may subsequently be deposited on and/or over layer of material **16**. The layer of material **18** may be manufactured from a material having less adhesion to the conductor traces **14** but good adhesion to the layer of material **16**. Thus, by way of example only, the material **16** may comprise the repeat structure $(—CH_2C_6H_4CH_2—)_n$ where n ranges from about 4,500 to about 5,500; and material **18** may comprise a fluorinated parylene, such as, by way of example only, one having the repeat structure $(—CHFC_6H_2F_2CHF—)_n$ wherein n is an integer having a value ranging from about 2,000 to about 8,000; more preferably from about 3,000 to about 7,000; and most preferably from about 4,000 to about 6,000. The low dielectric constant for material **16** may have a value which is less than, or more than, the value of the low dielectric constant for the material **18**. More specifically, the dielectric constant for material **16** may be less than about 2.3 (or less than about 1.8) whereas the dielectric constant for material **18** may be greater than about 2.3 (or greater than about 1.8), i.e., a value ranging from greater than about 1.8, or from about 2.3 to about 3.8, and vice versa, i.e., dielectric constant for material **18** is less than about 2.3, or less than about 1.8, and the dielectric constant for material **16** is greater than about 1.8, or greater than about 2.3 up to and including about 3.8.

[0108] A gap-filling material **20** is subsequently deposited (e.g., spun on) in voids **24** between spaced material **16** (see **FIG. 2A** and **FIG. 4**). In **FIGS. 1 and 2B**, the gap-filling material **20** is disposed (e.g., spun on) in voids **26** between spaced material **18** which is supported by material **16**. Any excess gap-filling material **20** extending about material **16** and/or material **18** may be polished or planarized down until a planar surface **20*a*** registers with planar surfaces **16*a*-16*a*** of material **16** or with planar surfaces **20*a*-20*a*** of material **20** (see **FIG. 2A**). The material **20** is one or more of the previously mentioned low dielectric constant materials. The low dielectric constant for material **20** may be the same as, less than, or greater than the dielectric constant for material **16** and/or material **18**.

[0109] Fluorinated parylene AF_4 has a dielectric constant of approximately 2.3 with a very low dissipation constant (approaching that of Teflon). Future AF_4 variants will have even lower values of dielectric constant and dissipation factor. It has been surprisingly discovered that heat treatments in a specific temperature range result in highly desirable improvements in the mechanical properties of parylene AF_4 films. Without this inventive heat treatment, the thermal expansion coefficient of films are in excess of 100 ppm. Following the heat treatment, the films exhibit thermal expansion coefficients of ~35 ppm. Even more importantly, the total elongation to plastic instability of the films is changed >100% from undesirable values of 5-10% to much more desirable values in excess of 15-20%. Without

a property enhancement such as this, it is very unlikely that multilayer electrical circuits could be manufacturable or made reliable.

[0110] Free standing parylene AF_4 films of 50-100 micron thickness were deposited by the Gorham process at platen temperatures of both −15° C. and −25° C. The lower temperature deposition temperature is believed to result in higher molecular weights of the polymer film. From these films dogbone specimens with gauge widths of 4 mm and gauge lengths of 1 cm were cut using a YAG laser. The specimens were then pulled to failure in an Instron at strain rates of 10^{-2}/sec. The lower molecular weight film became plastically unstable and fractured at essentially the same lower strain values of ~6-9%. The higher molecular weight films became plastically unstable at essentially the same strains as the higher molecular weight film. The toughness of these films is unacceptable for multilayer film build-up (strains in excess of 10% prior to plastic instability are required). The films exhibit young's moduli of approximately 1 Gpa and sustain stresses of roughly 50 Mpa to the point of plastic instability. The following vacuum (<1 mbar) heat treatments of the films as set forth in the following Table 1 were performed prior to cutting the tensile specimens:

TABLE 1

Heat Treatment (HT) Temperature (° C.)	Time @ HT Temperature	Elongation prior to plastic instability
As-Received		<5–8%
280	1 hr	~10%
300	1 hr	~10%
300	4 hr	~10%
330	Ramp and cool	~20%
330	1 hr	~20%
330	16 hr	~20%
400	1 hr	~20%
450	1 hr	~10%

[0111] In another embodiment of the invention and as best shown in **FIG. 3**, a ground layer **30** may be disposed over material **20**; or alternatively, over material **18** which is used to fill the voids **24** instead of material **20**. Subsequently, a second material **16***s* is deposited as indicated with second conductor traces **14***s* disposed as shown in **FIG. 3**. The ground layer **30** may serve to both control impedance and provide mechanical stability to the structure.

[0112] Referring now to FIGS. **4-8** for another embodiment of the invention, masking may be used on the layer of material **16** to remove or discontinue material **16** from one conductor trace **14** to a contiguous conductor trace **14**, as best shown in **FIG. 5**. Subsequently, a low dielectric constant material **34**, such as xerogel, sesquisilones, etc., is deposited over the material **16**. The layer of material **34** may be thermally cured and may contain or develop voids and cracks, especially as deposited layers exceed about one micron in thickness. Subsequently chemical mechanical polishing (CMP) and structural stability are facilitated with a deposit of a low dielectric constant layer **36** (see **FIG. 7**), such as Teflon AF, parylene, PAE, BCB or low molecular weight reactive oligimers with low dielectric constants. CMP may then be performed and a next layer may be constructed. An additional or alternative layer (not shown in the drawings) of parylene, PAE, BCB or low molecular weight reactive oligimers with low dielectric constants may be deposited after CMP of the layer of material **34** to better enable a subsequent layer (not shown) of conductor to adhere. As was seen for the embodiment of the invention in **FIG. 3**, the conformal coating of material **36** may be thicker than the layer of material **34**, and subsequently the conducting ground layer **30** may be deposited on material **36** as shown in **FIG. 8**. This ground layer **30** may serve to both control impedance and provide mechanical stability to the structure. These "sidewalls" of the impedance controlling ground layer **30** may alternatively be deposited to a thickness for which adjoining sidewalls bridge one another.

[0113] Referring now to FIGS. **9-22** for additional embodiments of the present invention, there is seen in **FIG. 11** a plurality of low dielectric constant particulate material **40**. The particulate material **40** may comprise or consist of material **16** and/or material **18** and/or material **34**, or any of the previously mentioned low dielectric constant material(s). The particulate material **40** may be applied to the surface of material **16** and/or material **18** by any suitable manner, such as by spreading, spray, transfer, etc. The particulate material **40** is then thermally processed to flow material **40** and enable it to substantially fill the gaps to produce material **40***a* (see **FIG. 12**). The temperature (e.g., a temperature ranging from about 85° C. to about 200° C.) to cause particulate material **40** to flow would depend on the composition of low dielectric constant material **40**. Voids may be retained in this layer if desired. Material **36** may be disposed on material **40***a*, and ground layer **30** may be deposited on material **36**, followed by disposing on ground layer **30** another assembly of traces **14**, material **16** and material **40***a*.

[0114] Referring now to FIGS. **14-17**, a thin, essentially conformal coating of one low dielectric constant material **16** (i.e., parylene, PAE, BCB or low molecular weight reactive oligimers with low dielectric constants) is first deposited over the conductor traces **14** (i.e., Cu). The conductor traces **14** may be plated and/or sputtered onto substrate **10**. Layer of material **16** possesses good adhesion for the conductor traces **14**. Material **16**, as previously indicated, is preferably deposited from the vapor phase, but may be spun or sprayed on. An optional separate or phased-in (gradient composition or co-deposited) thin conformal layer **18** with less adhesion to the conductor traces **14** but good adhesion to the first layer **16** (e.g., inorganic containing dielectrics, fluorinated parylene, fluorinated PAE, fluorinated BCB or low molecular weight reactive oligimers with low dielectric constants) may then be deposited, as shown in **FIG. 2B**. This layer **18** should also have good adhesion to successive additions and layers. Masking can be used to make such polymer layers discontinuous from conductor to conductor. Such layers may serve as a diffusion or electromigration barriers as well as an adhesion promoter.

[0115] Next, and as shown in **FIG. 16**, a composite layer of polymer **42** (e.g., Teflon AF, liquid crystal polymer, etc.) and/or inorganic containing dielectrics is deposited together within another planarizing low dielectric constant material (e.g., inorganic containing dielectrics, fluorinated BCB or low molecular weight reactive oligimers with low dielectric constants). Particulates **44** may be pressed into fluid or fluid spun on lightly compressed (and/or partially sintered) particulates. Also, they can be co-deposited by spray or spin-on processes. Alternatively, the particulates **44** may be precipitated out of solution (chemically or via solvent removal).

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The structure may alter its spatial geometry during curing as the thermoplastics may flow somewhat at elevated temperatures. Voids may be retained in this layer. Subsequent CMP and structural stability may be facilitated with a planarizing deposit of inorganic dielectric, BCB or low molecular weight reactive oligimers with low dielectric constants deposition on top of the thermoplastic. CMP may then be performed and a next layer can be constructed. An additional layer of inorganic containing dielectric, parylene, PAE, BCB or low molecular weight reactive oligimers with low dielectric constants may be deposited after CMP to better enable the next layer of conductor to adhere.

[0116] As best shown in **FIG. 17**, another conformal polymer layer **42** and conductor traces **14** may be formed for further circuit buildup. The optional ground layer **30** may be deposited prior to this second layer buildup for dimensional stability and/or electrical performance.

[0117] Referring now to FIGS. **18-22**, after the low dielectric constant assembly is formed (see FIGS. **18-19**), as the same low dielectric assembly of FIGS. **4-5**, **9-10** and **14-15** was formed, a thermoplastic film **50** (e.g., Teflon AF, PFTE, PFA, FEP, liquid crystal polymer, etc.) with low dielectric constant is placed over the appropriately coated circuitry. The film **50** may be thermally laminated or autoclaved onto the circuitry, as best shown in **FIG. 21**. Subsequent CMP and structural stability may be facilitated with a planarizing deposit of inorganic dielectric, BCB or low molecular weight reactive oligimers with low dielectric constants deposition on top of the thermoplastic. As previously indicated, CMP may then be performed and a next layer may be formed. An additional layer of inorganic containing dielectric material **54**, such as parylene, PAE, BCB or low molecular weight reactive oligimers with low dielectric constants may be deposited on film **50**, followed preferably by CMP to better enable the next layer of conductor to adhere. **FIG. 22** discloses a second layer build-up, similar to the second layer build-ups of **FIGS. 8, 13, 17** and **22**.

[0118] Referring now to FIGS. **23-36** for describing a method and structure which utilizes the "Wire Interconnect Structure" (WIT) and "Transient Liquid Alloy Bonding" (TLAB) on ultra-fine-pitch flip chip technology. WIT structure provides an ultra-fine-pitch interconnection method between LSI and a substrate. TLAB provides a reliable lead-free bonding method. The depletion layer of the TLAB can be located at the bottom pad (substrate side), on the wire structure, or at the middle of the wire structure.

[0119] As respectively illustrated in FIGS. **23-26**, FIGS. **27-29**, FIGS. **30-32**, and FIGS. **33-36**, embodiments of the invention include four types of structures. The first structure of FIGS. **23-26** illustrates the WIT on an LSI side and a depletion phase (Sn, In or Sn/In alloy) on a substrate side. The second structure of FIGS. **27-29** illustrates the depletion phase on the WIT structure, which may be done by sequential electroplating. The third structure of FIGS. **30-32** illustrates the depletion phase located at the middle of the final WIT structure, which is accomplished by electroplating of depletion phase on one side of WIT or both sides (i.e., half-WIT is built on both sides first). The fourth structure of FIGS. **33-36** illustrates a cup structure combined with the WIT structure. The cup structure provides an anchoring function to hold the WIT tip. It supports the structure with a good laterally mechanical strength and can transfer the shearing stain/stress directly to the WIT structure but not the joint interface. In the fourth structure, the Sn can be within the cup structure or on the tip of WIT. Also, the cup height can be low, which will be functioned to compensate the stress concentration directly, or be high to avoid the high stress point.

[0120] Referring more specifically now to FIGS. **23-36**, there is seen a substrate **56** supporting a plurality of metal pads **58** (i.e., pads **58*a***, **58*b***, **58*c***, **58*d*** and **58*e***) which in turn support depletion layers **60** (i.e., depletion layers **60*a***, **60*b***, **60*c***, **60*d*** and **60*e*** such as Sn and/or In deposited by electroplating). There is also seen an LSI substrate **62** supporting a plurality of conductive pads **64** (i.e., conductive pads **64*a***, **64*b***, **64*c***, **64*d*** and **64*e***), having connected thereto wire interconnect structures (WISs) **66** (i.e., WTIs **66*a***, **66*b***, **66*c***, **66*d*** and **66*e***) which may be fabricated by electroplating with a thick photoresist and preferably may be copper and/or gold. The advantage of gold is that it can provide better elasticity when employed at a high CTE mismatch circumstance. In **FIGS. 27, 30** and **33**, the depletion layers **60*a***, **60*b***, **60*c***, **60*d*** and **60*e*** are respectively deposited on the terminal ends of the WTIs **66*a***, **66*b***, **66*c***, **66*d*** and **66*e***. In **FIG. 30**, WTIs **66** are divided such that part of the respective WTIs **66** is coupled to and supported by LSI substrate **62** and part is coupled to and supported by substrate **56**. Furthermore with respect to the embodiment of the invention in **FIG. 30**, depletion layers **60** are divided between the two sets of WTIs **66-66** and disposed on terminal ends of the respective WTIs **66-66**. In **FIG. 33** substrate **56** supports a plurality of conductive cups **68** (i.e., cups **68*a***, **68*b***, **68*c***, **68*d*** and **68*e***) for receiving terminal ends of WTIs **66** including the respective depletion layers **60** associated with the terminal ends of WTIs **66**. The conductive (e.g., copper) cups **68** are preferably fabricated by electroplating. A donut shape ring is exposed for depositing the conductive cups **68**. The depletion layers **60** may be deposited on the terminal ends of the WTIs **66** or inside the respective conductive cups **68** either by electroplating, immersion or evaporation.

[0121] The LSI substrate **62** and substrate **56** are aligned by a suitable aligner, e.g., a flip-chip bonder by Karl Suess. The aligned pair is subsequently pressed and heated by a flip-chip bonder in air or nitrogen environment. The temperature needs to be higher than the melting point of the depletion layers **60** and held for a certain period of time. The melting temperature is around 232° C. for Sn, 157° C. for In and between 120° C. to 232° C. for Sn-In temperature alloy(depending on the alloy composition). The time should be long enough to convert the molten phase of depletion layers **60** completely into an alloy or intermetallic compounds **60*a'***, **60*b'***, **60*c'***, **60*d'*** and **60*e'*** with the base metal (e.g., copper or gold). More desirably, the depletion layers **60** are to be converted completely into a strong and reliable metal phase which depends on the metallurgical system used. Lastly, the underfill is applied between the interconnects to form a reliable chip packaging. Another alternative way to put in underfill material is during the bonding process by using a liquid-type underfill that can be cured during the bonding process.

[0122] Referring in detail now to FIGS. **37-52**, embodiments of the invention are directed to methods for forming multilayer circuit structures. In preferred embodiments, the methods comprise forming a first plurality of conductive posts on first and second sides of a circuitized core structure.

Each conductive post has an end proximate to the core structure and an end distal to the core structure. After the conductive posts are formed, a first dielectric layer is deposited on the first side of the core structure and a second dielectric layer is deposited on the second side of the core structure. Dielectric layer material deposited on the distal ends of the first plurality of conductive posts is then removed. After removing the dielectric layer material from the ends of the posts, circuit patterns are formed on the dielectric layers. The formed circuit patterns can include conductive pads disposed over the cleaned distal ends of the posts. A second plurality of conductive posts can then be formed on the conductive pads on the distal ends. The second plurality of conductive posts can be stacked on the first plurality of conductive posts. Additional sets of subsequently formed conductive posts (e.g., third, fourth pluralities) and pads can be stacked on the second plurality of conductive posts to form a plurality of generally vertical conductive pathways (e.g., generally perpendicular to the orientation of the core structure) through the dielectric layers. The generally vertical conductive pathways can result in a multilayer circuit structure which occupies less space than a similar multilayer circuit structure having staggered via structures.

[0123] In embodiments of the invention, multilayer circuit structures can be formed quickly and efficiently. For example, in preferred embodiments, the dielectric layers, conductive posts, and conductive patterns including conductive pads can be simultaneously formed or deposited on opposite sides of multilayer circuit structure precursors (e.g., a core structure). For example, in embodiments of the invention, conductive posts can be simultaneously electroplated on conductive regions on opposite sides of a core structure. Furthermore, in preferred embodiments, the multilayer circuit structures having stacked conductive posts can be formed using less expensive processes such as photolithography and electroplating. More expensive techniques such as laser drilling are not needed in preferred embodiments of the invention. Consequently, high density multilayer circuit structures having high circuit densities can be formed efficiently and cost-effectively.

[0124] The conductive posts and conductive patterns in the multilayer circuit structures are preferably formed by additive processes. Additive processes have advantages over subtractive processes. For example, subtractive processes use etchants to remove metal from continuous metal layers to form conductive patterns. The uniformity of the lines in the etched patterns can be difficult to control, because etchants can undercut the lines. Consequently, it can be difficult to form fine line patterns using subtractive processes. In an additive process, however, the conductive pattern resolution is limited only by the resolution of the photoresist used to form the conductive patterns. Consequently, fine line and high density circuit patterns can be produced using additive processes. For instance, the circuit lines can have widths of 25 microns or less, and can be at a pitch of about 50 microns or less. In addition, in subtractive processes, metal layers are etched and then rinsed. The etching and rinsing processes consume large amounts of wet chemicals and water and can generate large amounts of waste (e.g., wasted metal). However, because of the reduced number of etching steps used in a typical additive process, the waste generated from a typical additive process is less than a typical subtractive process.

[0125] Embodiments of the invention can be described with reference to the Figures. **FIG. 38** shows a circuitized core structure **122** upon which a plurality of conductive posts are formed. The core structure **122** includes a first side **122(*a*)** and a second side **122(*b*)**, and can be flexible or rigid. The first and second sides **122(*a*)**, **122(*b*)** can have, respectively, a first plurality of conductive regions **124(*a*)** and a second plurality of conductive regions **124(*b*)**. The first and second conductive regions **124(*a*)**, **124(*b*)** can include, e.g., lines, pads, or the ends of via structures. Moreover, the first and second conductive regions **124(*a*)**, **124(*b*)** can be made of any suitable conductive material including copper, and can have any suitable thickness including a thickness of less than about 50 microns, and preferably between about 18 to about 36 microns. In addition to having conductive regions **124(*a*)**, **124(*b*)** on the outer surfaces of the core structure **122**, the core structure **122** may also include two or more dielectric layers and one or more conductive layers (not shown) embedded within the core structure **122**.

[0126] The core structure **122** can also include one or more via structures **123**. The via structures can communicate the conductive regions **124(*a*)**, **124(*b*)** on the first and second sides **122(*a*)**, **122(*b*)** of the core structure **122**. The via structures can be solid conductive posts, or can be plated through holes (PTH) which have been filled with a conductive or a non-conductive material. For example, the PTH can be filled with a polymeric material such as an epoxy-based polymer, with or without an embedded conductive material. In another example, the PTH can be filled with a conductive paste such as a silver filled conductive paste. Filling the PTH with a material displaces any air which might otherwise reside in the PTH. It is preferable to remove any air pockets which might reside in the resulting multilayer circuit structure, because trapped air may cause reliability problems in some instances.

[0127] In a typical PTH filling process, an aperture can be formed in a rigid insulating board. Metal can be electroplated onto the wall of the aperture to form a PTH. After forming the PTH, a conductive or non-conductive filler material can be deposited within the PTH by, e.g., stenciling. If the filler material is curable, the filler material can be cured within the PTH. Before or after curing, any excess filler material on the first and second sides of the core structure can be removed.

[0128] In preferred embodiments, after the core structure is formed, a first plurality of conductive posts are formed on both the first and second sides of the circuitized core structure. Each conductive post can have an end proximate to the core structure and an end distal to the core structure. The conductive posts are preferably solid and/or substantially homogeneous in composition (e.g., all metal). The posts may also include any suitable conductive material. Suitable conductive materials include metal or metal alloys including copper, silver, gold, nickel, palladium, and aluminum. The conductive material is preferably copper.

[0129] The conductive posts may include any suitable dimensions. For example, the conductive posts can have a height of at least about 10 microns, preferably between about 15 to about 75 microns, and more preferably between about 25 to about 50 microns. The conductive posts can have any suitable diameter including a diameter between about 10 to about 150 microns, preferably between about 25 to about

75 microns. In addition, each of the posts may have a generally round radial cross-section.

[0130] The conductive posts (e.g., the first plurality of conductive posts) can be formed using any suitable process. For example, plating processes such as electroless or electroplating processes can be used to form the conductive posts.

[0131] The conductive posts are preferably formed by electroplating. With reference to **FIG. 39**, seed layers **125(*a*)**, **125(*b*)** can be deposited on the first and second sides **122(*a*)**, **122(*b*)** of the core structure **122**. The seed layers **125(*a*)**, **125(*b*)** can be used to help initiate the plating of the subsequently formed conductive posts. Preferably, the seed layers **125(*a*)**, **125(*b*)** are deposited simultaneously, but they can be deposited sequentially in some instances. Any suitable process including sputtering and electroless plating can be used to deposit the seed layers. Electroless plating is preferred as it is generally less expensive than sputtering. Regardless of how they are deposited, the seed layers **125(*a*)**, **125(*b*)** may have a thickness of about 3 microns or less. Preferably, the thickness of each seed layer is between about 0.1 to about 1.0 micron, and is more preferably between about 0.3 to about 0.6 micron.

[0132] Prior to depositing the seed layers, the first and second sides of the core structure may be conditioned. For example, to increase the adhesion of seed layers to the sides of the core structure, the surfaces of the core structure can be roughened. Roughening can be performed using any suitable process including an etch process such as a permanganate etch process. By roughening the surfaces of the core structure prior to depositing the seed layers, the seed layers are more likely to adhere to the surfaces of the core structure.

[0133] After depositing the seed layers, photoresist layers can be deposited on the seed layers. The photoresist layers can be in the form of a film or a liquid prior to being deposited on the first and second sides of the core structure. An example of a suitable dry film photoresist is Riston□ 9000, commercially available from E.I. du Pont de Nemours, Inc. An example of a suitable liquid photoresist is AZ4620 liquid photoresist commercially available from Clariant, Inc. The photoresist layers may be positive or negative, and can be deposited on the first and second sides of the core structure simultaneously or sequentially.

[0134] The photoresist layers may be deposited by any suitable process including roller coating, spin coating, curtain coating, screen printing, slot coating, spray coating, and doctor blade coating. These processes are suitable for depositing liquid photoresist layers. Preformed photoresist layers may be deposited by laminating. Preferably, the photoresist layers are deposited by laminating. For example, in some embodiments, a double-sided hot roll laminator may be used to laminate preformed layers of photoresist on both sides of the core structure simultaneously.

[0135] After depositing the photoresist layers, photoresist patterns can be formed using conventional photolithographic techniques. For example, the deposited photoresist layers can be irradiated with a pattern of radiation. The irradiated photoresist layers can then be developed to form patterned photoresist layers. For example, with reference to **FIG. 40**, after the photoresist layers on both sides of the core structure **122** are developed, the developed photoresist layers **131(*a*)**, **131(*b*)** can have a plurality of apertures **132(*a*)**, **132(*b*)** disposed over one or more conductive regions **124(*a*)**, **124(*b*)** on opposite sides of the core structure **122**. The patterned photoresist layers can be used as masks to selectively deposit conductive material in predetermined areas. Deposition processes such as electroplating or electroless plating can be used to deposit the conductive material on regions not covered by the patterned photoresist layers.

[0136] With reference to **FIGS. 40 and 41**, a first plurality of conductive posts **134(*a*)**, **134(*b*)** are formed within the apertures **132(*a*)**, **132(*b*)** of the photoresist layers **131(*a*)**, **131(*b*)**, and on the conductive regions **124(*a*)**, **124(*b*)** exposed through the photoresist layers **131(*a*)**, **131(*b*)**. In this example, the first plurality of conductive posts includes conductive posts **134(*a*)** on the first side of the core structure **122** and conductive posts **134(*b*)** on the second side of the core structure **122**. The first plurality of conductive posts **134(*a*)**, **134(*b*)** are preferably formed on both sides of the core structure simultaneously. For example, the structure shown in **FIG. 40** can be placed in an electroplating bath. In the electroplating bath, conductive material can plate from the conductive regions **124(*a*)**, **124(*b*)** to the open ends of the apertures **132(*a*)**, **132(*b*)** to form a first plurality of conductive posts **134(*a*)**, **134(*b*)**.

[0137] Although the use of seed layers are described in detail with respect to the illustrated embodiments, seed layers need not be used in other embodiments. For example, the conductive regions **124(*a*)**, **124(*b*)** exposed through the photoresist layers **131(*a*)**, **131(*b*)** may be suitable to initiate the direct plating of posts within the apertures **132(*a*)**, **132(*b*)** of the photoresist layers **131(*a*)**, **131(*b*)**, without the need to deposit seed layers.

[0138] After the first plurality of conductive posts **134(*a*)**, **134(*b*)** are formed, the photoresist layers **131(*a*)**, **131(*b*)** which were used to form the conductive posts **134(*a*)**, **134(*b*)** can be removed (e.g., stripped) from the core structure **122**. As shown in **FIG. 42**, after the photoresist layers **131(*a*)**, **131(*b*)** are removed, the first plurality of conductive posts **134(*a*)**, **134(*b*)** are disposed on the core structure **122** and protrude from the surfaces of the core structure **122**.

[0139] After the photoresist layers **131(*a*)**, **131(*b*)** are removed, the seed layers **125(*a*)**, **125(*b*)**, if present, can also be removed. Preferably, the seed layers are etched in a flash etching process. In a typical flash etching process, the seed layers can be etched for a short period of time. After flash etching, the seed layers are completely removed from the dielectric layer surfaces, and an insubstantial portion of the formed conductive posts **134(*a*)**, **134(*b*)** may also be removed.

[0140] After the first plurality of conductive posts are formed on the core structure, dielectric layers may be deposited on the first and second sides of the core structure. The dielectric layers may include any suitable material including any suitable polymeric material. Exemplary dielectric layer materials include polyimide, epoxy-functional materials, and BT resins. Moreover, the dielectric layers may optionally include a filler. Preferable fillers can include particles such as silica or alumina particles, but may include chopped, woven, or non-woven fibers. Preferably, the dielectric layers are in the form of a preformed layer. Examples of preformed dielectric layers include ABF-SH9

film commercially available from Ajinomoto, Inc., and BT346 film commercially available from Mitsubishi Gas and Chemical, Inc. In addition, the dielectric layers are preferably non-photoimageable. Non-photoimageable dielectric materials typically have a higher glass transition temperature (Tg) and a lower moisture absorption rate than photoimageable dielectric layers. Consequently, multilayer circuit structures having non-photoimageable dielectric layers are generally more reliable than photoimageable dielectric layers.

[0141] The deposited dielectric layers may have any suitable thickness including a thickness of about 75 microns or less, preferably between about 25 to about 50 microns. The individual dielectric layers on the core structure may have the same or different thickness. Preferably, an individual dielectric layer can have a thickness which is less than or equal to the combined height of a post and pad upon which the post is disposed. For example, the thickness of a dielectric layer may be about 2 to about 8% less (e.g., 5% or less) than the combined height of a conductive post and a conductive pad upon which the conductive post is disposed.

[0142] The dielectric layers may be sequentially or simultaneously deposited onto opposite sides of the core structure. For example, a first dielectric layer can be deposited on a first side of a core structure by depositing a liquid dielectric material on the first side. The deposited liquid can then be softbaked to solidify the deposited layer, and can then be optionally cured. After the first dielectric layer is deposited, a second dielectric layer can be deposited on the second side of the core structure in the same or different manner as the first dielectric layer.

[0143] The dielectric layers may be deposited using any suitable process including spin coating, screen printing, slot coating, doctor blade coating, curtain coating, etc. These processes can be used to deposit liquid dielectric layers. Laminating can be used to deposit preformed dielectric layers. The dielectric layers may even be deposited by a gas-phase deposition process such as a chemical vapor deposition (CVD).

[0144] Preferably, the first and second dielectric layers are respectively laminated to the first and second sides of the core structure. In these embodiments, the dielectric layers may be preformed prior to being deposited on the core structure. By depositing a preformed dielectric layer onto the core structure, the thickness of the dielectric layer is substantially uniform when present on the core structure. In addition, by laminating preformed dielectric layers onto a core structure, dielectric layers on opposite sides of the core structure can be deposited simultaneously, thus providing for more efficient processing.

[0145] Preferably, a preformed dielectric layer is disposed on a carrier layer prior to being laminated to the core structure. The carrier layer may include any suitable polymeric material including polyethylene terephthalate. The preformed dielectric layer and the carrier layer may form a composite. Suitable composites are commercially available from Ajinomoto, Inc. (e.g., ABF-SH9). With reference to **FIG. 43**, composites **140(*a*)**, **140(*b*)** including a carrier layer **142(*a*)**, **142(*b*)** and a dielectric layer **141(*a*)**, **141(*b*)** are laminated to the first and second sides of the core structure **122**. The composites **140(*a*)**, **140(*b*)** are laminated to the core structure **122** so that the carrier layers **142(*a*)**, **142(*b*)** are disposed on the outer surfaces of the dielectric layers **141(*a*)**, **141(*b*)**. The composites **140(*a*)**, **140(*b*)** are preferably flexible and can be laminated to the core structure **122** simultaneously or sequentially.

[0146] The composites can be laminated to the core structure using any suitable apparatus. Heat and pressure can be applied to the dielectric layers to soften them so that they can conform to the surfaces to which they are laminated. The heating temperature and/or pressure can chosen in accordance with the particular material used for the dielectric layer. For example, a hot roll laminator can be used to laminate composites of this type onto opposing sides of the core structure simultaneously or sequentially. In some embodiments, the rolls of the hot roll laminator can be between about 60° C. to about 120° C. (preferably 80° C. to about 90° C.), and the rollers can run at a speed of about 1 to about 2 meters per minute. A vacuum laminator can also be used to laminate the dielectric layers or composites to the core structure. For example, using heat, the vacuum laminator can operate near vacuum (e.g., less than 1 atm) for a few minutes (e.g., 5 minutes or more). Alternatively, composites can be laid on opposite sides of a core structure, placed in a lamination press (e.g., a hydraulic press), and then laminated together. The lamination press can operate at a temperature of about 80° C. to about 90° C., and at a pressure of about 1 to about 3 kg/cm2 for a few minutes, (e.g., about 5 minutes or more). Regardless of the specific lamination apparatus used, after lamination, the dielectric layers may be disposed on opposite sides of the core structure and can be sandwiched between carrier layers.

[0147] After depositing the dielectric layers **141(*a*)**, **141(*b*)**, the dielectric layers **141(*a*)** may be optionally cured. The dielectric layers can be cured in any suitable manner. For example, an electron-beam, heat, and/or U-V radiation can be used to cure the dielectric layers. The dielectric layers are cured in a lamination press, or preferably an oven, using heat.

[0148] Release layers may be optionally disposed on the uncured dielectric layers prior to and/or during curing (e.g., in a lamination press). The release layers preferably include a heat resistant material. Exemplary release layer materials include Teddler™ paper (commercially available from du Pont), fluoropolymeric materials such as polytetrafluoroethylene (Teflon™), or metal (e.g., aluminum, copper). If the release layer is a copper foil, a shiny side of the foil is preferably in contact with the dielectric layer. In these embodiments, the previously described carrier layer (if used) may be optionally replaced with a release layer which has a higher melting temperature than the carrier layer. For example, the carrier layer can have a melting temperature less than 150° C. while the release layer can have a melting temperature greater than about 150° C.

[0149] With reference to FIGS. **43** to **45**, carrier layers **142(*a*)**, **142(*b*)** can be separated (e.g., peeled) from the first and second dielectric layers **141(*a*)**, **141(*b*)** after they are laminated to the core structure **122**. Then, release layers **151(*a*)**, **151(*b*)** can be deposited on the uncured first and second dielectric layers **141(*a*)**, **141(*b*)**. Preferably, the release layers **151(*a*)**, **151(*b*)** are laminated to the first and second dielectric layers **141(*a*)**, **141(*b*)**. Heat, and optionally pressure, are applied to the structure to cure the dielectric layers **141(*a*)**, **141(*b*)**. For example, the first and second

dielectric layers **141**(*a*), **141**(*b*) can be heated to a temperature of about 170° C. or more and can be subjected to a pressure of about 3.5 to about 20 kg/cm2 for about 60 minutes or more. The heat and pressure may be applied with a lamination press. After curing, the release layers **151**(*a*), **151**(*b*) can then be separated (e.g., by peeling) from the cured dielectric layers **141**(*a*), **141**(*b*).

[0150] In preferred embodiments, (with reference to **FIGS. 43 and 44**) an uncured dielectric layer on the core structure may be cured without the use of a release layer. For example, after laminating a carrier layer/dielectric layer composite to a core structure, the carrier layer can be removed from the dielectric layer. Then, the dielectric layer on the core structure can be cured.

[0151] In other embodiments, the dielectric layers can be partially cured and then conditioned (e.g., roughened) prior to complete curing. For instance, a precursor structure including a core structure and dielectric layers may be placed in an oven and baked for about 150° C. or more for about 30 minutes or less to partially cure the dielectric layers. Then, the outer surfaces of the dielectric layers may be roughened. For example, an etch process such as a permanganate etch process can be used to roughen the surfaces of a dielectric layer. After roughening, circuit patterns can be formed on the dielectric layer. The circuit patterns can include conductive pads disposed on the distal ends of the first plurality of conductive posts. The dielectric layers may then be baked again to fully cure them. For example, to fully cure the dielectric layers, the dielectric layers can be additionally heated at about 170° C. or more for about 60 to about 90 minutes, or more. Then, a second plurality of conductive posts can be formed on the conductive pads. Advantageously, by roughening the outer surfaces of the dielectric layers, any subsequently deposited seed layers or conductive layers can tightly adhere to the surfaces of the dielectric layers.

[0152] After the dielectric layers **141**(*a*), **141**(*b*) are deposited on the core structure **122**, dielectric layer material present on the distal ends of the first plurality of conductive posts **134**(*a*), **134**(*b*) can be removed to clean the post ends. In some embodiments, residual dielectric layer material can be present on the distal ends of the conductive posts after one or more dielectric layers are deposited on the core structure. For example, after laminating and curing, a dielectric layer on the conductive posts on the core structure, residual dielectric layer material can remain on the post ends. The residual dielectric material is typically 10 microns or less, and is often is about 2 to about 5 microns thick. After the post ends are cleaned, additional conductive posts can be subsequently formed on the first plurality of conductive pads and posts **134**(*a*), **134**(*b*). The formed conductive posts can be stacked and are electrically coupled together to form a generally vertical electrical pathway through one or more dielectric layers.

[0153] Any suitable process can be used to remove dielectric material from the distal ends of the conductive posts. Exemplary removal processes include etching processes such as a permanganate etch process, plasma etch process, or an abrading process such as mechanical polishing. In preferred embodiments, mechanical polishing can be used to remove the dielectric layer material. Mechanical polishing can be performed by using a polishing apparatus such as an oscillation deburrer. Oscillation deburrers are commercially available from Ishii Hyoki. The polishing apparatus can include buffing elements such as SiC and Al_2O_3 buffing wheels. In a typical operation, the revolution speed of the wheels can be about 2000 revolutions per minute (rpm) or more, and the oscillation cycle of the wheels is about 470 (cycles per minute) or more, and the oscillation stroke of the wheels is about 5 mm or more. The wheel pressure can be controlled automatically by preset pressure at a range of 0.25 to about 20 kg/cm^2. In other embodiments, the dielectric material on the distal ends of the conductive posts may be ablated. For example, a laser can be used to ablate the dielectric layer material from the ends of the conductive posts.

[0154] Optionally, protective layers may be used during the dielectric material removal process to protect the dielectric layer regions not disposed on the conductive posts. With reference to **FIG. 46**, protective layers **161**(*a*), **161**(*b*) can be disposed on the dielectric layers **141**(*a*), **141**(*b*). The apertures **162**(*a*), **162**(*b*) of the protective layers **161**(*a*), **161**(*b*) can be disposed over the distal ends of the conductive posts **134**(*a*), **134**(*b*). Dielectric layer material on the distal ends of the conductive posts are exposed through the protective layer apertures. By using a protective layer during the dielectric material removal process, the deposited dielectric layers are protected in the regions not disposed on the ends of the posts. Consequently, in these embodiments, unwanted dielectric layer material can be selectively removed. For example, a wide area laser can scan the outer surface of a protective layer disposed on a dielectric layer. The laser can ablate dielectric layer material exposed through apertures in the protective layer. Regardless of the particular removal process used, after removing the dielectric material from the ends of the conductive posts, the protective layers can be removed from the dielectric layers. For instance, the protective layers may be removed by etching or peeling.

[0155] The protective layers may deposited onto or formed on the previously deposited dielectric layers in any suitable manner. For example, in one embodiment, a layer of photoresist can be deposited, irradiated, and developed on a deposited dielectric layer to form a protective layer. In another embodiment, a protective layer with apertures is preformed, and is then laminated to a dielectric layer so that the distal ends of the posts (and any dielectric layer material thereon) are accessible through the apertures. The apertured protective layer may be the same as, derived from, or different from the previously described release or carrier layers.

[0156] In another example, apertures in the protective layers **161**(*a*), **161**(*b*) can be formed when the dielectric layer material is removed from the distal ends of the conductive posts. For example, a continuous protective layer can be laminated to a dielectric layer on a core structure. The dielectric layer material on the distal ends of the conductive posts may be ablated along with portions of the protective layer disposed on the distal ends. In this case, additional cleaning of the distal ends of the posts may not be needed after ablation and the formed apertured protective layer can simply be removed from the dielectric layers. Any residual material from the ablation process can remain on the outer surface of the formed protective layers and can be removed along with the protective layers. For example, any ash

generated by the ablation process can be removed along with the protective layers when the protective layers are peeled off of the dielectric layers.

[0157] After the dielectric layers are deposited, conductive patterns can be formed on the dielectric layers. This can be done before the second plurality of conductive posts are formed. The conductive patterns are preferably formed by an additive process such as electroplating. For example, with reference to **FIGS. 47 and 48**, after any carrier layers, release layers, or protective layers are removed (if used), seed layers **155**(*a*), **155**(*b*) may be deposited on the outer surfaces of the first and second dielectric layers **131**(*a*), **131**(*b*) and over the distal ends of the first plurality of conductive posts **134**(*b*), **134**(*b*). Prior to depositing the seed layers, the dielectric layer surfaces can be conditioned (e.g., roughened) in the same or different manner as described above for the core structure **122**. Then, photoresist layers may be deposited over the seed layers **155**(*a*), **155**(*b*), irradiated, and then developed to form patterned photoresist layers **161**(*a*), **161**(*b*). The photoresist layers **161**(*a*), **161**(*b*) may have the same or different characteristics as the previously described photoresist layers **131**(*a*), **131**(*b*). As shown in **FIG. 49**, the patterned photoresist layers **161**(*a*), **161**(*b*) can be disposed on the seed layers **155**(*a*), **155**(*b*).

[0158] With reference to **FIG. 50**, conductive patterns **156**(*a*), **156**(*b*) are then formed (e.g., by electroplating) on the portions of the seed layers not covered by the developed photoresist layers **161**(*a*), **161**(*b*). The conductive patterns are preferably made of the same material as the conductive posts. The thickness of the formed conductive patterns **156**(*a*), **156**(*b*) can be between about 5 to about 35 microns, preferably between about 10 and about 20 microns. After the conductive patterns **156**(*a*), **156**(*b*) are formed, the photoresist layers **161**(*a*), **161**(*b*) can be removed (e.g., by stripping) from the surfaces of the dielectric layers **131**(*a*), **131**(*b*).

[0159] The conductive patterns may include a number of pads **139**(*a*), **139**(*b*) which are disposed on the distal ends of the first plurality of conductive posts. The pads generally have a larger surface area than the diameter of the conductive posts upon which they are disposed. Typically, a pad is disposed between respectively stacked conductive posts and is in direct contact with the stacked conductive posts.

[0160] Then, a second plurality and any subsequent plurality of conductive posts, dielectric layers, and conductive patterns can be formed on the structure shown in **FIG. 51**, or any subsequent multilayer circuit structure precursor, by repeating one or more of the previously described steps. For example, the process used to form the second plurality of conductive posts can be the same or different process used to form the first plurality of conductive posts. Preferably, the first, second, and any subsequent plurality of posts are formed by electroplating. Once the conductive patterns **156**(*a*), **156**(*b*) and conductive posts are formed, any seed layers **155**(*a*), **155**(*b*) can be etched (e.g., by flash etching).

[0161] Any number of conductive patterns, conductive posts, and dielectric layers can be included in the formed multilayer circuit structure. For example, the multilayer circuit structure **170** shown in **FIG. 52** includes a circuitized core structure **122**, and three dielectric layers and three conductive layers on each side of the core structure **122**. The multilayer circuit structure **170** also includes generally vertical conductive pathways, each pathway including stacked conductive posts, with a pad between each adjacent pair of stacked posts. The generally vertical conductive pathways permit the size of the formed multilayer circuit structure to be reduced in comparison with a similar multilayer circuit structure with staggered via structures. Consequently, embodiments of the invention can be used to produce reliable, high density multilayer circuit structures efficiently and in a cost efficient manner.

[0162] After the multilayer circuit structure is formed, surface finishes or solder masks can be applied to the outer surfaces of the multilayer circuit structure. For example, a Ni/Au pad finish and/or a solder mask can be formed on the outer surfaces of a formed multilayer circuit structure. Accordingly, the multilayer circuit structures can be used in, for example, single chip modules, multichip modules and/or as mother or daughter boards in an electrical assembly.

[0163] Referring in detail now to FIGS. **53**-**65**B, there is seen in **FIG. 53** a multilayer laminated substrate, generally illustrated as **200**. The multilayer laminated substrate **200** includes conventional laminated substrates **202**, **204**, **206** and **208** which are electrically coupled together by aligned metal-filled interconnected vias, each generally illustrated as **210**. Any two contiguous laminated substrates are separated by a bonding sheet **212**, such as bonding sheets **212***a*, **212***b* and **212***c*.

[0164] Referring now to FIGS. **54**-**57**, there is seen in **FIG. 54** a conventional laminated substrate **202** (e.g., fiberglass reinforced laminate) having a copper layer **214** disposed on an underside thereof. Subsequently, blind vias **216***a*, **216***b* and **216***c* are laser drilled down to copper layer **214** by any conventional means, such as by CO_2, U-Yag or eximer laser. The CO_2 laser is preferred since it is easy to drill through a fiber glass reinforced laminate and the drilling speed is much faster than others. Subsequently, and as shown in **FIG. 56**, the blind vias **216***a*, **216***b* and **216***c* are respectively filled with copper **218***a*, **218***b* and **218***c*, by any conventional manner. Due to plating non-uniformity (typically 10%), slightly over plating is necessary to make sure that every blind via **216***a*, **216***b* and **216***c* is filled up or above the top surface of laminated substrate **202**. After plating, buff polishing of surface is applied to remove excess plating and flatten copper-filled blind vias by a deburr machine, such as Ishii Hyoki's oscillation deburrer. After the blind vias **216***a*, **216***b* and **216***c* have been copper-filled, and preferably subsequently buffed, a solder bump **220** is deposited on each of the copper-filled blind vias **216***a*, **216***b* and **216***c*.

[0165] In one embodiment of the invention and as best shown in **FIG. 57**B, one or more solder bumps **220** may comprise three (3) separate superimposed solder layers **220***a*, **220***b* and **220***c*. In another embodiment of the invention and as best shown in **FIG. 57**C, one or more solder bumps **220** may comprise two (2) separate superimposed solder layers (e.g., solder layers **220***a* and **220***b*) on one substrate and a single solder layer (e.g., solder layer **220***c*) on a second substrate. Thus, two superimposed solder layers may be disposed on one substrate (e.g., substrate **220***a*), while a single layer may be disposed on another substrate (e.g., substrate **220***b*).

[0166] The material for the solder layer(s) **220** comprises a conductive composition which may include pure metals, metal alloys, metal alloy precursors, metallic compositions,

metallic compounds, and combinations thereof. For example, the conductive composition can include one or more materials selected from the group consisting of In, Sn, Bi, Sb, Pb, Ni, Zn, Cu, Cd, Pt, Pd, Au and Ag.

[0167] Preferably, the conductive composition includes soft solder materials which can readily deform when pressed, thus providing for good areal contact between conducting surfaces. For instance, deforming the conductive compositions against conductive surface can increase the contact area with the support area. Suitable examples of solder compositions can include metals, or single or multi-phase alloys. The alloys may be binary, ternary, or other higher order compositions. Examples include alloys comprising In—Sn, Bi—Sn, In—Ag, Sn—Sb, Au—Sn, and Pb—Sn. More specific examples of solder material combinations include 52In/48Sn, 58Bi/42Sn, 97In/3Ag, In, 37Pb/63Sn, 96.5Sn/3.5Ag, 95Sn/5Sb, 80Au/20Sn, and 90Pb/10Sn (described in terms of weight percentages). More specifically and in a preferred embodiment of the invention, when the solder layer(s) **220** comprises three (3) superimposed layers (e.g., solder layers **220***a*, **220***b* and **220***c*), the conductive composition comprises the following elements of Table II (numbers representing weight percentages):

TABLE II

	Approach I	Approach II
Solder Layer 220a	2–5 um of eutectic solder: 37 Pb/63 Sn or 40 Pb/60 Sn	2–5 um of Sn
Solder Layer 220b	10–20 um of high lead solder: 90–97 Pb/3–10 Sn	10–20 um of Ag
Solder Layer 220c	2–5 um of eutectic solder: 37 Pb/63 Sn or 40 Pb/60 Sn	2–5 um of Sn

[0168] In the embodiment of the invention illustrated in **FIG. 57C**, solder layers **220***a* and **220***b* may respectively include the conductive composition set forth in Table II above for solder layers **220***a* and **220***b*. If a single solder layer, such as solder layer **220***c*, is to be employed on a separate first substrate (e.g., substrate **202**) while another or second substrate (e.g., substrate **204**) supports two (2) superimposed solder layers (such as solder layers **220***a* and **220***b*), the single solder layer (i.e., solder layer **220***c*) may comprise the conductive composition set forth in Table II above for solder layer **220***c*.

[0169] Referring now to FIGS. **58A-63A**, photoresist **224** is disposed on at least one side, more preferably photoresist **224** is disposed on two opposing sides and is patterned over copper layer **214** which is subsequently etched. Either dry film or liquid photoresist may be used. Photoresist **224** is stripped, and then a dielectric polymer bonding film (e.g., bonding sheet **212***a*), and a release layer **226** coupled or attached thereto, is secured or tacked in any conventional manner to the exposed top side of the laminated substrate **202**, as best shown in **FIG. 60A**. Tacking may be accomplished by lamination. During the lamination, the bonding film or sheet (such as Ajinomoto bonding film) is heated to its maximum flow rate temperature (e.g., 80-90° C.) without curing it so that the solder bumps **220** can easily pierce or pass through it. Alternatively, a liquid polymer may be substituted for the bonding film. The liquid polymer may be coated on by screen printing, curtain coating or spray coating. The release layer **226** is then removed or stripped from the bonding film (i.e., bonding sheet **212***a* in **FIG. 61A**).

[0170] A plurality of the formed substrate assembly of **FIG. 61A** may be produced with laminated substrates **202**, **204**, **206** and **208**, then aligned as shown in **FIG. 62A**, and subsequently laminated together by any conventional means to make intermetallic joints and the multilayer laminated substrate **200** (see **FIGS. 53 and 63A**). More specifically, a plurality of the formed substrate assembly of **FIG. 61A** may be interconnected by lamination to make the intermetallic joint and to cure bonding film, such as bonding film **212***a*. First, the substrate, such as substrate **202**, will be heated slightly higher than the solder layers (i.e., solder layers **220***a* and **220***c*) melting temperature (e.g., 185-230° C. for the eutectic solder of Approach I in Table II above and 235-250° C. for the Sn of Approach II in Table II above). It is well known that the melting temperature of lead (e.g., 300° C. to 325° C.) is higher than the melting temperature of tin (e.g., about 260° C.), and the melting temperature of gold (e.g., about 900° C.) is higher than that of lead. Thus, preferably the melting temperature for solder layers **220***a* and **220***c* is lower than the melting temperature for solder layer **220***b*. The solder compositions(s) of the solder layers will melt and fuse together to make the intermetallic joint. At the same time, the solder layers **220***a* and **220***c* and solder layer **220***b* will comingle and/or diffuse into each other and raise the melting temperature of the whole intermetallic joint. Finally, the joint will be "frizzed" at much higher temperature than the melting temperature of solder layers **220***a* and **220***c* (i.e., a "frizze" temperature of about 260-300° C. for Approach I in Table II and >300° C., such as 310-500° C., for Approach II in Table II) and higher than the melting temperature of solder layer **220***b* to further comingle and diffuse the solder layers into each other. Then, the temperature is reduced to the curing temperature (e.g., 95-140° C.) of the bonding film (e.g., bonding film **212***a*) to cure the bonding film, such as bonding film **212***a*. It should be readily apparent that the two opposed substrates **202** and **208** of the alignment of **FIG. 62A** are rotated 180 degrees to align copper **218***c* in via **216***c* of one substrate (e.g., substrate **208**) with copper **218***a* in via **216***a* of a contiguous substrate (e.g. substrate **206**).

[0171] Referring now to FIGS. **58B-65B**, there is seen a sequential process by which an initially pair of substrates (e.g., substrates **202** and **204** in **FIGS. 60B and 61B**) are laminated together as previously indicated to produce the substrate assembly of **FIG. 61B**. Subsequently, the exposed copper layers **214-214** are patterned with photoresist **224-224**. Bonding sheets **212***c* and **212***b* are then disposed on the patterned copper layers **214-214** in accordance with the previously indicated procedure. Substrates **206** and **208** with associated copper fillings (i.e., copper fillings **218***a*, **218***b*, and **218***c*) and copper layers **214-214** are produced in accordance with the previously mentioned procedure, and subsequently coupled to the substrate assembly of **FIG. 63B** through lamination on the bonding sheets **212***b* and 212*c*, as previously indicated. The exposed copper layers **214-214** are then patterned with the assistance of photoresist **224-224**. By performing the foregoing procedure the solder layers **220** will not be exposed to lithographic patterning process.

[0172] The embodiments of the invention of FIGS. **53-65B** has many advantages over conventional plated

through hole (PTH) vias. For example, embodiments of the present invention enable the production of much smaller (50-150 um vs. >200 um in diameter) vias so that the density is much higher. For L/D (laminated core+build-up deposited layer) package substrate application, the via of laminated core has to be filled before any deposited layer can be build up on top. Embodiments of the present invention has automatically filled vias so that no extra process steps are needed. For conventional plated through hole vias, the center hole of the plated vias have to be filled after via plating (forming). The typical filling material is a suitable liquid polymer (e.g., epoxy). Since the coefficient of thermal expansion (CTE) of typical polymer filler is much higher, it will generate reliability problem. For solving this problem, a copper capping layer is plated usually after via filling to "cap" the filler inside the via, but this way increases total thickness of copper before patterning so that the subtractive patterning resolution decreases. Embodiments of the present invention provide stack via structures to save the space. As previously mentioned embodiments of the present invention can make "frizzed" solder joints so that the solder joints can easily survive from further chip assembly processing, such as solder reflow to mount chips on a substrate.

[0173] Referring now to FIGS. **66-87** for additional embodiments of the present invention. There is seen in **FIG. 66** a broad illustration of a de-plating process to remove metal **310** pads (e.g., copper pads) connected to defective capacitors **320***b* with shorts (or high leakage) to a substrate **300**. Broadly, mask design opens resist over the entire metal **310** capacitor pads, or only the trace leading to the pad. Breaking the capacitor into many small capacitors, allows the isolation (de-plating) of defects without large reductions in capacitiance. There is more specifically illustrated in **FIG. 66**, substrate **300** supporting field oxide layers **302**, a good capacitor **320***a* including gate oxide **306***a* without a short and a layer of polysilicon metal **312**, a defective capacitor **320***b* including gate oxide **306***b* with a short **307** and a layer of polysilicon metal **312**, and a passivation layer **308** providing the appropriate isolation. Resist **324** may be conveniently disposed as illustrated. Mask design opens resists **324** over all metal **310** capacitor pads.

[0174] Deplating of defective capacitor **320***b* may be accomplished by any suitable means, such as by a conventional plating fixture. Water is placed in a plating fixture, followed by adding a plating solution to the water. The plating bias is the reverse of that used to plate copper, i.e., a negative voltage is applied to the back of wafer and a positive voltage is applied to the solution. Plating solution can be copper sulfate, sulfuric acid, and additives. Contact to the backs of the wafer may be from the frontside, metal **310** pads to metal **312** to the silicon. Wet etch is performed with the assistance of resist **320**. The deplating procedure is followed with Cu etch to remove residue, and then the adhesion layer is etched to remove any exposed adhesion layer. Resist **324** may be conveniently stripped.

[0175] Referring now to **FIG. 67** there is illustrated a substrate assembly produced by the following semiconductor manufacturing process: nitride deposition on substrate **300**, field oxide **302** (MASK 1) deposition, followed by nitride etch, field oxidation (1 um), nitride stripe, and gate oxidation (10 nm). A contact mask (MASK 2) is then deposited, followed by oxide etch, polysilicon deposit **312** and metal deposit. MASK 3 is deposited for etching metal **312**, followed by aluminum etch, polysicon etch, and passivation layer **308** deposition. Pad mask (MASK 4) is disposed conveniently, followed by passivation etch, TiCu deposition, metal **310** mask (MASK 5), patterning metal **310**, de-plating MASK (MASK 6) placement, de-plating defective capacitors **320***b*, and polyimide coat **330** deposition.

[0176] Referring now to **FIG. 68**, there is seen a MCM assembly **360** formed by producing the assembly of **FIG. 67**, followed by the following procedures: depositing metal layer **334**, then depositing dielectric layer **336**, and subsequently depositing metal layer **338** on the dielectric layer **336** and forming metal pads **342** and dielectric layers **340**. From the MCM assembly **360** of **FIG. 68**, through via formation is conducted by the following steps: backgrind wafer or substrate **300** to 200 u, backside silicon nitride passivation (0.2 u), deposit adhesive **350**, mount temporary carrier **350**, form through via (MASK 7) in substrate, plasma etch nitride, KOH etch through wafer (stop on field oxide **302**), plasma etch oxide **302** down to polysilicon **312**, vapor deposit parylene **370** (20 u), laser via in parylene **370**, and plasma clean via CrCu seed deposition. Subsequently, via pad is deposited in contact with polysilicon metal **312** (MASK 8) using laminated resist, followed by Cu plate **380** (10 u) formation, seed etch, and eless Ni/Au plating.

[0177] Referring now to **FIG. 70** for illustration of a process for forming support substrate attachment, the assembly of **FIG. 69** is diced to size. Adhesive layer **384** is tacked to ceramic substrate **388** having vias **381**. The adhesive layer **384** over the copper plating **380** is removed by using the ceramic substrate **388** including vias **381** as a laser mask to remove the appropriate amount of adhesive layer **384**. The ceramic substrate **388** is subsequently laminated to parylene layer **370** supported by substrate **300**. Subsequently, paste **390** (e.g., SnAg) is screened into the vias **381**, and then SnAg solder balls are placed to increase volume and reflow. In an alternate embodiment and as best shown in **FIG. 71**, the assembly of **FIG. 70** includes CPU **398** mounted to pads **342** of the assembly of **FIG. 70** through solder (e.g., AuSn) **394**.

[0178] Referring now to FIGS. **76-87**, there is seen an exemplary multichip module with capacitor structures, generally illustrated as **410** in **FIG. 76**. To simplify the visual presentation of module **410**, only a cross-sectional slice of the module is shown in the Figures, with it being understood that additional portions of the module lie to the left of the left straight edge of the slice and to the right of the right straight edge of the slice. Substrate **410** comprises a primary substrate **411** which is affixed to a secondary substrate **470** by an adhesive layer **480**. Primary substrate **411** preferably comprises a silicon wafer, and secondary substrate **470** preferably comprises a ceramic substrate. Adhesive layer **480** may comprise a bonding sheet (also called a bonding film), and examples thereof are described in greater detail below. Several dielectric and conductive layers are formed on top of primary substrate **411**, ending with a plurality of conductive interconnect pads **461** at the top of module **410**. Among other purposes, some of the pads **461** are used to interconnect to one or more integrated circuit chips **442**, each of which has a plurality of corresponding interconnect pads **443**. The interconnection of the pads **461** and **443** is

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preferably made by way of a plurality of reflowed solder bumps **445**, such an may be formed in a conventional flip-chip bounding process.

[0179] One aspect of the present application is provided by a plurality of high-value capacitance structures, each of which comprises a conductive (e.g., doped) region **412** of primary substrate **411**, an ultra-thin dielectric layer **414** (which preferably comprises silicon oxide) formed over a portion of conductive region **412**, a first conductive layer **421** formed over the dielectric layer **414**, a second dielectric layer **425** formed over the first conductive layer **421** with at least one aperture **422** therein and formed over the layer **421**, a body **432** of a conductive material filled within each aperture **422**, and a second conductive layer **431** formed over second dielectric layer **425** and electrically contacting body **432** of conductive material. After the first and second conductive layers **421** and **431** are formed, capacitance structures which have defective dielectric layers **414** (such as caused by pin holes formed through the layer) are detected by a de-plating process according to the present invention and their second conductive layers **431** are removed by the de-plating process. A bypass-capacitor is then constructed from non-defective capacitance structures by coupling a third conductive layer **441A** to selected ones of the conductive layers **431** which remain after the de-plating process. Third conductive layer **441A** is then coupled to an interconnect pad **461A** directly or by an intervening layer **451A** of conductive material, the latter being shown in **FIG. 76**.

[0180] Conductive region **412** of primary substrate **411** serves as a common bottom electrode for two or more capacitor structures according to the present invention, and preferably comprises a heavily doped N+type layer formed at the top surface of substrate **411**, such as that made by diffusion or ion implantation, and more preferably comprises the entire substrate **411** doped with n-type impurities to have a relatively low bulk resistivity of 0.01 ohm-cm. A bulk doping level of 5×10^{-18} n-type impurities per cubic centimeter (5×10^{-18} cm^{-3}) can be used to achieve this level of resistivity. In general, the bulk resistivity for this implementation of regions **412** should be at or above 0.002 ohm-cm, corresponding to a doping level of 1×10^{-8} cm^{-3} and above.

[0181] Thin dielectric layer **414** preferably comprises silicon dioxide and has a thickness of around 10 nm. A range of thickness of between 7 nm and 20 nm may be used. Such thin dielectric layers are susceptible to the formation of pin holes through the dielectric layer, which can cause a short circuit across the capacitor's electrodes. As described below, the present invention addresses this problem by coupling two or more capacitor structures together in order to provide a composite bypass capacitor, and includes a selective de-plating process during manufacturing which automatically detects the presence of pin holes in the thin dielectric layer **414** and de-plates the second conductive layer **431** of the defective capacitor structure. In order to reduce the potential of edge leakage currents around the periphery of each thin dielectric layer, and thereby to improve the reliability of the capacitor structure, each thin dielectric layer **414** is preferably surrounded by a thicker layer **415** of silicon dioxide **415**, oftentimes called the "field" oxide layer.

[0182] First conductive layer **421** preferably comprises a first sub-layer of n-type conductive polysilicon, which contacts the thin dielectric layer **414**, and a second sub-layer of aluminum. The sub-layers may be relatively thick with respect to thin dielectric layer, such as on the order of 0.25 μm to 1 μm in thickness. Second dielectric layer **425** may comprise a number of suitable dielectric materials, such as polyimide or deposited silicon dioxide, and also has a thickness which is preferably greater than that of layer **414**, such as a thickness in the range of 2 μm to 10 μm. Aperture **422** within second dielectric layer **425** is preferably filled with a body **432** (i.e., via) of conductive material which is different from the material of the top sub-layer of first conductive layer **421**, and/or which is different from the material at the bottom of second conductive layer **431**. This difference enables the de-plating process according to the present invention to remove the second conductive layer **431** without removing first conductive layer **421** when it is found that the thin dielectric layer **414** is defective. Second conductive material **431** comprises a metal which can be readily de-plated, such as copper.

[0183] In preferred embodiments of the present invention, the above requirements for via body **432** are met by a construction of second conductive layer **431** which comprises a first sub-layer of titanium and a second sub-layer of copper, with the second sub-layer having a greater thickness than that of the first sub-layer. The first sub-layer is deposited after aperture **422** has been formed in second dielectric layer **425**, thereby at least partially filling aperture **422** with a material which is different from the top sub-layer of first layer **421** (e.g., aluminum), as well as covering the top portions of second dielectric layer **425**. The second sub-layer of copper provides a metal which can be readily de-plated, and is different from both the sub-layer of titanium at the bottom of aperture **422** and the aluminum sub-layer of first conductive layer **421**.

[0184] Another feature of the present invention is the provision of large-diameter vias **490** at the bottom side of module **410** which provide low-inductance pathways for current to flow to and from the capacitance structures on module **410**, as well as to and from other components on module **410**. Vias **490** are formed through the top and bottom surfaces of secondary substrate **470**, further through the top and bottom surfaces of adhesive layer **480**, and further through the bottom surface of primary substrate **411** up to near the top surface of substrate **411**, where each via **490** contacts a respective conductive backside contact **467**. Each backside contact **467** is conductively isolated from primary substrate **411** by a dielectric passivation layer **465**, and is electrically coupled to a respective instance **421C** and **421D** of first conductive layer **421**. Each backside contact **467** mechanically couples its respective via **490** to primary substrate **411**, and electrically couples its respective via **490** to a conductive layer **421C**, **421D**. A via may be configured to provide a power supply voltage to module **410**, to provide a ground potential to module **410**, to convey an input signal (e.g., data signal, clock signal, etc.) to module **410**, or to convey an output signal from module **410**. While only two vias **490** and two backside contacts **467** are shown in the figures for visual simplicity, it may be appreciated that module **410** may comprise hundreds to thousands of vias **490** and corresponding backside contacts.

[0185] Each via **490** is preferably formed through an aperture **472** in secondary substrate **470**, and preferably mechanically coupled to substrate **470** by a metal layer **474**

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formed and adhered to the inside surface of aperture **472**. Each metal layer **474** preferably extends outside of its aperture to a top or bottom surface of secondary substrate **470**, where power, ground, or electrical signals may be coupled to it.

[0186] In **FIG. 76**, the via **490** shown on the right of the figure is configured to provide a ground potential to conductive region **420** of primary substrate **411**. The backside contact **467** that is coupled to this via **490** is, in turn, electrically coupled to a respective first conductive layer **421D**. In turn, layer **421D** is electrically coupled to an ohmic contact **418** formed on a portion of doped region **412** (e.g., an ohmic contact to a spot on the top surface of primary substrate **411**). Thus, the via **490** shown at the right of the figure is electrically coupled to the common bottom electrode (i.e., doped region **412**) of all the capacitor structures. Ohmic contact **418** may be formed in a number of ways. As one example, n-type polysilicon may be deposited onto portion of doped region **412**. This is, in fact, done as a matter of course when the first conductive layer **421** (and its instances **421C** and **421D**) comprise a bottom sub-layer of n-type polysilicon and a top sub-layer of aluminum. An ohmic contact may also be formed by depositing aluminum directly onto a portion of doped region **412**, or by depositing a 10%-90% alloy of titanium-tungsten (Ti—W) on top of a portion of doped region **412**, followed by depositing aluminum on top of this alloy. The use of n-doped polysilicon or the use of the titanium-tungsten alloy are preferred over the direct deposit of aluminum over the portion of doped region **412**.

[0187] Also in **FIG. 76**, the via **490** shown on the left is configured to provide an electrical signal from conductive layer **421C** to a contact pad **461C** through a series of intervening conductive layers **431C**, **441C**, and **451C**, which are electrically coupled to one another, with layer **431C** being electrically coupled to layer **421C** and layer **451C** being electrically coupled to layer **461C**. However, the left via **490** may also be configured to provide a power voltage to third conductive layer **441**, which couples the second layers **431** (i.e., the top electrodes) of one or more capacitor structures together. This may be accomplished by including a bridge **443B** of conductive material between conductive layers **441C** and **441A**, which is shown in dashed lines in the figure. This configuration provides a low-impedance source of power voltage to the top electrodes of the capacitance structures.

[0188] We note that, for the purposes of visual clarity, the vertical thicknesses of conductive layers **421**, **431**, **441**, **451**, and **461** and dielectric layers **414**, **425**, **435**, **445**, and **455** have been enlarged with respect to the vertical thicknesses of substrate **411** and **470**. For the same reason, the vertical thicknesses of layers **465** and **480**, and of contacts **467** have also been enlarged.

[0189] Having generally described an exemplary module according to embodiment of the present invention, we now turn to describing exemplary methods of constructing modules according to the present invention. First we will describe exemplary methods of constructing primary substrate **411** and the various elements disposed above, and then we will describe exemplary methods for constructing vias **490**.

[0190] Referring to **FIG. 77**, an exemplary method according to the present invention begins with silicon substrate **411'** having a crystal orientation of <1, 0, 0>, and a thickness of 500 μm to 675 μm. The substrate may be uniformly doped with n-type dopant at a concentration of 1×10^{16} dopant atoms per cubic centimeter (cm^{-3}) or more as one example, or may comprises a silicon substrate which has a top surface that has had dopant implanted or diffused into it to create a conductive region **412** at the top surface as another example. In the first example, a bulk doping of 1×10^{18} dopant atoms per cm^{-3} is preferred to provide a bulk resistivity of 0.01 ohm-cm. In the second example, the level of doping in the doped layer and the depth of the doped layer are selected to provide an equivalent surface resistance as found in the former case. Various combinations of thickness and dopant levels are possible, and it is well within the skill of one of ordinary skill in the art to select one such combination.

[0191] Next, the layers **414** of ultra-thin dielectric material for the capacitance structures are defined. We show here a preferred approach which reduces peripheral leakage current by defining the layers **414** within regions **415** of a thicker field oxide. In this preferred approach, a mask layer **514** comprising silicon nitride is deposited and patterned to act as an oxidation mask in a subsequent first oxidation step. The patterning may be accomplished by photo-lithographic and etching processes that are well-known in the semiconductor fabrication art. Substrate **411'** will be subsequently oxidized to form field oxide regions **415A**, **415C**, and **415D** at those locations where silicon nitride layer **514** has been removed. The portions of mask layer **514** which are retained on the surface of substrate **411'** are indicated in the figure at reference numbers **514A** and **514B**. Dielectric layers **414** will be subsequently formed at layer portions **514A** and **514B**. Accordingly then, with mask layer **514** formed and patterned, silicon substrate **411'** is exposed to an oxidation step to form field oxide regions **415A-415D** by oxidizing the portions of substrate **411'** which are not covered by mask layer **514** to silicon dioxide. The oxidatation step is performed such that the field oxide preferably has a thickness of approximately 1 μm. As is well known in the semiconductor fabrication art, a wide range of combinations of oxidation temperature and oxidation time may be used to accomplish the preferred thickness, and it is readily within the skill of one of ordinary skill in the art to select one such combination.

[0192] Next, mask layers **514A** and **514B** are removed from the surface of substrate **411'**, and silicon substrate **411'** is again exposed to an oxidation step to form thin dielectric layers **414** of silicon dioxide with thicknesses of approximately 10 nm, which is equivalent to 100 Angstroms. The resulting structure is shown in **FIG. 78**. As is well known in the semiconductor fabrication art, a wide range of combinations of oxidation temperature and oxidation time may be used to accomplish the preferred thickness, and it is readily within the skill of one of ordinary skill in the art to select one such combination. This oxidation step adds less than 10 μm of thickness to field oxide layers **415A-415D**. With this approach, a smooth transition from the thin oxide layer **414** to the field oxide layer **415** is achieved at the peripheral edge of thin oxide layer, which reduces the chances of pin holes and leakage current at the peripheral edge.

[0193] As the next general step in the exemplary method according to the present invention, ohmic contacts **418**, the first conductive layers **421**, the second conductive layers

431, and the intervening dielectric layer 425 are formed. A preferred way of accomplishing this is disclosed herein which enables the interconnection of the first conductive layers with the backside vias 490 and enables the detection of defective oxide layers 414. The preferred approach starts by defining windows in the field oxide layer 415 for the locations of ohmic contacts 418. This may be accomplished by forming a layer of photo-resist over layer 415, patterning the photo-resist layer by conventional photo-lithographic methods to remove portions in the photo-resist layer which overlie the locations where the windows in layer 415 are to be made, and thereafter etching the exposed portions of layer 415 with a chemical etchant to form the windows. The results of these steps are shown in FIG. 79 (with the photo-resist layer removed), where the windows in oxide layer 415 is shown by reference number 515C.

[0194] Next, conductive layer 421 is formed by depositing a first sub-layer of N+doped polysilicon over the top surface of the substrate structure shown in FIG. 79, and thereafter depositing a sub-layer of aluminum over the sub-layer of polysilicon. Each of these steps, separately by itself, is well-known to the semiconductor fabrication art, and it is within the skill of one of ordinary skill in that art to perform each of these steps. An inventive feature provided by the present application is the particular sequence of these steps. The deposition of the N+ polysilicon layer at windows 515C creates ohmic contacts at the interface between the polysilicon and substrate 411'. Thereafter, the particular regions, or instances, 421A-421D of first conductive layer 421 are formed by conventional photo-lithographic and etching methods. For example, a photo-resist layer is formed over the wholly formed layer 421 and then patterned to expose portions of the wholly formed layer 421, followed by etching the exposed aluminum with an aluminum etchant to remove the aluminum and to expose the underlying portions of polysilicon, and thereafter etching the exposed polysilicon portions with a polysilicon etchant to remove them to finally define the instances 421A-421D. As another example, a conventional lift-off technique can be used. The reader may refer ahead to FIG. 80 to see the resulting patterned layer 421.

[0195] The next steps in the preferred method comprise forming second dielectric layer 425, forming apertures 422 in dielectric layer 425, and thereafter depositing second conductive layer 431, which fills each aperture 422 with a body of conductive material. Dielectric layer 425 may comprise any number of dielectric materials, including CVD deposited glasses such as phosphosilicate (PSG) glasses, borophosphosilicate (BPSG) glasses, TEOS glasses (tetraethyloxysilane), deposited silicon nitrides, polyimides, and other polymer dielectrics. At present polyimides and deposited glasses are preferred. Apertures 422 may be formed by conventional photo-lithographic and etching steps. In additionally, some polymeric dielectrics are photoimageable, and apertures can be defined by direct pattern exposure of the dielectric material to actinic radiation followed by exposure to the material's developer. Next, the bodies 432 of conductive material and second conductive layer 431 are formed. The types of material deposited for bodies 432 and conductive layer 431 are selected according to the previously described criterion, namely that the material at the bottom of each body 432 be different from the material at the top of first conductive layer 421 and/or different from the material at the bottom of second conductive layer 431. To accomplish this, the inventors' preferred approach is to form bodies 432 and second conductive layer 431 at the same time by depositing conductive layer 431 as a first sub-layer titanium (Ti) and a second sub-layer of copper (Cu), with the titanium sub-layer being deposited first to fill the bottom of each aperture 422 and to served as the bottom portion of each conductive body 432. Second conductive layer 431 is then patterned by conventional photo-lithographic and etch methods. The resulting structure is shown in FIG. 80.

[0196] At this stage, two capacitance structures according to the present invention are shown in FIG. 80. The first such structure comprises common conductive region 412, thin dielectric layer 414A bordered by thick field oxide instances 415A and 415C, first conductive layer instance 421A, and second conductive layer instance 431A. The second capacitance structure comprises common conductive region 412, thin dielectric layer 414B bordered by thick field oxide instances 415C and 415D, first conductive layer instance 421B, and second conductive layer instance 431B.

[0197] The next general step in the exemplary methods according to the present invention is to expose the instances of conductive layer 431 to a de-plating process with a de-plating voltage (i.e., anode voltage) being applied to conductive region 412, and a plating voltage (i.e., cathode voltage) being applied to the anodic bar. The de-plating process can use any conventional electrolytic plating solution. With conductive layer 431 comprising a top copper sub-layer, the plating solution comprises a copper electrolytic plating solution and the anodic bar comprises copper, but with a cathodic potential applied to it. When the instances of conductive layer 431 are exposed to the plating solution with the de-plating voltage applied to region 412, the de-plating voltage will couple through any defective dielectric layer 414A, 414B and onto the overlying instances of conductive layers 421 and 431. Therefore, an instance of conductive layer 431 which overlies a defective layer 414A, 414B will have the de-plating voltage applied to it, and will have its copper sub-layer de-plated. As an example, we assume that dielectric layer 414B has a pin hole which makes it defective. In this case, the copper sub-layer of conductive layer instance 431B is de-plated, as shown in FIG. 81 by the dash-lines which show the outline of its copper sub-layer. The endpoint of the de-plating process may be detected by a substantial drop in the de-plating current. Alternatively, one may use a pre-set time period which has a sufficient duration to ensure that all of the copper sub-layer is removed. Prior to the de-plating step, the top surface of the substrate is preferably covered with a photo-resist mask which is subsequently developed to uncover only those portions (instances) of layer 431 which are electrically coupled to a second layer instance 421 of a capacitance structure. This mask protects the other portions of the substrate from the acid which is typically present in electrolytic plating solutions. The photo-resist mask is removed (stripped) after the de-plating step.

[0198] After the de-plating step, the titanium sub-layer of layer instance 431B may then be removed by suitable chemical etchant which preferably does not etch first conductive layer 421 or dielectric layer 425. When dielectric layer 425 comprises a deposited glass and first conductive layer 421 comprises aluminum, suitable titanium etchants are hydrogen chloride (HCl) aqua regia ($HCl+HNO_3$), and ntric acid (HNO_3). When dielectric layer 425 comprises a

polyimide material, one may use these etchants, as well as hydrofluoric acid (HF) and a combination of hydrofluoric and nitric acids.

[0199] The above described process enables the removal of the instance **431B** of second conductive layer **431** that overlies a defective dielectric layer **414B** without removing the underlying instance **421B** of the first conductive layer **421**, as shown in **FIG. 82**. The preservation of the instance **421B** of first conductive layer **421** in this manner improves the planarity of the subsequently formed layers **435**, **441**, **445**, **451**, and **455**, and prevents dielectric layer **425** from caving in during subsequent processing steps.

[0200] The remaining layers of module **10** may then be formed, as shown in **FIG. 83**. Here it is seen that the instance **441A** of third conductive layer **441** has a vertical portion which contacts instance **431A** of second conductive layer (part of the good capacitance structure), and also has a vertical portion which would have contacted instance **431B**, but instead terminates on the top surface of second dielectric layer **425**. This prevents the instance **421B** of first conductive layer from being electrically coupled to pad **461A** at the top surface of the substrate.

[0201] We now describe the formation of vias **490**. First, substrate **411'** is back lapped at its bottom surface to reduce its thickness to a value of around 200 μm. For reasons explained below, this step will enable the present invention to achieve a high density of vias **490**. The lapped bottom surface is then coated with a 0.2 μm thick passivation layer **520** which comprises silicon nitride. The resulting substrate is designed with reference number **411**, and is thereafter mounted to a temporary support substrate **611** because the thinned substrate **411** is fragile. The result of these steps is shown in **FIG. 84**. Temporary substrate **611** may be attached to substrate **411** by a layer **612** of temporary adhesive which can be later removed with an organic solvent. In addition, the temporary substrate attachment processes described in U.S. Pat. No. 5,258,236 to Arjavlingam, et al. may be used.

[0202] The next set of processing steps are as follows, with **FIG. 85** showing the final result of these steps. A window **522** is plasma etched in silicon nitride layer **520** at each location where a backside contact **467** is to be made. Substrate **411** is then subjected to a hot potassium hydroxide (KOH) etchant, which etches the portion of silicon substrate **411** behind each window **522**. This etch is performed until the etchant reaches portions of the undersides of field oxide regions **415A** and **415D** which are opposite to windows **522**. The KOH etchant preferentially etches the **(500)** plane of the silicon crystal structure with respect to the **(510)** and **(511)** planes, and therefore creates side edges that slope at 54.7 degrees. To form a widow of width W at the underside of field oxide region **415A** or **415D**, the corresponding window **522** is selected to have a width of $W+2\cdot d\cdot\cot(54.7°)=W+1.42\cdot d$, where d is the thickness of substrate **411** (after lapping). By back lapping substrate **411'** to produce substrate **411**, the value of d is reduced by 60% to 70%, which significantly reduces the width of window **522**, which in turn enables one to form more windows **522** and corresponding vias **490** over a given area of the substrate **411**. As the next step, mask layer **520** is then removed (as shown by dashed lines in **FIG. 85**), and the newly exposed portions of the undersides of field oxide regions **415A** and **415D** are plasma etched (using the newly formed apertures in substrate **411** as a mask) until the plasma etchant reaches the polysilicon sub-layer of first conductive layers **421C** and **421D**. A plasma gas for preferentially etching silicon dioxide over silicon is used. Field oxide region **415A** is divided into regions **415A** and **415B**, and field oxide region **415D** is divided into regions **415D** and **415E**. As the next step, the polysilicon sub-layer of first conductive layers **421C** and **421D** are plasma etched using a suitable plasma gas. The result of these steps is shown in **FIG. 85**.

[0203] The next set of processing steps are as follows, with **FIG. 86** showing the final result of these steps. A passivation layer **465** is formed on the back surface of substrate **411**, which also coats the exposed underside portions of conductive layers **421C** and **421D**, and the exposed side portions of field oxide regions **415A**, **415B**, **415D**, and **415E**. Passivation layer **465** preferably comprises vapor deposited parylene, and preferably has a thickness of approximately 20 μm. Holes are laser etched through passivation layer **465** at those locations where backside contact **467** is to contact first conductive layers **421C** and **421D**, after which passivation layer **465** is plasma cleaned to removed the debris left over from the laser etch process. Next, backside contacts **467** are formed, preferably by first depositing a seed plating layer over the back surface of substrate **411**, laminating a resist layer (e.g., RISTON) over the back surface of substrate, patterning the laminated resist layer to form windows therein which overlie the areas where contacts **467** are to be formed, and thereafter plating additional conductive material over the seed layer in those areas exposed by the resist windows. Next, the resist layer is removed, and the portions of the seed layer which are not covered by plated material are removed. The seed layer preferably comprises a thin layer of sputtered chromium (e.g., 200 Angstroms to 400 Angstroms in thickness), followed by a thicker layer of sputtered copper (e.g., 0.1 μm to 0.2 μm in thickness). The additional conductive material plated onto the seed layer preferably comprises copper, with a thickness of approximately 10 μm. In the case where the seed layer comprises sputtered copper over sputtered chromium, the seed layer may be removed by a short exposure to any of the common copper etching solutions, followed by a short exposure to any of the common chromium etching solutions (e.g., HCl, dilute H_2SO_4). The brief exposure to the copper etching solution may also etch the plated material of contacts **467**, but this is of little consequence since the thickness of plated material is substantially greater than the thickness of the seed layer. As a final preferred step, a thin layer of nickel is plated over the copper by an electroless plating process, and a thin layer of gold is plated over the nickel layer by an electroless plating process.

[0204] The next set of processing steps are as follows, with **FIG. 87** showing the final result of these steps. Adhesive layer **480** is bonded to the top surface of secondary substrate **470**. To enable vias **490** to pass through layer **480**, the portions of layer **480** which overlie apertures **472** of secondary substrate **470** are removed by laser ablation. The laser light is directed through the apertures **472** from the bottom surface of substrate **470**. In this manner, substrate **470** acts as a mask and directs the laser light to only those portions of adhesive layer **480** that are to be removed. A self-aligned pattern in layer **480** is thereby created. As the next steps, primary substrate **411** is diced to a final size, removed from temporary substrate **611**, and mounted onto adhesive layer **480** to thereby laminate it onto secondary

substrate **470**, with its bottom surface facing the top surface of secondary substrate **470**. These three steps may be done in any order. In a preferred embodiment, the first two steps are performed in either order, followed by the third step. In another embodiment, temporary substrate **612** is first removed from primary substrate **411**, then substrate **411** is mounted onto secondary substrate, and finally substrate **411** is diced to size. Adhesive layer **480** preferably comprises a bonding sheet. Exemplary bonding sheet are, for example, Mitsubishi BT bonding film BT F346, Mitsubishi LCP reinforced BT prepreg GMPL-195, and Shin-etsu epoxy bonding sheets types E31 through E38. Each of these examples are thermosetting bonding sheets which comprise epoxy which has been gelled to the intermediate B-stage. Adhesive layer **480** may also comprise a polyimide bonding sheet, such as Nippon Steel polyimide bonding sheet SPB-A. The result of these steps is shown in **FIG. 86**.

[0205] As the next step, a solder paste is screened into apertures **472** of secondary substrate **470**, and then reflowed to make electrical connections between conductive layers **474** and layers **421C** and **421D**. The solder paste generally comprises a volatile carrier which evaporates during reflow, thereby reducing the volume of conductive mass formed within each aperture **472**. The reduction of volume can cause a problem if each aperture **472** does not have a conductive layer **474** which extends from the substrate's top surface to the substrate's bottom surface. In those cases where layers **474** do not extend from top surface to bottom surface, Additional volume may be added by placing reflowed solder balls over the screened solder paste prior to the reflow operation, and thereafter reflowing the solder paste with the solder balls disposed over the respective bodies of solder paste. The solder bodies meld with the reflowed solder pastes, and compensate for the volume lost by the evaporation of the volatile components in the solder paste. The result of this approach is show in **FIG. 76**. In constructed embodiments of the present invention, a tin-silver (SnAg) solder paste and tin-silver solder balls are used. However, other solders may be used. In addition, a conductive adhesive may be used in place of solder, particularly for lower speed (frequency) application.

[0206] Thus, by the practice of the embodiments of the present invention there is provided a capacitor deplating method (see **FIGS. 66 and 67**) wherein metal contacts from defective capacitors **320*b*** are removed. In the method, a number of capacitors **320** are formed on a semiconductor substrate **300**. Metal contacts are formed over the capacitors **320**. A photoresist layer **324** is patterned over the metal contacts such that the metal contacts are exposed through the layer. The resulting structure is then placed in an electrolytic bath and the contacts over defective capacitors **320*b*** can be deplated. For example, if the defective capacitor **320*b*** has a short circuit **307**, current flows through the structure and the short circuit **307** so that deplating can occur. Good capacitors have an insulating layer which prevents the formation of a complete circuit and prevents deplating. By removing the contacts over defective capacitors **320*b***, yields can be increased.

[0207] By the further practice of embodiments of the present invention there are provided methods for forming a multi-chip module (MCM) having an active or passive semiconductor device embedded within the chip package structure. Other embodiments of the invention relate to the MCM and any subcomponents thereof (see FIGS. **68-73** by way of illustration). For example, **FIG. 71** illustrates a substrate for a CPU. The substrate includes a silicon layer disposed between a copper/polyimide thin film structure and ceramic carrier (AlN). The silicon layer can include active device or passive devices. For instance, the silicon layer can include a chip capacitor to decouple noise in a power distribution system.

[0208] While the present invention has been described herein with reference to particular embodiments thereof, a latitude of modification, various changes and substitutions are intended in the foregoing disclosure, and it will be appreciated that in some instances some features of the invention will be employed without a corresponding use of other features without departing from the scope and spirit of the invention as set forth. Therefore, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope and spirit of the present invention. It is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments and equivalents falling within the scope of the appended claims.

What is claimed is:

1. A method for deplating defective capacitors comprising:

forming a plurality of capacitors on a semiconductor substrate;

forming a plurality of metal contacts on the plurality of capacitors;

depositing a layer of photoresist on the semiconductor substrate;

patterning the photoresist layer so that the plurality of metal contacts are exposed;

contacting the exposed metal contacts with an electrically conductive solution; and

deplating metal contacts which are disposed over defective capacitors.

2. The method of claim 1 wherein the defective capacitors comprise capacitors having at least one short circuit.

3. A method for forming a multi-chip module comprising:

forming a thin-film polymeric interconnect structure having a first side and a second side disposed on a silicon substrate which includes active or passive devices; and

mounting a computer chip on the first side of the thin film interconnect structure.

4. The method of claim 3 further comprising reducing the thickness of the semiconductor substrate to form a thin semiconductor layer, and then forming an aperture through the thin semiconductor layer.

5. The method of claim 3 further comprising disposing a ceramic carrier on the semiconductor layer on the side opposite the interconnect structure.

6. A multi-chip module comprising:

a thin-film polymeric interconnect structure having a first side and a second side;

a chip disposed on the first side;

a semiconductor layer disposed directly on the second side and including active or passive devices.

7. The multi-chip module of claim 6 wherein the active devices comprise SRAMs and wherein the passive devices comprise chip capacitors.

8. The multi-chip module of claim 6 wherein the semiconductor layer further comprises an aperture extending through the layer.

9. The multi-chip module of claim 8 wherein the aperture is filled with solder.

10. A multichip module substrate capacitor structure comprising:

a substrate having a top surface and a bottom surface;

a doped region of the substrate located at the substrate's top surface;

an ohmic contact located on the top surface of the substrate, and a first dielectric layer disposed over the doped region;

a first conductive layer having a top surface and a bottom surface, and being disposed over the first dielectric layer with its bottom surface adjacent to the first dielectric layer, said first conductive layer having at least a sub-layer of a first conductive material disposed at its top surface;

a second dielectric layer disposed over the first conductive layer;

an aperture formed in the second dielectric layer and disposed over the first conductive layer to expose a portion thereof;

a conductive via formed through the aperture and disposed against a portion of the first conductive layer and comprising a second conductive material disposed adjacent to the sub-layer of first conductive material of said first conductive layer, said second conductive material being different from said first conductive material; and

a second conductive layer having a top surface and a bottom surface, and being disposed over the second dielectric layer with its bottom surface adjacent to second dielectric layer, said second conductive layer having a portion therefor disposed over the conductive via.

11. The module of claim 10 wherein said first conductive layer comprises polysilicon and a top layer of aluminum.

12. The module of claim 10 wherein the doped region comprises a top dope layer formed over substantially the entire surface of the substrate.

13. The module of claim 10 wherein said substrate comprises a doping level of more than 1×10^{-18} cm^{-3} and wherein the doped region is provided by the entire substrate.

14. The module of claim 10 wherein said first dielectric layer comprises silicon oxide.

* * * * *

#4

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/137,163
Filing Date	May 2, 2002
First Named Inventor	Karl Pichler
Group Art Unit	~~Not yet assigned~~ 2823
Examiner Name	~~Not yet assigned~~ H. LEE
Attorney Docket Number	2002P03156US

PE JC79 AUG 13 2002 PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
Lee	A1	4,682,565		Carrico	July 28, 1987	
Lee	A2	5,757,126		Harvey III et al.	May 28, 1998	
Lee	A3	5,874,804		Rogers	Feb. 23, 1999	
Lee	A4	5,895,228		Biebuyck et al.	Apr. 20, 1999	
Lee	A5	6,102,541		Yang et al.	Aug. 15, 2000	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
Lee	A6	WO	00/36665		Battelle Memorial Ins.	22 June 2000		
Lee	A7	DE	196 03 746		Wolfgang Grothe	24 Apr. 1997		

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
Lee	A8	Hayes, Donald J. et al., "Low-cost display assembly and interconnect using ink-jet printing technology", Journal of the SID, **9/1**, 2001, pps. 9-13.	
Lee	A9	Le, Hue P., "Porgress and Trends in Ink-jet Printing Technology, Part 4", Society for Imaging Science and Technology, **42/1**, Jan/Feb. 1998, pps. 1-9.	
Lee	A10	Wilson, J.S. et al., "Spin-dependent exciton formation in π-conjugated compounds", Nature, **413**, Oct. 2001 pp. 828-831	

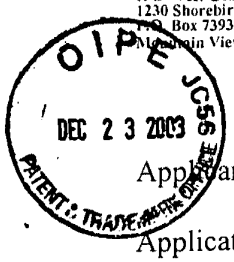
Examiner Signature	Kevin Min Lee	Date Considered	6/7/03

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Image

2823



ATTORNEY DOCKET NO.: 2002P03156US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Karl Pichler, et al.

Application No.: 10/137,163

Filed: 5/2/02

Title: IMPROVED ENCAPUSLATION FOR ORGANIC LIGHT EMITTING DIODES

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date.

12/19/03 Cynthia Reese
Date

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted under 37 CFR 1.97 (c) together with either a Certification under 37 CFR 1.97 (e), or a $180.00 fee under 37 CFR 1.17 (p) authorized to be charged to Deposit Account **19-2179** . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **19-2179** pursuant to 37 CFR 1.25. After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first.

Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Citation together with copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

The undersigned certifies under 37 CFR 1.97(e)(2) that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 1.56(c) more than three months prior to the filing of the information disclosure statement.

The filing of this information disclosure statement shall not be construed as a representation that a search has been made or that no other material information exists. Further, the filing of this information disclosure statement shall not be construed as an admission against interest in any manner or as an admission that the information cited is, or is considered to be material to patentability.

It is requested that the information disclosed herein be made of record in this application.

Date: Dec. 19, 2003

Respectfully requested,

By: Thomas George

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OIPE JC56
DEC 2 3 2003
PATENT AND TRADEMARK OFFICE

FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) (37 CFR 1.98(b))	ATTY. DOCKET NO.: 2002P03156US	SERIAL NO.: 10/137,163
	APPLICANT(S): Karl Pichler et al.	
	FILING DATE: 5/2/02	GROUP ART UNIT: 2823

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUB-CLASS	FILING DATE if appropriate
	AA	6,570,352 B2	5/27/03	Graff, et al.	313	506	6/22/01
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						

FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUB-CLASS	TRANSLATION	
							YES	NO
	AI							
	AJ							
	AK							
	AL							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AM	
	AN	
	AO	
	AP	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/137,163	05/02/2002	Karl Pichler	2002P03156US	1705

7590 02/19/2004

Siemens Corporation
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186 Wood Avenue South
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EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/137,163	PICHLER ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *41-46* is/are allowed.

6)☒ Claim(s) *1-40 and 47-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. The objection to specification, claims 14, 16, 56; 112-second-paragraph rejection to claim 24 and 102 rejections are withdrawn.

2. Claims 1-58 are pending in the application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 51-53 are rejected under 35 U.S.C. 102(e) as being anticipated by Ghosh et al. (US 2001/0052752).

Ghosh et al., in Fig. 4 and related text, teach the claimed method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

- fabricating a plurality of devices 13 (i.e. OLED) on a substrate 2;
- depositing at least one planarization layer 21 upon said devices 13;
- depositing at least one barrier layer 22 over planarization layer 21; and
- depositing a secondary encapsulation layer 23 over said barrier layer 22, wherein the secondary encapsulation layer 152 comprises depositing a polymer (paragraph [0032]); and wherein at least one deposition step is accomplished by gas nozzle

deposition because Ghosh et al. use atomic layer deposition (i.e. ALD) for deposition , which inherently teaches using gas nozzle.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-2, 10-12, 19, 20-27, 30-31, 33-34, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghosh et al. (US 2001/0052752) in view of Boroson et al. (US 6,590,157).

In re claims 1, 19, 20-23, 25-27, 34, Ghosh et al. teach a method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

- fabricating a plurality of devices 3 (i.e. OLED) on a substrate 2 (Fig.3);
- depositing at least one planarization layer 21 (i.e. a polymer layer, paragraph [0031]) upon said devices 3 (Fig.3);
- removing unwanted areas of the at least one planarization layer 21 (i.e. removing by patterning the one planarization layer 21, paragraph [0031]); and
- selectively depositing at least one barrier layer 22 (i.e. a dielectric layer, oxide) over said over the patterned planarization layer, wherein the barrier layer 22 is in a larger area than the planarization layer 21 (Fig.3).

Ghosh et al. further teach steps of patterning the planarization layer 21 (i.e. polymer layer) via masking technique (paragraph [0032]) but do not teach hardening or curing said at least one

planarization layer 21 in a patterned manner such that the hardened region substantially covers said devices 3.

Boroson et al., in an analogous art, teach forming a plurality of devices 32 (i.e. OLED) on the substrate 10, depositing a planarization layer (i.e. a sealing layer, which is a polymer material) and utilizing UV light to cure or harden the planarization layer (col. 9, lines 28-52).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to harden the planarization layer as taught by Boroson et al, in the method of Ghosh et al. so that it would cure the planarization layer and proceed the patterning step to remove areas of the planarization layer that are not hardened.

In re claim 2, one of the ordinary skilled in the art would have recognized that the polymer layer (i.e. the planarization layer) is formed by spin coating.

In re claims 10-12, Ghosh et al. in view of Boroson et al teach the claimed limitation because Boroson et al. teach utilizing UV light for hardening the planarization, which can be integrated with the patterning step of Ghosh et al.

In re claim 24, Ghosh et al. also teach that the plurality of devices are a plurality of OLED displays and substantially only light emissive areas are covered by the planarization layer and the barrier layer.

In re claims 30-31 and 33, Ghosh et al. teach removing unwanted planarization layer by patterning, which comprising chemically etching and removing the organic layer (i.e. the polymer layer).

In re claim 37, Ghosh et al. further teach depositing the organic layer (i.e. polymer layer) through a shadow mask (paragraph [0032]).

7. Claims 3-9, 35-36, 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghosh et al. in view of Boroson et al. as applied to claims 1-2 above and further in view of Amundson et al. (US 6,498,114) and Massingill et al. (US 2002/0155661).

In re claims 3-4, 6-9, 35-36 and 38-40, Ghosh et al. in view of Boroson et al. do not teach depositing at least one planarization layer and the barrier layer by evaporation (claims 3 and 4) or roll coating (claim 6) or dip coating (claim 7) or spray coating (claim 8) or screen printing (claims 9, 36, 39-40) or ink jet (claims 35 and 38).

However, the aforementioned methods have been widely used for depositing the polymer layer, as evidenced by Amundson et al.. Amundson et al., in col. 4, lines 56-62 and col. 7, lines 17-32, teach forming the planarization layer 20 over a substrate 10 (Fig.1) using evaporation, roll coating, dip coating, spray coating and ink jet printing processes.

Therefore, it would have been obvious to one of the ordinary skilled in the art, at the time the invention was made, to utilize methods of evaporation, roll coating, dip coating, spray coating, screen printing and ink jet processing as taught by Amundson et al for depositing the planarization layer or the polymer layer in Ghosh et al. in view of Boroson et al., since these methods are good candidates for forming the planarization layer.

In re claim 5, Ghosh et al. in view of Boroson et al. do not teach depositing at least one planarization layer by blade coating.

However, the aforementioned method has been widely used for depositing the polymer layer (i.e. planarization layer), as evidenced by Massingill et al. in paragraph [0134], wherein they teach forming the photoresist layer comprising blade coating, roll coating, spray coating and screen printing.

Therefore, it would have been obvious to one of the ordinary skilled in the art, at the time the invention was made, to utilize the blade coating of Massingill et al for depositing the planarization layer in Ghosh et al. in view of Boroson et al. , since the method is a good candidate for forming the planarization layer.

8. Claims 13-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Ghosh et al. in view of Boroson et al. as applied to claim 1 above and further in view of Cheng et al. (US 6,524,937).

Ghosh et al. in view of Boroson et al. do not expressly teach hardening the planarization layer by cross-linking (claim 13); and removing areas of the organic layer that are not cross-linked by thermal evaporation (claim 14) or by applying a short high temperature pulse (claim 15-16).

However, as the polymer layer is exposed to the UV light, it would form cross-linking compound, as evidenced by Cheng et al. (col. 5, lines 30-31). Cheng et al. teach that the cross-linking of the polymer layer (i.e. photoresist layer) can be achieved by exposing to a high temperature (col. 5,lines 63-67), which would cause thermal evaporation of solvent in the photoresist layer.

Therefore, it would have been obvious to one of the ordinary skilled in the art, at the time the invention was made, to utilize the methods of Cheng et al in the method of Ghosh et al. in view of Boroson et al. to form cross-linking, since by doing so it would form the planarization layer with etch selectivity, which, in turn, is beneficial to the subsequent patterning step.

9. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghosh et al. in view of Boroson et al. as applied to claim 1 above and further in view of Fujibayasni et al. (US 5,369,151).

Ghosh et al. in view of Boroson et al. do not teach removing areas of the planarization layer that are not hardened by pumping in a vacuum or by thermal evaporation and pumping in a vacuum.

However, removing the planarization layer by the thermal evaporation in a vacuum system has been widely used in the art, as evidenced by Fujibayasni et al. in col. 8, lines 42-47.

Therefore, it would have been obvious to one of the ordinary skilled in the art, at the time the invention was made, to utilize methods of Fujibayasni et al. for removing the unwanted planarization layer in the method of Ghosh et al. in view of Boroson et al. , since by doing so it would satisfactory provide a patterned layer over the plurality of the devices.

10. Claims 28, 29 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghosh et al. in view of Boroson et al. as applied to claim 1 above and further in view of Dimitrakopoulos et al. (US 6,500,604).

In re claim 28 and 29, Ghosh et al. in view of Boroson et al. do not teach depositing the planarization layer by evaporating a plurality of reactive organic molecules, said reactive organic molecules comprising a condensed conformal film on the substrate; and the planarization layer comprises one of a group, said group comprising a Parylene coating of said organic layer over the substrate, and a plasma-assisted organic material deposition.

However, Dimitrakopoulos et al. teach forming a planarization layer (i.e. a protective material layer) comprising a Parylene coating of said organic layer over the substrate, and a plasma-assisted deposition (col. 4, lines 16-17 and 45-46).

Therefore, it would have been obvious to one of the ordinary skilled in the art, at the time the invention was made, to utilize the plasma-assisted depositing methods of Dimitrakopoulos et al. in the method of Ghosh et al. in view of Boroson et al. , since by doing so it would satisfactory form the planarization layer comprising Parylene.

In re claim 32, Ghosh et al. in view of Boroson et al. do not teach removing said areas of unwanted planarization layer by one of a group, said group comprising etching an organic layer with a plasma-assisted etching process, oxygen plasma, reactive ion-etch, anisotropic etch, laser assisted/based removal and laser ablation.

However, utilizing the aforementioned methods for patterning the planarization layer has been widely used in the art, as evidenced by Dimitrakopoulos et al. in col. 5, lines 40-45, wherein the reactive ion-etch and plasma-assisted etching are used.

Therefore, it would have been obvious to one of the ordinary skilled in the art, at the time the invention was made, to utilize the removing methods of Dimitrakopoulos et al. in the method of Ghosh et al. in view of Boroson et al., since by doing so it would satisfactory remove the unwanted portion of the planarization layer.

11. Claims 47-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghosh et al. (US '752) in view of Ahn et al. (US 2002/0094624).

Ghosh et al. teach the claimed method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

- fabricating a plurality of devices 13 (i.e. OLED) on a substrate 2 (Fig.2);
- depositing at least one planarization layer 11 upon said devices 13 (Fig.2); and
- depositing at least one barrier layer 12 over said planarization layer 11 (Fig.2).

Ghosh et al. further teach that the method is performed by atomic layer deposition (ALD) technique but do not expressly teach that the method is accomplished in an inert atmosphere.

However, ALD technique has been widely used in depositing dielectric materials, wherein the technique is performed in inert atmosphere to prevent unwanted residues, as evidenced by Ahn et al. (paragraph [0021]).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to perform the method of Ghosh et al. in inert atmosphere, as taught by Ahn et al., since by doing so it would prevent the devices from contamination.

12. Claims 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghosh et al. (US '752) in view of Chang et al. (US 2003/0194493).

Ghosh et al. teach using ALD for deposition but do not expressly teach that the deposition is accomplished by gas nozzle and an array nozzles are positioned above the substrate and moving the array and the substrate in relative motion in depositing.

However, Chang et al. teach using ALD apparatus for depositing, wherein ALD includes the array nozzles positioning above the substrate and moving the array and the substrate in relative motion in depositing (paragraphs [0048]. [0049], [0051]).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to include the teachings as taught by Chang et al. in the method of Ghosh et al., since by this manner it would provide a uniform deposition.

13. Claims 57-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghosh et al. (US '752)

Ghosh et al., in Fig. 4, also teach the claimed electronic device, comprising" a substrate 2; a plurality of active areas 13 (i.e. OLED) disposed upon the substrate 2; a planarization layer 21 disposed on the substrate 2 substantially covering the active areas 13; and a barrier layer 22 disposed on the substrate 2 whereby the barrier layers 22 cover substantially only the planarization layer 21.

Ghosh et al. do not teach that the planarization and barrier layers are plural.

However, one of the ordinary skilled in the art would have been motivated to repeat the deposition to form plural layers, since by doing so it would protect the active areas from moisture attack. In other words, although reference did not disclose a plurality of planarization and barrier layers, mere duplication of layers has no patentable significance unless an unexpected result is produced. See M.P.E.P. 2144.04 VI.

Allowable Subject Matter

14. Claims 41-46 are allowed.

15. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record, Ghosh et al. to US 2001/0052752, teaches a related method, as stated above. However, Ghosh et al. neither teach nor suggest depositing a *mask* on top of the substrate such that mask *openings are placed on top* the devices; and *removing the mask* from the substrate.

Response to Arguments

16. Applicant's arguments with respect to claims 1-58 have been considered but are moot in view of the new ground(s) of rejection.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Examiner
Art Unit 2823

Feb. 13, 2004



Notice of References Cited	Application/Control No. 10/137,163	Applicant(s)/Patent Under Reexamination PICHLER ET AL.	
	Examiner Hsien-Ming Lee	Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
X	A	US-2001/0052752	12-2001	Ghosh et al.	313/512
X	B	US-6,590,157	07-2003	Boroson et al.	174/52.2
X	C	US-6,498,114	12-2002	Amundson et al.	438/780
X	D	US-2002/0155661	10-2002	Massingill et al.	438/244
X	E	US-6,524,937	02-2003	Cheng et al.	438/574
X	F	US-5,369,151	11-1994	Fujibayashi et al.	523/414
X	G	US-6,500,604	12-2002	Dimitrakopoulos et al.	430/322
X	H	US-2002/0094624	07-2002	Ahn et al.	438/200
X	I	US-2003/0194493	10-2003	Chang et al.	427/248.1
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

OIPE JC56
DEC 2 3 2003
PATENT & TRADEMARK OFFICE

FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) (37 CFR 1.98(b))	ATTY. DOCKET NO.: 2002P03156US	SERIAL NO.: 10/137,163
	APPLICANT(S): Karl Pichler et al.	
	FILING DATE: 5/2/02	GROUP ART UNIT: 2823

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUB-CLASS	FILING DATE if appropriate
Lee	AA	6,570,352 B2	5/27/03	Graff, et al.	313	506	6/22/01
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						

FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUB-CLASS	TRANSLATION YES	TRANSLATION NO
	AI							
	AJ							
	AK							
	AL							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AM	
	AN	
	AO	
	AP	

EXAMINER Lee	DATE CONSIDERED 2/12/04

EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this f rm with next communication t applicant.

Search Notes

Application No.	Applicant(s)	
10/137,163	PICHLER ET AL.	
Examiner	**Art Unit**	
Hsien-Ming Lee	2823	

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EASt attached (USPAT,USPG, EPO,JPO, Derwent)	2/13/2004	LEE

Index of Claims

Application No.	Applicant(s)
10/137,163	PICHLER ET AL.
Examiner	**Art Unit**
Hsien-Ming Lee	2823

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date	Claim		Date	Claim		Date
Final	Original	2/12/04	Final	Original	2/12/04	Final	Original	
	1	√		51	√		101	
	2	√		52	√		102	
	3	√		53	√		103	
	4	√		54	√		104	
	5	√		55	√		105	
	6	√		56	√		106	
	7	√		57	√		107	
	8	√		58	√		108	
	9	√		59			109	
	10	√		60			110	
	11	√		61			111	
	12	√		62			112	
	13	√		63			113	
	14	√		64			114	
	15	√		65			115	
	16	√		66			116	
	17	√		67			117	
	18	√		68			118	
	19	√		69			119	
	20	√		70			120	
	21	√		71			121	
	22	√		72			122	
	23	√		73			123	
	24	√		74			124	
	25	√		75			125	
	26	√		76			126	
	27	√		77			127	
	28	√		78			128	
	29	√		79			129	
	30	√		80			130	
	31	√		81			131	
	32	√		82			132	
	33	√		83			133	
	34	√		84			134	
	35	√		85			135	
	36	√		86			136	
	37	√		87			137	
	38	√		88			138	
	39	√		89			139	
	40	√		90			140	
	41	=		91			141	
	42	=		92			142	
	43	=		93			143	
	44	=		94			144	
	45	=		95			145	
	46	=		96			146	
	47	√		97			147	
	48	√		98			148	
	49	√		99			149	
	50	√		100			150	

L Number	Hits	Search Text	DB	Time stamp
1	1646	(Uv with cur$4) with (planariz$5 or photoresist or resist or organic)	USPAT; US-PGPUB	2004/02/12 11:35
2	35	((Uv with cur$4) with (planariz$5 or photoresist or resist or organic)) same devices	USPAT; US-PGPUB	2004/02/12 11:44
3	2	(("20030087476") or ("20030082889")).PN.	USPAT; US-PGPUB	2004/02/12 11:40
4	719	(harden$3 with (planariz$5 or photoresist or resist or organic)) and (OLED or LED)	USPAT; US-PGPUB	2004/02/12 11:51
5	177	((harden$3 with (planariz$5 or photoresist or resist or organic)) and (OLED or LED)) and barrier	USPAT; US-PGPUB	2004/02/12 11:45
6	1276	harden$3 and (OLED or LED) and barrier	USPAT; US-PGPUB	2004/02/12 11:52
7	25	harden$3 and (plurality with (OLED or LED)) and barrier	USPAT; US-PGPUB	2004/02/12 11:55
8	0	harden$3 and (plurality with (OLED or LED)) and barrier	EPO; JPO; DERWENT; IBM_TDB	2004/02/12 11:55
9	14	harden$3 and (plurality with (OLED or LED))	EPO; JPO; DERWENT; IBM_TDB	2004/02/12 12:00
10	262	harden$3 and (plurality with (OLED or LED))	USPAT; US-PGPUB	2004/02/12 12:00
11	215	(harden$3 and (plurality with (OLED or LED))) and @ad<20020503	USPAT; US-PGPUB	2004/02/12 12:00

L Number	Hits	Search Text	DB	Time stamp
1	863	((OLED or devices) with plurality) same mask	USPAT; US-PGPUB	2004/02/13 10:01
2	135	(((OLED or devices) with plurality) same mask) and substrate and barrier	USPAT; US-PGPUB	2004/02/13 10:01
3	106	((((OLED or devices) with plurality) same mask) and substrate and barrier) and @ad<20020502	USPAT; US-PGPUB	2004/02/13 10:33
4	116	(ALD same inert) and @ad<20020502	USPAT; US-PGPUB	2004/02/13 10:34
5	18	(ALD same inert same dielectric) and @ad<20020502	USPAT; US-PGPUB	2004/02/13 10:55
6	2	(ALD same inert same polymer) and @ad<20020502	USPAT; US-PGPUB	2004/02/13 10:37
7	5	(ALD same nozzles) and @ad<20020502	USPAT; US-PGPUB	2004/02/13 10:56

Image

2823

SIEMENS CORPORATION
Intellectual Property Department
170 Wood Avenue South
Iselin, New Jersey 08830

Attn: Elsa Keller, Legal Department
Telephone: 732-321-3026

OIPE JC173 FEB 0 9 2004 PATENT & TRADEMARK OFFICE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

February 6, 2004

Vicki Chia

By: Vicki W. Chia

ATTORNEY DOCKET NO.: 2002P03156US

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Karl Pichler, et al.

Serial No.: 10/137,163

Filing Date: 05/02/2002

Title: **IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES**

Examiner: Lee, Hsien Ming

Art Unit: 2823

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

[ ] under 37 CFR 1.97 (b), or
(Within three months of filing national application; or date of entry of international application; or before mailing date of either a first office action on the merits or a first office action after filing of a Request for Continued Examination under § 1.114; whichever occurs last)

[X] under 37 CFR 1.97 (c) together with either a:
[ ] Certification under 37 CFR 1.97 (e), or
[X] A $240.00 fee under 37 CFR 1.17 (p) authorized to be charged to Deposit Account **19-2179**.
At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **19-2179** pursuant to 37 CFR 1.25.
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

[ ] under 37 CFR 1.97 (d) together with a:
[ ] Certification under 37 CFR 1.97 (e), and
[ ] the required fee under 37 CFR 1.97 (d) (2) which is $240.00 under 37 CFR 1.17(p) is authorized to be charged to Deposit Account **19-2179.** (Filed after final action or notice of allowance, whichever occurs first, but on or before payment of the issue fee)

[ ] under 37 CFR 1.97 (i)
[ ] Filed after payment of issue fee, but before grant of patent - No fee or certification required

Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Citation together with copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

02/12/2004 TBESHAH1 00000118 192179 10137163

01 FC:1806 180.00 DA

SDC EX. 1002 - 307/544

[ ] A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content that is given on the attached sheet or by the enclosed English-language search report.

[X] The undersigned hereby certifies under 37 CFR 1.97(e)(1) that each item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; or

[ ] The undersigned certifies under 37 CFR 1.97(e)(2) that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 1.56(c) more than three months prior to the filing of the information disclosure statement.

[ ] Applicants do not believe any fee is due. However, at any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **19-2179** pursuant to 37 CFR 1.25. A duplicate copy of this sheet is enclosed.

The filing of this information disclosure statement shall not be construed as a representation that a search has been made or that no other material information exists. Further, the filing of this information disclosure statement shall not be construed as an admission against interest in any manner or as an admission that the information cited is, or is considered to be material to patentability.

It is requested that the information disclosed herein be made of record in this application.

Respectfully Submitted,

Thomas George

Thomas George, Reg. No. 45,740
Attorney for Applicant(s)
Date: 2/5/04
Telephone No.: (650) 694-5191

SDC EX. 1002 - 308/544

OIPE JC173 FEB 0 8 2004 PATENT & TRADEMARK OFFICE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	1

Complete if Known	
Application Number	10/137,163
Filing Date	05/02/2002
First Named Inventor	Pichler, et al.
Group Art Unit	2823
Examiner Name	Lee, Hsien Ming
Attorney Docket Number	02P03156US

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (*if known*)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		6,570,325 B2		Graff, et al.	05/27/2003	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (*if known*)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	A		
	B		
	C		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

05-03-02 A

J1131 U.S. PTO 05/02/02

Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

PATENT APPLICATION
Attorney Docket No. : 2002P03156US
Express Mail Label No. EV 048645610US
Date of Deposit : May 2, 2002

jc986 U.S. PTO 10/137163 05/02/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

THE ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

TRANSMITTAL LETTER FOR NEW APPLICATION

Sir:

Transmitted herewith for filing is a(n) [X]Original patent application.
[X] Utility [ ] Design [ ]Continuation-in-part application

INVENTOR(S): Karl Pichler and Kyle D. Firschknecht

TITLE: IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

Enclosed with this Transmittal (submitted in duplicate) are:

[X] Twenty-four (24) page specification.
[X] Eight (8) sheets of drawings [ ] formal [X] informal drawings (one set)
[X] The Declaration and Power of Attorney [] signed [X] unsigned
[X] Filing fee has been calculated as shown below (other than small entity):

For	Number Filed	Number Extra	Rate	Additional Fees
Total Claims	58 - 20	= 38	x $ 18	$684.00
Indep. Claims	8 - 3	= 5	x $ 84	$420.00
[ ] First Presentation of a Multiple Dependent Claim			+ $260	$ -0-
		Basic filing Fee		$ 740.00
			Total	$1,844.00

Please charge my Deposit Account No. 19-2179 in the amount of $1,844.00 . The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment to Deposit Account No. 19-2179 pursuant to 37 CFR 1.25. A duplicate copy of this sheet is enclosed.

PLEASE MAIL CORRESPONDENCE TO:
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UNITED STATES PATENT APPLICATION

FOR:

IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

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Background of the Invention

One of the last manufacturing steps in the construction of an organic light emitting diode ("OLED") is encapsulation. Encapsulation is a way to protect the OLED device from the damaging environmental effects – primarily from oxygen and moisture. It is well known in the art to encapsulate an OLED device by physically mating a top glass (or other suitable material) layer over, but usually not touching, the OLED device with an epoxy border. The glass, together with its epoxy border, typically is an effective, tried-and-true way to provide the necessary environmental protection required for long-lived OLED usage.

Of late, there has been some discussion in the art to provide a cheaper and better manner of encapsulation, called "direct thin-film" encapsulation. In this manner, thin film encapsulation is typically described as a "polymer multi-layer" (PML) comprising alternating and repeating layers of an organic (usually acrylate or the like) and a barrier layer. **Figure 1** depicts a typical PML structure 100 as is currently known in the art. A glass (or other suitable material) substrate 102 provides the support structure for OLED structure 104 formed on top of substrate 102 in any manner known in the art. Layers 102 and 104 form typically the structure that requires encapsulation – either by known techniques or by the encapsulation techniques of the present invention.

Typically, for PML structures, a planarization layer 106 is formed on top of OLED structure 104. Planarization layer 106 typically is an organic layer (e.g. acrylate or the like) and is provided to give a planar surface for the deposition of the PML structure 112a. PML structure 112a typically comprises barrier layer 108 and another planarization layer 110.

Barrier layer 108 typically comprises a sputtered metal, metal-oxide or a dielectric layer. Barrier layer 108 provides the necessary environmental isolation from the corrosive effects of oxygen and moisture. Planarization layer 110 may again comprise an organic layer (e.g. acrylate or the like) and is typically laid down to provide a planar surface for deposition of the barrier layer 108. This entire PML structure 112a may be repeated (e.g. PML structure 112b) -- possibly several times -- for additional encapsulation of the entire OLED device.

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The advantages of direct thin-film encapsulation over the prior art are primarily cost reduction and improved reliability. Using direct thin-film encapsulation, the package may also be thinner and/or lighter and/or mechanically more flexible. Several structures and steps of the prior art may be excluded with this process. For example, there is no need for a separate glass plate, no need for an epoxy seal, no need for a getter (which is typical in the prior art).

One of the problems of the direct thin film encapsulation occurs with the barrier layer. The barrier layer should ideally not contain any point defects (i.e. pin holes) in its surface --- otherwise its usefulness as a barrier layer is severely compromised. That is primarily the reason that a planar organic layer is typically used as a substrate upon which the barrier layer is deposited.

This problem is exacerbated during the batch fabrication of many OLED devices upon a single large sheet of glass – such as shown as a top view in **Figure 2**. Upon such a single glass sheet 200, several tens (or even hundreds) of OLED devices 202 may be so fabricated. As depicted, OLED devices 202 are typically laid down in rows and columns on a large sheet of glass 200. Typically, each OLED 202 comprises an electrical contact area 204 for electrically mating the OLED device to a driver circuit.

At the thin film encapsulation step, the PML structure is deposited where at least one UV-curable organic liquid material is deposited over the entire glass sheet containing the multiple OLED devices. This organic layer is subsequently cured – followed by a deposition of a barrier layer (e.g. sputtered metal-oxide or dielectric). Such a process may be repeated to form a PML structure – primarily to avoid external particle/dirt-induced pinhole defects. After encapsulation, singulation is performed, for example by forming scribe and break lines 206 upon the entire structure so that individual OLED devices 202 may be separated and further processed.

The problem with this PML technique is that the only part of the device that requires encapsulation is the OLED structure itself – and not, e.g., the electrical contact pads. In fact, the contact pad must typically be exposed for electrical mating with external driver circuitry. So, at a minimum, additional processing must be performed for the removal of the PML structure over these areas.

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Another potential problem with the current PML techniques is that by having the PML layer over the scribe and break lines and/or the glue lines the integrity of the sealed package may be deteriorated, for example by delamination of the PML layer over these areas.

Approaches other than PML are known in the prior art that use combination of organic planarizing layers together with inorganic barrier layers to achieve some degree of thin-film direct encapsulation. Organic planarization layers that do not require special cure may be used as well as layers that are electron-beam or thermally cured, in vacuum or gas atmosphere, preferably inert gas. Such organic layers may also be deposited in non-liquid form, e.g. be evaporated or plasma-deposited (e.g. Parylene).

Summary of the Invention

In one embodiment, herein is described a method of encapsulating a plurality of OLED devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of OLED devices on a substrate;

depositing at least one planarization layer upon said OLED devices;

hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said OLED device;

removing areas of the at least one planarization layer that are not hardened; and

selectively depositing at least one barrier layer over said hardened region.

In yet another embodiment, herein is described a method of encapsulating a plurality of OLED devices fabricated upon a substrate, the steps of said method comprising

fabricating a plurality of OLED devices on a substrate;

depositing at least one planarization layer upon said OLED devices wherein said planarization layer is deposited as an unpatterned liquid film;

selectively depositing at least one barrier layer over said planarization layer; and

removing said areas of unwanted planarization layer.

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In yet another embodiment, herein is described a method of encapsulating a plurality of OLED devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of OLED devices on a substrate;

selectively depositing at least one planarization layer upon said OLED devices; and

selectively depositing at least one barrier layer over said planarization layer.

In yet another embodiment, herein is described a method of encapsulating a plurality of OLED devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of OLED devices on a substrate;

depositing a mask on top of said substrate, such that mask openings are placed on top of said OLED devices;

depositing at least one planarization layer upon said mask;

removing said mask from said substrate; and

selectively depositing at least one barrier layer over said planarization layer.

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Brief Description of the Drawings

Figure 1 is side view of a typical PML encapsulation structure formed over an OLED device.

Figure 2 is a top view of an array of mass-produced OLED structures upon a large glass substrate.

Figures 3A and 3B are a set of side view diagrams showing the processing steps of one embodiment of the encapsulation techniques as made in accordance with the principles of the present invention.

Figures 4A and 4B are a set of side view diagrams showing another embodiment of the present invention.

Figure 5 is a side view of yet another embodiment of the present invention.

Figures 6A through 6E are a set of side view diagrams showing still yet another embodiment of the present invention.

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Figures 7A through 7C are a set of diagrams depicting a gas nozzle deposition system made in accordance with the principles of the present invention.

Detailed Description of the Invention

Turning attention to **Figures 3A – 3B**, there is shown a series of side views of OLED devices being encapsulated in accordance with the principles of the present invention. In **Figure 3A**, substrate 300 has formed upon its surface several OLED devices 302. For the purposes of the present invention, this structure is to be construed very broadly. For example, substrate 300 could be comprised of glass (possibly with ITO as a first electrode), quartz, plastic foils, metal, metal foils, silicon wafers or any other potential substrate material that encompasses very broad classes of OLED devices. Broadly, the OLED device could be bottom-emitting or top-emitting. The device could have the bottom electrode as anode or cathode respectively – in either a top or bottom emitting configuration.

Additionally, the encapsulation techniques and structures of the present invention could be used for any number of applications – e.g. active matrix, passive matrix, segmented, alpha-numeric, or backlight OLED displays or any combination thereof. It will be appreciated that any of these OLED devices could be some that have structures patterned on the OLED substrate that are much higher than the OLED stack itself -- e.g. several micron high row separators (e.g. mushrooms) or an ink-confinement well / bank such as used in ink-jet-printed OLEDs. It is intended that the scope of the present invention includes encapsulating over these structures that are within the active areas of the display.

Additionally, it should be appreciated that the scope of the present invention also includes other displays and any electronic or other devices that require encapsulation – e.g. general organic electronic devices such as organic transistors, detectors, solar-cells, etc. (particular OLEDS) and also includes displays for lighting such as OLED-based light sources and backlights.

It should be appreciated that the present invention also comprises a myriad of electronic devices, said devices comprising: a substrate; a plurality of active areas disposed upon said substrate; a plurality of planarization layers disposed on said

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substrate whereby said planarization layer cover substantially only said active areas; and a plurality of barrier layers disposed on said substrate whereby said barrier layers cover substantially only said planarization layers. In particular, the present invention comprises electronic devices such as an OLED, an organic electronic circuit, an organic detector, an organic solar cell.

A UV-curable organic layer 304 is substantially deposited over the entire display glass comprise a plurality of OLED devices. Such suitable organic layer could be a liquid comprising acrylate, together with a photo initiator for selective curing – or other materials such as generally known in the PML and UV or otherwise curable organic planarization layer technology / prior art..

It should be appreciated that layer 304 could also be any suitable planarization layer. For example, an inorganic or hybrid planarization layer might also suffice as a buffer layer that has desirable planarizing and/or protecting properties from the barrier layer deposition process.

Additionally, a wet-processable and post-processing curable organo-metallic compounds such as spin-on glasses might suffice. Such an organic layer might provide a planar structure on which to deposit a barrier layer and to substantially cover point defects (e.g. dirt particles) in lower layers. It is generally desirable that the organic layer be deposited in sufficient quantity so that any such layer is no longer "conformal" to the point defect – i.e. any point defects are not geometrically projected upwards into layers deposited above. Such a first organic layer might also serve to protect the underlying OLED from potential damage due to the deposition of the first barrier layer.

In yet other embodiments, non-PML approaches could be used within the scope and principles of the present invention. For example, a non-liquid evaporated organic – e.g. polysiloxane as might be applied to later Figures.

It will be appreciated that there are many manners of depositing this organic layer upon the OLED device. For example, the layer could be either evaporated or flash evaporated. Alternatively, a liquid organic layer could be spun coated, dip coated, roll coated, spray-coated or blade coated – as is well known in the art. Additionally, other suitable printing technology could be employed, in particular, screen-printing or ink-jet printing.

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Once the organic layer is deposited upon the OLED devices, UV-light is used to selectively cure the layer over the OLED devices to produce the desired cross-linking. This step could be accomplished by a mask 306 which blocks the UV light from areas where it is desired that the organic layer be removed. Alternatively, the cross-linking could be accomplished by using a UV light having an optical patterning system, such as a projection exposure system. In another embodiment, the cross-linking could be accomplished by selectively scanning the UV beam across the plate. In yet another embodiment, the layer need not necessarily have to be UV-cured. Instead, it could be thermally cured -- e.g. using a heat source that has a temperature profile, an IR laser, a stencil/stamp, or e-beam cured. Other methods might include: cross-linking, patterned heat transfer system, patterned IR source, masked IR source, scanned IR source, patterned e-beam, masked e-beam and scanned e-beam.

Once the organic layer has been selectively cross-linked, the remaining uncross-linked layer should be removed. This removal may be accomplished by thermal evaporation (e.g. by heating the substrate) or by using short higher temperature pulses (e.g. placing the OLED plate onto a hotplate). Other removal methods are also possible – e.g. pumping in a vacuum to remove the liquid organic layer. A combination of techniques is also possible – applying thermal energy while pumping in a vacuum.

Still other methods of removal are possible – immersion in a rinse tank, spray-rinsing, ultra-sonicing (either dry or wet), or some combination of techniques (e.g. dry ultra-sonic or mega-sonic in a vacuum). Plasma etching techniques could also be employed to aid the removal process. Additionally, laser-assisted methods such as laser ablation or providing heat via laser might suffice.

Once the residual organic layer has been removed, then a barrier layer is selectively deposited on the OLED plate. **Figure 3B** shows that barrier layer 308 is selectively deposited over the OLED devices where the organic layer has been also deposited. Barrier layer 308 comprises any material that is suitable to protect the OLED device from the environmental effects of oxygen and moisture – and, as such, should be relatively impervious to them. Such barrier layer material might comprise a metal-oxide or a dielectric layer, e.g. SiOx (e.g. SiO2), SiNx (e.g. Si2N3), SiOxNy, AlOx (e.g. Al2O3), AlNx, ITO, ZnOx, Al-doped ZnOx, or any high barrier dielectrics or conductive

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oxides. Generally, any inorganic materials known in the prior art that give good oxygen and water barrier properties would suffice for purposes of the present invention. In the case of a bottom emitting display, the encapsulation does not have to be transparent, then metal or alloy films (e.g. Al or alloys, Cr, Cu or alloys, etc.) or non-transparent or colored dielectric films are potentially suitable, both evaporated or sputtered.

The deposition of the barrier layer can be any suitable method known in the art to deposit dielectric layers, metal-oxides, metals or alloys. For example, sputtering or reactive sputtering (DC, AC, pulsed, or a combination thereof) would suffice. Additionally, evaporation of such dielectrics (resistive heating or electron beam) or metal films is possible. Further, ion-beam assisted or other plasma-enhanced deposition methods are also possible.

It should be appreciated that other embodiments are possible. For example, the patterned UV cure described herein could be done such that the thickness of the planarization layer gradually decreases from the value over the active area to zero or near zero somewhere outside the active area. This may facilitate a nice smooth encapsulation of the OLED (or other structures) plus the planarization layer from the active area out to where there is no encapsulation (e.g. scribe / break line and/or contacts). It might be desirable to have the barrier layer slightly larger in area to cover the planarization layer because the planarization layer might not have such a sharp step and such a barrier layer coverage might provide adequate side step coverage. This embodiment applies also to the embodiments discussed herein, as they may be tuned to provide such a smooth transition of the buffer layer by way of re-flow or evaporation or printing or partial pre-cure and the like of the planarization layer at the edges prior to barrier layer deposition. In yet another embodiment, it might be desirable to encapsulate only the organic light-emissive areas (e.g. pixels) and leave the contact pads, auxiliary encapsulation areas, scribe/break areas free of the organic and barrier layers.

Figures 4A and 4B depict another embodiment of the present invention and particularly a different manner of encapsulating OLED devices. **Figure 4A** shows a step in the processing of present invention in which OLED devices 404 are formed on top of substrate 402. Organic layer 406 is deposited over the entire substrate, covering OLED devices 404. Then, barrier layer 408 is selectively deposited in a manner known in the art

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– e.g. through a mask or screen 410 – situated on top of the OLED devices. **Figure 4B** shows the next step in the processing after that portion of the unwanted organic layer 406 is removed by methods known in the art.

It will be appreciated that organic layer 406 may or may not be cured in its entirety and may or may not be cured selectively through a mask or screen. Likewise, it might be desirable not to cure the organic layer at all. In several embodiments, the organic may be either fully cured before patterned barrier layer deposition, partly cured or completely non-cured and that after the barrier layer deposition, there may be another cure step to ensure that the underlying organic is cured to the intended level, if it wasn't already before the barrier layer deposition. If the unwanted organic layer is etched away (by any number of etching methods known – e.g. chemical (dry or wet) etch, plasma-assisted (with or without oxygen), reactive-ion etching, anisotropic reactive-ion etching, etc.) then barrier layer 408 might act as an effective etch stop as well as laser assisted/based removal (e.g. laser ablation).

In addition, the organic layer could be deposited in any manner previously described (e.g. evaporation of a plurality of reactive organic molecules to form a condensed conformal layer on the substrate) or by well-known Parylene coating methods.

In one embodiment, it may be the case that the edges of the active areas are exposed; however, even if the planarization layer is only a few microns thick and the planarization + barrier layer perimeter around the active device is tens or even over 100 microns wide, then permeation of e.g. water through this thin planarization layer along the 10's or >100 microns should be slow. Alternatively, a second barrier layer may be larger than the area of the planarization layer so that the exposed planarization layer edge is covered with barrier layer also. This could also be achieved by making a potential second planarization layer + barrier layer stack wider than the first and so on. This can naturally already be done in previous embodiments by making the barrier layer mask wider.

Figure 5 depicts another embodiment of encapsulation techniques in accordance with the present invention. In this embodiment, OLED device 504 is again formed upon substrate 502. Organic layer 506 is deposited in a patterned fashion as well as barrier layer 508. As organic layer 506 is deposited selectively; there may be no need to cure the

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layer. It should be appreciated that the cure and patterning aspects could be independent; -- relating to the type of material and deposition technique of for the planarization layer. For example, if UV (or other)-curable liquids such as for PML or screen- or ink-jet print are used, then it is possible to cure. Alternatively, if evaporation of an organic through a mask is the relevant step, there may be no need to cure.

The manner of selectively depositing the organic layer and the barrier layer may be accomplished in a variety of ways. For example, organic layer may be selectively deposited though a shadow mask (as depicted as mask 510) or by ink jet deposition or other screen printing techniques. In fact, generally any printing techniques suitable to deliver the desired planarization layer material can be used. In similar fashion, barrier layer 508 may be selectively deposited. For alternative embodiments, it is possible to employ all options for selective deposition: same mask, different masks and also same mask with different substrate to mask distances (e.g. smaller distance for planarizing layer and then larger distance for barrier such that the barrier coverage is wider – because of slight non-directionality of and differences in the materials deposition).

In the case of printing, screen-printing, ink-jet-printing, the masks can either be not required (ink-jet) or possibly different from that used for a patterned sputter-deposited barrier layer deposition. For other embodiments, it may also be possible to partially cure the planarization layer, deposit the barrier layer and then complete the cure of the planarization layer, if necessary.

Figures 6A through 6E depict yet another embodiment of encapsulation techniques in accordance with the principles of the present invention. First, OLED device 602 is formed on substrate 600. Then, mask 604 is formed onto substrate 600 with mask openings for OLED devices 602.

It will be appreciated that a suitable mask might be formed in many possible manners. For example, such a mask might be a film laminated to the OLED or a mask pressed or pushed or clamped to the OLED. Additionally, such mask might be a multi-use mask or a one-off that then gets removed. Such mask might comprise a metal, ceramic, or plastic foil or sheet; it could also comprise a PTFE (Teflon) or a poly-siloxane type material (e.g. polydimethylsiloxane) or generally any material that does not stick to the OLED (which might cause damage or delamination when the mask is

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removed) and/or a material to which the encapsulation organic does not stick so well so that the mask's removal after encapsulation organic deposition and cure (complete or partial) does not remove the organic.

The mask might be such that it could be brought into contact with the OLED sufficiently well so that the encapsulation organic is confined over the desired areas and does not seep under the areas where the encapsulation organic is not desired (e.g. contact pads). Such a mask might comprise a "stamp" mask. Such a mask could be pressed on, clamped on, or the mask could be made of magnetic material and thus held by magnetic forces (e.g. with sheet magnet behind substrate that 'sucks' the mask to substrate). Additionally, the mask could be multi-use mask or one-off use. Vacuum-suction masks may also suffice. Additionally, a laminated film-mask could also suffice.

Once mask 604 is deposited, organic layer 606 is deposited in any suitable manner. For example, organic layer could be dispensed, squashed, rolled, printed, blade-coated, dropped into, sprayed onto the mask openings. Once deposited, then the organic layer may or may not be cured – either partially or completely prior to the removal of mask 604. The mask could be removed by any means known in the art --e.g. by peeling it off; mechanical removal if a stencil, and the like.

It will be appreciated that the edges of the planarization layer may or may not re-flow such that the subsequently deposited barrier gives better barrier edge coverage.

After the mask is removed, then barrier layer 608 is selectively deposited over the planarization layers covering the OLED devices. Any known technique for such selective deposition is suitable for purposes of the present invention. For various alternative embodiments, it is possible to either fully cure then remove mask; partly cure then remove mask; no cure then remove mask. These variations may also be in combination with potentially another cure after the barrier layer deposition. Specifically, it might be possible to slightly cure then remove mask then e.g. heat to reflow to smoothen the edges – then continue with full cure / barrier layer deposition.

In yet another embodiment, it is also possible to deposit both the planarization and barrier layer(s) before the removal of the mask.

In yet other embodiments, all encapsulation process steps could be accomplished in an inert atmosphere (i.e. with reduced oxygen, ozone, other reactive gases and in

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particular moisture). Alternatively, only the first organic layer and first barrier layer ("dyad") could be done in an inert atmosphere. Alternatively, only the first organic layer could be done in an inert atmosphere.

Other embodiments might include encapsulation with a secondary encapsulation layer for additional protection. This might be accomplished by laminating, glueing or otherwise depositing a plastic, metal, metal plus plastic foil, thin glass, thick glass or metal sheet over said OLED display sheet. Said secondary encapsulation may include a getter material (e.g. zeolite, reactive metal, reactive metal-oxide, metal-sulfide, etc.; in film, powder, paste, tablet, etc. form) in the package to absorb water, oxygen or other reactive gases. Singulation could be accomplished either before or after secondary encapsulation.

Figures 7A through 7C depict a novel gas nozzle deposition system for the deposition of several layers, including the planarization layer. **Figure 7A** shows one gas nozzle 704 as it is depositing a layer onto a device 702 upon a substrate 700. Nozzle 704 comprises at least a nozzle 706 that directs a gas, preferably inert, ~~to the layer being deposited~~ and a nozzle 708 that directs the material to be deposited – e.g. acrylate – onto the device. The gas directs the depositing material away from areas that should be free of deposition. **Figure 7B** shows the device 702 after having been covered with the layer by the gas nozzle system. More precisely, area 710 has been covered with the layer – while area 712 is left free of the deposit. Such an area 712 might represent electrical contacts, scribe lines, or other areas that are desired to be free of such deposit.

Figure 7C depicts the action of an array of such gas nozzles 720 that effects a deposition over a plate 700 of devices 702. Array 720 would comprise a plurality of planarization layer nozzles 721 and inert gas nozzles 723 that are advantageously disposed above the plate of devices so that the layer being deposited is done in only those areas desired. Area 730 is such a desired area for deposition, out of a total area 732 for the device. Array 720 and plate 700 could be placed into relative motion in order to effect an efficient deposition upon a plurality of devices. Direction 722 depicts a possible motion of the array over the plate; while direction 724 depicts a possible motion of the plate under the array – any combination of the two motions are also possible.

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It has now been shown several embodiments of advanced encapsulation techniques performed in accordance with the principles of the present invention. It will be appreciated that the present invention is meant to cover any and all obvious variations as described herein.

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CLAIMS:

1. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices;

hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said device;

removing areas of the at least one planarization layer that are not hardened; and

selectively depositing at least one barrier layer over said hardened region.

2. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises spin coating.

3. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises flash evaporation.

4. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises evaporation.

5. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises blade coating.

6. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises roll coating.

7. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises dip coating.

8. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises spray-coating.

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9. The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises one among a group, said group comprising: screen printing and ink jet printing.

10. The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises one of a group, said group comprising flood-exposure of UV light through a mask and scanning a line-source of UV light through a mask.

11. The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises exposure by UV light comprising an optical patterning system.

12. The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises exposure by UV light comprising a UV-beam scanning system.

13. The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer further comprises one of a group, said group comprising: cross-linking, patterned heat transfer system, patterned IR source, masked IR source, scanned IR source, patterned e-beam, masked e-beam and scanned e-beam.

14. The method as recited in Claim 1 wherein the step of removing areas of the at least one organic layer that are not cross-linked comprises removing by thermal evaporation.

15. The method as recited in Claim 14 wherein the step of removing by thermal evaporation further comprises applying a short high temperature pulse.

16. The method as recited in Claim 15 wherein the step of applying a short high temperature pulse further comprises placing the OLED plate onto a hotplate.

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17. The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises removing by pumping in a vacuum.

18. The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises removing by thermal evaporation and pumping in a vacuum.

19. The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises one of a group, said group comprising: washing, blowing away, rinsing, sonicing, and plasma.

20. The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises a barrier layer comprising one of a group, said group comprising a dielectric, a metal, a metal-oxide and an alloy.

21. The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing said barrier layer through a mask.

22. The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing the barrier layer in a larger area than the planarization layer.

23. The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing one of a group, said group comprising: metal-oxide, dielectric layer, SiOx, SiNx , SiOxNy, AlOx, AlNx, ITO, ZnOx, Al-doped ZnOx, metal film, and alloy film.

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24. The method as recited in Claim 1 wherein substantially only the light emissive areas are covered by the planarization layer and the barrier layer.

25. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices wherein said planarization layer is deposited as an unpatterned liquid film;

selectively depositing at least one barrier layer over said planarization layer; and

removing said areas of unwanted planarization layer.

26. The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises curing an organic layer selectively over the substrate.

27. The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises curing an organic layer over the entire substrate.

28. The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises evaporating a plurality of reactive organic molecules, said reactive organic molecules comprising a condensed conformal film on the substrate.

29. The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises one of a group, said group comprising a Parylene coating of said organic layer over the substrate, and a plasma-assisted organic material deposition.

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30. The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises etching an organic layer.

31. The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises etching an organic layer with a chemical etch process.

32. The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises one of a group, said group comprising etching an organic layer with a plasma-assisted etching process, oxygen plasma, reactive ion-etch, anisotropic etch, laser assisted/based removal and laser ablation.

33. The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises removing said organic layer.

34. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

selectively depositing at least one planarization layer upon said devices; and

selectively depositing at least one barrier layer over said planarization layer.

35. The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by ink jet of an organic layer.

36. The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by one of a group, said group comprising: screen printing of an organic layer and depositing by gas nozzle.

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37. The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing an organic layer through a shadow mask .

38. The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by ink jet of said barrier layer.

39. The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by screen printing of said barrier layer.

40. The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises one of a group, said group comprising: depositing by shadow mask, sputtering, ink jet deposition, screen printing and evaporation.

41. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing a mask on top of said substrate, such that mask openings are placed on top of said devices;

depositing at least one planarization layer upon said mask;

removing said mask from said substrate; and

selectively depositing at least one barrier layer over said planarization layer.

42. The method as recited in Claim 41 wherein the step of depositing said mask further comprises one of group, said group comprising: depositing a stamp mask, depositing a laminated film-mask, depositing a vacuum mask, magnetically held mask.

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43. The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing said mask such that said mask is in contact with said substrate.

44. The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising a material substantially non-sticking to OLED substrate over the areas in between the active areas.

45. The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising one of a group, said group comprising a metal, a ceramic, a plastic, a polymer, PTFE, and poly-siloxane.

46. The method as recited in Claim 41 wherein the step of depositing at least one planarization layer further comprises depositing an organic layer over the entire mask.

47. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices; and

depositing at least one barrier layer over planarization layer wherein at least one said step is accomplished in an inert atmosphere.

48. The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is the step of depositing at least one planarization layer.

49. The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is the step of depositing at least one barrier layer.

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50. The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is both the step of depositing at least one planarization layer and the step of depositing at least one barrier layer.

51. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices;

depositing at least one barrier layer over planarization layer; and

depositing a secondary encapsulation layer over said barrier layer.

52. The method as recited in Claim 51 wherein the step of depositing a secondary encapsulation layer further comprises depositing one of a group, said group comprising: a plastic, a metal, a metal plus plastic foil, a polymer, and glass.

53. The method as recited in Claim 51 wherein the step of depositing a secondary encapsulation layer further comprises singulating the devices before the deposition of said secondary encapuslation.

54. A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices; and

depositing at least one barrier layer over planarization layer wherein at least one said deposition step is accomplished by gas nozzle deposition.

55. The method as recited in Claim 54 wherein one said deposition step is accomplished by gas nozzle deposition further comprises depositing a layer over a plurality of devices with an array of nozzles positioned above said substrate.

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56. The method as recited in Claim 55 wherein the step of depositing a layer over a plurality of devices further comprises moving said array and said substrate in relative motion.

57. An electronic device, said device comprising:

a substrate;

a plurality of active areas disposed upon said substrate;

a plurality of planarization layers disposed on said substrate whereby said planarization layer cover substantially only said active areas; and

a plurality of barrier layers disposed on said substrate whereby said barrier layers cover substantially only said planarization layers.

58. The electronic device as recited in Claim 57 wherein said electronic device is one of a group, said group comprising an OLED, an organic electronic circuit, an organic detector, an organic solar cell.

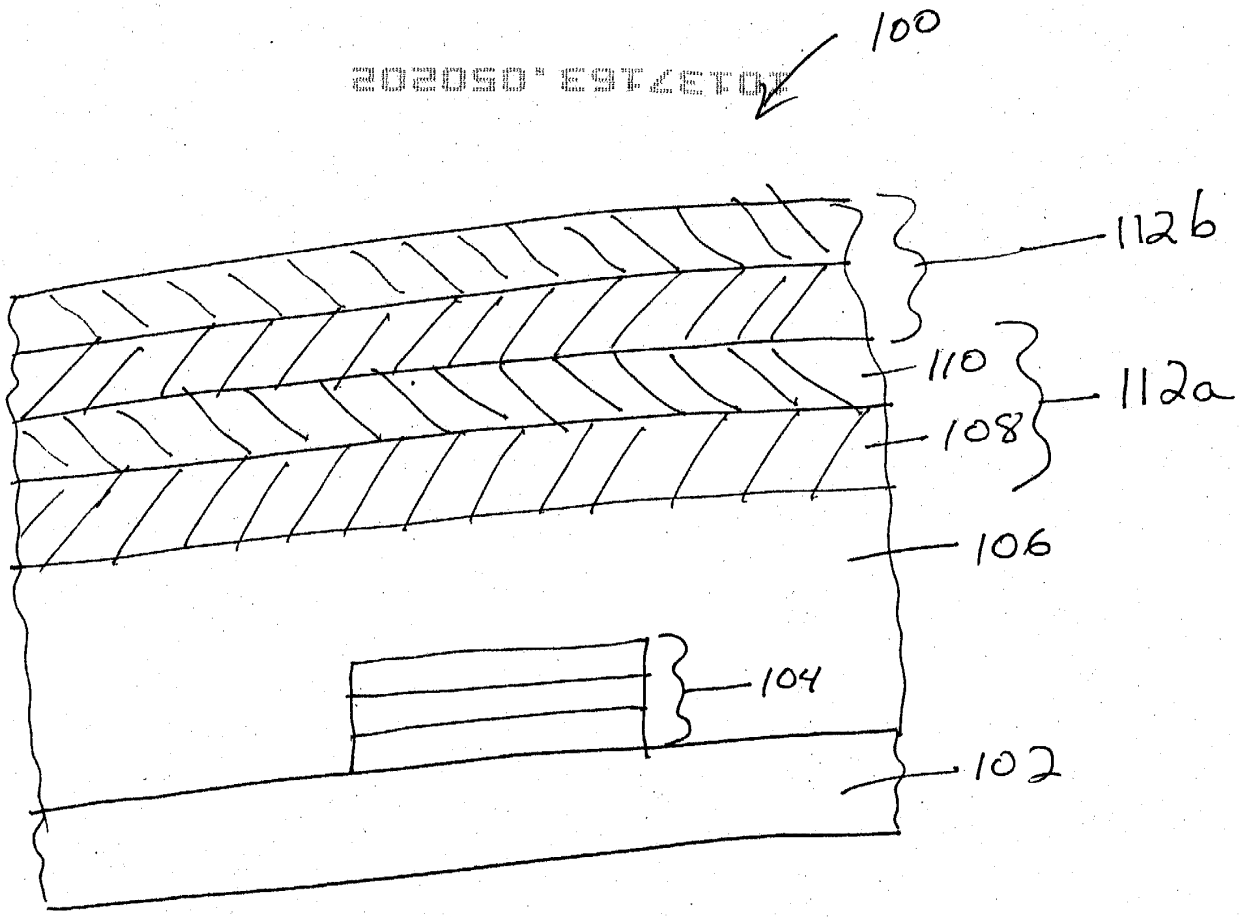
SDC EX. 1002 - 333/544

ABSTRACT

A method of encapsulating a plurality of OLED devices fabricated upon a substrate is described, the steps of said method comprising: fabricating a plurality of OLED devices on a substrate; depositing at least one planarization layer upon said OLED devices; hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said OLED device; removing areas of the at least one planarization layer that are not hardened; and selectively depositing at least one barrier layer over said hardened region.

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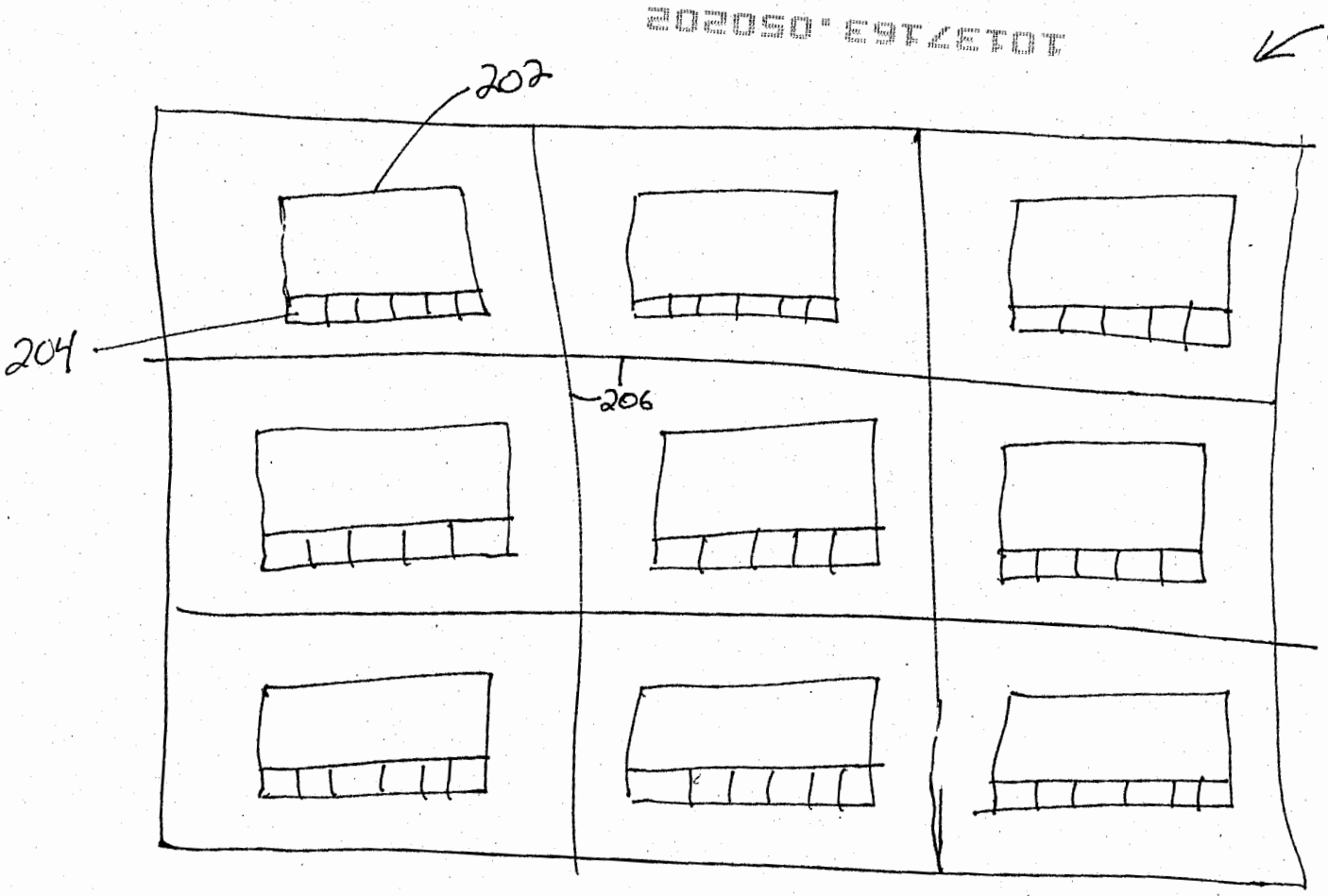
SDC EX. 1002 - 334/544



(PRIOR ART)

FIGURE 1

SDC EX. 1002 - 335/544



(PRIOR ART)

FIGURE 2

SDC EX. 1002 - 336/544

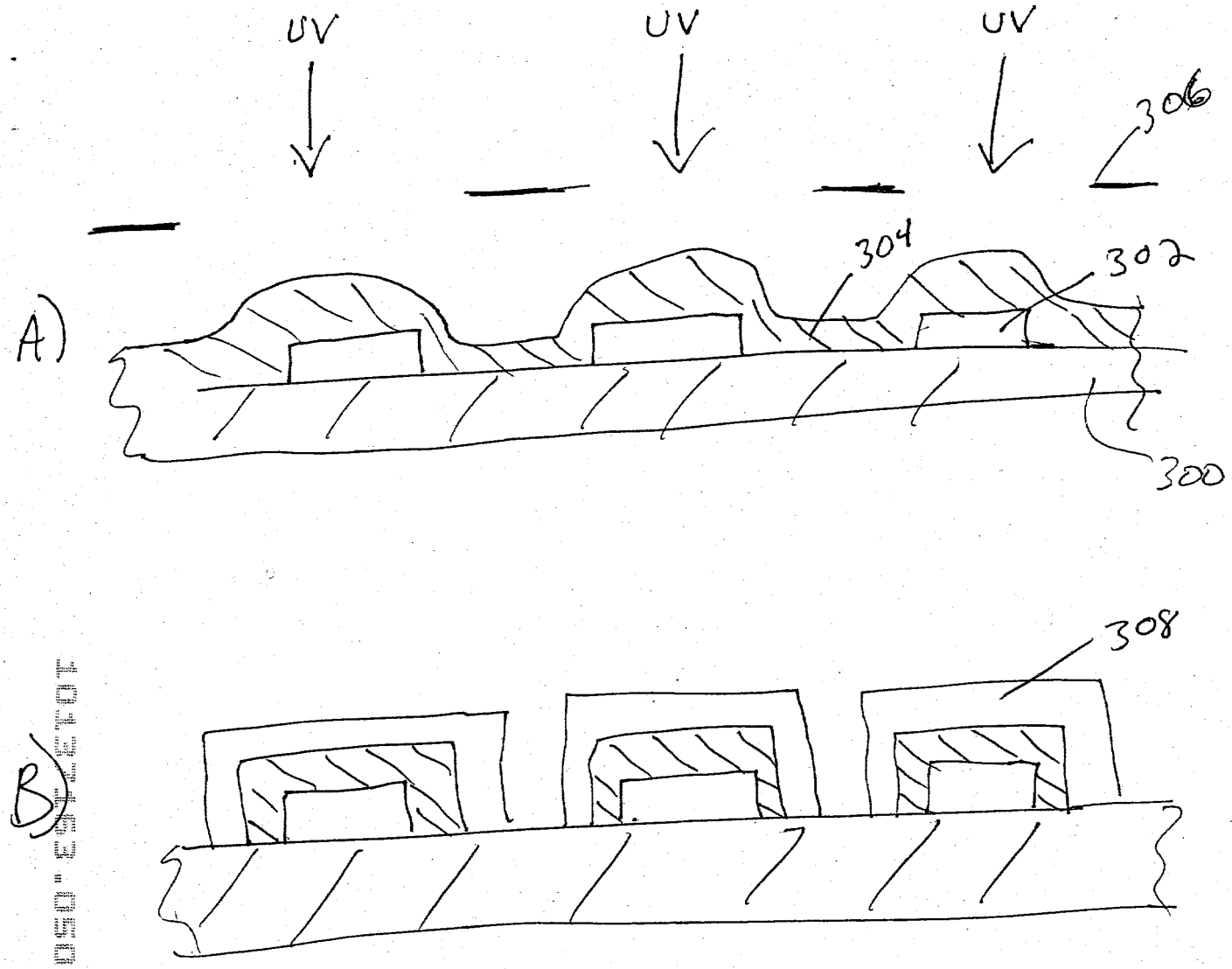


FIGURE 3

Petitioner's Exhibit 1002

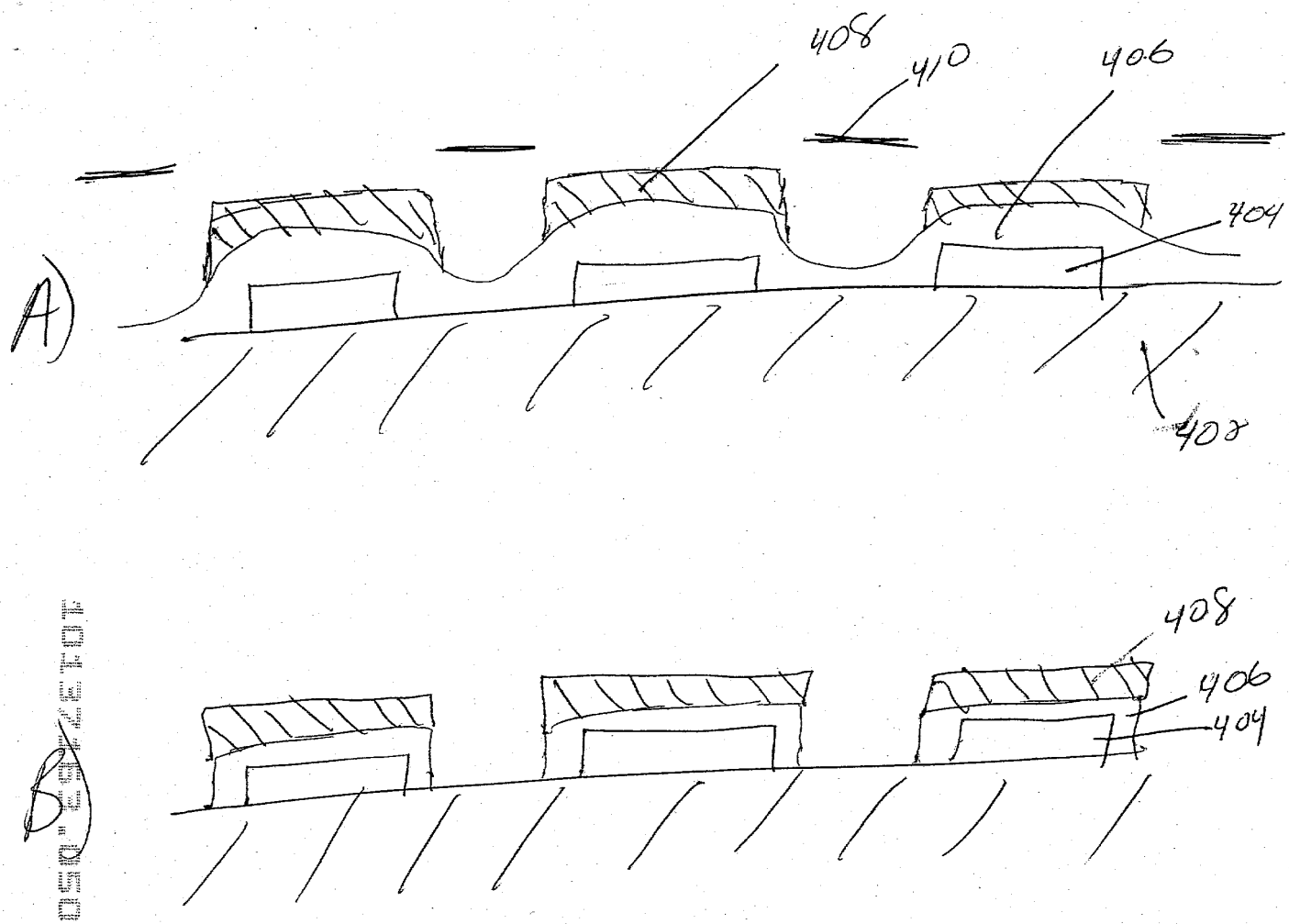


FIGURE 4

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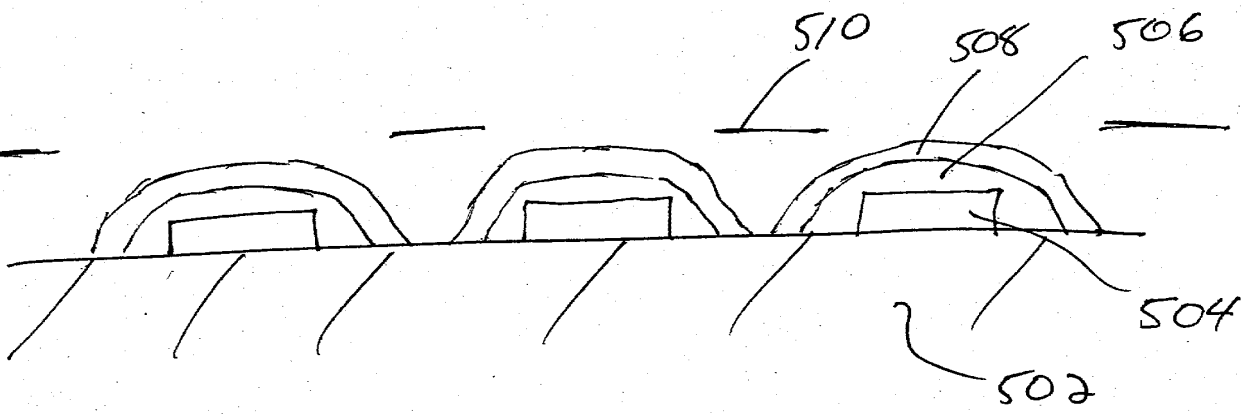


FIGURE 5

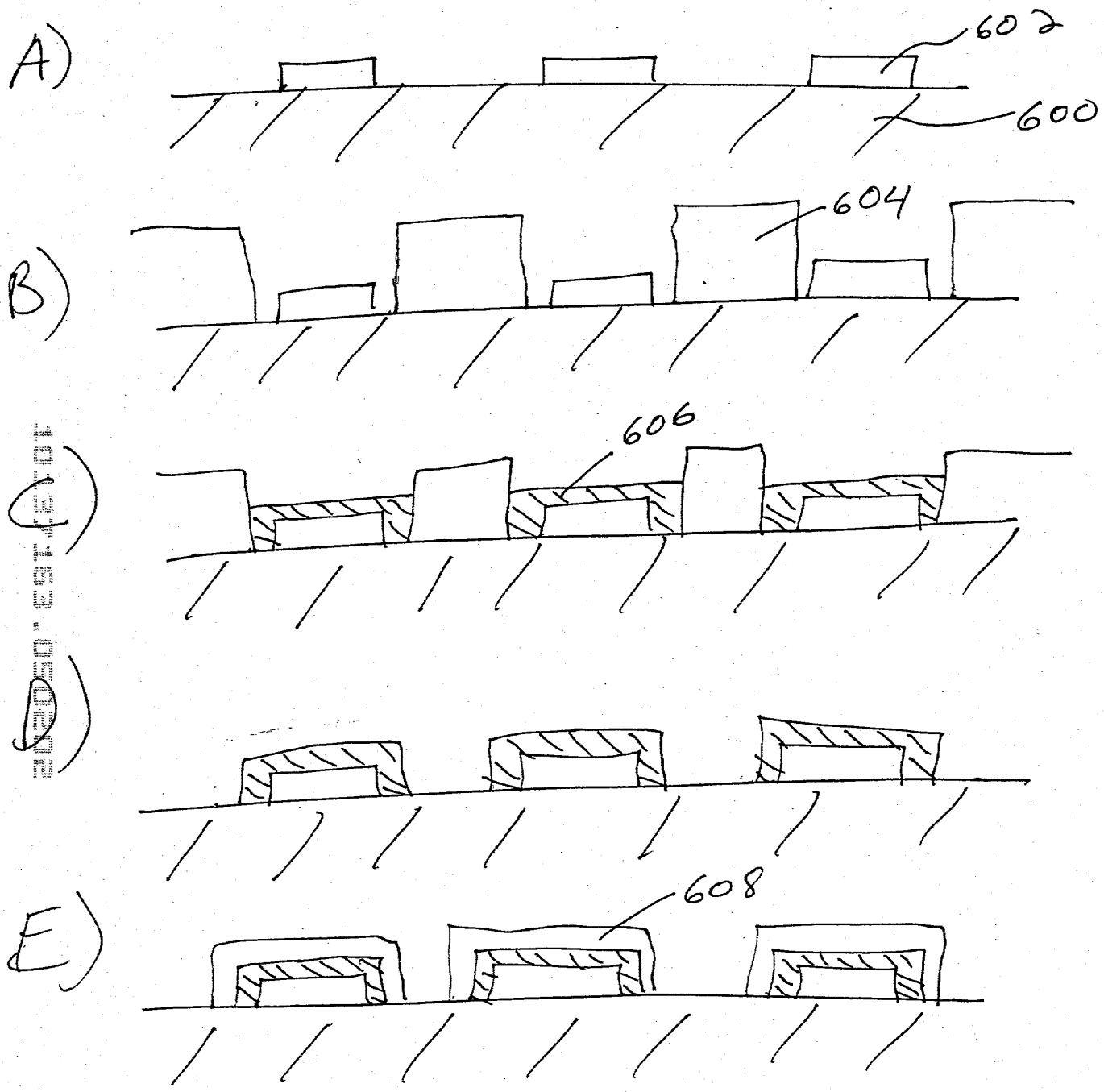


FIGURE 6

SDC EX. 1002 - 340/544

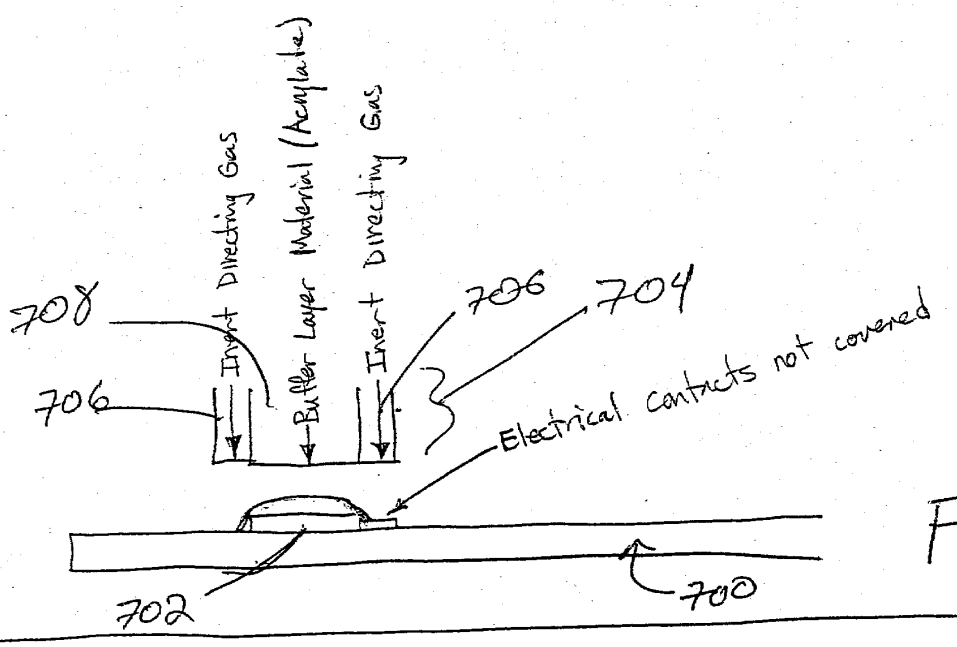


FIG 7A

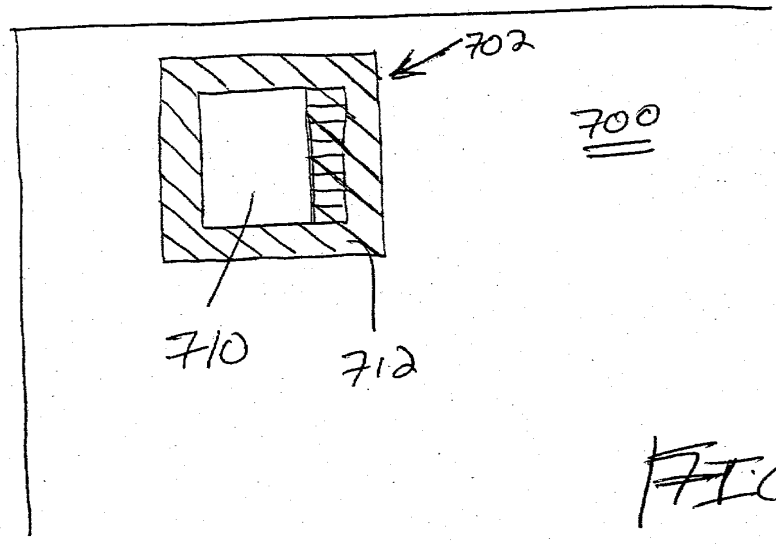


FIG 7B

SDC EX. 1002 - 341/544

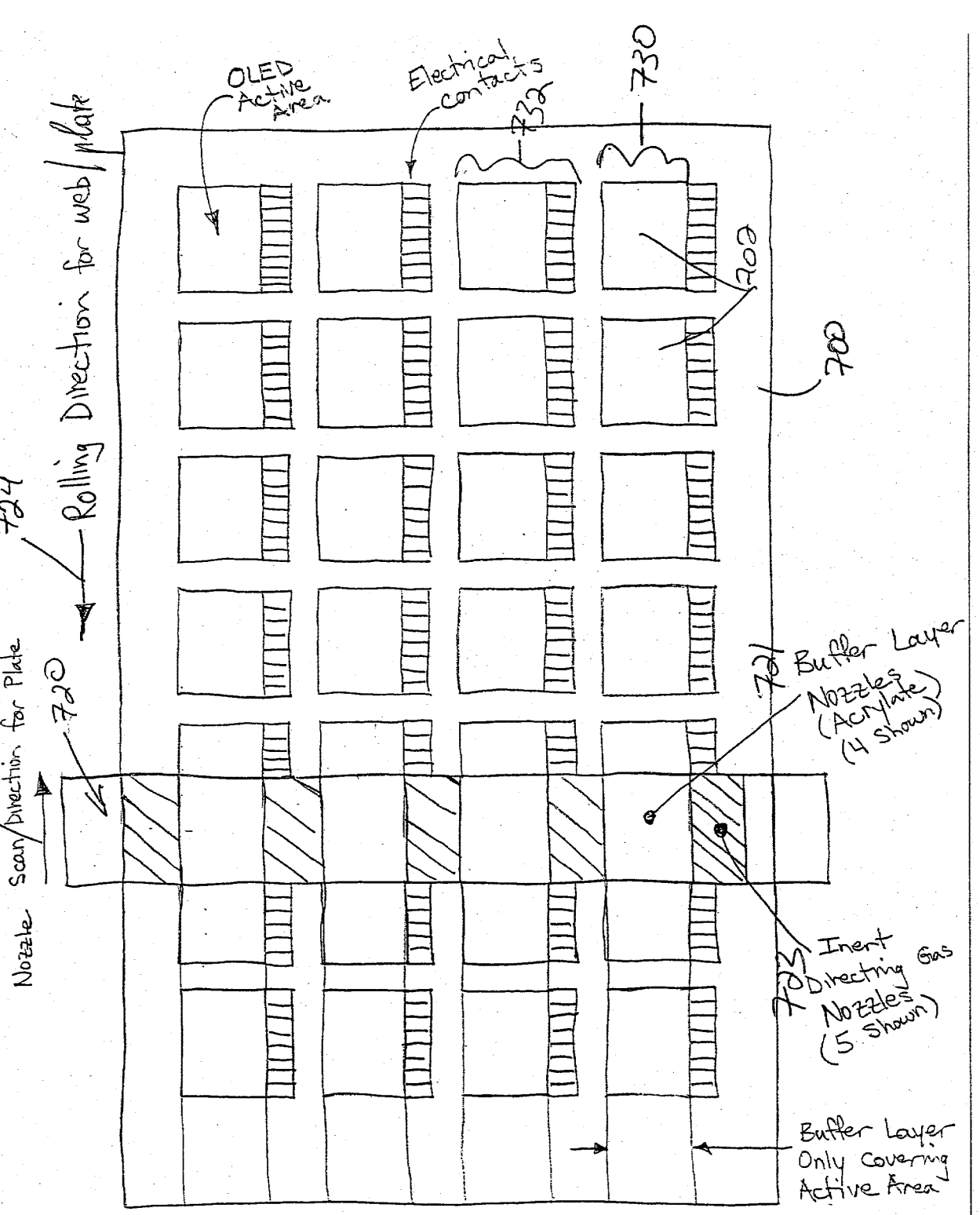


Fig 7C

SDC EX. 1002 - 342/544

DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

the specification of which (check one)
__is attached hereto.
___ was filed on as Application Serial No.
and was amended on _____ (if applicable)

List of Inventors: Karl Pichler AND Kyle D. Firschknecht

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Codes, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			Priority claimed	
(Number)	(Country)	(Day/month/year filed)	Yes	No
(Number)	(Country)	(Day/month/year filed)	Yes	No

application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

2002P03156US

(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)
(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application listed below:

(Application Serial No.)	(Filing date)	(Status)

Power of Attorney: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Adel A. Ahmed, Reg. No. 29,606; I. Marc Asperas, Reg. No. 37,274; Stanton C. Braden, Reg. No. 32,556; Alexander J. Burke, Reg. No. 40,425; Dexter K. Chin, Reg. No. 38,842; David D. Chung, Reg. No. 38,409; Joseph S. Codispoti, Reg. No. 31,819; Henry J. Groth, Reg. No. 39,696; Mark H. Jay, Reg. No. 27,507; Brian K. Johnson, Reg. No. 46,808; Stuart P. Kaler, Reg. No. 35,913; Rosa S. Kim, Reg. No. 39,728; Jenny G. Ko, Reg. No. 44,190; Peter A. Luccarelli Jr., Reg. No. 29,750; James M. Markarian, Reg. No. 31,277; Jeffrey P. Morris, Reg. No. 25,307; Pasquale Musacchio, Reg. No. 36,876; John Musone, Reg. No. 44,961; Frank J. Nuzzi, Reg. No. 42,944; Donald B. Paschburg, Reg. No. 33,753; Laura M. Slenzak, Reg. No. 35,363; Daniel J. Staudt, Reg. No. 34,733; Erik C. Swanson, Reg. No. 40,194; Heather S. Vance, Reg. No. 39,033; and Michael J. Wallace, Reg. No. 44,486.

Send correspondence to:

Siemens Corporation
Intellectual Property Department
186 Wood Avenue South
Iselin, N.J. 08830

Direct telephone calls to:

Elsa Keller
Legal Administrator (908) 321-3026

I hereby declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

2002P03156US-050206

Full name of first joint inventor:	Karl Pichler
Inventor's signature:	
Date:	
Residence:	Santa Clara, CA
Citizenship:	Austria
Post Office Address:	444 Saratoga Avenue, #15C, Santa Clara, CA 95050
Full name of second joint inventor:	Kyle D. Firschknecht
Inventor's signature:	
Date:	
Residence:	Livermore, CA
Citizenship:	USA
Post Office Address:	566 Shelley Street, Livermore, CA 94550

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OIPE JC19
AUG 13 2002
PATENT & TRADEMARK OFFICE

MP #13

PATENT
Atty. Docket No.: 2002P03156US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Karl Pichler et al.

Application No.: 10/137,163

Filed: May 2, 2002

For: IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

Examiner: Unassigned
Group: Unassigned

I hereby certify that this correspondence is being deposited on this date with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: The Assistant Commissioner of Patents, Washington D.C. 20231 on the below date:

Date: August 9, 2002
By: Jeanette L. Taplin

RESPONSE TO NOTICE TO FILE MISSING PARTS

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

This is in response to the Notice to File Missing Parts mailed June 13, 2002, a copy of which is enclosed. Submitted herewith is the executed Declaration and Power of Attorney. An Assignment is being concurrently submitted to the Assignment Branch under separate cover.

Please charge the $130.00 surcharge for this response to our Deposit Account No. 19-2179. The Assistant Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment, to this deposit account. A duplicate copy of this sheet is enclosed.

Respectfully requested,

By: Tom George

Tom George
Registration No. 45,740
Attorney for Applicants
Tel: 650-694-5191
Fax: 650-968-4517

SIEMENS CORPORATION
Intellectual Property Department
186 Wood Avenue South
Iselin, New Jersey 08830
ATTENTION: Elsa Keller, IP Department
Telephone: (732) 321-3026

2002 AUG 13 PM 4:54



PATENT
Atty. Docket No.: 2002P03156US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Karl Pichler et al.

Application No.: 10/137,163

Filed: May 2, 2002

For: IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

Examiner: Unassigned
Group: Unassigned

I hereby certify that this correspondence is being deposited on this date with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: The Assistant Commissioner of Patents, Washington D.C. 20231 on the below date:

Date: August 9, 2002
By: Jeanette L. Taplin

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

This is in response to the Notice to File Corrected Application Papers in that the drawings did not have the appropriate margins. Enclosed herewith are the Formal Drawings consisting of eight (8) sheets.

We believe there is no fee due for this response, however, if the Assistant Commissioner does not agree, please charge Deposit Account No. **19-2179** for any fees or credit to any overpayments. A duplicate copy of this sheet is enclosed.

Respectfully requested,

SIEMENS CORPORATION
Intellectual Property Department
186 Wood Avenue South
Iselin, New Jersey 08830
ATTENTION: Elsa Keller, IP Department
Telephone: (732) 321-3026

By: Tom George

Tom George
Registration No. 45,740
Attorney for Applicants
Tel: 650-694-5191
Fax: 650-968-4517

20624 PATENT

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/137,163	05/02/2002	Karl Pichler	2002P03156US

CONFIRMATION NO. 1705

Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

OIPE JC79
AUG 13 2002
PATENT & TRADEMARK OFFICE

FORMALITIES LETTER

OC000000008284291

Date Mailed: 06/13/2002

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

10137163 050202

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(l) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Substitute drawings in compliance with 37 CFR 1.84 because:
    - drawing sheets do not have the appropriate margin(s) (see 37 CFR 1.84(g)). Each sheet must include a top margin of at least 2.5 cm. (1 inch), a left side margin of at least 2.5 cm. (1 inch), a right side margin of at least 1.5 cm. (5/8 inch), and a bottom margin of at least 1.0 cm. (3/8 inch);

Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$130** for a Large Entity

- **$130** Late oath or declaration Surcharge.

A copy of this notice <u>MUST</u> be returned with the reply.

Tsehai H

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

20243702, 08/15/2024

20E780 E97ZE10T

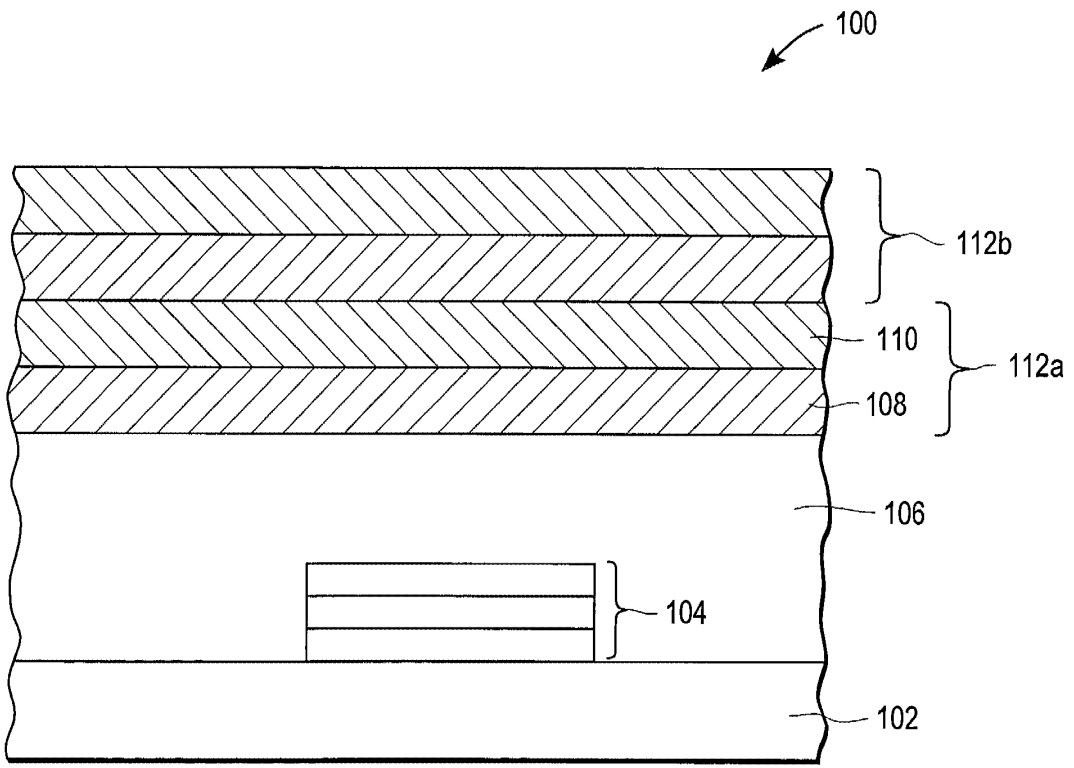


FIG. 1 (PRIOR ART)

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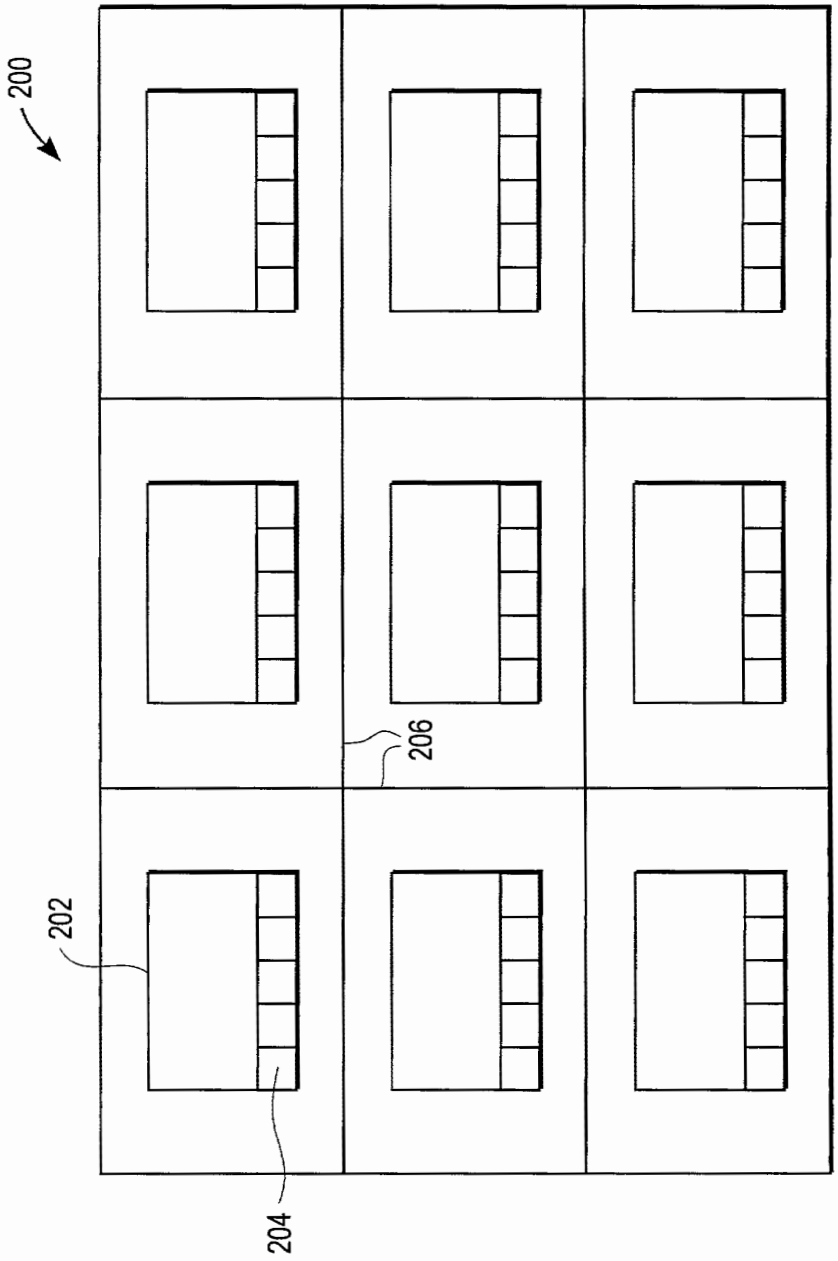


FIG. 2 (PRIOR ART)

DETAILED DESCRIPTION

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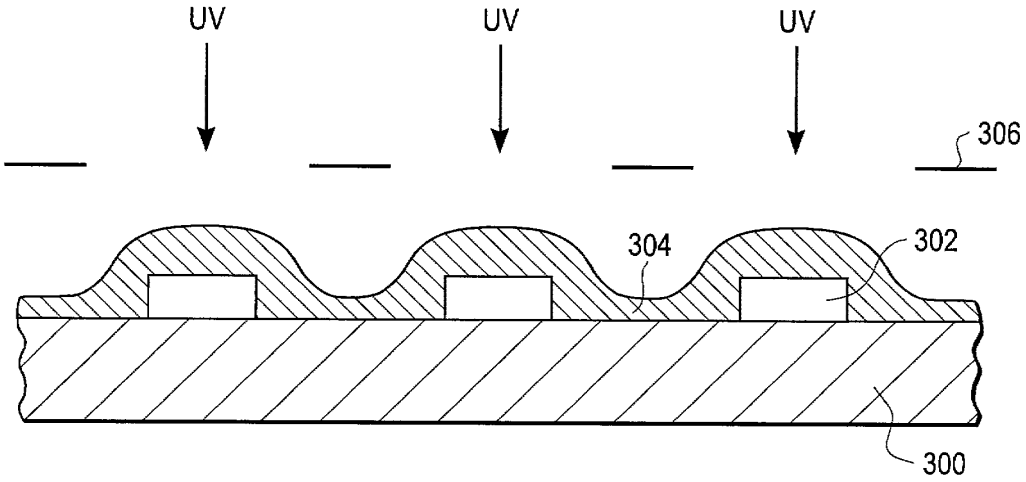


FIG. 3A

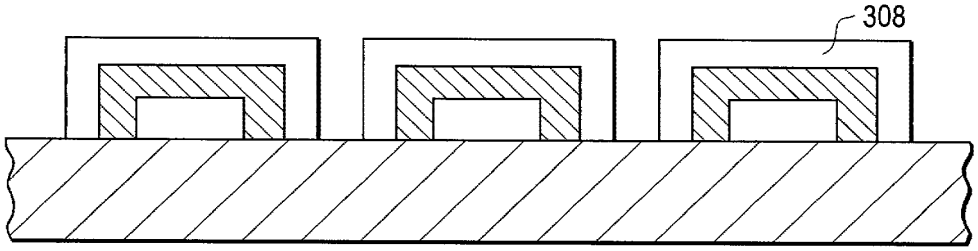


FIG. 3B

Petition Exhibit

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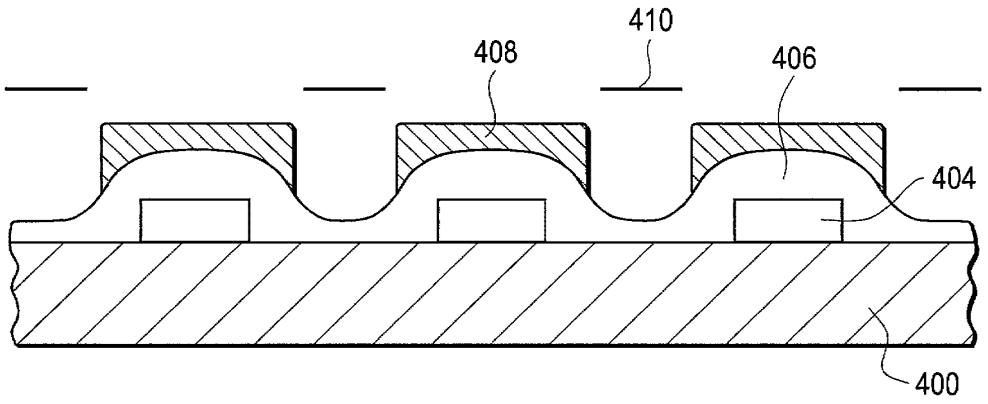


FIG. 4A

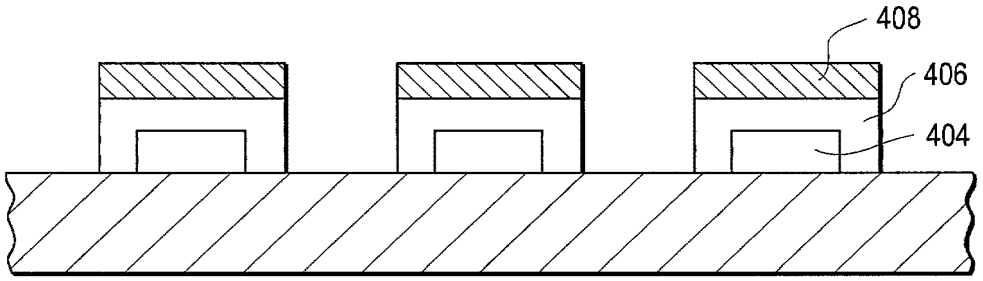


FIG. 4B

Docket: 52427.007

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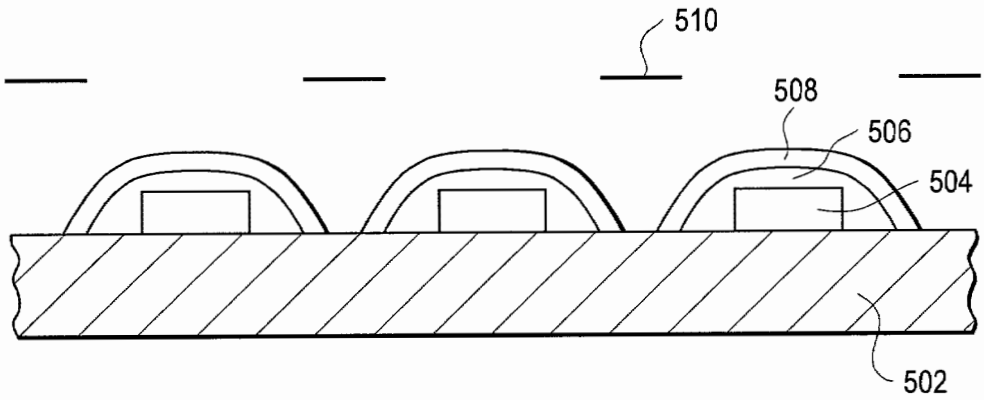


FIG. 5

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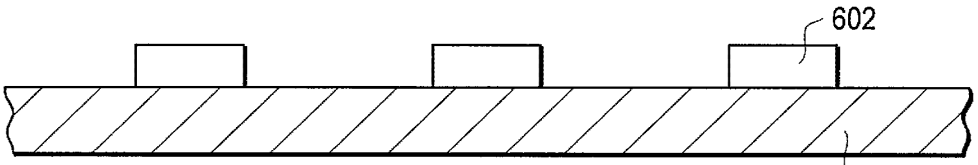


FIG. 6A

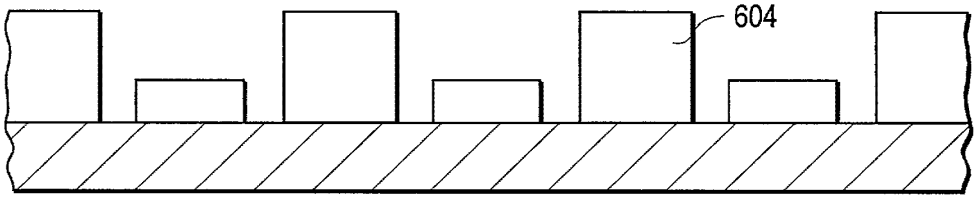


FIG. 6B

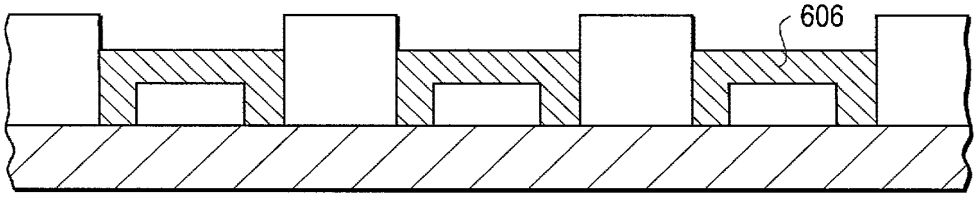


FIG. 6C

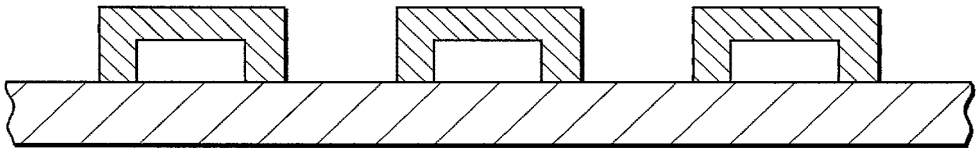


FIG. 6D

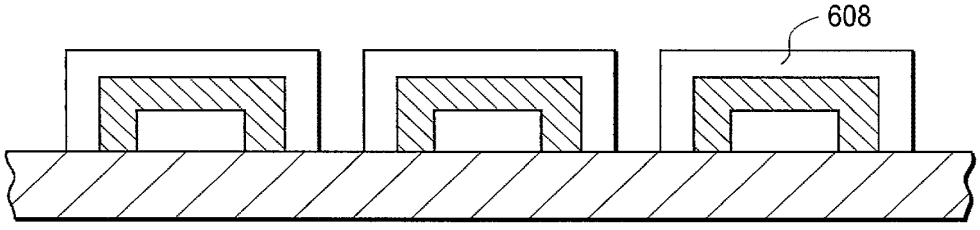


FIG. 6E

ADOBE EXHIBIT

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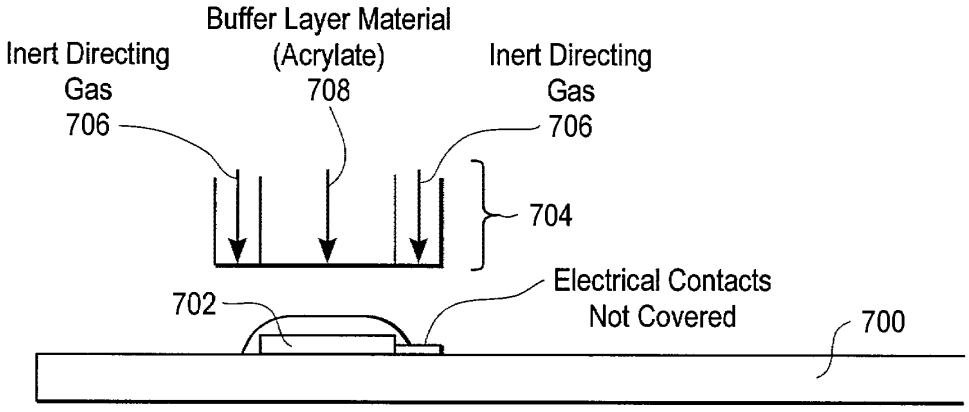


FIG. 7A

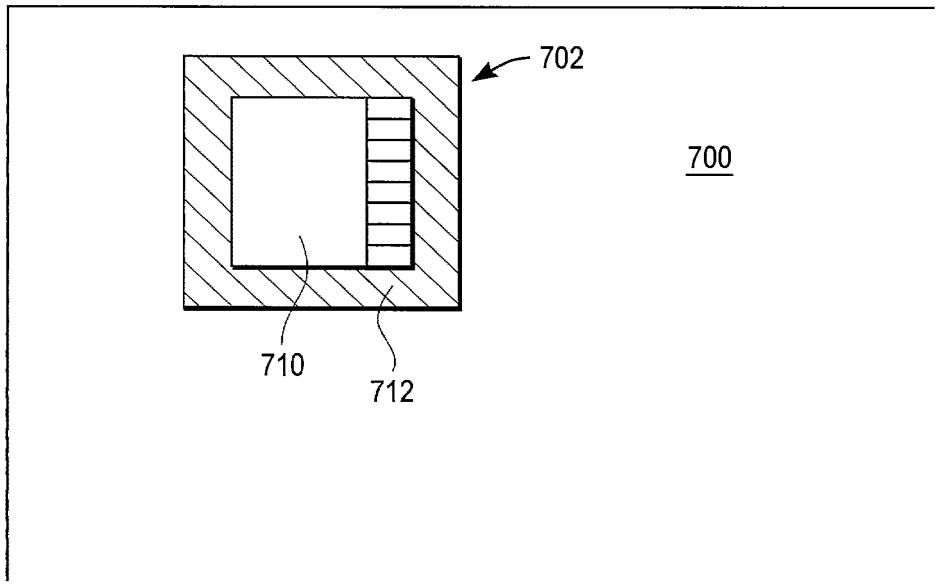


FIG. 7B

ANOTHER EXHIBIT

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AUG 13 2002

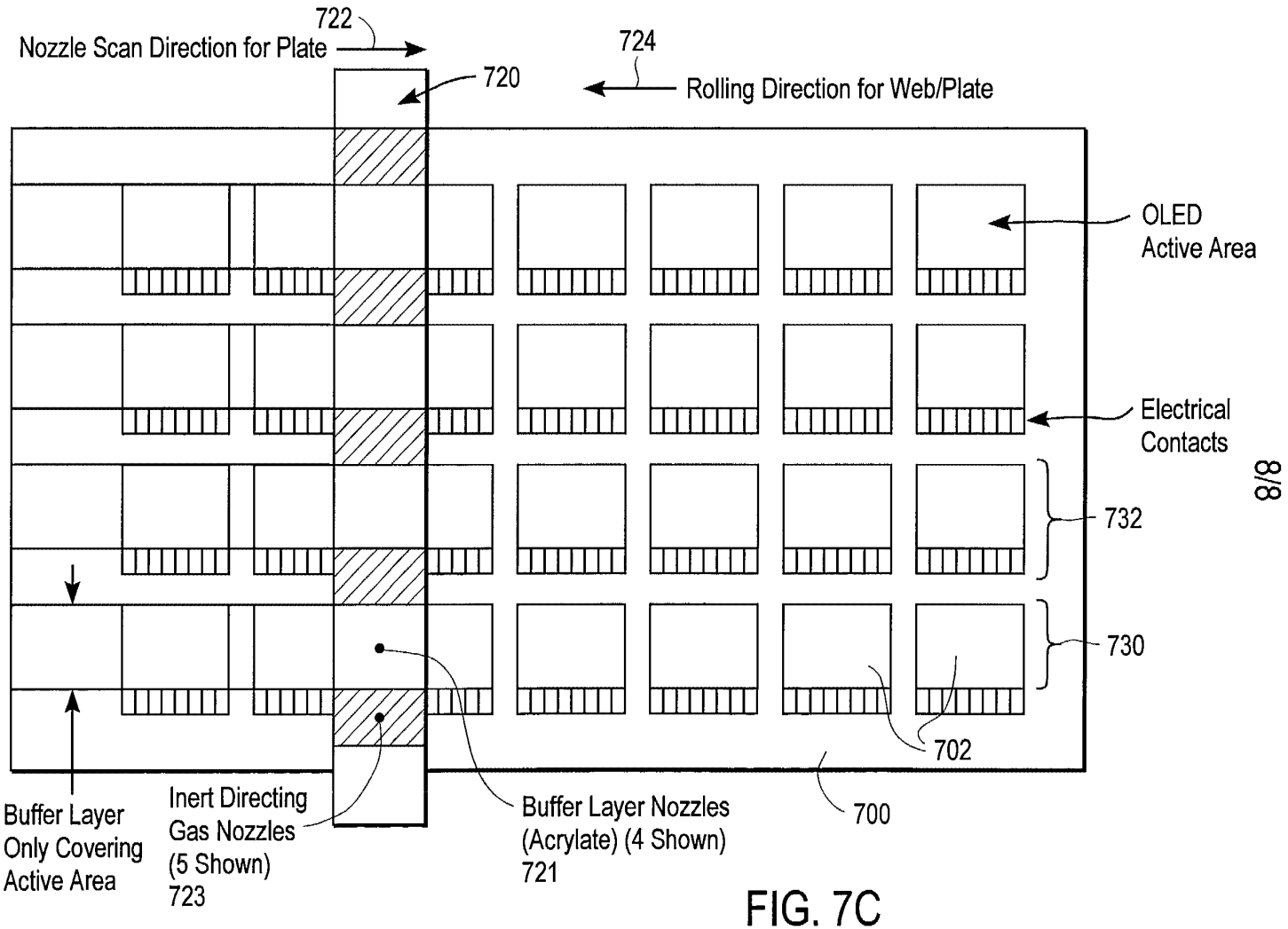


FIG. 7C

SDC EX. 1002 - 357/544

#3

Attorney Docket: 2002P03156US
Page -1-

OIPE JC19 AUG 13 2002 PATENT & TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

the specification of which (check one)
___is attached hereto.
_X_ was filed on **May 2, 2002** as Application Serial No. **10/137,163**
and was amended on _____ (if applicable)

List of Inventors: Karl Pichler and Kyle D. Firschknecht

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Codes, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			Priority claimed	
(Number)	(Country)	(Day/month/year filed)	Yes	No
(Number)	(Country)	(Day/month/year filed)	Yes	No

application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

2002P03156US

(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)
(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application listed below:

(Application Serial No.)	(Filing date)	(Status)

Power of Attorney: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

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I hereby declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Express Mail Label No. EV339744925US

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First Named Inventor:	Karl Pichler
Application No.:	10/137,163
Filing Date:	May 2, 2002
Group Art Unit:	2823
Examiner:	Lee, Hsien Ming
Title:	Improved Encapsulation for Organic Light Emitting Diodes Devices
Attorney Docket No.:	2002P03156US

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

RESPONSE PURSUANT TO 37 C.F.R. § 1.111

In response to the Office Action mailed February 19, 2004, please amend the above-identified application as follows:

AMENDMENTS TO THE CLAIMS begin on page 2 of this paper.

REMARKS/ARGUMENTS begin on page 10 of this paper.

AMENDMENTS TO THE CLAIMS:

1. (original): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices;

hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said device;

removing areas of the at least one planarization layer that are not hardened; and

selectively depositing at least one barrier layer over said hardened region.

2. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises spin coating.

3. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises flash evaporation.

4. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises evaporation.

5. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises blade coating.

6. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises roll coating.

7. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises dip coating.

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8. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises spray-coating.

9. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises one among a group, said group comprising: screen printing and ink jet printing.

10. (original): The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises one of a group, said group comprising flood-exposure of UV light through a mask and scanning a line-source of UV light through a mask.

11. (original): The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises exposure by UV light comprising an optical patterning system.

12. (original): The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises exposure by UV light comprising a UV-beam scanning system.

13. (original): The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer further comprises one of a group, said group comprising: cross-linking, patterned heat transfer system, patterned IR source, masked IR source, scanned IR source, patterned e-beam, masked e-beam and scanned e-beam.

14. (previously presented): The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises removing by thermal evaporation.

15. (original): The method as recited in Claim 14 wherein the step of removing by thermal evaporation further comprises applying a short high temperature pulse.

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16. (previously presented): The method as recited in Claim 15 wherein the step of applying a short high temperature pulse further comprises placing the plurality of devices onto a hotplate.

17. (original): The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises removing by pumping in a vacuum.

18. (original): The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises removing by thermal evaporation and pumping in a vacuum.

19. (original): The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises one of a group, said group comprising: washing, blowing away, rinsing, sonicing, and plasma.

20. (original): The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises a barrier layer comprising one of a group, said group comprising a dielectric, a metal, a metal-oxide and an alloy.

21. (original): The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing said barrier layer through a mask.

22. (original): The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing the barrier layer in a larger area than the planarization layer.

23. (original): The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing one of a group, said

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group comprising: metal-oxide, dielectric layer, SiOx, SiNx , SiOxNy, AlOx, AlNx, ITO, ZnOx, Al-doped ZnOx, metal film, and alloy film.

24. (previously presented): The method as recited in Claim 1 wherein said plurality of devices are a plurality of OLED displays and substantially only light emissive areas of said plurality of OLED displays are covered by the planarization layer and the barrier layer.

25. (original): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices wherein said planarization layer is deposited as an unpatterned liquid film;

selectively depositing at least one barrier layer over said planarization layer; and

removing said areas of unwanted planarization layer.

26. (original): The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises curing an organic layer selectively over the substrate.

27. (original): The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises curing an organic layer over the entire substrate.

28. (original): The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises evaporating a plurality of reactive organic molecules, said reactive organic molecules comprising a condensed conformal film on the substrate.

29. (original): The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises one of a group, said group comprising a

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Parylene coating of said organic layer over the substrate, and a plasma-assisted organic material deposition.

30. (original): The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises etching an organic layer.

31. (original): The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises etching an organic layer with a chemical etch process.

32. (original): The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises one of a group, said group comprising etching an organic layer with a plasma-assisted etching process, oxygen plasma, reactive ion-etch, anisotropic etch, laser assisted/based removal and laser ablation.

33. (original): The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises removing said organic layer.

34. (original): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

selectively depositing at least one planarization layer upon said devices; and

selectively depositing at least one barrier layer over said planarization layer.

35. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by ink jet of an organic layer.

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36. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by one of a group, said group comprising: screen printing of an organic layer and depositing by gas nozzle.

37. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing an organic layer through a shadow mask .

38. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by ink jet of said barrier layer.

39. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by screen printing of said barrier layer.

40. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises one of a group, said group comprising: depositing by shadow mask, sputtering, ink jet deposition, screen printing and evaporation.

41. (previously presented): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing a mask on top of said substrate, such that mask openings are placed on top of said devices;

depositing at least one planarization layer upon said mask and said plurality of devices;

removing said mask from said substrate; and

selectively depositing at least one barrier layer over said planarization layer.

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42. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises one of group, said group comprising: depositing a stamp mask, depositing a laminated film-mask, depositing a vacuum mask, magnetically held mask.

43. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing said mask such that said mask is in contact with said substrate.

44. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising a material substantially non-sticking to OLED substrate over the areas in between the active areas.

45. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising one of a group, said group comprising a metal, a ceramic, a plastic, a polymer, PTFE, and poly-siloxane.

46. (original): The method as recited in Claim 41 wherein the step of depositing at least one planarization layer further comprises depositing an organic layer over the entire mask.

47. (currently amended): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices; and

depositing at least one barrier layer over planarization layer wherein ~~at least one said step is accomplished in an inert atmosphere~~ one or both said layers are directed away from areas that should be free of deposition by an inert gas.

48. (original): The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is the step of depositing at least one planarization layer.

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49. (original): The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is the step of depositing at least one barrier layer.

50. (original): The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is both the step of depositing at least one planarization layer and the step of depositing at least one barrier layer.

Cancel claims 51-56.

57. (original): An electronic device, said device comprising:

a substrate;

a plurality of active areas disposed upon said substrate;

a plurality of planarization layers disposed on said substrate whereby said planarization layer cover substantially only said active areas; and

a plurality of barrier layers disposed on said substrate whereby said barrier layers cover substantially only said planarization layers.

58. (original): The electronic device as recited in Claim 57 wherein said electronic device is one of a group, said group comprising an OLED, an organic electronic circuit, an organic detector, an organic solar cell.

59. (new): The method as recited in Claim 47 wherein said inert gas is injected through an array of nozzles and at least one of said planarization layer and said barrier layer are deposited using said array of nozzles.

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REMARKS/ARGUMENTS

Claims 1-58 were considered by the Examiner. In the Office Action mailed February 19, 2004, claims 1-40 and 47-58 were rejected, and claims 41-46 were allowed. In this Response, claims 51-56 have been cancelled without prejudice, claim 47 has been amended, and claim 59 has been newly added. For the reasons set forth below, Applicants respectfully request reconsideration and allowance of all the pending claims.

Allowance of Claims

In the Office Action mailed February 19, 2004, the Examiner allowed claims 41-46.

Cancellation of Claims

Please cancel claims 51-56 without prejudice.

New Claim 59

New claim 59 depends from amended claim 47. The Applicants submit that the cited prior art references do not disclose or suggest the device encapsulation method claimed in new claim 59. Support for claim 59 is provided at, for example, page 13 of the Applicant's specification.

Section 103 Rejections

Claims 1-24:

(a) Claims 1-2, 10-12, and 19-24

Claims 1-2, 10-12, and 19-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2001/0052752 by Ghosh et al. ("*Ghosh*") in view of U.S. Patent No. 6,590,157 by Boroson et al. ("*Boroson*") ("the proposed combination").

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With respect to claim 1, the Applicants submit that the proposed combination does not disclose "hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said device" as recited in claim 1. On pages 3-4 of the Office Action, the Examiner concedes that *Ghosh* "do not teach hardening or curing said at least one planarization layer 21 in a patterned manner such that the hardened region substantially covers said devices 3." *Boroson* also does not disclose "hardening the planarization layer" as recited in claim 1." On page 4 of the Office Action, the Examiner refers to the "sealing material 20" of *Boroson* as a planarization layer; however, this "sealing material 20" is not a planarization layer since it is not used to interrupt the propagation of defects from one layer to another layer (see Applicants' specification at page 7, lines 16-21). Rather than being a planarization layer, the "sealing material 20" of *Boroson* is an adhesive that is used to bond the "encapsulation enclosure 30" to the "substrate 10". See *Boroson* at col. 8, lines 36-42. In addition, the "sealing material 20" of *Boroson* is not hardened "in a patterned manner such that the hardened region substantially covers said device" (underline added) as recited in claim 1. The "sealing material 20" of *Boroson* is not deposited "upon said devices" as specified by claim 1; rather, as shown in Fig. 5B of *Boroson*, the "sealing material 20" is deposited around the electronic device such that the sealing material surrounds the electronic device. See *Boroson* at col. 9, lines 29-30. Therefore, since the "sealing material 20" is deposited around the electronic device rather than upon the device, the "sealing material 20" does not cover the device.

In addition, the Applicants submit that the proposed combination does not disclose "removing areas of the at least one planarization layer that are not hardened" as recited in claim 1. Since the Examiner conceded that *Ghosh* does not disclose hardening the planarization layer (see, e.g., pages 3-4 of the Office Action), *Ghosh* cannot and does not disclose "removing areas of the at least one planarization layer that are not hardened" (underline added). In *Boroson*, there is no mention or suggestion that the non-hardened portion of the "sealing material 20" be removed. In fact, it would be nonsensical and impractical to remove the non-hardened portion of the "sealing material 20", and since it is desirable to have a strong bond between the "encapsulation enclosure 30" and the "substrate 10", all of the "sealing material 20" should be hardened such that there is no

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non-hardened portion. For the foregoing reasons, the proposed combination does not disclose "removing areas of the at least one planarization layer that are not hardened" as recited in claim 1.

Also, the Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Ghosh* and the *Boroson* references. The Examiner has the burden of showing that the cited references provide a suggestion to combine them. *See* MPEP 2142. References cannot be combined where the reference teaches away from their combination. *See* MPEP 2145. *Ghosh* teaches the use of thin films (i.e., the "first encapsulation layer 21", the "second encapsulation layer 22", etc.) to encapsulate the "display devices 3" and the use of thin films is cheaper and provides better device encapsulation than the conventional device encapsulation described in *Boroson* which is to employ a top glass (e.g., the "encapsulation enclosure 30" of *Boroson*) and an adhesive (e.g., the "sealing material 20" of *Boroson*) that bonds the top glass to the substrate. See, e.g., the Applicants specification at page 2, lines 5-14. By teaching thin-film device encapsulation, *Ghosh* teaches away from the conventional device encapsulation described in *Boroson* of curing the adhesive to bond the top glass to the substrate. See, e.g., *Boroson* at col. 9, lines 48-52. Therefore, there is no motivation to combine *Ghosh* and *Boroson*.

Claims 2, 10-12, 19-24 depend from claim 1. Accordingly, they are patentable over the proposed combination of *Ghosh* and *Boroson* for at least the reasons set forth above with respect to claim 1.

(b) Claims 3-9

Claims 3-9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ghosh* in view of *Boroson* and further in view of U.S. Patent No. 6,498,114 by Amundson et al. ("*Amundson*") and U.S. Patent Application Publication No. 2002/0155661 by Massingill et al. ("*Massingill*") ("the proposed combination").

With respect to claim 1, the Applicants submit that this proposed combination does not disclose "hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said device" nor "removing areas of

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the at least one planarization layer that are not hardened" as recited in claim 1. *Amundson* discloses patterning semiconductor films when manufacturing a transistor, but does not disclose or suggest either of those two elements of claim 1. *Massingill* discloses manufacturing multichip modules and deplating defective capacitors, but does not disclose or suggest either of those two elements of claim 1. Claims 3-9 depend from claim 1. Accordingly, these claims are patentable over the proposed combination of *Ghosh*, *Boroson*, *Amundson*, and *Massingill* for at least these reasons.

Also, the Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Ghosh*, *Boroson*, *Amundson*, and *Massingill* references. *Ghosh* and *Boroson* are not combinable for the reasons set forth above. In addition, *Amundson* and *Massingill* are not analogous prior art since they do not pertain to encapsulating the electronic device.

(c) Claims 13-16

Claims 13-16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ghosh* in view of *Boroson* and further in view of U.S. Patent No. 6,524,937 by Cheng et al. ("*Cheng*") ("the proposed combination").

With respect to claim 1, the Applicants submit that this proposed combination does not disclose "hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said device" nor "removing areas of the at least one planarization layer that are not hardened" as recited in claim 1. *Cheng* discloses forming metal features on a substrate for a transistor, but does not disclose or suggest either of those two elements of claim 1. Claims 13-16 depend from claim 1. Accordingly, these claims are patentable over the proposed combination of *Ghosh*, *Boroson*, and *Cheng* for at least these reasons.

Also, the Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Ghosh*, *Boroson*, and *Cheng* references. *Ghosh* and *Boroson* are not combinable for the reasons set forth above. In addition, *Cheng* is not analogous prior art since it does not pertain to encapsulation of the electronic device.

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(d) Claims 17-18

Claims 17-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ghosh* in view of *Boroson* and further in view of U.S. Patent No. 5,369,151 by Fujibayashi et al. ("*Fujibayashi*") ("the proposed combination").

With respect to claim 1, the Applicants submit that this proposed combination does not disclose "hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said device" nor "removing areas of the at least one planarization layer that are not hardened" as recited in claim 1. *Fujibayashi* discloses a resin composition for aqueous paints that has improved water dispersibility, bath stability, and pigment dispersibility, but does not disclose or suggest either of those two elements of claim 1. Claims 17-18 depend from claim 1. Accordingly, these claims are patentable over the proposed combination of *Ghosh*, *Boroson*, and *Fujibayashi* for at least these reasons.

Also, the Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Ghosh*, *Boroson*, and *Cheng* references. *Ghosh* and *Boroson* are not combinable for the reasons set forth above. In addition, *Fujibayashi* is not analogous prior art since it refers to resin for paints but does not pertain to encapsulating the electronic device.

Claims 25-33:

(a) Claims 25-27, 30-31, 33

Claims 25-27, 30-31, and 33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ghosh* in view of *Boroson* ("the proposed combination").

With respect to claim 25, the Applicants submit that the proposed combination does not disclose "selectively depositing at least one barrier layer over said planarization layer" as recited in claim 25. In *Ghosh*, the "second encapsulation layer 22" (in the Office Action, the Examiner refers to this layer as the "barrier layer"), is nonselectively

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deposited using either atomic layer epitaxy or atomic layer deposition. See, e.g., *Ghosh* at ¶0027. *Boroson* also does not disclose selectively depositing a barrier layer.

In addition, for the reasons described earlier, the Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Ghosh* and the *Boroson* references.

Claims 26-27, 30-31, and 33 depend from claim 25. Accordingly, they are patentable over the proposed combination of *Ghosh* and *Boroson* for at least the reasons set forth above with respect to claim 25.

(b) Claims 28-29, 32

Claims 28-29, and 32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ghosh* in view of *Boroson* and further in view of U.S. Patent No. 5,369,151 by Dimitrakopoulos et al. ("*Dimitrakopoulos*") ("the proposed combination").

With respect to claim 25, the Applicants submit that the proposed combination does not disclose "selectively depositing at least one barrier layer over said planarization layer" as recited in claim 25. *Dimitrakopoulos* discloses a method to pattern chemically sensitive organic thin film using a "photoresist layer 16", however, it does not disclose or suggest selectively depositing a barrier layer; in fact, *Dimitrakopoulos* does not even disclose applying a barrier layer. Claims 28-29 and 32 depend from claim 25. Accordingly, these claims are patentable over the proposed combination of *Ghosh*, *Boroson*, and *Dimitrakopoulos* for at least these reasons.

In addition, for the reasons described earlier, the Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Ghosh*, the *Boroson*, and the *Dimitrakopoulos* references. *Ghosh* and *Boroson* are not combinable for the reasons set forth above. In addition, *Dimitrakopoulos* is not analogous prior art since it pertains to covering a single organic layer with the "protective material 14" rather than covering/encapsulating an entire electronic device.

Claims 34-40:

PAGE 17/21 * RCVD AT 7/19/2004 6:32:48 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:6509684517 * DURATION (mm-ss):05-32

SDC EX. 1002 - 375/544

(a) Claims 34, 37

Claims 34 and 37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ghosh* in view of *Boroson* ("the proposed combination").

With respect to claim 34, the Applicants submit that the proposed combination does not disclose "selectively depositing at least one barrier layer over said planarization layer" as recited in claim 25. In *Ghosh*, the "second encapsulation layer 22" (in the Office Action, the Examiner refers to this layer as the "barrier layer"), is nonselectively deposited using either atomic layer epitaxy or atomic layer deposition. See, e.g., *Ghosh* at ¶0027. *Boroson* also does not disclose selectively depositing a barrier layer. For theses reasons, claim 34 is patentably distinguishable over the proposed combination. Claim 37 depends from claim 34. Accordingly, it is patentable over the proposed combination of *Ghosh* and *Boroson* for at least the reasons set forth above with respect to claim 34.

In addition, for the reasons described earlier, the Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Ghosh* and the *Boroson* references.

(b) Claims 35-36, 38-40

Claims 35-36, and 38-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ghosh* in view of *Boroson* and further in view of *Massingill*.

With respect to claim 34, the Applicants submit that the proposed combination does not disclose "selectively depositing at least one barrier layer over said planarization layer" as recited in claim 34. *Massingill* discloses manufacturing multichip modules and deplating defective capacitors, but does not disclose or suggest selectively depositing a barrier layer over the planarization layer. Claims 35-36 and 38-40 depend from claim 34. Accordingly, these claims are patentable over the proposed combination of *Ghosh*, *Boroson*, and *Massingill* for at least these reasons.

In addition, for the reasons described earlier, the Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Ghosh*, the *Boroson*, and the *Massingill* references.

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SDC EX. 1002 - 376/544

Claims 47-50:

Claims 47-50 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ghosh* in view of U.S. Patent Application Publication No. 2002/0094624 by Ahn et al. ("*Ahn*") ("the proposed combination").

With respect to claim 47, the Applicants submit that the proposed combination does not disclose "one or both said layers are directed away from areas that should be free of deposition by an inert gas" as recited in claim 47. On page 9 of the Office Action, the Examiner concedes that *Ghosh* does not disclose use of an inert gas. *Ahn* discloses injecting an inert gas between the injection of two other gasses to prevent residue of each material. *Ahn*, however, does not disclose using the inert gas to direct the layer material away from areas that should be free of deposition (example of areas that should be free of deposition are electrical contacts and scribe lines as described on page 13 of Applicants specification). For these reasons, claim 47 is patentably distinguishable over the proposed combination. Claims 48-50 depend from claim 47. Accordingly, these claims are patentable over the proposed combination for at least the reasons provided for claim 47.

In addition, the Applicants submit that the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine the *Ghosh* and the *Ahn* references. *Ahn* in nonanalogous prior art because it pertains to manufacturing a cell capacitor that has excellent leakage current, but it does not pertain to encapsulating an electronic device.

Claims 57-58:

Claims 57-58 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ghosh* combined with ordinary skill in the art ("proposed combination").

With respect to claim 57, the Applicants submit that the proposed combination does not disclose "a plurality of planarization layers disposed on said substrate" and "a plurality of barrier layers disposed on said substrate whereby said barrier layers cover

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substantially only said planarization layers" (underline added) as recited in claim 57. As the Examiner conceded on page 10 of the Office Action, *Ghosh* does not disclose multiple planarization layers. In addition, as shown in Figures 3 and 4, the "encapsulation layer 22" covers more than just the planarization layer since it also covers a significant portion of the substrate. For the foregoing reasons, claim 57 is patentably distinguishable over the proposed combination. Claim 58 depends from claim 57. Accordingly, this claim is patentable over the proposed combination for at least the reasons provided for claim 57.

On page 10 of the Office Action, the Examiner states that "one of the ordinary skilled in the art would have been motivated to repeat the deposition to form plural layers." However, speculation in hindsight to make the proposed combination because the proposed combination would supposedly be helpful is insufficient under the M.P.E.P. and governing Federal Circuit case law. If the Examiner is relying on "common knowledge" or "well known" art in support of his rationale for modifying the reference, the Examiner is requested to produce a reference in support of his position pursuant to M.P.E.P. § 2144.03. If the Examiner is relying on personal knowledge to supply the required motivation of suggestion to combine, Applicants respectfully request that the Examiner produce an affidavit supporting such facts pursuant to M.P.E.P. § 2144.03.

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CONCLUSION

Applicants have made an earnest attempt to place this case in condition for allowance. For the foregoing reasons, and for other reasons clearly apparent, Applicants respectfully request allowance of all pending claims.

If the Examiner feels that a telephone conference or an interview would advance prosecution of this Application in any manner, the undersigned attorney for Applicants stands ready to conduct such a conference at the convenience of the Examiner.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayments to Deposit Account No. 19-2179 of Siemens Corp.

Date: July 19, 2004

Respectfully requested,

By: Thomas George

SIEMENS CORPORATION
Intellectual Property Department
170 Wood Avenue South
Iselin, New Jersey 08830
ATTENTION: Elsa Keller, IP Department
Telephone: (732) 321-3026

Thomas George
Registration No. 45,740
Attorney for Applicants
Tel: 650-694-5191
Fax: 650-968-4517

PAGE 21/21 * RCVD AT 7/19/2004 6:32:48 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:6509684517 * DURATION (mm-ss):05-32

SDC EX. 1002 - 379/544

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]

I hereby certify that this correspondence is being:

____ deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

✓ transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (703) 872-9306.

7-19-2004
Date

Signature

Vicki Chia
Type or printed name of person signing certificate

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED
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JUL 19 2004
OFFICIAL

First Named Inventor:	Karl Pichler
Application No.:	10/137,163
Filing Date:	May 2, 2002
Group Art Unit:	2823
Examiner:	Lee, Hsien Ming
Title:	Improved Encapsulation for Organic Light Emitting Diodes Devices
Attorney Docket No.:	2002P03156US

Fee Only

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

RESPONSE PURSUANT TO 37 C.F.R. § 1.111

In response to the Office Action mailed February 19, 2004, please amend the above-identified application as follows:

AMENDMENTS TO THE CLAIMS begin on page 2 of this paper.

REMARKS/ARGUMENTS begin on page 10 of this paper.

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10/137163

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 52	Minus	** 58	=
Independent	* 6	Minus	*** 6	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SDC EX. 1002 - 381/544

Index of Claims

Application No	Applicant(s)
10/137,183	PICHLER ET AL.
Examiner	Art Unit
Hsien-Ming Lee	2823

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	2/12/04
	1	√
	2	√
	3	√
	4	√
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	9	√
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	38	√
	39	√
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Claim		Date
Final	Original	2/12/04
	51	√
	52	√
	53	√
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	57	√
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Claim		Date
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/137,163	05/02/2002	Karl Pichler	2002P03156US	1705

7590 09/24/2004

Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

SDC EX. 1002 - 383/544

Office Action Summary	Application No.	Applicant(s)	
	10/137,163	PICHLER ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50 and 57-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-24,34-50 and 57-59* is/are allowed.

6)☒ Claim(s) *25* is/are rejected.

7)☒ Claim(s) *26-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

9/21/2004

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. Applicant's cancellation to claims 51-56 is acknowledged. Thus, claims 1-50 and 57-59 are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Amundson et al. (US 6,498,114).

In re claim 25, Amundson et al., in Fig. 6 and related text, teach a method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

- fabricating a plurality of devices 40 (i.e. transistors) on a substrate 10;
- depositing at least one planarization layer 30 upon said devices 40; and
- selectively depositing at least one barrier layer 70' via screen-printing or ink-jet printing process (col. 6, lines 47-49 and 63-66; col. 7, lines 20-21 and 27-28).

Amundson et al., is silent as to removing unwanted areas of the at least one planarization layer. Amundson et al, however, do suggest a desirability of performing subsequent processing steps, such as making electrical connection with other conductive portions to complete the formation of a display (col. 7, lines 33-34).

Therefore, one of the ordinary skill in the art, at the time of the invention was made, would have been motivated to remove a portion of the planarization layer 30 to form an opening in the planarization layer located between two transistors and to deposit a conductive layer in the opening, since by this manner it would form a desired electrical connection to other conductive portions.

Allowable Subject Matter

4. Claims 1-24, 34-50 and 57-59 are allowed.

5. Claims 26-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record at least neither teach nor suggest *hardening* the planarization layer in a *patterned manner* such that the hardened region substantially covers the devices (claim 1); depositing the planarization layer comprising curing an *organic* layer *selectively* over the substrate (claim 26); *selectively* depositing at least one planarization layer upon the devices (claim 34); depositing a *mask* on top of the substrate such that mask *openings are placed on top* the devices (claim 41); one or both the barrier and planarization layers are *directed away* from areas that should be *free* of deposition by an *inert* gas (claim 47); and a plurality of planarization layers disposed on a substrate cover substantially only the active areas (claim 57).

Response to Arguments

7. Applicant's arguments filed 7/19/04 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection against claim 25 is made, as stated above.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Primary Examiner
Art Unit 2823

Sep. 21, 2004

HSIEN-MING LEE
PRIMARY EXAMINER
9/21/2004

Index of Claims

Application No.	Applicant(s)	
10/137,163	PICHLER ET AL.	
Examiner	**Art Unit**	
Hsien-Ming Lee	2823	

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

Claim		Date	Claim		Date	Claim		Date
Final	Original	9/21/04	Final	Original	9/21/04	Final	Original	
	1	=		51	=		101	
	2	=		52	=		102	
	3	=		53	=		103	
	4	=		54	=		104	
	5	=		55	=		105	
	6	=		56	=		106	
	7	=		57	=		107	
	8	=		58	=		108	
	9	=		59	=		109	
	10	=		60			110	
	11	=		61			111	
	12	=		62			112	
	13	=		63			113	
	14	=		64			114	
	15	=		65			115	
	16	=		66			116	
	17	=		67			117	
	18	=		68			118	
	19	=		69			119	
	20	=		70			120	
	21	=		71			121	
	22	=		72			122	
	23	=		73			123	
	24	=		74			124	
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	26	O		76			126	
	27	O		77			127	
	28	O		78			128	
	29	O		79			129	
	30	O		80			130	
	31	O		81			131	
	32	O		82			132	
	33	O		83			133	
	34	=		84			134	
	35	=		85			135	
	36	=		86			136	
	37	=		87			137	
	38	=		88			138	
	39	=		89			139	
	40	=		90			140	
	41	=		91			141	
	42	=		92			142	
	43	=		93			143	
	44	=		94			144	
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	49	=		99			149	
	50	=		100			150	

SDC EX. 1002 - 388/544

Search Notes	Application No.	Applicant(s)	
	10/137,163	PICHLER ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EASt attached (USPAT, USPG, EPO, JPO, IBM, Derwent)	9/21/2004	LEE

L Number	Hits	Search Text	DB	Time stamp
1	1	(plurality near3 devices) and (hardening with (planarization or planarized or planarizing)) and ((selective or selectively) with (deposition or depositing))	USPAT; US-PGPUB	2004/09/21 13:46
2	0	(plurality near3 devices) and (hardening with (planarization or planarized or planarizing)) and ((selective or selectively) with (deposition or depositing))	EPO; JPO; DERWENT; IBM_TDB	2004/09/21 13:46
3	6	(plurality near3 devices) and (hardening with (planarization or planarized or planarizing))	USPAT; US-PGPUB	2004/09/21 13:49
4	0	(plurality near3 devices) and (hardening with (planarization or planarized or planarizing))	EPO; JPO; DERWENT; IBM_TDB	2004/09/21 13:56
5	0	(plurality near3 devices) and (hardened with (planarization or planarized or planarizing))	EPO; JPO; DERWENT; IBM_TDB	2004/09/21 13:56
6	16	(plurality near3 devices) and (hardened with (planarization or planarized or planarizing))	USPAT; US-PGPUB	2004/09/21 14:02
7	378	(plurality near3 devices) and (planarization or planarized or planarizing) and ((selective or selectively) with (deposition or depositing or deposited))	USPAT; US-PGPUB	2004/09/21 14:40
8	265	((plurality near3 devices) and (planarization or planarized or planarizing) and ((selective or selectively) with (deposition or depositing or deposited))) and @ad<20020502	USPAT; US-PGPUB	2004/09/21 14:41
9	0	(plurality near3 devices) and (planarization or planarized or planarizing) and ((selective or selectively) with (deposition or depositing or deposited))	EPO; JPO; DERWENT; IBM_TDB	2004/09/21 14:21
10	15	(plurality near3 OLED) and (planarization or planarized or planarizing) and ((selective or selectively) with (deposition or depositing or deposited))	USPAT; US-PGPUB	2004/09/21 14:44
11	8	((plurality near3 OLED) and (planarization or planarized or planarizing) and ((selective or selectively) with (deposition or depositing or deposited))) and @ad<20020502	USPAT; US-PGPUB	2004/09/21 15:05
12	0	(plurality near3 OLED) and (planarization or planarized or planarizing) and ((selective or selectively) with (deposition or depositing or deposited))	EPO; JPO; DERWENT; IBM_TDB	2004/09/21 14:44
13	34	((hardened or hardening) same (planarization or planarizing or planarized)) and ((selective or selectively) with (depositing or deposition)) and @ad<20020502	USPAT; US-PGPUB	2004/09/21 15:27
14	1	((hardened or hardening) same (planarization or planarizing or planarized)) and ((selective or selectively) with (depositing or deposition))	EPO; JPO; DERWENT; IBM_TDB	2004/09/21 15:10
15	633	((selective or selectively) with (depositing or deposition) with ((planarization or planarized or planrizing) or barrier)) and @ad<20020502	USPAT; US-PGPUB	2004/09/21 16:00

17	235	(((selective or selectively) with (depositing or deposition) with ((planarization or planarized or planrizing) or barrier)) and @ad<20020502) and (plurality)	USPAT; US-PGPUB	2004/09/21 15:32
16	26	(((selective or selectively) with (depositing or deposition) with ((planarization or planarized or planrizing) or barrier)) and @ad<20020502) and (plurality near3 (devices or OLED))	USPAT; US-PGPUB	2004/09/21 15:32
18	209	((((selective or selectively) with (depositing or deposition) with ((planarization or planarized or planrizing) or barrier)) and @ad<20020502) and (plurality)) not ((((selective or selectively) with (depositing or deposition) with ((planarization or planarized or planrizing) or barrier)) and @ad<20020502) and (plurality near3 (devices or OLED)))	USPAT; US-PGPUB	2004/09/21 15:32
19	164	((selective or selectively) with (depositing or deposition) with ((planarization or planarized or planrizing) or barrier))	EPO; JPO; DERWENT; IBM_TDB	2004/09/21 15:42
20	2645	((selective or selectively) adj (depositing or deposition or deposited)) and (planarization or planarized or planrizing or barrier) and @ad<20020502	USPAT; US-PGPUB	2004/09/21 16:01
21	636	((selective or selectively) adj (depositing or deposition or deposited)) same (planarization or planarized or planrizing or barrier) and @ad<20020502	USPAT; US-PGPUB	2004/09/21 16:02
22	282	(((selective or selectively) adj (depositing or deposition or deposited)) same (planarization or planarized or planrizing or barrier) and @ad<20020502) and plurality	USPAT; US-PGPUB	2004/09/21 16:02
23	78	(((selective or selectively) adj (depositing or deposition or deposited)) same (planarization or planarized or planrizing or barrier) and @ad<20020502) and (plurality with (devices or OLED or units or elements))	USPAT; US-PGPUB	2004/09/21 16:05
24	37	(((selective or selectively) adj (depositing or deposition or deposited)) same (planarization or planarized or planrizing or barrier) and @ad<20020502) and (plurality with (transistors))	USPAT; US-PGPUB	2004/09/21 16:05

US-PAT-NO: 6448644

DOCUMENT-IDENTIFIER: US 6448644 B1

TITLE: Flip chip assembly with via interconnection

---------- KWIC ---------

Detailed Description Text - DETX (16):
FIGS. 5A through 5E illustrate a process for producing another embodiment of the flip chip assembly according to the present invention. Referring now to FIG. 5A, an integrated circuit chip 501 similar to that in example 1 is cleaned in an alkaline solution containing 0.05 M phosphoric acid at room temperature (25 degrees C.) with immersion time of 1 minute. The chip is then thoroughly rinsed in distillated water to ensure there is no residue left on the surface of integrated circuit chip. A multi-layered thin film 503 having the structure of chromium (500 A)/copper (700 A)/gold (1000 A), respectively, was **selectively deposited** on the terminal pads 502 to serve a barrier and adhesive layer.

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X transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (703) 872-9306.

Jan. 24, 2005
Date

Thomas George
Signature

THOMAS GEORGE
Type or printed name of person signing certificate

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Karl Pichler
Application No.:	10/137,163
Filing Date:	May 2, 2002
Group Art Unit:	2823
Examiner:	Lee, Hsien Ming
Title:	Improved Encapsulation for Organic Light Emitting Diodes Devices
Attorney Docket No.:	2002P03156US

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

RESPONSE PURSUANT TO 37 C.F.R. § 1.111

In response to the Office Action mailed September 24, 2004, please amend the above-identified application as follows:

AMENDMENTS TO THE CLAIMS begin on page 2 of this paper.

REMARKS/ARGUMENTS begin on page 10 of this paper.

Attorney Docket No.: 2002P03156US

AMENDMENTS TO THE CLAIMS:

1. (original): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices;

hardening said at least one planarization layer in a patterned manner such that the hardened region substantially covers said device;

removing areas of the at least one planarization layer that are not hardened; and

selectively depositing at least one barrier layer over said hardened region.

2. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises spin coating.

3. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises flash evaporation.

4. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises evaporation.

5. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises blade coating.

6. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises roll coating.

7. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises dip coating.

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8. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises spray-coating.

9. (original): The method as recited in Claim 1 wherein said step of depositing at least one planarization layer comprises one among a group, said group comprising: screen printing and ink jet printing.

10. (original): The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises one of a group, said group comprising flood-exposure of UV light through a mask and scanning a line-source of UV light through a mask.

11. (original): The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises exposure by UV light comprising an optical patterning system.

12. (original): The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer in a patterned manner comprises exposure by UV light comprising a UV-beam scanning system.

13. (original): The method as recited in Claim 1 wherein the step of hardening said at least one planarization layer further comprises one of a group, said group comprising: cross-linking, patterned heat transfer system, patterned IR source, masked IR source, scanned IR source, patterned e-beam, masked e-beam and scanned e-beam.

14. (previously presented): The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises removing by thermal evaporation.

15. (original): The method as recited in Claim 14 wherein the step of removing by thermal evaporation further comprises applying a short high temperature pulse.

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16. (previously presented): The method as recited in Claim 15 wherein the step of applying a short high temperature pulse further comprises placing the plurality of devices onto a hotplate.

17. (original): The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises removing by pumping in a vacuum.

18. (original): The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises removing by thermal evaporation and pumping in a vacuum.

19. (original): The method as recited in Claim 1 wherein the step of removing areas of the at least one planarization layer that are not hardened comprises one of a group, said group comprising: washing, blowing away, rinsing, sonicing, and plasma.

20. (original): The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises a barrier layer comprising one of a group, said group comprising a dielectric, a metal, a metal-oxide and an alloy.

21. (original): The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing said barrier layer through a mask.

22. (original): The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing the barrier layer in a larger area than the planarization layer.

23. (original): The method as recited in Claim 1 wherein the step of selectively depositing at least one barrier layer further comprises depositing one of a group, said

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group comprising: metal-oxide, dielectric layer, SiOx, SiNx , SiOxNy, AlOx, AlNx, ITO, ZnOx, Al-doped ZnOx, metal film, and alloy film.

24. (previously presented): The method as recited in Claim 1 wherein said plurality of devices are a plurality of OLED displays and substantially only light emissive areas of said plurality of OLED displays are covered by the planarization layer and the barrier layer.

25. (original): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices wherein said planarization layer is deposited as an unpatterned liquid film;

selectively depositing at least one barrier layer over said planarization layer; and

removing said areas of unwanted planarization layer.

26. (original): The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises curing an organic layer selectively over the substrate.

27. (original): The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises curing an organic layer over the entire substrate.

28. (original): The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises evaporating a plurality of reactive organic molecules, said reactive organic molecules comprising a condensed conformal film on the substrate.

29. (original): The method as recited in Claim 25 wherein said step of depositing at least one planarization layer further comprises one of a group, said group comprising a

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Parylene coating of said organic layer over the substrate, and a plasma-assisted organic material deposition.

30. (original): The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises etching an organic layer.

31. (original): The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises etching an organic layer with a chemical etch process.

32. (original): The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises one of a group, said group comprising etching an organic layer with a plasma-assisted etching process, oxygen plasma, reactive ion-etch, anisotropic etch, laser assisted/based removal and laser ablation.

33. (original): The method as recited in Claim 25 wherein the step of removing said areas of unwanted planarization layer further comprises removing said organic layer.

34. (original): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

selectively depositing at least one planarization layer upon said devices; and

selectively depositing at least one barrier layer over said planarization layer.

35. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by ink jet of an organic layer.

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36. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing by one of a group, said group comprising: screen printing of an organic layer and depositing by gas nozzle.

37. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one planarization layer further comprises depositing an organic layer through a shadow mask .

38. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by ink jet of said barrier layer.

39. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises depositing by screen printing of said barrier layer.

40. (original): The method as recited in Claim 34 wherein the step for selectively depositing at least one barrier layer further comprises one of a group, said group comprising: depositing by shadow mask, sputtering, ink jet deposition, screen printing and evaporation.

41. (previously presented): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing a mask on top of said substrate, such that mask openings are placed on top of said devices;

depositing at least one planarization layer upon said mask and said plurality of devices;

removing said mask from said substrate; and

selectively depositing at least one barrier layer over said planarization layer.

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42. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises one of group, said group comprising: depositing a stamp mask, depositing a laminated film-mask, depositing a vacuum mask, magnetically held mask.

43. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing said mask such that said mask is in contact with said substrate.

44. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising a material substantially non-sticking to OLED substrate over the areas in between the active areas.

45. (original): The method as recited in Claim 41 wherein the step of depositing said mask further comprises depositing a mask, said mask comprising one of a group, said group comprising a metal, a ceramic, a plastic, a polymer, PTFE, and poly-siloxane.

46. (original): The method as recited in Claim 41 wherein the step of depositing at least one planarization layer further comprises depositing an organic layer over the entire mask.

47. (previously presented): A method of encapsulating a plurality of devices fabricated upon a substrate, the steps of said method comprising:

fabricating a plurality of devices on a substrate;

depositing at least one planarization layer upon said devices; and

depositing at least one barrier layer over planarization layer wherein one or both said layers are directed away from areas that should be free of deposition by an inert gas.

48. (original): The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is the step of depositing at least one planarization layer.

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49. (original): The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is the step of depositing at least one barrier layer.

50. (original): The method as recited in Claim 47 wherein the at least one said step accomplished in an inert atmosphere is both the step of depositing at least one planarization layer and the step of depositing at least one barrier layer.

Cancel claims 51-56.

57. (original): An electronic device, said device comprising:

a substrate;

a plurality of active areas disposed upon said substrate;

a plurality of planarization layers disposed on said substrate whereby said planarization layer cover substantially only said active areas; and

a plurality of barrier layers disposed on said substrate whereby said barrier layers cover substantially only said planarization layers.

58. (original): The electronic device as recited in Claim 57 wherein said electronic device is one of a group, said group comprising an OLED, an organic electronic cir*Cuit*, an organic detector, an organic solar cell.

59. (new): The method as recited in Claim 47 wherein said inert gas is injected through an array of nozzles and at least one of said planarization layer and said barrier layer are deposited using said array of nozzles.

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SDC EX. 1002 - 401/544

REMARKS/ARGUMENTS

Claims 1-58 were considered by the Examiner. In the Office Action mailed September 24, 2004, claims 1-24, 34-50, and 57-59 were allowed; claim 25 was rejected; and claims 26-33 were objected to. For the reasons set forth below, Applicants respectfully request reconsideration and allowance of all the pending claims.

Allowance of Claims

In the Office Action mailed September 24, 2004, the Examiner allowed claims 1-24, 34-50, and 57-59.

Objection to Claims

In the Office Action mailed September 24, 2004, the Examiner objected to claims 26-33 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Section 103 Rejections

Claim 25 is rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,498,114 by Amundson et al. ("*Amundson*") combined with the knowledge of those skilled in the art ("the proposed combination").

With respect to claim 25, the Applicants submit that the proposed combination does not disclose the following elements: (1) "depositing at least one planarization layer upon said devices wherein said planarization layer is deposited as an unpatterned liquid film", (2) "selectively depositing at least one barrier layer over said planarization layer", and (3) "removing said areas of unwanted planarization layer" as recited in claim 25.

With regards to (1), the Applicants submit that the proposed combination does not disclose that the planarization layer is deposited upon "devices". In Amundson, the "gate dielectric 30" is deposited on a portion of the device (i.e., transistor) rather than on the complete device; that is, the "gate dielectric 30" is deposited on the "gate electrode 40"

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which is only a portion of the transistor and not on a complete transistor since the complete transistor also includes the "source 50" and the "drain 60". *See, e.g.,* Amundson at col. 6, lns. 44-47, 53-55. In fact, Amundson states that all three components (i.e., the gate 40, the source 50, and the drain 60) are required to make a complete transistor (i.e., device). *See, e.g.,* Amundson at col. 6, lns. 53-55. In addition, the proposed combination does not disclose that the "planarization layer is deposited as an unpatterned liquid film." There is no mention in Amundson that the "gate electrode 30" is a "liquid film" and the Examiner does not specify where in Amundson it is disclosed that the "gate electrode 30" is a "liquid film".

With regards to (2), the Applicants submit that the proposed combination does not disclose "selectively depositing at least one barrier layer over said planarization layer". The "patterned mask 70'" is not a "barrier layer"; the function of a "barrier layer" is to keep out oxygen and moisture, while, on the other hand, the function of the "patterned mask 70" is to pattern the "semiconductor layer 20". *See, e.g.,* Amundson at col. 6, lns. 50-53. Another difference is that the "barrier layer" is present in the resulting device, while in Amundson, the "patterned mask 70'" is removed and is not part of the eventual device. *See, e.g.,* Amundson at col. 6, lns. 52-55.

With regards to (3), the Applicants submit that the proposed combination does not disclose "removing said areas of unwanted planarization layer". On page 2 of the Office Action, the Examiner concedes that *Amundson* "is silent as to removing unwanted areas of the at least planarization layer." The Examiner combines Amundson with the knowledge of one skilled in the art to assert that this element is obvious. The Applicants assert that one skilled in the art would not remove the "gate dielectric 30" since removal of the dielectric decreases electrical isolation of individual transistors thus increasing the likelihood that the transistor array will fail. *See, e.g.,* Amundson at col. 6, lns. 47-49. As MPEP 2145 states, there is no motivation to combine references where the reference teaches away from their combination. Amundson teaches away from removing the dielectric layer since the dielectric layer is needed to separate individual transistors. Thus the Examiner has not established a prima facie case of obviousness since the Examiner has not provided an adequate suggestion to combine Amundson with the knowledge of one skilled in the art.

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In addition, the Applicants assert that *Amundson* is not analogous prior art since it does not pertain to encapsulating the electronic device (i.e, transistor), but rather Amundson merely pertains to formation of an electronic device without regard to encapsulating it.

For the foregoing reasons, the Applicants assert that claim 25 is patentable over the proposed combination of Amundson and the knowledge of one skilled in the art. Claims 26-33 depend from claim 25. Accordingly, they are patentable over the proposed combination at least the reasons set forth above with respect to claim 25.

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SDC EX. 1002 - 404/544

Attorney Docket No.: 2002P03156US

CONCLUSION

Applicants have made an earnest attempt to place this case in condition for allowance. For the foregoing reasons, and for other reasons clearly apparent, Applicants respectfully request allowance of all pending claims.

If the Examiner feels that a telephone conference or an interview would advance prosecution of this Application in any manner, the undersigned attorney for Applicants stands ready to conduct such a conference at the convenience of the Examiner.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayments to Deposit Account No. 19-2179 of Siemens Corp.

Respectfully requested,

Date: January 24, 2005

By: Thomas George

CUSTOMER NUMBER 28524
SIEMENS CORPORATION
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Iselin, New Jersey 08830
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PAGE 17/17 * RCVD AT 1/24/2005 11:49:39 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:6509684517 * DURATION (mm-ss):04-18

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Jan. 24, 2005
Date

Thomas George
Signature

THOMAS GEORGE
Type or printed name of person signing certificate

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Karl Pichler
Application No.:	10/137,163
Filing Date:	May 2, 2002
Group Art Unit:	2823
Examiner:	Lee, Hsien Ming
Title:	Improved Encapsulation for Organic Light Emitting Diodes Devices
Attorney Docket No.:	2002P03156US

PETITION FOR EXTENSION OF TIME

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant(s) hereby petition(s) for a one month extension of time to respond to the Office Action mailed on September 24, 2004. This one month extension will extend the due date from December 24, 2004 to January 24, 2005.

Attorney Docket No.: 2002P03156US

Please charge the extension fee of $120.00 to Deposit Account No. 19-2179. A duplicate copy of this sheet is enclosed.

Date: Jan. 24, 2005

Respectfully requested,

CUSTOMER NUMBER – 28524
SIEMENS CORPORATION
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Serial No. 60/609,101

Applicant requests favorable action on this petition.

Respectfully submitted,

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1-19-05

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2823

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope address to:
Commissioner for Patents and Trademarks, P.O. Box 1450, Alexandria, VA 22313-1450

By: Raquel C. West 01/26/05 Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Karl Pichler
Application No.:	10/137,163
Filing Date:	May 2, 2002
Group Art Unit:	2823
Examiner:	Lee, Hsien Ming
Title:	Improved Encapsulation for Organic Light Emitting Diodes Devices
Attorney Docket No.:	2002P03156US

Mail Stop IDS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

[ ] under 37 CFR 1.97 (b), or
(Within three months of filing national application; or date of entry of international application; or before mailing date of first office action on the merits; whichever occurs last)

[X] under 37 CFR 1.97 (c) together with either a:
[ ] Certification under 37 CFR 1.97 (e), or
[X] A $180.00 fee under 37 CFR 1.17 (p) authorized to be charged to Deposit Account 19-2179. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 19-2179 pursuant to 37 CFR 1.25.
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

[ ] under 37 CFR 1.97 (d) together with a:
[ ] Certification under 37 CFR 1.97 (e), and
[ ] a petition under 37 CFR 1.97 (d) (2) (ii), required with fee under 37 CFR 1.17(i)(1)
(Filed after final action or notice of allowance, whichever occurs first, but on or before payment of the issue fee)

[ ] under 37 CFR 1.97 (i)
[ ] Filed after payment of issue fee, but before grant of patent - No fee or certification required

Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Citation together with copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

[ ] A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content that is given on the attached sheet or by the enclosed English-language search report.

SDC EX. 1002 - 409/544

[ ] The undersigned hereby certifies under 37 CFR 1.97(e)(1) that each item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; or

[ ] The undersigned certifies under 37 CFR 1.97(e)(2) that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 1.56(c) more than three months prior to the filing of the information disclosure statement.

[ ] Applicant does not believe any fee is due. However, at any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 19-2179 pursuant to 37 CFR 1.25. A duplicate copy of this sheet is enclosed.

The filing of this information disclosure statement shall not be construed as a representation that a search has been made or that no other material information exists. Further, the filing of this information disclosure statement shall not be construed as an admission against interest in any manner or as an admission that the information cited is, or is considered to be material to patentability.

It is requested that the information disclosed herein be made of record in this application. Copies of the references are included herewith, along with a copy of the PCT International Search Report.

PLEASE MAIL CORRESPONDENCE TO:

Siemens Corporation
Customer No. 28524
Attn: Elsa Keller, Legal Administrator
170 Wood Avenue South
Iselin, NJ 08830

Respectfully submitted,

Thomas George, Reg. No. 45,740
Attorney(s) for Applicant(s)
Telephone: 650-694-5191
Date: January 25, 2005

SDC EX. 1002 - 410/544

OIPE JC32
JAN 31 2005
PATENT & TRADEMARK OFFICE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/137,163
Filing Date	05/02/2002
First Named Inventor	Pichler, et al.
Group Art Unit	1775
Examiner Name	Lee, Hsien Ming
Attorney Docket Number	2002P03156US

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	6,268,695		Affinito	07/31/01	
	2	6,522,067		Graff, et al.	02/18/03	
	3	6,720,203		Carica, et al.	04/13/04	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

PATENT APPLICATION FEE DETERMINATION RECORD

Effective December 8, 2004

10/137163

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	150.00	OR	BASIC FEE	300.00
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1)		(Column 2)	(Column 3)
1-24-05	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 53	Minus	** 58	=
Independent	* 6	Minus	*** 8	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 03/31/2005

Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

EXAMINER	
LEE, HSIEN MING	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/31/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/137,163	05/02/2002	Karl Pichler	2002P03156US	1705

TITLE OF INVENTION: ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	06/30/2005

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 12/04) Approved for use through 04/30/2007.

SDC EX. 1002 - 413/544

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 03/31/2005

Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/137,163	05/02/2002	Karl Pichler	2002P03156US	1705

TITLE OF INVENTION: ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	06/30/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
LEE, HSIEN MING	2823	438-026000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):
- ☐ A check in the amount of the fee(s) is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

SDC EX. 1002 - 414/544

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/137,163	05/02/2002	Karl Pichler	2002P03156US	1705

7590 03/31/2005

Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/31/2005

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571) 272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (Rev. 12/04) Approved for use through 04/30/2007.

SDC EX. 1002 - 415/544

H·A

Notice of Allowability	Application No.	Applicant(s)	
	10/137,163	PICHLER ET AL.	
	Examiner	Art Unit	
	Hsien-ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *1/24/2005*.

2. ☒ The allowed claim(s) is/are *1-50 and 57-59*.

3. ☒ The drawings filed on *13 August 2002* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 013105, 020904 & 122303
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

HSIEN-MING LEE
PRIMARY EXAMINER
3/22/2005

SDC EX. 1002 - 416/544

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 1/24/2005 have been fully considered and are persuasive. The 103(a) rejection against claims 25 has been withdrawn.

Examiner's Amendment

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Thomas George (Reg. No. 45,740) on March 22, 2005.

3. The application has been amended as follows:

In claim 9, at line 2, **delete** "one among a group, said group comprising:" and at line 3, **replace** "and" with -- or --.

In claim 10, at line 2, **delete** "one of a group, said group comprising" and at line 3, **replace** "and" with -- or --.

In claim 13, at line 2, **delete** "one of a group, said group comprising:" and at line 4, **replace** "and" with -- or --.

In claim 19, at lines 2-3, **delete** "one of a group, said group comprising:" and at line 3, **replace** "and" with -- or --.

In claim 20, at lines 2-3, **delete** "comprising one of a group, said group" and at line 3, **replace** "and" with -- or --.

In claim 23, at lines 2-3, **delete** " one of a group, said group comprising:" and at line 4, **replace** "and" with -- or --.

In claim 29, at line 2, **delete** "one of a group, said group comprising" and at line 3, **replace** "and" with -- or --.

In claim 32, at lines 2-3, **delete** "one of a group, said group comprising" and at line 4, **replace** "and" with -- or --.

In claim 36, at lines 2-3, **delete** "one of a group, said group comprising :" and at line 3, **replace** "and" with -- or --.

In claim 40, at lines 2-3, **delete** "one of a group, said group comprising :" and at line 4, **replace** "and" with -- or --.

In claim 42, at line 2, **delete** "one of a group, said group comprising :" and at line 3, **add** -- or – before "magnetically."

In claim 45, at lines 2-3, **delete** "one of a group, said group comprising" and at line 3, **replace** "and" with -- or --.

In claim 58, at line 2, **replace** "is one of a group, said group comprising" with – comprises --; at line 2, **replace** "cirCuit" with – circuit --; and at line 3, **replace** "detector," with – detector or --.

Allowable Subject Matter

4. Claims 1-50 and 57-59 are allowed.

5. The following is an examiner's statement of reasons for allowance: see previous Office Action, paragraph 6.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee
Primary Examiner
Art Unit 2823

March 22, 2005

HSIEN-MING LEE
PRIMARY EXAMINER

3/22/2005

OIPE JC29
JAN 31 2005
PATENT & TRADEMARK OFFICE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/137,163
Filing Date	05/02/2002
First Named Inventor	Pichler, et al.
Group Art Unit	~~1775~~ 2823
Examiner Name	Lee, Hsien Ming
Attorney Docket Number	2002P03156US

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
HL	1	6,268,695		Affinito	07/31/01	
HL	2	6,522,067		Graff, et al.	02/18/03	
HL	3	6,720,203		Carica, et al.	04/13/04	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]

Examiner Signature	Hsien Ming Lee	Date Considered	2/8/2005

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

paper No.: 013105

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/137,163
Filing Date	05/02/2002
First Named Inventor	Pichler, et al.
Group Art Unit	2823
Examiner Name	Lee, Hsien Ming
Attorney Docket Number	02P03156US

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
HL		6,570,325 B2		Graff, et al.	05/27/2003	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	A		
	B		
	C		

Examiner Signature	Hsien Ming Lee	Date Considered	3/22/05

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[1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

Paper No. : 020904

OIPE JC56
DEC 23 2003
PATENT AND TRADEMARK OFFICE

FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.: 2002P03156US	SERIAL NO.: 10/137,163
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT(S): Karl Pichler et al.	
(Use several sheets if necessary)	FILING DATE: 5/2/02	GROUP ART UNIT: 2823
(37 CFR 1.98(b))		

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUB-CLASS	FILING DATE If appropriate
Lee	AA	~~6,570,352 B2~~	5/27/03	Graff, et al.	313	506	6/22/01
	AB	6,570,325					
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						

FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUB-CLASS	TRANSLATION YES	TRANSLATION NO
	AI							
	AJ							
	AK							
	AL							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AM	
	AN	
	AO	
	AP	

EXAMINER	DATE CONSIDERED
Kevin Min Lee	~~2/12/04~~ 3/22/05

EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Paper No.: 122303

Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/137,163	PICHLER ET AL.	
	Examiner	Art Unit	
	Hsien-ming Lee	2823	

ISSUE CLASSIFICATION

ORIGINAL CLASS	ORIGINAL SUBCLASS	CROSS REFERENCE(S) CLASS	CROSS REFERENCE(S) SUBCLASS (ONE SUBCLASS PER BLOCK)						
438	26	438	28	30	48	55	531	627	

INTERNATIONAL CLASSIFICATION	
H01L	21/00
H01L	21/425
	/
	/
	/

(Assistant Examiner) (Date)

(Legal Instruments Examiner) 3/30/05 (Date)

HSIEN-MING LEE
PRIMARY EXAMINER

Hsien Ming Lee

(Primary Examiner) 3/22/2005 (Date)

Total Claims Allowed: 53

O.G. Print Claim(s)	O.G. Print Fig.
1	3A, 3B

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	31	31		61		91		121		151		181
2	2	32	32		62		92		122		152		182
3	3	33	33		63		93		123		153		183
4	4	34	34		64		94		124		154		184
5	5	35	35		65		95		125		155		185
6	6	36	36		66		96		126		156		186
7	7	37	37		67		97		127		157		187
8	8	38	38		68		98		128		158		188
9	9	39	39		69		99		129		159		189
10	10	40	40		70		100		130		160		190
11	11	41	41		71		101		131		161		191
12	12	42	42		72		102		132		162		192
13	13	43	43		73		103		133		163		193
14	14	44	44		74		104		134		164		194
15	15	45	45		75		105		135		165		195
16	16	46	46		76		106		136		166		196
17	17	47	47		77		107		137		167		197
18	18	48	48		78		108		138		168		198
19	19	49	49		79		109		139		169		199
20	20	50	50		80		110		140		170		200
21	21		51		81		111		141		171		201
22	22		52		82		112		142		172		202
23	23		53		83		113		143		173		203
24	24		54		84		114		144		174		204
25	25		55		85		115		145		175		205
26	26		56		86		116		146		176		206
27	27	52	57		87		117		147		177		207
28	28	53	58		88		118		148		178		208
29	29	51	59		89		119		149		179		209
30	30		60		90		120		150		180		210

SDC EX. 1002 - 423/544

Search Notes

Application No.	Applicant(s)	
10/137,163	PICHLER ET AL.	
Examiner	**Art Unit**	
Hsien-Ming Lee	2823	

SEARCHED

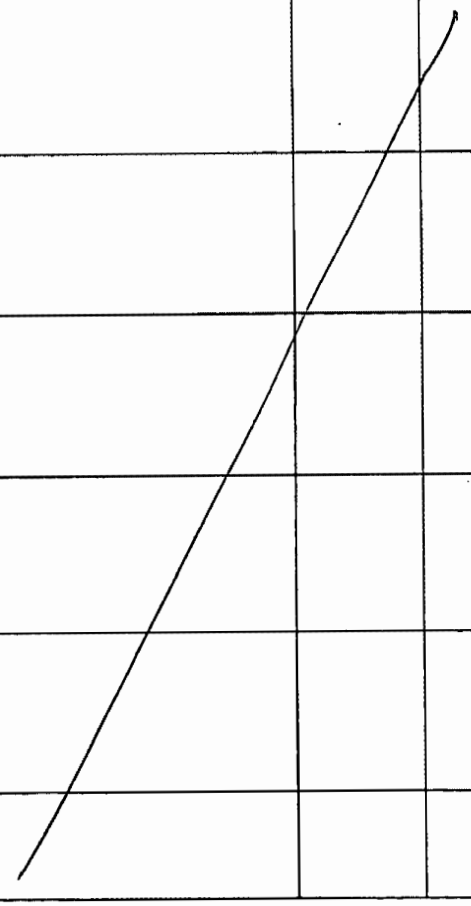
Class	Subclass	Date	Examiner
438	26, 28	3/22/05	Lee
438	30, 48		
438	55, 551		
438	624, 627		
438	641		
257	53, 21		
257	59, 414		
257	431, 701		
257	760		
updated search	above	3/22/05	Lee

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner
438	26, 28	3/22/05	Lee
438	30, 48		
438	55, 551		
438/624, 627, 641			

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

	DATE	EXMR
EAST attached (USPAT, USPG, EPO, JPO, IBM, Derwent)	9/21/2004	LEE
Ditto	3/22/2005	Lee



SDC EX. 1002 - 424/544

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Bib Data Sheet

CONFIRMATION NO. 1705

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/137,163	05/02/2002 RULE	438	2823	2002P03156US

APPLICANTS

Karl Pichler, Santa Clara, CA;

Kyle D. Firschknecht, Livermore, CA;

** CONTINUING DATA **********
NONE

** FOREIGN APPLICATIONS **********
NONE

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 06/13/2002

		STATE OR	SHEETS	TOTAL	INDEPENDENT
Foreign Priority claimed	☐ yes ☒ no				
35 USC 119 (a-d) conditions met	☐ yes ☒ no ☐ Met after Allowance	COUNTRY	DRAWING	CLAIMS	CLAIMS
Verified and Acknowledged	Examiner's Signature / Initials	CA	8	58	8

ADDRESS
Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin , NJ
08830

TITLE
Encapsulation for organic light emitting diodes devices

FILING FEE	FEES: Authority has been given in Paper	☐ All Fees
RECEIVED 1974	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue)

SDC EX. 1002 - 425/544

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	(("6,268,695") or ("6,522,067") or ("6,720,203")).PN.	US-PGPUB; USPAT	OR	OFF	2005/03/22 08:50
L2	48258	devices and (hardening or hardened)	US-PGPUB; USPAT	OR	ON	2005/03/22 10:08
L3	28065	2 and (remove or removing or etch or etching)	US-PGPUB; USPAT	OR	ON	2005/03/22 10:05
L4	10620	3 and (deposit or depositing or deposited)	US-PGPUB; USPAT	OR	ON	2005/03/22 10:06
L6	8160	4 and @ad<"20020502"	US-PGPUB; USPAT	OR	ON	2005/03/22 08:54
L7	3449	6 and organic	US-PGPUB; USPAT	OR	ON	2005/03/22 08:55
L8	4799	6 and light	US-PGPUB; USPAT	OR	ON	2005/03/22 10:06
L9	856	6 and (light with (harden or hardening or hardened))	US-PGPUB; USPAT	OR	ON	2005/03/22 10:11
L10	17038	devices and (hardening or hardened)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 10:05
L11	5899	10 and (remove or removing or etch or etching)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 10:06
L12	1332	11 and (deposit or depositing or deposited)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 10:06
L13	519	12 and light	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 10:06
L14	77	13 and (light with (harden or hardening or hardened))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 10:07
L16	3279	438/26,28,30,48,55,531,624,627, 641.ccls. and @ad<"20020502"	US-PGPUB; USPAT	OR	ON	2005/03/22 10:15
L17	1075	16 and devices and light	US-PGPUB; USPAT	OR	ON	2005/03/22 10:15
L18	82	17 and (harden or hardened or hardening)	US-PGPUB; USPAT	OR	ON	2005/03/22 10:15
L19	71	18 not 9	US-PGPUB; USPAT	OR	ON	2005/03/22 10:11
L20	4012	257/53,21,59,414,431,701,760.ccls. and @ad<"20020502"	US-PGPUB; USPAT	OR	ON	2005/03/22 10:15

SDC EX. 1002 - 426/544

L21	1937	20 and devices and light	US-PGPUB; USPAT	OR	ON	2005/03/22 10:15
L22	99	21 and (harden or hardened or hardening)	US-PGPUB; USPAT	OR	ON	2005/03/22 10:15
L23	93	22 not 19	US-PGPUB; USPAT	OR	ON	2005/03/22 10:16
L24	87	23 not 9	US-PGPUB; USPAT	OR	ON	2005/03/22 10:16

SDC EX. 1002 - 427/544

US-PAT-NO: 6555288

DOCUMENT-IDENTIFIER: US 6555288 B1

TITLE: Optical **devices** made from radiation curable fluorinated compositions

---------- KWIC ---------

Abstract Text - ABTX (1):

The invention provides organic optical waveguide **devices** which employ perfluoropolymeric materials having low optical loss and low birefringence. An optical element has a substrate; a patterned, light transmissive perfluoropolymer core composition; and a light reflecting cladding composition on the pattern of the core. Writing of high-efficiency waveguide gratings is also disclosed.

TITLE - TI (1):

Optical **devices** made from radiation curable fluorinated compositions

Brief Summary Text - BSTX (2):

The invention relates to organic optical **devices,** such as planar single mode waveguides made from radiation curable materials. Specifically, the invention relates to low loss, low polarization dependent, **devices** made from fluorohydrocarbon monomers, oligomers, or polymer components end-capped with radiation curable ethylenically unsaturated groups, such as acrylate or methacrylate groups. The **devices** made from these materials show good long term and short term stability, good flexibility, and reduced stress or crack induced optical scattering loss.

Brief Summary Text - BSTX (6):

A wide variety of optical **devices** can be made which incorporate a light guiding structure as the light transmissive elements. Illustrative of such **devices** are planar optical slab waveguides, channel optical waveguides, rib waveguides, optical couplers, optical splitters, optical switches, optical filters, variable attenuators, micro-optical elements and the like. These **devices** are described in more detail in U.S. Pat. Nos. 4,609,252, 4,877,717, 5,136,672, 5,136,682, 5,481,385, 5,462,700, 5,396,350, 5,428,468, 5,850,498, and U.S. patent application Ser. No. 08/838,344 filed Apr. 8, 1997, the disclosures of which are all incorporated herein by reference.

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Brief Summary Text - BSTX (7):

It is known in the art to make optical waveguides and other optical interconnect **devices** from organic polymeric materials. Whereas single mode optical **devices** made from planar glass are relatively unaffected by temperature, **devices** made from organic polymers show a far greater variation with temperature because the refractive index changes much faster with temperature in polymeric materials than in glass. This property can be exploited to make active, thermally tunable or controllable **devices** incorporating light transmissive elements made from organic polymers. One type of thermally tunable **devices** is a directional coupler activated by a thermo-optic effect. The thermo-optic effect is a change in the index of refraction of the optical element that is induced by heat. Thermo-optic effect **devices** help to provide less costly routers when the activation speed of a coupler state is not too high, i.e., when the activation speed is in the range of milliseconds.

Brief Summary Text - BSTX (8):

Unfortunately, most polymeric materials contain carbon-to-hydrogen chemical bonds which absorb strongly at the 1550 nm wavelength that is commonly used in telecommunication applications. It has long been known that fluoropolymers, for example, have significantly reduced absorption at 1550 nm. While planar waveguides made from fluorinated polyimide and deuterated polyfluoromethacrylate have achieved single mode losses of as little as 0.10 db/cm at 1300 nm, it is relatively difficult to make optical **devices** from these materials. Specifically, the photolithographic process by which they have been made includes a reactive ion etching step. Fluorinated polyimide and deuterated polyfluoromethacrylate also have higher losses at 1550 nm, typically on the order of 0.6 dB/cm.

Brief Summary Text - BSTX (11):

Among the many known photopolymers, acrylate materials have been widely studied as waveguide materials because of their optical clarity, low birefringence and ready availability of a wide range of monomers. However, the performance of optical **devices** made from many acrylate materials has been poor, due to high optical losses, poor resistance to aging and yellowing, and thermal instability of the polymerized material.

Brief Summary Text - BSTX (12):

There continues to be a need for low loss radiation curable materials that can be used to make optical **devices** by a more direct process having fewer manufacturing steps. Specifically, a process is desired that does not require

a reactive ion etching (RIE) step to develop the pattern of the optical element core. Such materials could be used to make optical **devices** by a relatively simple and more direct lithographic procedure.

Brief Summary Text - BSTX (13):

It is also important that these materials have little or no birefringence. As is well known in this art, birefringence is the difference between the refractive index of the transverse electric or TE polarization (parallel to the substrate surface) and the transverse magnetic or TM polarization (perpendicular to the substrate surface). Such birefringence is undesirable in that it can lead to **devices** with large polarization dependant losses and increased bit error rates in telecommunication systems.

Brief Summary Text - BSTX (14):

Another type of useful optical device is a waveguide grating. Diffraction gratings, e.g., Bragg gratings, are used in the telecommunications industry to isolate a narrow band of wavelengths from a broader telecommunications signal. Polymeric planar waveguide gratings have a number of advantages in terms of their relative ease of manufacture and their ability to be tuned over a wide range of frequencies by temperature or induced stress. In addition, such **devices** have the advantage of being easily incorporated into integrated **devices**. Unfortunately, such gratings in polymeric materials typically are of relatively low efficiency. This drawback can result in poor signals with increased bit error rates. It would, therefore, be beneficial to find a method of making polymeric planar waveguide gratings with improved efficiency.

Brief Summary Text - BSTX (16):

WDM **devices** can be designed by using planar waveguides with gratings that can reflect a single wavelength or channel as a building block. These **devices** can be fabricated with low temperature processes and high throughput. In this disclosure, we focus on the properties of this fundamental building block, the fabrication of a grating in a waveguide structure, outline what we believe is the basic mechanism responsible for the grating formation, and its environmental, humidity and temperature performance.

Brief Summary Text - BSTX (19):

According to one aspect of the invention, there is provided a photolithographic method of making optical elements comprising: a) applying a core photopolymerizable composition to a support to form a core photopolymerizable composition layer, said core photopolymerizable composition including at least one photoinitiator and at least one core photopolymerizable monomer, oligomer, or polymer having at least one photopolymerizable group,

said core photopolymerizable monomer, oligomer, or polymer including a perfluorinated substituent; b) imagewise exposing the core photopolymerizable composition layer to sufficient actinic radiation to effect the at least partial polymerization of an imaged portion and to form at least one non-imaged portion of said core photopolymerizable composition layer; c) **removing** said at least one non-imaged portion without **removing** said imaged portion, thereby forming a light transmissive patterned core from said imaged portion; d) applying an upper cladding polymerizable composition onto the patterned core; and e) curing said upper cladding composition, wherein said upper cladding and the core-interfacing surface of said support are each made from materials having a lower refractive index than said core.

Detailed Description Text - DETX (9):

After the core polymerizable composition has been at least partially polymerized to form the predetermined pattern of the polymer on the surface of the lower cladding, the pattern is developed by **removing** the nonimage areas and leaving intact the predetermined pattern of core 8, as shown in FIG. 5. Any conventional development method can be used, for example, flushing with a solvent for the unirradiated composition. Such solvents include polar solvents, such as alcohols and ketones. The most preferred solvents are acetone, methanol, propanol, tetrahydrofuran and ethyl acetate. For highly fluorinated materials, the preferred solvent is Galden.RTM. HT-110, a perfluorinated ether available from Ausimont USA.

Detailed Description Text - DETX (10):

Although FIG. 4-FIG. 5 show the formation of just one core using a photomask having one transparent image-forming region, the skilled artisan will appreciate that multiple spaced-apart cores could be formed on the lower cladding simultaneously using a photomask having multiple transparent image-forming regions or similar **devices** capable of causing the exposure of multiple image areas.

Detailed Description Text - DETX (29):

The substrate may be any material on which it is desired to establish a waveguide. The substrate material may, for example, be selected from glass, quartz, plastics, ceramics, crystalline materials and semiconductor materials, such as silicon, silicon oxide, gallium arsenide, and silicon nitride. Formation of the optical elements on wafers made of silicon or other compositions are specifically contemplated. Silicon wafers are preferred substrates in part due to their high surface quality and excellent heat sink properties. To improve adhesion of the photopolymer to the silicon wafer, the wafer may be cleaned and treated with silane or other adhesion promoter, if

desired. The substrate may or may not contain other **devices,** either topographical features such as grooves or electrical circuits, or electro-optic **devices** such as laser diodes.

Detailed Description Text - DETX (30):

A preferred plastic substrate is a urethane-coated polycarbonate substrate which is described in provisional patent application Ser. No. 60/121,259 filed on Feb. 23, 1999, for "Control of Temperature Dependent Planar Polymeric Waveguide **Devices** through the use of Substrate and Suprastrate Layers with Specific Coefficients of Thermal Expansion," the disclosure of which is incorporated herein by reference.

Detailed Description Text - DETX (59):

In selecting other monomers and oligomers that may be suitable for forming planar light guiding **devices,** the following observations should be considered. For high purity fluorinated acrylates, the majority of the absorbance at 1550 nm is a result of carbon-to-hydrogen bonds. The absorption spectra for the non-fluorinated compound hexanediol diacrylate (HDDA) and the fluorinated compound octafluorohexanediol diacrylate (OFHDDA), in which eight hydrogen atoms are replaced by fluorine, as shown in FIG. 31, illustrate this point. The small peaks around the 1550 nm and 1310 nm regions of the spectra are characteristic of uncured liquids. After cure, virtually all of these fluctuations are eliminated, as shown in the spectrum of cured octafluorohexanediol diacrylate appearing at FIG. 32. Most of the elimination is probably due to the conversion of the carbon double bonds to carbon single bonds as the acrylate cures. Further, differences in the baseline absorbance values are believed to be the result of the higher level of scattering in the solid sample. Such scattering is an artifact of the way in which the sample was made and the thickness variation in the sample. Actual waveguide losses for this material would be substantially lower than indicated in FIG. 32.

Detailed Description Text - DETX (64):

The polymerizable compound is present in each polymerizable composition in an amount sufficient to polymerize upon exposure to sufficient heat and/or actinic radiation. The amount of the photopolymerizable compound in the composition may vary widely and amounts normally used in photopolymerizable compositions for use in the preparation of photopolymers for use as the light transmissive element of light transmissive **devices** may be used. The amount of photopolymerizable compound is generally used in an amount of from about 35 to about 99.9% by weight of the composition. In the preferred embodiment, one or more photopolymerizable compounds in the overall photopolymerizable composition account for from about 80% to about 99.5% by weight, most preferably from about

95 to about 99.5% based on the weight of the overall composition.

Detailed Description Text - DETX (71):

Photopolymerizable compositions may include mixtures of polymerizable compounds end-capped with at least one actinic radiation curable group, such as the above-described epoxy or ethylenically unsaturated groups, specifically acrylate, methacrylate, and vinyl ether. Vinyl ethers can react with acrylates. Although acrylates and vinyl ethers do not ordinarily react with epoxies, mixed systems of vinyl ethers, acrylates, and epoxies can form interpenetrating networks if suitable photoinitiators are used. Accordingly, mixed systems can be used in making optical **devices** by the methods described here. Photoinitiators that are suitable for use in such mixed systems are described in U.S. Pat. No. 5,510,226, the disclosure of which is incorporated herein by reference.

Detailed Description Text - DETX (79):

Control of the spatial profile of the actinic radiation, that is, where it falls on the layer of photopolymerizable material may be achieved by conventional methods. For example, in one conventional method, a mask bearing the desired light transmissive pattern is placed between the source of actinic radiation and the photopolymerizable composition film. The mask has transparent and opaque regions which allow the radiation to fall only on the desired regions of the film surface. Masked exposure of thin films is well known in the art and may include contact, proximity and projection techniques for printing the light transmissive pattern onto the film. Another conventional method of spatial control is to use a source of actinic radiation which comprises a directed or focused beam such as a laser or electron beam. Such a beam intersects only a small area of the photo-polymerizable material film surface. The pattern of the desired light transmissive regions is achieved by moving this small intersection point around on the film surface either by scanning the beam in space or by moving the substrate so that the intersection point is changed relative to a stationary beam. These types of exposure using a beam source are known in the art as direct-write methods. By choosing the spatial characteristics of irradiation, it is possible to create light transmissive regions on the surface of the substrate and produce slab and channel waveguides. A slab waveguide is one in which the optical wave is confined only to the plane of the film. A channel waveguide is one in which the optical wave is also confined laterally within the film. A channel structure is necessary for many nonlinear and electro-optic **devices** because it allows the light to be directed to certain areas of the substrate as well as providing a mechanism for splitting, combining optical waves, coupling light from the waveguide to optical fibers, and maintaining the high intensity

available in an optical fiber.

Detailed Description Text - DETX (82):

Device testing and modeling suggest a device lifetime (time for 0.1 dB/cm loss) of more than 10 years at 120.degree. C. (operation temperature) and more than 1 hour at 250.degree. C. (a typical device packaging temperature), thus allowing for use of **devices** made in accordance with this disclosure applicable in the aerospace, military, and telecommunications industries. Flexibility of the materials allows for fabrication of **devices** with desired bending angles. Cracking is also avoided even when the device is exposed to very high or very low temperatures. Good adhesion of the materials permits fabrication of robust **devices** on a variety of substrates without delamination even in some harsh environments such as high temperature and high humidity. Compatibility of device fabrication techniques with those of the semiconductor industry allows for development of hybrid optoelectronic circuitry.

Detailed Description Text - DETX (108):

The refractive index of each of the polymerizable compounds made in Example A-B, or described above at Examples C-D, was measured by mixing each with 1% by weight of an appropriate photoinitiator. The mixtures were then spin coated onto a silicon wafer at a thickness of 5 to 10 microns. The samples were purged with nitrogen and cured to a **hardened** film with UV **light**. The refractive index of the films was then measured using a Metricon 2010 testing apparatus with a 1550 nm laser source in the TE mode. The results are tabulated in Table 2.

Detailed Description Text - DETX (130):

The materials from Examples E, F and G also exhibited no measurable polarization dependence when tested using a Metricon 2010 prism coupling refractive index measuring device in both the TE and TM modes at 1550 nm. The results observed imply a refractive index difference between the TE and TM polarizations of less than 0.0001,the measurement sensitivity of the testing instrument. The results for the invention compare to differences of 0.008 (at 1.3 .mu.m wavelength light) for high T.sub.g fluorinated polyimides, as reported in U.S. Pat. No. 5,598,501. While fluorinated polyimides exhibit low loss, their birefringence is a clear disadvantage to their use. As is known in the art, a birefringent material has different refractive indices depending on orientation of the material. Since the operation of **devices,** such as thermo-optic switches, directional couplers, and the like depends on small refractive index differences, the operation may be different for TE and TM polarizations in highly birefringent materials. This is generally unacceptable since the light coming into the device will have an unknown state of

polarization. The virtual absence of polarization dependence in Examples E, F, and G indicates that these materials are capable of low loss and can produce waveguides with minimal polarization losses and shifts.

Detailed Description Text - DETX (154):

A method of writing diffraction gratings in polymeric waveguides is described in patent application Ser. No. 09/026,764 for "Fabrication of Diffraction Gratings for Optical Signal **Devices** and Optical Signal **Devices** Containing the Same, " filed on Feb. 20, 1998, the disclosure of which is incorporated herein by reference. In that disclosure, core and cladding waveguide structures are described as being formed in partially cured UV curable materials. The curable compositions include at least two photopolymerizable comonomers. The partially cured waveguide structure is then exposed with additional UV light through a photomask that generates light and dark regions in both the core and cladding. In the light regions, the UV radiation causes additional polymerization of the monomers to occur. Because the monomers are chosen so as to have different polymerization and diffusion rates, the polymer formed in the light areas during the phase mask exposure, or "writing," step has a different composition than the polymer in the dark areas. After exposure through the mask is complete, there remains unreacted monomer.

Detailed Description Text - DETX (196):

Gratings have been written in planar waveguiding optical **devices** according to the invention using both the phase mask and interfering beam approach.

Detailed Description Text - DETX (203):

Additional cladding composition as listed above is formulated and spin-coated onto the core structure so as to form a conformal layer that is 10 microns thick and that layer is subsequently blanket UV-exposed under the mercury lamp to form a solid conformal film of refractive index 1.3723 (at 1550 nm when fully cured) as an overcladding layer. This layer is also exposed for a short time (1 sec.) to ensure only partial polymerization at this stage. A phase mask with a grating is used to print (using an Argon ion laser operating at 363.8 nm) a grating across the core in each of the four Mach-Zehnder **devices**. The sample with the planar waveguiding circuit is held parallel to the phase masks at 50 microns from the mask. The laser beam is directed perpendicularly to the mask and the sample. The laser beam diameter is 3 mm (at 1/e.sup.2 intensity). The laser is scanned 3 mm across the center of the 6-mm-long Mach-Zehnder arms, creating gratings in the three partially cured waveguide layers. The sample is finally subjected to a final UV cure in a nitrogen ambient atmosphere under the mercury lamp (60 sec.) and a final thermal cure (90 deg. C for 1 h) is carried out to effect a full

polymerization of all three layers. Testing of the sample reveals that all the gratings are reflecting the desired wavelength channels.

Detailed Description Text - DETX (205):

While this property of linear tunability is a highly desired property in making thermo-optic **devices,** it also useful in making gratings which are stable to temperature changes. This can be accomplished by changing the substrate on which the grating is made. By choosing substrates with different coefficients of thermal expansion (CTE), the expansion rate of the Bragg grating can be altered. The change in the Bragg wavelength of the grating with temperature (d.lambda..sub.B /dt), as shown in FIG. 39, can be altered by using substrates with different CTEs. Substrates that produce a value of d.lambda..sub.B /dt as little as -0.06 nm/.degree. C. have been developed. Datum 30 refers to the urethane-coated polycarbonate substrate noted above.

Detailed Description Text - DETX (206):

Gratings made from the octafluorohexanediol di-acrylate/tetra-acrylate of Fluorolink.RTM. T material in accordance with the invention showed a Bragg wavelength shift of just 0.2 nm when the ambient relative humidity was changed by 90% at a constant temperature of 50.degree. C. This result was favorably much smaller than the result obtained using gratings made from other materials where the shift was 3.7 nm. This unexpected benefit may allow optical **devices** made in accordance with the invention to be packaged without having to be hermetically sealed.

Other Reference Publication - OREF (1):

L. Eldada, "Laser-Fabricated Low-Loss Single-Mode Raised-Rib Waveguiding **Devices** in Polymers", J. of Lightwave Tech., vol. 14, No. 7 (1996) 1704.

Other Reference Publication - OREF (2):

U.S. patent application Ser. No. 60/121,259, filed Feb. 23, 1999 "Control of the Temperature Dependence of Planar Polymeric Waveguide **Devices** through the use of Substrate or Suprastrate Layers with Specific Coefficients of Thermal Expansion," (30-4558) expired.

Other Reference Publication - OREF (5):

U.S. patent application Ser. No. 09/510,331 "Planar Polymeric Waveguide **Devices** with Temperature Dependence Control Features", filed Feb. 22, 2000, (AL00-024).

US-PAT-NO: 6039898

DOCUMENT-IDENTIFIER: US 6039898 A
See image for Certificate of Correction

TITLE: Optical memory device and a method for manufacturing thereof

---------- KWIC ---------

Assignee Name - ASNM (1):
O.M.D. Optical Memory **Devices,** Ltd.

Assignee Group - ASGP (1):
O.M.D. Optical Memory **Devices,** Ltd. Rehovot IL 03

Brief Summary Text - BSTX (2):
The present invention relates to methods for manufacturing optical memory **devices** such as compact discs (CD), tapes, cards, wires, cylindrical drums, or the like, the information from which is read out by optical means.

Brief Summary Text - BSTX (4):
Compact discs are known optical memory **devices** which are widely used particularly with playback and computer **devices** for retrieving musical and software compositions. Such **devices** typically comprise only one information carrying layer and, therefore, suffer from a limited amount of recorded data.

Brief Summary Text - BSTX (5):
Three-dimensional optical memory **devices** have been developed typically comprising a plurality of parallel, spaced-apart layers having information carrying regions in which optical properties differ from those of adjacent regions of the layers. One example of such a device is disclosed in U.S. Pat. No. 4,090,031. The device comprises a substrate and a plurality of data layers provided on one side of the substrate. Each of the layers comprises data tracks formed of lines of data spots. The data spots are, in turn, formed of either binary coded digital information or frequency or pulse length modulated analog information which is photographically recorded. The data spots are light reflective. Selection of one data track for playback is accomplished by changing the focus of a reading light beam from one data layer to another, or by making the data tracks of materials having different optical properties, the

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reading light being of different wavelengths for different layers. To this end, different color dyes or different photoluminescent materials are used and corresponding color filters are selectively positioned in front of light detectors.

Brief Summary Text - BSTX (9):

It is a major object of the present invention to provide a novel method of manufacturing an optical memory device, particularly such a method which is suitable for mass production of the optical memory **devices**.

Brief Summary Text - BSTX (15):

(c) **removing** the recording medium from the patterned surface after the recording regions have obtained the desired optical properties.

Brief Summary Text - BSTX (22):

(iii) **removing** the recording medium from the patterned surface after the recording regions have obtained the desired optical properties; and

Detailed Description Text - DETX (17):

Thereafter, although not specifically illustrated, the fluorescent material 210 is removed from the regions 209b by washing and cleaning procedures as described above. As shown in FIG. 3e, the resulted structure is coated by an additional layer 212 which is made of a transparent material 213 such as, for example, the same photoresist mixture but without the light sensitive components. If the photoresist 205 is based on polymethylmethacrylate (PMMA), then the latter could be used as the material 213 for the additional layer 212. The illumination of the layer 212 with UV **light** and/or baking provides desirable **hardening** and protection. Hence, a one-layer disc, generally designated 214, is provided.

Detailed Description Text - DETX (18):

As shown in FIG. 3g, in order to provide a multi-layered structure a further layer 216 formed of a photoresist material 217 is deposited on the layer 212 and exposed through a photomask 218 so as to obtain a desired pattern formed of a plurality of regions 220a of the photoresist material which are specifically arranged on a surface of the layer 216 defining regions 220b between the regions 220a. It is appreciated that further processes of inserting the fluorescent dye into the regions 220a, **removing** the dye from the regions 220b and coating the structure by an intermediate protective layer would complete a two-layered optical disc, which is not specifically shown.

Detailed Description Text - DETX (23):

It is appreciated that the provision of such a reflective material underneath the fluorescent material, on the one hand, increases the fluorescent properties of the material 311 and, on the other hand, provides a desired protection for the substrate layer 302 when **removing** therefrom the excess of the fluorescent material 311. Obviously, although not specifically shown, a multi-layered structure may be obtained by gluing such **devices** 312 to each other in the above described manner.

Claims Text - CLTX (10):

8. The method according to claim 1, further comprising the steps of coating the patterned surface of the substrate with a reflective material, and **removing** said reflective material from the spaces between said spaced-apart regions.

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OIPE JC24 APR 20 2005 PATENT & TRADEMARK OFFICE

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Pichler, et al.

Appln. No.: 10/137,163

Filing Date: 05/02/2002

Title: **IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES**

Examiner: Lee, Hsien Ming

Art Unit: 1775

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This Information Disclosure Statement is submitted:

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04/20/2005 CNGUYEN 00000030 192179 10137163

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Substitute for Form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/137,163
Filing Date	05/02/2002
First Named Inventor	Pichler, et al.
Group Art Unit	1775
Examiner Name	Lee, Hsien Ming
Attorney Docket Number	2002P03156US

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	A	WO	02/05361	A1	McCormick, et al.	01-17-2002		
	B	WO	01/81649	A1	Graff, et al.	11-01-2001		
	C	EP	1183567	B1	Guehler, et al.	05-07-2003		

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[1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

Stand der Technik / Prior Art Documents

Unser Zeichen / Our Ref. P2002,0833

Titel / Title: Improved encapsulation for organic light emitting diodes devices

DE-Recherche / Prüfungsverfahren
DE-Search / Examination Report

	Already in the file of:
WO02/05361	
WO01/81649	
EP 1183567	

Vom Erfinder mit der E-Meldung genannter StdT
Mentioned in the invention disclosure by inventor

	Already in the file of:
PML patent literature "UV-curable printing inks	www.markem.com or www.vanet.hitachi.co.jp
Hue P. Le	The Society for Imaging Sciences and Technology, Vol 42, No. 1, Jan/Feb 1998
Hayes, D.J. et al.	Journal of the SID, Vol. 9/1, 2001

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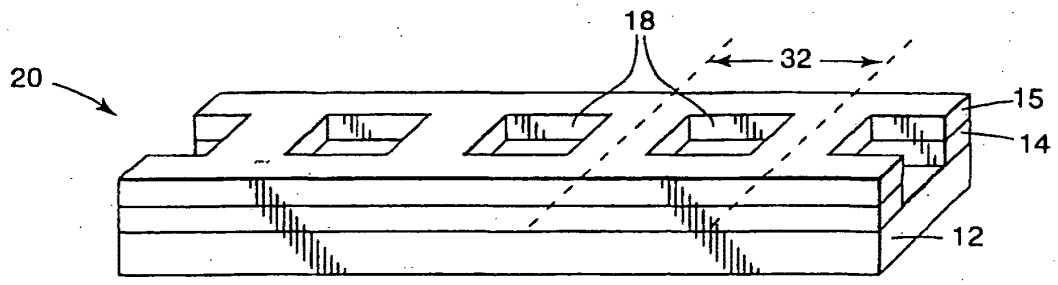
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Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ENCAPSULATED ORGANIC ELECTRONIC DEVICES AND METHOD FOR MAKING SAME



(57) Abstract: The invention provides methods for making encapsulated organic electronic devices (OED) including organic light emitting diodes (OLED). The present invention can provide a robust OED device by means of in situ edge sealing enhancing structural integrity and device lifetime. The edge sealing is provided by using an adhesive component (14) applied to a substrate (12) prior to OED element (16) deposition. In one OLED embodiment of the present invention, a thin layer of an adhesive (pressure sensitive adhesive, hot melt, or curable) is applied to release liner, openings are cut in the adhesive/liner composite, then the composite is adhered to an electrode-coated substrate. Alternatively, an adhesive may be applied directly onto the electrode-coated substate, e.g., by printing in a desired pattern, optionally partially cured or dried, then covered with one or more liners that act as a mask during deposition of the OLED elements. Another method would be to prepare a blank liner with a patterned adhesive, then die cut openings compplementary to the adhesive pattern in the liner to allow deposition of OLED elements once the adhesive/liner is placed on the substrate.

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ENCAPSULATED ORGANIC ELECTRONIC DEVICES AND METHOD FOR MAKING SAME

TECHNICAL FIELD

This invention relates to a method for making an encapsulated organic electronic device.

BACKGROUND

Organic electronic devices (OED)s are articles that include layers of organic materials, at least one of which can conduct an electric current. Illustrative examples of known OED constructions include photovoltaic devices, rectifiers, transmitters, and organic light emitting diodes (OLED)s.

An organic light emitting diode (OLED) is a typical example of an OED. OLEDs, sometimes referred to as lamps, are desirable for use in electronic media because of their thin profile, low weight, and low driving voltage, *i.e.,* less than about 20 volts. OLEDs have potential use in applications such as backlighting of graphics, pixelated displays, and large emissive graphics.

OLEDs typically consist of an organic light emitter layer and additional organic charge transport layers on both sides of the emitter, all of which are sandwiched between two electrodes: a cathode and an anode. The charge transport layers comprise an electron transporting layer and a hole transporting layer. Charge carriers, *i.e.,* electrons and holes, are injected into the electron and hole transporting layers from the cathode and anode, respectively. Electrons are negatively charged atomic particles and holes are vacant electron energy states that behave as though they are positively charged particles. The charge carriers migrate to the emitter layer, where they combine to emit light.

Examples of OLEDs include molecularly doped polymer devices where charge carrying and/or emitting species are dispersed in a polymer matrix (*see* J. Kido, "Organic Electroluminescent devices Based on Polymeric Materials," *Trends in Polymer Science,* **1994,** *2,* 350-355), conjugated polymer devices where layers of polymers such as

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poly(phenylenevinylene) act as the charge carrying and emitting species (*see* J. J. M. Halls, D. R. Baigent, F. Cacialli, N. C. Greenham, R. H. Friend, S. C. Moratti, and A. B. Holmes, "Light-emitting and Photoconductive Diodes Fabricated with Conjugated Polymers," *Thin Solid Films,* **1996,** *276*, 13-20), vapor deposited small molecule heterostructure devices (*see* U. S. Pat. No. 5,061,569, and C. H. Chen, J. Shi, and C. W. Tang, "Recent Developments in Molecular Organic Electroluminescent Materials," *Macromolecular Symposia,* **1997,** *125*, 1-48), light emitting electrochemical cells (*see* Q. Pei, Y.Yang, G. Yu, C. Zang, and A. J. Heeger, "Polymer Light-Emitting Electrochemical Cells: In Situ Formation of Light-Emitting p-n Junction," *Journal of the American Chemical Society,* **1996,** *118*, 3922-3929), vertically stacked organic light-emitting diodes capable of emitting light of multiple wavelengths (*see* U. S. Pat. No. 5,707,745, and Z. Shen, P. E. Burrows, V. Bulovic, S. R. Forrest, and M. E. Thompson, "Three-Color, Tunable, Organic Light-Emitting Devices," *Science,* **1997,** *276*, 2009-2011).

Essentially all organic light emitting materials, organic charge transport materials and organic hole transport materials are adversely affected by heat, light, oxygen, and moisture. The low work function metal cathodes typically used in OLEDs are also sensitive to oxygen and moisture, which can cause corrosion and failure of the cathode. It is important, therefore, to protect these layers from exposure to the open air. Some methods of making OEDs such as OLEDs partially protect these layers, for example, methods that use barrier films as substrates, but the top layer of the OLED remains exposed. A separate encapsulation step, such as bonding a metal cap on top of an OLED, is typically required. This separate encapsulation step adds to manufacturing complexity and is not generally suited to the fabrication of flexible OLEDs.

SUMMARY OF INVENTION

The present invention describes a novel protected OED and a novel method of making a protected OED. The method of the present invention protects the applied layers of an OED from exposure to the open air, particularly during manufacture of an OLED, in order to assure the maximum possible lifetime of the device.

In one aspect, the present invention provides a method for making an organic electronic device comprising:

providing an adhesive-coated release liner from which a pattern has been cut,

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applying the adhesive-coated side of the patterned release liner to an electrode substrate to form a composite structure having at least a portion of the electrode substrate exposed,

depositing one or more organic electronic elements on the exposed electrode of the composite structure,

removing the release liner from the composite structure, and

adhering a sealing layer to the exposed adhesive of the composite structure.

In another aspect, the invention provides a method for making an organic electronic device comprising;

coating an adhesive in a pre-determined pattern on an electrode substrate to form a composite structure wherein areas of the substrate remain exposed;

optionally at least partially curing, or drying, the adhesive;

applying a liner mask to the patterned adhesive such that at least a portion of the exposed substrate areas remain exposed;

depositing one or more organic electronic elements on the masked composite structure;

removing the liner mask from the adhesive; and

applying a sealing layer.

In yet another aspect, the invention provides an article comprising an organic electronic device wherein the layers between the anode and cathode are surrounded by an adhesive layer and wherein the circumference of the adhesive layer is equal to the circumference of one or both of the electrode substrate or sealing layer.

In another aspect, the present invention provides a method for making an OED such as an OLED wherein an encapsulating component, which is incorporated into the OED structure, also serves as a mask while the OED is being constructed. Pursuant to one aspect of the present invention, an adhesive-coated liner, having openings cut through it in the desired shape of the OED, is applied, adhesive side down, to the OED substrate.

In another aspect of the invention, the adhesive may be precisely applied to the OED substrate in a liquid form, *e.g.*, by an inkjet printing method or screen printing. One or more solid liner layers, having openings complementary to the openings in the adhesive layer may then be applied. After this step, the desired element layers of the OED are

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sequentially deposited onto the liner/adhesive/substrate composite structure. Once all the desired OED layers have been applied, the liner is removed from the adhesive, leaving complete or substantially complete OED structures surrounded by an adhesive structure.

In yet another aspect of the invention, an OED may be an OLED. The present invention will allow an OLED to be constructed from the anode or cathode side. In either case, a sandwich structure can be made by applying the adhesive layer to an electrode layer then depositing the OLED elements in the order necessary to construct an OLED.

In a further aspect, the OLED may be partially constructed on each electrode substrate and the final operational OLED obtained by laminating the two partial lamps together. The sandwich structure would be attained by first applying the adhesive/liner layer on one or both electrode substrates and depositing, for example, hole transport material onto the anode substrate and electron transport and emitter material on the cathode substrate and subsequently aligning and laminating said films together with heat and/or pressure. The final OLED device can have enhanced structural stability over other types of laminated OLED devices due to the adhesive forming the *in situ* edge seal.

In some embodiments, it may be preferable to have the organic OLED elements coated over an area larger than the underlying electrode layer. Having the organic layers cover a larger area than the electrodes helps avoid electrical shorting.

After the OLED organic layers have been applied, a counter electrode is applied. If the counter electrode is a cathode, the electrode may comprise a sheet of electrically conductive material, *e.g.,* aluminum, that is placed on the adhesive structure to form a sealing layer, thereby encapsulating each OLED device. If the counter electrode is an anode, the electrode may comprise a sheet of electrically conductive material, *e.g.,* ITO on a polymer film substrate, that is placed on the adhesive structure to form a sealing layer, thereby encapsulating each OLED device. If the sealing layer is a counter electrode, it must touch the entire top organic element layer to provide illumination of the total area of the OLED device. In these cases, the counter electrode will also act as a barrier to water and air. Alternatively, the counter electrode may be deposited within the boundaries of the adhesive structure and a protective material may be placed on top of the adhesive structure, thereby encapsulating each OLED device. The protective layer may be conducting or non-conducting. If it is conducting, it may be used as a conducting lead, and it must touch at least one point of the adjacent electrode layer. The resulting sheet of

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OLED devices may then be cut in patterns defined by the adhesive portion, thereby providing individual OLED devices, each of which is encapsulated between two substrates that are edge sealed by an adhesive.

As used in this invention:

"partially cure" means increasing the viscosity to induce film formation or reduce creep or flow, *i.e.*, wherein the physical state of the composition is altered, such as by transforming from a fluid to less fluid state, going from a tacky to a non-tacky state, going from a soluble to insoluble state, or decreasing the amount of polymerizable material by its consumption in a chemical reaction.

An advantage of at least one embodiment of the present invention is that it allows an OED to be made without exposure to the atmosphere at any time during the process, for example by conducting the deposition steps in a vacuum.

Another advantage of at least one embodiment of the present invention is that it allows for encapsulated OEDs to be made on a continuous basis.

Another advantage of at least one embodiment of the present invention is that it provides an OED having structural stability.

Another advantage of at least one embodiment of the present invention is that because the OED is not exposed to the atmosphere while being constructed, air and water sensitive materials can be used in the OED.

Another advantage of at least one embodiment of the present invention is that OEDs can easily be made in any desired shape.

Another advantage of at least one embodiment of the present invention is that OEDs can be made continuously in a roll-to-roll process.

Another advantage of at least one embodiment of the present invention is that OEDs may be made on a flexible substrate as compared to conventional methods that require a rigid substrate.

Although the invention described herein may be used for a wide variety of OED devices, for illustrative purposes, only OLEDs will be discussed in detail.

Other features and advantages of the invention will be apparent from the following drawings, detailed description, and claims.

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BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 illustrates the substrate with the applied adhesive-coated liner mask.

Fig. 2 illustrates the final sheet of OLED devices after the OLED elements have been deposited, the liner has been removed, and the sealing layer has been applied to the exposed transfer adhesive. Lines where cuts can be made to convert the sheet of OLED devices into individual devices (*i.e.*, singulate) are also shown.

Fig. 3 illustrates an exploded view of the components of an organic electronic device made by a method of the present invention.

Fig. 4 illustrates a simplified representation of a vapor coating process that could be used in the present invention.

Fig. 5 illustrates a typical OLED construction without the encapsulating material of the present invention.

Fig. 6 illustrates a cross-sectional view of an OLED construction made using the present invention.

Fig. 7 illustrates a top view of the OLED of Fig. 6.

Fig. 8 illustrates a cross-sectional view of another OLED construction made using the present invention.

Fig. 9 illustrates a top view of the OLED of Fig. 8.

Fig. 10 illustrates the use of multiple adhesive/liner pairs of different sizes and shapes in OED fabrication.

Fig. 11 illustrates the use of adhesive and liner layers of different sizes in conjunction with directional layer deposition to control the area on which various deposited layers are applied.

Fig. 12 illustrates an OLED constructed by laminating together two partial OLED structures, at least one of which is made by a method of the present invention.

The present invention is susceptible to various modifications and alternative forms. Some specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of

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the invention as described by the following detailed description and as defined by the appended claims.

DETAILED DESCRIPTION

The present invention can provide a robust OED device by means of *in situ* edge sealing thereby enhancing structural integrity and device lifetime. The edge sealing is provided by using an adhesive component applied to a substrate prior to OED element deposition.

In one OLED embodiment of the present invention, a thin layer of an adhesive (pressure sensitive adhesive, hot melt, or curable) is applied to a release liner, openings are cut in the adhesive/liner composite, then the composite is adhered to an electrode-coated substrate. Alternatively, an adhesive may be applied directly onto the electrode-coated substrate, *e.g.*, by printing in a desired pattern, optionally partially cured or dried, then covered with one or more liners that act as a mask during deposition of the OLED elements. The OLED elements may be applied in one or more patterns (circles, rectangles, letters, numbers, bar code and so forth) through openings in the liner and the adhesive. If multiple masks having different sizes or shapes are used, the OLED element layers may be applied in different or overlapping areas of the opening, depending on when each mask is removed during the deposition process. Alternatively, the elements may be deposited through an additional mask placed over the openings, which results in thin film deposition in a different, typically smaller, pattern than that defined by the adhesive liner mask described above. Another method would be to prepare a blank liner with a patterned adhesive, then die cut openings complementary to the adhesive pattern in the liner to allow deposition of OLED elements once the adhesive/liner is placed on the substrate.

Examples of suitable adhesives include pressure sensitive adhesives (PSA) made from acrylates such as Ultra-Clean Laminating Adhesive 501FL and Optically Clear Laminating Adhesive 8141 both available from 3M Bonding Systems Division, St. Paul, MN, rubbers such as KRATON styrenic block copolymers from Shell Chemicals, Houston, TX, silicones such as RHODOTAK 343 from Rhodia Silicones, Lyon, France, and polyolefins such as poly(1-hexene), poly(1-octene), and poly(4-ethyl-1-octene) described in US 5,112,882; hot melt adhesives such as unfilled versions of the tackified polyamide-polyether copolymers described in U.S. Pat. No. 5,672,400 and the

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thermoplastic polymer adhesive films described in U.S. Pat. No. 5,061,549; curable adhesives, thermosets, and crosslinking systems such as the unfilled versions of the epoxy/thermoplastic blends described in U.S. Pat. No. 5,362,421; the cyanate ester/ethylenically unsaturated semi-IPNs described in U.S. Pat. No. 5,744,557; the epoxy/acrylate compositions described in WO 97/43352; two-part epoxies like ARALDITE 2011 from Ciba Specialty Chemicals, Brewster, NY; and UV curing resins like the Series 3100 adhesives from Three Bond of America, Inc., Torrance, CA. Various combinations of pressure sensitive adhesive, hot melt, and curable adhesives may be useful in the practice of the invention.

The adhesives may be filled with various particulates and fillers to provide special functionality such as controlling the bond line thickness, providing electrical or thermal conductivity, or desiccating the interior of the packaged OLED device. Filled adhesives would include thermally conductive adhesive such as 9882 Thermally-Conductive Adhesive Transfer Tape available from 3M Bonding Systems Division; electrically conductive adhesives such as 9703 Conductive Adhesive Transfer Tape, 5303R Z-Axis Adhesive Film, and 7303 Z-Axis Adhesive Film, all of which are available from 3M Bonding Systems Division; and desiccant filled adhesives such as DESIMAX SLF Hot Melt films available from Multisorb Technologies Inc., Buffalo, NY. Filled adhesives may be used in conjunction with unfilled adhesives.

The adhesive may be applied to a release liner by any suitable coating method such as knife coating, extrusion, offset coating, spray coating, and curtain coating. The thickness of the adhesive will depend on the desired thickness of the finished product. Typical thicknesses for the adhesive structures range from about 500 to 0.05 micrometers. Thicknesses above or below this range may also be used as desired to suit the application.

Suitable release liner materials include polypropylene and fluoropolymer films, polymer films, such as polyester, coated with siloxanes or fluorocarbons, paper coated with siloxanes or fluorocarbons, metal foils coated with siloxanes or fluorocarbons, and metallized polymer films, such as metallized polyester, coated with siloxanes or fluorocarbons. The choice of liner will be dependent on its compatibility with subsequent processing steps.

Patterns may be cut through the adhesive-coated liner by die cutting, laser cutting or other precision cutting methods such as kiss cutting. The patterns may be any desired

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shape. More than one shape may be cut into a single sheet of adhesive-coated liner. Additionally, the shapes and sizes of material removed from the adhesive and liner need not be the same. For example, a square area may be removed from the adhesive layer while a smaller star-shaped area of the liner, located within the square area of the removed adhesive, may be removed from the liner layer such that after the OLED layers have been deposited through the star-shaped opening in the liner, a gap exists between the finished star-shaped OLED and the surrounding adhesive structure.

As shown in Figure 10, multiple layers of adhesives and liners may be used where each adhesive/liner layer has differently shaped openings to allow depositions in different areas at different stages of the fabrication process. Adhesive/liner mask layers **14a, 15a** closest to the deposition substrate will typically have a larger opening than adhesive/liner mask layers **14b, 15b** placed on top of layers **14a, 15a**. In Figure 10, the organics for an OLED would be deposited onto ITO anode **46** with both adhesive/liner masks in place. Adhesive/liner mask layers **14b, 15b** would then be removed and the cathode would be deposited through adhesive/liner mask layers **14a, 15a.** Liner **15a** would be removed and replaced with a protective layer. The cathode would thus contact the ITO cathode pad **48** without any electrical shorts to the ITO anode **46**. Attaching the anode lead **46** and cathode lead **48** to a power supply would allow the final encapsulated OLED to operate. Adhesive/liner mask layers **14b, 15b** could be removed after depositing one set of organic layers and be replaced by different adhesive/liner mask layers that had a different size or shape mask opening than adhesive/liner mask layers **14b, 15b**. This would allow for more complex deposition patterns to be obtained, such as those required for multi-color devices. This could be particularly effective in a roll-to-roll process.

The patterned adhesive-coated liner may be applied by any convenient method, *e.g.*, lamination methods such as hot, cold, pressure, and vacuum lamination, to a substrate thereby forming a mask on the substrate. Figure 1 illustrates a substrate **12** having a patterned transfer adhesive **14** with liner mask **15**. Transfer adhesive **14** and liner mask **15** both have openings **18** that extend through to substrate **12**. Cut lines **32** exemplify the location at which the finished sheet of devices will be singulated.

An alternative method of applying an adhesive layer to the substrate is to deposit a liquid adhesive by precision methods such as ink jet or screen printing in a desired pattern thereby leaving areas of substrate exposed, optionally partially curing or drying the

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adhesive to reduce flow and prevent adhesive migration, then covering the adhesive with a solid film liner layer that has complementary patterned openings. By this method, the openings in the liner mask may be made bigger or smaller than the underlying exposed substrate area. The ability to make the liner mask and OLED structure different sizes can be advantageous. For example, to prevent electrical shorting it may be advantageous to make the interior OLED elements cover a larger area than the bottom and/or top electrode so the electrodes do not touch. In other instances, it may be preferable to make the mask openings smaller than the electrodes.

Figure 11 shows another construction method to avoid electrical shorting in an OLED. The method comprises evaporating, for example, organic layers **16**, from direction A, and cathode layers **17**, from direction B, onto substrate **12** which is coated with ITO anode **46** and ITO cathode pad **48**. The shadowing effects of adhesive/liner mask **14/15** would allow for selective deposition of organic and cathode layers near the edges of the mask. This may be particularly effective when the opening in adhesive **14** is larger than the opening in liner **15**.

Once adhesive/liner mask **14/15** is applied, one or more OLED elements may be deposited onto the masked substrate by any suitable coating method such as vacuum deposition, solution coating, and thermal transfer. These coating methods are further described in copending patent application USSN 09/389926, pp. 7-10. The layers of individual OLED elements may be from about 200 to about 5000 Å thick. In some cases, the thickness of the combined layers is approximately equal to the thickness of adhesive layer **14**, for example when the final applied film is a metal foil that is a cathode or that makes electrical contact with the cathode layer. Having the thicknesses of the adhesive and OLED element layers be equal is also preferable when the adhesive does not flow much during bonding. This is typically true of pressure sensitive adhesives. However, when the adhesive flows well during bonding, as is typical with hot melt or curable adhesives, the thickness of the bond line, *i.e.*, the final thickness of the adhesive when the bond is complete, can be controlled by adjusting the curing chemistry and the bonding conditions, which control the flow of the adhesive, or by adding filler particles of a specific size, which thereby define the bond line thickness. Methods known in the art can be used to control the flow of the adhesive to obtain such adjustments. In such a case, the thickness of the adhesive may be greater than that of the OLED element layers.

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A preferred encapsulated OLED structure may have conducting leads, such as indium tin oxide (ITO) leads extending under the bond line and making electrical contact with the anode and cathode as shown in Figures 6 and 7. In this case, the encapsulating film, *i.e.*, the final top layer, would not need to act as an electrical contact. In some embodiments, leaving a gap between the protective layer and OLED, as is shown in Figures 6 and 7 may be desirable, for example when including a desiccant in the gap or when protecting the OLED from abrasion is desired. This may be achieved by having the adhesive layer substantially thicker than the OLED element layers.

The OLED element coating process may be conducted in a controlled atmosphere such as nitrogen, argon, or vacuum. This conveniently allows OLEDs to be made with air- and water-sensitive materials such as the electroluminescent materials comprising OLEDs as described herein. The process allows the production of an encapsulated OLED that has not been contaminated by exposure to air. Subsequent lamination of the coated substrate to a sealing layer may provide a finished OLED that is edge-sealed and has enhanced structural stability.

The suitability of a particular counter electrode, which may be used as a sealing layer, will depend on the desired application and the other OLED elements. Examples of cathode counter electrode materials include calcium, lithium, aluminum, ITO, barium, ytterbium, samarium, magnesium/silver alloys, and multiple layer structures such as calcium/aluminum and copper phthalocyanine/ITO. Examples of anode counter electrode materials include ITO and gold. It is preferred that at least one counter electrode be transparent. Alternatively, the counter electrode may be coated onto the OLED construction as are the other OLED elements, after which a protective layer may be laminated over the counter electrode layer.

A sealing protective layer for an OLED may comprise, *e.g.*, dielectric/polymer and metal/polymer layered composite films (sometimes referred to as polymer multilayer, or PML, films) such as those described in WO 00026973, US 5,725,909, US 4,954,371, and *Thin Solid Films*, **1997**, *308-309* 19-25, metal foils, metallized polymer films, dielectric coated polymer films such as SiO_x coated polymer films (TECHBARRIER S available from Mitsubishi Chemical Corporation, Tokyo), thin flexible glass such as 0.03 mm thick D 263 T glass available from Schott Displayglas GmbH, Mainz, Germany, and thin glass adhesively laminated to polymer films as described in WO 99/21708, metal plates, glass

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plates, plastic plates, and fluoropolymer films such as ACLAR films available from Allied Signal Inc., Specialty Films, Pottsville, PA. Rigid protective layers, such as metal, glass, or plastic plates, may be more suited for batch OLED manufacturing processing. Flexible barrier films, such as thin glass, multilayer polymer films, such as those described in U.S. Pat. No. 4,954,371, metal foils, and metallized polymers may be preferred in many instances because they can be used in a roll-to-roll process as well as in a batch process. Depending on the intended use of the OLED, the protective layer need not necessarily be transparent or conducting.

Figure 2 illustrates an embodiment of an OLED construction after sealing layer **30** has been applied. Cut lines **32** are shown. Cut lines **32** indicate where the structure can be cut through the layers of sealing layer **30**, transfer adhesive **14** and substrate **12** to provide individual OLEDs **10** such that the OLED elements **16** are encapsulated by adhesive **14** and sandwiched between substrate **12** and sealing layer **30**.

An exploded view of an exemplary individual OLED structure made by the foregoing method is shown in Figure 3. Adhesive **14** on substrate **12** surrounds OLED elements **16**. Sealing layer **30** forms the top layer of OLED construction **10**. A conventional OLED construction without the encapsulating structure of the present invention is shown in Figure 5.

Suitable OLED substrates **100** include glass, transparent plastics such as polyolefins, polyethersulfones, polycarbonates, polyesters, polyarylates, and polymeric multilayer films, ITO coated barrier films such as the Plastic Film Conductor available from 3M Optical Systems Division, surface-treated films, and selected polyimides. It is highly desirable that the OLED substrate has barrier properties matching those of the protective (or counter electrode) film. Flexible rolls of glass may also be used. Such a material may be laminated to a polymer carrier for better structural integrity.

The anode material **102** coating the substrate is electrically conductive and may be optically transparent or semi-transparent. Suitable anode materials include indium oxide, ITO, fluorine tin oxide (FTO), zinc oxide, vanadium oxide, zinc-tin oxide, gold, platinum, palladium silver, other high work function metals, and combinations thereof.

The lamp elements that may be deposited on the masked anode-coated substrate include an optional hole injecting layer **104**, a hole transporting layer **106**, a light emitting

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layer **108**, an electron transporting layer **110**, an optional electron injecting layer **112**, and a second electrode (cathode) **114**.

Suitable materials for the optional hole injecting layer **104**, which accepts holes from the anode and transmits them to hole transporting layer, include porphyrinic compounds, *e.g.*, copper phthalocyanine (CuPc), zinc phthalocyanine, acid doped poly(ethylenedioxythiophene) (PEDOT), and acid doped polyaniline.

Suitable materials for the hole transporting layer **106**, which facilitates the movement of holes from the anode layer **102** to the emitter layer **108**, include, *e.g.*, aromatic tertiary amine materials described in U.S. Pat. Nos. 5,374,489 and 5,756,224, such as 4,4',4"-tri(N-phenothiazinyl)triphenylamine (TPTTA), 4,4',4"-tri(N-phenoxazinyl)triphenylamine (TPOTA), N,N'-bis(3-methylphenyl)-N,N'-diphenyl benzidine (TPD), and polyvinyl carbazole.

Suitable materials for the emitter layer **108**, in which the holes and electrons combine to produce light, include, *e.g.*, tris(8-hydroxyquinolinato)aluminum (AlQ). The emission of light of different colors may be achieved by the use of different emitters and dopants in the emitter layer as described in the art (*see* C.H. Chen, J. Shi, and C.W. Tang "Recent Developments in Molecular Organic Electroluminescent Materials," *Macromolecular Symposia* **1997** *125*, 1-48).

Suitable materials for the electron transporting layer **110**, which facilitates the movement of electrons from the cathode to the emitter layer, include, *e.g.*, AlQ, bis(10-hydroxy-benzo(h)quinolinato) beryllium, bis(2-(2-hydroxy-phenyl)-benzolthiazolato) zinc, 3,4,5-triphenyl-1,2,4-triazole, 2-(4-biphenylyl)-5-(4-*t*-butylphenyl)-1,3,4-oxadiazole, and combinations thereof.

Suitable materials for the optional electron injecting layer **112**, which accept electrons from the cathode and transmit them to the electron transporting layer, include metal fluorides such as LiF, CsF, as well as SiO_2, Al_2O_3, copper phthalocyanine (CuPc), and alkaline metal compounds comprising at least one of Li, Rb, Cs, Na, and K such as alkaline metal oxides, alkaline metal salts, *e.g.*, Li_2O, Cs_2O, and $LiAlO_2$.

Suitable materials for the cathode **114**, which provides electrons, include, *e.g.*, LiF, Mg, Ca, Ag, Al, Li, Ba, Yb, Sm, and other low work function metals, alloys of Ca and Mg, ITO, FTO, zinc oxide, and lithium,.

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Alternatively, one or more layers of light emitting polymers such as poly(phenylenevinylene)s (PPV), polyfluorenes, and other light emitting polymers known in the art may replace layers **106**, **108**, and **110**.

Once all of the desired OLED elements have been deposited, the liner may be removed to provide a substrate with an OLED construction surrounded by adhesive. Subsequent covering or sealing of this coated substrate with a protective layer would provide an OLED that is edge-sealed and has enhanced structural (and environmental) stability. Alternatively, the cathode layer may comprise a sheet of material that is applied to the adhesive matrix after the preceding OLED element layers have been deposited and the release liner has been removed. If a sheet of cathode layer material is used, this cathode layer can also serve as a sealing layer that provides edge sealing of the OLED structure. In such a case, no additional protective layer would be necessary.

The process of the present invention could be readily carried out using a roll-to-roll continuous web process as illustrated by Figure 4. For example, to prepare an OLED, a roll of flexible substrate **12** with precut adhesive-coated liner mask **14/15** could be fed from roll **230** into vacuum chamber **210** of coater **200** where OLED elements could be deposited by vaporization from deposition sources **220** and **222**, which may deposit the first two organic layers of an OLED, corresponding, for example, to layers **104** and **106** of the device shown in Figure 5. Alternatively, deposition source could furnish ITO anode layer **102** of Figure 5. This step would be followed by a second set of vapor depositions in chamber **212** from deposition sources **224** and **226**. Typically, deposition sources **220** to **226** will supply all of the layers necessary to produce a working OLED device on substrate **12**. It will be obvious to one of skill in the art that the number of deposition sources in processing line **200** may vary according to the OLED device to be built. This step will be followed removal of release liner **15** onto take-up roll **232** in take-up chamber **214** and application of sealing layer **30** from roll **234** onto exposed adhesive mask **14** to encapsulate and protect the OLED device. Sealing layer **30** may be a counter electrode or a protective layer, depending on the particular construction of the OLED device. Take-up chamber **214** can be under vacuum or can be at atmospheric pressure and filled with an inert atmosphere, such as argon or nitrogen. It will be obvious that the number of vacuum and take-up chambers may vary according to the desired set of process conditions. The finished sheet of OLED devices is then collected on take-up roll **236** from which it can be

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further dispensed for conversion into individual OLEDs by singulation, as shown in Figures 1-3. Other arrangements and combinations of applied layers are also possible and would be apparent to one skilled in the art. The entire process could be carried out in a controlled atmosphere, such as under a vacuum or nitrogen, to minimize the possibility of environmental damage to the OLED. The finished sheet of OLEDs could be removed from the coater and converted to individual OLEDs by cutting through the adhesively-bonded areas of the electrode and substrate films to give the final (or at least partially) packaged OLED of the general structure shown in Figure 3. Further encapsulation may also be done after fabrication. For example, after an electrode or protective layer is laminated to the OLED structure, an additional protective encapsulating layer may be added by, for example, dipping the entire assembly into a liquid epoxy resin and curing said resin by heat and/or light.

The roll-to-roll process may be a solution process, a thermal transfer process, a vacuum process, or various combinations thereof. For example, a conducting polymer buffer layer, such as PEDOT, could be solution coated (knife coat, curtain coat, micro gravure coat, screen printed, etc.) onto an ITO deposition substrate **12** with the adhesive/liner mask **14/15** in place. After drying, the organic OLED layers and the cathode layers could be deposited by vacuum deposition in chambers **210** and **212** onto the moving web. Liner mask **15** would then be removed to take-up reel **232** and in its place protective layer **30** would be laminated to the newly formed OLED film to produce a roll of encapsulated OLED devices ready for singulation. Alternatively, OLED layers may be solution coated (knife coat, curtain coat, micro gravure coat, screen printed, *etc.*) onto an ITO deposition substrate with the adhesive/liner mask in place. After drying, the cathode layers may be deposited by vacuum deposition onto the moving web. The liner mask could be removed to a take-up reel and in its place a protective layer would be laminated to the newly formed OLED film to produce a roll of encapsulated OLED devices ready for singulation.

The roll-to-roll process may be done on a continuously moving web or it may be accomplished by a step-and-repeat roll-to-roll process. A step and repeat process could allow for more precise thickness control during the various vacuum deposition steps and could enable the use of more complex and finer featured shadow masks during the vacuum deposition steps. Different shadow masks could be easily moved in and out of position

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during the deposition of the various layers while still maintaining the convenience of a roll-to-roll process. Step-and-repeat web processing will likely be slower than continuous web processing. A web with sprocket holes along the edges may be advantageous in step-and-repeat and continuous web processing.

The use of the in situ edge seal adhesives of the current invention can provide structural stability to OLEDs prepared by physical lamination of two substrates carrying the appropriate active layers. Although there are several ways to apply the current invention to the fabrication of OLEDs by lamination, only one will be exemplified herein. Such fabrication is illustrated by Figure 12. For structure **300**, adhesive/liner mask **314/315** may be placed on the metallized side of a polyester film **310** coated with aluminum **312** and placed into a vacuum deposition chamber. Approximately 5,000 Å of aluminum **316**, 10 Å of LiF **318**, 400 Å of AlQ **320**, and 400 Å of 4,4'-bis(naphthalen-2-yl)-N-N- diphenyl benzidine (α-NPD) **322** can be deposited in that order. Separately, for structure **400**, polyester substrate **328** coated with ITO layer **326** can be coated with 1,000 Å of aqueous poly(ethylenedioxythiophene) (PEDOT) solution **324** and allowed to dry. Both film structures may be transferred to an inert atmosphere glove box. Liner **315** may be removed from structure **300**, which structure **300** may then be laminated by heat and pressure to structure **400**. Completed OLED device **500** would thus be formed where an interface between active layers **322** and **324**, in this example between a hole injecting layer and a hole transport layer, would be created by physical lamination of these two layers. The completed device has improved structural stability by virtue of the adhesive forming the in situ edge seal around the device.

Finely patterned and addressable devices may be fabricated by the methods of the current invention. For example, a passively addressable monochrome dot matrix display may be fabricated in a roll-to-roll process. ITO on polyester could be patterned by a combination of standard photolithography and acid etching into columns that run across the web. An adhesive/liner mask which contains rectangular openings that define the desired area of the display would be applied to the web. Small molecule OLED layers would be vacuum deposited onto the web or light emitting polymers solution coated onto the web to essentially cover the rectangular opening in the adhesive/liner mask. Cathode metal would then be vapor deposited through a slotted mask to create rows of cathode metal parallel to the web direction. The liner would then be removed and a protective film

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laminated to the passive matrix display. Electrical connection to the anode would be simply made by contacting the columns of ITO that pass underneath the encapsulating adhesive. Electrical connection to the cathode rows could be made in a number of ways. The protective film laminated to the cathode side of the device could carry conductive traces that could be in registration with the rows of anode. These could be in physical contact with the cathode rows or could be attached by, for example, a Z-axis conductive adhesive film. Alternatively, the ITO substrate could be patterned to include ITO cathode contact pads, which pass underneath the encapsulating adhesive. The cathode rows can be contacted to these pads by, for example, the use of various deposition masks or by angle evaporation techniques.

This invention may also be useful to temporarily protect an OLED or a partial OLED device. Copending U.S. patent application 09/231723 describes the use of OLED donor sheets to create OLED devices by thermal transfers. These donor sheets may benefit from protection from the atmosphere to increase their shelf life. An adhesive/liner mask could be applied to a donor substrate prior to the deposition of the desired OLED layers. The liner could be removed and a protective film could be applied before the donor sheets are exposed to oxygen or moisture. The protective film could be removed from the donor film immediately prior to thermally imaging the donor sheet thereby minimizing or eliminating the exposure of the donor sheet to oxygen and moisture. It would be preferred that the donor substrate also have good oxygen and moisture barrier properties.

Another unforeseen advantage of the current invention is protection of the OLED and electrode layers from damage in a roll-to-roll process. The adhesive/liner mask will generally be thicker in the z direction than the various OLED and electrode layers. When the front face of the OLED film passes over various rollers in the web handling system required for a roll-to-roll process, the adhesive/liner mask can prevent or minimize the contact between the active OLED layers and these rollers. Furthermore, when the finished OLED film is wound up on the final take-up reel or "jumbo" roll, the adhesive/liner mask or the laminated protective film can prevent or minimize pressure induced damage to the OLED devices (or thermal donor films) as they are wound up on the final take-up reel.

It is also possible to establish electrical connections on the completed structure by removing some adhesive material from the outer edges of the OLED structure. When

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anode and cathode leads are in the form of ITO or other conductive paths that pass under the adhesive bond line, electrical connections to drive the device are made by attaching the leads to a power supply or drive electronics. It may be desirable to remove portions of the protective layer and adhesive, which may cover these leads, to facilitate attachment of the power supply or drive electronics.

EXAMPLES

Unless otherwise specified, all chemicals were obtained from Eastman Kodak, Rochester, NY.

Example 1.

Figures 6 and 7 show an ITO-coated glass substrate, 5 cm x 7.6 cm x 1 mm (Thin Film Devices, Inc., Anaheim, CA) **42**. The ITO coating **44** was divided into two strips of conductive areas **46** and **48** by removing a portion of the ITO coating approximately 10 mm wide across the width of the glass substrate by acid-etching. In addition, ITO was removed along the outer lengths of the substrate such that strip **46** was wider than strip **48**, as illustrated in Figure 7. A portion of the substrate approximately 10 mm x 20 mm that spanned portions of both ITO strips **46** and **48** was isolated by hand-laminating onto the substrate a piece of pressure-sensitive adhesive transfer tape (3M™ Ultra Pure Viscoelastic Damping Polymer 242F01, 3M Company, St. Paul, MN) **50** having a release liner on its upper side (not shown) from which a central hole area had been removed, to form a shape like a picture frame. The upper release liner of adhesive **50** remained in place. Glass substrate **42** was rinsed with methanol and dried under a nitrogen flow, then placed in a spin-coater, covered with xylene, and spun dry. An aqueous solution of poly(ethylenedioxythiophene) (PEDOT) conductive polymer (BAYTRON, Bayer Corp., Pittsburgh, PA) **52** was applied to the cut-out area, spun-coated at 5000 rpm for 20 seconds, then dried at 100° C on a hotplate for 15 minutes. The coated slide was immediately placed in an evaporator vacuum chamber and the chamber was sealed and evacuated to approximately 10^{-5} torr. A light-emitting construction was prepared on the PEDOT surface by vacuum deposition, in the following order, of: 100 Å layer of copper phthalocyanine (CuPc), at 1 Å/sec; 200 Å 4,4'-bis(naphthalen-2-yl)-N,N'- diphenyl

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benzidine (α-NPD) hole transport layer, at 3 Å/sec; 350 Å tris(8-hydroxyquinolinato)aluminum (AlQ) doped at approximately 1% during the first 200 Å with a coumarin dye (C545T™) electron transport layer, at 2 Å/sec; 10 Å lithium fluoride, at 1 Å/sec; and 4000 Å aluminum, at 10 Å/sec, thereby creating organic thin films layer **54** and cathode layer **56**.

In the vacuum chamber, organic layers **54** (CuPc, α-NPD, and AlQ and coumarin dye) were coated directionally from one end of the chamber and a LiF/aluminum cathode **56** from the opposite end of the chamber. Deposition of organic layers **54** was shaded on one end of the coated substrate by the sample holder (not shown), leaving portions of strips **46** and **48** uncoated. Deposition of LiF/aluminum cathode **56** from the opposite end of the chamber allowed some of the LiF and aluminum to be deposited on the uncoated portion of the ITO layer **48**, providing an electrical contact.

The device was removed from the vacuum chamber and placed in a glove box under nitrogen. The upper liner was removed from the adhesive 'frame' **50** that surrounded the deposited lamp, and a clean glass cover slide **58** was pressed in place on the exposed adhesive, completely covering the lamp while leaving ITO strips **46** and **48** exposed on each end of the substrate. The covered device was removed from the glove box and tested by connecting an electrical power source to ITO strips **46** and **48**. Light was emitted from the lamp when current was passed through the contacts.

Example 2.

Figures 8 and 9 show an ITO-coated glass substrate, 5 cm x 7.6 cm x 1 mm (Thin Film Devices, Inc., Anaheim, CA) **72**. Using standard electron beam evaporation methods, a layer of Al_2O_3 approximately 1000 Å μm thick **74** was deposited on the ITO **76** using a shadow masking method that left an approximately 10 mm x 20 mm area of uncovered ITO **76a** in the middle of substrate **72** and approximately 10 mm uncovered at one end of the substrate.

An electroluminescent lamp was constructed on the substrate as described in Example 1, wherein a portion of the Al_2O_3 surrounding the central ITO area was surrounded by a pressure-sensitive adhesive transfer tape **78**, and a lamp was prepared in the interior isolated area by depositing PEDOT layer **86** and organic films layer **80** and

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aluminum anode layer **82**. In the nitrogen glove box, the lamp was sealed by placing a sample of clean aluminum foil **84** on the exposed adhesive and in contact with the upper aluminum layer **82** of the lamp.

The device was removed from the glove box and tested by connecting an electrical power source to the aluminum foil encapsulating layer **82** (as the cathode) and to the uncovered ITO strip **76b** at the end of the substrate (as the anode). Light was emitted from the lamp when current was passed through the contacts.

In the foregoing description, certain terms have been used for brevity, clarity, and understanding. No unnecessary limitations are to be implied therefrom beyond the requirement of the prior art because such terms are used for descriptive purpose and are intended to be broadly construed. Moreover, the description and illustration of the invention is by way of example, and the scope of the invention is not limited to the exact details shown or described.

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What is claimed is:

1. A method for making an organic electronic device comprising:

a. providing an adhesive-coated release liner from which a pattern has been cut,

b. applying the adhesive-coated side of the patterned release liner to an electrode substrate to form a composite structure having at least a portion of the electrode substrate exposed,

c. depositing one or more organic electronic elements on the exposed electrode of the composite structure,

d. removing the release liner from the composite structure, and

e. adhering a sealing layer to the exposed adhesive of the composite structure.

2. A method for making an organic electronic device comprising:

a. coating an adhesive in a pre-determined pattern on an electrode substrate to form a composite structure wherein areas of the substrate remain exposed;

b. applying a mask or release liner to the patterned adhesive such that at least a portion of the exposed substrate areas remain exposed;

c. depositing one or more organic electronic elements on the composite structure;

d. removing the mask or release liner from the adhesive; and

e. applying a sealing layer.

3. The method of claim 1 or 2 wherein a protective film is applied to the composite structure after the release liner is removed, which protective film is removed prior to adhering of the sealing layer.

4. The method of claim 1 or 2 wherein the adhesive-coated liner is thicker in the z direction than the organic electronic elements.

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5. The method of claim 1 or 2 wherein the adhesive is selected from the group comprising hot melt adhesives, pressure sensitive adhesives, curable adhesives, and filled adhesives.

6. The method of claim 5 wherein the filled adhesive is selected from the group comprising electrically conductive adhesives, thermally conductive adhesives, and desiccating adhesives.

7. The method of claim 6 wherein the filled adhesive is used in conjunction with an unfilled adhesive.

8. The method of claim 1 or 2 wherein the adhesive-coated liner is selected from the group comprising polypropylene films, metal foils coated with siloxanes or fluorocarbons, polyester coated with siloxanes or fluorocarbons, and fluoropolymer films.

9. The method of claim 1 or 2 wherein multiple adhesive-coated liners are applied to the electrode substrate and are removed at different stages during organic electronic element deposition.

10. The method of claim 2 wherein the adhesive is one or both of partially cured and dried between a. and b.

11. The method of claim 1 or 2 wherein the sealing layer is a counter electrode.

12. The method of claim 11 wherein the material comprising the counter electrode is selected from the group comprising lithium fluoride, calcium, aluminum, barium, ytterbium, samarium, lithium, indium tin oxide, fluorine tin oxide, zinc oxide, magnesium, silver, gold, and alloys of calcium and magnesium.

13. The method of claim 1 or 2 wherein the sealing layer comprises a partial organic electronic device construction that is laminated to the composite structure.

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14. The method of claim 1 or 2 wherein a counter electrode layer is applied after the final organic element layer and the sealing layer is a protective layer.

15. The method of claim 14 wherein the adhesive-coated liner is thicker in the z direction than the organic electronic elements and the counter electrode layer.

16. The method of claim 14 wherein the material comprising the protective layer is selected from the group comprising metallized polymer films, polymer multilayer films, metal plates, foils, and thin flexible glasses.

17. The method of claim 15 wherein the material comprising the counter electrode is selected from the group comprising lithium fluoride, calcium, aluminum, barium, ytterbium, samarium, lithium, indium tin oxide, fluorine tin oxide, zinc oxide, calcium, magnesium, silver, gold, and alloys of calcium and magnesium.

18. The method of claim 2 further comprising the step of fully curing the adhesive after the device has been constructed.

19. The method of claim 1 or 2 wherein the organic electronic device is an organic light emitting diode.

20. The method of claim 19 wherein the substrate is selected from glass and polymer multilayer films, the anode comprises indium tin oxide, the hole transporting layer comprises 4,4'-bis(naphthalen-2-yl)-N,N'-diphenyl benzidine, the light emitting layer comprises coumarin-doped tris(8-hydroxyquinolinato)aluminum, the electron transporting layer comprises, and the cathode comprises lithium fluoride and aluminum.

21. An article comprising an organic electronic device wherein the layers between the anode and cathode are surrounded by an adhesive layer and wherein the circumference of the adhesive layer is equal to the circumference of one or both of the electrode substrate or sealing layer.

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22. The article of claim 21 wherein the circumference of the adhesive layer is greater than that of an electrode.

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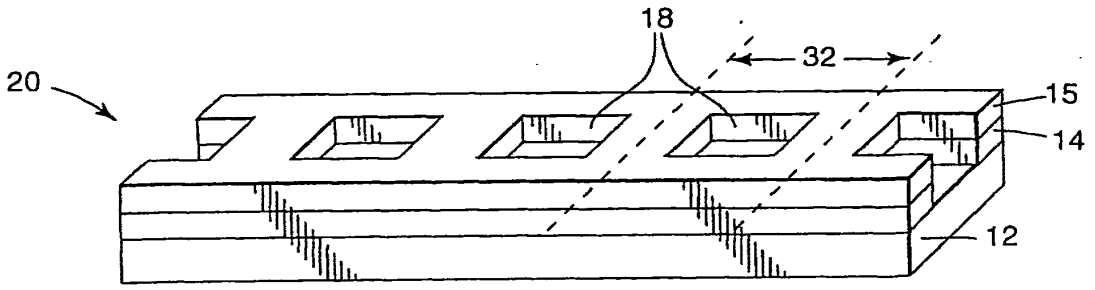


Fig. 1

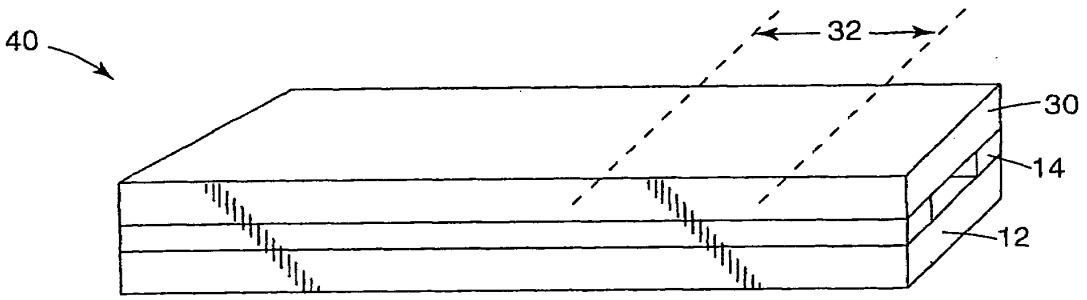


Fig. 2

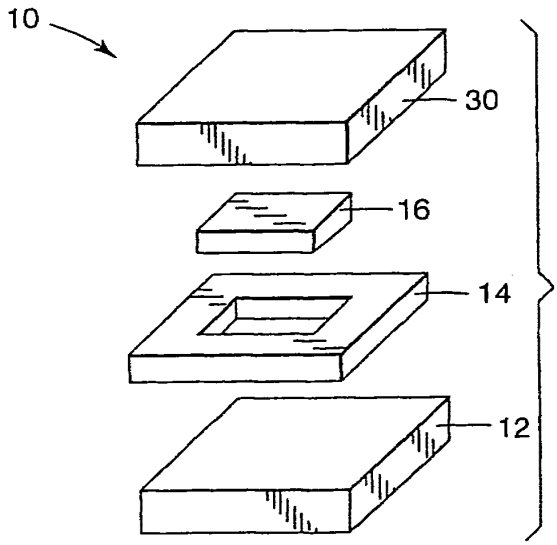


Fig. 3

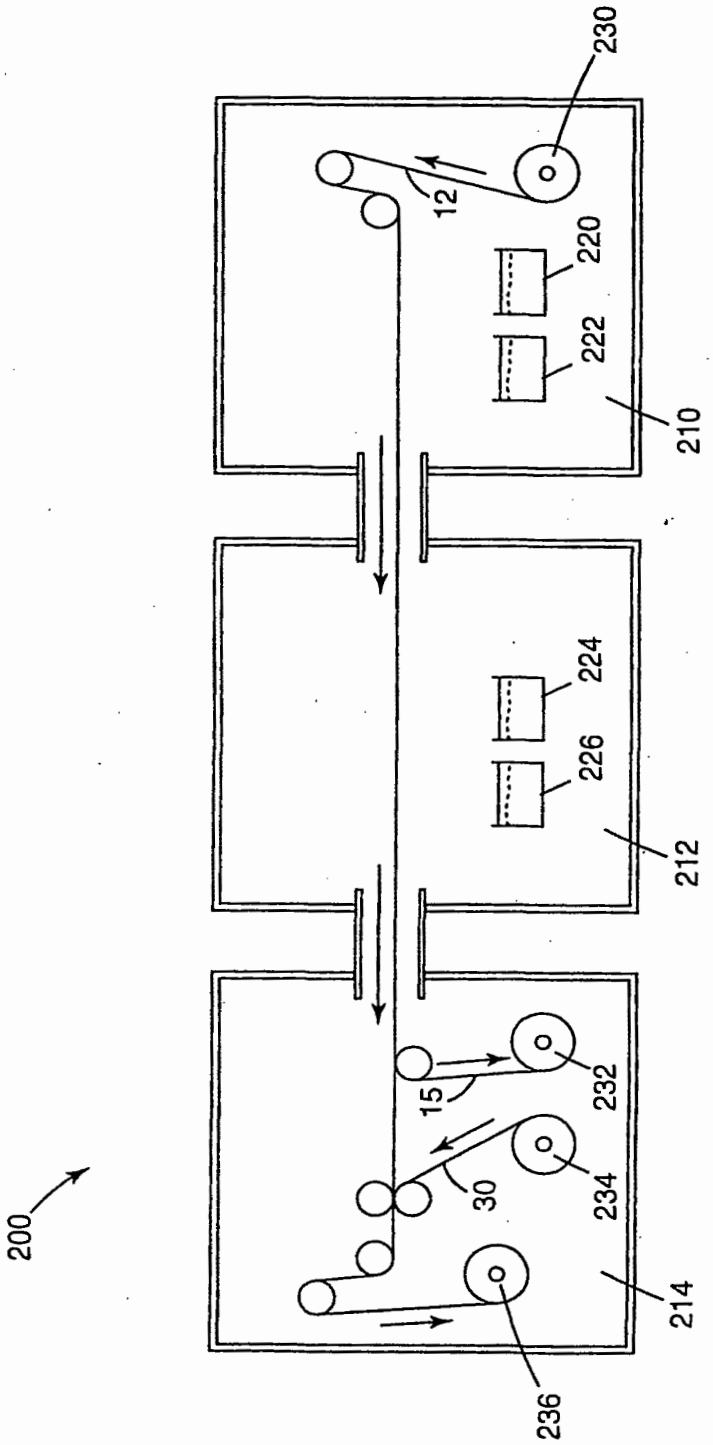


Fig. 4

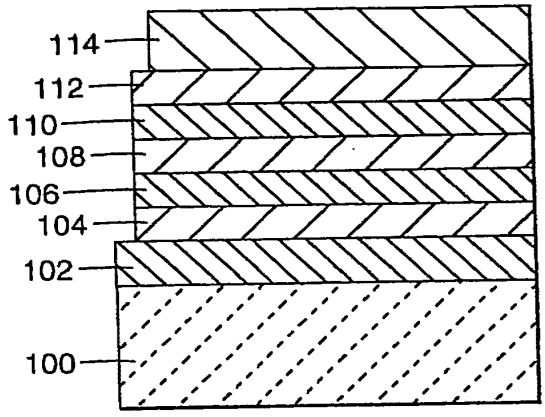


Fig. 5

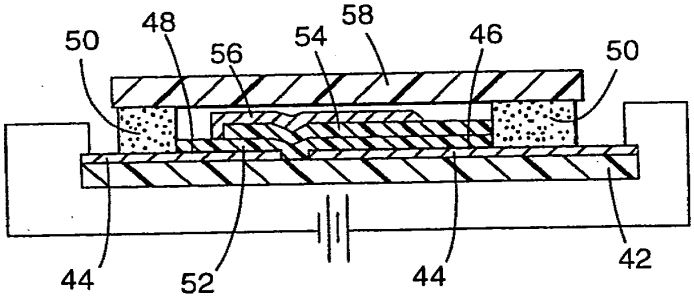


Fig. 6

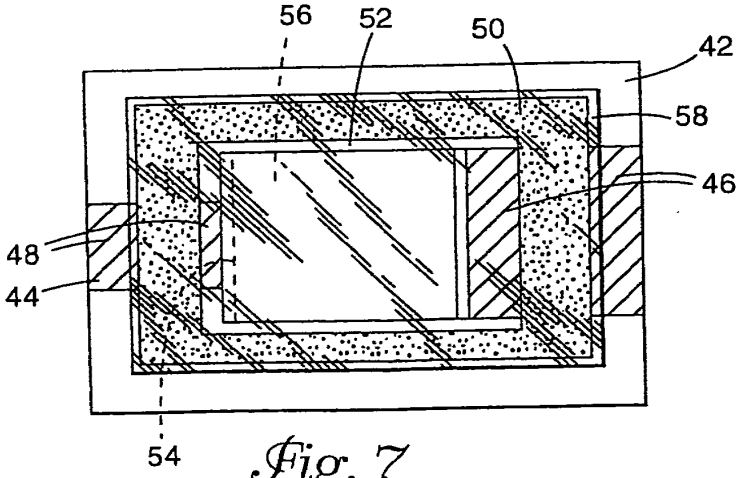


Fig. 7

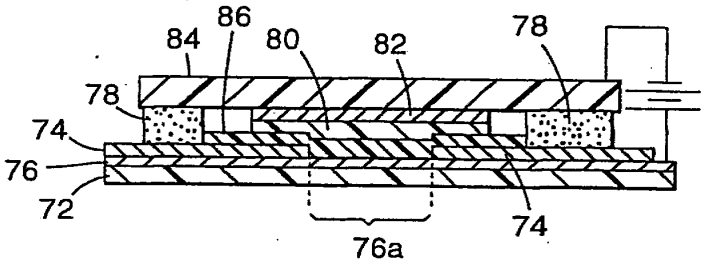


Fig. 8

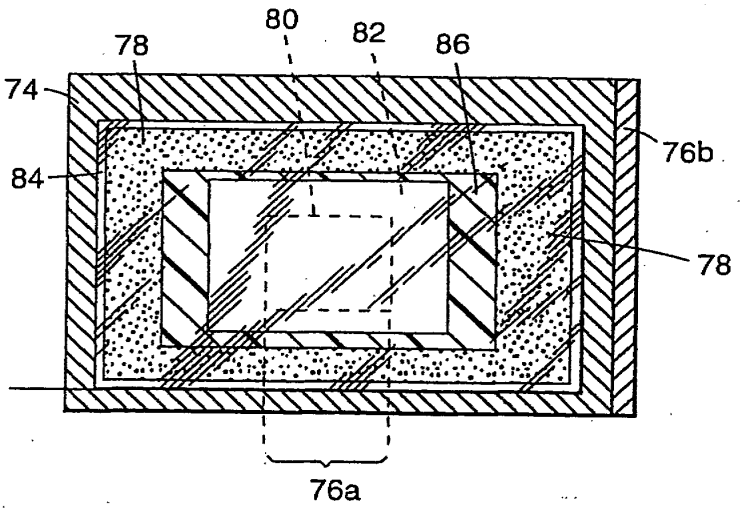


Fig. 9

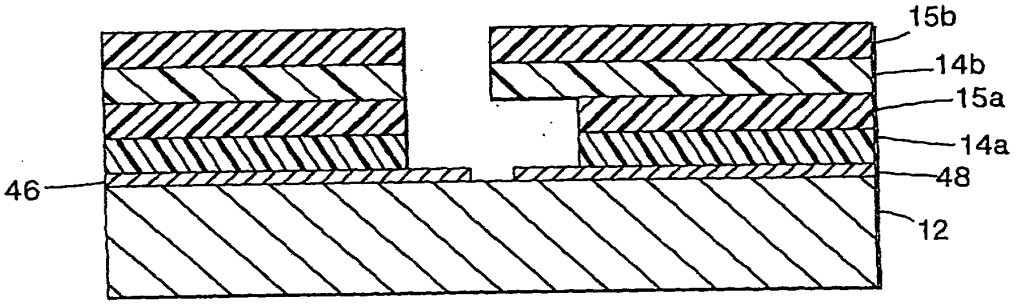


Fig. 10

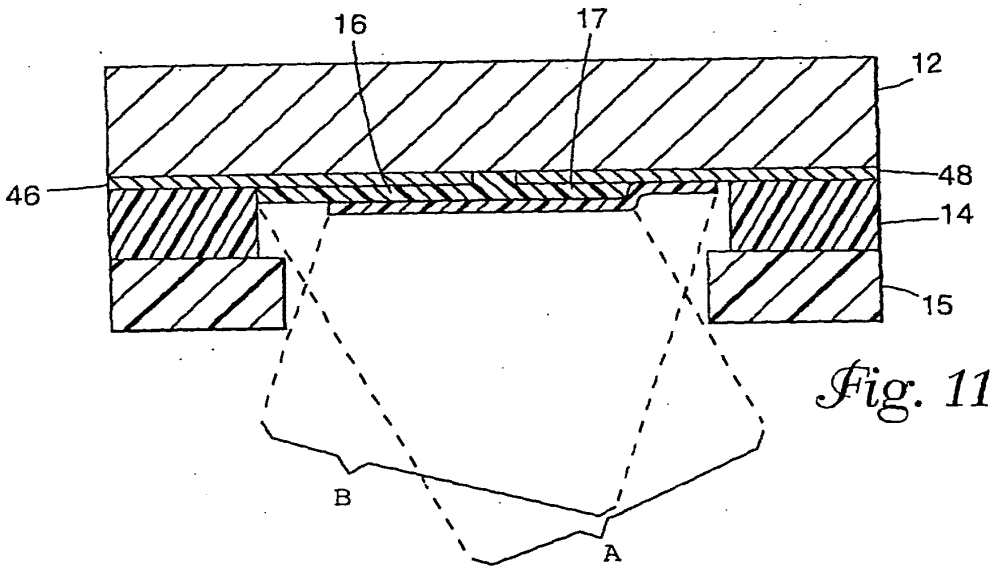


Fig. 11

Fig. 12a

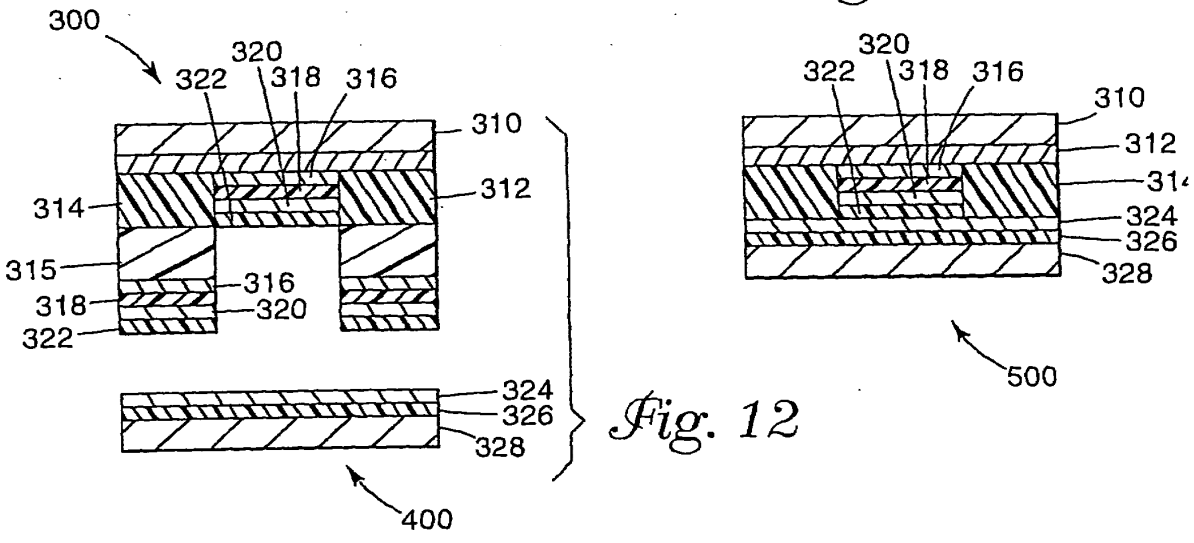


Fig. 12

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 00/31393

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L51/20 H01L51/40 H05B33/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 786 664 A (LIU YOUMIN) 28 July 1998 (1998-07-28) column 3, line 12 -column 4, line 60 ---	21
A	EP 0 884 930 A (IDEMITSU KOSAN CO) 16 December 1998 (1998-12-16) the whole document ---	1,2,4,5, 11-17, 19-21
A	EP 0 762 806 A (MOTOROLA INC) 12 March 1997 (1997-03-12) the whole document --- -/--	2,4,10, 11, 13-17, 19,20

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 May 2001	07/06/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	van der Linden, J.E.

Form PCT/ISA/210 (second sheet) (July 1992)

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INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 00/31393

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	WO 00 05929 A (SEIKO EPSON CORP) 3 February 2000 (2000-02-03) -& EP 1 018 857 A (SEIKO EPSON CORP) 12 July 2000 (2000-07-12) the whole document	1,2,21, 22
P,X	EP 1 021 070 A (TDK CORP) 19 July 2000 (2000-07-19) the whole document	21,22

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

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INTERNATIONAL SEARCH REPORT

Inter nal Application No
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5786664 A	28-07-1998	NONE	
EP 0884930 A	16-12-1998	US 6175186 B WO 9731508 A	16-01-2001 28-08-1997
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EP 1021070 A	19-07-2000	JP 2000208252 A	28-07-2000

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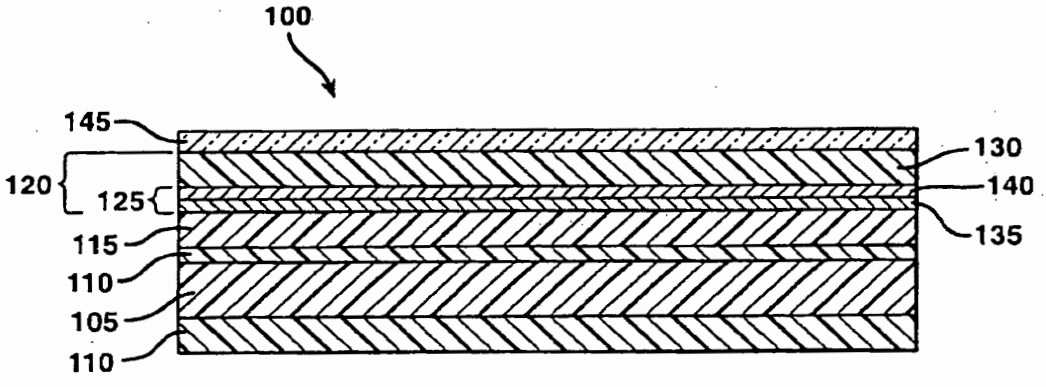
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(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: BARRIER COATING



(57) Abstract: A barrier assembly. The barrier assembly includes at least one barrier stack having at least one barrier layer and at least one polymer layer. The barrier stack has an oxygen transmission rate of less than 0.005 cc/m²/day at 23 °C and 0 % relative humidity, and an oxygen transmission rate of less than 0.005 cc/m²/day at 38 °C and 90 % relative humidity. The barrier stack also has a water vapor transmission rate of less than 0.005 g/m²/day at 38 °C and 100 % relative humidity. A method for making a barrier assembly is also disclosed.

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BARRIER COATING

The present invention relates generally to barrier coatings, and more particularly to barrier coatings having improved barrier properties.

Many different types of products are sensitive to gas and liquids, which can cause deterioration of the product or render it useless, including electronics, medical devices, and pharmaceuticals. Barrier coatings have been included in the packaging for these environmentally sensitive products to protect them from gas and liquid transmission. As used herein, the term environmentally sensitive means products which are subject to degradation caused by permeation of environmental gases or liquids, such as oxygen and water vapor in the atmosphere or chemicals used in the processing, handling, storage, and use of the product.

Plastics are often used in product packaging. However, the gas and liquid permeation resistance of plastics is poor, often several orders of magnitude below what is required for product performance. For example, the oxygen transmission rates for materials such polyethylene terephthalate (PET) are as high as 1550 $cc/m^2/day/micron$ of thickness (or 8.7 $cc/m^2/day$ for 7 mil thickness PET), and the water vapor transmission rates are also in this range. Certain display applications using environmentally sensitive display devices, such as organic light emitting devices, require encapsulation that has a maximum oxygen transmission rate of 10^{-4} to 10^{-2} $cc/m^2/day$, and a maximum water vapor transmission rate of 10^{-5} to 10^{-6} $g/m^2/day$.

Barrier coatings have been applied to plastic substrates to decrease their gas and liquid permeability. Barrier coatings typically consist of single layer thin film inorganic materials, such as Al, SiO_x, AlO_x, and Si_3N_4 vacuum deposited on polymeric substrates. A single layer coating on PET reduces oxygen permeability to levels of about 0.1 to 1.0 $cc/m^2/day$, and water vapor permeability to about 0.1 to 1.0 $g/m^2/day$, which is insufficient for many display devices.

Barrier coatings which include alternating barrier layers and polymeric layers have been developed. For example, U.S. Patent Nos. 5,607,789 and 5,681,666 disclose a moisture barrier for an electrochemical cell tester. However, the claimed

moisture barrier ranges from 2 to 15 micrograms/in^2/day which corresponds to a rate of 0.003 to 0.023 g/m^2/day. U.S. Patent No. 5,725,909 to Shaw et al. discloses a coating for packaging materials which has an acrylate layer and an oxygen barrier layer. The oxygen transmission rate for the coating was reported to be 0.1 cc/m^2/day at 23°C and the water vapor transmission rate was reported to be 0.01 g/m^2/day in D. G. Shaw and M. G. Langlois, Society of Vacuum Coaters, 37th Annual Technical Conference Proceedings, p. 240-244, 1994. The oxygen transmission rates for these coatings are inadequate for many display devices.

Thus, there is a need for an improved, lightweight, barrier coating, and for methods for making such a barrier coating.

The present invention meets these needs by providing a barrier assembly and a method for making such an assembly . The barrier assembly includes at least one barrier stack having at least one barrier layer and at least one polymer layer. The barrier stack has an oxygen transmission rate of less than 0.005 cc/m^2/day at 23°C and 0% relative humidity, and an oxygen transmission rate of less than 0.005 cc/m^2/day at 38°C and 90% relative humidity. It also preferably has a water vapor transmission rate of less than 0.005 g/m^2/day at 38°C and 100% relative humidity.

Preferably, the barrier layers of the barrier stacks are substantially transparent. At least one of the barrier layers preferably comprises a material selected from metal oxides, metal nitrides, metal carbides, metal oxynitrides, metal oxyborides, and combinations thereof.

The barrier layers can be substantially opaque, if desired. The opaque barrier layers are preferably selected from opaque metals, opaque polymers, and opaque ceramics.

The barrier assembly can include a substrate adjacent to the at least one barrier stack. By adjacent, we mean next to, but not necessarily directly next to. There can be additional layers intervening between the adjacent layers. The substrate can either be flexible or rigid. It is preferably made of a flexible substrate material, such as polymers, metals, paper, fabric, and combinations thereof. If a

rigid substrate is used, it is preferably a ceramic (including glasses), a metal, or a semiconductor.

The polymer layers of the barrier stacks are preferably acrylate-containing polymers. As used herein, the term acrylate-containing polymers includes acrylate-containing polymers, methacrylate-containing polymers, and combinations thereof. The polymer layers can be the same or different.

The barrier assembly can include additional layers if desired, such as polymer smoothing layers, scratch resistant layers, antireflective coatings, or other functional layers.

The present invention also involves a method of making the barrier assembly. The method includes providing a substrate, and placing at least one barrier stack on the substrate. The barrier stack includes at least one barrier layer and at least one polymer layer.

The at least one barrier stack can be placed on the substrate by deposition, preferably vacuum deposition, or by laminating the barrier stack over the environmentally sensitive device. The lamination can be performed using an adhesive, solder, ultrasonic welding, pressure, or heat.

Accordingly, it is an object of the present invention to provide a barrier assembly, and to provide a method of making such a barrier assembly.

Fig. 1 is a cross-section of one embodiment of the barrier assembly of the present invention.

Fig. 2 is a cross-section of an encapsulated device made using the barrier assembly of the present invention.

One embodiment of the barrier assembly of the present invention is shown in Fig. 1. The barrier assembly is supported by a substrate 105. The substrate 105 can be either rigid or flexible. A flexible substrate can be any flexible material, including, but not limited to: polymers, for example, polyethylene terephthalate (PET), polyethylene naphthalate (PEN), or high temperature polymers, such as polyether sulfone (PES), polyimides, or Transphan™ (a high glass transition temperature cyclic olefin polymer available from Lofo High Tech Film, GMBH of Weil

am Rhein, Germany); metal; paper; fabric; and combinations thereof. Rigid substrates are preferably glass, metal, or silicon.

There are scratch resistant layers 110 on either side of the substrate 105 to protect it. When a scratch resistant layer is included, it is preferred that both sides of the substrate have a scratch resistant layer. This helps to balance stresses and prevent deformation of a flexible substrate during processing and use.

On top of the scratch resistant layer 110, there is a polymer smoothing layer 115. The polymer smoothing layer decreases surface roughness, and encapsulates surface defects, such as pits, scratches, and digs. This produces a planarized surface which is ideal for subsequent deposition of layers. Depending on the desired application, there can be additional layers deposited on the substrate 105, such as organic or inorganic layers, planarizing layers, electrode layers, antireflective coatings, and other functional layers. In this way, the substrate can be specifically tailored to different applications.

The first barrier stack 120 is adjacent to the polymer smoothing layer 115. The first barrier stack 120 includes a barrier layer 125 and a polymer layer 130. The first barrier layer 125 includes barrier layers 135 and 140. Barrier layers 135 and 140 can be made of the same barrier material or of different barrier materials.

Although Fig. 1 shows a barrier stack with two barrier layers and one polymer layer, the barrier stacks can have one or more polymer layers and one or more barrier layers. There could be one polymer layer and one barrier layer, there could be one or more polymer layers on one side of one or more barrier layers, or there could be one or more polymer layers on both sides of one or more barrier layers. The important feature is that the barrier stack have at least one polymer layer and at least one barrier layer. The barrier layers and polymer layers in the barrier stack can be made of the same material or of a different material. The barrier layers are typically about 100-400 Å thick, and the polymer layers are typically about 1000-10,000 Å thick.

Although only one barrier stack is shown in Fig. 1, the number of barrier stacks is not limited. The number of barrier stacks needed depends on the substrate material used and the level of permeation resistance needed for the particular

application. One or two barrier stacks should provide sufficient barrier properties for some applications. The most stringent applications may require five or more barrier stacks.

There is a transparent conductor 145, such as an indium tin oxide layer, adjacent to the first barrier stack 120. There can be additional overcoat layers on top of the barrier stack, such as organic or inorganic layers, planarizing layers, transparent conductors, antireflective coatings, or other functional layers, if desired. This allows the barrier assembly to be tailored to the application.

Fig. 2 shows a barrier assembly being used to encapsulate an environmentally sensitive display device. The substrate 205 has an environmentally sensitive display device 210 on it. There is a barrier stack 215 over the environmentally sensitive display device 210 encapsulating it. The barrier stack 215 includes a barrier layer 220 and a polymer layer 225.

The environmentally sensitive display device 210 can be any display device which is environmentally sensitive. Examples of environmentally sensitive display devices include, but are not limited to liquid crystal displays (LCDs), light emitting diodes (LEDs), light emitting polymers (LEPs), electronic signage using electrophoretic inks, electroluminescent devices (EDs), and phosphorescent devices. These display devices can be made using known techniques, such as those described in U.S. Patent Nos. 6,025,899, 5,995,191, 5,994,174, 5,956,112 (LCDs); U.S. Patent Nos. 6,005,692, 5,821,688, 5,747,928 (LEDs); U.S. Patent Nos. 5,969,711, 5,961,804, 4,026,713 (E Ink); U.S. Patent Nos. 6,023,373, 6,023,124, 6,023,125 (LEPs); and U.S. Patent Nos. 6,023,073, 6,040,812, 6,019,654, 6,018,237, 6,014,119, 6,010,796 (EDs), which are incorporated herein by reference.

The method of making the barrier assembly will be described with reference to Figs. 1 and 2. Any initial layers which are desired, such as scratch resistant layers, planarizing layers, electrically conductive layers, etc., can be coated, deposited, or otherwise placed on the substrate. A polymer smoothing layer is preferably included to provide a smooth base for the remaining layers. It can be formed by depositing a layer of polymer, for example, an acrylate-containing polymer, onto the substrate or previous layer. The polymer layer can be deposited in

vacuum or by using atmospheric processes such as spin coating and/or spraying. Preferably, an acrylate-containing monomer, oligomer, or resin is deposited and then polymerized *in situ* to form the polymer layer. As used herein, the term acrylate-containing monomer, oligomer, or resin includes acrylate-containing monomers, oligomers, and resins, methacrylate-containing monomers, oligomers, and resins, and combinations thereof.

The barrier stack is then placed on the substrate. The barrier stack includes at least one barrier layer and at least one polymer layer. The barrier stacks are preferably made by vacuum deposition. The barrier layer can be vacuum deposited onto the polymer smoothing layer, the substrate, or the previous layer. The polymer layer is then deposited on the barrier layer, preferably by flash evaporating acrylate-containing monomers, oligomers, or resins, condensing on the barrier layer, and polymerizing *in situ* in a vacuum chamber. U.S. Patent Nos. 5,440,446 and 5,725,909, which are incorporated herein by reference, describe methods of depositing thin film, barrier stacks.

Vacuum deposition includes flash evaporation of acrylate-containing monomer, oligomer, or resin with *in situ* polymerization under vacuum, plasma deposition and polymerization of acrylate-containing monomer, oligomer, or resin, as well as vacuum deposition of the barrier layers by sputtering, chemical vapor deposition, plasma enhanced chemical vapor deposition, evaporation, sublimation, electron cyclotron resonance-plasma enhanced vapor deposition (ECR-PECVD), and combinations thereof.

In order to protect the integrity of the barrier layer, the formation of defects and/or microcracks in the deposited layer subsequent to deposition and prior to downstream processing should be avoided. The barrier assembly is preferably manufactured so that the barrier layers are not directly contacted by any equipment, such as rollers in a web coating system, to avoid defects that may be caused by abrasion over a roll or roller. This can be accomplished by designing the deposition system such that the barrier layers are always covered by polymer layers prior to contacting or touching any handling equipment.

When the barrier stack is being used to encapsulate an environmentally sensitive display device, the substrate can be prepared as described above, and the environmentally sensitive display device placed on the substrate. Alternatively, the environmentally sensitive display device can be placed directly on a substrate (or on a substrate with functional layers, such as planarizing layers, scratch resistant layers, etc.).

The environmentally sensitive display device can be placed on the substrate by deposition, such as vacuum deposition. Alternatively it can be placed on the substrate by lamination. The lamination can use an adhesive, glue, or the like, or heat to seal the environmentally sensitive display device to the substrate.

A barrier stack is then placed over the environmentally sensitive display device to encapsulate it. The second barrier stack can be placed over the environmentally sensitive display device by deposition or lamination.

The barrier layers in the first and second barrier stacks may be any barrier material. The barrier layers in the first and second barrier stacks can be made of the same material or a different material. In addition, multiple barrier layers of the same or different barrier materials can be used in a barrier stack.

The barrier layers can be transparent or opaque, depending on the design of the packaging, and application for which it is to be used. Preferred transparent barrier materials include, but are not limited to, metal oxides, metal nitrides, metal carbides, metal oxynitrides, metal oxyborides, and combinations thereof. The metal oxides are preferably selected from silicon oxide, aluminum oxide, titanium oxide, indium oxide, tin oxide, indium tin oxide, tantalum oxide, zirconium oxide, niobium oxide, and combinations thereof. The metal nitrides are preferably selected from aluminum nitride, silicon nitride, boron nitride, and combinations thereof. The metal oxynitrides are preferably selected from aluminum oxynitride, silicon oxynitride, boron oxynitride, and combinations thereof.

Opaque barrier layers can be also be used in some barrier stacks. Opaque barrier materials include, but are not limited to, metals, ceramics, polymers, and cermets. Examples of opaque cermets include, but are not limited to, zirconium

nitride, titanium nitride, hafnium nitride, tantalum nitride, niobium nitride, tungsten disilicide, titanium diboride, and zirconium diboride.

The polymer layers of the first and second barrier stacks are preferably acrylate-containing monomers, oligomers, or resins. The polymer layers in the first and second barrier stacks can be the same or different. In addition, the polymer layers within each barrier stack can be the same or different.

In a preferred embodiment, the barrier stack includes a polymer layer and two barrier layers. The two barrier layers can be made from the same barrier material or from different barrier materials. The thickness of each barrier layer in this embodiment is about one half the thickness of the single barrier layer, or about 50 to 200 Å. There are no limitations on the thickness, however.

When the barrier layers are made of the same material, they can be deposited either by sequential deposition using two sources or by the same source using two passes. If two deposition sources are used, deposition conditions can be different for each source, leading to differences in microstructure and defect dimensions. Any type of deposition source can be used. Different types of deposition processes, such as magnetron sputtering and electron beam evaporation, can be used to deposit the two barrier layers.

The microstructures of the two barrier layers are mismatched as a result of the differing deposition sources/parameters. The barrier layers can even have different crystal structure. For example, Al_2O_3 can exist in different phases (alpha, gamma) with different crystal orientations. The mismatched microstructure can help decouple defects in the adjacent barrier layers, enhancing the tortuous path for gases and water vapor permeation.

When the barrier layers are made of different materials, two deposition sources are needed. This can be accomplished by a variety of techniques. For example, if the materials are deposited by sputtering, sputtering targets of different compositions could be used to obtain thin films of different compositions. Alternatively, two sputtering targets of the same composition could be used but with different reactive gases. Two different types of deposition sources could also be

used. In this arrangement, the lattices of the two layers are even more mismatched by the different microstructures and lattice parameters of the two materials.

A single pass, roll-to-roll, vacuum deposition of a three layer combination on a PET substrate, i.e., PET substrate/polymer layer/barrier layer/polymer layer, can be more than five orders of magnitude less permeable to oxygen and water vapor than a single oxide layer on PET alone. See J.D.Affinito, M.E.Gross, C.A.Coronado, G.L.Graff, E.N.Greenwell, and P.M.Martin, Polymer-Oxide Transparent Barrier Layers Produced Using PML Process, 39th Annual Technical Conference Proceedings of the Society of Vacuum Coaters, Vacuum Web Coating Session, 1996, pages 392-397; J.D.Affinito, S.Eufinger, M.E.Gross, G.L.Graff, and P.M.Martin, PML/Oxide/PML Barrier Layer Performance Differences Arising From Use of UV or Electron Beam Polymerization of the PML Layers, Thin Solid Films, Vol.308, 1997, pages 19-25. This is in spite of the fact that the effect on the permeation rate of the polymer multilayers (PML) layers alone, without the barrier layer (oxide, metal, nitride, oxynitride) layer, is barely measurable. It is believed that the improvement in barrier properties is due to two factors. First, permeation rates in the roll-to-roll coated oxide-only layers were found to be conductance limited by defects in the oxide layer that arose during deposition and when the coated substrate was wound up over system idlers/rollers. Asperities (high points) in the underlying substrate are replicated in the deposited inorganic barrier layer. These features are subject to mechanical damage during web handling/take-up, and can lead to the formation of defects in the deposited film. These defects seriously limit the ultimate barrier performance of the films. In the single pass, polymer/barrier/polymer process, the first acrylic layer planarizes the substrate and provides an ideal surface for subsequent deposition of the inorganic barrier thin film. The second polymer layer provides a robust "protective" film that minimizes damage to the barrier layer and also planarizes the structure for subsequent barrier layer (or environmentally sensitive display device) deposition. The intermediate polymer layers also decouple defects that exist in adjacent inorganic barrier layers, thus creating a tortuous path for gas diffusion.

The permeability of the barrier stacks used in the present invention is shown in Table 1. The barrier stacks of the present invention on polymeric substrates, such as PET, have measured oxygen transmission rate (OTR) and water vapor transmission rate (WVTR) values well below the detection limits of current industrial instrumentation used for permeation measurements (Mocon OxTran 2/20L and Permatran). Table 1 shows the OTR and WVTR values (measured according to ASTM F 1927-98 and ASTM F 1249-90, respectively) measured at Mocon (Minneapolis, MN) for several barrier stacks on 7 mil PET, along with reported values for other materials.

Table 1

Sample	Oxygen Permeation Rate ($cc/m^2/day$)		Water Vapor Permeation ($g/m^2/day$)+	
	23°C	38°C	23°C	38°C
Native 7 mil PET	7.62	-	-	-
1-barrier stack	<0.005	<0.005*	-	0.46+
1-barrier stack with ITO	<0.005	<0.005*	-	0.011+
2-barrier stacks	<0.005	<0.005*	-	<0.005+
2-barrier stacks with ITO	<0.005	<0.005*	-	<0.005+
5-barrier stacks	<0.005	<0.005*	-	<0.005+
5-barrier stacks with ITO	<0.005	<0.005*	-	<0.005+
DuPont film[1] (PET/Si_3N_4 or PEN/Si_3N_4)	0.3	-	-	-
Polaroid[3]	<1.0	-	-	-
PET/Al[2]	0.6	-	0.17	-
PET/silicon oxide[2]	0.7 – 1.5	-	0.15 – 0.9	-
Teijin LCD film (HA grade - TN/STN)[3]	<2	-	<5	-

(*) 38°C, 90% RH, 100% O_2
(+) 38°C, 100% RH
1 - P. F. Carcia, 46th International Symposium of the American Vacuum Society, Oct. 1999
2 - Langowski, H.C., 39th Annual Technical Conference Proceedings, SVC, pp. 398-401 (1996)
3 - Technical Data Sheet

As the data in Table 1 shows, the barrier stacks of the present invention provide oxygen and water vapor permeation rates several orders of magnitude better than PET coated with aluminum, silicon oxide, or aluminum oxide. Typical oxygen permeation rates for other barrier coatings range from about 1 to about 0.1

cc/m^2/day. The oxygen transmission rate for the barrier stacks of the present invention is less than 0.005 cc/m^2/day at 23°C and 0% relative humidity, and at 38°C and 90% relative humidity. The water vapor transmission rate is less than 0.005 g/m^2/day at 38°C and 100% relative humidity. The actual transmission rates are lower, but cannot be measured with existing equipment.

The barrier assemblies were also tested by encapsulating organic light emitting devices using the barrier stacks of the present invention. The organic light emitting devices are extremely sensitive to water vapor, and they are completely destroyed in the presence of micromole quantities of water vapor. Experimentation and calculations suggest that the water vapor transmission rate through the encapsulation film must be on the order of about 10^{-6} to 10^{-5} g/m^2/day to provide sufficient barrier protection for acceptable device lifetimes. The experiments/calculations are based on the detrimental hydrolysis reaction of water vapor with the extremely thin (less than 10 nm), low work function, cathode materials (Ca, Mg, Li, LiF). Hydrolysis of the cathode leads to the formation of non-conductive reaction products (such as hydroxides and oxides) that delaminate or blister away from the electron transport layers of the organic light emitting devices, resulting in the formation of dark spots on the device.

The organic light emitting devices encapsulated in the barrier stacks of the present invention have been in operation for over six months without measurable degradation. The extrapolated lifetime for the encapsulated devices exceeds the required 10,000 hours necessary to satisfy industry standards. The barrier stacks are extremely effective in preventing oxygen and water penetration to the underlying components, substantially outperforming other thin-film barrier coatings on the market.

The preferred deposition process is compatible with a wide variety of substrates. Because the preferred process involves flash evaporation of a monomer and magnetron sputtering, deposition temperatures are well below 100°C, and stresses in the coating can be minimized. Multilayer coatings can be deposited at high deposition rates. No harsh gases or chemicals are used, and the process can be scaled up to large substrates and wide webs. The barrier properties of the coating can be tailored to the application by controlling the number of layers, the

materials, and the layer design. Thus, the present invention provides a barrier stack with the exceptional barrier properties necessary for hermetic sealing of an environmentally sensitive display device, or other environmentally sensitive device. It permits the production of an encapsulated environmentally sensitive display device.

While certain representative embodiments and details have been shown for purposes of illustrating the invention, it will be apparent to those skilled in the art that various changes in the compositions and methods disclosed herein may be made without departing from the scope of the invention, which is defined in the appended claims.

CLAIMS

1. A barrier assembly comprising:

at least one barrier stack comprising at least one barrier layer and at least one polymer layer, wherein the at least one barrier stack has an oxygen transmission rate of less than 0.005 cc/m^2/day at 23°C and 0% relative humidity

2. The barrier assembly of claim 1 wherein the at least one barrier stack has an oxygen transmission rate of less than 0.005 cc/m^2/day at 38°C and 90% relative humidity.

3. The barrier assembly of claim 1 wherein the at least one barrier stack has a water vapor transmission rate of less than 0.005 g/m^2/day at 38°C and 100% relative humidity.

4. The barrier assembly of claim 1 further comprising a substrate adjacent to the at least one barrier stack.

5. The barrier assembly of claim 1 wherein the at least one barrier layer is substantially transparent.

6. The barrier assembly of claim 1 wherein at least one of the at least one arrier layer comprises a material selected from metal oxides, metal nitrides, metal carbides, metal oxynitrides, metal oxyborides, and combinations thereof.

7. The barrier assembly of claim 6 wherein the metal oxides are selected from silicon oxide, aluminum oxide, titanium oxide, indium oxide, tin oxide, indium tin oxide, tantalum oxide, zirconium oxide, niobium oxide, and combinations thereof.

8. The barrier assembly of claim 6 wherein the metal nitrides are selected from aluminum nitride, silicon nitride, boron nitride, and combinations thereof.

9. The barrier assembly of claim 6 wherein the metal oxynitrides are selected from aluminum oxynitride, silicon oxynitride, boron oxynitride, and combinations thereof.

10. The barrier assembly of claim 1 wherein the at least one first barrier layer is substantially opaque.

11. The barrier assembly of claim 1 wherein at least one of the at least one first barrier layers is selected from opaque metals, opaque polymers, opaque ceramics, and opaque cermets.

12. The barrier assembly of claim 4 wherein the substrate comprises a flexible substrate material.

13. The barrier assembly of claim 12 wherein the flexible substrate material is selected from polymers, metals, paper, fabric, and combinations thereof.

14. The barrier assembly of claim 4 wherein the substrate comprises a rigid substrate material.

15. The barrier assembly of claim 14 wherein the rigid substrate material is selected from ceramics, metals, and semiconductors.

16. The barrier assembly of claim 1 wherein at least one of the at least one polymer layers comprises an acrylate-containing polymer.

17. The barrier assembly of claim 4 further comprising a polymer smoothing layer adjacent to the substrate.

18. The barrier assembly of claim 4 further comprising a scratch resistant layer adjacent to the substrate.

19. The barrier assembly of claim 1 further comprising an anti-reflective coating adjacent to the substrate.

20. The barrier assembly of claim 1 further comprising an anti-fingerprint coating adjacent to the substrate.

21. The barrier assembly of claim 1 further comprising an anti-static coating adjacent to the substrate.

22. The barrier assembly of claim 1 wherein the at least one barrier layer comprises two barrier layers.

23. The barrier assembly of claim 22 wherein the two barrier layers are made of the same barrier material.

24. The barrier assembly of claim 22 wherein the two barrier layers are made of different barrier materials.

25. A method of making a barrier assembly comprising:
providing a substrate; and
placing at least one first barrier stack comprising at least one first barrier layer and at least one first polymer layer on the substrate, wherein the at least one barrier stack has an oxygen transmission rate of less than 0.005 cc/m^2/day at 23°C and 0% relative humidity.

26. The method of claim 25 wherein the at least one barrier stack has an oxygen transmission rate of less than 0.005 cc/m^2/day at 38°C and 90% relative humidity.

27. The method of claim 25 wherein the at least one barrier stack has an water vapor transmission rate of less than 0.005 g/m^2/day at 38°C and 100% relative humidity.

28. The method of claim 25 wherein the step of placing the at least one barrier stack on the substrate comprises depositing the at least one barrier stack on the substrate.

29. The method of claim 28 wherein the at least one barrier stack is vacuum deposited.

30. The method of claim 28 wherein the at least one barrier layer is vacuum deposited and the at least one polymer layer is deposited.

31. The method of claim 28 wherein the step of placing the at least one barrier stack on the substrate comprises laminating the at least one barrier stack on the substrate.

32. The method of claim 31 wherein the at least one barrier stack is laminated using an adhesive.

33. The method of claim 31 wherein the at least one barrier stack is laminated using heat.

34. The method of claim 31 wherein the at least one barrier stack is laminated using solder.

35. The method of claim 31 wherein the at least one barrier stack is laminated using ultrasonic welding.

36. The method of claim 31 wherein the at least one barrier stack is laminated using pressure.

37. The method of claim 25 further comprising depositing a polymer smoothing layer on the substrate before the at least one barrier stack is placed thereon.

38. The method of claim 25 further comprising depositing a scratch resistant layer on the substrate before the at least on barrier stack is placed thereon.

39. The method of claim 25 further comprising depositing an anti-reflective coating on the substrate before the at least one barrier stack is placed thereon.

40. The method of claim 25 further comprising depositing an anti-fingerprint coating on the substrate before the at least one barrier stack is placed thereon.

41. The method of claim 25 further comprising depositing an anti-static coating on the substrate before the at least one barrier stack is placed thereon.

42. The method of claim 25 wherein the at least one barrier layer comprises two barrier layers.

43. The method of claim 42 wherein the two barrier layers are deposited using the same deposition source.

44. The method of claim 42 wherein the two barrier layers are deposited using different deposition sources.

45. The method of claim 42 wherein the two barriers layers are vacuum deposited.

46. The method of claim 42 wherein the two barrier layers are made of the same barrier material.

47. The method of claim 42 wherein the two barrier layers are made of different barrier materials.

FIG. 1

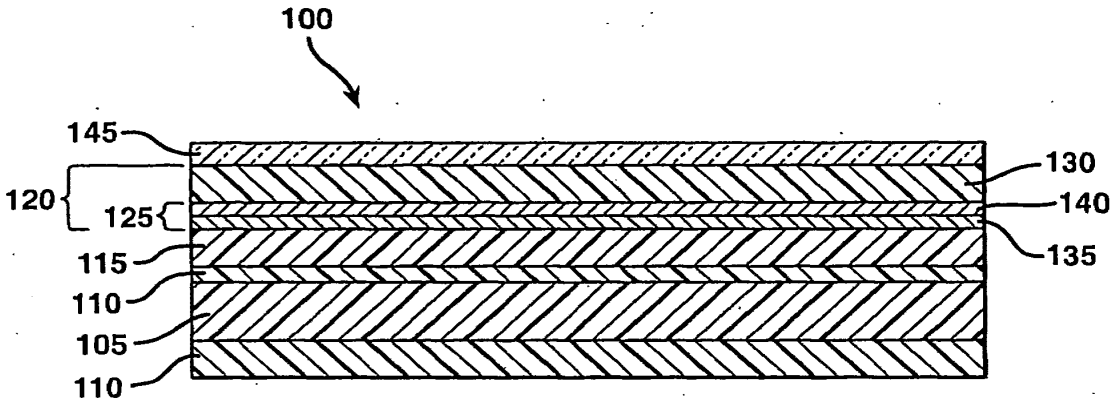
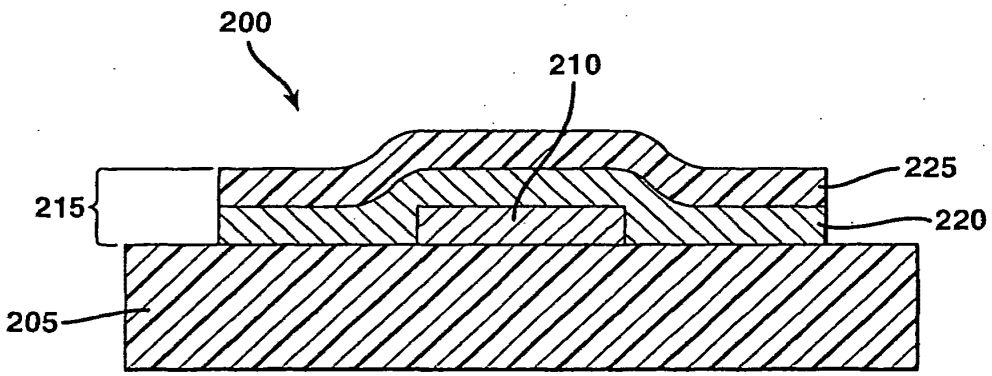

100
145
120
125
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FIG. 2


200
210
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205
225
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INTERNATIONAL SEARCH REPORT

Inte[illegible] al Application No
PC[illegible] 01/06596

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 C23C14/08 B05D7/24 B65D65/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 B05D C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data, IBM-TDB, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	AFFINITO J D ET AL: "A new method for fabricating transparent barrier layers" 23RD INTERNATIONAL CONFERENCE ON METALLURGICAL COATINGS AND THIN FILMS, SAN DIEGO, CA, USA, 22-26 APRIL 1996, vol. 290-291, pages 63-67, XP004173291 Thin Solid Films, 15 Dec. 1996, Elsevier, Switzerland ISSN: 0040-6090	1-7, 12-14, 25-30, 37-41
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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'A' document defining the general state of the art which is not considered to be of particular relevance

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'P' document published prior to the international filing date but later than the priority date claimed

'T' later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

'X' document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

'Y' document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

'&' document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 August 2001	05/09/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Ekhult, H

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SDC EX. 1002 - 498/544

INTERNATIONAL SEARCH REPORT

Inte al Application No
PC1/US 01/06596

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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(54) **METHOD OF MAKING ACTIVE SUBSTRATES FOR COLOR LIQUID CRYSTAL DISPLAYS**

VERFAHREN ZUR HERSTELLUNG VON AKTIVEN SUBSTRATEN FÜR FARBFLÜSSIGKRISTALLANZEIGEN

PROCEDE DE FABRICATION DE SUBSTRATS ACTIFS POUR ECRAN COULEUR A CRISTAUX LIQUIDES

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Description

[0001] The present invention pertains to improved color electronic displays, to active substrates for use in electronic displays, and to methods of making active elements that have color filters for use in electronic displays.

[0002] Difficulties can arise in the fabrication of full color active matrix liquid crystal displays (LCD), especially as demand increases for displays to become larger, brighter, thinner, and lighter, with higher resolution and faster switching times, all at a lower cost.

[0003] Active matrix LCDs commonly include a liquid crystal material disposed between an active substrate and a non-active (passive) substrate. The active substrate generally has a regular array, or matrix, of thin film transistors (TFT) arranged in pixels. To add color, color filters can be provided for each of the pixels in an LCD. Currently, color filters in active matrix displays are typically formed onto the flat, non-active display substrates, using either photolithography or direct printing techniques.

[0004] Methods of making active substrates with color filters are known from EP-A-0 556 809, EP-A-0 702 250, and EP-A-0 759 564.

[0005] Increasing the size and/or the resolution of electronic displays also increases the number of pixels to control in the display. With more pixels to control, issues regarding electronic switching speed, liquid crystal response times, and color filter alignment can become more important. For example, when assembling color LCDs, improperly aligned or otherwise defective color filters can necessitate discarding the color filter substrate during processing. The associated cost of waste, as well as the probability for error, tends to increase as the number of pixels in the display increases. In addition, there is an ever-growing desire for these displays to have thinner and lighter weight constructions, to use less power while providing enhanced brightness, and to have improved reliability and durability.

[0006] The present invention provides improved liquid crystal display constructions that have components selected to enhance overall display performance. Components can be selected to construct improved displays according to the present invention that have, for example, enhanced brightness, lower power consumption, and/or faster switching rates. The present invention also includes improved displays that can be made thinner and lighter while maintaining reliability and durability.

[0007] According to the present invention, the following components can be selected to achieve enhanced display performance. Color filters can be provided on the active substrate of an active matrix display, for example, to increase the aperture ratio of the display, resulting in more light through the display. Liquid crystal materials and alignment layers can be selected to increase response times, reduce power consumption, and increase contrast. Spacers can be provided that allow for thinner constructions that are durable. Reflective polarizers can be used that increase lighting efficiency by increasing brightness for the same lighting conditions. These and other components can be selected individually or in combination, for example to synergistically enhance one or more display performance properties.

[0008] In accordance with the present invention there is provided a method of making an electronic display as recited in claims 1 and 6, and a process of making a color display substrate as recited in claims 11 and 18.

[0009] The liquid crystal layer of the displays can comprise a fluorinated chiral ferroelectric liquid crystal material.

[0010] FIG. 1 is a schematic cross-section of a liquid crystal display 200.

[0011] FIG. 2(a) is a schematic plan view of an active substrate element 300 for electronic displays.

[0012] FIG. 2(b) is a schematic cross-sectional view of a liquid crystal display panel 310 that includes an embodiment of active substrate element 300 viewed along line 2b from FIG. 2(a).

[0013] FIG. 3 is a schematic flow chart of steps in a method of the present invention.

[0014] The present invention pertains to improved active matrix color displays and to a method of making color display substrates. The improved displays include components selected to enhance the performance of active matrix displays. The improved displays can also include color filter substrates made according to a method of the present invention. The method includes thermally transferring multiple color filters to a display substrate and crosslinking the color filters after transfer.

[0015] Liquid crystal light modulators are commonly used in electronic displays where pixilated information is to be visually displayed to a user or an observer. Other uses for liquid crystal light modulators include data transmission devices where information is transmitted as light which can be controlled by a liquid crystal light modulator. In the case of data transmission, light can be "displayed" from one device to another device, and is not necessarily displayed directly to a user or observer. As used herein, therefore, the terms "liquid crystal display", "electronic display", and "liquid crystal light modulator" are meant to encompass electronic devices that modulate light transmission for display, whether that display is to a passive observer, an active user, an active or passive device, photographic film, a projection screen, and the like.

[0016] FIG. 1 schematically shows components that can be included in an improved display 200 according to the present invention. In various embodiments, these and other components (as described in more detail below) can be selected (individually or in combination) to improve display performance characteristics, including enhanced brightness, lower power consumption, faster switching times, and thinner overall construction. In brief, selectable components of

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display 200 can include bottom polarizer 210, bottom substrate 212, active layer 214, color filter layer 216, bottom alignment layer 218, liquid crystal layer 220, top alignment layer 222, sustain electrode layer 224, top substrate 226, and top polarizer 228. As used throughout this document, the term "active layer" refers to a layer in an electronic display construction that includes one or more active devices, and "active substrate" refers to a substrate that has an active layer. Examples of active devices include transistors, counters, gates, and other such devices, whereas examples of passive devices include capacitors, resistors, and other such devices. These and other layers and components includeable in a display according to the present invention are described in more detail in discussions that follow.

[0017] FIG. 1 also shows internal light source 202 that can be provided to illuminate display 200. While display 200 is shown to be a transmissive display, it is recognized that the various aspects of the present invention also apply to transflective and reflective displays that may be illuminated from the front using ambient light or an internal light source and front light guide.

[0018] Display 200 can optionally include various optical components and/or light management films positioned between light source 202 and polarizer 210, as indicated by region 240 in FIG. 1. The components can be provided alone or in combination to improve the overall performance of the display. Examples of suitable components include: a sheet of BRIGHTNESS ENHANCEMENT FILM (BEF) (commercially available from Minnesota Mining and Manufacturing Company, St. Paul, MN) used in a prisms up configuration, a prisms down configuration, and/or in combination with another sheet of BEF (e.g., two sheets oriented in a crossed prisms configuration); a sheet of a light management film sold under the trade designation DBEF (commercially available from Minnesota Mining and Manufacturing Company); a turning film or other light direction changing film; a cholesteric reflective polarizer (such as those commercially available from Nitto Denko under the trade designation NIPPOX); diffuse reflective polarizing films such as those described in U.S. Pat. No. 5,783,120 and International Publication WO 97/32223; retarder films; lenses and lens arrays; and other such films and optical components.

[0019] One embodiment of an improved display of the present invention is a color filter active substrate element 300 as shown in FIG. 2(a) that can be used, for example, in an active matrix LCD construction 310 as shown in FIG 2(b). The particular embodiments are meant to be illustrative and not to limit the scope of the invention. The various components shown in FIGs. 2(a) and (b), and the selection of such components for improved overall display performance, are described in more detail below after a brief identification of various components shown.

[0020] FIG. 2(a) shows a plan view of a portion of an active substrate element 300 for an electronic display panel. Substrate element 300 can be integrated, using proper components, into transmissive, transflective, or reflective electronic displays that can range in size from microdisplays (on the order of 1 cm or less), to small displays (about 1 to several cm), to large displays (tens or several tens of cm), and to very large displays (on the order of 1 m or more). Substrate element 300 has a plurality of independently addressable devices 20, such as thin film transistors (TFTs), arranged in a regular pattern. The transistors form an active layer along with address lines and other (optional) active or passive devices that may be provided, including additional transistors, capacitors, resistors, organic or inorganic light emitting devices, and other such devices. The TFTs 20 are commonly provided in a rectangular array as shown in FIG. 2(a), although they can be arranged in any suitable manner. Transparent sub-pixel electrodes 12 can be associated with the transistors 20 to allow independent application of an electric field in each sub-pixel area to re-orient liquid crystal material in selected sub-pixels of the display. Color filters R, G, and B can be provided on the active substrate element 300 using the method of the present invention, as described in more detail below.

[0021] An individual transistor 20 can be addressed by supplying a voltage to an associated gate electrode 22 from one of a series of parallel gate driver electrodes 32 so that a signal supplied from one of a series of parallel signal driver electrodes 34 can pass from the source 24 of the transistor 20 to the drain 26 of the transistor 20. Drain 26 can be electrically connected to an associated transparent sub-pixel electrode 12. If any layers separate transparent sub-pixel electrode 12 and drain 26, the electrical connection can optionally be made via a through hole 28 in the intervening layer or layers. By so addressing a transistor, an electric field can be created in an area between the transistor's associated transparent sub-pixel electrode and an electrode supplied on an opposing substrate. The area associated with each transparent sub-pixel electrode defines a sub-pixel in the display. To add color, a color filter can be provided for each sub-pixel. In a full color display, a full pixel is made up of three adjacent sub-pixels, each having a different color filter, typically red, blue, and green (although other color combinations can be used, such as cyan, magenta, and yellow).

[0022] FIG. 2(b) shows a portion of a liquid crystal display panel 310 that includes an embodiment of the active substrate element 300 shown in FIG. 2(a). Display panel 310 is shown in cross-section taken along line 2b from FIG. 2(a). The electronic display panel 310 includes bottom (active) substrate 10a, top (non-active) substrate 10b, and a variety of components sandwiched between the substrates. Bottom substrate 10a includes a series of independently addressable TFT devices 20 that are addressable via signal driver electrodes 34 electrically connected to source electrodes 24 and gate driver electrodes (not shown) electrically connected to gate electrodes 22. Using high conductivity driver electrodes with TFTs can allow for faster switching times. Color filters R, G, and B, can be disposed on the TFTs. To prevent ambient light from undesirably inducing activation of the TFTs, an optional black matrix material 50

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can also be deposited on top of the TFTs, using methods described in more detail below. Black matrix 50 can also be deposited on the active substrate to delineate sub-pixels and provide for higher contrast. Planarization layer 16 can optionally be provided to give a uniform surface on which to apply transparent sub-pixel electrodes 12.

[0023] Through holes 28 can be provided in the planarization layer 16 and color filters R, G, and B, to allow electrical connection between TFT drain electrodes 26 and transparent conductive electrodes 12 as shown in FIG. 2(b). Alignment layer 18a can be provided over the transparent conductive electrodes to orient the liquid crystal material used in the display. Top substrate 10b can also be provided with an alignment layer 18b, which can be similar or dissimilar to alignment layer 18a, depending on the desired liquid crystal alignment. Spacers 42 can be provided to maintain a uniform gap between the top and bottom substrates, and a liquid crystal material 40 can be disposed in the gap between the substrates. Depending on how spacers 42 are provided, an amount of residual binder material 44 can be associated with the spacers. As described below, spacers can be selectively deposited to form a black matrix, for example, positioned directly above the TFTs to protect the transistors from undesired light-induced activation.

[0024] Top substrate 10b has a transparent electrode 12', commonly called a sustain electrode. Electrode 12' serves as a counter electrode to the sub-pixel electrodes 12. For example, sustain electrode 12' can be held at a constant potential so that applying an appropriate voltage to a selected sub-pixel electrode or electrodes creates an electric field in the selected sub-pixel area(s) to orient a liquid crystal material for transmission of light having a desired polarization state. Sustain electrode 12' can be patterned or provided as a single continuous layer.

[0025] The discussion that follows describes in further detail various components of improved displays of the present invention as introduced above and as shown in FIGs. 1, and 2(a) and (b).

[0026] In one embodiment, the performance of a display of the present invention can be improved by forming color filters on the active substrate of an active matrix display. Referring to FIG. 1, color filter layer 216 can be provided on the active layer 214 using methods in accordance with the present invention, as described in detail below. Color filters can be deposited as separate filters for each sub-pixel, or in parallel strips that span multiple sub-pixels, for example, as indicated by color filters R, G, and B in FIGs. 2(a). In either case, the color filters can be arranged so that adjacent filters include different colorants. A typical arrangement has a repeating pattern of red, green, and blue color filters, or other suitable combination of color filters (e.g., other primary colorants such as magenta, cyan, and yellow, or other color combinations that may or may not provide a display that has full color capabilities). Other repeating patterns also exist, and the particular pattern used typically depends on the arrangement of active devices and sub-pixel electrodes on the active substrate.

[0027] When color filters that contain transparent primary colorants are suitably arranged, proper activation of adjacent sub-pixels allows mixing of colors for a ful color display. Color mixing can also include the introduction of gray scale. Gray scale can be introduced by spatial or temporal dithering of the electronic signal controlling the sub-pixel electrodes (as is well known in the art), or by providing a liquid crystal material that provides continuous gray scale as a function of applied field (e.g. for twisted nematic and super twisted nematic liquid crystal materials as well as for certain ferroelectric liquid crystals such as those discussed in U.S. Pat. No. 5,062,691). The combination of primary color mixing and the introduction of gray scale gives the ability to achieve a full color electronic display.

[0028] The performance of displays of the present invention can be enhanced by providing color filters on the active layer, for example, to increase the aperture ratio of the display relative to other displays that have color filters disposed on the opposing, passive substrate. Increasing the aperture ratio increases the brightness of the display. When color filters are provided in an active matrix display on the passive substrate, precise alignment can be difficult to achieve between (1) the pattern of color filters and the black matrix on the passive substrate and (2) the pattern of active devices, sub-pixel electrodes, and optional black matrix on the active substrate. To compensate for the difficulties that arise in precision alignment, the black matrix lines on the passive color filter substrate are commonly widened to ensure a certain amount of overlap between the patterns on each substrate. The patterns are overlapped to help prevent cross over of light from one sub-pixel to an adjacent sub-pixel, which can cause discoloration in the display. However, widening of the black matrix also tends to reduce the aperture ratio of the display and, in turn, reduces the amount of light transmitted through the display. By way of the present invention, the color filter layer can be provided on the active layer rather than on the passive substrate. This construction can be used to eliminate the color filter and the (widened) black matrix from the passive substrate, and thereby increase the aperture ratio and brightness of the display. By providing color filters on the active substrate, the aperture ratio of the display can be increased by 10% to 30% or more relative to constructions that have color filters and black matrix on the passive substrate.

[0029] Color filters can be provided on the active substrate between the substrate and the active layer, within the active layer, or between the active layer and the liquid crystal layer. The color filters can be provided on active substrates using any suitable method now known or later developed. Suitable methods can include conventional photolithography, thermal head or ink jet printing, colorant sublimation, and selective thermal mass transfer. Preferably, the color filters are formed by selective thermal transfer of a colorant. An exemplary method of selective thermal transfer of a colorant is laser induced thermal mass transfer of a colorant from a donor sheet to a display substrate, as described in detail below.

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[0030] Thermal mass transfer occurs, for example, when portions of a donor element transfer layer are thermally transferred to a receptor so that the transferred portions remain substantially intact, that is the material within the transferred portions remains in substantially the same physical arrangement as prior to transfer. For example, thermal mass transfer includes thermal melt stick type transfers where the heat generated in the donor element is sufficient to cause portions of the transfer layer to detach at the interface between the transfer layer and the donor element support so that the detached portions of the transfer layer can be transferred as "plugs" onto a receptor. Thermal mass transfer may be a preferred transfer method as compared to other methods identified above, for example, due to high placement accuracies (i.e., when a laser is used to induce the thermal mass transfer), applicability to large and small displays as well as to high and low resolution displays, and compatibility with systems that use thermal mass transfer to provide other components (e.g., black matrix or spacers, as discussed below).

[0031] FIG. 3 indicates steps for transferring multiple color filters to display substrates according to the present invention. A first color filter material can be selectively transferred to portions of a display substrate by thermal transferring a color filter material to the selected portions of the substrate. A second color filter material can similarly be selectively transferred to portions of the substrate. This procedure can optionally be repeated for a third (or more) color filter material.

[0032] After selectively transferring two or more color filter materials, the color filters disposed on the active substrate can optionally be inspected for defects, alignment, and so forth. After an optional inspection, the color filters can be crosslinked, for example, by radiation curing, thermal curing, or exposure to chemical curatives. Crosslinking hardens the color filter material on the substrate, thereby making the color filters more chemically, physically, and/or thermally stable, and thus less susceptible to damage that can be caused by later processing or operation. However, crosslinking can also make removal of the color filter material more difficult. Therefore, prior to crosslinking and after an optional inspection, the present invention includes an alternative step of removing the color filters prior to crosslinking for reworking of the active substrate, as indicated in FIG. 3. The ability to successfully deposit multiple color filters before crosslinking or setting any one color filter provides the advantage that multiple color filters can be inspected at the same time, removed at the same time (if removal is necessary), and crosslinked at the same time.

[0033] Exemplary processes for selective thermal transferring of color filter materials include thermal mass transfer, ink jet printing, and colorant sublimation. Thermal mass transfer techniques include the imagewise transfer of color filter material from a donor sheet by selectively exposing the donor sheet to imaging radiation (e.g., from a laser or a flash lamp), and selective direct heating of portions of the donor sheet, for example by using a thermal print head or by direct resistance heating of a layer contacting or disposed in the donor element. Colorant sublimation techniques include selective dye sublimation from areas of a donor sheet. Ink jet techniques include forming a directed flow of a dye or pigment through an aperture or nozzle using heat or otherwise.

[0034] Methods for an imagewise thermal mass transfer of color filter materials are discussed, for example, in U.S. Pat. Nos. 5,521,035 (Wolk) and 5,725,989 (Chang). Briefly, these processes involve thermally transferring material from selected areas of a color donor element sheet. Suitable donor elements are described in detail below. Heat can be generated using imaging radiation from a laser, flash lamp, or other suitable source to irradiate selected portions of a light-to-heat converter (LTHC) material in the donor element. The LTHC can be present as a separate layer in the donor media and/or included in other layers of the donor media, including in a color filter transfer layer.

[0035] During imaging, the color transfer layer of the donor element can be brought into intimate contact with a receptor (e.g., an active display substrate that has a plurality of devices, a passive display substrate that has one or more addressable electrodes, or other suitable display substrates). Pressure or vacuum can optionally be used to secure the donor element to the display substrate receptor. The radiation source can be used to heat the LTHC in an imagewise fashion (e.g., digitally, analog exposure through a mask, etc.) to cause imagewise transfer of portions of a color thermal transfer layer from the donor to the receptor. A variety of light-emitting sources can be utilized. Infrared, visible, and ultraviolet lasers are particularly useful when using digital imaging techniques. When analog techniques are used (e.g., exposure through a mask) high powered light sources (e.g., xenon flash lamps, etc.) are also useful.

[0036] During imaging, it may be desirable to minimize formation of interference patterns due to multiple reflections from the imaged material. This can be accomplished by various methods. A common method is to effectively roughen the surface of the donor element on the scale of the incident radiation as described in U.S. Pat. No. 5,089,372. This has the effect of disrupting the spatial coherence of the incident radiation, thus minimizing self interference. An alternate method is to employ an antireflection coating within the donor element. The general use of anti-reflection coatings is known, and may consist of quarter-wave thicknesses of a coating such as magnesium fluoride, as described in U.S. Pat No.5,171,650.

[0037] Large donor elements can be used, including donor elements that have length and width dimensions of a meter or more. In operation, a laser can be rastered or otherwise moved across the donor element, the laser being selectively operated to illuminate portions of the donor element according to a desired pattern. Alternatively, the laser may be stationary and the donor element and/or receptor substrate moved beneath the laser.

[0038] In the present invention, it may be desirable and/or convenient to sequentially use two or more different color

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donor elements to form a plurality of color filters on a display substrate. Alternatively, a single donor element (e.g., one that has multiple different color filter materials patterned to form the color transfer layer) can be used to transfer multiple color filters from the donor element.

[0039] As an alternative to using imaging radiation, a heating element, such as a resistive heating element, may be used to selectively transfer portions of the color transfer layer. The donor element can be selectively contacted with a heating element to cause thermal transfer of a portion of the transfer layer according to a pattern. In another embodiment, the donor element may include a layer that can convert an electrical current applied to the layer into heat.

[0040] Ink jet printing can also be useful in selective thermal transfer of color filters to active display substrates. Methods for ink jet printing of color filters are described in U.S. Pat. Nos. 5,714,195 and 5,716,740. Exemplary color filter materials transferable using ink jet methods include an ink and a crosslinkable binder. The ink can include any suitable colorants such as dyes and pigments (as discussed above), and the ink can be liquid or solid. The binder can be any suitable binder that is ink compatible, examples of which include acrylic resins, epoxy resins, silicone resins, cellulose derivatives such as hydroxypropyl cellulose, hydroxyethyl cellulose, methyl cellulose, and carboxymethyl cellulose, and modified resins thereof. The color filter material can optionally include additives such as cure initiators, dispersing agents, surfactants, and other suitable additives.

[0041] For embodiments in which color filters are selectively thermally mass transferred from a donor element, suitable donor elements that can be used typically include a base substrate layer, a light-to-heat-converter (LTHC), a color transfer layer that includes a colorant dispersed in a crosslinkable composition, an optional interlayer disposed between the base layer and the color transfer layer, and an optional transfer assist layer.

[0042] The donor substrate can be a polymer film. One suitable type of polymer film is a polyester film, for example, polyethylene terephthalate or polyethylene naphthalate films. However, other films with sufficient optical properties (if light is used for heating and transfer), including high transmission of light at a particular wavelength, as well as sufficient mechanical and thermal stability for the particular application, can be used. The donor substrate, in at least some instances, is flat so that uniform coatings can be formed. The donor substrate is also typically selected from materials that remain stable despite heating of the LTHC during thermal transfer. The typical thickness of the donor substrate ranges from 0.025 to 0.15 mm, preferably 0.05 to 0.1 mm, although thicker or thinner donor substrates may be used.

[0043] Typically, the materials used to form the donor substrate and the LTHC layer are selected to improve adhesion between the LTHC layer and the donor substrate. An optional priming layer can be used to increase uniformity during the coating of subsequent layers and also increase the interlayer bonding strength between the LTHC layer and the donor substrate. One example of a suitable substrate with primer layer is available from Teijin Ltd. (Product No. HPE100, Osaka, Japan).

[0044] For radiation-induced thermal transfer, a separate LTHC layer is typically incorporated within the donor element to couple the energy of light radiated from a light-emitting source into the donor element. The LTHC layer preferably includes a radiation absorber that absorbs incident radiation (e.g., laser light) and converts at least a portion of the incident radiation into heat to enable transfer of the transfer layer from the donor element to the receptor. In some embodiments, there is no separate LTHC layer and, instead, the radiation absorber is disposed in another layer of the donor element, such as the donor substrate or the transfer layer. In other embodiments, the donor element includes an LTHC layer and also includes additional radiation absorber(s) disposed in one or more of the other layers of the donor element, such as, for example, the donor substrate or the transfer layer. In yet other embodiments, the donor element does not include an LTHC layer or radiation absorber and the transfer layer is transferred using a heating element that contacts the donor element.

[0045] Typically, the radiation absorber in the LTHC layer (or other layers) absorbs light in the infrared, visible, and/or ultraviolet regions of the electromagnetic spectrum and converts the absorbed radiation into heat. The radiation absorber is typically highly absorptive of the selected imaging radiation, providing a LTHC layer with an optical density at the wavelength of the imaging radiation in the range of about 0.2 to 3, or from about 0.5 to 2.5. (Optical density is the logarithm of the ratio of a) the intensity of light incident on the layer and b) the intensity of light transmitted through the layer.) Thicker coatings generally have higher optical densities, but may, at least in some instances, have less efficient heat transfer. Higher optical density LTHC layers may provide improved surface topography of the transferred layer (i.e., a smoother top surface), but may also result in increased edge roughness of the transferred layer.

[0046] Suitable radiation absorbing materials can include, for example, dyes (e.g., visible dyes, ultraviolet dyes, infrared dyes, fluorescent dyes, and radiation-polarizing dyes), pigments, metals, metal compounds, metal films, and other suitable absorbing materials. Examples of suitable radiation absorbers include carbon black, metal oxides, and metal sulfides. One example of a suitable LTHC layer can include a pigment, such as carbon black, and a binder, such as an organic polymer. The amount of carbon black may range, for example, from 2 to 50 wt.% or 5 to 20 wt.%. High carbon black loadings may improve sensitivity and edge roughness of the transferred layer, but may also degrade the surface topography of the transferred color filter (e.g., due to excessive heating of the transfer layer during imaging). A suitable LTHC layer formulation is given in Table I.

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Table I:

LTHC Coating Formulation	
Component	**Wt.%**
Raven™ 760 Ultra carbon black pigment (available from Columbian Chemicals, Atlanta, GA)	8.0
Butvar™ B-98 (polyvinylbutyral resin, available from Monsanto, St. Louis, MO)	1.4
Joncryl™ 67 (acrylic resin, available from S.C. Johnson & Son, Racine, WI)	4.2
Elvacite™ 2669 (acrylic resin, available from ICI Acrylics, Wilmington, DE)	31.8
Disperbyk™ 161 (dispersing aid, available from Byk Chemie, Wallingford, CT)	0.7
FC-430™ (fluorochemical surfactant, available from 3M, St. Paul, MN)	0.03
Ebecryl™ 629 (epoxy novolac acrylate, available from UCB Radcure, N. Augusta, SC)	47.6
Irgacure™ 369 (photocuring agent, available from Ciba Specialty Chemicals, Tarrytown, NY)	5.3
Irgacure™ 184 (photocuring agent, available from Ciba Specialty Chemicals, Tarrytown, NY)	0.8

[0047] In a particular embodiment, LTHC layers can be used that contain conductive materials dissipate charge built up during the process of coating layers to form the donor element. For example, LTHC layers can be used that contain carbon black in a binder that has ionic functional groups. LTHC layers so formulated that have conductivities of about 10^7 Ω/square or more may provide adequate anti-static properties. An example of such a formulation includes components as shown in Table II.

Table II:

LTHC Coating Formulation			
Material	**Supplier**	**Function**	**Parts by weight**
Ketjen Black EC600JD	Ketjen International	Carbon Black	100.0
Disperbyk 161	BYK Chemie	Dispersant	73.02
UR8300	Toyobo Co.	Binder	500.4
Evecryl EB629	UCB Radcure, Inc.	Binder	542.0
Irgacure 369	Ciba-Geigy	Initiator	40.6
Irgacure 184	Ciba-Geigy	Initiator	6.0

[0048] Another suitable LTHC layer includes metal or metal/metal oxide formed as a thin film, for example, black aluminum (i.e., a partially oxidized aluminum having a black visual appearance). Metallic and metal compound films may be formed by techniques, such as, for example, sputtering and evaporative deposition. Particulate coatings may be formed using a binder and any suitable dry or wet coating techniques.

[0049] Dyes suitable for use as radiation absorbers in a LTHC layer may be present in particulate form, dissolved in a binder material, or at least partially dispersed in a binder material. When dispersed particulate radiation absorbers are used, the particle size can be, at least in some instances, about 10 µm or less, and may be about 1 µm or less. Suitable dyes include those dyes that absorb in the IR region of the spectrum. Examples of such dyes may be found in Matsuoka, M., "Infrared Absorbing Materials", Plenum Press, New York, 1990; Matsuoka, M., *Absorption Spectra of Dyes for Diode Lasers*, Bunshin Publishing Co., Tokyo, 1990, U.S. Patent Nos. 4,722,583; 4,833,124; 4,912,083; 4,942,141; 4,948,776; 4,948,778; 4,950,639; 4,940,640; 4,952,552; 5,023,229; 5,024,990; 5,156,938; 5,286,604; 5,340,699; 5,351,617; 5,360,694; and 5,401,607; European Patent Nos. 321,923 and 568,993; and Beilo, K.A. et al., *J. Chem. Soc., Chem. Commun.*, 1993, 452-454 (1993). IR absorbers marketed by Glendale Protective Technologies, Inc., Lakeland, Fla., under the trade designation CYASORB IR-99, IR-126 and IR-165 may also be used. A specific dye may be chosen based on factors such as, solubility in, and compatibility with, a specific binder and/or coating solvent, as well as the wavelength range of absorption.

[0050] Pigmentary materials may also be used in the LTHC layer as radiation absorbers. Examples of suitable pigments include carbon black and graphite, as well as phthalocyanines, nickel dithiolenes, and other pigments described in U.S. Pat. Nos. 5,166,024 and 5,351,617. Additionally, black azo pigments based on copper or chromium complexes

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of, for example, pyrazolone yellow, dianisidine red, and nickel azo yellow can be useful. Inorganic pigments can also be used, including, for example, oxides and sulfides of metals such as aluminum, bismuth, tin, indium, zinc, titanium, chromium, molybdenum, tungsten, cobalt, iridium, nickel, palladium, platinum, copper, silver, gold, zirconium, iron, lead, and tellurium. Metal borides, carbides, nitrides, carbonitrides, bronze-structured oxides, and oxides structurally related to the bronze family (e.g., $WO_{2.9}$) may also be used.

[0051] Metal radiation absorbers may be used, either in the form of particles, as described for instance in U.S. Pat. No. 4,252,671, or as films, as disclosed in U.S. Pat. No. 5,256,506. Suitable metals include, for example, aluminum, bismuth, tin, indium, tellurium and zinc.

[0052] As indicated, a particulate radiation absorber may be disposed in a binder. The weight percent of the radiation absorber in the coating, excluding the solvent in the calculation of weight percent, is generally from 1 wt.% to 30 wt.%, preferably from 3 wt.% to 20 wt.%, and most preferably from 5 wt.% to 15 wt.%, depending on the particular radiation absorber(s) and binder(s) used in the LTHC.

[0053] Suitable binders for use in the LTHC layer include film-forming polymers, such as, for example, phenolic resins (e.g., novolak and resole resins), polyvinyl butyral resins, polyvinyl acetates, polyvinyl acetals, polyvinylidene chlorides, polyacrylates, cellulosic ethers and esters, nitrocelluloses, polycarbonates, and acrylic and methacrylic copolymers. Suitable binders may include monomers, oligomers, or polymers that have been or can be polymerized or crosslinked. In some embodiments, the binder is primarily formed using a coating of crosslinkable monomers and/or oligomers with optional polymer. When a polymer is used in the binder, the binder includes 1 to 50% polymer by non-volatile weight, preferably, 10 to 45% polymer by non-volatile weight.

[0054] Upon coating on the donor substrate, the monomers, oligomers, and polymers are crosslinked to form the LTHC. In some instances, if crosslinking of the LTHC layer is too low, the LTHC layer may be damaged by the heat and/or permit the transfer of a portion of the LTHC layer to the receptor with the transfer layer.

[0055] The inclusion of a thermoplastic resin (e.g., polymer) may improve, in at least some instances, the performance (e.g., transfer properties and/or coatability) of the LTHC layer. It is thought that a thermoplastic resin may improve the adhesion of the LTHC layer to the donor substrate. In one embodiment, the binder includes 25 to 50% thermoplastic resin by non-volatile weight, and, preferably, 30 to 45% thermoplastic resin by non-volatile weight, although lower amounts of thermoplastic resin may be used (e.g., 1 to 15 wt.%). The thermoplastic resin is typically chosen to be compatible (i.e., form a one-phase combination) with the other materials of the binder. A solubility parameter can be used to indicate compatibility, *Polymer Handbook*, J. Brandrup, ed., pp. VII 519-557 (1989). In at least some embodiments, a thermoplastic resin that has a solubility parameter in the range of 9 to 13 $(cal/cm^3)^{1/2}$, preferably, 9.5 to 12 $(cal/cm^3)^{1/2}$, is chosen for the binder. Examples of suitable thermoplastic resins include polyacrylics, styrene-acrylic polymers and resins, and polyvinyl butyral.

[0056] Conventional coating aids, such as surfactants and dispersing agents, may be added to facilitate the coating process. The LTHC layer may be coated onto the donor substrate using a variety of coating methods known in the art. A polymeric or organic LTHC layer is coated, in at least some instances, to a thickness of 0.05 μm to 20 μm, preferably, 0.5 μm to 10 μm, and, more preferably, 1 μm to 7 μm. An inorganic LTHC layer is coated, in at least some instances, to a thickness in the range of 0.001 to 10 μm, and preferably, 0.002 to 1 μm.

[0057] An optional interlayer may be disposed in the donor element between the donor substrate and the transfer layer to minimize damage and contamination of the transferred portion of the transfer layer and to reduce distortion in the transferred portion of the transfer layer. The interlayer may also influence the adhesion of the transfer layer to the rest of the donor element. Typically, the interlayer has high thermal resistance. The interlayer typically remains in contact with the LTHC layer during the transfer process and is not substantially transferred with the transfer layer.

[0058] Suitable interlayers include, for example, polymer films, metal layers (e.g., vapor deposited metal layers), inorganic layers (e.g., sol-gel deposited layers and vapor deposited layers of inorganic oxides (e.g., silica, titania, and other metal oxides)), and organic/inorganic composite layers. Organic materials suitable as interlayer materials include both thermoset and thermoplastic materials, and are preferably coated on the donor element between the LTHC layer and the transfer layer. Coated interlayers can be formed by conventional coating processes such as solvent coating, extrusion coating, gravure coating, and the like. Suitable thermoset materials include resins that may be crosslinked by heat, radiation, or chemical treatment including, but not limited to, crosslinked or crosslinkable polyacrylates, polymethacrylates, polyesters, epoxies, polyurethanes, and acrylate and methacrylate co-polymers. The thermoset materials may be coated onto the LTHC layer as, for example, thermoplastic precursors and subsequently crosslinked to form a crosslinked interlayer.

[0059] Suitable thermoplastic materials include, for example, polyacrylates, polymethacrylates, polystyrenes, polyurethanes, polysulfones, polyesters, and polyimides. These thermoplastic organic materials may be applied via conventional coating techniques (for example, solvent coating, spray coating, or extrusion coating). Typically, the glass transition temperature (T_g) of thermoplastic materials suitable for use in the interlayer is about 25 °C or greater, preferably 50 °C or greater, more preferably 100 °C or greater, and even more preferably 150 °C or greater. In an exemplary embodiment, the interlayer has a T_g that is greater that a temperature attained in the transfer layer during imaging.

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The interlayer may be either transmissive, absorbing, reflective, or some combination thereof, at the imaging radiation wavelength.

[0060] Inorganic materials suitable as interlayer materials include, for example, metals, metal oxides, metal sulfides, and inorganic carbon coatings, including those materials that are highly transmissive or reflective at the imaging light wavelength. These materials may be applied to the light-to-heat-conversion layer via conventional techniques (e.g., vacuum sputtering, vacuum evaporation, or plasma jet deposition).

[0061] The interlayer may provide a number of benefits. The interlayer may be a barrier against the transfer of material from the LTHC layer. It may also modulate the temperature attained in the transfer layer so that thermally unstable materials can be transferred. For example, the interlayer can act as a thermal diffuser to control the temperature at the interface between the interlayer and the transfer layer relative to the temperature attained in the LTHC layer. This can improve the quality (i.e., surface roughness, edge roughness, etc.) of the transferred layer.

[0062] The interlayer may contain additives, including, for example, photoinitiators, surfactants, pigments, plasticizers, and coating aids. The thickness of the interlayer may depend on factors such as, for example, the material of the interlayer, the material of the LTHC layer, the material of the transfer layer, the wavelength of the imaging radiation, and the duration of exposure of the donor element to imaging radiation. For polymer interlayers, the thickness of the interlayer typically is in the range of 0.05 μm to 10 μm, preferably, from about 0.1 μm to 4 μm, more preferably, 0.5 to 3 μm, and, most preferably, 0.8 to 2 μm. For inorganic interlayers (e.g., metal or metal compound interlayers), the thickness of the interlayer typically is in the range of 0.005 μm to 10 μm, preferably, from about 0.01 μm to 3 μm, and, more preferably, from about 0.02 to 1 μm.

[0063] Table III indicates an exemplary solution for coating an interlayer.

Table III:

Interlayer Formulation	
Component	Parts by Weight
Butvar™ B-98 (polyvinylbutyral resin, available from Monsanto, St. Louis, MO)	0.98
Joncryl™ 67 (acrylic resin, available from S.C. Johnson & Son, Racine, WI)	2.95
Sartomer™ SR351™ (trimethylolpropane triacrylate, available from Sartomer, Exton, PA)	15.75
Irgacure™ 369 (photocuring agent, available from Ciba Specialty Chemicals, Tarrytown, NY)	1.38
Irgacure™ 184 (photocuring agent, available from Ciba Specialty Chemicals, Tarrytown, NY)	0.2
-methoxy-2-propanol	31.5
methyl ethyl ketone	47.24

[0064] The transfer layer, or colorant layer, of the donor element can include an organic or inorganic colorant in an organic or inorganic crosslinkable composition. The colorant generally includes pigments, dyes, or inks, generally disposed in a binder. The transfer layer can optionally include a surfactant and other additives. Other additives may also be included such as an IR absorber, dispersing agents, surfactants, stabilizers, plasticizers, crosslinking agents and coating aids. The colorant layer may also contain a variety of additives including but not limited to dyes, plasticizers, UV stabilizers, film forming additives, and adhesives. Suitable dispersing resins include vinyl chloride/vinyl acetate copolymers, poly(vinyl acetate)/crotonic acid copolymers, polyurethanes, styrene maleic anhydride half ester resins, (meth)acrylate polymers and copolymers, poly(vinyl acetals), poly(vinyl acetals) modified with anhydrides and amines, hydroxy alkyl cellulose resins and styrene acrylic resins. An exemplary color transfer layer composition comprises 5-80% by weight colorant, 15-95% by weight resin, and 0-80% by weight crosslinking agent, dispersing agents, and additives.

[0065] Exemplary pigments and dyes include those listed as having good color permanency and transparency in the NPIRI Raw Materials Data Handbook, Volume 4 (Pigments). Examples of suitable transparent colorants include Ciba-Geigy Cromophtal Red A2B™, Dainich-Seika ECY-204™, Zeneca Monastral Green 6Y-CL™, and BASF Heliogen Blue L6700F™. Other suitable transparent colorants include Sun RS Magenta 234-007™, Hoechst GS Yellow GG 11-1200™, Sun GS Cyan 249-0592™, Sun RS Cyan 248-061, Ciba-Geigy BS Magenta RT-333D™, Ciba-Geigy Microlith Yellow 3G-WA™. Ciba-Geigy Microlith Yellow 2R-WA™, Ciba-Geigy Microlith Blue YG-WA™, Ciba-Geigy Microlith Black C-WA™, Ciba-Geigy Microlith Violet RL-WA™, Ciba-Geigy Microlith Red RBS-WA™, any of the Heucotech Aquis II™ series, any of the Heucosperse Aquis III™ series, and the like. Another class of pigments that can be used for color filter materials in the present invention are various latent pigments such as those available from Ciba-Geigy.

[0066] Either non-aqueous or aqueous dispersions of a colorant in a binder may be used. In the non-aqueous case,

solvent-based colorant dispersions may be used along with an appropriate solvent based binder (i.e. Elvacite™ acrylic resins available from ICI Chemicals). It can often be useful to employ an aqueous dispersion of colorant in binder. In this case, exemplary colorants include pigments in the form of binderless aqueous dispersions (i.e. Aquis II™ supplied by Heucotech) and exemplary binders include those specifically designed for pigment wetting (i.e. Neocryl BT™ acrylic resins from Zeneca Resins). The use of appropriate binders can promote the formation of sharp, well defined edges of the color filters during transfer. When the colorant transfer is induced by a high powered light source (i.e., xenon flash lamp), it may be helpful to include as a binder an energetic or gas producing polymer such as disclosed in U.S. Pat. Nos. 5,308,737 and 5,278,023.

[0067] The binder system includes organic and/or inorganic polymerizable and/or crosslinkable materials (i.e., monomers, oligomers, prepolymers, and/or polymers), and optionally an initiator system. Using monomers or oligomers can assist in reducing binder cohesive forces in the transfer layer, therefore improving imaging sensitivity and/or transferred image resolution.

[0068] The colors used to form the color filters are generally primary additive colors (i.e. red, green, and blue), and can also be primary subtractive color (e.g., cyan, magenta, and yellow). Each of these primary colors can have high color purity and transmittance, and, when combined, an appropriate white balance. For use in full color liquid crystal displays, exemplary color filters can have spectral characteristics of red, green, and blue, for example, that show chromaticity close to the National Television Standards Committee (NTSC) standard colors indicated by the Commission International de l'Eclairage (CIE) chromaticity diagram.

[0069] The optional transfer assist layer is typically a layer of adhesive coated as the outermost layer of the donor sheet. The adhesive serves to promote complete transfer of the colorant, especially during the separation of the donor from the receptor substrate after imaging. Exemplary transfer assist layers include colorless, transparent materials with a slight tack or no tack at room temperature, such as the family of resins sold by ICI Chemicals under the trade designation Elvacite™ (e.g., Elvacite™ 2776). Transfer assist layers can also be optionally disposed on the receptor.

[0070] Referring again to FIG. 3, after transferring multiple color filters to a display substrate and prior to crosslinking the transferred color filters, the color filters can be inspected for proper alignment, undesired defects, and the like. Inspection can take place using any suitable method of inspection. After an optional inspection and prior to crosslinking, the color filters can be removed for reworking of the display substrate. Removal of the color filters can be performed in any suitable manner. Typically, the color filters are removed before crosslinking by contact with a washing solution in which the color filter material is soluble. The color filters can be contacted with any suitable washing solution using any suitable method including spraying, immersing, and wiping. The particular washing solution used generally depends on the material of the binder and colorant in the color filter layer. For example, washing solutions suitable for removing some acrylate-based color filters prior to crosslinking include dilute ammonia, sodium hydroxide, various alcohols and ketones, and other such suitable solvents.

[0071] Removal of the color filters for reworking of the substrate can be particularly advantageous when using active display substrates. Active display substrates have a plurality of devices and can be a relatively expensive component in the display. Thus, the ability to rework an active substrate after removal of color filters can limit waste and reduce costs.

[0072] Referring again to FIG. 1, active layer 214 is commonly provided on bottom substrate 212 as shown. In other embodiments, active layer 214 can be provided on top substrate 226. For the sake of clarity, the active layer has been described throughout this document as being disposed on the bottom substrate; however, it is understood that the provision of an active layer on either or both substrates is contemplated in the present invention.

[0073] In general, active layer 214 includes a plurality of addressable devices, such as thin film transistors, and a plurality of address lines electrically connected to the devices. FIGs. 2(a) and (b) show a particular embodiment where thin film transistors 20 are arranged in a rectangular array, are addressed by address lines 32 and 34, and are connected to sub-pixel electrodes 12. The sub-pixel electrodes are typically made from a transparent conductive material, and each electrode typically covers an area that corresponds to a sub-pixel in the display. An exemplary transparent conductive material is indium tin oxide (ITO). Each pixel or sub-pixel of the display is preferably provided with one or more active devices, and may also be provided with one or more passive devices, such as capacitors, resistors, and the like. For example, capacitors can be added to sustain an address signal for a longer period of time so that the pixels can be refreshed less often. This can help increase the overall speed and brightness of the display.

[0074] Active layers can optionally include a black matrix to enhance contrast in the overall display by providing lines of relatively high optical density (and preferably relatively low surface reflectivity) that separate pixels or sub-pixels and/or that protect the active devices from undesired light-induced activation. The black matrix can be disposed between the active layer and the substrate, within the active layer, or between the active layer and the liquid crystal layer. One embodiment is shown in FIG. 2(b) where black matrix 50 is disposed on the active layer. Whereas the address lines can be used as a black matrix, a higher optical density and lower surface reflectivity can often be obtained by depositing a separate black matrix material.

[0075] Examples of suitable black matrix materials include metals, such as chromium, provided as a layer or as

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particles in a binder; metal oxides, nitrides, sulfides, and the like, including chromium oxides, aluminum oxides, and others provided as a layer or as particles in a binder; other opaque inorganic materials provided as a layer or as particles in a binder; and organic materials such as carbon black, dark pigments or dyes, or other black colorants disposed in a binder. An exemplary black matrix has on optical density that is greater than 2, and preferably greater than 2.5.

[0076] A black matrix can be provided on an active substrate using any suitable method. For example, conventional photolithography techniques can be used to pattern black matrix on the active substrate. Black matrix materials can also be directly patterned on the substrate by deposition through a mask or by various conventional printing methods including thermal print head and ink jet methods. An exemplary method of patterning black matrix on active substrates is by selective thermal mass transfer of black matrix material from a donor element to the active substrate by selectively exposing the donor element to imaging radiation such as from a laser or a flash lamp, as discussed in more detail below.

[0077] When black matrix material is disposed adjacent to active layers on active substrates, it may be desirable for the material to combine the advantages of a high optical density (i.e., 2 or greater) using a relatively thin coating while having a high resistivity (i.e., 1×10^{10} ohm-cm or greater) that substantially prevents crosstalk between adjacent devices through the black matrix. Crosstalk is an undesired leakage of current or inducement of a signal voltage between devices or electrodes. Various metal oxides, nitrides, sulfides, etc. can be used that provide the benefits of high optical density and high resistivity. An exemplary organic black matrix material that has high optical density and high resistivity and that is suitable for use on active display substrates is disclosed in WO-A-00/69649. The black matrix material there disclosed can be especially useful when constructing thin displays because a thin black matrix can be formed using organic material while maintaining a high optical density and high resistivity.

[0078] An exemplary method of patterning a black matrix onto display substrates for active displays includes selective thermal mass transfer of a black matrix material from a donor element. The donor element can be heated by the application of directed heat on selected portions of the donor element. Heat can be generated by using a heating element, converting radiation (e.g., light) to heat, and/or applying an electrical current to a layer of the donor element. In many instances, thermal transfer using light from, for example, a lamp or laser, is advantageous because of the accuracy and precision that can often be achieved. Imagewise transfer of material from the donor element to a receptor can be achieved by placing a radiation absorber in the donor element and selectively radiating the donor element, for example, using a directed laser beam or a flash lamp shined through a mask. To effect transfer of material from the donor to the receptor, imaging radiation can generally be directed through the donor element. In some instances, it may be desirable to direct imaging radiation through the receptor.

[0079] Donor elements suitable for transferring black matrix material are similar to donor elements suitable for selective thermal mass transfer of color filter material as described above. Exemplary donor element constructions for transferring black matrix materials are disclosed in WO-A-00/69649. One suitable donor element construction includes a polyester film substrate that has an optional primer layer, an LTHC layer, a temperature modulation interlayer, and a black matrix transfer layer. Another suitable donor element has a two-layer construction including a base film and a transferable layer of black matrix material coated on the base film. The transferable layer can function as an LTHC layer in this construction.

[0080] Referring again to FIG. 2(b), a planarization layer 16 can also be included on the active substrate 10a. Due to the many components disposed on the active substrate, the surface profile of the active substrate tends to be non-uniform. Without a planarization layer, the non-uniform surface profile can lead to non-uniform spacings between the top and bottom substrate. Non-uniform spacings can undesirably affect liquid crystal performance and lead to non-uniform display characteristics. The planarization layer can be used to provide a substantially planar surface so that a uniform gap between substrates can be maintained. Planarization layer materials are preferably non-birefringent and substantially transparent to light so that the display performance is not adversely affected. Suitable planarization layer materials include various planarization layer and overcoat materials known in the art such as the overcoat materials for LCD panel construction commercially available from JSR Corporation, Yokkaichi, Japan.

[0081] In a particular embodiment, when the sub-pixel electrodes 12 are formed on the planarization layer 16 as in FIG. 2(b), through holes 28 can be formed in the intermediate layers, such as the planarization layer 16 and color filters R, G, and B, so that electrical contact can be made between the sub-pixel electrodes 12 and the drain electrodes 26 of transistors 20. Through holes can be made using any suitable technique such as etching (e.g., using an etch mask to define through hole positions) or laser ablation. An exemplary method involves coating a photoresist material over the color filters and planarization layer, photolithographically creating holes in the resist coating in the positions where the through holes are to be formed, and etching the exposed portions of the planarization layer and color filters to form through holes for connecting the sub-pixel electrodes to the drain electrodes. The photoresist mask can then be removed.

[0082] Another method involves patterning a curable photoresist planarization layer to also act as a through hole etch mask. In this way, the portions of the color filters exposed by the patterned holes in the planarization layer/etch mask can be etched to complete the through holes. The photoresist coating can remain after etching to form the planarization layer.

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[0083] In one embodiment, color filter formulations suitable for use with through hole etching processes include those that have a colorant dispersed in a binder that is soluble in solvents compatible with active matrix display substrates. Examples include color filter materials that have a colorant dispersed in an alkali soluble resin and a water soluble thermal crosslinker. The alkali soluble resin can include an acrylic copolymer that contains an acrylic acid unit or a methacrylic acid unit, and the crosslinker can include a water soluble melamine resin. Illustrative formulations of alkali soluble color filter materials for red, green, and blue color filters are given in Table IV.

Table IV:

Alkali Soluble Color Filter Formulations			
Red Color Filter Material			
Material	**Source**	**Function**	**Parts by weight**
Cromophtal Red A2B	Ciba-Geigy	red pigment	80
ECY-204	Dainich-Seika	yellow pigment	20
Disperbyk 161	BYK-Chemie	dispersant	18.4
Elvacite 2669	ICI	acrylic resin	134.3
Cymel 370	Mitsui Cytec	crosslinker	80.6
Green Color Filter Material			
Monastral Green 6Y-CL	Zeneca	green pigment	80
ECY-204	Dainich-Seika	yellow pigment	20
Disperbyk 161	BYK-Chemie	dispersant	17.4
Elvacite 2669	ICI	acrylic resin	121.9
Cymel 370	Mitsui Cytec	crosslinker	73.2
Blue Color Filter Material			
Heliogen Blue L6700F	BASF	blue pigment	100
Disperbyk 161	BYK-Chemie	dispersant	15
Elvacite 2669	ICI	acrylic resin	178.1
Cymel 370	Mitsui Cytec	crosslinker	106.9

[0084] Referring again to FIGs. 2(a) and (b), transparent sub-pixel electrodes 12 can be any suitable conductive material that is substantially transparent to light, and can be patterned using any suitable patterning method such as conventional photolithography and/or sputter deposition through a mask. Various transparent conductive oxides can be used, typically indium tin oxide (ITO). For application of a uniform electric field through the sub-pixel area defined by a sub-pixel electrode, the electrode is preferably formed on a substantially flat surface. For example, the sub-pixel electrodes can be formed directly on the bottom substrate or directly on a planarization layer or other layer. FIG. 2(b) shows transparent sub-pixel electrodes 12 formed on planarization layer 16.

[0085] In a particular embodiment, the liquid crystal material in a display of the present invention can be selected to improve display performance. Referring again to FIG. 1, liquid crystal layer 220 can contain any liquid crystal material or mixture of liquid crystal materials suitable for electronic display device applications. Commonly used liquid crystal materials include nematic, chiral nematic, and ferroelectric liquid crystals. In general, these materials are classified according to their mode of operation, which includes their orientation in a display and behavior upon application of an electric field.

[0086] Some liquid crystal materials are oriented to wind and unwind in the plane of the liquid crystal layer. The rotation of the liquid crystal material causes the polarization of transmitted light to rotate as it passes through the liquid crystal. Application of an electric field changes the rotation of the liquid crystal material so that light rays transmitted through activated pixel areas have differently oriented polarizations than those transmitted through non-activated pixel areas. Some liquid crystal materials are oriented so that their molecules tilt along the surface of a cone whose symmetry axis lies in the plane of the liquid crystal layer. Upon application of an electric field, the liquid crystal molecules tilt along the surface of the cone. The orientation of the molecules controls the polarization of light transmitted.

[0087] The modes of liquid crystal displays that are most extensively employed at the present time are twisted nematic

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(TN), supertwisted birefringence effect (SBE), and dynamic scattering (DS), all employing nematic or chiral nematic (cholesteric) liquid crystals. These devices are based upon the dielectric alignment effects of the nematic and/or chiral nematic liquid crystal (or mixtures of nematic or chiral nematic liquid crystals) upon application of an electric field. The average molecular long axis of the liquid crystal material takes up a preferred orientation in the applied electric field, the orientation of which is dependent on the sign of the dielectric anisotropy of the material or mixture, and this orientation relaxes upon removal of the applied electric field. This reorientation and relaxation is slow, on the order of a few milliseconds.

[0088] Although nematic and chiral nematic liquid crystals are the most extensively employed, there are liquid crystal devices that employ more highly ordered smectic liquid crystals. These devices are also based on the dielectric reorientation of the liquid crystals, and response times are on the order of milliseconds. A recent advance in the liquid crystal art has been the utilization of tilted chiral smectic liquid crystals, which are also termed ferroelectric liquid crystals (FLC), in devices which give microsecond switching. Accordingly, displays of the present invention can employ FLC material to obtain faster switching speeds. FLC materials properly aligned in a liquid crystal display can exhibit bistability and symmetric switching characteristics, which can lead to reduced power consumption, as discussed in more detail below with regard to alignment layers.

[0089] In a particular embodiment, displays of the present invention can include FLC materials and mixtures thereof. In some embodiments, the liquid crystal material can contain fluorinated chiral FLC compositions. Particularly suited fluorine-containing FLC materials that have recently been developed include those disclosed in U.S. Pat. Nos. 4,886,619; 5,082,587; and 5,262,082.

[0090] FLC development has been hindered by problems with defects in the liquid crystal layer structure. These defects arise due to layer shrinkage upon cooling (through the temperature ranges associated with the tilted smectic mesophases) and the resulting formation of a "chevron" layer structure (see, e.g., the discussion by T. P. Rieker et al. in *Phys. Rev. Lett.* 59, 2658 (1987) and *Ferroelectrics* 113, 245 (1991), as well as the discussion by Y. Ouchi et al. in *Jpn. J. Appl. Phys.* 27, L1993 (1988)). The defects and chevron layer structure often result in a poor contrast ratio and unstable bistability.

[0091] To minimize these defects, admixtures of liquid crystal compounds that contract upon cooling through at least one tilted smectic mesophase (positive compounds) and liquid crystal compounds that expand upon cooling through at least one tilted smectic mesophase (negative compounds) can be prepared to control the liquid crystal layer expansion or contraction behavior, as disclosed in U.S. Pat. No. 5,417,883. Such mixtures can be used to effect an essentially temperature-independent layer spacing in the tilted smectic mesophase(s), as well as a reduced temperature dependence of the layer spacing in the temperature range associated with the transition between the non-tilted and the tilted mesophases. The process of proper admixing of liquid crystal compounds to yield a mixture that has complementary expansion and contraction behavior enables the control of layer spacing in the tilted smectic mesophase(s) and thereby the control or suppression of chevron layer geometry. Such suppression reduces or eliminates the formation of zigzag alignment defects upon cooling through the tilted smectic mesophase(s), resulting in an improved electrooptical switching performance, increased memory to driven cone-tilt angle ratios, and improved contrast ratios. The process also enables the reduction or elimination of the stress-induced defects and non-bookshelf layer geometry which result from heating and cooling cycles.

[0092] Preferred smectic or latent smectic liquid crystal compounds which can be utilized in the negative compositions are chiral or achiral liquid crystal compounds which have at least one fluorinated terminal portion and which exhibit negative thermal layer expansion behavior in at least one tilted (or latent tilted) smectic mesophase. A preferred class of such compounds is that class of chiral or achiral liquid crystal compounds which have at least one fluoroether terminal portion containing at least two catenary, i.e., in-chain, ether oxygen atoms and which exhibit negative thermal layer expansion behavior. Such compounds can comprise, e.g., (a) an aliphatic fluorocarbon terminal portion containing at least two catenary ether oxygen atoms; (b) an aliphatic hydrocarbon terminal portion; and (c) a central core connecting the terminal portions. The aliphatic hydrocarbon terminal portion of the compounds can be either chiral or achiral. (Such achiral compounds are described in U.S. Pat. No. 5,262,082 to Janulis et al.)

[0093] Another preferred class of liquid crystal compounds which have at least one fluorinated terminal portion and which can be utilized in the negative compositions are those smectic or latent smectic, chiral or achiral liquid crystal compounds which have at least one fluoroaliphatic terminal portion (e.g., the compounds described in U.S. Pat. No. 4,886,619 and U.S. Pat. No. 5,082,587 and which exhibit negative thermal layer expansion behavior in at least one tilted (or latent tilted) smectic mesophase. For example, 5-hexyl-2-(4'-1,1-dihydroperfluorooctyloxy) phenylpyrimidine has been found to exhibit such behavior and to be suitable for such use.

[0094] Other liquid crystal compounds which possess a mechanism which offsets the layer shrinkage associated with the tilting of the molecules in at least one tilted (or latent tilted) smectic mesophase and which thereby exhibit negative thermal expansion behavior in the mesophase(s) can also be utilized in the negative compositions.

[0095] Liquid crystal compositions suitable for use in admixture with the above-described negative compositions are those compositions which have a net positive thermal layer expansion in at least one tilted (or latent tilted) smectic

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mesophase and which comprise at least one smectic or latent smectic liquid crystal compound. Smectic (or latent smectic) liquid crystal compounds suitable for inclusion in the liquid crystal compositions having net positive thermal expansion behavior (hereinafter termed "positive compositions") include chiral and achiral liquid crystal compounds which have aliphatic terminal portions and which exhibit positive thermal layer expansion behavior in at least one tilted (or latent tilted) smectic mesophase, e.g., compounds such as the alkyl, alkoxy phenylpyrimidines and the alkoxy, alkoxy phenylbenzoates described by D. Demos et al., *Flussige Kristalle in Tabellen, VEB Deutscher Verlag fur Grundstoffindustrie*, pages 65-76 and 260-63, Leipzig (1974) and by S. Kumar, *Phys. Rev. A* 23, 3207 (1984); chiral and achiral liquid crystal compounds which have at least one fluoroaliphatic terminal portion (such compounds are described, e.g., in U.S. Pat. No. 4,886,619 and U.S. Pat. No. 5,082,587) and which exhibit positive thermal layer expansion behavior in at least one tilted (or latent tilted) smectic mesophase; and chiral and achiral liquid crystal compounds which have at least one fluoroether terminal portion containing only one catenary ether oxygen atom and which exhibit positive thermal layer expansion behavior in at least one tilted (or latent tilted) smectic mesophase. The latter compounds can be, e.g., compounds which comprise (a) an aliphatic fluorocarbon terminal portion containing one catenary ether oxygen atom; (b) an aliphatic hydrocarbon terminal portion; and (c) a central core connecting the terminal portions.

[0096] When compound(s) that have a fluoroether terminal portion containing at least two catenary ether oxygen atoms are used as the major component(s) of the negative compositions, the compositions can preferably be combined with positive compositions comprising (as the major component(s)) at least one chiral or achiral liquid crystal compound having a fluoroaliphatic terminal portion or, more preferably, a fluoroether terminal portion containing only one catenary ether oxygen atom. Such combinations are preferred from the standpoint of compatibility.

[0097] An important characteristic of a liquid crystal display device is its response time, i.e., the time required for the device to switch from the on (light) state to the off (dark) state. In a ferroelectric or anti-ferroelectric device, the response time is proportional to the rotational viscosity of the liquid crystal compound(s) contained within the device and is inversely proportional to their polarization and to the applied electric field. Thus, the response time can be reduced by using compound(s) having high polarizations or low viscosities. Briefly, liquid crystal materials suitable for use in this invention and that provide fast response times include fluorine-containing, chiral liquid crystal compounds having smectic mesophases or latent smectic mesophases. (Compounds having latent smectic mesophases are those which by themselves do not exhibit a smectic mesophase, but which, when in admixture with compounds having smectic mesophases or with other compounds having latent smectic mesophases, develop smectic mesophases under appropriate conditions.) Chiral liquid crystal compounds that provide fast response times include those materials described in the following U.S. Patents: 5,855,812; 5,702,637; 5,658,491; 5,482,650; 5,474,705; 5,437,812; 5,417,883; 5,399,291; 5,377,033; 5,262,082; 5,254,747; 5,082,587; 5,062,691; and 4,886,619.

[0098] Another advantage that can be obtained from using suitable liquid crystal mixtures as described above in displays of the present invention is a low birefringence. The low birefringence of these fluorine-containing liquid crystal compounds (relative to their nonfluorine-containing analoques) allows the fabrication of devices with somewhat larger device spacings without substantial loss of light transmission. Light transmission through, e.g., a surface-stabilized ferroelectric device (as described in U.S. Pat. No. 4,367,924) with two polarizers is represented by the following equation:

$$I=I_o\,(\sin^2(4\Theta))(\sin^2(\pi\Delta nd/\lambda))$$

where I_o is the transmission through parallel polarizers, Θ is the liquid crystal material tilt angle, Δn is the liquid crystal birefringence, d is the device spacing, and λ is the wavelength of light used. To maximize the transmission, both $\sin^2(4\Theta)$ and $\sin^2(\pi\Delta nd/\lambda)$ should be at maximized. This occurs when each term equals one. The first term is a maximum when the tilt angle equals 22.5°. This is a function of the liquid crystal and is constant for a given material at a given temperature. The second term is maximum when $\Delta nd=\lambda/2$. This demonstrates the criticality of the low birefringence of the materials of this invention. Low birefringence allows a larger device thickness, d, for a given wavelength of light. Thus, a larger device spacing is possible while still maximizing transmission, allowing easier device construction.

[0099] Referring again to FIG. 1, alignment layers 218 and 222 can be applied to portions of the interior surfaces of the substrate elements of the display to cause a desired orientation of the liquid crystal material at the interface of the liquid crystal layer 220. A proper alignment of the liquid crystal molecules allows light to be rotated through angles that are complementary to the alignment of the polarizers associated with the cell. The particular alignment layers used commonly depends on the type of liquid crystal material used. Examples of alignment layer materials include certain polyimides, polyamides, polyesters, polysiloxanes, nylon copolymers, organosilsequioxane polymers, and other suitable polymers capable of being disposed on a display substrate and oriented for alignment. Inorganic alignment layers, such as silicon oxides, can also be used. A common method of orienting polymeric alignment coatings is by a physical rubbing process. Alignment layers 218 and 222 can be the same or different materials that provide symmetric or asym-

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metric alignment. Particularly useful asymmetric alignment schemes are described in U.S. Pat. Nos. 5,377,033 and 5,831,705.

[0100] When FLC materials are used, alignment layer schemes that provide the FLC layer with good bistability and symmetric switching characteristics can result in displays that have lower power consumption. Good bistability and symmetric switching potentials can reduce the need for frequent pixel resetting and/or depolarization due to charge build up. An alignment layer scheme that may be suitable for these purposes is disclosed in U.S. Pat. No. 5,831,705.

[0101] In a particular embodiment, displays of the present invention include spacers selected to improve overall display performance. Referring again to FIG. I, spacers (not shown) can be provided in the liquid crystal layer 220 to maintain a desired gap between the top substrate 226 and bottom substrate 212. For example, FIG. 2(b) shows spacers 42 disposed in liquid crystal layer 40 to maintain a gap between top substrate 10b and bottom substrate 10a. Control of the spacings and mechanical forces within the construction of a flat panel display can often be critical to the performance of the device, and can depend upon the incorporation of physical spacers into the display. In liquid crystal displays (LCDs), the polarization of the light exiting the display is controlled in part by the optical path length through the liquid crystal layer. In current display technology, the thickness of the liquid crystal layer is determined by spacers, which may be in the form of particles (i.e., spherical beads or fibers), columnar structures (i.e., posts or pillars), microribs, etc.

[0102] A common method for controlling the thickness of the liquid crystal layer is to deposit a random arrangement of particles having a narrow size distribution over the entire surface of the substrate or alignment layer. This process has an obvious disadvantage in that there is no control over the placement of the particles resulting in a high percentage of the particles appearing in the display windows, thus decreasing the amount of light that may pass through the display. In many applications, the particles are not anchored to the substrate and may shift or migrate causing artifacts to appear in those areas in the display cell. To prevent particle migration, the opposing display substrates are commonly compressed so that the smaller spacer particles become pinned. Generally, thicker glass substrates are preferred to withstand the compression step and to resist local deformation from the larger spacer particles that are stressed during compression.

[0103] Spacers can also be selectively placed in desired locations between substrate elements in a liquid crystal display, for example by photolithographic techniques and by thermal mass transfer techniques. These techniques can be used to form highly uniform spacers that typically include a binder material. The binder material can help prevent migration of the spacers by adhering to the substrate. In addition, the binder material can give more compressibility to the spacers during assembly of the display, thus reducing stresses on the glass substrates during assembly, and can be hardened after assembly to hold the desired spacing. The sizes of the spacers can also be better controlled. These factors can allow thinner glass substrates to be used.

[0104] Selectively placed spacers can also be used as a black matrix. For example, spacers that have a relatively high optical density (e.g., 2 or greater) can be selectively placed in alignment with devices on active substrates to prevent undesired light induced activation of the devices. FIG. 2(b) shows a construction where spacers 42 are aligned with transistors 20.

[0105] An exemplary method for providing uniform spacers in flat panel displays is disclosed in U.S. Pat. No. 5,710,097. Spacer elements can be placed between substrates by selectively irradiating a thermal transfer donor sheet that comprises (a) a support, (b) an optional light-to-heat conversion layer, (c) an optional non-transferable interlayer, (d) a transferable spacer layer and (e) an optional adhesive layer. The process includes the following steps: (i) placing in intimate contact a receptor and the thermal transfer donor sheet described above, (ii) irradiating at least one of the thermal transfer donor sheet or the receptor (or a portion thereof, i.e., substrate, spacer layer, interlayer, light-to-heat conversion layer, and/or adhesive layer) with imaging radiation to provide sufficient heat in the irradiated areas to transfer the spacer layer to the receptor, and (iii) transferring the transferable spacer layer in the irradiated areas to the receptor.

[0106] The thermal transfer donor sheet can be prepared by depositing layers (b), (c), (d) and/or (e) described above onto a support. The support may be constructed of any material known to be useful as a support for a thermal transfer donor sheet. The support may be either a rigid sheet material such as glass or a flexible film. The support may be smooth or rough, transparent, opaque, translucent, sheet-like or non-sheet-like. Suitable film supports include polyesters, especially polyethylene terephthalate (PET), polyethylene naphthalate (PEN), polysulfones, polystyrenes, polycarbonates, polyimides, polyamides, cellulose esters such as, cellulose acetate and cellulose butyrate, polyvinyl chlorides and derivatives thereof, and copolymers comprising one or more of the above materials. Typical thicknesses of the support are between about 1 to 200 microns.

[0107] The transferable spacer layer may include organic materials, inorganic materials, or a composite comprising organic materials or inorganic materials that have particles or fibers incorporated therein. Suitable materials include any number of known polymers, copolymers, oligomers and/or monomers. Suitable polymeric binders include materials such as thermoset, thermosettable, or thermoplastic polymers, including phenolic resins (i.e., novolak and resole resins), polyvinylacetates, polyvinylidene chlorides, polyacrylates, cellulose ethers and esters, nitrocelluloses, polycar-

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bonates, polysulfones, polyesters, styrene/acrylonitrile polymers, polystyrenes, cellulose ethers and esters, polyacetals, (meth)acrylate polymers and co-polymers, polyvinylidene chloride, a-chloroacrylonitrile, maleic acid resins and copolymers, polyimides, poly(amic acids), and poly(amic esters) and mixtures thereof.

[0108] When the transferable spacer layer includes a thermosettable binder, the thermosettable binder may be crosslinked after transfer to the receptor. The binder may be crosslinked by any method which is appropriate for that particular thermosettable binder, for example, exposing the thermosettable binder to heat, irradiating with a suitable radiation source, or a chemical curative.

[0109] Particles or fibers may be added to the transferable spacer layer to form a composite. The addition of particles or fibers to the transferable spacer layer may be accomplished by using any known particle or fiber with a spacing dimension less than or equal to the spacing required in the particular display device of interest. The particles may have a spacing dimension smaller than the thickness of the transferable spacer layer or a spacing dimension larger than the thickness of the transferable spacer layer. When the particle size is smaller, the thickness of the transferable spacer layer controls the spacing within the display device. Whereas, when larger particles are used the spacing dimension of the particles used in the composite controls the spacing in the display device. Preferably at least 5% of the particles have a spacing dimension greater than the thickness of the spacer layer and more preferably at least 10%. Either approach may be used as a means for achieving uniform separation and support of the substrates within the display. Suitable particles include organic and/or inorganic materials (solid or hollow) having any suitable shape (i.e., spheres, rods, posts, triangles, and trapezoids) and size distribution consistent with maintaining the desired separation. Preferred particles include current LCD spacer spheres, rods, etc. comprised of glass or plastic such as those referenced in Japanese Kokai Patent Application No. HEI 7[1995]-28068; U.S. Pat. Nos. 4,874,461; 4,983,429; and 5,389,288. In LCD displays, it is preferred that the standard deviation for the size distribution of particles is + or - 20% of the mean particle spacing dimension (i.e., mean diameter of a spherical or cylindrical shaped particle, or average height of a cylindrical shaped particle). More preferably, the standard deviation is + or -10% of the mean. Most preferably, the standard deviation is + or -5% of the mean. When a fiber is used, the dimensions are typically measured as the denier (or fineness) of the fiber.

[0110] Dispersants, surfactants and other additives (i.e., antioxidants, light stabilizers, and coating aid may be included to aid in the dispersion of the particles and/or fibers or impart other desirable properties to the transferable spacer layer as known to those skilled in the art.

[0111] The compressibility of the element bearing the forces in the display (e.g., the particles in the case where the spacer layer comprises particles with a particle spacing dimension greater than the thickness of the transferable spacer layer and the transferable spacer layer in cases where the spacer layer does not comprise particles with particle spacing dimensions greater than the thickness of the transferable spacer layer) should be sufficient to maintain a uniform spacing gap in the corresponding display.

[0112] The receptor for spacer placement may be any flat panel display element benefiting from the application of spacers. The spacers can be precisely placed in the desired locations to avoid optical interference in the display windows of the display device. The receptor may be optionally coated with an adhesive topcoat to facilitate the transfer of the transferable spacer layer to the receptor.

[0113] Referring again to FIG. 1, bottom substrate 212 and top substrate 226 can be any type of substrate suitable for display applications. Substrates suitable for use in transmissive or transflective liquid crystal displays of the present invention include rigid or flexible substrates that are substantially transmissive to visible light. Non-birefringent substrates are particularly suited. Examples of rigid substrates include glass, low temperature polysilicon (LTPS), and rigid plastic. Suitable flexible substrates include substantially clear and transmissive polymer films. Suitable polymer substrates include polyester base (e.g., polyethylene terephthalate, polyethylene naphthalate), polycarbonate resins, polyolefin resins, polyvinyl resins (e.g., polyvinyl chloride, polyvinylidene chloride, polyvinyl acetals, etc.), cellulose ester bases (e.g., cellulose triacetate, cellulose acetate), and other conventional polymeric films used as supports in various imaging arts. A transparent polymeric film base of 2 to 100 mils (i.e. 0.05 to 2.54 mm) is preferred.

[0114] For glass substrates, a preferred thickness is 0.2 to 2.0 mm. It is often desirable to use glass substrates that are 1.0 mm thick or less, or even 0.7 mm thick or less. Thinner substrates result in thinner and lighter weight displays. Certain processing, handling, and assembling conditions, however, may suggest that thicker substrates be used. For example, some assembly conditions may require compression of the display assembly to fix the positions of spacers disposed between the substrates. The spacers are distributed to help maintain a uniform gap between the substrates in which the liquid crystal material can be disposed. Under such assembly conditions, suitable substrates are those that can withstand the stresses required to compress the spacers as well as resist local deformation caused by larger spacers that undergo higher compressive stressing. The competing concerns of thin substrates for lighter displays and thick substrates for reliable handling and processing can be balanced to achieve a preferred construction for particular display dimensions. As described above, an improved display of the present invention can include spacers that allow reliable assembly of displays that have thinner substrates.

[0115] If the substrate is a polymeric film, it is preferred that the film be non-birefringent to substantially prevent

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interference with the operation of the display in which it is to be integrated. Exemplary non-birefringent substrates are polyesters that are solvent cast. Typical examples of these are those derived from polymers consisting or consisting essentially of repeating, interpolymerized units derived from 9,9-bis-(4-hydroxyphenyl)-fluorene and isophthalic acid, terephthalic acid or mixtures thereof, the polymer being sufficiently low in oligomer (i.e., chemical species having molecular weights of about 8000 or less) content to allow formation of a uniform film. This polymer has been disclosed as one component in a thermal transfer receiving element in U.S. Pat. No. 5,318,938. Another class of non-birefringent substrates are amorphous polyolefins (e.g., those sold under the trade designation Zeonex™ from Nippon Zeon Co., Ltd.).

[0116] In a particular embodiment of a display of the present invention, a bottom polarizer (or combination of polarizers) can be selected to improve the display performance. Referring again to FIG. 1, polarizer 210 can be a reflective polarizer, dichroic polarizer, or other suitable polarizer or combination of polarizers. For back-lit display modes that use a light source such as light source 202 to illuminate the display from below the bottom substrate 212, an exemplary polarizer 210 is a combination of a reflective polarizer and a dichroic polarizer. For example, FIG. 2(b) shows a combination bottom polarizer 64 that includes a reflective polarizer 60 and a dichroic polarizer 62. An exemplary combination polarizer is disclosed in International Publication WO 95/17691. The reflective and dichroic polarizers can be provided in close proximity to one another, and are preferably bonded together to eliminate the air gap between the polarizers. A particularly suited reflective polarizer/dichroic polarizer combination is one in which a polyvinyl alcohol (PVA) coating is disposed on a multilayer birefringent reflective polarizer and is concurrently oriented. The PVA is dyed to form a dichroic polarizer coating on the reflective polarizer, as disclosed in International Publication WO 95/17691. The combination of a dichroic polarizer coated onto a reflective polarizer can provide a particularly thin and efficient polarizer.

[0117] An advantage of including a reflective polarizer in the bottom polarizer of a display of the present invention is that light having an undesired polarization state can be reflected by the reflective polarizer and recycled for transmission through the reflective polarizer. Recycling of light in this manner can allow more light to pass through the display relative to using absorptive polarizers. This can allow brighter displays that use less power. Particularly suited reflective polarizers include birefringent multilayer reflective polarizers as disclosed in U.S. Pat. No. 5,686,979 and in International Publication WO 95/17691 and birefringent diffusely reflective polarizers as disclosed in International Publication WO 97/32226. When birefringent multilayer reflective polarizers are combined with a dichroic polarizer coating as discussed above, a particularly thin combination reflective/dichroic polarizer can be obtained that can also enhance the brightness of the display.

[0118] This invention may be suitably practiced in the absence of any element not specifically described in this document.

[0119] Various modifications and alterations of this invention will be apparent to one skilled in the art from the description herein without departing from the scope of this invention as recited in the appended claims. Accordingly, the invention is to be defined by the limitations in the claims and any equivalents thereto.

Claims

1. A method of making an electronic display comprising:

    a light source;
    a polarizer disposed to transmit and polarize a portion of light from the light source; and
    a liquid crystal display panel disposed to utilize polarized light transmitted by the polarizer, the display panel including

        a bottom substrate,
        a top substrate spaced a distance apart from the bottom substrate,
        a bistable liquid crystal layer comprising a fluorinated chiral ferroelectric liquid crystal material disposed between the top and bottom substrates, and
        a multi-color active layer disposed between the bottom substrate and the liquid crystal layer, including a plurality of independently addressable active elements electrically connected to transparent conductive sub-pixel elements and a plurality of thermally transferred color filters that include a colorant in a crosslinked composition, each color filter aligned with one or more of the transparent conductive sub-pixel elements;

    whereby the method comprises the steps of:

        providing a display substrate comprising the bottom substrate and the plurality of independently address-

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able active elements electrically connected to transparent conductive sub-pixel elements;
thermally mass transferring a plurality of color filters to selected portions of the substrate, each color filter comprising a colorant in a crosslinkable composition;
inspecting the color filters after the transferring step
performing a washing step, if necessary, to remove the color filters from the substrate for reworking of the active substrate; and
crosslinking the color filters after the inspecting step.

2. The method of claim 1, wherein the electronic display further comprises a black matrix disposed on the active substrate to separate sub-pixels, the black matrix having an optical density sufficient to provide an optical contrast between sub-pixels and a resistivity to substantially prevent crosstalk between adjacent independently addressable transistors.

3. The method of claim 1, wherein the electronic display further comprises a plurality of spacers disposed between the first and second substrates to maintain a substantially uniform gap therebetween.

4. The method of claim 3, wherein the spacers are selectively thermally mass transferred.

5. The method of claim 1, wherein the polarizer includes a birefringent reflective polarizer and a dichroic polarizer interposed between the reflective polarizer and the bottom substrate.

6. A method of making an electronic display comprising:

a first transparent substrate having a plurality of independently addressable thin film transistors disposed thereon, each transistor electrically connected to an associated transparent conductive sub-pixel element;
a second transparent substrate spaced a distance apart from the first transparent substrate;
a liquid crystal layer disposed between the first substrate and the second substrate; and
a plurality of thermally transferred color filters disposed between the first substrate and the liquid crystal layer, the color filters comprising a colorant in a crosslinked composition, each color filter aligned with one or more of the transparent conductive elements associated with the transistors;

whereby the method comprises the steps of:

providing a display substrate comprising the first transparent substrate thermally mass transferring a plurality of color filters to selected portions of the substrate, each color filter comprising a colorant in a crosslinkable composition;
inspecting the color filters after the transferring step;
performing a washing step, if necessary, to remove the color filters from the substrate for reworldng of the active substrate; and
crosslinking the color filters after the inspecting step.

7. The method of claim 6, wherein the electronic display further comprises a black matrix disposed on the first substrate, the black matrix having an optical density sufficient to provide an optical contrast between sub-pixels and a resistivity to substantially prevent crosstalk between adjacent independently addressable transistors.

8. The method of claim 6, wherein the electronic display further comprises a plurality of spacers disposed between the first and second substrates to maintain a substantially uniform gap therebetween.

9. The method of claim 8, wherein the spacers are disposed to prevent light induced activation of the transistors.

10. The method of claim 6, wherein the electronic display further comprises a light source and a reflective polarizer disposed to transmit to the liquid crystal layer light from the light source having a first polarization state and to reflect light having a second, orthogonal polarization state back toward the light source.

11. A process for making a color display substrate comprising the steps of:

providing an active display substrate;
thermally mass transferring a plurality of color filters to selected portions of the substrate, each color filter

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comprising a colorant in a crosslinkable composition;
inspecting the color filters after the transferring step
performing a washing step, if necessary, to remove the color filters from the substrate for reworking of the active substrate; and
crosslinking the color filters after the inspecting step.

12. The process of claim 11, wherein the step of thermally mass transferring a plurality of color filters comprises:

providing a donor sheet comprising a base layer, a light to heat converter, and a transfer layer comprising a colorant in a crosslinkable composition;
placing the transfer layer proximate to the display substrate; and
selectively irradiating portions of the donor sheet to thermally transfer portions of the transfer layer from the donor sheet to the display substrate.

13. The process of claim 11, further comprising the step of forming a black matrix on the display substrate.

14. The process of claim 11, wherein the display substrate includes a plurality of independently addressable active devices.

15. The process of claim 14, further comprising the step of forming through holes in the color filters to allow electrical connection of transparent conductive sub-pixel electrodes to the independently addressable active devices.

16. The process of claim 15, wherein the step of forming through holes in the color filters comprises patterning a photoresist on the color filters and etching portions of the color filters left exposed by the patterned photoresist.

17. The process of claim 15, wherein the step of forming through holes in the color filters comprises laser ablating portions of the color filters.

18. A process for making a color display substrate comprising the steps of:

providing an active display substrate having a plurality of independently addressable active devices thereon;
thermally transferring a plurality of color filters to the active substrate, each color filter comprising a colorant in a crosslinkable composition;
inspecting the color filters after the transferring step;
performing a washing step, if necessary, to remove the color filters from the active substrate for reworking of the active substrate; and
crosslinking the color filters after the inspecting step.

19. The process of claim 18, wherein the step of thermally transferring a plurality of color filters comprises:

providing a donor sheet comprising a base layer, a light to heat converter, and a transfer layer comprising a colorant in a crosslinkable composition;
placing the transfer layer proximate to the active substrate; and
selectively irradiating portions of the donor sheet to thermally transfer portions of the transfer layer from the donor sheet to the active substrate.

Patentansprüche

1. Verfahren zum Herstellen einer elektronischen Anzeige umfassend:

eine Lichtquelle;
einen Polarisator, der so angeordnet ist, dass er einen Teil des Lichts von der Lichtquelle durchläßt und polarisiert; und
eine Flüssigkristall-Anzeigentafel, die so angeordnet ist, dass sie durch den Polarisator durchgelassenes Licht nutzt, wobei die Anzeigentafel beinhaltet:

ein unteres Substrat,

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ein oberes Substrat, das von dem unteren Substrat beabstandet ist,
eine bistabile Flüssigkristallschicht, umfassend ein fluoriertes chirales ferroelektrisches Flüssigkristallmaterial, das zwischen dem oberen und dem unteren Substrat angeordnet ist, und
eine mehrfarbige aktive Schicht, die zwischen dem unteren Substrat und der Flüssigkristallschicht angeordnet ist, einschließend eine Mehrzahl unabhängig ansprechbarer aktiver Elemente, die mit transparenten, leitfähigen Subpixelelementen elektrisch verbunden sind, und eine Mehrzahl thermisch übertragener Farbfilter, die einen Farbstoff in einer vernetzten Zusammensetzung beinhalten, wobei jeder Farbfilter mit einem oder mehreren der transparenten, leitfähigen Subpixelelemente ausgerichtet ist;

wobei das Verfahren die Schritte umfasst:

Bereitstellen eines Anzeigensubstrats, umfassend das untere Substrat und die Mehrzahl unabhängig ansprechbarer aktiver Elemente, die mit den transparenten, leitfähigen Subpixelelementen elektrisch verbunden sind;
Thermotransfer einer Mehrzahl Farbfilter auf ausgewählte Abschnitte des Substrats,

wobei jeder Farbfilter einen Farbstoff in einer vernetzbaren Zusammensetzung umfasst;

Untersuchung der Farbfilter nach dem Transferschritt;
Durchführen eines Waschschritts, falls notwendig, um die Farbfilter von dem Substrat zu entfernen, um das aktive Substrat nachzubearbeiten; und
Vernetzen der Farbfilter nach dem Untersuchungsschritt.

2. Verfahren nach Anspruch 1, wobei die elektronische Anzeige weiterhin eine schwarze Matrix umfasst, die auf dem aktiven Substrat angeordnet ist, um Subpixel zu trennen, wobei die schwarze Matrix eine ausreichende optische Dichte, um einen optischen Kontrast zwischen Subpixeln zu schaffen, und einen ausreichenden spezifischen Widerstand, um eine Kreuzkopplung ("crosstalk")zwischen angrenzenden unabhängig ansprechbaren Transistoren im Wesentlichen zu vermeiden, aufweist.

3. Verfahren nach Anspruch 1, wobei die elektronische Anzeige weiterhin eine Mehrzahl Abstandshalter umfasst, die zwischen dem ersten und dem zweiten Substrat angeordnet sind, um einen im Wesentlichen gleichmäßigen Spalt zwischen ihnen zu erhalten.

4. Verfahren nach Anspruch 3, wobei die Abstandshalter selektiv durch Thermotransfer übertragen werden.

5. Verfahren nach Anspruch 1, wobei der Polarisator einen doppelbrechenden reflektierenden Polarisator und einen dichroitischen Polarisator umfasst, der sich zwischen dem reflektierenden Polarisator und dem unteren Substrat befindet.

6. Verfahren zum Herstellen einer elektronischen Anzeige, umfassend:

ein erstes transparentes Substrat mit einer Mehrzahl auf diesem angeordneter, unabhängig ansprechbarer Dünnfilmtransistoren, wobei jeder Transistor elektrisch mit einem zugeordneten transparenten leitfähigen Subpixelelement verbunden ist;
ein zweites transparentes Substrat, das von dem ersten transparenten Substrat beabstandet ist;
eine Flüssigkristallschicht, die zwischen dem ersten Substrat und dem zweiten Substrat angeordnet ist; und
eine Mehrzahl mittels Thermotransfer übertragener Farbfilter, die zwischen dem ersten Substrat und der Flüssigkristallschicht angeordnet sind, wobei die Farbfilter einen Farbstoff in einer vernetzten Zusammensetzung umfassen, wobei jeder Farbfilter mit einem oder mehreren der transparenten leitfähigen Elemente, die den Transistoren zugeordnet sind, ausgerichtet ist;

wobei das Verfahren die Schritte umfasst:

Bereitstellen eines Anzeigesubstrats, umfassend das erste transparente Substrat;
Thermotransfer einer Mehrzahl Farbfilter auf ausgewählte Abschnitte des Substrats,

wobei jeder Farbfilter einen Farbstoff in einer vernetzbaren Zusammensetzung umfasst;

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Untersuchung der Farbfilter nach dem Transferschritt;
Durchführen eines Waschschritts, falls notwendig, um die Farbfilter von dem Substrat zu entfernen, um das aktive Substrat nachzubearbeiten; und
Vernetzen der Farbfilter nach dem Untersuchungsschritt.

7. Verfahren nach Anspruch 6, wobei die elektronische Anzeige weiterhin eine schwarze Matrix umfasst, die auf dem ersten Substrat angeordnet ist, wobei die schwarze Matrix eine ausreichende optische Dichte, um einen optischen Kontrast zwischen Subpixeln zu schaffen, und einen ausreichenden spezifischen Widerstand, um eine Kreuzkopplung zwischen angrenzenden unabhängig ansprechbaren Transistoren im Wesentlichen zu vermeiden, aufweist.

8. Verfahren nach Anspruch 6, wobei die elektronische Anzeige weiterhin eine Mehrzahl Abstandshalter umfasst, die zwischen dem ersten und dem zweiten Substrat angeordnet sind, um einen im Wesentlichen gleichmäßigen Spalt zwischen diesen zu erhalten.

9. Verfahren nach Anspruch 8, wobei die Abstandshalter so angeordnet sind, dass sie eine lichtinduzierte Aktivierung der Transistoren vermeiden.

10. Verfahren nach Anspruch 6, wobei die elektronische Anzeige weiterhin eine Lichtquelle und einen reflektierenden Polarisator umfasst, der so angeordnet ist, dass er zu der Flüssigkristallschicht Licht von der Lichtquelle mit einem ersten Polarisationszustand durchläßt und Licht mit einem zweiten, orthogonalen Polarisationszustand zurück zur Lichtquelle reflektiert.

11. Verfahren zum Herstellen eines Farbanzeigesubstrats, umfassend die Schritte:

Bereitstellen eines aktiven Anzeigesubstrats;
Thermotransfer einer Mehrzahl Farbfilter auf ausgewählte Abschnitte des Substrats,

wobei jeder Farbfilter einen Farbstoff in einer vernetzbaren Zusammensetzung umfasst;

Untersuchung der Farbfilter nach dem Transferschritt;
Durchführen eines Waschschritts, falls notwendig, um die Farbfilter von dem Substrat zu entfernen, um die aktiven Substrate nachzubearbeiten; und
Vernetzen der Farbfilter nach dem Untersuchungsschritt.

12. Verfahren nach Anspruch 11, wobei der Thermotransfer-Schritt von einer Mehrzahl Farbfilter umfasst:

Bereitstellen einer Donorfolie, umfassend eine Basisschicht, einen Licht-Wärme-Wandler und eine Transferschicht, umfassend einen Farbstoff in einer vernetzbaren Zusammensetzung; Platzieren der Transferschicht in der Nähe des Anzeigesubstrats; und
selektives Bestrahlen von Abschnitten der Donorfolie, um Abschnitte der Transferschicht von der Donorfolie auf das Anzeigesubstrat mittels Thermotransfer zu übertragen.

13. Verfahren nach Anspruch 11, weiterhin umfassend den Schritt des Bildens einer schwarzen Matrix auf dem Anzeigesubstrat.

14. Verfahren nach Anspruch 11, wobei das Anzeigesubstrat eine Mehrzahl unabhängig ansprechbarer aktiver Vorrichtungen umfasst.

15. Verfahren nach Anspruch 14, weiterhin umfassend den Schritt des Bildens von durchgängigen Löchern in den Farbfiltern, um eine elektrische Verbindung von transparenten leitfähigen Subpixelelektroden mit den unabhängig ansprechbaren aktiven Vorrichtungen zu ermöglichen.

16. Verfahren nach Anspruch 15, wobei der Schritt des Bildens der durchgängigen Löcher in den Farbfiltern das Erzeugen eines Musters in einem Photoresist auf den Farbfiltern und das Ätzen von Abschnitten der Farbfilter, die von dem gemusterten Photoresist ungeschützt gelassen werden, umfasst.

17. Verfahren nach Anspruch 15, wobei der Schritt des Bildens von durchgängigen Löchern in den Farbfiltern das Durchführen einer Laser-Ablation an Abschnitten der Farbfilter umfasst.

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18. Verfahren zum Herstellen eines Farbanzeigesubstrats, umfassend die Schritte:

Bereitstellen eines aktiven Anzeigesubstrats mit einer Mehrzahl darauf befindlicher unabhängig ansprechbarer aktiver Vorrichtungen;
Thermotransfer einer Mehrzahl Farbfilter auf das aktive Substrat, wobei jeder Farbfilter einen Farbstoff in einer vernetzbaren Zusammensetzung umfasst;
Untersuchung der Farbfilter nach dem Transferschritt;
Durchführen eines Waschschritts, falls notwendig, um die Farbfilter von dem aktiven Substrat zu entfernen, um das aktive Substrat nachzubearbeiten; und
Vernetzen der Farbfilter nach dem Untersuchungsschritt.

19. Verfahren nach Anspruch 18, wobei der Thermotransfer-Schritt einer Mehrzahl Farbfilter umfasst:

Bereitstellen einer Donorfolie, umfassend eine Basisschicht, einen Licht-Wärme-Wandler und eine Transferschicht, umfassend einen Farbstoff in einer vernetzbaren Zusammensetzung;
Platzieren der Transferschicht in der Nähe des aktiven Substrats; und
selektives Bestrahlen von Abschnitten der Donorfolie, um Abschnitte der Transferschicht von der Donorfolie auf das aktive Substrat mittels Thermotransfer zu übertragen.

Revendications

1. Procédé de fabrication d'un dispositif d'affichage électronique comprenant :

une source lumineuse ;
un polariseur disposé pour laisser passer et polariser une partie de la lumière émise par la source lumineuse ; et
un écran d'affichage à cristaux liquides disposé pour utiliser la lumière polarisée que laisse passer le polarisateur, l'écran d'affichage comportant

un substrat inférieur,
un substrat supérieur espacé d'une certaine distance du substrat inférieur,
une couche de cristaux liquides bistables comprenant une substance à cristaux liquides ferroélectriques chiraux fluorés disposée entre les substrats supérieur et inférieur, et
une couche active polychrome disposée entre le substrat inférieur et la couche de cristaux liquides, comportant une pluralité d'éléments actifs à adressage indépendant, connectés électriquement à des éléments conducteurs transparents à sous-pixels et une pluralité de filtres colorés qui sont soumis à un transfert thermique et qui contiennent un colorant dans une composition réticulée, chaque filtre coloré étant aligné avec un ou plusieurs des éléments conducteurs transparents à sous-pixels,

le procédé comprenant les étapes consistant à:

fournir un substrat d'affichage comportant le substrat inférieur et la pluralité d'éléments actifs à adressage indépendant connectés électriquement à des éléments conducteurs transparents à sous-pixels ;
réaliser un transfert thermique de masse d'une pluralité de filtres colorés vers certaines parties du substrat, chaque filtre coloré contenant un colorant dans une composition réticulable ;
examiner les filtres colorés après l'étape de transfert ;
effectuer si nécessaire une étape de lavage pour retirer les filtres du substrat pour retravailler le substrat actif ; et
réticuler les filtres colorés après l'étape d'examen.

2. Procédé selon la revendication 1, dans lequel le dispositif d'affichage électronique comprend une matrice noire disposée sur le substrat actif pour séparer les sous-pixels, la matrice noire ayant une densité optique suffisante pour fournir un contraste optique entre les sous-pixels et une résistivité pour empêcher sensiblement la diaphonie entre des transistors à adressage indépendant.

3. Procédé selon la revendication 1, dans lequel le dispositif d'affichage électronique comprend en outre une pluralité de moyens d'espacement disposés entre les premier et second substrats pour maintenir un espace sensiblement

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uniforme entre eux.

4. Procédé selon la revendication 3, dans lequel les moyens d'espacement font l'objet d'un transfert thermique sélectif de masse.

5. Procédé selon la revendication 1, dans lequel le polariseur comporte un polariseur réfléchissant biréfringent et un polariseur dichroïque intercalé entre le polariseur réfléchissant et le substrat inférieur.

6. Procédé de fabrication d'un dispositif d'affichage électronique comprenant :

un premier substrat transparent sur lequel est disposée une pluralité de transistors à couches minces à adressage indépendant, chaque transistor étant connecté électriquement à un élément conducteur transparent à sous-pixels correspondant ;
un second substrat transparent espacé par rapport au premier substrat transparent ;
une couche de cristaux liquides disposée entre le premier substrat et le second substrat ; et
une pluralité de filtres colorés soumis à un transfert thermique, disposés entre le premier substrat et la couche de cristaux liquides, les filtres colorés contenant un colorant dans une composition réticulée, chaque filtre coloré étant aligné avec un ou plusieurs des éléments conducteurs transparents associés aux transistors; le procédé comprenant les étapes consistant à :

fournir un substrat d'affichage comprenant le premier substrat transparent ;
réaliser un transfert thermique de masse d'une pluralité de filtres colorés vers certaines parties du substrat, chaque filtre coloré contenant un colorant dans une composition réticulable ;
examiner les filtres colorés après l'étape de transfert ;
effectuer si nécessaire une étape de lavage pour retirer les filtres du substrat pour retravailler le substrat actif ; et
réticuler les filtres colorés après l'étape d'examen.

7. Procédé selon la revendication 6, dans lequel le dispositif d'affichage électronique comprend en outre une matrice noire disposée sur le premier substrat, la matrice noire ayant une densité optique suffisante pour fournir un contraste optique entre les sous-pixels et une résistivité pour empêcher sensiblement la diaphonie entre des transistors à adressage indépendant.

8. Procédé selon la revendication 6, dans lequel le dispositif d'affichage électronique comprend en outre une pluralité de moyens d'espacement disposés entre les premier et second substrats pour maintenir un espace sensiblement uniforme entre eux.

9. Procédé selon la revendication 8, dans lequel les moyens d'espacement sont disposés pour empêcher l'activation des transistors par la lumière.

10. Procédé selon la revendication 6, dans lequel le dispositif d'affichage électronique comprend en outre une source lumineuse et un polariseur réfléchissant disposé pour laisser passer vers la couche de cristaux liquides la lumière émise par la source lumineuse ayant un premier état de polarisation et pour réfléchir de la lumière ayant un deuxième état de polarisation orthogonale et la renvoyer vers la source lumineuse.

11. Procédé pour fabriquer un substrat d'affichage couleur, comprenant les étapes consistant à :

fournir un substrat d'affichage actif ;
réaliser un transfert thermique de masse d'une pluralité de filtres colorés vers certaines parties du substrat, chaque filtre coloré contenant un colorant dans une composition réticulable ;
examiner les filtres colorés après l'étape de transfert ;
effectuer si nécessaire une étape de lavage pour retirer les filtres du substrat pour retravailler le substrat actif ; et
réticuler les filtres colorés après l'étape d'examen.

12. Procédé selon la revendication 11, dans lequel l'étape de transfert thermique de masse d'une pluralité de filtres colorés comporte :

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la réalisation d'un feuille donneuse comportant une couche de base, un convertisseur de lumière en chaleur et une couche de transfert contenant un colorant dans une composition réticulable ;
la mise en place de la couche de transfert tout près du substrat d'affichage; et
l'irradiation sélective de parties de la feuille donneuse pour le transfert thermique de parties de la couche de transfert de la feuille donneuse vers le substrat d'affichage.

13. Procédé selon la revendication 11, comprenant en outre l'étape consistant à former une matrice noire sur le substrat d'affichage.

14. Procédé selon la revendication 11, dans lequel le substrat d'affichage comporte une pluralité de dispositifs actifs à adressage indépendant.

15. Procédé selon la revendication 14, comprenant en outre l'étape consistant à former des trous traversants dans les filtres colorés pour permettre la connexion électrique d'éléments conducteurs transparents à sous-pixels aux dispositifs actifs à adressage indépendant.

16. Procédé selon la revendication 15, dans lequel l'étape de formation de trous traversants dans les filtres colorés comporte la formation d'un motif de réserve sur les filtres colorés et l'attaque chimique de parties des filtres colorés laissées découvertes par le motif de réserve.

17. Procédé selon la revendication 15, dans lequel l'étape de formation de trous traversants dans les filtres colorés comporte l'ablation par laser de parties des filtres colorés.

18. Procédé pour fabriquer un substrat d'affichage couleur, comprenant les étapes consistant à :

fournir un substrat d'affichage actif sur lequel est disposée une pluralité de dispositifs actifs à adressage indépendant ;
réaliser un transfert thermique de masse d'une pluralité de filtres colorés vers le substrat actif, chaque filtre coloré contenant un colorant dans une composition réticulable;
examiner les filtres colorés après l'étape de transfert ;
effectuer si nécessaire une étape de lavage pour retirer les filtres du substrat actif pour retravailler le substrat actif ; et
réticuler les filtres colorés après l'étape d'examen.

19. Procédé selon l'étape 18, dans lequel l'étape de transfert thermique d'une pluralité de filtres colorés comprend :

la réalisation d'un feuille donneuse comportant une couche de base, un convertisseur de lumière en chaleur et une couche de transfert contenant un colorant dans une composition réticulable ;
la mise en place de la couche de transfert tout près du substrat d'affichage; et
l'irradiation sélective de parties de la feuille donneuse pour le transfert thermique de parties de la couche de transfert de la feuille donneuse vers le substrat d'affichage.

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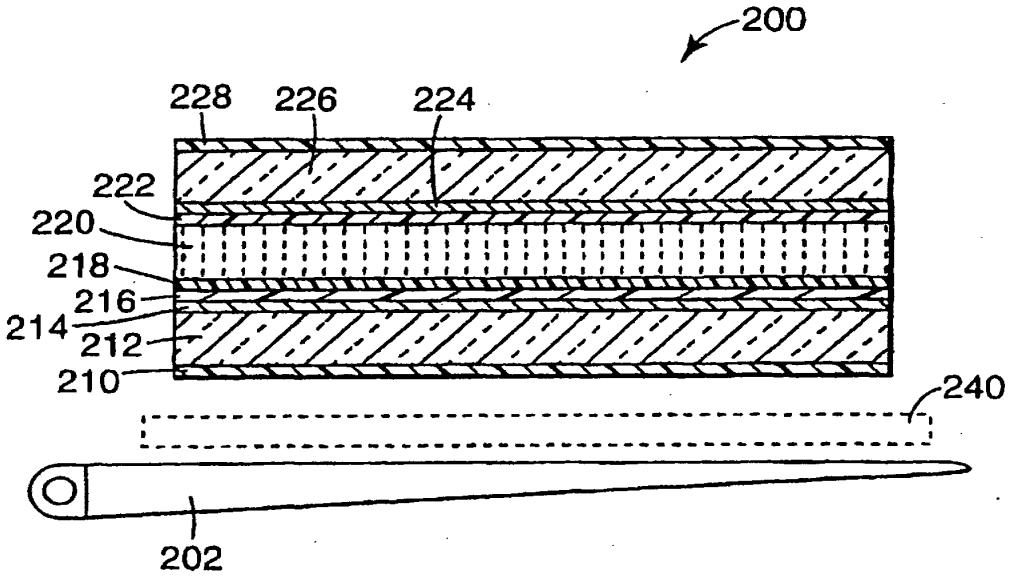


Fig. 1

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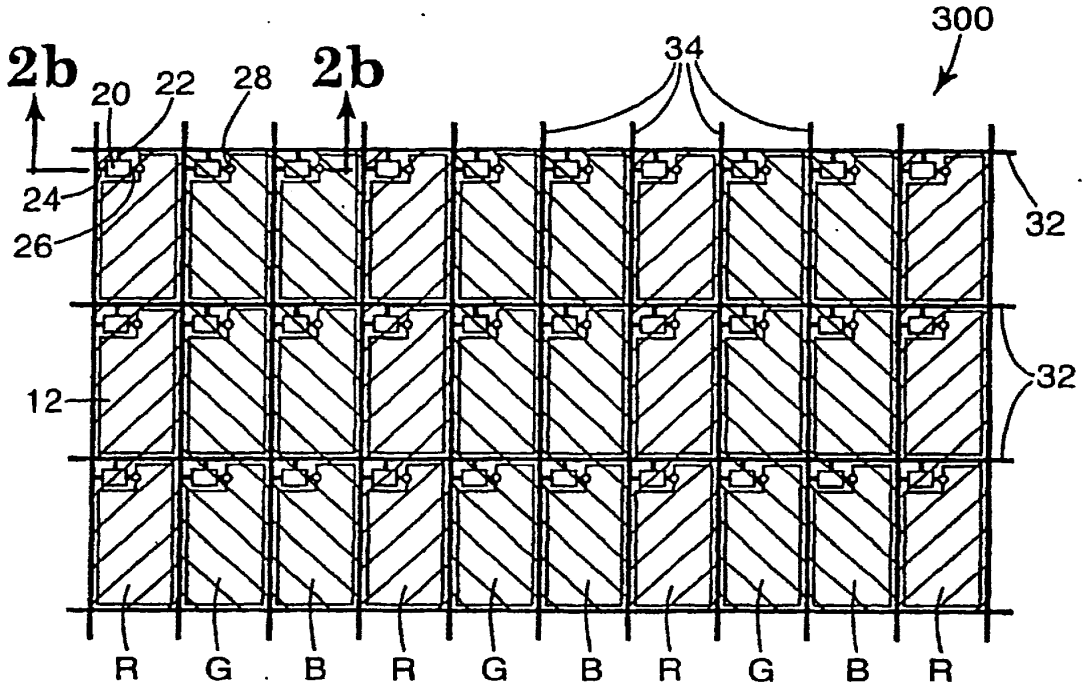


Fig. 2a

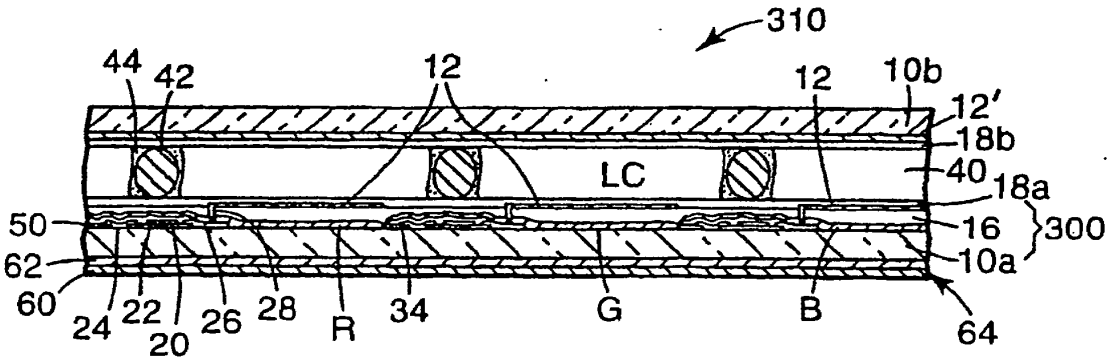


Fig. 2b

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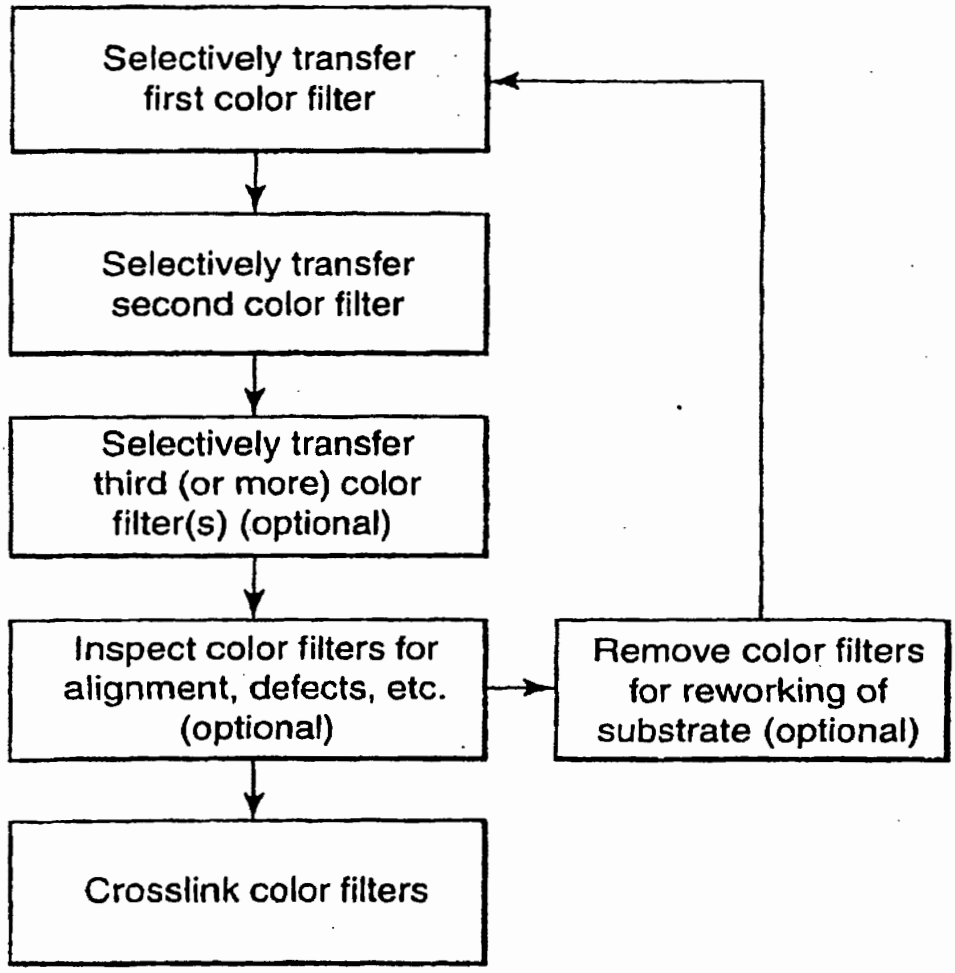


Fig. 3

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/137,163	05/02/2002	Karl Pichler	2002P03156US	1705

TITLE OF INVENTION: ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	06/30/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
LEE, HSIEN MING	2823	438-026000

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(B) RESIDENCE: (CITY and STATE OR COUNTRY): Regensburg, Germany

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SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/137,163	05/02/2002 RULE	438	2823	2002P03156US

APPLICANTS

Karl Pichler, Santa Clara, CA;
Kyle D. Firschknecht, Livermore, CA;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS *********************

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Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
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35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance				
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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7590 07/06/2005

Siemens Corporation
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EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/06/2005

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
10/137,163	05/02/2002	Pichler, et al.	2002P03156US

EXAMINER	
H. LEE	
ART UNIT	PAPER
	070505

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Commissioner for Patents

The IDS submitted on April 20, 2005 was filed after the mailing date of the Notice of Allowance on March 31, 2005. The submission is in compliance with the provisoions of 37 CFR 1.97. Accordingly, the IDS is being considered by the Examiner.

HSIEN-MING LEE
PRIMARY EXAMINER
7/5/2005

Hsien-ming Lee
Primary Examiner
Art Unit: 2823

PTO-90C (Rev.04-03)

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Sheet 1 of 1

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Application Number	10/137,163
Filing Date	05/02/2002
First Named Inventor	Pichler, et al.
Group Art Unit	1775
Examiner Name	Lee, Hsien Ming
Attorney Docket Number	2002P03156US

U.S. PATENT DOCUMENTS

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HL	A	WO	02/05361	A1	McCormick, et al.	01-17-2002		
HL	B	WO	01/81649	A1	Graff, et al.	11-01-2001		
HL	C	EP	1183567	B1	Guehler, et al.	05-07-2003		

Examiner Signature	Hsien Ming Lee	Date Considered	7/5/2005

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Application :	10/137163	**Examiner :**	Lee Ming	**GAU :**	2823
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Patent Number	6,949,389
Issue Date	Sept. 27, 2005
Application Number	10/137,163
Filing Date	May 2, 2002
First Named Inventor	Karl Pichler
Attorney Docket Number	2002P03165US

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☐ Patentee.

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Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☑ Attorney or agent of record. Registration Number 43,351.

Signature [signature]

Typed or Printed Name Anand Sethuraman

Date 12/22/05 Telephone 650-943-7554

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of ____ forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Post Issue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Attorney Docket No.: 2002P03156US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Pichler, et al.

Patent No.: 6,949,389 B2

Issue Date: Sept. 27, 2005

Serial No.: 10/137,163

Filing Date: May 2, 2002

For: ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

Examiner: Hsien-Ming Lee

Group Art Unit: 2823

Certificate
DEC 28 2005
of Correction

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please issue a Certificate of Correction for the above-identified patent to correct the errors listed on the accompanying PTO Form 1050. In the Declaration, the last name of the second named inventor was misspelled. The last name of the second named inventor is spelled Frischknecht not Firschknecht. This error is typographical in nature (or a mistake of minor character) since the inventor correctly spelled his name when signing the Declaration. In addition, the correction does not constitute new matter nor require reexamination.

This request is being made pursuant to 35 U.S.C. § 255 and so the Commissioner is hereby authorized to charge $100.00 per 37 CFR 1.20(a) to Deposit Account No. 19-2179..

The Commissioner is hereby authorized to charge any other fees required to Deposit Account No. 19-2179.

PLEASE MAIL CORRESPONDENCE TO:

Siemens Corporation
Customer No. 28524
Attn: Elsa Keller, Legal Administrator
170 Wood Avenue South
Iselin, NJ 08830

Respectfully submitted,

Thomas George

Thomas George, Reg. No. 45,740
Attorney(s) for Applicant(s)
Telephone: 650-694-5191
Date: Dec 16, 2005

12/27/2005 YPOLITE1 00000015 192179 6949389
01 FC:1811 100.00 DA

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. :6,949,389 B2
DATED :September 27, 2005
INVENTOR(S): Karl Pichler and Kyle D. Frischknecht

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Correct spelling of second named inventor is: Kyle D. Frischknecht.

Mailing Address of Sender:
Siemens Corporation
Intellectual Property Department
1230 Shorebird Way Bldg.4
Mountain View, CA 94043

Patent No. 6,949,389 B2

US006949389B2

(12) **United States Patent**
Pichler et al.

(10) **Patent No.: US 6,949,389 B2**
(45) **Date of Patent: Sep. 27, 2005**

TG 8083

(54) **ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES**

(75) Inventors: **Karl Pichler**, Santa Clara, CA (US); **Kyle D. ~~Firschknecht~~ FRISCHKNECHT**, Livermore, CA (US)

(73) Assignee: **Osram Opto Semiconductors GmbH**, Regensburg (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/137,163**

(22) Filed: **May 2, 2002**

(65) **Prior Publication Data**

US 2003/0205845 A1 Nov. 6, 2003

(51) **Int. Cl.**[7] **H01L 21/00**; H01L 21/425

(52) **U.S. Cl.** **438/26**; 438/28; 438/30; 438/48; 438/55; 438/531; 438/627

(58) **Field of Search** 438/26, 28, 30, 438/48, 55, 531, 624, 627, 641; 257/53, 21, 59.414, 431, 701, 760

(56) **References Cited**

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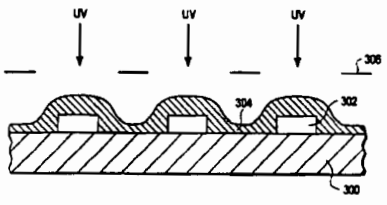
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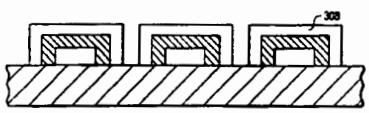
Primary Examiner—Hsien-Ming Lee
(74) *Attorney, Agent, or Firm*—Thomas George

(57) **ABSTRACT**

An embodiment of an encapsulated OLED device is described. This embodiment of the encapsulated OLED device is formed by: fabricating multiple OLED devices on a substrate; depositing at least one planarization layer on the OLED devices; hardening the at least one planarization layer in a patterned manner such that the hardened region substantially covers the OLED device; removing areas of the at least one planarization layer that are not hardened; and selectively depositing at least one barrier layer over the hardened region.

53 Claims, 8 Drawing Sheets





OIPE IAP19
DEC 28 2005
PATENT & TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

IMPROVED ENCAPSULATION FOR ORGANIC LIGHT EMITTING DIODES DEVICES

the specification of which (check one)
___is attached hereto.
_X_ was filed on **May 2, 2002** as Application Serial No. **10/137,163**
and was amended on _____ (if applicable)

List of Inventors: Karl Pichler and Kyle D. Firschknecht

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Codes, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			Priority claimed	
(Number)	(Country)	(Day/month/year filed)	Yes	No
(Number)	(Country)	(Day/month/year filed)	Yes	No

application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)
(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application listed below:

(Application Serial No.)	(Filing date)	(Status)

Power of Attorney: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Adel A. Ahmed, Reg. No. 29,606; I. Marc Asperas, Reg. No. 37,274; Stanton C. Braden, Reg. No. 32,556; Alexander J. Burke, Reg. No. 40,425; Dexter K. Chin, Reg. No. 38,842; David D. Chung, Reg. No. 38,409; Joseph S. Codispoti, Reg. No. 31,819; Thomas George, Reg. No. 45,740; Henry J. Groth, Reg. No. 39,696; Mark H. Jay, Reg. No. 27,507; Brian K. Johnson, Reg. No. 46,808; Stuart P. Kaler, Reg. No. 35,913; Rosa S. Kim, Reg. No. 39,728; Jenny G. Ko, Reg. No. 44,190; Peter A. Luccarelli Jr., Reg. No. 29,750; James M. Markarian, Reg. No. 31,277; Jeffrey P. Morris, Reg. No. 25,307; Pasquale Musacchio, Reg. No. 36,876; John Musone, Reg. No. 44,961; Frank J. Nuzzi, Reg. No. 42,944; Donald B. Paschburg, Reg. No. 33,753; Laura M. Slenzak, Reg. No. 35,363; Daniel J. Staudt, Reg. No. 34,733; Erik C. Swanson, Reg. No. 40,194; Heather S. Vance, Reg. No. 39,033; and Michael J. Wallace, Reg. No. 44,486.

Send correspondence to:

Siemens Corporation
Intellectual Property Department
186 Wood Avenue South
Iselin, N.J. 08830

Direct telephone calls to:

Elsa Keller
Legal Administrator (908) 321-3026

I hereby declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full name of first joint inventor:	Karl Pichler
Inventor's signature:	
Date:	July 22 2002
Residence:	Santa Clara, CA
Citizenship:	Austria
Post Office Address:	444 Saratoga Avenue, #15C, Santa Clara, CA 95050

Full name of second joint inventor:	Kyle D. Firschknecht
Inventor's signature:	Kyle Firschknecht
Date:	July 22, 2002
Residence:	Livermore, CA
Citizenship:	USA
Post Office Address:	566 Shelley Street, Livermore, CA 94550

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CERTIFICATE OF CORRECTION

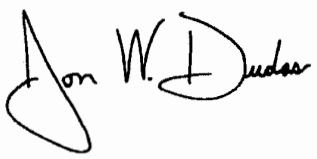
PATENT NO. : 6,949,389 B2
DATED : September 27, 2005
INVENTOR(S) : Karl Pichler and Kyle D. Frischknecht

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [75], Inventors, second inventor should read -- **Kyle D. Frischknecht** --.

Signed and Sealed this

Seventh Day of February, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office

AO 120 (Rev. 08/10)

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2:23cv495	10/19/2023	Eastern District of Texas Marshall Division

PLAINTIFF	DEFENDANT
Pictiva Displays International LTD.	Samsung Electronics Co., Ltd Samsung Electronics America, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,949,389	9/27/2005	Pictiva Displays International LTD.
2	8,314,547	11/20/2012	Pictiva Displays International LTD.
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:23cv495	10/19/2023	Eastern District of Texas

PLAINTIFF	DEFENDANT
Pictiva Displays International Ltd.	Samsung Electronics Co., Ltd., Samsung Electronics America Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,949,389	9/27/2005	Pictiva Displays International Ltd.
2	8,314,547	11/20/2012	Pictiva Displays International Ltd.
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