

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.
Petitioner

v.

UNIVERSITY OF ROCHESTER
Patent Owner

Inter Partes Review No.
IPR2024-01225

Patent No. 7,089,443 B2
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**DECLARATION OF R. JACOB BAKER, P.E., PH.D.
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,089,443 B2**

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I, R. Jacob Baker, declare the following:

I. INTRODUCTION

1. I have been retained by Lenovo (United States) Inc. (“Lenovo” or “Petitioner”) as an independent technical expert consultant in connection with the above-captioned *Inter Partes* Review of U.S. Patent No. 7,089,443 B2 (“the ’443 Patent”) (Ex. 1001). Although I am being compensated at my normal consulting rate of \$765 per hour for the time I spend on this matter, no part of my compensation is dependent on the outcome of this proceeding or any other related proceeding. I have no other interest in this proceeding.

2. Based on a review of the front page of the ’443 Patent, I understand that the ’443 Patent is assigned to the University of Rochester (“University” or “Patent Owner”). In addition, I understand that the ’443 Patent issued from U.S. Application No. 10/762,550, filed on January 23, 2004, which claims the benefit of priority to U.S. Application No. 60/441,759 (“the ’759 application”), a provisional application that was filed on January 23, 2003. Ex. 1001, p. 1, item (21).¹

¹ In this Declaration, I refer to the written portions of a patent document by making reference to the column:line number or paragraph number of the exhibit. For all other documents or portions of patent documents, I refer to the page number of the exhibit.

3. I am familiar with the technology at issue as of January 23, 2003, i.e., the filing date of the '759 application to which the '443 Patent claims priority, as explained immediately above.²

4. I have been asked to consider how a person having ordinary skill in the art (“person having ordinary skill in the art” or “POSITA”) would have understood the claims of the '443 Patent and the applied references. More specifically, I have been asked to provide my technical opinion on concepts discussed in the '443 Patent and the applied references, as well as my technical opinion on how these concepts relate to the '443 Patent’s claim limitations in the context of its written description.

5. In reaching the opinions stated herein, I have considered the '443 Patent and the various other documents listed in Section III below in the context of my own education, training, research, knowledge, and personal and professional experiences. My opinions are provided below.

A. Background and Qualifications

6. My qualifications generally are set forth in my Curriculum Vitae, which is attached as Appendix A. Appendix A also includes a list of the publications I have

² I have been informed by counsel that, while the '759 application may or may not provide support for the claims of the '443 Patent, I am to provide my analysis based on the assumption that there is support.

authored and a list of the other cases in which I have testified during the last four years.

7. I have been working as an Engineer since 1985 and I have been teaching Electrical and Computer Engineering courses since 1991. I am currently a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (“UNLV”).

8. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

9. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 V and 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled “Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices,” published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

1. *Industry Experience*

10. I have done technical and expert witness consulting for over 200 companies and their subsidiaries since I started working as an engineer in 1985.

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From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada test site. During this time, I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments, including high-speed cable and fiber-optic receiver/transmitters, phase locked loops (PLLs), frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel's cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

11. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working in industry. I hold a patent, Patent No. 5,874,830, in the area of power supply design, titled, "Adaptively biased voltage regulator and operating method," which was issued on February 23, 1999. I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

12. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change

Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. (“MTI”) in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system’s performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via inter-process communications (IPC) with the memory controller (MC). This included interfacing with processors having multiple cores that operate at various independent clock frequencies using, for

example, DDR protocols. The operation of the computer memory systems used multiple clock domains both in the processors and in the memory. My experience included using internally operated asynchronous clocks to allow, for example, for more time for sense amps to conduct the sensing. The slower clocks were generated with, in some systems, phase-locked loops. I also developed delay locked loops in DDR memory to adjust for slack and ensure critical timing delays were adjusted for changes in temperature voltage and process shifts. I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and 2010. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

13. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB,

firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics. For example, a part of my research at Boise State, for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density 3D packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while I did consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc. in the late 1990s. The main processor and GPU ran at independent clock frequencies which required the design of a phase-locked loop on the GPU. Using multiple clock domains and asynchronous communications employing FIFOs having flags identifying full/empty were used to improve performance such as lowering power and improving computation speed. I did similar work for Amkor also in the late 1990s. From 1994 to 1996, I worked on the design of displays at Micron Display and MTI in Boise, Idaho. This work was at a time when cathode ray tubes (CRTs) were still the dominant type of display. Flat panel displays were being developed with the hope of replacing CRTs in the consumer market. I worked on flat panel displays which resulted in 5 patents: U.S. Patent Nos. 5,598,156, 5,638,085, 5,818,365, 5,894,293, and 5,909,201. I worked on the design of the pixels, both active and passive, as well as the supporting

electronics for processing video signals. I was involved with the evaluation of display technologies including liquid crystal displays (LCDs), light-emitting diodes, plasma displays, and organic light emitting diode (OLED) displays; the display technologies that were looking to displace CRTs in the consumer market. I was also involved with the packaging of the displays including the vacuum sealing and deposition of the phosphors for light wavelength conversion. I also taught display design as a topic in my courses and did display design consulting again in industry for Cirque in 2013.

14. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (Light Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years focused on the digitization of IQ channels using delta-sigma modulation. The knowledge and experience gained from this effort are reflected in my textbook *CMOS Mixed-Signal Circuit Design*.

2. Academic Experience

15. I was an adjunct faculty member in the Electrical Engineering departments of UNLV and University of Nevada, Reno (UNR) from 1991-1993.

From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University (“BSU”), where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate programs in Electrical and Computer Engineering including, in 2006, the university’s second Ph.D. degree. In 2012, I rejoined the faculty at UNLV. Over the course of my career as a professor, I have advised more than 100 masters and doctoral students.

16. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President’s Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the “Father of Silicon Valley”). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator’s contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I have been back at UNLV.

17. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and

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Simulation (Baker, R.J., Wiley-IEEE, ISBN: 9781119481515 (4th ed., 2019)) and CMOS Mixed-Signal Circuit Design (Baker, R.J., Wiley-IEEE, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I co-authored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 9780470184752 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley - IEEE, ISBN: 9780780334168 (1998)). I contributed as an editor and co-author on several other electrical and computer engineering books.

3. Other Relevant Experience

18. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries, and given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication, and packaging.

19. I currently serve, or have served, as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS

2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-present). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

20. In addition to the above, I am an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

B. Materials Reviewed

21. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my knowledge and experience in designing, developing, and researching wireless communication networks and systems, I reviewed the following documents:

- '443 Patent (Ex. 1001)
- Prosecution History of the '443 Patent (Ex. 1003)
- U.S. Patent Publication No. 2003/0030326 A1 to Shenai ("*Shenai*") published on February 13, 2003 (Ex. 1004)

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- International Publication No. WO 01/53921 A1 to Halepete (“*Halepete*”) issued on July 26, 2001 (Ex. 1005)
- U.S. Patent Publication No. 2002/0169990 A1 to Sherburne (“*Sherburne*”) published on November 14, 2002 (Ex. 1006)
- U.S. Patent No. 5,473,756 to Traylor (“*Traylor*”) issued on December 5, 1995 (Ex. 1007)
- U.S. Patent No. 6,047,248 to Georgiou (“*Georgiou*”) issued on April 4, 2000 (Ex. 1008)
- International Publication No. WO 01/33352 A1 to Kranich (“*Kranich*”) published on May 10, 2001 (Ex. 1009)
- Webpage for Datamath Calculator Museum - archived by WayBackMachine on February 26, 2001 (“*Datamath*”) (Ex. 1010)
- Stanly Mazor, The History of the Microcomputer –Invention and Evolution (1995) (“*Mazor*”) (Ex. 1011)
- William M. Johnson, Super-Scalar Processor Design, June 1989 (“*Johnson*”) (Ex. 1012)
- Exalibur, Excalibur Arm-Based Hardware Reference Manual, January 2001 (“*Excalibur*”) (Ex. 1013)
- Texas Instruments, TMS320C64x Technical Overview, January 2001 (“*TMS*”) (Ex. 1014)
- Kenneth C. Yeager, The MIPS R100 Superscalar Microprocessor (1996) (“*Yeager*”) (Ex. 1015)
- Texas Instruments, FIFO Architecture, Functions, and Applications, November 1999 (“*FIFO*”) (Ex. 1016)
- Eric Tune et al., Dynamic Prediction of Critical Path Instructions (2001) (“*Tune*”) (Ex. 1017)
- U.S. Patent No. 6,289,465 B1 to Kuermerle (“*Kuermerle*”) issued on September 11, 2001 (Ex. 1018)

- Anand Lal Shimpi, POWERNOW!, September 12, 2000 (“*PowerNow!*”) (Ex. 1019)
- Anand Lal Shimpi, POWERNOW! Operating Modes, September 12, 2000 (“*POWERNOW! Operating Modes*”) (Ex. 1020)
- Bruce R. Childers et al., Adapting Processor Supply Volatage to Instruction-Level Parallelism, December 2001 (“*Childers*”) (Ex. 1021)
- Globally Asynchronous, Locally Synchronous Systems (“*GALS*”) (Ex. 1022)
- U.S. Patent No. 6,141,762 to Nicol (“*Nicol*”) issued on October 31, 2000 (Ex. 1023)
- Actel Corporation, 3200DX Dual-Port Random Access Memory (RAM), September 1997 (Ex. 1026)
- Barr Group, Types of Memory in Embedded Systems, May 1, 2001 (Ex. 1027)
- Wavecrest corporation, Understanding Jitter, 2001 (Ex. 1028)
- U.S. Application No. 60/441,759 (“the ’759 application”) (Ex. 1029)
- U.S. Patent No. 7,739,537 (“the ’537 Patent”) (Ex. 1030)

II. LEGAL STANDARDS FOR PATENTABILITY

22. I am not an attorney and I offer no opinions on the law itself. My understanding of the relevant legal principles in this section is based on information provided to me by counsel which I have applied in performing my analysis in this matter.

A. Anticipation

23. I have been informed by counsel that under 35 U.S.C. § 102, for a claim to be invalid as “anticipated,” every limitation of the claim must be found in a single prior art reference, either expressly or inherently.

B. Obviousness

24. I have been informed by counsel that a patent claim may be found invalid under 35 U.S.C. § 103(a) if the subject matter of the claim as a whole would have been obvious to a hypothetical person of ordinary skill in the art in view of a prior art reference or in view of a combination of references at the time of the alleged invention. I have been informed that obviousness is determined from the perspective of a person of ordinary skill in the art and that the challenged claims should be read from the point of view of such a person at the time the alleged invention was made. I have also been informed that a person of ordinary skill in the art is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent in suit, and would thus have been familiar with each of the references cited herein, as well as the background knowledge in the art discussed in Section III(A), and the full range of teachings they contain.

25. I have been informed of two criteria for determining whether a prior art reference is analogous and therefore qualifies as prior art: (1) whether the art is from the same field of endeavor as the challenged claims, regardless of the problem

addressed, and (2) if the reference is not within the field of endeavor of the challenged claims, whether the reference still is reasonably pertinent to the particular problem which the challenged claims purport to address. I have additionally been informed that the field of endeavor of a patent is not limited to a specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference may be reasonably pertinent if, even though it may be in a different field, it is one which logically would have commended itself to a patentee's attention in considering his problem because of the subject matter with which it deals.

26. I have further been informed that whether an alleged invention would have been obvious should be analyzed in view of the scope and content of the prior art, the differences (if any exist) between the prior art references and the challenged claims, and the level of ordinary skill in the pertinent art involved. I have additionally been informed that a prior art reference should be viewed as a whole when performing the above analysis.

27. I have been informed that in considering whether a claimed combination would have been obvious, I may assess whether there were apparent reasons to combine elements in the prior art in the manner claimed in view of interrelated teachings of one or more prior art references, the impact of demands known to the community or present in the market place, and/or the general

knowledge possessed by a person of ordinary skill in the art at the time of alleged invention. I have been informed that other principles may be relevant in evaluating whether an alleged invention would have been obvious, and that these principles may include the following:

- A combination of prior art elements according to known methods is likely to be obvious when it does nothing more than yield predictable results;
- When a known device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or in a different one, so that if a person of ordinary skill in the art is able to implement a predictable variation, then that variation is likely obvious;
- If a known technique has been used to improve a device, method, or product, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same predictable way, using the technique is obvious unless the actual implementation of the technique is beyond his or her skill;
- An explicit or implicit teaching, suggestion, or motivation in the prior art to combine the prior art references to form the claimed combination may demonstrate obviousness (but a teaching, suggestion, or motivation to combine is not a requirement for proving obviousness);
- Market demand, rather than scientific literature, can drive design trends and may show obviousness;
- In determining whether the subject matter of a patent claim would have been obvious, neither the motivation nor the purpose of the named inventor controls;
- The subject matter of a patent may be proved obvious by demonstrating that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;

- Any need or problem known in the field and addressed by the prior art can provide a reason for a person of ordinary skill in the art at the time of the invention to combine the elements in the manner claimed;
- “Common sense” indicates that known items and methods may have obvious uses beyond their primary purposes, and in many cases, a person of ordinary skill in the art would be able to fit the teachings of multiple prior art references together similar to the pieces of a puzzle;
- A person of ordinary skill in the art is also a person of ordinary creativity, and is not an automaton;
- A patent claim may be proved obvious by demonstrating that the claimed combination of elements was “obvious to try,” especially when there exists a design need or market pressure to solve the problem and there are a limited number of identified, predictable solutions such that person of ordinary skill in the art would have had good reason to pursue the known options within his or her technical grasp; and

28. I have further been informed that, in making a determination as to whether or not the alleged invention would have been obvious to a person of ordinary skill in the art, the Board might consider the presence of additional objective or secondary factors, such as: commercial success of products which practice the purported invention; a long-felt but unsolved need; teaching away; unexpected results; copying; and industry praise. These factors are typically referred to as “secondary considerations” or “objective indicia” of non-obviousness. I have been informed, however, that for such objective indicia or secondary evidence to be relevant to the obviousness analysis, there must be a causal relationship (known as a “nexus”) between the challenged claim and the objective indicia evidence and that this nexus must be based on what is claimed and novel in the claim, and not

something in the prior art. I have also been informed by counsel that even when objective indicia evidence is present, these secondary considerations may be unable to overcome sufficiently strong primary evidence showing obviousness (*e.g.*, motivation to combine with predictable results).

C. Level of Ordinary Skill in the Art

29. My opinions are based on my understanding of the perspective of a POSITA on January 23, 2003, *i.e.*, the filing date of the '759 application to which the '443 Patent purports to claim priority. *See* Ex. 1029. In determining the level of ordinary skill, I have been asked to consider, for example, the types of problems encountered in the field, prior solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the education level of active workers in the field.

30. In my opinion, based on the materials and information I have reviewed and based on my experience in the technical areas relevant to the '443 Patent, a POSITA at the time of the alleged invention of the '443 Patent would have had a bachelor's degree in electrical engineering, computer engineering, or the equivalent, and two to three years of experience designing computing circuits and systems. More practical experience could offset the aforementioned education while a higher level of education could offset a lesser amount of practical experience.

31. Under these definitions, I am qualified as a person of ordinary skill in the art during the relevant time frame stated above (i.e., January 2003). I provide my analysis of the '443 Patent, the prior art, and my opinions in this Declaration from the perspective of a POSITA, as I have defined it above, during the relevant time frame stated above, where appropriate.

D. Claim Construction

32. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a POSITA, during the relevant time frame, which I was asked to assume was in January of 2003. In considering the meaning of the claims, I also understand that one must consider the claim language, specification, prosecution history, and the knowledge of a POSITA at the relevant time. I have followed these principles in my analysis. I believe all terms in the challenged claims should be given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the purported invention.

III. OPINION

A. Background of the Technology

33. In this section, I discuss the state of the art relevant to the subject matter of the '443 Patent, as would have been known, understood, and appreciated by a POSITA at the time of the alleged invention of the '443 Patent.

1. *Microprocessors and Memory*

34. Microprocessors have been commercially available since 1972 when Intel released their 8008 (and 4004) microprocessor. Ex. 1010 at p. 1. Microprocessors were immediately used as architecture and instruction sets could easily be defined. *Id.* More importantly, microprocessors are small, programmable computers, which provide infinite possibilities and solutions to existing problems. *Id.* For example, the 4004 microprocessor replaced “what would otherwise have been six customized chips, usable by only one customer.” *Id.* In essence, the single-chip microprocessor was a device “that revolutionized electronics by putting all the functions of a computer on one piece of silicon.” *Id.*

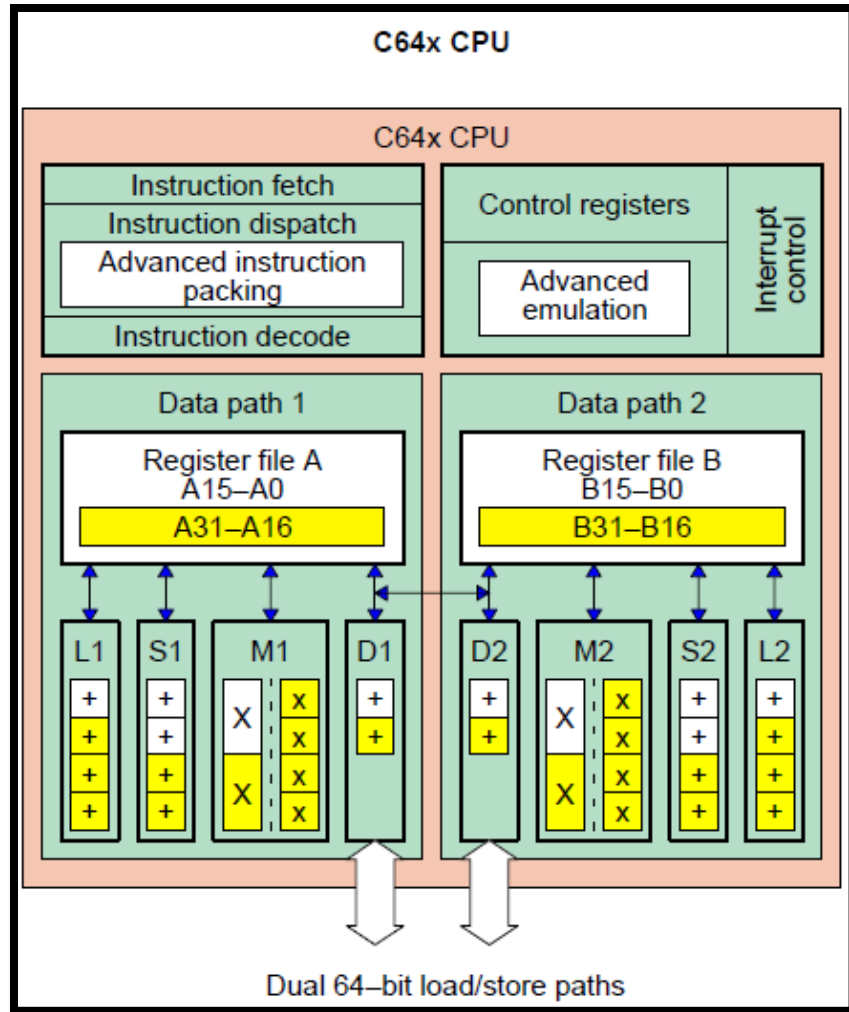
35. Around 1980, local connections on the microprocessor chips were being improved. Ex. 1011 at p. 6. Previously, metal was used for “global connections such as power, ground, clocks, and major busses,” while local connections “were made using poorer quality, higher resistance, lines of poly-silicon or diffusion.” *Id.*

36. Superscalar processors, processors that are “capable of sustaining an instruction-execution rate of more than one instruction per clock cycle,” quickly became prevalent throughout the 1980s and early 1990s. Ex. 1012 at p. 1. Superscalar processors achieve this by performing instructions in parallel over multiple functional units. *Id.* For example, microprocessors could have “[m]ultiple and separate clock domains controlled by software-programmable phased-lock

loops (PLLs)[.]” Ex. 1013 at p. 8. Moreover, the average number of cycles required for an application could be reduced by having multiple processor units. Ex. 1012 at p. 1.

37. Such PLLs were implemented using an external reference clock that did not need “to be synchronous to any of the system operation.” Ex. 1013 at p. 42. It was known that “[c]lock signals are typically susceptible to Duty Cycle Distortion (DCD) and Periodic Jitter (PJ)” where such jitter “is typically caused by cross talk, EMI, simultaneous switching outputs (SSO), device function dependency (pattern [dependent] jitter) and other regularly occurring interference signals. Cross talk occurs when a victim line (a trace on a circuit board or 2 adjacent wires in a cable) is affected by the magnetic field from a driver line.” Ex. 1028 at p. 1.

38. Introduced in 2000, the TMS320C64x improved the already existing TMS320 line of digital signal processors produced by Texas Instruments. Ex. 1014 at pp.8-9. The C64x CPU included eight functional units to perform faster operations. *Id.* A diagram of the C64x CPU (reproduced below) shows the functional units, each tasked with performing different functions. The .M units can perform bit multiples, the .D units can access words and double words, the .L units can perform byte shifts, and the .S units can perform shifts. *Id.* at p. 26.



Reproduced from TMS

Id. at p. 10. “The eight functional units in the [] data paths can be divided into two groups of four; each functional unit in one data path is almost identical to the corresponding unit in the other data path.” *Id.* at p. 20.

39. Microprocessor components were known to receive inputs such as clocks or voltages over inputs such as input pins that can be used “as an input to the device.” Ex. 1013 at p. 175. For example, a “clock input pin” may be “2.5/3.3-V [low voltage Transistor-Transistor Logic] LVTTL.” *Id.* at p. 42. As another example,

“[i]f the selected input mode requires use of a voltage reference, the appropriate VREF pins are enabled.” *Id.* at p. 138. *Childers* describes using multiple input supply voltages “on chip to run different circuit paths at varying speeds. By bringing multiple voltages on chip, we expect that a processor will be able to quickly change its voltage level.” Ex. 1021 at p. 3.

40. Such microprocessors included advanced memory configuration support implemented using, for example, internal single-port SRAM, internal dual-port SRAM, external SDRAM, double-data rate memory, and/or flash memory. Ex. 1013 at p. 7. The supported memory further included dual-port Random Access Memory (RAM) such as dual-port Static Random Access Memory (SRAM) which offered “independent read and write ports.” Ex. 1026 at p. 1 (titled “3200DX Dual-Port Random Access Memory (RAM)” which references its 3200DX product as “dual-port SRAM” which “offers dual-port SRAM capable of supporting a system speed of 100 MHz”.) SRAM was used to provide for a system’s memory needs such as “transferring data in high-speed bursts[,]” accessing a system bus “with minimum interruption[,]” and for simultaneous read and write operations. *Id.* at p. 1, 2. It was also known that the “RAM family includes two important memory devices: static RAM (SRAM) and dynamic RAM (DRAM)” where SRAM and DRAM are types of “volatile memory[.]” Ex. 1027 at p. 2, 5.

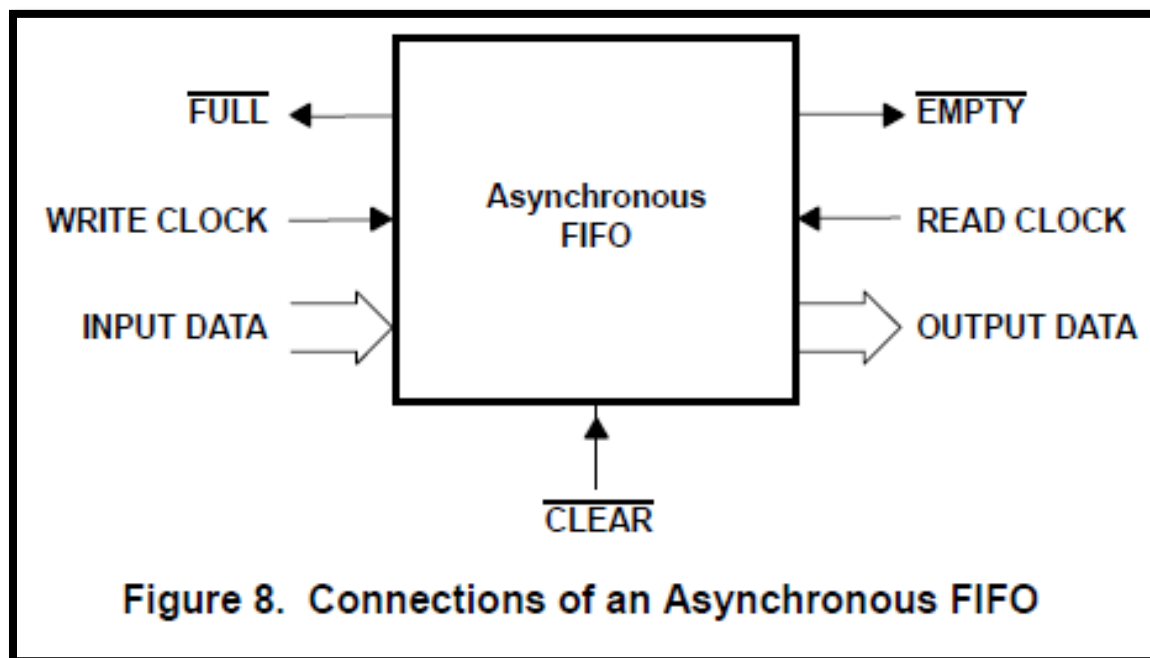
2. *Buffer and Queue Structures for Microprocessors*

41. First-in first-out (FIFO) operations and corresponding elements have been included in microprocessors as a way to provide a buffer for processing elements. FIFOs are queues that may hold instructions between communicating processors, processing units, etc., until the instructions are ready to be written or read. Since out-of-order superscalar processors are complex, microprocessors were designed to include an instruction queue. Ex. 1015 at p. 1. For example, the R10000 microprocessor, when receiving an instruction pipeline, “writes the renamed instructions into the queues and reads the busy-bit table to determine if the operands are initially busy. Instructions wait in the queues until all their operands are ready.” *Id.* at p. 2. In other words, queues in microprocessors act similar to that of a controller for the conveyor belt in an assembly line. If the next step in the line is not ready to receive the product, the controller can be used to stop the conveyor belt and thus stop the assembly line until the next step is ready. Thus, queues hold instructions until the functional unit that is receiving the instructions is ready to receive them.

42. Because of this, functional units can have separate instruction queues. *Id.* (“The integer and floating-point sections have separate instruction queues[.]”) For example, instruction queues can include an integer queue to allocate an entry to each integer instruction as it is decoded, an address queue to allocate an entry when the processor decodes each load or store instruction, and a floating-point queue to allocate integer instructions that are not immediate values. *Id.* at pp. 6-8. In general,

when memory is needed to be written and read, a FIFO is often used to facilitate this process.

43. A FIFO includes a FULL signal when limited space is available such as when “there is space ... for only one data word[.]” Ex. 1016 at p. 12. The FULL signal is queried to see if there is space. If the FULL signal is not given, then free space is indicated. *Id.* at p. 11. Similarly, the EMPTY status output “has to be queried before reading, because data can be read out only if it is stored in the FIFO.” *Id.* An example FIFO is shown below in Figure 8 of *FIFO*.



Reproduced from *FIFO*

Id. at p. 10.

44. FIFOs can be used for processors since processors can be faster than the peripherals connected to them. *Id.* at p. 24. “FIFOs can be used so that the

processing speed of a processor need not be reduced when it exchanges data with a peripheral. If the peripheral is sometimes faster than the processor, a FIFO can again be used to resolve the problem.” *Id.* Moreover, a FIFO can buffer input data and then use an interrupt, such as a FULL flag, to indicate the processor needs to read the data. *Id.*

3. *Critical Execution, Slack, and Dynamic Voltage/Frequency Scaling*

45. Critical execution and slack are concepts related to determining the time in which functional units or instruction pipelines will have their dependencies completed. The critical execution path is the path which takes the longest to complete. This is considered “critical” because the path will determine the maximum frequency that the system can use. *See* Ex. 1017 at p. 1 (“The particular dependences that constrain execution speed constitute the critical path of execution.”). Slack refers to the “dead time” between when a pipeline is completed and when the critical path is completed. In other words, slack is the time in which a functional unit is left idling while still powered due to another pipeline. *Tune* describes several techniques to dynamically predict the critical path instructions.

46. “This paper describes Critical Path Prediction for dynamically identifying instructions likely to be on the critical path, allowing various processor optimizations to take advantage of this information.” *Id.* It is important to know which instructions are critical as this can allow the processor to “improve

performance by giving those instructions preference any time the processor needs to arbitrate between instructions.” *Id.* As an example, a processor with an architecture capable of reducing the length of a dependency chain would target the critical dependency chain. *Id.* Heuristics can be applied to identify critical path instructions. *Id.* at p. 1, 2.

47. In some microprocessors, time-critical execution units, such as units executing complex instructions, will have more power gated to them than execution units that are not time-critical, such as units executing simple instructions. Ex. 1018 at 1, item (57). In other words, “individual execution units are provided selectable power to increase processing speed in critical units while reducing power in less critical units without delaying completion of processing in the critical units.” *Id.* at 2:16-22.

48. The instructions of some execution units may be “deemed non-critical (and, consequently, powered at a lower Vdd).” *Id.* at 4:30-31. *Kuemerle* shows an example of execution timing without variable Vdd, as seen in Table 1 below, and an example of execution timing with variable VDD, as seen in Table 2 below. *Id.* at 40-65.

TABLE 1	
Execution Timing Without Variable Vdd	
Mult Pipe:	 aaaaaaaaaaaaaaaaaaaaaaaaaaaaaa
Add Pipe:	 bbbbbccecc dddddd

Reproduced from *Kuemerle*

TABLE 2	
Execution Timing With Variable Vdd	
Mult Pipe:	 aaaaaaaaaaaaaaaaaaaaaaaaaaaaaa
Add Pipe:	 bbbbbbcccccccccccccccc dddddd

Reproduced from *Kuemerle*

Id. at 4:40-58.

49. With respect to Table 1, operation d is held out due to its dependencies. When implementing variable Vdd such that operations b and c can be “powered down (use less power, and consequently take longer to execute),” the instructions can complete in “exactly the same amount of time” with significantly less power consumption as seen in Table 2. *Id.*

50. AMD introduced PowerNow! which allowed a CPU to “dynamically adjust its operating frequency according to the needs of the tasks that the CPU is running.” Ex. 1019 at p. 1. PowerNow! was introduced in the late 1990s to “more

intelligently manage the amount of power being used by the CPU depending on the type of task [being ran].” *Id.* Instead of simply switching between two presets of power consumption, PowerNow! was able to dynamically switch the power and/or frequency provided, depending on the task being performed. *Id.* “Instead of constantly running a CPU at its maximum frequency, PowerNow! allows the CPU to dynamically adjust its operating frequency according to the needs of the tasks that the CPU is running.” *Id.* As an example, PowerNow! may instruct the CPU to run at a high clock speed when launching an application but subsequently instruct the CPU to reduce the clock speed when idle after opening the application. *Id.*

51. PowerNow! labeled this dynamically changing power consumption as “Automatic Mode” and provided it as an option to consumers. Ex. 1020 at p. 1. “In Automatic Mode, PowerNow! can adjust the clock frequency and voltage of the processor according to the demands of the applications being run while optimizing for battery life.” *Id.* Thus, the CPU usage is monitored to balance performance and battery life. *Id.*

52. PowerNow! was one of several techniques to adjust supply voltage and frequency at run-time to save energy, another of which is described in *Childers*. See Ex. 1021 at p. 1 (“This paper describes a technique for adjusting supply voltage and frequency at run-time to save energy. Our technique monitors a program’s instruction-level parallelism (ILP) and adjusts processor voltage and speed in

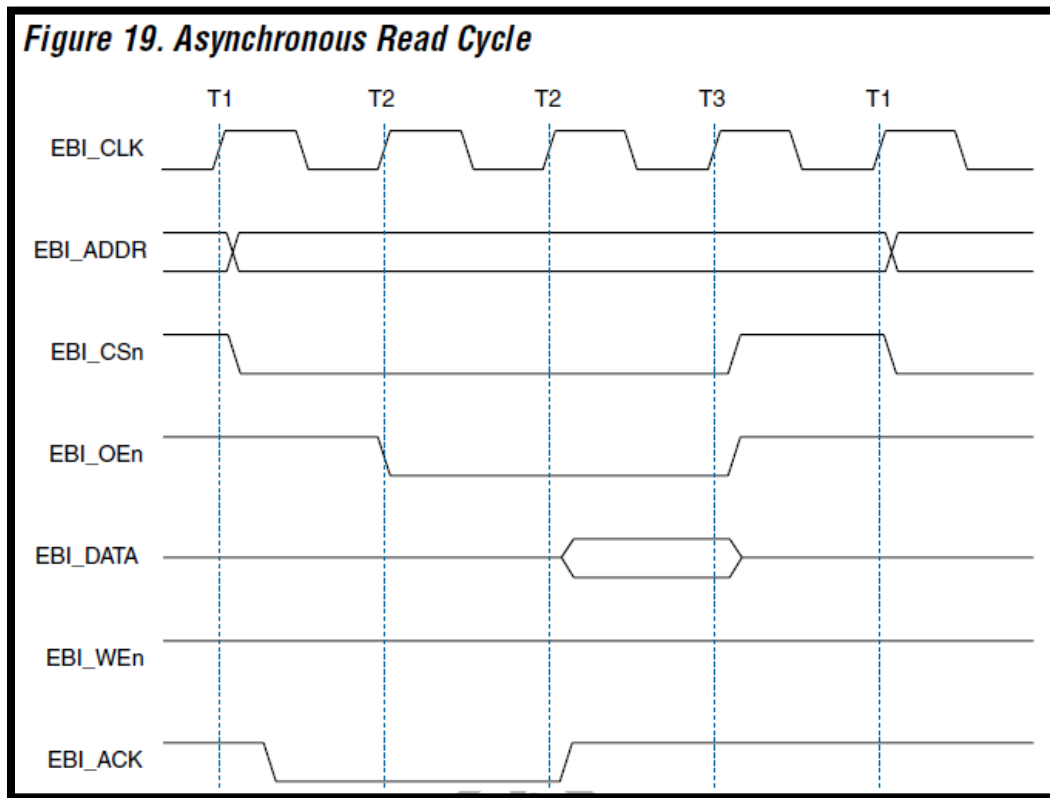
response to the amount of observed ILP.”). *Childers* explains that energy savings are implemented by calculating a frequency and voltage adjustment based on the expenditure of a processor based on determining the processing needs of a processor calculated in Million Instructions Per Second (MIPS). *Id.* at p. 3 (“[t]he processor measures ILP over some specified interval of time in terms of a MIPS rate. If the MIPS rate changes appreciably either up or down, the processor adjusts its supply voltage accordingly.” “Using this MIPS rate, a new frequency (and, hence, voltage level) is calculated.” *Id.* Changing processor supply voltage in response to ILP can conserve power and energy. *Id.* at p. 1.

4. *Asynchronous and Synchronous Operations*

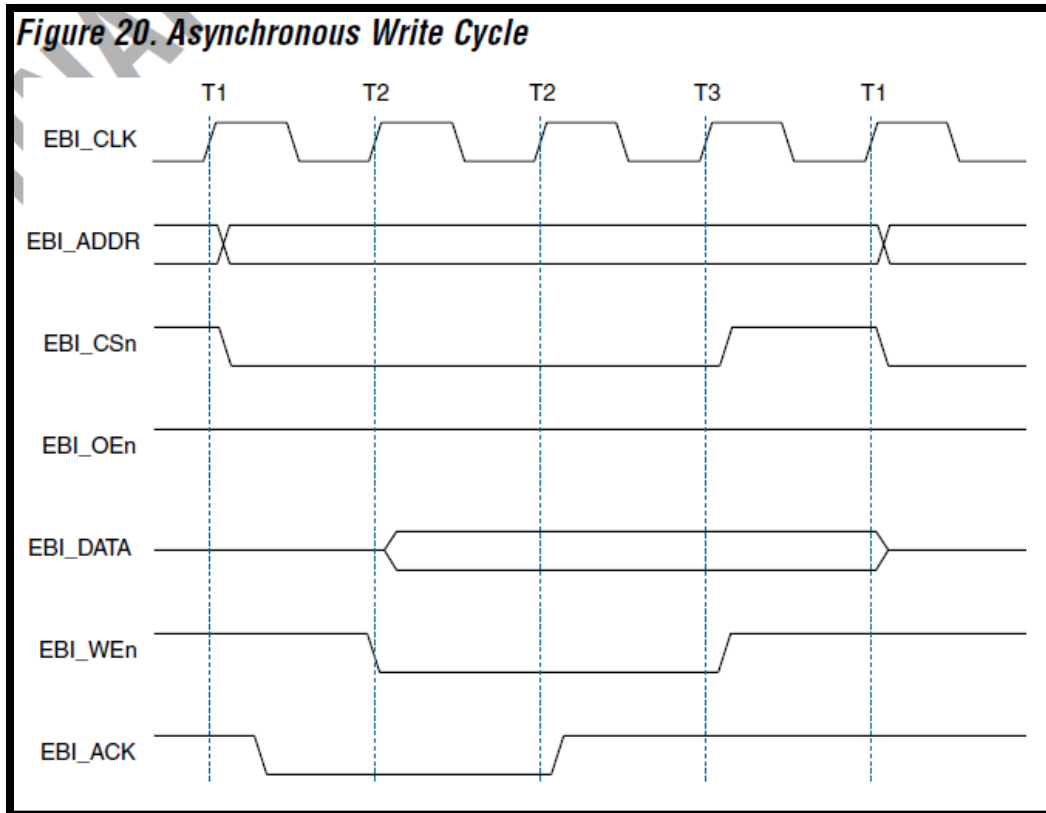
53. Superscalar microprocessors, or other microprocessors that utilize multiple functional units to perform parallel processing, often find solutions to problems that occur due to the functional units running at different operating frequencies and becoming asynchronous (e.g., intercommunication can be challenging between functional units running at different clock frequencies). For example, the memory ports are “synchronous to the separate PLD clock domains that drive them; however, the embedded processor domain and PLD domain can be asynchronous, to allow optimized clock frequencies for each domain.” Ex. 1013 at p. 13. “Resynchronization across the domains is handled by the AHB bridges within the stripe.” *Id.* Some microprocessors, like the ARM-based embedded processor,

came equipped with a synchronous mode and an asynchronous mode. *Id.* at p. 21.

An asynchronous read cycle can be seen in Figure 19 of *Excalibur* below and an asynchronous write cycle can be seen in Figure 20 of *Excalibur* below:



Reproduced from *Excalibur*



Reproduced from *Excalibur*

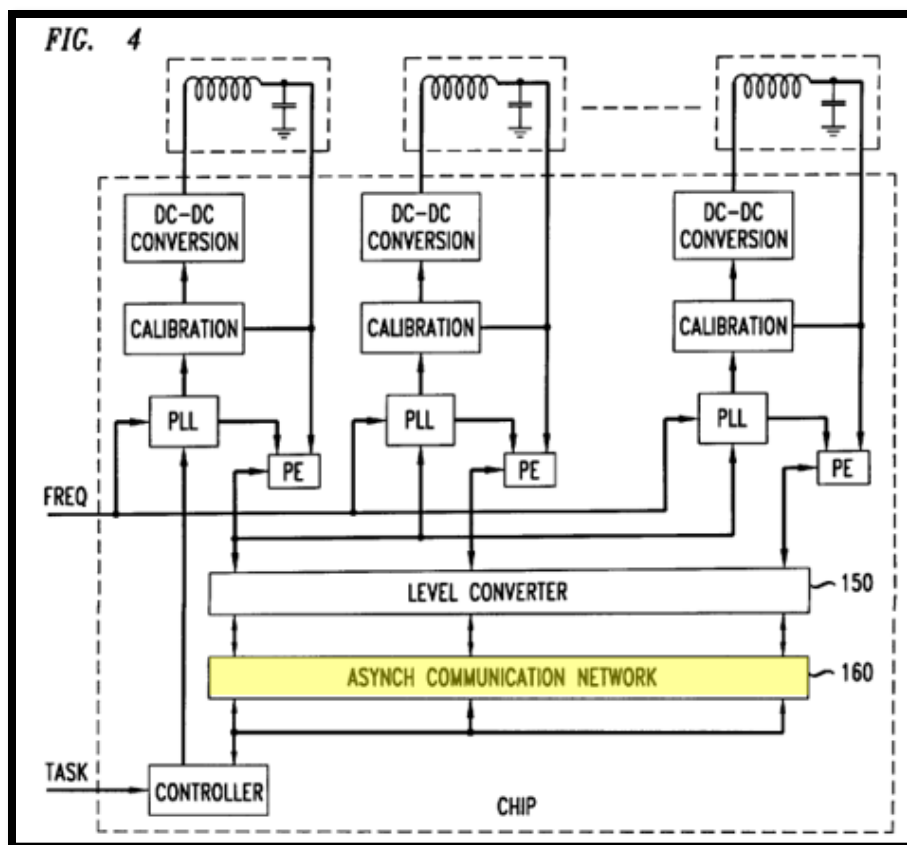
Id. at p. 73.

54. As discussed in the '443 Patent, globally asynchronous, locally synchronous (GALS) systems were becoming popular as architects realized the advantages they provided. Globally synchronous systems can cause clock skew (e.g., the delay between the clock input and the reception of the input by different functional units) and unnecessary power consumption as discussed above. Ex. 1022 at p. 1. Accordingly, GALS systems have “a locally generated clock for every module.” *Id.* “It can be seen how this reduces the complexity of clock distribution since the clock need only be locally distributed.” *Id.* Since the functional units cannot

be synchronized if they use different clocks, an “asynchronous protocol [is used] to communicate between them.” *Id.*

55. *Nicol* also describes a system that uses a plurality of clocks. The system determines the required completion time and divides the collection of task “as evenly as possible (in terms of needed processing time)[.]” Ex. 1023 at 3:66-4:1. The system subsequently determines which processing element (PE) will become the critical path PE. That is, the system determines which PE has the tasks that will require the longest time to perform, and adjusts the clock frequency of that PE to assist in performing the tasks. *Id.* at 4:1-4. *Nicol* acknowledges the fact that asynchronous PEs may cause issues with inter-communication between PEs. For example, “if the frequencies at which the individual PEs operate differ from one another and from other elements within the system where the multiprocessor chip is employed, ... a synchronization schema must be implemented when there is a need to communicate data between PEs (or with other system elements) that operate at different frequencies. *Id.* at 6:14-21.

56. “To effect such synchronization, each PE within the FIG. 4 arrangement is connection [sic] to an arrangement comprising elements 150 and 160.” *Id.* at 6:29-31.



Reproduced from *Nicol*³

Id. at p. 3, annotated. *Nicol* explains that the network 160 “resolves the issue of different clock domains.” *Id.* at 6:29-31.

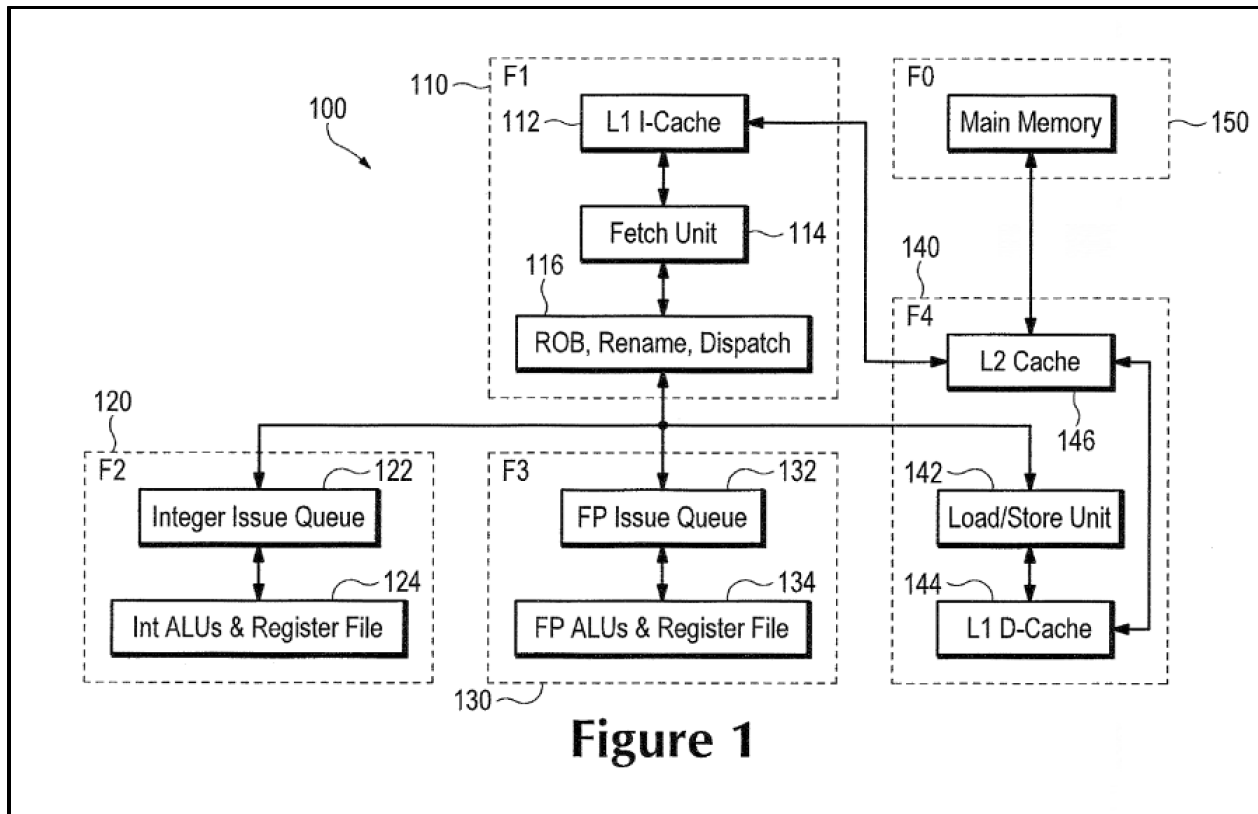
B. Overview of the '443 Patent

57. The '443 patent describes systems and methods for microprocessors with multiple clock domains. Ex. 1001 at 1:19-21. Specifically, the '443 patent describes a multiple clock domain (“MCD”) microarchitecture that uses a globally-

³ All annotations included in this document are added by me unless indicated otherwise.

asynchronous, locally-synchronous clocking style. *Id.* at p. 1, item (57). The '443 patent asserts that the techniques described are useful in increasing microprocessor performance by providing an approach that “allows for aggressive future frequency increases, maintains a synchronous design methodology, and exploits the trend towards making functional blocks more autonomous.” *Id.* at 4:9-12. The '443 patent uses existing queue structures in a superscalar processor core to isolate the different clock domains in a way that minimizes the need for inter-domain synchronization.” *Id.* at 5:1-4. Figure 1 of the '443 patent⁴ below illustrates an MCD processor block diagram.

⁴ I note that Figure 1 of the '443 patent is illegible as it includes dark and/or greyscale blocks with overlaid dark text. Accordingly, the Figure 1 I provide is from the '537 Patent, which claims priority to U.S. Application No. 10/762,550, which matured as the '443 patent. This Figure 1 was filed in a replacement sheet during prosecution the '537 Patent's underlying application and includes the same content as Figure 1 of the '443 patent.

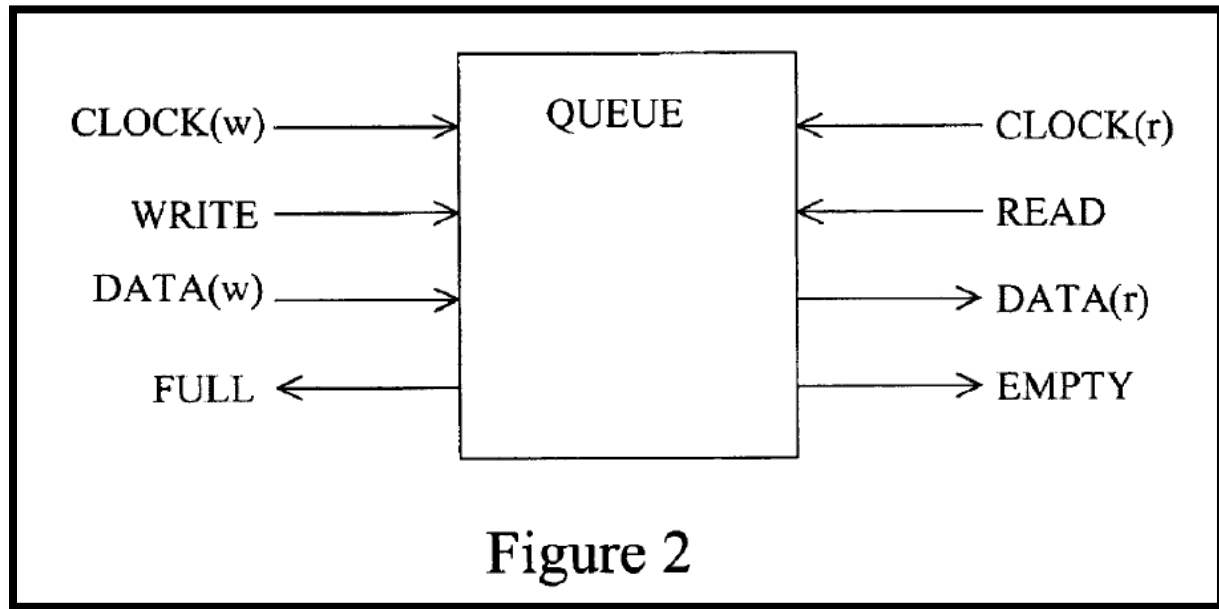


Reproduced from the '537 Patent

Ex. 1030 at p. 3.

58. Figure 1 includes four domains, those being front end 110, integer issue/execute 120 (which includes integer issue queue 122), floating point issue/execute 130 (which includes floating point issue queue 132), and load/store issue/execute 140 (which includes load/store queue within load/store unit 142). Ex. 1001 at 6:1-8, 6:46. The '443 patent explains that, while the performance impact of implementing separate load/store and integer domains was a concern, “the additional synchronization penalty did not significantly degrade performance.” *Id.* at 6:11-15. However, the '443 patent states the main disadvantage of an MCD processor is

“performance overhead due to inter-domain synchronization.” *Id.* at 6:27-28. The queues included in the block diagram of FIG. 1 are chosen as inter-domain synchronization points to help hide the synchronization cost “whenever the queue is neither full nor empty.” *Id.* at 6:45-53.



Reproduced from the '443 Patent

Id. at p. 2.

59. Figure 2 above shows a general queue structure that is used for inter-domain communication. *Id.* at 6:54-55. “The assertion of the Full flag indicates to the producer that it can no longer write to the queue until the flag is deasserted ($\overline{\text{Full}}$), while the Empty flag when asserted indicates that there is no valid data for the consumer to read from the queue. The consumer waits until Empty is deasserted before reading again.” *Id.* at 6:55-60.

60. Instead of using a full handshake protocol, which would require the producer/consumer to check the Full/Empty flag after every operation, the '443 patent assumes the "Full and Empty flags are generated far enough in advance such that writes and reads can occur every clock cycle without over- or underflowing the queue." *Id.* at 6:66-7:2. The '443 patent describes the worst-case situation for an MCD design occurs "when the producer is operating at the maximum frequency (max_freq) and the consumer at the minimum frequency (min_req)[,]" while an additional complication occurs "due to the need to compare queue head and tail pointers from different clock domains in order to generate the Full and Empty flags." *Id.* at 7:18-24.

61. "Even with completely independent clocks for each interface, the queue structure is able to operate at full speed for both reading and writing under certain conditions. This concurrency requires a dual-ported SRAM structure where simultaneous read and write cycles are allowed to different SRAM cells." *Id.* at 7:29-34. Due to the nature of the queue structure, when the queue is not full the producer can write data on every rising edge of Clock_w and when the queue is not empty the consumer can read on every rising edge of Clock_r. *Id.* at 7:36-41. The '443 patent describes a simulated processor using a "simulation testbed [] based on the SimpleScalar toolset with the Wattch power estimation extensions." *Id.* at 8:27-28. The simulation assumed, for dynamic voltage and frequency scaling configurations,

32 frequency points spanning a linear range from 1 GHz down to 250 MHz with a corresponding voltage spanning a linear range from 1.2 V down to 0.65 V. *Id.* at 9:25-29.

62. As previously explained, a disadvantage of MCDs is rooted in the fact data in one domain is needed in another which can incur synchronization costs. In order to accurately model the potential synchronization costs, the simulation accounts “for the fact that the clocks driving each domain are independent by modeling independent jitter, the variation in the clock, on a cycle-by-cycle basis[,]” which includes an external Phase Lock Loop jitter on top of the internal Phase Lock Loop. *Id.* at 10:30-37. A purported advantage of the MCD design is that it greatly simplifies the global clock distribution network, “requiring only the distribution of the externally generated clock to the local Phase Lock Loop (PLL) in each domain.” *Id.* at 4:25-28.

63. Additionally, an off-line tool is used that “analyzes a trace collected during a full-speed run of an application in an attempt to determine the minimum frequencies and voltages that could have been used by various domains during various parts of the run without significantly increasing execution time.” *Id.* at 10:4-9. Trace information is used to construct a dependence directed acyclic graph (“DDAG”), a representation of dependencies among events/programs in the simulation, for each 50K cycle interval. *Id.* at 11:12-15.

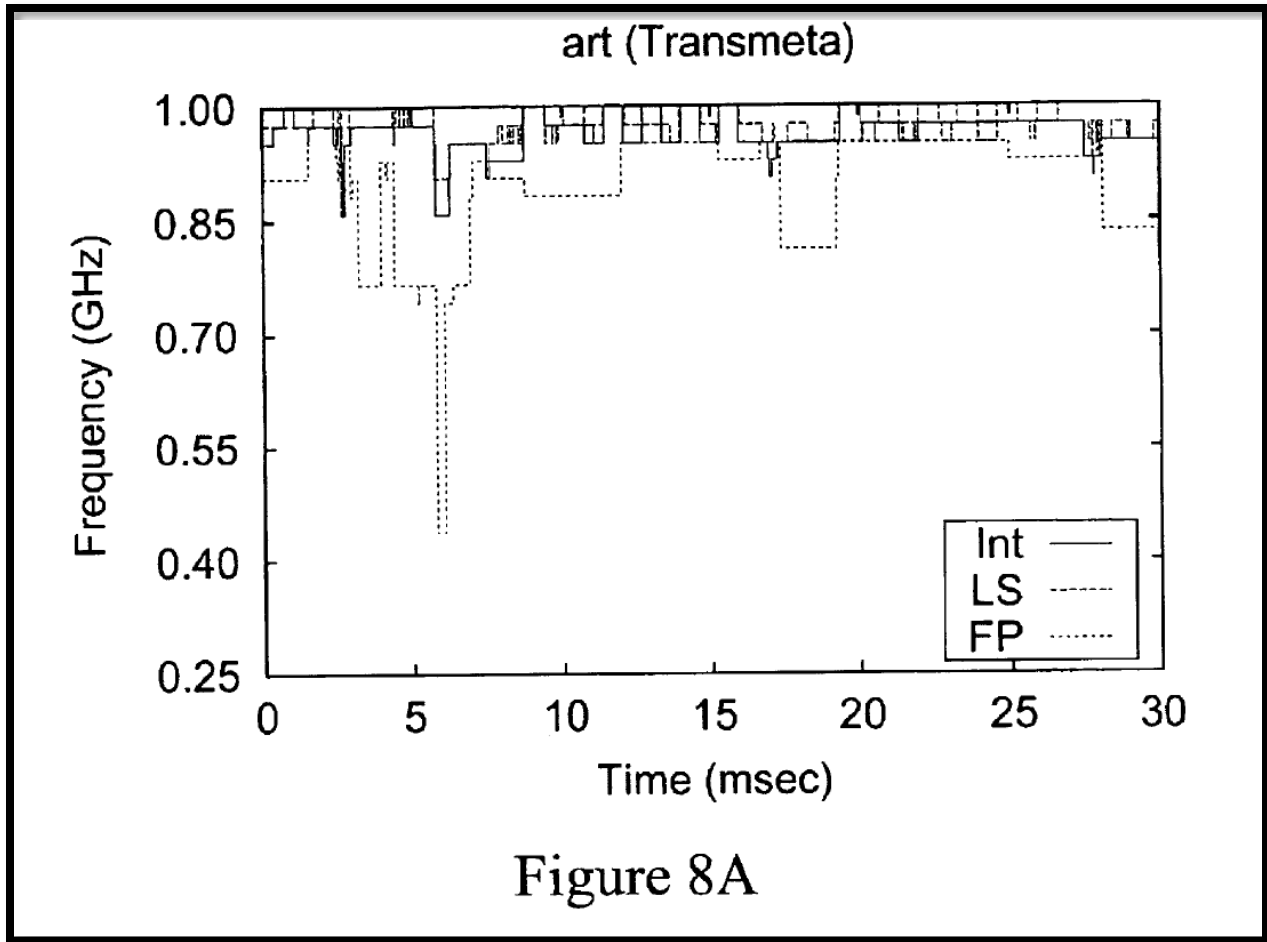
64. The microprocessor's execution flow represented by the DDAG may include an event with multiple incoming dependencies with different overall speeds of execution. *Id.* at 11:25-32. Because of this, one arc, the path that has the slowest speed of execution, will become the critical path while the other arcs, which execute faster than the critical path, will include slack that indicates "the previous operation completed earlier than necessary." *Id.* When all outgoing arcs of an event have slack, the microprocessor can "save energy by performing the event at a lower frequency and voltage." *Id.* The off-line analysis tool includes a clustering phase that recognizes "frequencies cannot change on an instantaneous, instruction-by-instruction basis[,]" and allows "for a certain amount of performance degradation." *Id.* at 12:20-23.

65. "When it is done performing mergers, the clustering algorithm calculates the times at which reconfiguration must begin in order to reach target frequencies and voltages at target times." *Id.* at 12:65-13:1. The algorithm avoids impossible reconfigurations, i.e., reconfigurations that a large swing in frequency would take longer than the available interval. *Id.* at 13:1-4. The algorithm then writes a log file to specify times at which the application could request changes in the frequencies and voltages of various domains. *Id.* at 13:7-11.

66. The '443 patent compares performance, energy, and energy-delay product between the MCD microprocessor and a conventional single clock domain

system. More specifically, the energy savings of the MCD system is compared to conventional voltage and frequency scaling of the same level of performance degradation. *Id.* at 13:36-40. The benefits of MCDs are modeled via the global configuration models by using the baseline configuration with the addition of dynamic scaling of its single voltage and frequency. *Id.* at 13:27-30.

67. FIGs. 8A through 9B of the '443 patent allegedly illustrate “the value of using different frequencies in different clock domains: by controlling these frequencies independently we can maintain the required frequency in domains that are critical to performance, while aggressively scaling those domains that are less performance-critical.” *Id.* at 15:41-46. The '443 patent states the contribution to the field is meant to “demonstrate that a microprocessor with multiple clock domains provides the opportunity to reduce power consumption on a variety of different applications without a significant performance impact by reducing frequency and voltage in domains that do not contribute significantly to the critical path of the current application phase.” *Id.* at 16:8-14. Figure 8A reproduced below shows frequency changes for art generated by the off-line algorithm for the dynamic 1% configuration for Transmeta. *Id.* at 5:43-44.



Reproduced from the '443 Patent

Id. at p. 6.

C. Overview of the '443 Patent's File History

68. The '443 patent was filed as Application No. 10/762,550 ("550 application") on January 23, 2004 and claims priority to Provisional Application No. 60/441,759, filed on January 23, 2003. The '550 application was initially filed with three claims, but a preliminary amendment was filed to cancel the original three claims and added 12 new claims. Ex. 1003 at p. 98 and pp. 40-42.

69. In a first Office Action dated May 19, 2005, all pending claims were allowed and a Notice of Allowance was provided. *Id.* at pp. 24-29. The Notice of Allowance stated the “cited prior art describe systems that change the voltage and frequency of components in data processing systems [but] ... does not describe the domains in a microprocessor and does not describe dynamically controlling the clock frequency and voltage in each domain independently of the clock frequencies and voltages in each of the other domains.” *Id.* at p 28. Additionally, the Notice of Allowance stated that the prior art “does not describe a plurality of domains in a microprocessor or using their system in a microprocessor having a plurality of domains.” *Id.* A Certificate of Correction was issued on June 14, 2011. *Id.* at pp. 4-6. The Certificate of Correction amended claims 1, 10, and 11. *Id.* at p. 5.

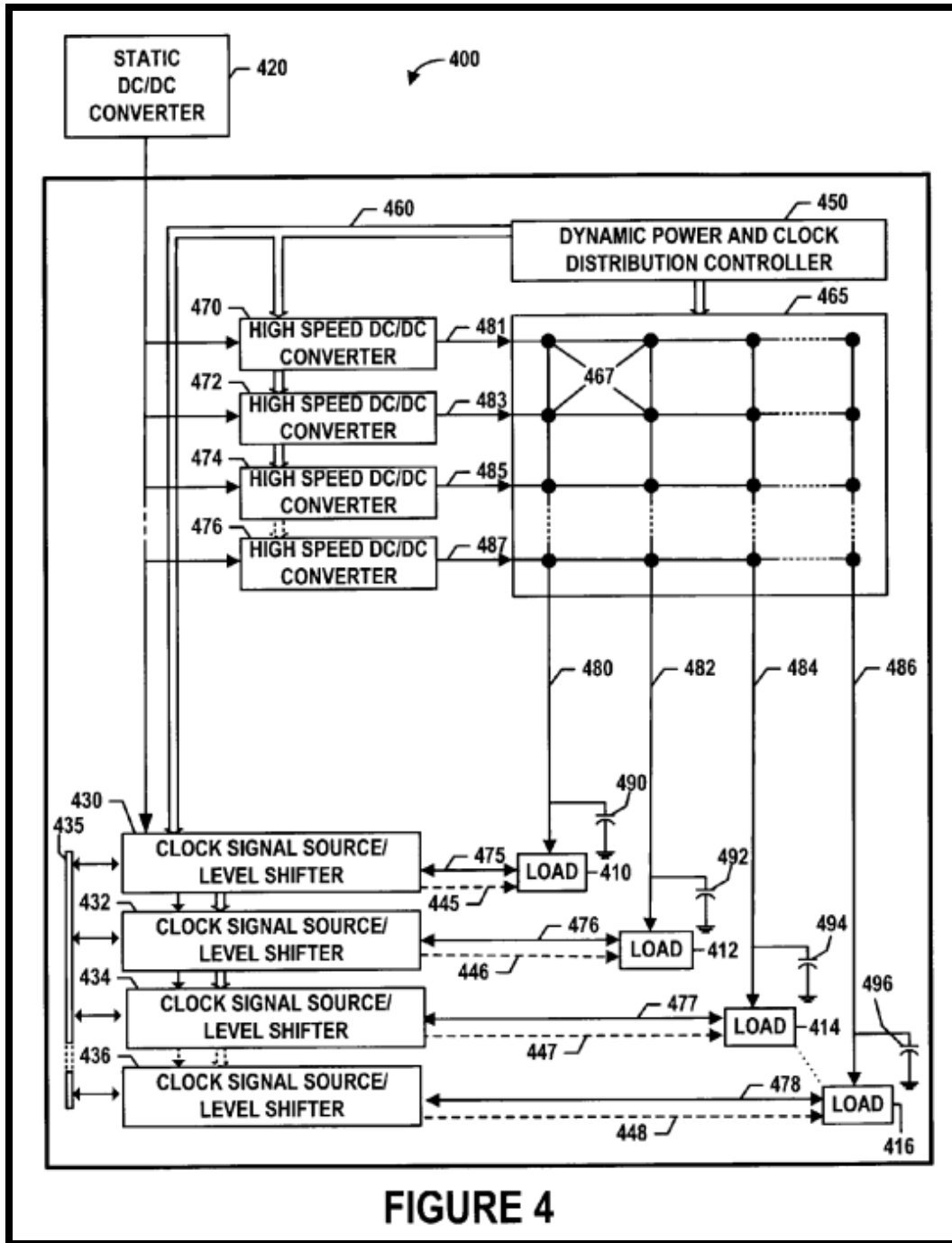
D. Overview of the Prior Art References

1. *Shenai*

70. U.S. Patent Publication No. 2003/0030326 to Shenai et al. (“*Shenai*”) is a patent application related to the architecture of microprocessors which was filed on August 12, 2002, and published on February 13, 2003. Thus, *Shenai* was filed before the ’443 Patent’s earliest priority date of January 23, 2003.

71. *Shenai* discloses a “power distribution management apparatus for supplying power to two or more loads includes a power and clock distribution controller capable of determining voltage, current and clock signal frequency targets

for the loads.” Ex. 1004 at p. 1, item (57). The power distribution management apparatus includes multiple power sources and multiple clock signal sources coupled to the loads to selectively provide target voltages and target frequencies to each load respectively. *Id.* The architecture of the system is shown in Figure 4.



Reproduced from *Shenai*

Id. at p. 5.

72. The circuit 400 is used to balance power consumption and performance for loads 410, 412, 414, and 416. *Id.* at [0025]. The loads can be “individual components, functional blocks of a single component or independent systems,” or “components or subsystems of a microprocessor or microcontroller such as cache memory, register files, arithmetic logic units (ALU), integer units, instruction pipeline circuitry, hardware multipliers, floating point circuits, non-volatile memory units, or circuitry clusters[.]” *Id.*

73. Controller 450 uses clock/shifters 430, 432, 434, and 436 to generate target frequencies to respective loads, and uses DC/DC converters 470, 472, 474, and 476 to generate target voltages to respective loads. *Id.* at [0035] and [0037]. The clock/shifters are “coupled with loads 410-416 so as to provide clock signals via clock signal buses 445, 446, 447 and 448 to the loads at the target frequencies, which may be determined by controller 450[.]” *Id.* at [0035]. Similarly, controller 450 selectively couples “DC/DC converters 470-476 with loads 410-416 via connection network 465's nodes 467 and voltage supply lines 480, 481, 482, 483, 484, 485, 486 and 487.” *Id.* at [0037].

74. Because “certain processing activities of software running on a microprocessor may utilize various subsystems more heavily,” the controller 450 allows each load to receive variable voltage and frequency values depending on the needs of the specific load. *Id.* at [0030]. “By sensing high levels of activity of certain

strategically identified nodes, the requirements for those subsystems may be identified as requiring higher (or lower) clocking frequency, and hence higher (or lower) operating voltages.” *Id.*

75. The controller 450 determines “voltage, current and clock signal frequency targets for the plural loads.” *Id.* at [0026]. The controller “makes dynamic determinations of actual performance versus required performance, and further adapts voltage and frequency parameters of the various subsystems.” *Id.* at [0027]. By communicating with DC/DC converters and clock/shifters, the controller 450 establishes an appropriate operating voltage and frequency for each load. *Id.* at [0028]. Controller 450 communicates these voltage and frequency requirements via bus 460 while DC/DC converters and clock circuits communicate information to the controller, such as “circuit activity information, as described herein, information from clock circuits regarding lock state, such as for phase-locked-loop circuits, for example, or any other information controller 450 might employ when managing power and clock distribution.” *Id.* at [0029].

2. Halepete

76. International Publication No. WO 01/53921 to Halepete et al. (“*Halepete*”) is a patent application related to determining the operating needs of a central processor to adaptively change the power to the processor, which published

on July 26, 2001. Thus, *Halepete* was published more than one year before the '443 Patent's earliest priority date of January 23, 2003.

77. *Halepete* is directed to:

[C]ontrolling the power used by a computer including the steps of measuring the operating characteristics ... of a central processor of the computer, determining when the operating characteristics of the central processor are significantly different than required by the operations being conducted ([] increase and decrease frequency and voltage conditionals), and changing the operating characteristics of the central processor to a level commensurate with the operations being conducted ([] increase and decrease frequency and voltage steps).

Ex. 1005 at p. 1, item (57). In other words, *Halepete* describes a system that is capable of determining the necessary operating frequency and voltage for a processor and dynamically changing the current operating frequency and voltage to match the necessary values determined.

78. Figure 1 of *Halepete* shows a processor 10, a clock generator 11, a programmable voltage generator 12, and other components. *Id.* at p. 4, ll. 21-23.

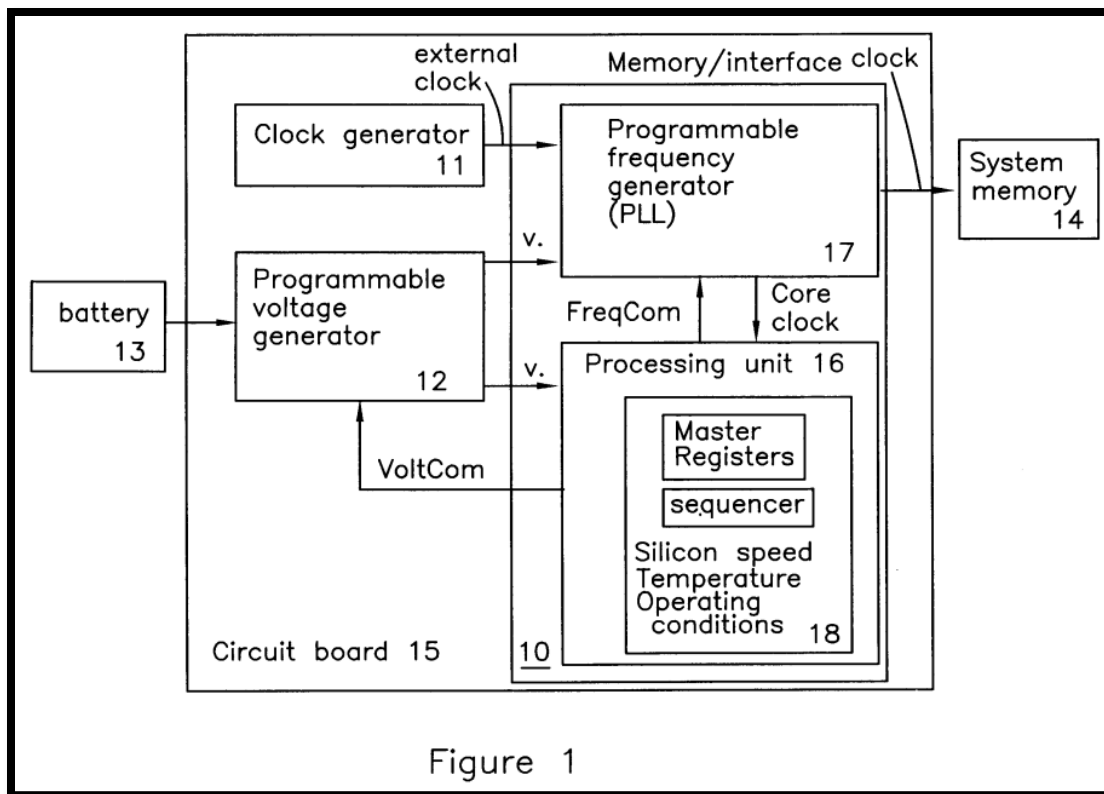


Figure 1

Reproduced from *Halepete*

Id. at p. 24. As shown, the clock generator 11 supplies an external clock to the processor 10, and more specifically to the phase-locked loop (PLL) 17. The PLL 17 “receives an external frequency often referred to as a ‘slow clock’ from the external clock generator 11.” *Id.* at p. 6, ll. 3-5. While only processing unit 16 is shown, *Halepete* states that the processor 10 “also typically includes a number of other components which are known to those skilled in the art but are not pertinent to the present invention and are therefore not illustrated.” *Id.* at p. 5, ll. 7-10. With respect to processing unit 16, “processing unit 16 includes a number of logical components

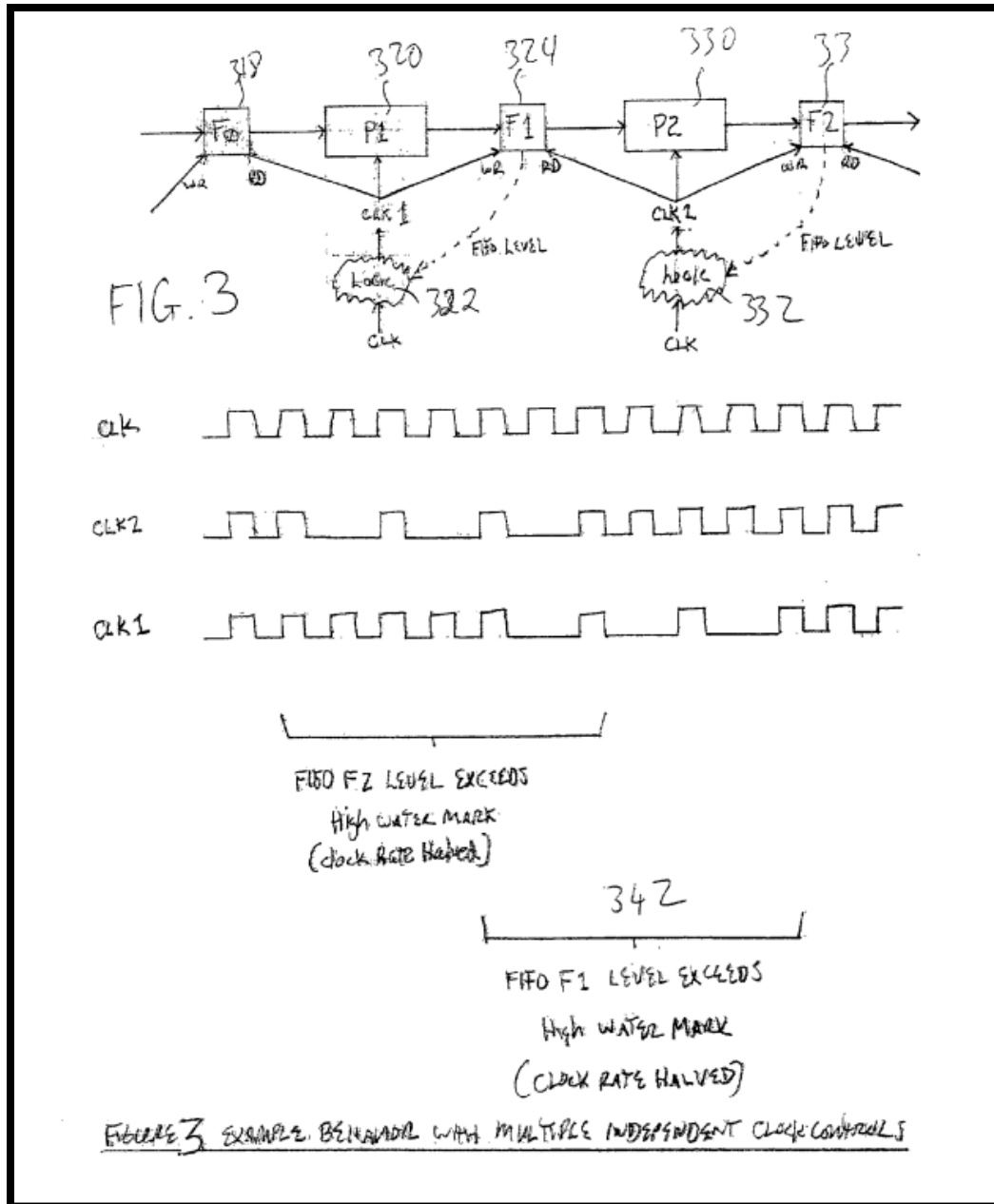
including a master control unit 18 which is the central portion for accomplishing clock and voltage control.” *Id.* at p. 5, ll. 10-12.

79. “In the present invention, the master control unit 18 also includes circuitry for monitoring the operating characteristics of the processor. Various monitoring functions (such as circuitry for accomplishing voltage and frequency monitoring) which are well known to the prior art are included as a part of the logical master control unit 18.” *Id.* at p. 5, ll. 12-17. For more adaptability, separate clocks are provided for each component within processor 10. *Id.* at p. 6, ll. 5-10. *Halepete* explicitly states that the frequency generator is able to “provide individual frequencies selectable for each of these components.” *Id.* at p. 6, ll. 11-13. The control software “detects operating characteristics and determines whether those characteristics indicate that the frequency and the voltage of operation should be changed.” *Id.* at p. 11, ll. 14-16.

3. *Sherburne*

80. U.S. Patent Publication No. 2002/0169990 to Sherburne et al. (“*Sherburne*”) is a patent application related to processing units in communication with one another which was filed on March 21, 2001, and published on November 14, 2002. Thus, *Sherburne* was filed and published before the ’443 Patent’s earliest priority date of January 23, 2003.

81. *Sherburne* discloses “one or more processing units, each unit having a clock input that controls the performance of the unit; one or more clock controllers having clock outputs coupled to the clock inputs of the processing units, the controller operating [by] varying the clock frequency of each processing unit to optimize speed and processing power for a task; and a high-density memory array core coupled to the processing units.” Ex. 1006 at p.1, item (57). *Sherburne* provides alternatives to the processor units described, such as functional units. *Id.* at [0069]. *Sherburne* describes a FIFO buffer that facilitates communication between the processing units, as seen in Figure 3 below:



Reproduced from *Sherburne*

Id. at p. 4.

82. A data processing unit, such as processor 330, receives the output of a FIFO buffer, such as buffer 324. *Id.* at [0029]. The processor 330 then generates data and provides the data to buffer 334, which in turn provides the data to the next

processor. *Id.* The buffers provide a “buffer fill level feedback signal to the controller 332 such as BUFFER_FULL, BUFFER_EMPTY[.]” *Id.* Based on this, the controller 332 varies the clock signal to the processor either reading or writing on the buffer to adjust the fill rate. *Id.*; *see also id.* at [0013] (“The clock input to the processor and the first buffer can be varied based on the fill status of the first buffer by slowing down or stopping the clock if the first buffer is below its low water mark or if the first buffer is empty. The clock input to the processor and the second buffer based on the fill status of the second buffer can increase the clock if the second buffer is below its low water mark or if the second buffer is empty.”)

83. The clock rate can be reduced to zero for a buffer that is full and provides a high water mark or a BUFFER_FULL signal. *Id.* at [0029]. In other words, the buffer provides a signal to prevent any further writes as it cannot accept any until it is no longer full. *Id.* Similarly, a BUFFER_EMPTY signal indicates the buffer is empty and thus it is impossible for the buffer to perform any reads.

4. Traylor

84. U.S. Patent No. 5,473,756 to Traylor (“*Traylor*”) is a patent related to FIFO buffers which published on December 5, 1995. Thus, *Traylor* was published more than one year before the ’443 Patent’s earliest priority date of January 23, 2003.

85. *Traylor* is directed to “generating control signals for a high speed First In First Out (FIFO) buffer” that “limits the instances where signal glitches may

occur.” Ex. 1007 at p. 1, item (57). The FIFO buffers include logic such that EMPTY and FULL conditions are detected, and ALMOST EMPTY and ALMOST FULL signals can be generated. *Id.* A flag is provided to generate FULL and EMPTY control signals. *Id.* at 5:38-42. For example, a certain AND gate is used to drive the EMPTY signal while a different AND gate is used to drive the FULL signal. *Id.* at 6:11-14.

86. “EMPTY and FULL signals are used to avoid reading from an empty FIFO or writing to a full FIFO.” *Id.* at 5:44-46. *Traylor* explains EMPTY or FULL signals may not be recognized fast enough in a high speed system to “prevent writing to a FIFO that is full or reading from a FIFO that is empty.” *Id.* at 7:21-24. Thus, *Traylor* uses ALMOST EMPTY and ALMOST FULL signals as well as the EMPTY and FULL signals. *Id.* at 7:24-30.

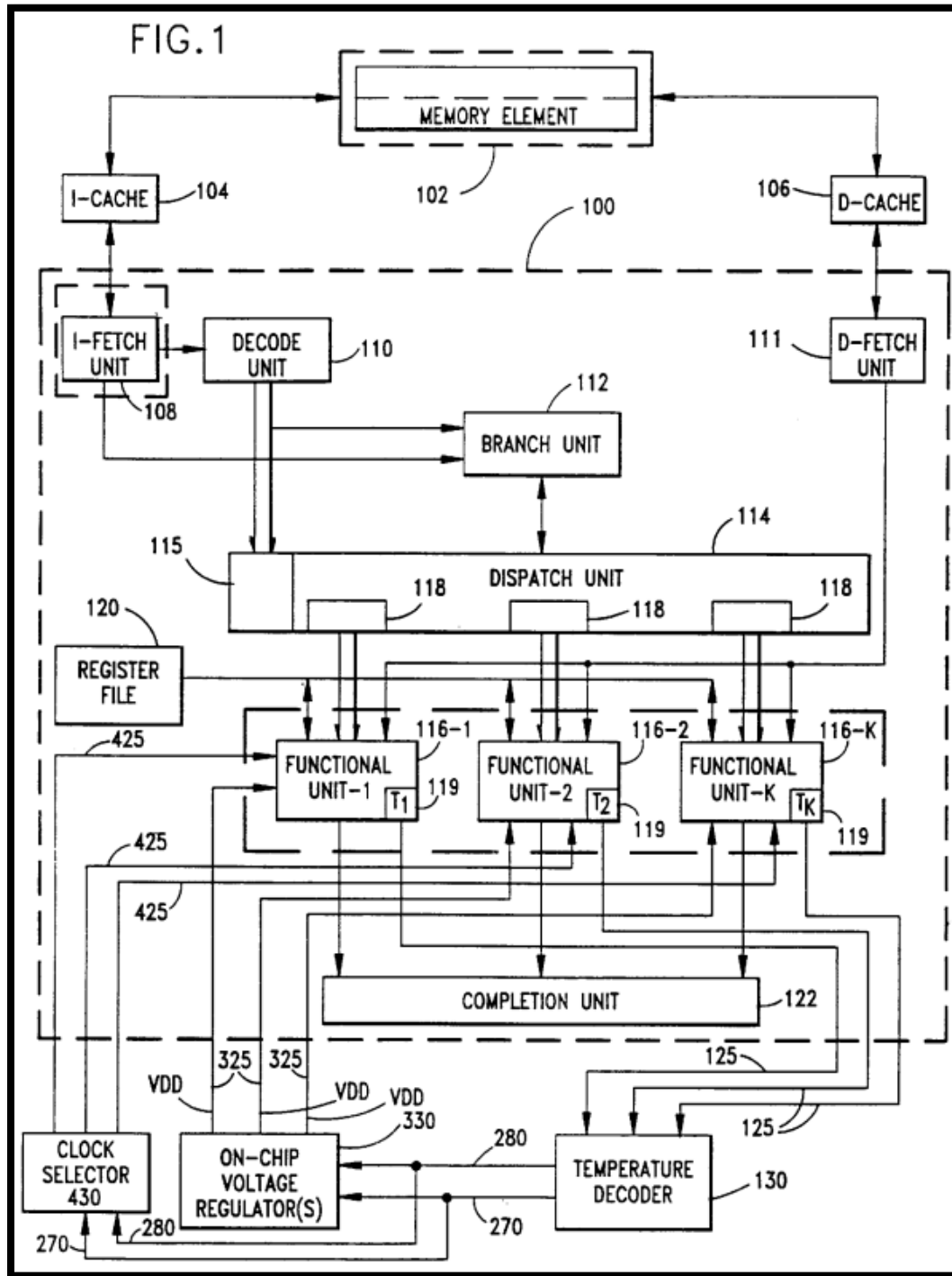
5. Georgiou

87. U.S. Patent No. 6,047,248 to Georgiou et al. (“*Georgiou*”) is a patent related to a superscalar microprocessor that published on April 4, 2000. Thus, *Georgiou* was published more than one year before the ’443 Patent’s earliest possible filing date of January 23, 2003.

88. *Georgiou* describes a system and method of “using thermal feedback to cooperatively vary a voltage and frequency of a circuit to control heating while maintaining synchronization.” Ex. 1008 at p. 1, item (57). Specifically, *Georgiou* is

directed to a superscalar microprocessor that is a “multi-functional unit processor[.]”

Id. at 3:50-52.



Reproduced from *Georgiou*

Id. at p. 3.

89. As seen in Figure 1, processing unit 100 includes functional units 116-1, 116-2...116-K, dispatch unit 114, branch unit 112, and other components. *Id.* *Georgiou* explains that the functional units may include “fixed-point units, floating point units, load/store units, and branch units found in typical general purpose and superscalar microprocessors.” *Id.* at 3:59-61; *see also id.* at 4:52-54 (“As is typical, the functional units may include a floating point unit, multiple load/store and fixed point units, and a branch execution unit.”).

90. *Georgiou* also discloses a clock selector 430 having a plurality of multiplexers 470 that generate respective clock inputs for the plurality of functional units. *Id.* at p. 3, 4:27-51. More specifically, clock selector 430 provides a separate clock frequency 425 (e.g., a clock signal) to each functional unit via a multiplexer 470 (e.g., a clock). *Id.* As further disclosed, each clock and voltage provided is dynamically changeable independently of the clocks and voltages of the other functional units, as *Georgiou* states “each functional unit may be operating under a different voltage 325 and frequency 425[.]” *Id.* at 5:5-6.

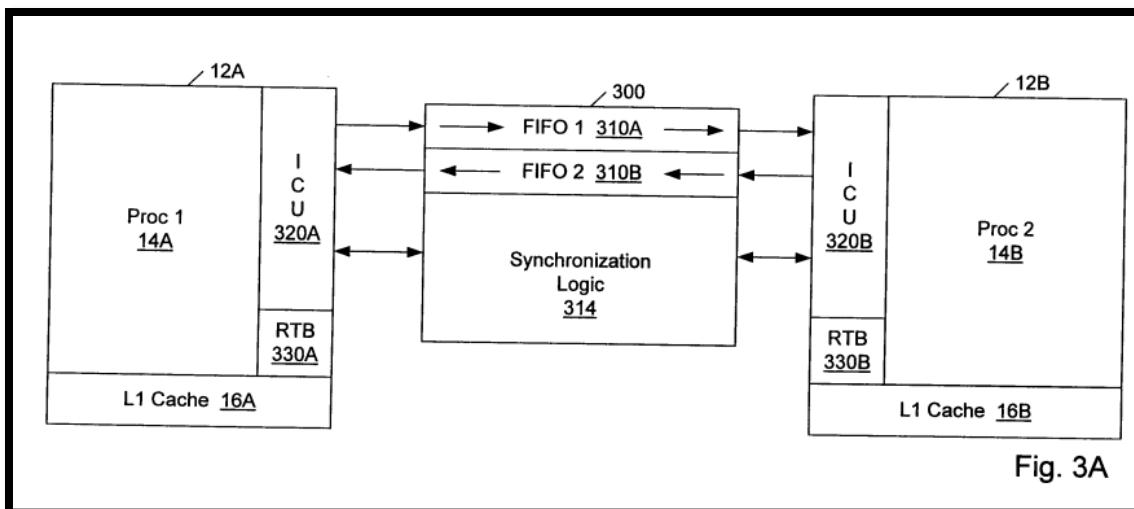
91. The thermal feedback system described by *Georgiou* provides information to the system to vary the voltage and the operating frequency of a specific functional unit within a multi-functional unit processor. *Id.* at 1:23-26. With

respect to Figure 1 again, the temperature decoder 130 generates a control signal 270 to compare values related to temperature change to a threshold value. *Id.* at 4:28-32. Signal 270 is then supplied to the voltage regulators 330 to, if necessary, reduce the supply voltage 325. *Id.* at 4:34-36. Similarly, the signal 270 is provided to clock selector 430 to “modulate the clock frequency sufficiently to maintain system synchronization at the reduced supply voltage.” *Id.* at 4:36-39. This clock frequency 425 is applied to a clock input of the associated functional unit. *Id.* at 4:42-44. Clock selector 430 “may be implemented on-chip and associated with each independently controllable functional unit[.]” *Id.* at 5:2-4.

6. *Kranich*

92. International Publication No. WO 01/33352 to Kranich et al. (“*Kranich*”) is a patent application related to a microprocessor with circuitry to enable symmetrical multiprocessing which published on May 10, 2001. Thus, *Kranich* was published more than one year before the ’443 Patent’s earliest priority date of January 23, 2003.

93. *Kranich* is directed to a “processor architecture containing multiple closely coupled processors in a form of symmetric multiprocessing system.” Ex. 1009 at p. 1, item (57). Specifically, *Kranich* describes interconnection between processors facilitated by FIFO buffers. *Id.* at p. 10, ll. 7-11. Figure 3A illustrates the relationship between the processors and the FIFO buffers, as seen below:



Reproduced from *Kranich*

Id. at p. 26.

94. Figure 3A shows processors 12A and 12B communicating with one another through FIFO 310A and 310B. *Id.* at p. 10, ll. 6-11 (“Each processor 12A-12B includes a processing core 14A-14B, an L1 cache 16A-16B, and an interprocessor communication unit (hereinafter ICU) 320A-320B.”). Accordingly, the ICUs of each processor are coupled to the thread control device 300 “which facilitates communication between processors 12A and 12B.” *Id.* at p. 9, ll. 12-13. The thread control device 300 includes FIFO buffer 310A and FIFO buffer 310B.

E. Summary of the Grounds

95. Below, I discuss the grounds why the challenged claims 1 and 3-12 of the '443 Patent would have been obvious to a POSITA.

96. Ground 1: Claims 1, 3, 4, 5, 8, 9, and 12 are obvious in view of *Shenai*.

97. Ground 2: Claims 4 and 9 are obvious over *Shenai* in view of *Halepete*.

98. Ground 3: Claims 5, 6, 7, 10, and 11 are obvious over *Shenai* in view of *Sherburne*.

99. Ground 4: Claim 7 is obvious over *Shenai* in view of *Sherburne* and in view of *Traylor*.

100. Ground 5: Claims 1, 3, 8, and 12 are obvious in view of *Georgiou*.

101. Ground 6: Claims 4 and 9 are obvious over *Georgiou* in view of *Halepete*.

102. Ground 7: Claims 5 and 10 are obvious over *Georgiou* in view of *Kranich*.

103. Below, I address each claim on a limitation-by-limitation basis for each reference and/or combination of references. When a single reference is used to address a claim limitation, I provide the reason why the claim limitation either would have been recognized by a POSITA as being disclosed by the reference at the time of the purported invention, or would have been obvious to a POSITA in view of the reference at the time of the purported invention. When a combination of references are used to address a claim limitation, I also provide the motivation to combine references and reasons that there would have been a reasonable expectation of success in doing so. Given certain similar claim limitations and the use of the same references in multiple combinations, many of the explanations herein would apply to multiple claim limitations and reasons that a POSITA would have been motivated

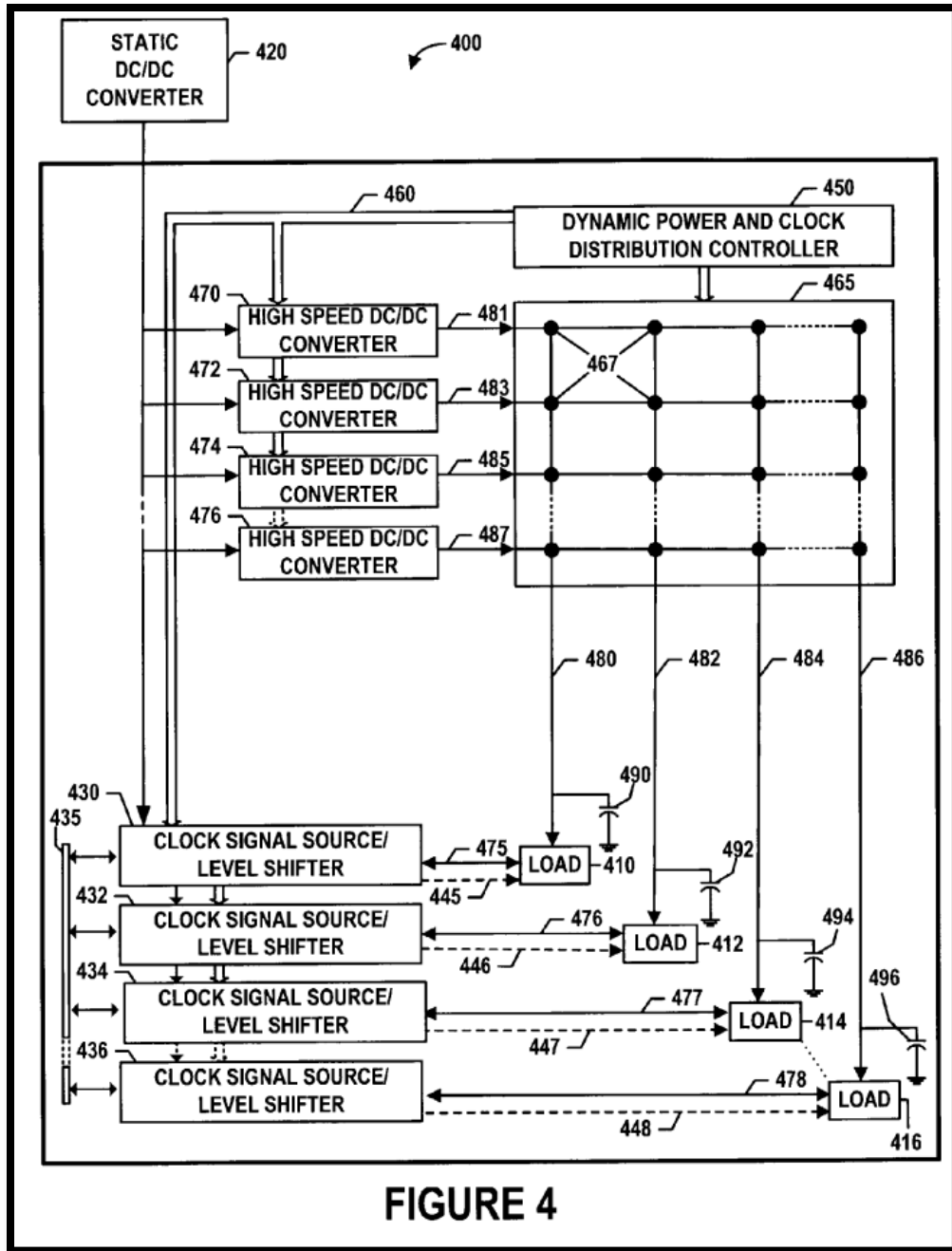
to combine these references and have a reasonable expectation of success in doing so. Therefore, my explanation regarding a certain claim limitation and certain reference or combination may also apply to other claim limitations, or the use of that same reference in another combination for the same or a similar claim limitation. This applies even if there is no explicit incorporation by reference. Furthermore, while I have cited portions of each reference to support my opinions below, I may rely on additional portions of the references to further support those opinions, or portions of other references, including portions identified above where I discussed the prior art and technology background.

F. Ground 1: Claims 1, 3, 4, 5, 8, 9, and 12 are obvious in view of Shenai

1. Claim 1

(a) *1[P]. A multiple clock domain microprocessor comprising:*

104. *Shenai* discloses a plurality of loads that are components of a microprocessor where the plurality of loads operate at independent clock frequencies (e.g., the claimed multiple clock domain). In general, *Shenai* is directed to the architecture of a microprocessor where “certain processing activities of software running on a microprocessor may utilize various subsystems more heavily.” Ex. 1004 at [0030]. Loads 410, 412, 414, and 416 may be “individual components, functional blocks of a single component or independent systems” as seen in replicated Figure 4 below. *Id.* at [0025].



Reproduced from *Shenai*

Id. at p. 5.

105. The power and clock distribution controller 450 can determine “voltage, current and clock signal frequency targets for the plural loads” such that

each load has a separate clock at any given time. *Id.* at [0026]; *see also id.* at [0030] (“For example, certain processing activities of software running on a microprocessor may utilize various subsystems more heavily. By sensing high levels of activity of certain strategically identified nodes, the requirements for those subsystems may be identified as requiring higher (or lower) clocking frequency.”). Specifically, clock/shifters 430, 432, 434, and 436 provide separate clock signals to respective loads at the target frequencies. *Id.* at [0035]. Accordingly, *Shenai*’s circuit 400 shown above includes a plurality of clocks (clock/shifters 430-436 corresponding to the recited multiple clock domain) for providing clock signals to respective plurality of loads, where the plurality of loads correspond to the recited domains, as further discussed below.

106. Examples of loads are provided in *Shenai*, including “components or subsystems of a microprocessor or microcontroller such as cache memory, register files, arithmetic logic units (ALU), integer units, instruction pipeline circuitry, hardware multipliers, floating point circuits, non-volatile memory units, or circuitry clusters, such as those that may be defined within an application specific integrated circuit (ASIC).” *Id.* at [0025].

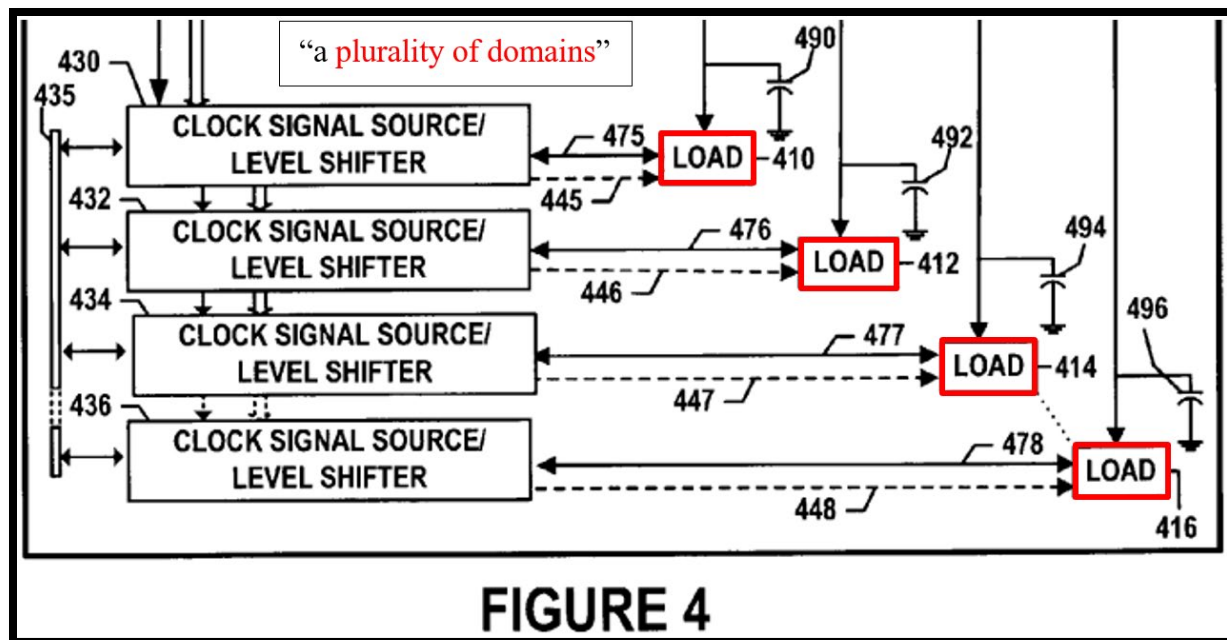
107. Moreover, the ’443 Patent provides examples of domains that are the same as the examples of loads provided in *Shenai*. The ’443 Patent describes a microprocessor that includes an “integer issue/execute 120” domain, a “floating

point issue/execute 130” domain, and a “load/store issue/execute 140” domain. Ex. 1001 at 6:4-8. *Shenai* not only lists arithmetic logic units and integer units as exemplary loads, but *Shenai* also states that the loads can be a “floating point unit” (e.g., the floating point issue/execute 130 domain described in the ’443 Patent) or an “integer unit” (e.g., the integer issue/execute 120 domain described in the ’443 Patent). Ex. 1004 at [0028]. Accordingly, a POSITA would have understood the loads described in *Shenai* are the domains described in the ’443 Patent. As *Shenai* is directed to a microprocessor circuit having a plurality of clocks for providing clock signals to respective plurality of loads, which correspond to multiple domains, *Shenai* teaches a multiple clock domain microprocessor⁵.

(b) *[1(a)] a plurality of domains;*

108. *Shenai* discloses two or more loads (e.g., the claimed plurality of domains). The power distribution management apparatus described in *Shenai* supplies power to “two or more loads” and, more specifically, supplies power to “plural loads 410, 412, 414, and 416[.]” *Id.* at p.1, item (57), [0025] respectively. “Loads 410-416 may be individual components, functional blocks of a single component or independent systems.” *Id.* at [0025].

⁵ I have formatted exact claim language with underlining and italicizing throughout this declaration for emphasis.



Reproduced from *Shenai* (Excerpted and Annotated)⁶

Id. at p. 5, excerpted and annotated. As seen in annotated Figure 4 above, *Shenai* illustrates and describes a plurality of loads in the form of loads 410, 412, 414, and 416.

109. As I discussed above in reference to Claim 1[P] at Section III(F)(1)(a), examples of loads are provided in *Shenai*. *See Id.* at [0025]. Moreover, as I discussed above in reference to Claim 1[P] at Section III(F)(1)(a), the '443 Patent provides examples of domains that are the same as the examples of loads provided in *Shenai*. Based at least on this overlap between the example loads of *Shenai* and the domains

⁶ Quoted claim elements in text boxes are added by me in annotated figures unless indicated otherwise.

described in the '443 Patent, a POSITA would have understood that the loads described in *Shenai* are the same element as the claimed domains. Thus, for the reasons I have explained, *Shenai* teaches a plurality of domains.

- (c) *[1(b)] for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and*

110. *Shenai* discloses, for each of the plurality of loads (e.g., the claimed domains), a clock signal source/level shifter (a “clock/shifter”) (e.g., the claimed clock) for separately generating a clock signal at a frequency for that load, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of loads. For example, *Shenai* discloses a controller that communicates with “clock signal source/level shifters associated with each ‘load’ and establish[es] appropriate operating voltage and frequency values.” Ex. 1004 at [0028]. Further, “[c]lock/shifters 430-436 ... [are] coupled with loads 410-416 so as to provide clock signals via clock signal buses 445, 446, 447 and 448 to the loads at the target frequencies” since requirements for loads 410, 412, 414, and 416 “may be identified as requiring higher (or lower) clocking frequency[.]” *Id.* at [0035] and [0030] respectively. I have provided an annotated version of *Shenai*’s Figure 4 below to assist in illustrating the relationship between the clock/shifters and corresponding loads:

“for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains”

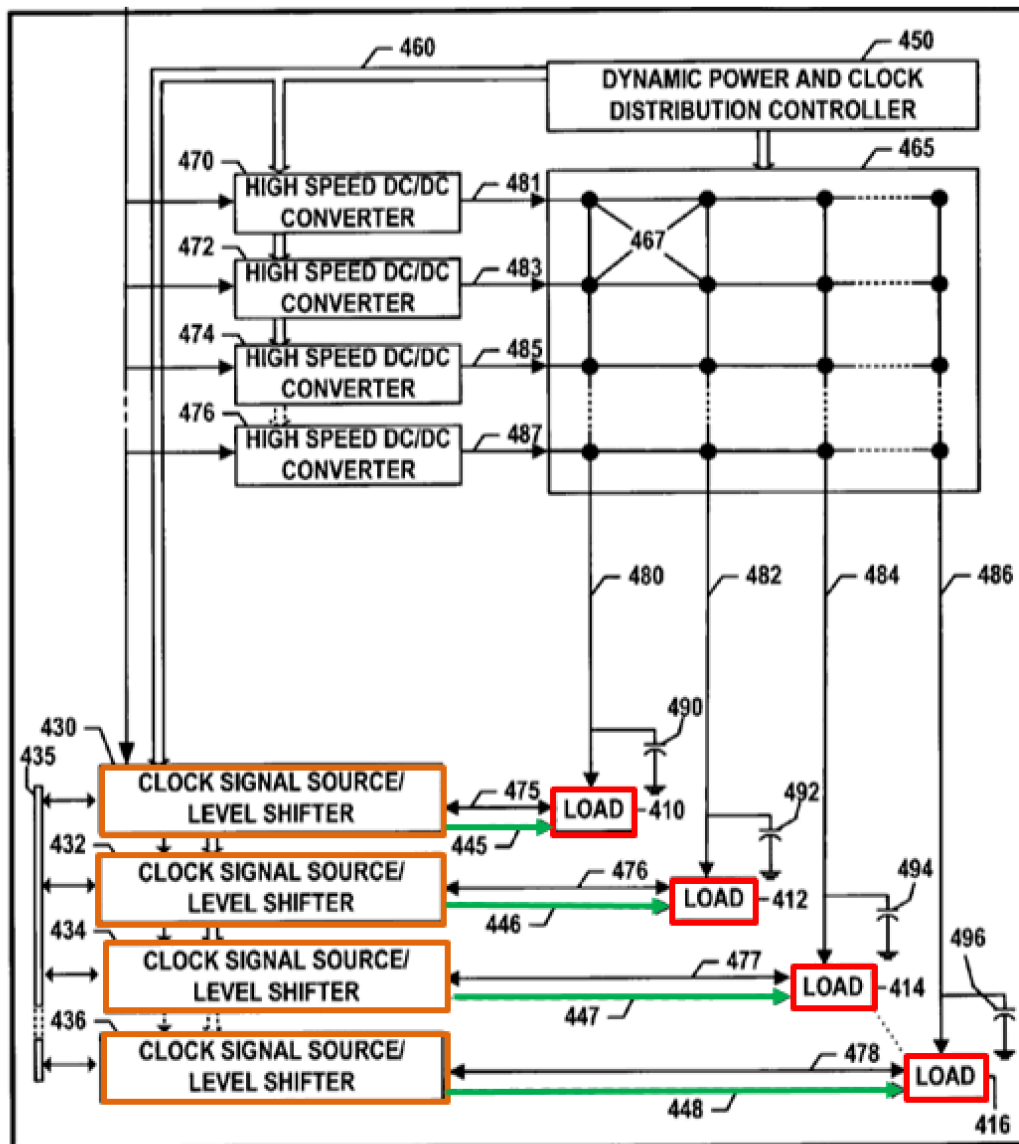


FIGURE 4

Reproduced from *Shenai* (Excerpted and Annotated)

Id. at p. 5, excerpted and annotated.

111. *Shenai* states that “clock/shifters 430-436 may comprise, phase-locked-loop circuits, delay-locked-loop circuits, or combinational logic circuits” that generate clock signals for loads 410-416 by, for example, operating at “at an integer multiplication, a half-integer multiplication or a quarter-integer multiplication of a reference clock signal.” *Id.* at [0036]. In annotated Figure 4 above, I have highlighted the fact that, in the annotated Figure 4, clock signal source/level shifter 430 sends clock signal via bus 445 to load 410, clock signal source/level shifter 432 sends clock signal via bus 446 to load 412, clock signal source/level shifter 434 sends clock signal via bus 447 to load 414, and clock signal source/level shifter 436 sends clock signal via bus 448 to load 416, each of which doing so independently of the other signal source/level shifters. A separate clock signal source/level shifter (e.g., the claimed clock for separately generating a clock signal at a frequency for that domain) provides a clock signal for each respective load and, as I will describe below, the clock signals are dynamically changed depending on load needs. Accordingly, a separate clock in the form of clock signal source/level shifter generates the clock signal that is then provided to the corresponding load.

112. The power and clock distribution controller 450 can determine “clock signal frequency targets for the plural loads” and then subsequently communicate the target frequencies to the respective clock/shifter for a given load. *Id.* at [0026] and [0028]. The controller “makes dynamic determinations of actual performance

versus required performance, and further adapts voltage and frequency parameters of the various subsystems.” *Id.* at [0027]. The controller 450 uses information collected to determine various target parameters for each load, including frequency. *Id.* at [0030]. “By sensing high levels of activity of certain strategically identified nodes, the requirements for those subsystems may be identified as requiring higher (or lower) clocking frequency, and hence higher (or lower) operating voltages.” *Id.*

113. *Shenai* explains that “loads may be partitioned” as seen in Figure 4. *Id.* at [0042]. “[E]ach load of a partitioned (or dynamically partitioned) complex electronic system may function at voltage and frequency values” that are specific for that load. *Id.* “That is, some non-critical components may be provided with clock and voltage settings that allow them to operate [at a lower level of performance] while only those load clusters that must operate at a higher level of performance [do so].” *Id.* The loads are dynamically controlled by rapidly varying clock signals dependent on the circuit operating conditions. *Id.* at [0043]. Therefore, not only are the clock signals provided independent to the other generated clock signals, the clock signals are also dynamically changeable depending on the individual needs of each load at a given time. As *Shenai*’s clock/shifter dynamically generates a clock signal for a given load at a frequency based on that load’s respective needs, the clock signal for each load is generated independent of the clock signal for each other load. For these reasons, *Shenai* teaches for each of the plurality of domains, a clock for

separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains.

- (d) *[1(c)] for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.*

114. *Shenai* discloses, for each of the plurality of loads (e.g., the claimed domains), a voltage supply line (e.g., the claimed voltage input) receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains. For example, *Shenai* discloses a controller that communicates with “clock signal source/level shifters associated with each ‘load’ and establish[es] appropriate operating voltage and frequency values.” Ex. 1004 at [0028]. Further, the circuit of the microprocessor in *Shenai* includes DC/DC converters that are “responsive to controller 450, such that they are selectively coupled with loads 410-416 to provide the respective target voltages and currents to the loads.” *Id.* at [0031]. I have provided an annotated version of *Shenai*’s Figure 4 below to assist in illustrating the relationship between the voltage supply line and corresponding load:

“for each of the **plurality of domains**, a **voltage input** for receiving a **voltage** which is dynamically changeable independently of the **voltages** applied to said others of the **plurality of domains**.”

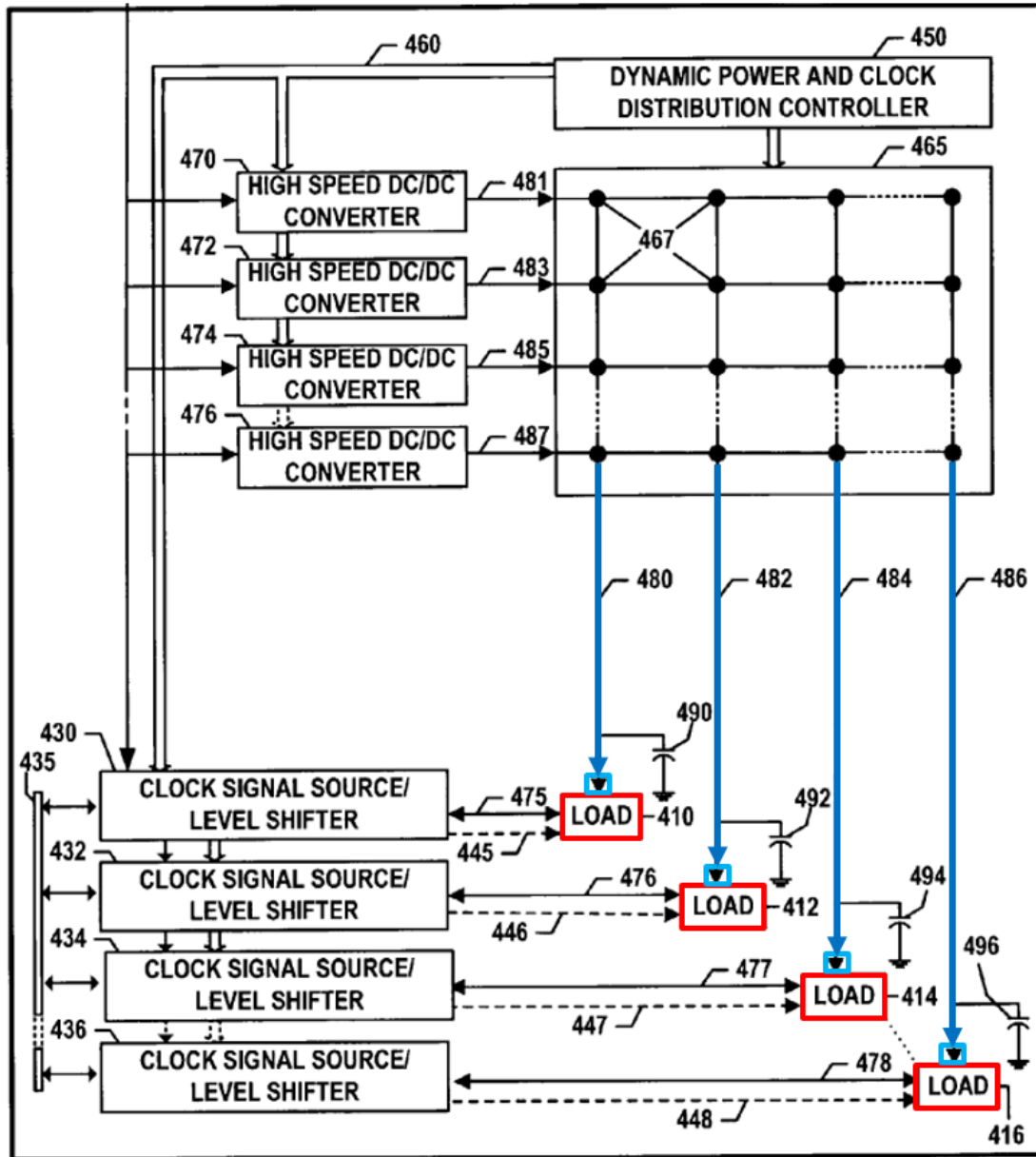


FIGURE 4

Reproduced from *Shenai* (Excerpted and Annotated)

Id. at p. 5, excerpted and annotated.

115. I have highlighted the fact that, in the annotated Figure 4, voltage supply line 480 provides voltage to load 410, voltage supply line 482 provides voltage to load 412, voltage supply line 484 provides voltage to load 414, and voltage supply line 486 provides voltage to load 416, each of which doing so independently of the other voltages. To the extent it is argued that a voltage input is not explicitly shown, it was well understood that, for a load to receive a voltage, the load must be configured to receive the voltage. Thus, it would have been obvious to a POSITA that each load includes a voltage input since the load receives a voltage from a voltage supply line. It would have been common sense for a POSITA that a voltage input is required for a load to receive a voltage from a voltage supply line. For example, in the Background of the Technology at Section III(A)(1), I describe that was known for microprocessors to use input pins to receive a voltage. *See* Ex. 1013 at p. 138, 175. A POSITA would have been motivated to apply a known technique of using a voltage input (e.g., an input pin) to known devices such as *Shenai's* microprocessor to yield the predictable result of receiving a voltage from a respective voltage supply line with a reasonable expectation of success.

116. Similar to determining a target frequency, the power and clock distribution controller 450 is capable of determining voltage and “includes two or more power sources responsive to the controller so as to be selectively coupled with the loads to provide the target voltage and current to the loads.” Ex. 1004 at p. 1,

item (57); *see also id.* at [0026] (“Power and clock distribution controller 450 may be capable of determining voltage, current and clock signal frequency targets for the plural loads.”). The controller makes “dynamic determinations of actual performance versus required performance, and further adapts voltage and frequency parameters of the various subsystems.” *Id.* at [0027]. The controller 450 uses information collected to determine various target parameters for each load, including frequency *Id.* at [0030].

117. Specifically, controller 450 communicates with DC/DC converters, such as high speed DC/DC converters 470, 472, 474, and 476 shown in Figure 4, to determine operating voltage. *Id.* at [0028]. This determined voltage is then provided to individual loads via separate corresponding voltage supply lines. “Network 465 may be responsive to controller 450 so as to selectively couple DC/DC converters 470-476 with loads 410-416 via connection network 465's nodes 467 and voltage supply lines 480, 481, 482, 483, 484, 485, 486 and 487.” *Id.* at [0037]. The DC/DC converters 470-476 are selectively coupled with loads 410-416 to provide the “respective target voltages[.]” *Id.* at [0031]. “By sensing high levels of activity of certain strategically identified nodes, the requirements for those subsystems may be identified as requiring higher (or lower) clocking frequency, and hence higher (or lower) operating voltages.” *Id.* at [0030].

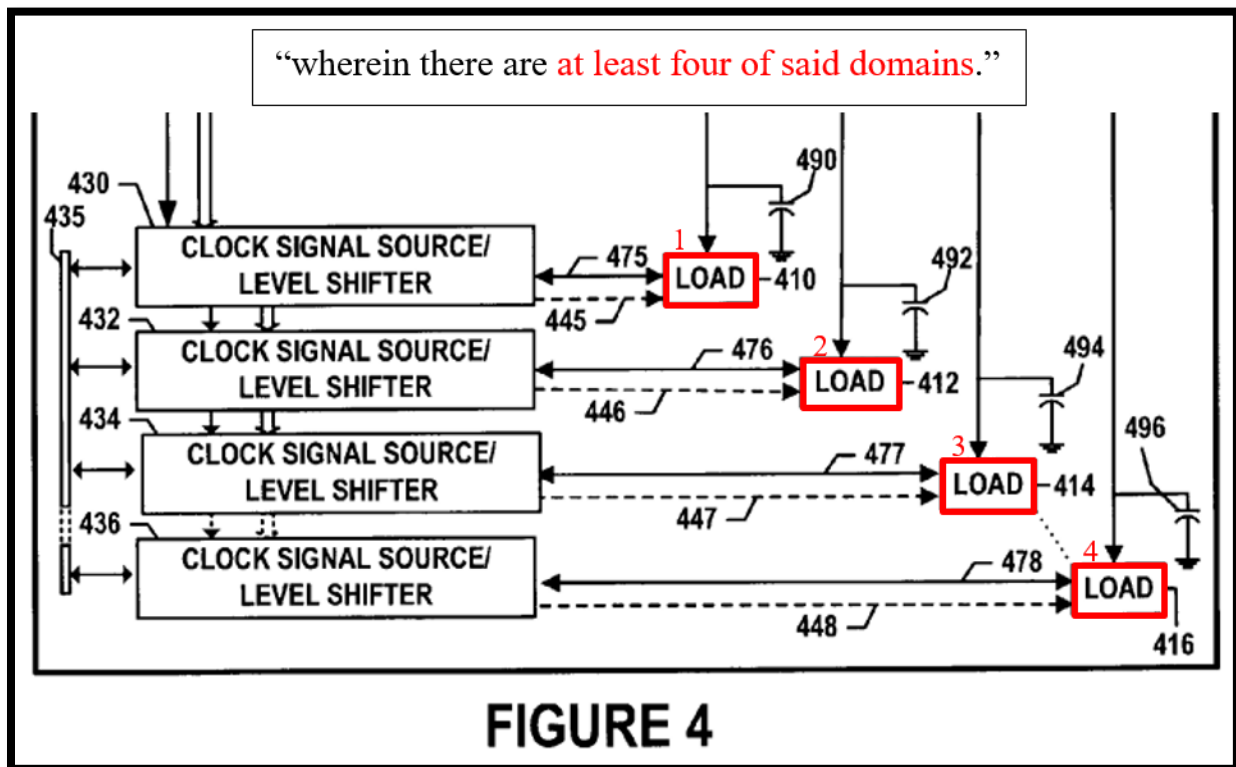
118. The circuit 400 even includes local capacitors 490, 492, 494, and 496 for each load to stabilize the voltage delivered to the load from the DC/DC converters via the separate voltage supply lines. *Id.* at [0034]. It is apparent that *Shenai* describes the ability to supply dynamically changeable voltages independent of the other voltages being supplied. *Shenai* explains that the loads can operate “at varying target voltages” such that the target voltage is decided depending on the needs of the system at a given time. *Id.* at [0035].

119. *Shenai* explains that “loads may be partitioned” as shown in its Figure 4. *Id.* at [0042]. “[E]ach load of a partitioned (or dynamically partitioned) complex electronic system may function at voltage and frequency values” that are specific for that load. *Id.* “That is, some non-critical components may be provided with clock and voltage settings that allow them to operate [at a lower level of performance] while only those load clusters that must operate at a higher level of performance [do so].” *Id.* The loads are dynamically controlled by rapidly varying voltage inputs dependent on the circuit operating conditions. *Id.* at [0043]. Therefore, not only are the voltage inputs provided independent to the other voltages supplied, but the voltages are also dynamically changeable depending on the individual needs of each load at a given time. As *Shenai*’s DC/DC converter dynamically generates a voltage for a given load based on that load’s changing needs, the voltage for each load is changed independent of the voltage for each other load. For these reasons, *Shenai*

renders obvious for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

2. Claim 3 – The microprocessor of claim 1, wherein there are at least four of said domains.

120. For the reasons I discussed above for Claim 1 at Section III(F)(1), Shenai renders obvious the microprocessor of claim 1. Additionally, Shenai discloses a plurality of loads, including explicitly illustrating and describing four separate loads 410, 412, 414, and 416 (e.g., the claimed at least four of said domains). The at least four loads (domains) can be seen in annotated Figure 4, which I have presented below.



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Ex. 1004 at p. 5, excerpted and annotated. As I have indicated, *Shenai* provides four loads as an example amount of loads but can have “additional loads [] included with circuit 400.” *Id.* at [0025].

121. As previously described, controller 450 determines voltage, current, and frequency targets for load 410, load 412, load 414, and load 416. *Id.* at [0030]. “DC/DC converters 470-476 may be responsive to controller 450, such that they are selectively coupled with loads 410-416 to provide the respective target voltages and currents to the loads.” *Id.* at [0031]. Thus, *Shenai* renders obvious the microprocessor of claim 1, wherein there are at least four of said domains.

3. Claim 4 – The microprocessor of claim 1, wherein the microprocessor is programmed to determine a slack in processing in one of the domains and to reduce the clock frequency and the voltage in said one of the domains to reduce the slack.

122. For the reasons I discussed above for Claim 1 at Section III(F)(1), *Shenai* renders obvious the microprocessor of claim 1. Additionally, as described in the '443 Patent and understood by a POSITA, “slack” in processing “indicates that [a] previous operation completed earlier than necessary.” Ex. 1001 at 11:28-29. In other words, as I also explain in the Background of the Technology Section III(A)(3), the difference in computing time between the slowest dependency (e.g., the critical path) and a different dependency within an operation defines the slack that

dependency has. *See* Ex. 1018 at p. 1, item (57), 2:16-22. Slack helps to determine operations that are completing faster than needed so a user can reduce the power provided to that operation, thus increasing the completion time (and reducing the slack). *Id.* With this in mind, *Shenai* discloses a microprocessor programmed to determine critical node paths (e.g., critical functions that can cause slack to occur) and to subsequently reduce the clock frequency and voltage provided to a load that has slack.

123. As I discussed in the Background of the Technology at Section III(A)(3), slack is often found by determining the circuitry activity a certain load (e.g., domain) needs to perform necessary functions. *See Id.* at p. 1, item (57), 2:16-22. Similarly, *Shenai* explains “controller 450 may comprise software instructions for determining the voltage, current and frequency targets based, on information provided by circuitry included with controller 450, which may indicate an amount of circuit activity for each of the loads.” Ex. 1004 at [0026]. More specifically, by sensing, via the controller 450, “high levels of activity of certain strategically identified nodes, the requirements for those subsystems may be identified as **requiring higher (or lower) clocking frequency, and hence higher (or lower) operating voltages.**” *Id.* at [0030], emphasis added. Additionally, the “controller 450 may comprise sensing circuits connected to **critical-nodes (nodes that tend to limit the rate at which a given operation may be completed) and responsively**

adjust (lower) frequencies of other non-critical signal paths, or adjust (increase) the frequency of the circuit elements containing the critical node paths.” *Id.*, emphasis added.

124. It would have been obvious to a POSITA that *Shenai*’s controller determines slack, using sensing circuits, in order to lower frequencies of non-critical signal paths and increase the frequency of circuit elements containing the critical node paths. *Shenai* explains that such sensing circuits “provide circuit activity information for loads 410-416” and “may determine a number of logic transitions in a predetermined time period.” *Id.* at [0029]-[0030]. As I have also explained in the Background of the Technology at Section III(A)(3), calculating processing needs and adjusting voltages and frequencies to save energy based on the processing needs was known in the art at the time of the invention. *See* Ex. 1021 at p.3 (“[t]he processor measures ILP over some specified interval of time in terms of a MIPS [(“Million Instructions Per Second”)] rate. If the MIPS rate changes appreciably either up or down, the processor adjusts its supply voltage accordingly.... Using this MIPS rate, a new frequency (and, hence, voltage level) is calculated.”).

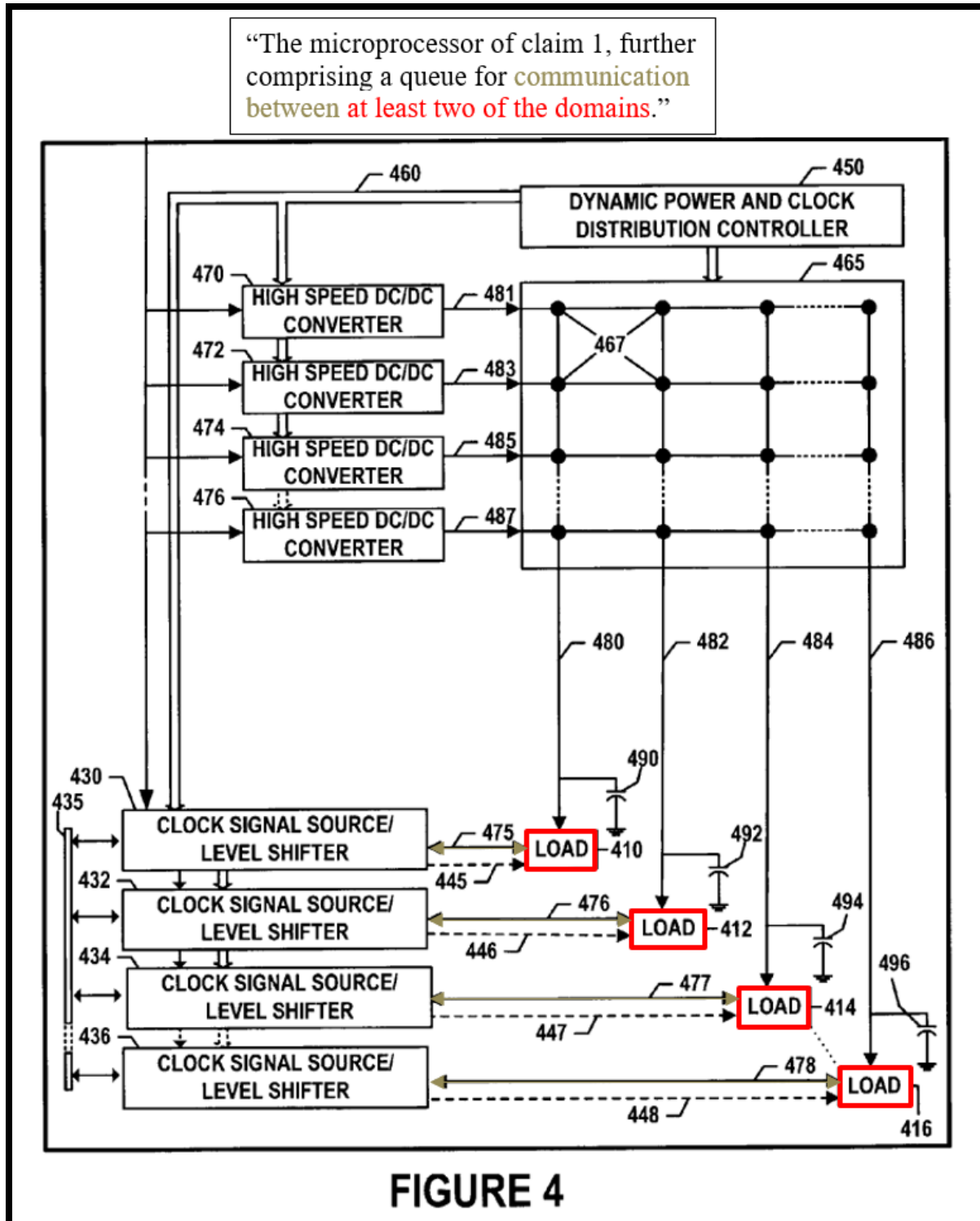
125. Accordingly, a POSITA would have understood that *Shenai*’s controller adjusts frequencies and voltages to reduce slack by identifying critical paths and non-critical paths using sensing circuits to determine a number of logic transactions in a given time and based on known techniques for identifying

processing needs. It would have been obvious to a POSITA that in order to identify the critical paths and non-critical paths of *Shenai*, processing would be needed to determine whether a path is critical or non-critical. A POSITA would have recognized that known techniques (e.g., measuring processing needs in terms of a MIPS rate) would have been used to determine the processing needs of *Shenai*'s loads to identify the critical and non-critical paths in the same way as was known in the art with a reasonable expectation of success.

126. Since *Shenai* provides circuitry for a microcontroller that allows for dynamically adjusting both clock frequency and voltage, “each load of a partitioned (or dynamically partitioned) complex electronic system may function at voltage and frequency values that allow the load to realize [certain] power savings.” *Id.* at [0042]. Thus, non-critical components are provided with clock and voltage settings that cause them to operate at a low level of power while critical components are provided with clock and voltage settings that cause them to operate at a high level of power. *Id.* Thus, *Shenai* renders obvious the microprocessor of claim 1, wherein the microprocessor is programmed to determine a slack in processing in one of the domains and to reduce the clock frequency and the voltage in said one of the domains to reduce the slack.

4. Claim 5 – The microprocessor of claim 1, further comprising a queue for communication between at least two of the domains.

127. For the reasons I have detailed above for Claim 1 at Section III(F)(1), *Shenai* renders obvious the microprocessor of claim 1. The '443 Patent describes a “queue” structure that asserts a FULL flag to assert that a producer “can no longer write to the queue until the flag is deasserted” and an EMPTY flag to assert “that there is no valid data [] to read from the queue.” Ex. 1001 at 6:54-60. *Shenai* discloses intercommunication between loads. For example, *Shenai* states “**clock/shifters 430-436 may also include circuitry that allows** electrical signal **communication between loads** operating at varying target voltages via signal buses 475, 476, 477 and 478. Such an approach may improve the noise tolerance of such electrical signal communication.” Ex. 1004 at [0035], emphasis added. I have provided an annotated version of Figure 4 below to further illustrate the buses 475, 476, 477, and 478 allowing for communication.



Reproduced from Shenai (Excerpted and Annotated)

Id. at p. 5, excerpted and annotated.

128. To the extent it is argued *Shenai* does not specify how such communication is implemented, the use of a queue would have been obvious to a POSITA. As I discuss in the Background of the Technology at Section III(A)(2), a POSITA would have understood the use of queue structures for inter-domain communication was well-known at the time of invention as it is one of the most common communication mechanisms in microprocessors. *See* Ex. 1015 at p. 1, 2, 6-8. A POSITA would have also appreciated using an effective, well-known microprocessor component in a similar microprocessor to allow inter-domain communication. *Shenai* already teaches that its clocks/shifters “include circuitry that allows electrical signal communication between loads operating at varying target voltages via signal buses 475, 476, 477 and 478.” Ex. 1004 at [0035]. A POSITA would have recognized that *Shenai*’s communication between loads could have been implemented using a queue and would have been improved by implementing a queue in the same predictable way as known in the art. For example, as I discuss in Section III(A)(2), a POSITA would have recognized a queue would have improved inter-domain communication between *Shenai*’s loads by allowing a respective load to be ready to receive communication before such communication is initiated. *See* Ex. 1015 at p. 1 (explaining that when an instruction pipeline is received, a microprocessor “writes the renamed instructions into the queues and reads the busy-bit table to determine if the operands are initially busy. Instructions wait in the

queues until all their operands are ready.”) For these reasons, a POSITA would have been motivated to combine prior art elements (e.g., the inter-load communication taught in *Shenai* with the queue structure known in the art) according to known methods to yield predictable results, and would have a reasonable expectation of success. Thus, a queue for communication between at least two of the domains would have been obvious to a POSITA over *Shenai* in view of queue structures known in the art.

5. Claim 8

- (a) 8[P]. *A method of operating a microprocessor, the method comprising:*

129. *Shenai* discloses a microprocessor. I have discussed this extensively with regards to Claim 1 at Section III(F)(1). For the same reasons I have provided above, *Shenai* also discloses a method of operating a processor. Additionally, *Shenai* explicitly states the invention is directed to the “organization and **method of operation**[.]” Ex. 1004 at [0006], emphasis added. Thus, *Shenai* renders obvious a method of operating a microprocessor.

- (b) [8(a)] (a) *providing a plurality of domains in the microprocessor;*

130. I have previously explained why *Shenai* discloses a plurality of domains in reference to Claim 1(a) at section III(F)(1)(b). Thus, for the same reasons, *Shenai* teaches providing a plurality of domains in the microprocessor.

- (c) [8(b)] (b) *clocking each of the domains separately at a clock frequency;*

131. I have previously explained why *Shenai* discloses for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain in reference to Claim 1(b) at section III(F)(1)(c). Thus, for the same reasons, *Shenai* teaches clocking each of the domains separately at a clock frequency.

- (d) [8(c)] (c) *applying a voltage to each of the domains separately;*

132. I have previously explained why *Shenai* renders obvious, for each of the plurality of domains, a voltage input for receiving a voltage in reference to Claim 1(c) at section III(F)(1)(d). Thus, for the same reasons, *Shenai* renders obvious applying a voltage to each of the domains separately.

- (e) [8(d)] (d) *operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another; and*

133. *Shenai* renders obvious operating the microprocessor such that each load operates synchronously while the loads operate asynchronously relative to one another. I have explained how *Shenai* describes a microprocessor with a plurality of loads where each load is provided a specific clock frequency independent of the clock frequencies for the other loads in reference to Claim Element 1(b) at section III(F)(1)(c). Because of this, coupled with the fact *Shenai* also discloses providing voltages to each load independent of the others as discussed in reference to Claim

Element 1(c) at Section III(F)(1)(d), *Shenai* describes operating a microprocessor such that the loads operate asynchronously relative to one another.

134. The '443 patent describes a multiple clock domain microprocessor where each functional block operates with “synchronizing circuits [that] ensure reliable **inter-domain** communication.” Ex. 1001 at 4:17-20, emphasis added. However, in case it is argued that *each domain operates synchronously* refers to intra-domain synchronization, I address below how it would have been obvious to a POSITA that *Shenai* discloses both inter-domain synchronization and intra-domain synchronization. The circuitry of the microprocessor described in *Shenai* can communicate electric signals between loads (for inter-load synchronized communication) and for each individual load (for intra-domain synchronized communication). This allows for the microprocessor to have loads function at different frequencies (at each given loads respective voltage and frequency), asynchronous of one another, while communicating synchronously with each other, as described below:

Circuit 400 may further include plural clock signal sources/level shifters (clock/shifters) 430, 432, 434 and 436, which may be coupled with a logic bus 435 for communication with other devices or components. **Clock/shifters 430-436 may also be responsive to controller 450 and coupled with loads 410-416 so as to provide clock signals via clock signal buses 445, 446, 447**

and 448 to the loads at the target frequencies, which may be determined by controller 450, as has been previously described. As was previously discussed, **clock/shifters 430-436 may also include circuitry that allows electrical signal communication between loads operating at varying target voltages via signal buses 475, 476, 477 and 478**. Such an approach may improve the noise tolerance of such electrical signal communication.

Ex. 1004 at [0035], emphases added. Accordingly, *Shenai* discloses that its loads operate asynchronously relative to each other by using each load's respective different voltage and frequency.

135. *Shenai* discloses inter-domain synchronization as “clock/shifters 430-436 may also include circuitry that allows electrical signal communication between loads operating at varying target voltages via signal buses 475, 476, 477 and 478.” *Id.* It would have been obvious to a POSITA that such circuitry that allows electrical signal communication between loads corresponds to synchronous operation as *Shenai* contemplates circuit operation configurations that “allow for synchronous communication between loads 410-416, as opposed to asynchronous communication, which may be undesirable.” *Id.* at [0036]. A POSITA would have recognized that applying known synchronization techniques, as suggested in *Shenai* and as I further discuss below, to *Shenai*'s inter-load communication would yield

predictable results for improved synchronized communication such by improving “the noise tolerance of such electrical signal communication.” *Id.* at [0035].

136. Each of *Shenai*’s loads are also intra-domain synchronized. *Shenai* discloses that loads may be “independent systems.” *Id.* at [0025]. As discussed above for Claim 8(b) at Section III(F)(5)(c) and Claim 8(C) at Section III(F)(5)(d), each load is provided a target frequency and voltage based on its respective needs. Accordingly, the components of each independent system that encompass a load operate using the same frequency and voltage. Thus, each load (e.g., components in an independent system) operates synchronously using its provided frequency and voltage.

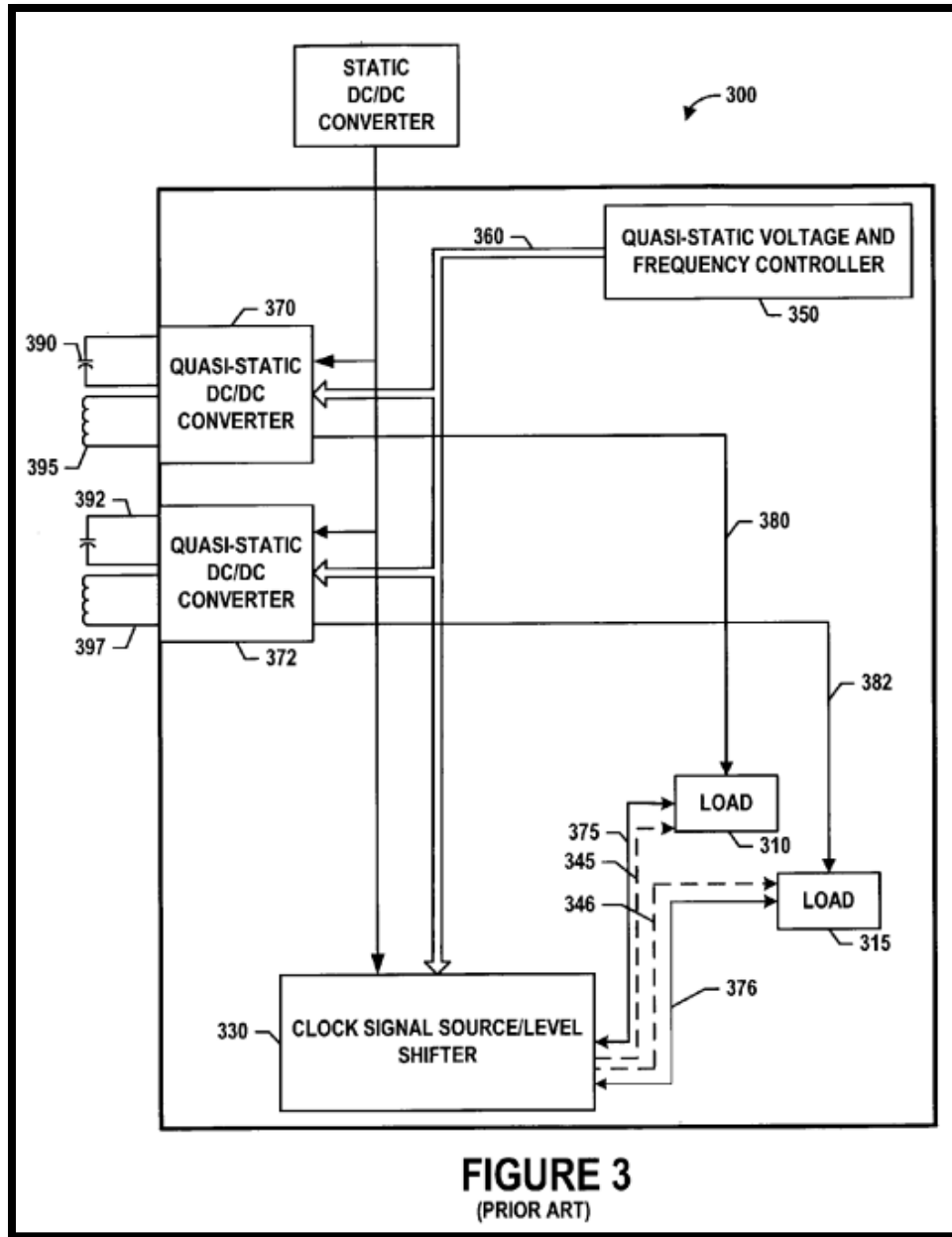
137. As I have also explained in the Background of the Technology at Section III(A)(4) above, operating separately partitioned domains within a microprocessor asynchronously while each domain operate synchronously was well known in the art prior to the time of invention. *See* Ex. 1022 at p.1 (“[Globally Asynchronous, Locally Synchronous “GALS”] systems aim to combat all three of these problems by doing away with a global clock and instead having a locally generated clock for every module. ... Obviously, modules cannot be [synchronized] if they all use different clocks, so we use an asynchronous protocol to communicate between them.”).

138. In reference to asynchronous operation, as discussed in the Background of the Technology at Section III(A)(4) above, functional units were known to need different levels of power, thus they needed different clocks and voltages. Because of this, it was inefficient not only to provide the same power to each functional unit, but also to have each functional unit operate synchronously as this could lead to large thermal dissipation. *Id.* Quickly, microprocessors were designed to have functional units operate asynchronously to conserve power and to reduce the overall strain and load on the microprocessor at any given time. *Id.*

139. As I discussed in the Background of the Technology at Section III(A)(4) above, intra-domain synchronization was known such that “[l]eaving a synchronous block into the asynchronous domain is a reasonably trivial matter.” *Id.* Additionally, for example, for inter-domain synchronization when re-entering another synchronous block, “GALS systems stretch the clock [by preventing] the clock from rising if asynchronous data is arriving” *Id.* Similarly, as another example of inter-domain synchronization, it was known that “if the frequencies at which [] individual [processing elements ‘PEs’] operate differ from one another and from other elements within the system where the multiprocessor chip is employed, ... a synchronization schema must be implemented when there is a need to communicate data between PEs (or with other system elements) that operate at different frequencies.” Ex. 1023 at 6:14-21. “To effect such synchronization, each PE...is

connection [sic] to an arrangement comprising elements 150 and 160. Level converter 150 converts the variable voltage swings of the PEs to a fixed level swing, and network 160 resolves the issue of different clock domains” *Id.* at 6:29-31.

140. Additionally, in reference to inter-domain synchronization, *Shenai* also describes prior art microprocessors including a clock signal source/level shifter that globally supplies a clock signal to more than one load and includes circuitry to “modify the voltage level of electrical signals, such as the clock signals and signals communicated between load 310 and 315 via signal lines 375 and 376 when they are operating at different voltage levels.” Ex. 1004 at [0022]. This is similar to the ’443 Patent: “The preferred embodiment uses four domains, one of which includes the L2 cache, so that domains may vary somewhat in size and still be covered by a single clock.” Ex. 1001 at 5:7-9. *Shenai* explains that such “level shifting techniques are known, and may reduce the effect of noise on the communication of electrical signals between loads 310 and 315” and designates Figure 3 as prior art as seen below.



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Id. at [0022], p. 4.

141. Accordingly, *Shenai* discloses that its loads operate asynchronously to each other using the specific frequencies and voltages provided to each respective load based on its needs. *Shenai* also discloses that each load is intra-load

synchronized as each of the components of a given load (an independent system's components) operate using the same specific frequency and voltage for that load. *Shenai* also discloses that each load is inter-load synchronized using "circuitry that allows electrical signal communication between loads operating at varying target voltages." *Id.* at [0035]. To the extent it is argued that *Shenai* does not disclose how its inter-load synchronization is implemented, a POSITA would have been motivated to implement *Shenai*'s inter-load communication using known synchronization techniques (e.g., by stretching a clock or using a synchronization schema as discussed in the Background of the Technology at Section III(A)(4)). *See* Ex. 1022 at p.1; *see also* Ex. 1023 at 6:14-21, 6:29-31. Such a combination would yield predictable results for improving "the noise tolerance of such electrical signal communication" as suggested in *Shenai*. Ex. 1004 at [0035]. Thus, operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another would have been obvious in view of *Shenai*.

- (f) [8(e)] (e) dynamically controlling the clock frequency and the voltage in each of the plurality of domains independently of the clock frequencies and the voltages in others of the plurality of domains.

142. I have previously explained why *Shenai* discloses both dynamically changing the clock frequency and the voltage in each load independently of the other loads in reference to Claim 1(b) at Section III(F)(1)(c) and Claim 1(c) at Section

III(F)(1)(d). Thus, for the same reasons, *Shenai* teaches dynamically controlling the clock frequency and the voltage in each of the plurality of domains independently of the clock frequencies and the voltages in others of the plurality of domains.

6. Claim 9

(a) 9[P]. The method of claim 8, wherein step (e) comprises:

143. For the reasons I have detailed above in reference to Claim 8 at Section III(F)(5), *Shenai* renders obvious the method of claim 8.

(b) [9(a)] (i) determining a slack in processing in one of the domains; and

144. I have previously explained why *Shenai* renders obvious a microprocessor that is programmed to determine a slack in processing in one of the loads in reference to claim 4 at Section III(F)(3). Thus, for the same reasons, *Shenai* renders obvious determining a slack in processing in one of the domains.

(c) [9(b)] (ii) reducing the clock frequency and the voltage in said one of the domains to reduce the slack.

145. I have previously explained why *Shenai* renders obvious a microprocessor that, after determining a slack in processing in one of the loads, the microprocessor is able to reduce the clock frequency and the voltage in that load to reduce the slack in reference to claim 4 at Section III(F)(3). Thus, for the same reasons, *Shenai* renders obvious reducing the clock frequency and the voltage in said one of the domains to reduce the slack.

7. Claim 12 – The method of claim 8, wherein there are at least four of said domains.

146. For the reasons I have detailed above in reference to claim 8 at Section III(F)(5), *Shenai* renders obvious the method of claim 8. Additionally, I have previously explained why *Shenai* discloses a microprocessor that has at least four loads (four domains) in reference to claim 3 at Section III(F)(2). Thus, for the same reasons, *Shenai* teaches wherein there are at least four of said domains.

G. Ground 2: Claims 4 and 9 are obvious over *Shenai* in view of *Halepete*

1. Claim 4 – The microprocessor of claim 1, wherein the microprocessor is programmed to determine a slack in processing in one of the domains and to reduce the clock frequency and the voltage in said one of the domains to reduce the slack.

147. I have explained above how *Shenai* renders obvious the limitations of Claim 4 at Section III(F)(3). To the extent it is argued *Shenai* alone does not disclose and render obvious the entirety of Claim 4, a POSITA would have found the limitations of Claim 4 obvious in view of *Halepete*. Similar to *Shenai*, *Halepete* describes a processor that includes, at the least, a processing unit 16 with a clock generator and a voltage generator. Ex. 1005 at pp. 4-5, ll. 2-6. Additionally, in *Halepete* the “processing unit 16 includes a number of logical components including a master control unit 18 which is the central portion for accomplishing clock and voltage control. In the present invention, the master control unit 18 also includes

circuitry for monitoring the operating characteristics of the processor.” *Id.* at p. 5, ll. 10-14.

148. As described in the ’443 Patent and understood by a POSITA, slack in processing “indicates that [a] previous operation completed earlier than necessary.” Ex. 1001 at 11:28-29. In other words, as I also explain in the Background of the Technology Section III(A)(3), the difference in computing time between the slowest dependency (e.g., the critical path) and a different dependency within an operation defines the slack that dependency has. *See* Ex. 1018 at 1, item (57) and 2:16-22. Slack helps to determine operations that are completing faster than needed so a user can reduce the power provided to that operation, thus increasing the completion time (and reducing the slack). *Id.* With this in mind, *Halepete* discloses determining “when the **operating characteristics of the central processor are significantly different than required by the operations being conducted** (Figure 2 increase and decrease frequency and voltage conditionals), **and changing the operating characteristics of the central processor to a level commensurate with the operations being conducted** (Figure 2 increase and decrease frequency and voltage steps).” Ex. 1005 at p. 1, item (57), emphases added. Thus, a POSITA would have recognized that *Halepete* is directed to a method of sensing computing needs for individual dependencies and consequently changing the frequency and voltage to an

individual dependency to provide a better power efficiency (e.g., *Halepete* is directed to determining a slack).

149. With reference to *Halepete*, “[t]he core frequency for the processing unit 16 is generated by multiplying the slow clock by a factor. This factor is computed by the control software of the present invention which monitors the operation of the processor to determine from the characteristics of the processor just what frequency should be selected.” *Id.* at p. 7, ll. 1-5. The system is capable of determining a certain frequency that is needed at a certain time for system operations. *Id.* at p. 7, ll. 8-25. The PLL provides a clock frequency that is then divided by a “plurality of different values determined by the control software, [such that] the operating frequencies for the different components of the system may be individually controlled and furnished to other components of the processor without the necessity of crossing chip boundaries with the consequent slowing caused by negotiating the boundaries.” *Id.* at p. 8, ll. 11-15.

150. Not only does *Halepete* describe a system that can select an operating frequency depending on the operations being performed, the system can also determine and select an appropriate voltage level. Specifically, *Halepete* explains that if a processor is spending “more than a preselected increment of its operation in” halted states “while operating at normal frequency and voltage, then power is being wasted.” *Id.* at p. 11, ll. 1-5. “The **detection of such operating characteristics**

therefore may indicate that the **frequency and voltage of operation should be reduced.**” *Id.* at p. 11, ll. 5-7, emphases added. The control software “detects operating characteristics and determines whether those characteristics indicate that the frequency and voltage of operation should be changed.” *Id.* at p. 11, ll. 14-16. In this way, the processor of *Halepete* is programmed to determine a discrepancy between necessary operating power and current operating power (e.g., slack) and to reduce the clock frequency and the voltage when that discrepancy indicates too much operating power is being provided.

151. If necessary, in *Halepete*, “the control software causes the voltage to be lowered to the calculated value.... At that point, the control software begins again to monitor the various conditions controlling the frequency and voltage of operation.” *Id.* at p. 15, ll. 6-12. As I have discussed in the Background of the Technology at Section III(A)(3), a POSITA at the time of invention would have understood the common practice of providing a dynamically changing frequency and voltage value to a microprocessor depending on the current operation needs of the microprocessor. Specifically, *Childers* describes “a technique for adjusting supply voltage and frequency at run-time to save energy” and provides the equation for power consumption for CMOS (complementary metal-oxide semiconductor – an extremely common semiconductor technology for integrated circuits) with the equation: $P_{avg} = \alpha_T \times f_{CLK} \times C_{load} \times V_{DD}^2$ where P_{avg} is the power consumption, f_{CLK}

is the clock frequency, and V_{dd} is the supply voltage. Ex. 1021 at Abstract and Section 2 respectively.

152. Moreover, AMD's "PowerNow!" function allowed for an automatic mode which could "adjust the clock frequency and voltage of the processor according to the demands of the applications being run while optimizing for battery life." Ex. 1020 at p. 1; *see also* Ex. 1019 at p. 2 ("Instead of constantly running a CPU at its maximum frequency, PowerNow! allows the CPU to dynamically adjust its operating frequency according to the needs of the tasks that the CPU is running. ... As we should all know by now, lower clocked processors don't always require that the same amount of voltage be supplied to them as those with higher operating frequencies. It would thus only make sense that as the clock frequency of the processor is varying that its core voltage should vary as well, which is exactly what PowerNow! does.")

153. Accordingly, a POSITA would have been well aware of the ability to dynamically change both clock frequency and voltage in a unit of a microprocessor depending on the operations being performed. A POSITA would have found it obvious to combine the control software capable of determining necessary clock frequency and voltage levels and consequently adjusting the clock frequency and voltage level taught by *Halepete* with the microprocessor including the plurality of loads taught by *Shenai*. *Halepete* describes different components of the processor

operating at different frequencies depending on the operations they perform. Ex. 1005 at 7:27-8:15. A POSITA would have appreciated the immense benefits from using software as suggested by *Halepete* to allow a microprocessor to be dynamically controlled and updated in such a way.

154. A POSITA would have been motivated, prior to the time of the invention, to combine the multi-load microprocessor of *Shenai* with the control software of *Halepete* as it would have been nothing more than a combination of prior art elements according to known methods to yield predictable results, and, accordingly, there is a reasonable expectation of success when combining the references. For example, *Shenai* already explains that “controller 450 may comprise software instructions for determining the voltage, current and frequency targets[.]” Ex. 1004 at [0026]. It would have been a simple software design choice to modify the software of *Shenai*’s controller to include the control software of *Halepete* in order to allow *Shenai*’s microprocessor to dynamically control frequencies and voltages of its loads, in the manner described in *Halepete*. As I discussed, *Shenai*’s sensing circuits “determine a number of logic transitions in a predetermined time period.” *Id.* at [0030]. A POSITA would have known to modify *Shenai*’s controller to include the control software of *Halepete* to yield predictable dynamic adjustments of load frequencies and voltages based on the logic transaction information already determined by *Shenai*’s sensing circuits.

155. Indeed, a POSITA would have recognized and appreciated that the dynamic control over frequency and voltage the *Halepete* control software provides would greatly reduce thermal output, greatly increase battery life, and provide overall system improvements to the microprocessor without otherwise impinging the operation of *Shenai*. Therefore, *Shenai* in view of *Halepete* renders obvious the microprocessor of claim 1, wherein the microprocessor is programmed to determine a slack in processing in one of the domains and to reduce the clock frequency and the voltage in said one of the domains to reduce the slack.

2. Claim 9

(a) 9[P]. The method of claim 8, wherein step (e) comprises:

156. For the reasons I have detailed above in reference to Claim 8 at Section III(F)(5), *Shenai* renders obvious the method of claim 8.

(b) [9(a)] (i) determining a slack in processing in one of the domains; and

157. I have previously explained why *Shenai* in view of *Halepete* renders obvious a microprocessor that is programmed to determine a slack in processing in one of the loads in reference to Claim 4 at Section III(G)(1). Thus, for the same reasons, *Shenai* in view of *Halepete* renders obvious determining a slack in processing in one of the domains.

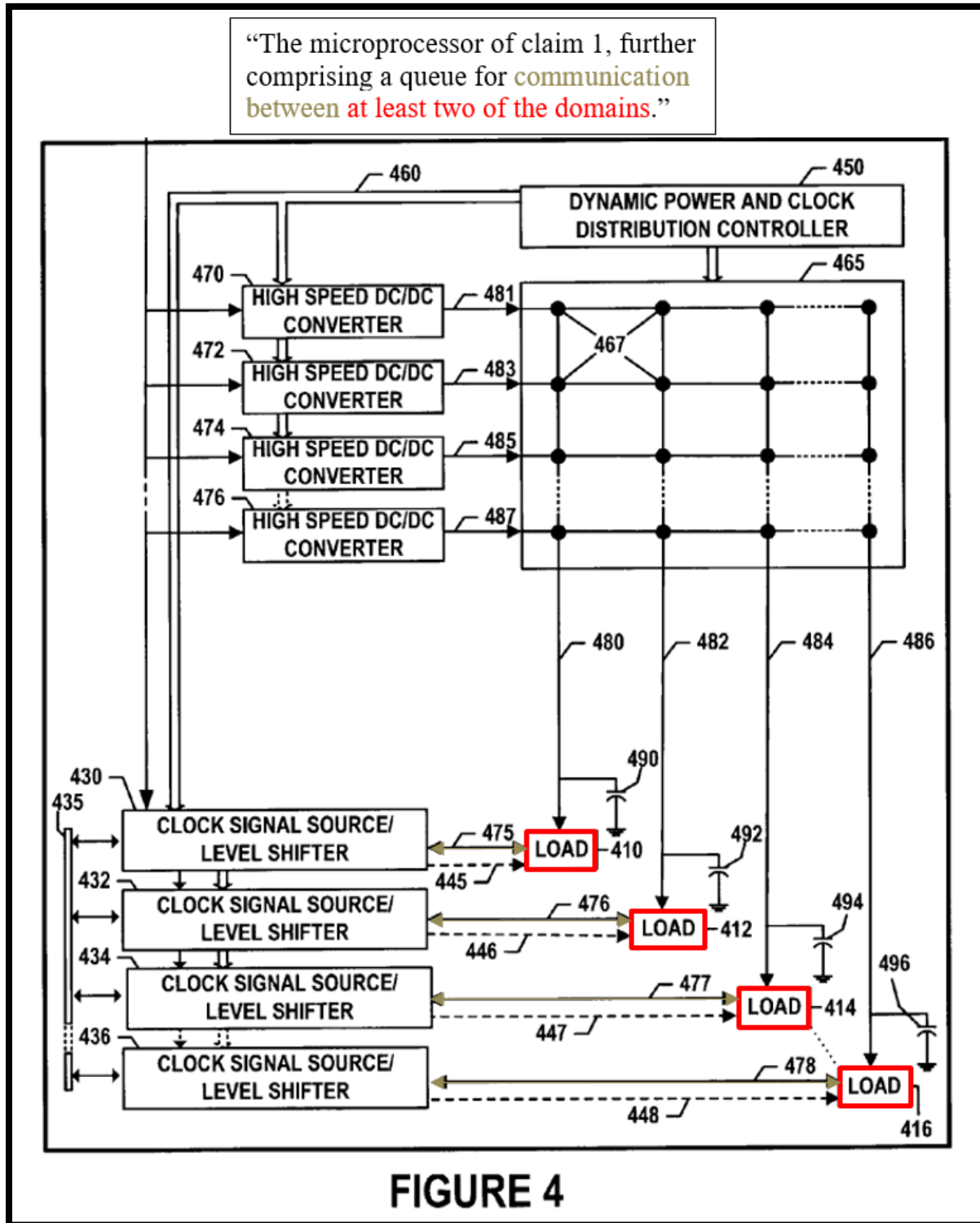
(c) [9(b)] (ii) reducing the clock frequency and the voltage in said one of the domains to reduce the slack.

158. I have previously explained why *Shenai* in view of *Halepete* renders obvious a microprocessor that is programmed to determine a slack in processing in one of the loads in reference to Claim 4 at Section III(G)(1). Thus, for the same reasons, *Shenai* in view of *Halepete* renders obvious reducing the clock frequency and the voltage in said one of the domains to reduce the slack.

H. Ground 3: Claims 5, 6, 7, 10, and 11 are obvious over *Shenai* in view of *Sherburne*

1. Claim 5 – The microprocessor of claim 1, further comprising a queue for communication between at least two of the domains.

159. For the reasons I have detailed above in reference to Claim 1 at Section III(F)(1), *Shenai* renders obvious the microprocessor of claim 1. The '443 Patent describes a “queue” structure that asserts a FULL flag to assert that a producer “can no longer write to the queue until the flag is deasserted” and an EMPTY flag to assert “that there is no valid data [] to read from the queue.” Ex. 1001 at 6:54-60. *Shenai* discloses intercommunication between loads. For example, *Shenai* states “**clock/shifters 430-436 may also include circuitry that allows electrical signal communication between loads** operating at varying target voltages via signal buses 475, 476, 477 and 478. Such an approach may improve the noise tolerance of such electrical signal communication.” Ex. 1004 at [0035], emphasis added. I have provided an annotated version of Figure 4 below to further illustrate the buses 475, 476, 477, and 478 allowing for communication.



Reproduced from Shenai (Excerpted and Annotated)

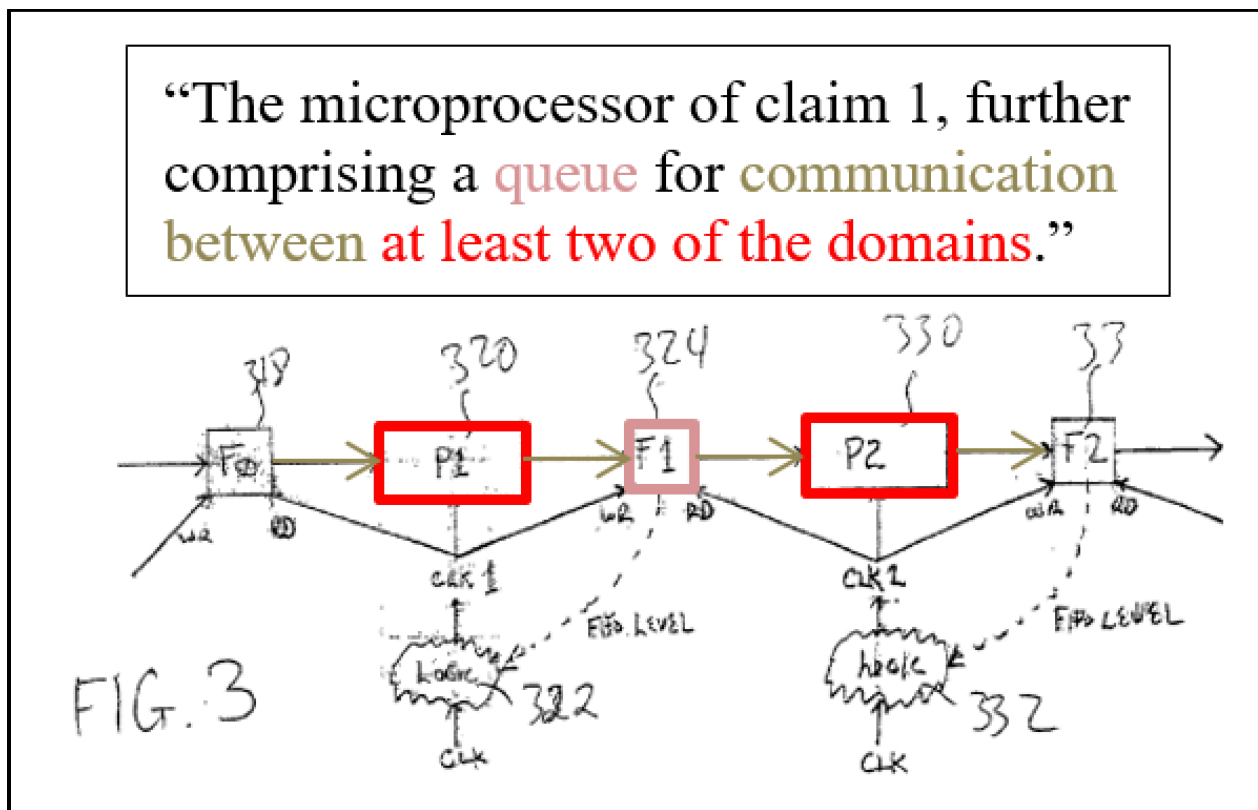
Id. at p. 5, excerpted and annotated.

160. To the extent it is argued that *Shenai* does not specify how this communication is implemented, as I discuss above in the Background of the Technology at Section III(A)(2), the use of a queue would have been obvious to a POSITA. A POSITA would have understood the use of queue structures for inter-domain communication was well-known at the time of invention as it is one of the most common communication mechanisms in microprocessors. A POSITA would have also appreciated using an effective, well-known microprocessor component in a similar microprocessor to allow inter-domain communication in the same way as known in the art. *See* Ex. 1015 at p. 1, 2; *see also* Ex. 1016 at p. 11, 12, 24. For these reasons, a POSITA would have been motivated to combine prior art elements (e.g., the inter-domain communication taught in *Shenai* with the queue structure known in the art) according to known methods to yield predictable results. A POSITA would have further found this obvious in view of the teachings of *Sherburne*.

161. *Sherburne* discloses a first-in-first-out (“FIFO”) data buffering queue element placed between functional units (e.g., the claimed “domains” or *Shenai*’s loads). As a note, while most of *Sherburne*’s disclosure describes a FIFO between processors, *Sherburne* clearly states “the notions of ‘FIFO’ and ‘processor’ can be expanded to include other types of functional blocks and units.” Ex. 1006 at [0069]. Thus, as would have been well understood by a POSITA and as explicitly stated in

Sherburne, I have analyzed the disclosure by using a plurality of functional units instead of a plurality of processors.

162. Buffers were well-known components in the field of microprocessors and were often arranged such that “a data processing unit [] is fed data through a data buffering element (such as a first-in-first-out (FIFO)) and which outputs data to another data buffering element.” *Id.* at [0004]. *Sherburne* illustrates the FIFO buffer unit being placed between two functional units in Figure 3. I have further annotated and provided an excerpt of Figure 3 below:



Reproduced from *Sherburne* (Excerpted and Annotated)

Id. at p. 4, excerpt and annotated.

163. With reference to Figure 3, *Sherburne* discloses:

Turning now to FIG. 3, an example with multiple processors and multiple FIFO units and pseudocode is discussed next. Similar to FIG. 2, the processor 320 receives its clock from a controller 322 and data from a FIFO 318. A master clock signal is provided to the controller 322. A FIFO 324 accepts data generated by the processor 310. The data is gated by a write signal from the controller 322, and the FIFO provides a FIFO fill level feedback signal to the controller 322 such as FIFO_FULL, FIFO_EMPTY, or in between, for example. Based on the FIFO fill level feedback signal, the controller 322 can vary the clock signal to the processor 320 and the FIFOs 318 and 324 to increase or decrease the processing speed of the processor 320, thereby adjusting the read rate from the FIFO 318 and the fill rate to the FIFO 324.

Id. at [0031].

164. *Sherburne* also explains that the “output of the buffer 324 is provided to a processor 330, which receives its clock from a controller 332.” *Id.* at [0029]. Buffer 334 then “accepts data generated by the processor 330.” *Id.* With *Sherburne*’s explicit teachings of a buffer to help facilitate communication between separate functional units, a POSITA would have found it obvious to incorporate the buffer described in *Sherburne* with the multi-load microprocessor described in *Shenai*. As

previously explained, implementing FIFOs or other buffers to act as a queue between functional units was well known in the art.

165. *Shenai* is directed to “power supply systems and, more particularly, to frequency and voltage tuning of distributed power supply systems” and describes “approaches for balancing power consumption reduction and performance.” Ex. 1004 at [0002], [0004]. Similarly, *Sherburne* is directed to “power clocking systems and methods” where “power can be saved by varying the clock frequency, the core voltage or a combination thereof, if necessary, to reduce heat or to reduce battery power consumption.” Ex. 1006 at p.1, item (54), [0021]. Therefore, *Shenai* and *Sherburne* are in the same field of endeavor and a POSITA would have been motivated to modify *Shenai* to realize improvements based on the disclosure of *Sherburne*.

166. For example, a POSITA would have appreciated using a buffer element to receive and store read and write communications, as discussed in *Sherburne*, between loads 410-416 of *Shenai*. See Ex. 1004 at [0035] (“clock/shifters 430-436 may also include circuitry that allows electrical signal communication between loads operating at varying target voltages via signal buses 475, 476, 477 and 478. Such an approach may improve the noise tolerance of such electrical signal communication.”) To the extent it is argued that *Shenai* alone does not disclose or render obvious details of the electrical signal communication between loads, a

POSITA would have understood that such communication would have been implemented in accordance with techniques known in the art, such as those provided in *Sherburne*. A POSITA would have understood the advantages well-known in the art at the time of invention for implementing a queue to facilitate the communication between separate domains. As discussed in *Sherburne*, such advantages include, for example, “to reduce or balance power consumption[,]” to “reduce clock rate, or even stop the clock, for localized portions of [a] system[,]” to dynamically control a system, among other advantages. Ex. 1006 at [0014]. Thus, a POSITA would have been motivated to combine prior art elements (e.g., the inter-domain communication taught in *Shenai* with the FIFO buffer elements taught in *Sherburne*) according to known methods to yield predictable results with a reasonable expectation of success. For these reasons, *Shenai* in view of *Sherburne* renders obvious the microprocessor of claim 1, further comprising a queue for communication between at least two of the domains.

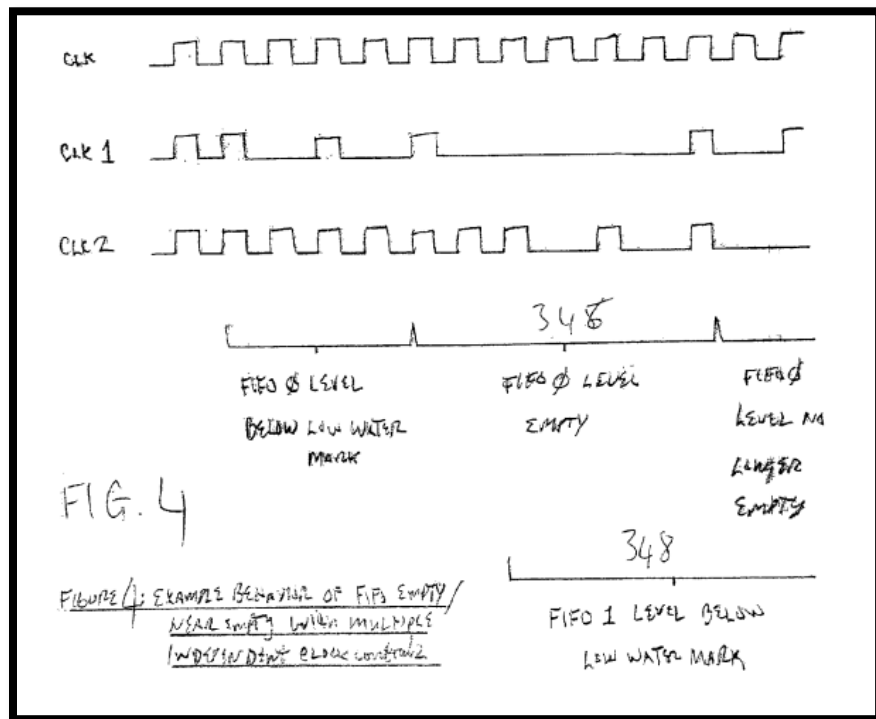
2. Claim 6

(a) 6[P]. *The microprocessor of claim 5,*

167. For the reasons I have detailed above in reference to Claim 5 at Section III(H)(1), *Shenai* in view of *Sherburne* renders obvious the microprocessor of claim 5.

(b) [6(a)] *wherein the queue has a Full flag and an Empty flag, and*

168. *Sherburne* discloses a “BUFFER_FULL” flag (e.g., a Full flag) and “BUFFER_EMPTY” flag (e.g., an Empty flag) for each buffer (e.g., queue). Ex. 1006 at [0028]. *Sherburne* also discloses each buffer including a high water mark and a low water mark. Figure 4 provides an illustration of the clock rate when a FIFO element produces a low water mark or empty flag.



Reproduced from *Sherburne* (Excerpted)

Id. at p. 5, excerpted. “FIG. 4 shows an example of clock behavior including clock rate reduction during FIFO empty condition. In period 344, the FIFO 318 is below its low water mark and in period 346, the FIFO 318 is empty. Eventually, the processor 320 runs out of work and is shut down to reduce power consumption. Since the processor 330 is still running, eventually, the FIFO 324’s low water mark

level is reached, and the controller 332 reduces the clock rate for the clock CLK2.”
Id. at [0039].

169. The FIFO provides a “FIFO fill level feedback signal to the controller 312 such as FIFO_FULL, FIFO_EMPTY[.]” *Id.* at [0022]. Similarly, a buffer provides a “buffer fill level feedback signal to the controller 332 such as BUFFER_FULL, BUFFER_EMPTY[.]” *Id.* at [0029]. The buffer can have a high water mark that defines the buffers as nearly full or full and a low water mark for when the buffer is nearly empty or empty. *Id.* at [0030] and [0040] respectively. It should be easily understood that the FIFO_FULL flags or BUFFER_FULL flags are considered Full flags while the FIFO_EMPTY flags or the BUFFER_EMPTY flags are considered Empty flags.

170. Flags have been used in computing logic and programming well before the time of the '443 Patent. A POSITA would have been motivated to improve similar communication between functional units in a microprocessor in the same way as taught by *Sherburne* by enabling the microprocessor of *Shenai* to include a queue that has a Full flag and an Empty flag. Since queue structures and flag values were well known and conventional prior to the time of the '443 Patent, as provided in *Sherburne* and as I discuss in the Background of the Technology at Section III(A)(2), there would have been a reasonable expectation of success implementing the queue structure with flag values in *Shenai*'s microprocessor. *See* Ex. 1015 at p.

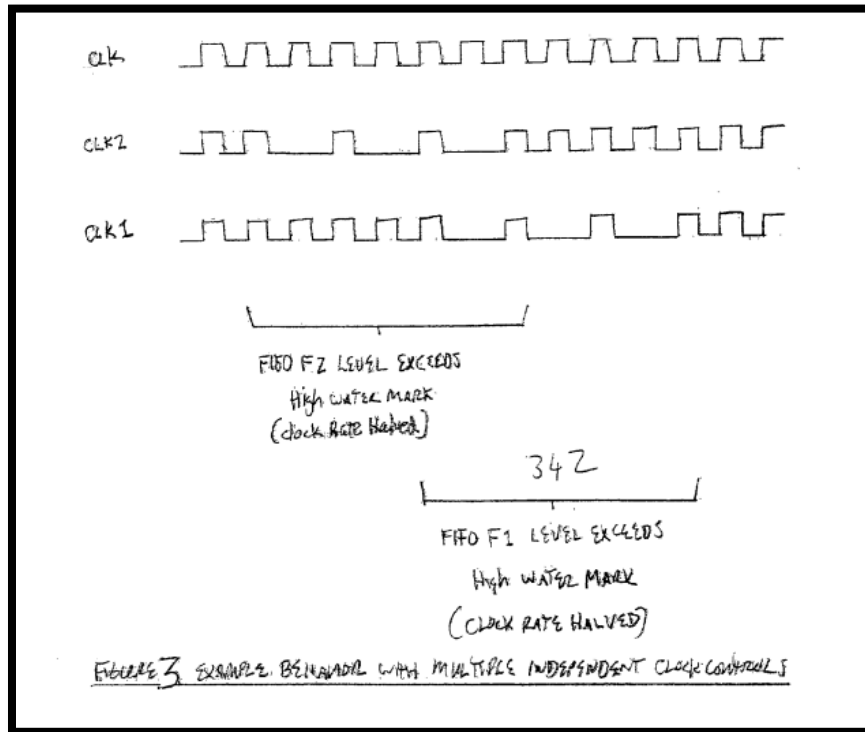
1, 2; *see also* Ex. 1016 at p. 11, 12, 24. Implementing *Sherburne*'s queue structure in *Shenai*'s microprocessor structure would have been nothing more than combining prior art elements according to known methods to yield predictable results with an expectation of success. A POSITA would have been motivated to combine the queue of *Sherburne* that includes the Full and Empty flags with the multi-load microprocessor of *Shenai* as I have explained above in Section III(H)(1). Thus, *Shenai* in view of *Sherburne* renders obvious wherein the queue has a Full flag and an Empty flag.

- (c) [6(b)] *wherein the microprocessor is programmed to prevent a write to the queue when the Full flag is asserted, until the Full flag is deasserted; and.*
- (d) [6(c)] *to prevent a read from the queue when the Empty flag is asserted, until the Empty flag is deasserted.*

171. Because Claim limitations 6(b) and 6(c) are highly related, I have decided to provide my analysis for both claim limitations in the same section. Thus, the discussion I provide below is meant to apply to both 6(b) and 6(c).

172. *Sherburne* discloses the microprocessor is programmed to prevent a write to the queue when the Full flag is asserted, until the Full flag is deasserted and to prevent a read from the queue when the Empty flag is asserted, until the Empty flag is deasserted. For example, *Sherburne* discloses “slowing down or stopping the clock if the second buffer is above its high water mark or if the second buffer is full” and shows a clock providing write data to a buffer at Figure 3, and discloses “if the

FIFO is still empty, the processor clock may be reduced to a low rate or zero” and shows a clock providing read data to buffer in Figure 3. Ex. 1006 at [0013] and [0035] respectively.



Reproduced from *Sherburne* (Excerpted)

Id. at p. 5, excerpted. “Turning now to FIG. 3, an example with multiple processors and multiple FIFO units and pseudocode is discussed next. Similar to FIG. 2, the processor 320 receives its clock from a controller 322 and data from a FIFO 318. A master clock signal is provided to the controller 322. A FIFO 324 accepts data generated by the processor 310. The data is gated by a write signal from the controller 322, and the FIFO provides a FIFO fill level feedback signal to the controller 322 such as FIFO_FULL, FIFO_EMPTY, or in between, for example.

Based on the FIFO fill level feedback signal, the controller 322 can vary the clock signal to the processor 320 and the FIFOs 318 and 324 to increase or decrease the processing speed of the processor 320, thereby adjusting the read rate from the FIFO 318 and the fill rate to the FIFO 324.” *Id.* at [0031].

173. To keep the buffers from overflowing, “the clock rate to [the] data source may be reduced” or stop when the buffer nears the full condition. *Id.* at [0023]. *Sherburne* discloses that the system is capable of preventing further writes to a buffer that has been designated as full. For example, *Sherburne* explains that, if the buffer nears full, “as defined by some ‘high water’ mark,” or if the buffer is full, “the clock rate to [the] processor ... may be reduced to ... zero.” *Id.* at [0030]. Claim 12 of *Sherburne*, as was in the published application on November 11, 2002, states “slowing down or stopping the clock if the second buffer is above its high water mark or if the second buffer is full.” *Id.* at p. 16.

174. *Sherburne* also explains the system is capable of preventing further reads to a buffer that has been designated as empty as the system can conserve power “when the FIFOs approach their empty condition.” *Id.* at [0035]. This is because, during “periods of FIFO empty condition, the units it feeds may have little or no computation to perform. Therefore a given system design may be amenable to reduced clock rate in presence of low or zero data input rate.” *Id.* *Sherburne* further states: “Once the source FIFO is empty, **assume the last data read** will be subject

to processing and later written out to the next FIFO after the processor.” *Id.*, emphasis added. Claim 13 of *Sherburne*, as was included in the published application on November 11, 2002, states “slowing down or stopping the clock if the first buffer is below its low water mark or if the first buffer is empty.” *Id.* at p. 16.

175. As I have detailed in this section, *Sherburne*’s queue structure includes computing logic that prevents a write when a full flag is asserted until it is deasserted and prevents a read when an empty flag is asserted until it is deasserted. For the same reasons as explained for Claim 5 at Section III(H)(1) and Claim limitation 6(a) at Section III(H)(2)(b), it would have been obvious to a POSITA to implement *Sherburne*’s queue structure, including its computing logic, in *Shenai*’s multi-load microprocessor structure as *Shenai*’s microprocessor structure already includes computing logic to facilitate communication between domains. Ex. 1004 at [0035]. Such a combination would have been nothing more than a combination of prior art elements according to known methods (e.g., *Sherburne*’s queue structure with *Shenai*’s microprocessor structure including computing logic to facilitate communication between domains) to yield predictable results (e.g., to prevent a write when a full flag is asserted until it is deasserted and prevent a read when an empty flag is asserted until it is deasserted) having a reasonable expectation of success. Accordingly, for these reasons and the reasons explained previously, *Shenai*

in view of *Sherburne* renders obvious wherein the microprocessor is programmed to prevent a write to the queue when the Full flag is asserted, until the Full flag is deasserted; and to prevent a read from the queue when the Empty flag is asserted, until the Empty flag is deasserted.

3. Claim 7 – The microprocessor of claim 6, wherein the queue is implemented as a dual-ported SRAM.

176. For the reasons I have detailed above in reference to Claim 6 at Section III(H)(2), *Shenai* in view of *Sherburne* renders obvious the microprocessor of claim 6.

177. *Sherburne* discloses the buffer (e.g., the claimed queue) implemented using a “dual port RAM.” For example, *Sherburne* states the buffer “is a first-in, first-out memory circuit (hereinafter FIFO memory) using a dual port RAM.” Ex. 1006 at [0026]. As I discuss in the Background of the Technology Section III(A)(1), a POSITA would have understood that the recited dual-ported SRAM is a type of the dual port RAM taught by *Sherburne*. See Ex. 1026 at 5-67 (titled “**3200DX Dual-Port Random Access Memory (RAM)**” which references its 3200DX product as “dual-port SRAM” which “offers dual-port SRAM capable of supporting a system speed of 100 MHz[,],” emphasis added.) As I also discuss in the Background of the Technology Section III(A)(1), it was known in the art that the “RAM family includes two important memory devices: static RAM (SRAM) and dynamic RAM (DRAM).” Ex. 1027 at p. 2. Accordingly, a POSITA would have understood that, based on

Sherburne's dual port RAM, that selecting a dual-ported SRAM would have been a simple design choice from a limited number of memory options in the RAM family.

178. Thus, a POSITA would have recognized an SRAM (e.g., a specific type of RAM) could be used to implement the FIFO buffer described in *Sherburne*. The use of SRAM in microprocessors has been well known and conventional prior to the '443 Patent, as I discuss in the Background of the Technology at Section III(A)(1). *Sherburne* expressly discloses the buffer being implemented as a "dual port RAM[.]" Ex. 1006 at [0027]. *Shenai* also discloses a subsystem of its microprocessor being "cache memory" (see Ex. 1004 at [0025]) which is a type of volatile memory just like RAM (e.g., SRAM). Importantly, as I discuss in Background of the Technology at Section III(A)(1), dual-port RAM is typically used in systems that need high-performance computing or where fast and simultaneous access to memory is required, like a multi-domain processor, since it has two independent access ports (hence dual-ported) to allow for simultaneous read and write operations from different parts of the memory. Multi-domain microprocessors often use dual-ported RAM to allow more than one domain to access the memory simultaneously so it can execute functions. *Sherburne* further explains that the dual port RAM can be used in a multi-state read/write system as its circuit "recognizes the state of the dual port RAM according to the data write signal, the data read signal, the write address signal and the read address signal." Ex. 1006 at [0027].

179. As I discussed above, *Shenai* is directed to “power supply systems and, more particularly, to frequency and voltage tuning of distributed power supply systems” and describes “approaches for balancing power consumption reduction and performance.” Ex. 1004 at [0002], [0004]. Similarly, *Sherburne* is directed to “power clocking systems and methods” where “power can be saved by varying the clock frequency, the core voltage or a combination thereof, if necessary, to reduce heat or to reduce battery power consumption.” Ex. 1006 at p. 1, item (54), [0021]. Therefore, *Shenai* and *Sherburne* are in the same field of endeavor and a POSITA would have been motivated to modify *Shenai* to realize improvements based on the disclosure of *Sherburne*.

180. In this way, *Shenai*’s microprocessor would have benefited from the implementation of a dual-port RAM buffer for the same reasons as *Sherburne*. For example, *Shenai*’s microprocessor would have benefited from using a dual-port RAM when implementing multi-state read/write operations as described in *Shurburne*. *Id.* at [0027]. Therefore, a POSITA would have been motivated to use the known technique of implementing a dual-ported SRAM queue, as obvious in view of *Sherburne*, as a way to optimize communication between domains of the microprocessor of *Shenai* in the same way. Since queue structures and dual-ported SRAM were well known and conventional prior to the ’443 Patent, there would have been a reasonable expectation of success implementing the dual-ported SRAM

queue of *Sherburne* (obvious in view of the dual port RAM explicitly disclosed in *Sherburne*) in *Shenai*'s microprocessor. Implementing such a dual-ported SRAM queue in *Shenai*'s microprocessor structure would have been nothing more than combining prior art elements according to known methods to yield predictable results.

181. Thus, *Shenai* in view of *Sherburne* renders obvious the microprocessor of claim 6, wherein the queue is implemented as a dual-ported SRAM.

4. Claim 10 – The method of claim 8, wherein step (d) comprises providing a queue for communication between at least two of the domains.

182. I have previously explained why *Shenai* in view of *Sherburne* renders obvious a microprocessor further comprising a queue for communication between at least two of the domains in reference to Claim 5 at Section III(H)(1). I have also previously explained why *Shenai* teaches the method of claim 8 at Section III(F)(5). Thus, for the same reasons, *Shenai* in view of *Sherburne* renders obvious the method of claim 8, wherein step (d) comprises providing a queue for communication between at least one of the domains.

5. Claim 11

- (a) 11[P]. The method of claim 10,

183. For the reasons I have detailed above in reference to Claim 10 at Section III(H)(4), *Shenai* in view of *Sherburne* renders obvious the method of claim 10.

- (b) *[11(a)] wherein the queue has a Full flag and an Empty flag, and wherein step (d) further comprises:*

184. I have previously explained why *Shenai* in view of *Sherburne* renders obvious a microprocessor further comprising a queue, wherein the queue has a Full flag and an Empty flag in reference to Claim limitation 6(a) at Section III(H)(2)(b). Thus, for the same reasons, *Shenai* in view of *Sherburne* renders obvious *wherein the queue has a Full flag and an Empty flag.*

- (c) *[11(b)] preventing a write to the queue when the Full flag is asserted, until the Full flag is deasserted; and*
(d) *[11(c)] preventing a read from the queue when the Empty flag is asserted, until the Empty flag is deasserted.*

185. Because Claim limitations 11(b) and 11(c) are highly related, I have decided to provide my analysis for both claim limitations in the same section. Thus, the discussion I provide below is meant to apply to both 11(b) and 11(c).

186. I have previously explained why *Shenai* in view of *Sherburne* renders obvious a microprocessor programmed to prevent a write to the queue when the Full flag is asserted, until the Full flag is deasserted and to prevent a read from the queue when the Empty flag is asserted, until the Empty flag is deasserted in reference to Claim limitations 6(b) and 6(c) at Section III(H)(2)(d). Thus, for the same reasons, *Shenai* in view of *Sherburne* renders obvious *preventing a write to the queue when the Full flag is asserted, until the Full flag is deasserted; and preventing a read from the queue when the Empty flag is asserted, until the Empty flag is deasserted.*

I. Ground 4: Claim 7 is obvious over *Shenai* in view of *Sherburne* and in view of *Traylor*

1. *Claim 7 – The microprocessor of claim 6, wherein the queue is implemented as a dual-ported SRAM.*

187. For the reasons I have detailed above in reference to claim 6 at Section III(H)(2), *Shenai* in view of *Sherburne* renders obvious *the microprocessor of claim 6*. *Sherburne* discloses the buffer (e.g., the claimed *queue*) as “dual port RAM[.]” To the extent it is argued that *Sherburne* does not explicitly disclose the buffer being a *dual-ported SRAM*, *Sherburne* states the buffer “is a first-in, first-out memory circuit (hereinafter FIFO memory) using a dual port RAM.” Ex. 1006 at [0026]. In Section III(H)(3) above, I discuss why a queue implemented as a *dual-ported SRAM* would have been obvious to a POSITA in view of the disclosure of *Sherburne*. Additionally, a POSITA would have found the teachings of a *dual-ported SRAM* obvious in view of *Traylor*. For example, as I discuss in the Background of the Technology at Section III(A)(1), it was known in the art that the “RAM family includes two important memory devices: static RAM (SRAM) and dynamic RAM (DRAM).” Ex. 1027 at p. 2. Accordingly, a POSITA would have understood that selecting a dual-ported SRAM would have been a simple design choice from a limited number of memory options in the RAM family.

188. *Traylor* discloses a queue buffer substantially similar to *Sherburne*. Just like *Sherburne*, the queue of *Traylor* is implemented as a FIFO with an “EMPTY

signal” and a “FULL signal[.]” Ex. 1007 at 1:39-50. The read counter and the write counter are “coupled to a **two-port Static Random Access Memory (SRAM) 330**.” *Id.* at 4:59-61, emphasis added. “The SRAM 330 is the memory device which stores data in the FIFO.” *Id.* at 4:61-62. In the prior art section, *Traylor* explains that: “Generally, a FIFO is comprised of a memory device, e.g. **a Static Random Access Memory (SRAM)**, and FIFO controller.” *Id.* at 1:19-21, emphasis added. Thus, A POSITA would also recognize that *Sherburne* and *Traylor* are in the same field of endeavor (e.g., buffering data). In view of the above, a POSITA would have been well aware of using a dual-port SRAM for a queue structure such as a FIFO.

189. Based on the teachings of *Traylor*, it would have been obvious to a POSITA to similarly configure *Shenai*’s microprocessor architecture to include a buffer (e.g., queue) as described in *Sherburne* and *Traylor*. Moreover, it would have been obvious to a POSITA to implement the queue as a two-port SRAM (e.g., dual-ported SRAM) as described in *Traylor*. Both *Traylor* and *Sherburne* describe FIFO elements that provide buffer queues between functional units. In both references, as I generally discuss in reference to Claim 6 at Section III(H)(2) and above in this Section III(I)(1), a Full and an Empty flag is provided to improve the performance of the FIFO element. Additionally, while *Sherburne* describes the FIFO buffers embodied as a dual-port RAM device, *Traylor* describes the FIFO buffers embodied as a two-port SRAM device.

190. Thus, a POSITA would have recognized an SRAM (e.g., a specific type of RAM) could be used to implement the FIFO buffer described in *Sherburne* as taught by *Traylor*. As is well-known in the art and described in *Traylor*, SRAM provides faster access times and simpler control mechanisms, making it much more suitable for high-speed buffering. Ex. 1007 at p. 1, item (57). The use of SRAM in microprocessors has been well known and conventional prior to the '443 Patent, as I discuss in the Background of the Technology at Section III(A)(1). *Sherburne* expressly discloses the buffer being implemented as a “dual port RAM[.]” Ex. 1006 at [0027]. *Shenai* also discloses a subsystem of its microprocessor being “cache memory” which is a type of volatile memory just like RAM (e.g., SRAM). Ex. 1004 at [0025]. Importantly, as I discuss in the Background of the Technology at Section III(A)(2), dual-port RAM is typically used in systems that need high-performance computing or where fast and simultaneous access to memory is required, like a multi-domain processor, since it has two independent access ports (hence dual-ported) to allow for simultaneous read and write operations from different parts of the memory. Multi-domain microprocessors often use dual-ported RAM to allow more than one domain to access the memory simultaneously so it can execute functions.

191. In this way, *Shenai*'s microprocessor would have benefited from the implementation of a dual-ported SRAM buffer, as explicitly disclosed in *Traylor*,

for the same reasons as *Sherburne*. Incorporating such a dual-ported SRAM buffer would allow, for example, “concurrent reading and writing” operations. Ex. 1007 at 4:64-65. Therefore, a POSITA would have been motivated to use the known technique of implementing a dual-ported SRAM queue, as explicitly disclosed in *Traylor*, as a way to optimize communication between domains of the microprocessor of *Shenai* in the same way. Since queue structures and dual-ported SRAM were well known and conventional prior to the ’443 Patent, there would have been a reasonable expectation of success implementing the *Traylor*-modified dual-ported SRAM queue of *Sherburne* in *Shenai*’s microprocessor. Implementing *Traylor*’s dual-ported SRAM queue in *Shenai*’s microprocessor structure would have been nothing more than combining prior art elements (e.g., *Traylor*’s dual-ported SRAM queue) according to known methods (as described in *Sherburne* and *Traylor*) to yield predictable results with a reasonable expectation of success. Thus, *Shenai* in view of *Sherburne* and in view of *Traylor* renders obvious the microprocessor of claim 6, wherein the queue is implemented as a dual-ported SRAM.

J. Ground 5: Claims 1, 3, 8, and 12 are obvious in view of Georgiou

1. Claim 1

- (a) *I[P]. A multiple clock domain microprocessor comprising:*

192. *Georgiou* discloses a plurality of functional units operating at independent frequencies (e.g., the recited multiple [/] domain[s/]) as components of a microprocessor (e.g., the recited microprocessor). In general, *Georgiou* is directed to the architecture and circuitry of a “superscalar microprocessor.” Ex. 1008 at 3:51-52. More specifically, *Georgiou* describes a “system and method for cooperatively varying the voltage and operating frequency of a functional unit in a multi-functional unit processor such as a superscalar microprocessor” where the functional units may be “fixed-point units, floating point units, load/store units, and branch units found in typical general purpose and superscalar microprocessors.” *Id.* at 3:49-63.

193. *Georgiou* discloses a clock selector that is associated with a “particular functional unit” to provide a clock signal and voltage for that functional unit. *Id.* at 8:37-67. “The decoder 460 decodes the signal 270 and outputs a clock select signal 465 to a select input (S) to the multiplexer associated with the particular functional unit. The clock select signal 465 is used to select the clock frequency corresponding to the voltage output by voltage regulator 330 according to signal 270.” *Id.* Specifically, the multiplexers 470 of clock selector 430 are associated with each “independently controllable functional unit” such that “each functional unit may be operating under a different voltage 325 and frequency 425 combination according to the thermal feedback from its associated thermal sensor 119.” *Id.* at 5:2-6.

Accordingly, the plurality of multiplexers 470 provide independent respective clocks for the recited multiple clock domain microprocessor.

194. Examples of functional units are provided in *Georgiou*, including “floating point unit, multiple load/store and fixed point units, and a branch execution unit” *Id.* at 4:52-54. Moreover, the ’443 Patent provides examples of domains that are the same as the examples of functional units provided in *Georgiou*. The ’443 Patent describes a microprocessor that includes an “integer issue/execute 120” domain, a “floating point issue/execute 130” domain, and a “load/store issue/execute 140” domain. Ex. 1001 at 6:4-8. *Georgiou* explicitly states the functional units can be a “floating point unit” (e.g., the floating point issue/execute 130 domain described in the ’443 Patent) or “multiple load/store and fixed point units” (e.g., load/store issue/execute 140 domain described in the ’443 Patent). Ex. 1008 at 4:52-54. Clearly, a POSITA would have understood that the functional units described in *Georgiou* are the same element as the domains claimed. Thus, *Georgiou* teaches a multiple clock domain microprocessor.

(b) [1(a)] a plurality of domains;

195. *Georgiou* discloses two or more functional units (e.g., the claimed plurality of domains). *Georgiou* describes “a thermal feedback system and method for cooperatively varying the voltage and operating frequency of a functional unit in a single or **multi-functional unit processor** to control heating.” Ex. 1008 at 1:22-

26, emphasis added. The functional units described in *Georgiou* are illustrated in Figure 1, which I have provided annotations for and reproduced below:

Reproduced from Georgiou (Annotated)

Id. at p. 3, annotated. As seen in annotated Figure 1 above, *Georgiou* illustrates and describes a plurality of functional units in the form of functional units 116-1, 116-2, ...116-K. *Id.* at 5:35-38 (“The dispatch unit 114 analyses dependencies among pending instructions, and schedules execution of instructions, one on each of functional units 116-1 through 116-K.”).

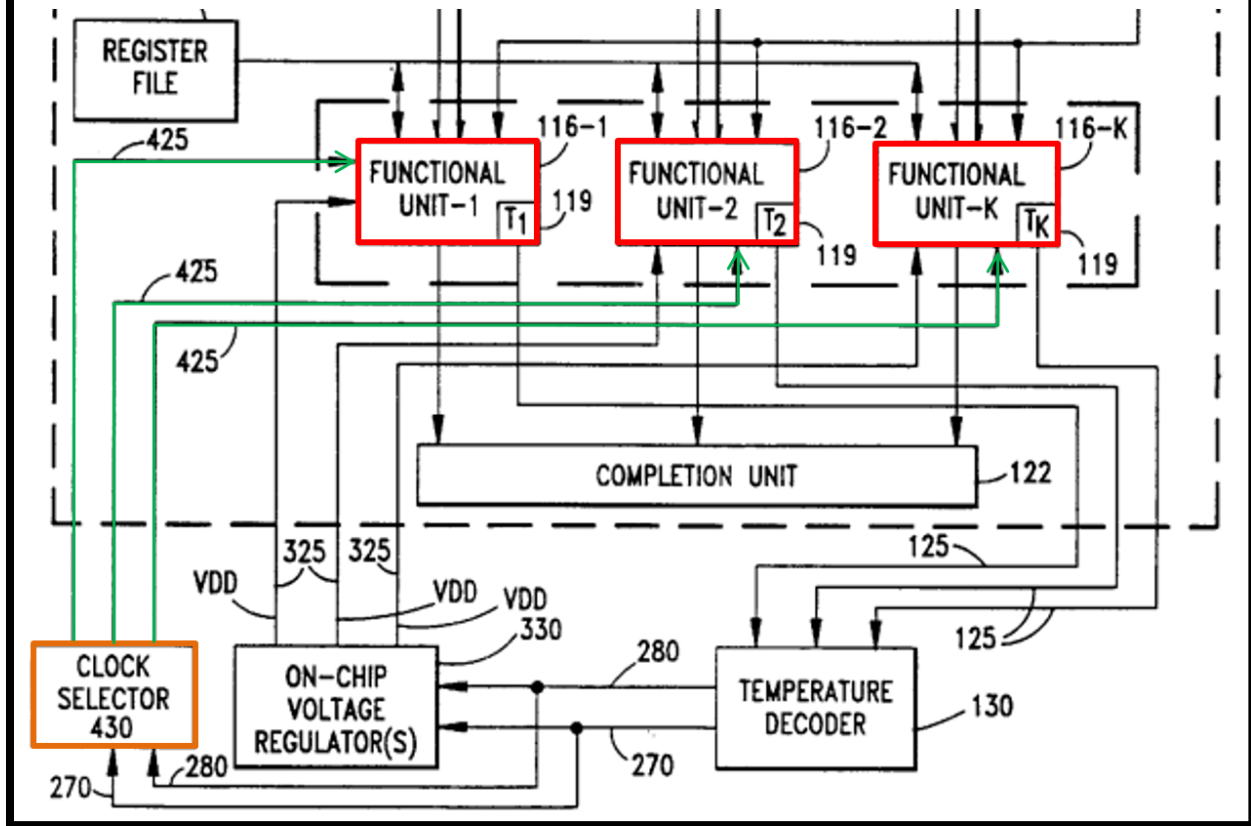
196. As I discussed above in reference to Claim Element 1[P] at Section III(J)(1)(a), examples of functional units are provided in *Georgiou* and overlap with the domains described in the '443 Patent. A POSITA would have understood that the functional units described in *Georgiou* are equivalent to the domains described in the '443 Patent. Clearly, a POSITA would recognize that the functional units described in *Georgiou* are the same element as the domains claimed. Thus, for the reasons I have explained, *Georgiou* teaches a plurality of domains.

- (c) *[1(b)] for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and*

197. *Georgiou* discloses, for each of the plurality of functional units (e.g., the claimed domains), a clock selector having respective multiplexers (e.g., each multiplexer corresponding to a claimed clock) for separately generating a clock signal at a frequency for that functional unit, the frequency being dynamically

changeable independently of the frequencies of the clock signals generated for others of the plurality of functional units. For example, *Georgiou* discloses “a thermal feedback system and method for cooperatively **varying the voltage and operating frequency of a functional unit** in a single or multi-functional unit processor to control heating.” Ex. 1008 at 1:22-26, emphases added. Further, the “modulated clock frequency 425 which corresponds to the reduced supply voltage 325 is applied to the clock inputs of the associated functional unit.” *Id.* at 4:41-44. I have provided an annotated version of an excerpt of Figure 1 below to assist in illustrating the relationship between the clock selector and corresponding functional unit:

“for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains”



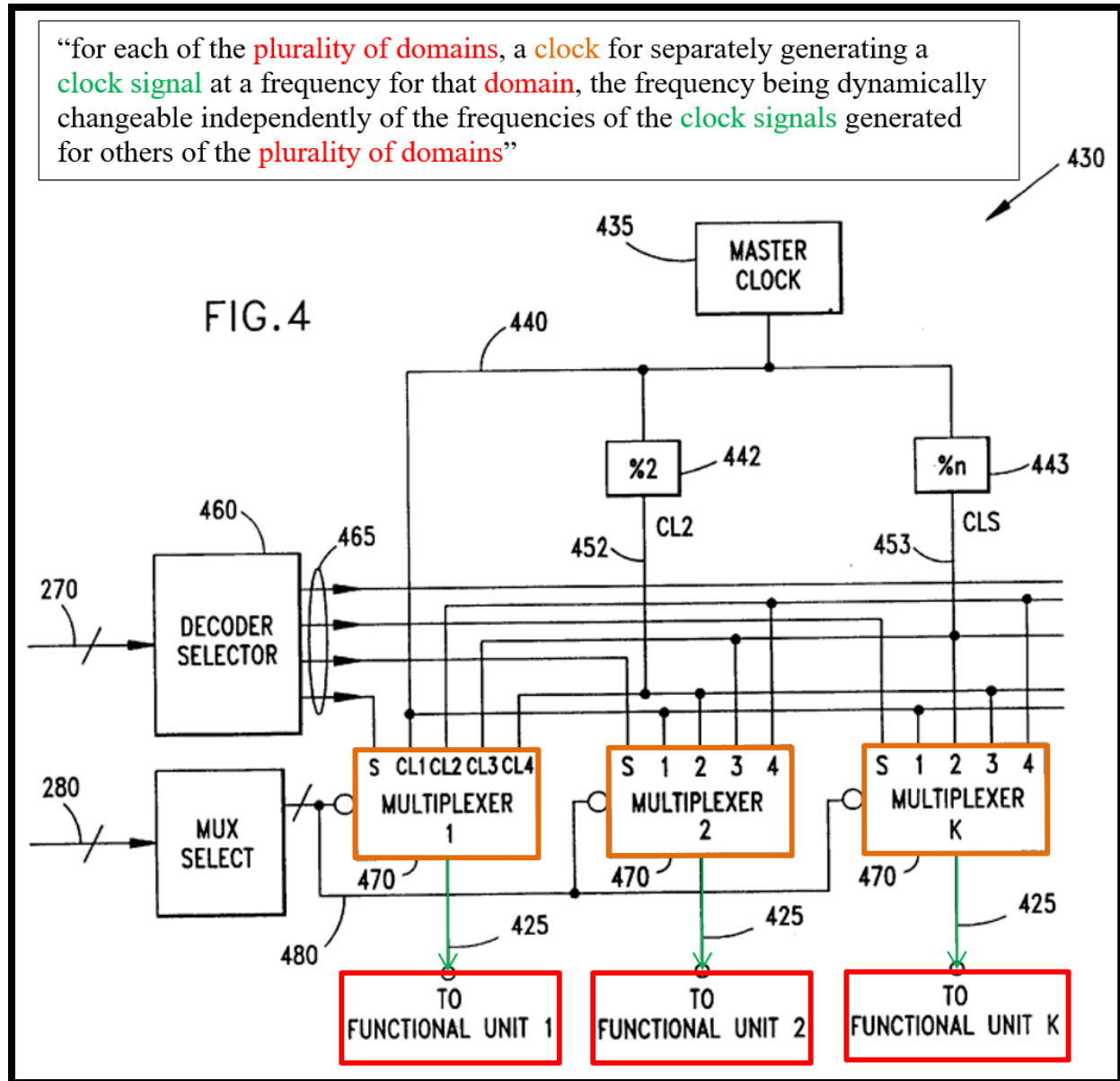
Reproduced from Georgiou (Excerpted and Annotated)

Id. at p. 3, excerpted and annotated.

198. As can be seen, current/clock control signal 270 is coupled to the “clock selector 430 to cooperatively modulate the clock frequency[.]” *Id.* at 4:37-39. As shown in annotated Figure 4 below, a respective modulated clock frequency 425 is generated by a multiplexer corresponding to a respective functional unit, and the respective modulated clock frequency 425 is then applied to each clock input of a

corresponding functional unit. Thus, the “clock frequency of the functional unit is modulated[.]” *Id.* at 4:61-62. The multiplexers 470 of clock selector 430 are associated with each “independently controllable functional unit” such that “**each functional unit may be operating under a different voltage 325 and frequency 425** combination according to the thermal feedback from its associated thermal sensor 119.” *Id.* at 5:2-6, emphases added.

199. Additionally, as shown in annotated Figure 4 below, *Georgiou* describes a clock generator for each of the plurality of domains consisting of the dividers 442, 443, etc., decoder selector 460, and the multiplexers 470. Thus, multiplexers 470 are each a separate clock, capable of outputting a certain output clock frequency for a specific functional unit. As indicated, Figure 4 shows components within clock selector 430.



Reproduced from Georgiou (Annotated)

Id. at p. 6, annotated.

200. Figure 4 shows a clock selector 430 with a master clock 435 running at a master clock frequency 440 that is used “as the common source and provides a common clock reference for a number of clock dividers[.]” *Id.* at 8:37-41. This is

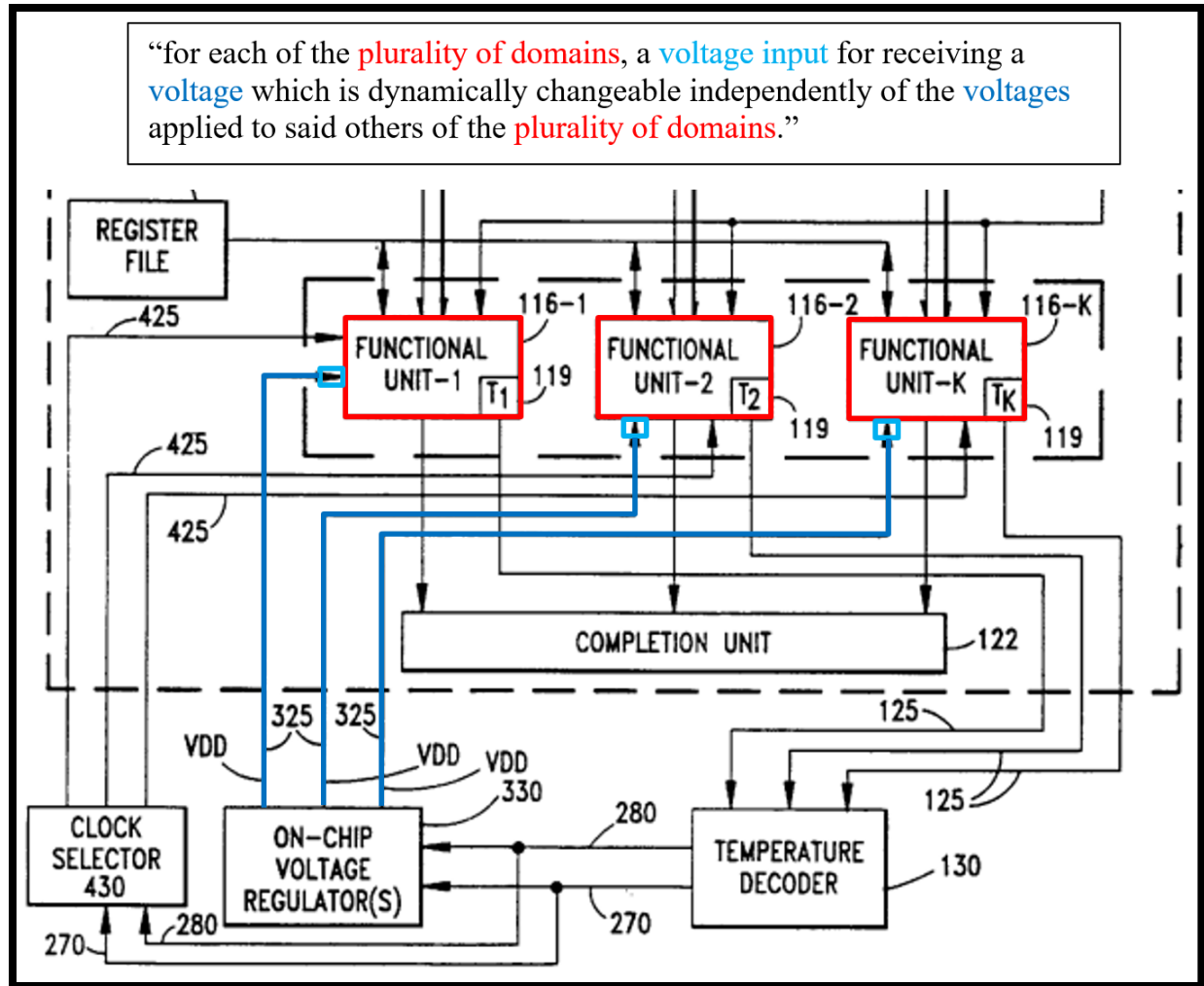
similar to the '443 Patent: “The preferred embodiment uses four domains, one of which includes the L2 cache, so that domains may vary somewhat in size and **still be covered by a single clock.**” Ex. 1001 at 5:7-9. As an example, *Shenai* explains that clock divider 442 is a “divide-by-two clock divider” and clock divider 443 is a “divide-by-n clock divider,” each of which are coupled the inputs of K multiplexers 470. *Id.* at 8:42-48. Additionally, the “clock selector includes a decoder 460 which receives signal 270 associated with a particular functional unit via its thermal sensor 119 and the temperature decoder 130. The decoder 460 decodes the signal 270 and outputs a clock select signal 465 to a select input (S) to the multiplexer associated with the particular functional unit.” *Id.* at 8:50-55. This clock selector includes a multiplexor selector to select and latch signal clock select signal 465 into the appropriate multiplexor according to the functional unit. *Id.* at 58-61.

201. The “technology associated with each functional unit has been characterized at a series of voltage-frequency pairs which satisfy critical timing paths over expected manufacturing process and operating conditions. **Each multiplexer 470 outputs the selected clock frequency which is coupled to the particular functional unit via the appropriate one of paths 425.**” *Id.* at 61-67, emphasis added. Therefore, not only are the clock signals provided independent to the other generated clock signals, but the clock signals are also dynamically changeable depending on the individual operating conditions of each functional unit

at a given time. For these reasons, *Georgiou* teaches for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains.

- (d) *[1(c)] for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.*

202. *Georgiou* discloses, for each of the plurality of functional units (e.g., the claimed domains), a voltage supply (e.g., the claimed voltage input) receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of functional units. For example, *Georgiou* discloses “a thermal feedback system and method for cooperatively **varying the voltage** and operating frequency **of a functional unit** in a single or multi-functional unit processor to control heating.” Ex. 1008 at 1:22-26, emphases added. Further, *Georgiou* explains “the output 325 of the adjustable voltage regulator 330 is applied to the **voltage supply** of the functional unit which provided the thermal signal 125.” *Id.* at 4:38-41, emphasis added. I have provided an annotated version of an excerpt of Figure 1 below to assist in illustrating the relationship between the voltage supply and corresponding functional unit:



Reproduced from *Georgiou* (Excerpted and Annotated)

Id. at p. 3, excerpted and annotated.

203. I have highlighted the fact that, in the annotated Figure 1, supply voltages 325 provide separate voltages to the inputs of functional unit 116-1, 116-2, ...116-K. As I discussed above, *Georgiou* teaches that “the output 325 of the adjustable voltage regulator 330 is applied to the **voltage supply** of the functional unit which provided the thermal signal 125.” *Id.* at 4:38-41, emphasis added. It would have been obvious to a POSITA that *Georgiou*’s voltage supply corresponds

to a voltage input as each functional unit receives a voltage from an “output 325 of the adjustable voltage regulator 330.” *Id.* at 4:38-41. To the extent *Georgiou’s* voltage supply does not teach the recited voltage input, a POSITA would have understood that a voltage input is known for each functional unit to receive a voltage from a respective voltage output. For example, in the Background of the Technology at Section III(A)(1), I describe that was known for microprocessors to use input pins to receive a voltage. *See* Ex. 1013 at p. 138, 175. A POSITA would have been motivated to apply a known technique of using a voltage input (e.g., an input pin) to known devices such as *Georgiou’s* microprocessor to yield the predictable result of receiving a voltage from a respective voltage output with a reasonable expectation of success.

204. The current/clock control signal 270, as seen in Figure 1, is coupled to the “adjustable on-chip voltage regulators 330 to reduce the supply voltage 325.” *Id.* at 4:35-36. “The output 325 of the adjustable voltage regulator 330 is applied to the **voltage supply of the functional unit** which provided the thermal signal 125.” *Id.* at 4:39-42, emphasis added. The regulator 330 is associated with each “independently controllable functional unit[.]” *Id.* at 5:2-4. Additionally, each functional unit can operate under a different voltage level supplied by voltage 325, according to the thermal feedback. *Id.* at 5:5-7. Therefore, not only are the voltage inputs for each functional unit provided independent to the other voltages supplied

to other functional units, but the voltages are also dynamically changeable depending on the individual needs (e.g., based on thermal feedback) of each functional unit at a given time. For these reasons, *Georgiou* renders obvious for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

2. Claim 3 – The microprocessor of claim 1, wherein there are at least four of said domains.

205. For the reasons I discussed above in reference to Claim 1 at Section III(J)(1), *Georgiou* renders obvious the microprocessor of claim 1. Additionally, *Georgiou* discloses a plurality of functional units, including functional units 116-1 through 116-K and explicitly including 116-1, 116-2, ...116-K with other units, such as a branch unit and a dispatch unit. Ex. 1008 at p. 3. A POSITA would have understood that “116-1, 116-2, ...116-K” represents four or more functional units as “K” is provided as a placeholder variable at the end of a sequence of numbers, which may be four or more (as three functional units are already shown and “K” represents a variable indicating more functional units than the three already shown functional units). *Georgiou* also explains the functional units can be “fixed-point units, floating point units, load/store units, and branch units found in typical general purpose and superscalar microprocessors.” *Id.* at 3:58-61.

206. As previously described in reference to Claim Element 1(a) at Section III(J)(1)(b), the functional units listed by *Georgiou* are the same as the ones

described in the '443 Patent. For example, *Georgiou* explains that the functional units include “floating point unit, multiple load/store and fixed point units, and a branch execution unit.” *Id.* at 4:52-54. Thus, *Georgiou* teaches the microprocessor of claim 1, wherein there are at least four of said domains.

3. Claim 8

- (a) *8[P]. A method of operating a microprocessor, the method comprising:*

207. *Georgiou* discloses a microprocessor. I have discussed this extensively with regards to Claim 1 at Section III(J)(1). For the same reasons I have provided above, *Georgiou* also discloses a method of operating a processor. Additionally, *Georgiou* explicitly states the invention is directed to a “method for cooperatively varying the voltage and operating frequency of a circuit to control heating while maintaining synchronization.” Ex. 1008 at 3:19-21. Thus, *Georgiou* renders obvious a method of operating a microprocessor.

- (b) *[8(a)] (a) providing a plurality of domains in the microprocessor;*

208. I have previously explained why *Georgiou* discloses a plurality of domains in reference to Claim Element 1(a) at Section III(J)(1)(b). Thus, for the same reasons, *Georgiou* teaches providing a plurality of domains in the microprocessor.

- (c) *[8(b)] (b) clocking each of the domains separately at a clock frequency;*

209. I have previously explained why *Georgiou* discloses for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain in reference to Claim Element 1(b) at Section III(J)(1)(c). Thus, for the same reasons, *Georgiou* teaches clocking each of the domains separately at a clock frequency.

(d) [8(c)] (c) applying a voltage to each of the domains separately;

210. I have previously explained why *Georgiou* discloses for each of the plurality of domains, a voltage input for receiving a voltage in reference to Claim Element 1(c) at Section III(J)(1)(d). Thus, for the same reasons, *Georgiou* teaches applying a voltage to each of the domains separately.

(e) [8(d)] (d) operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another; and

211. I have previously explained why *Georgiou* renders obvious each domain operating asynchronously relative to one another (e.g., each domain operating at respective independent frequencies and/or voltages) in reference to Claim Element 1(b) at Section III(J)(1)(c) and Claim Element 1(c) at Section III(J)(1)(d). It would have been obvious to a POSITA that operating a plurality of functional units with different clocks at the same time corresponds to the plurality of functional units operating asynchronously relative to one another, as recited. *Georgiou* describes that such different clocks and respective modulated voltages and

frequencies “are applied to the functional unit to dynamically control heating[.]” Ex. 1008 at 10:48-51.

212. The ’443 patent describes a multiple clock domain microprocessor where each functional block operates with “synchronizing circuits [that] ensure reliable **inter-domain** communication.” Ex. 1001 at 4:17-20, emphasis added. However, in case it is argued that each domain operates synchronously refers to intra-domain synchronization, I address below how both intra-domain synchronization and inter-domain synchronization would have been obvious to a POSITA, in view of *Georgiou*.

213. *Georgiou* discloses that “[a]s long as the sampled temperature exceeds the predetermined threshold temperature[,],” microprocessor components such as the on-chip voltage regulators and “clock selector 430 (voltage-frequency pair) will modulate the voltage 325 and corresponding clock frequency 425 respectively to control the heat generated by the **associated functional unit while maintaining synchronization and reliability.**” Ex. 1008 at 9:4-11, emphasis added. Accordingly, *Georgiou* teaches using microprocessor components (e.g., on-chip voltage regulators and clock selector) to modulate the voltage and clock frequency of a given functional unit (corresponding to the recited domain) to maintain inter-unit and intra-unit synchronization. Such modulated voltage and frequency “are

applied to the functional unit to dynamically control heating while maintaining synchronization and reliability.” *Id.* at 10:48-51.

214. Each of *Georgiou*’s functional units are intra-domain synchronized. As discussed above for Claim 8(b) at Section III(J)(3)(c) and Claim 8(C) at Section III(J)(3)(d), each functional unit is provided a frequency and voltage based on its respective needs (e.g., based on thermal feedback). Accordingly, the components of each functional unit operate using the same frequency and voltage. Thus, each functional unit operates synchronously using its provided frequency and voltage. Further, if necessary, a POSITA would have understood that *Georgiou*’s intra-domain synchronization would have been implemented in accordance with techniques known in the art. For example, *Georgiou*’s clock frequency for a given functional unit provides the period of time in which the given functional unit operates. The operations of the functional unit then operate synchronously with respect to the given clock frequency. As I discuss in the Background of the Technology at Section III(A)(3) and Section III(A)(4), domains operate synchronously to allow easy communication with parts within the domain while the different domains operate asynchronously to allow different clock values for different operations. For example, *GALS* explains that “[l]eaving a synchronous block into the asynchronous domain is a reasonably trivial matter.” Ex. 1022 at p. 1. As another example, *Traylor* describes translating “synchronous to asynchronous

signaling conventions.” Ex. 1007 at 4:21-23. “Here, the synchronous based signaling conventions are utilized by the processor, whereas the network operates in an asynchronous or self-timed scheme.” *Id.* at 4:23-27.

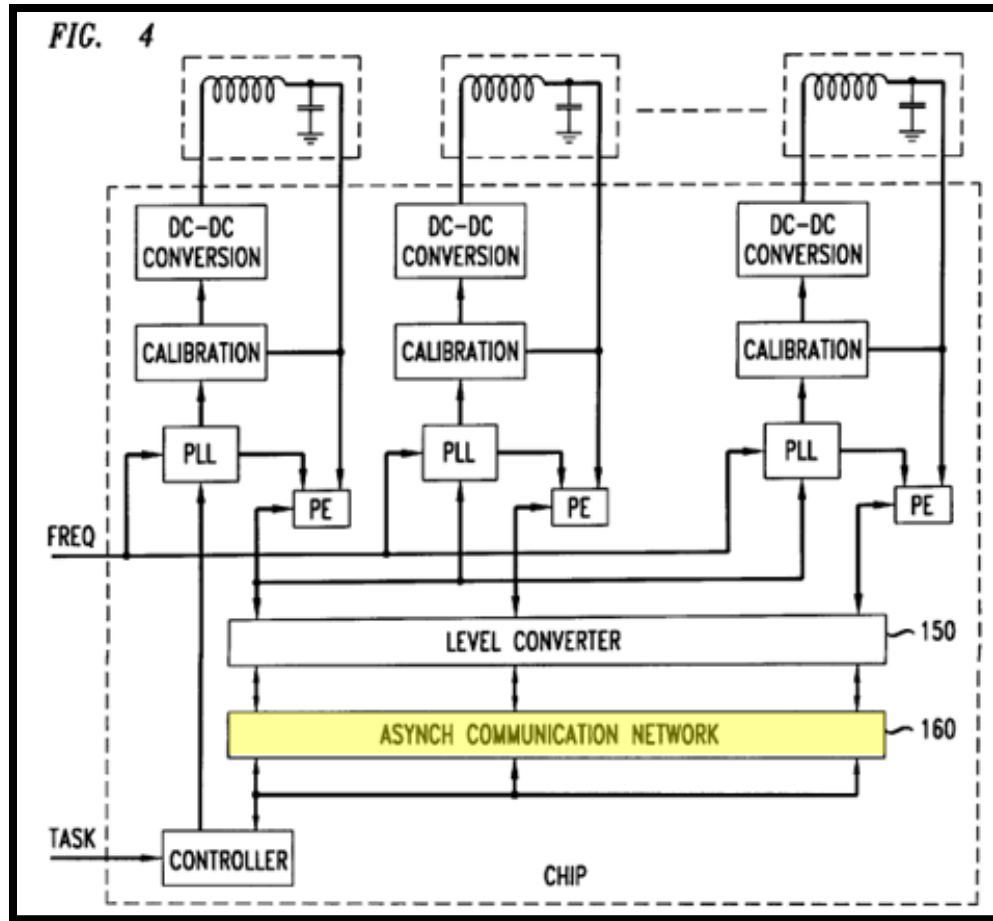
215. Further, operating each domain synchronously (in reference to inter-domain synchronization) while multiple domains operate asynchronously would have been obvious to a POSITA since *Georgiou* provides a microprocessor used to operate a plurality of functional units with respective different clocks at the same time. *Georgiou* also teaches that “[u]sing thermal sensors for feedback, the voltage swing and operating frequency of the circuit are cooperatively varied (also called voltage-frequency pairs) to reduce the power dissipation **without compromising reliability or system synchronization.**” Ex. 1008 at 2:21-26, emphases added. I have provided several references in the Background of the Technology at Section III(A)(3) and Section III(A)(4) that explain operating domains asynchronous to one another while the domains operate synchronously (in reference to inter-domain synchronization).

216. For example, *GALS* explains globally asynchronous, locally synchronous (GALS) systems, the same as which are described in the ’443 Patent, “aim to combat all three of these problems by doing away with a global clock and instead having a locally generated clock for every module.” Ex. 1022 at p. 1. “**Obviously, modules cannot be synchronized if they all use different clocks, so**

we use an asynchronous protocol to communicate between them.” *Id.*, emphasis added.

217. As another example, *Nicol* describes processing elements (e.g., functional units) that have adjustable clock frequencies depending on the time to carry out tasks. Ex. 1023 at 4:2-5. Since the individual processing elements (“PEs”) operate at different frequencies from one another, the multiprocessor may run into synchronization issues. *Id.* at 6:14-18. A “synchronization schema must be implemented when there is a need to communicate data between PEs (or with other system elements) that operate at different frequencies.” *Id.* at 6:18-21. Thus, since the functional units of *Georgiou* operate at different frequencies as also described by *Nicol*, a POSITA would have known that a functional unit of *Georgiou* also operates asynchronous with respect to other functional units, where known synchronization schema are used to yield predictable results for synchronizing inter-unit communication between asynchronous functional units.

218. Annotated Figure 4 of *Nicol*, reproduced below, illustrates separate clock frequencies for each processing element (PE) while also including an asynch communication network 160 to help synchronize inter-domain communication, similar to the asynchronous protocol mentioned in *GALS*.



Reproduced from Nicol (Annotated)

Ex. 1023 at p. 3, annotated. “To effect [the issue of inter-PE] synchronization, each PE within the Figure 4 arrangement is connect[ed] to an arrangement comprising elements 150 and 160. ... 160 resolves the issue of different clock domains.” *Id.* at 6:14-34.

219. To the extent it is argued that *Georgiou* does not disclose how its inter-unit synchronization is implemented, a POSITA would have been motivated to implement *Georgiou*’s inter-unit communication using known synchronization techniques (e.g., by stretching a clock or using a synchronization schema as

discussed in the Background of the Technology at Section III(A)(4)). *See* Ex. 1022 at p.1; *see also* Ex. 1023 at 6:14-21, 6:29-31. Such a combination would yield predictable results for improving “system synchronization” as suggested in *Georgiou*. Ex. 1008 at 2:21-26. As discussed above, it would also be obvious to a POSITA that *Georgiou* discloses intra-domain synchronization as the components of each functional unit operate using the same frequency and voltage. As also discussed above, a POSITA would have known that the microprocessor of *Georgiou* include functional units operating asynchronously to one another while also being locally synchronous. Specifically, *Georgiou* describes a microprocessor where each functional unit is provided a separate clock input and operates asynchronously. For these reasons, operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another would have been obvious to a POSITA in view of *Georgiou*.

- (f) [8(e)] (e) *dynamically controlling the clock frequency and the voltage in each of the plurality of domains independently of the clock frequencies and the voltages in others of the plurality of domains.*

220. I have previously explained why *Georgiou* renders obvious both dynamically changing the clock frequency and the voltage in each load independently of the other loads in reference to Claim Element 1(b) at Section III(J)(1)(c) and Claim Element 1(c) at Section III(J)(1)(d). Thus, for the same reasons, *Georgiou* renders obvious dynamically controlling the clock frequency and

the voltage in each of the plurality of domains independently of the clock frequencies and the voltages in others of the plurality of domains.

4. Claim 12 – The method of claim 8, wherein there are at least four of said domains.

221. For the reasons I have detailed above in reference to Section III(J)(1), *Georgiou* renders obvious the method of claim 8. Additionally, I have previously explained why *Georgiou* discloses a microprocessor that has at least four loads in reference to Claim 3 at Section III(J)(2). Thus, for the same reasons, *Georgiou* renders obvious wherein there are at least four of said domains.

K. Ground 6: Claims 4 and 9 are obvious over *Georgiou* in view of *Halepete*

1. Claim 4 – The microprocessor of claim 1, wherein the microprocessor is programmed to determine a slack in processing in one of the domains and to reduce the clock frequency and the voltage in said one of the domains to reduce the slack.

222. For the reasons I discussed above in reference to Claim 1 at Section III(J)(1), *Georgiou* renders obvious the microprocessor of claim 1. Additionally, for the reasons I discussed above in reference to Claim 4 at Section III(G)(1), *Shenai* in view of *Halepete* renders obvious wherein the microprocessor is programmed to determine a slack in processing in one of the domains and to reduce the clock frequency and the voltage in said one of the domains to reduce the slack.

223. For similar reasons as to why a POSITA would have found it obvious to combine the teachings of *Shenai* with the teachings of *Halepete*, a POSITA would

have found it obvious to combine the teachings of *Georgiou* with the teachings of *Halepete*. Just like *Shenai*, *Georgiou* is directed to a multi-functional unit microprocessor. Additionally, both *Shenai* and *Georgiou* describe circuitry and/or architecture to allow dynamic voltage and frequency changes for each individual functional unit. *Georgiou* also describes critical timing paths similar to the concept of slack. “For example, a digital chip is typically characterized by a critical timing path. Reducing the supply voltage will cause the propagation of a signal through the critical timing path to slow until a malfunction occurs.” Ex. 1008 at 1:49-54. The clock frequency is varied with the voltage to maintain these critical timing paths. *Id.* at 2:28-29.

224. Thus, a POSITA would have been motivated to combine the multi-functional unit microprocessor of *Georgiou* with the control software capable of determining necessary clock frequency and voltage levels and consequently adjusting the clock frequency and voltage level of *Halepete* as such a combination would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. I provide a more in-depth analysis on why a POSITA would have been motivated to combine *Halepete* with multi-domain microprocessors such as *Shenai* or *Georgiou* above in reference to Claim 4 at Section III(G)(1). Accordingly, *Georgiou* in view of *Halepete* renders obvious the microprocessor of claim 1, wherein the

microprocessor is programmed to determine a slack in processing in one of the domains and to reduce the clock frequency and the voltage in said one of the domains to reduce the slack.

2. Claim 9

(a) 9[P]. The method of claim 8, wherein step (e) comprises:

225. For the reasons I have detailed above in reference to Claim 8 at Section III(J)(3), *Georgiou* renders obvious the method of claim 8.

(b) [9(a)] (i) determining a slack in processing in one of the domains; and

226. I have previously explained why *Georgiou* in view of *Halepete* renders obvious a microprocessor that is programmed to determine a slack in processing in one of the loads in reference to Claim 4 at Section III(K)(1). Thus, for the same reasons, *Georgiou* in view of *Halepete* renders obvious determining a slack in processing in one of the domains.

(c) [9(b)] (ii) reducing the clock frequency and the voltage in said one of the domains to reduce the slack.

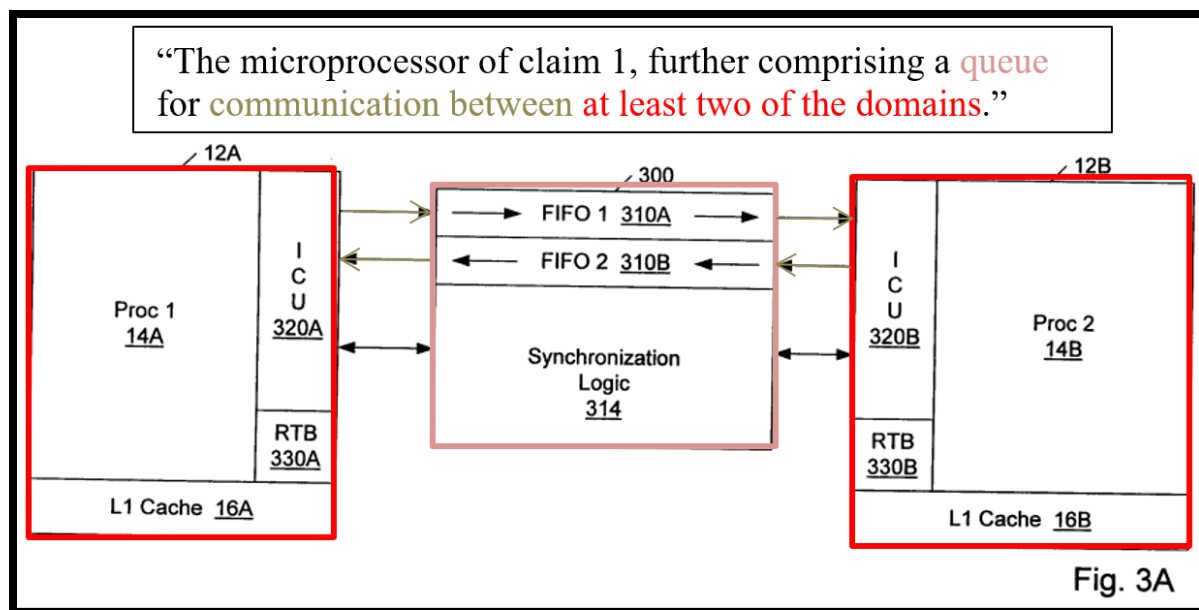
227. I have previously explained why *Georgiou* in view of *Halepete* renders obvious a microprocessor that is programmed to determine a slack in processing in one of the loads, in reference to Claim 4 at Section III(K)(1). Thus, for the same reasons, *Georgiou* in view of *Halepete* renders obvious reducing the clock frequency and the voltage in said one of the domains to reduce the slack.

L. Ground 7: Claims 5 and 10 are obvious over Georgiou in view of Kranich

1. Claim 5 – The microprocessor of claim 1, further comprising a queue for communication between at least two of the domains.

228. For the reasons I have detailed above in reference to Claim 1 at Section III(J)(1), *Georgiou* renders obvious the microprocessor of claim 1. The '443 Patent describes a “queue” structure that asserts a FULL flag to assert that a producer “can no longer write to the queue until the flag is deasserted” and an EMPTY flag to assert “that there is no valid data [] to read from the queue.” Ex. 1001 at 6:54-60. To the extent it is argued that *Georgiou* alone does not explicitly disclose or render obvious its microprocessor comprising a queue for communication between at least two of the domains, this would have been obvious to a POSITA in view of *Kranich*.

229. *Kranich* discloses “a plurality of processing units[.]” Ex. 1009 at p. 9, ll. 4-5. While the processing units are mainly described as processors, it should be easily understood that the processing units can also be individual functional units, within a single microprocessor. As I further discuss below, the disclosure of *Kranich* would still apply to a functional unit such as *Georgiou*’s “floating point unit, multiple load/store and fixed point units, [or] a branch execution unit.” Ex. 1008 at 4:52-54. *Kranich* shows an “interconnection between two processors 12A-12B” in Figure 3A. Ex. 1009 at p. 10, ll. 6-7.



Reproduced from *Kranich* (Annotated)

Id. at p. 26, annotated.

230. As I have shown with the annotations above, *Kranich* describes a “thread control device 300” that includes “first-in-first-out (hereinafter FIFO) buffers 310A-310B, and synchronization logic 314” to facilitate intercommunication between processors 12A and 12B. *Id.* at 10:6-11. Specifically, the interprocessor communication units (“ICU”) of “each processor 12 are coupled to thread control device 300 which facilitates communication between processors 12A and 12B.” *Id.* at 10:12-13. The ICU 320A and/or 320B communicates with the FIFO buffers 310A and 310B.

231. As I have discussed above with respect to *Sherburne* for Claim 5 at Section III(H)(1), it would have been obvious to a POSITA to include a well-known

method (e.g., implementing FIFO based queues) as described in *Kranich* (and in *Sherburne*) to facilitate the communication between the functional units of *Georgiou*.

232. Further, *Georgiou* is directed determining operating parameters “of a functional unit in a multi-functional unit processor such as a superscalar microprocessor.” Ex. 1008 at 3:48-53. Similarly, *Kranich* is directed to a “processor architecture containing multiple closely coupled processors in a form of symmetric multiprocessing system.” Ex. 1009 at p. 1, item (57). Therefore, *Georgiou* and *Kranich* are in the same field of endeavor of operating a plurality of units of a processing system. Accordingly, a POSITA would have been motivated to use known techniques to modify *Georgiou* to realize improvements based on the disclosure of *Kranich*, to obtain predictable results with an expectation of success.

233. A POSITA would have recognized the advantages of *Georgiou*’s functional units having the ability to communicate with one another. For example, a POSITA would have appreciated the fact that, since *Georgiou*’s microprocessor is maximizing the usage of each functional unit with the power provided, the functional units would have benefited from communicating necessary voltages and/or frequencies to one another to efficiently complete tasks and reduce any wait times (e.g., slack). For example, *Georgiou* teaches a dispatch unit that “analyses dependencies among pending instructions, and schedules execution of instructions,

one on each of functional units 116-1 through 116-K.” Ex. 1008 at 5:35-38. A POSITA would have recognized the advantage of modifying *Georgiou*’s dispatch unit with *Kranich*’s “thread control device 300” that includes “first-in-first-out (hereinafter FIFO) buffers 310A-310B, and synchronization logic 314” to facilitate intercommunication between processors. Ex. 1009 at 10:6-11. A POSITA would have recognized that such a modification would combine *Kranich*’s FIFO buffers with *Georgiou*’s functional units to allow increased communication between *Georgiou*’s functional units to yield predictable results without always having to interface with a dispatch unit, thereby increasing efficiency and scope of communication.

234. As I discuss in the Background of the Technology at Section III(A)(2), the FIFO queue buffer in *Kranich* was well-known in the art prior to the time of the invention. *See* Ex. 1015 at p. 1, 2; *see also* Ex. 1016 at p. 11, 12, 24. A POSITA would have appreciated allowing the functional units of *Georgiou* to communicate with one another. As such, it would have been obvious to a POSITA to incorporate the intercommunication of processing units via FIFO buffers taught in *Kranich* with the microprocessor architecture taught in *Georgiou*. Such a combination would have been nothing more than combining prior art elements (e.g., *Georgiou* microprocessor architecture implemented using *Kranich*’s FIFO) to yield predictable results (e.g., intercommunication of processing units) with a reasonable

expectation of success. For these reasons, *Georgiou* in view of *Kranich* renders obvious the microprocessor of claim 1, further comprising a queue for communication between at least two of the domains.

2. Claim 10 – The method of claim 8, wherein step (d) comprises providing a queue for communication between at least two of the domains.

235. I have previously explained why *Georgiou* in view of *Kranich* renders obvious a microprocessor further comprising a queue for communication between at least two of the domains in reference to Claim 5 at Section III(L)(1). I have also previously explained why *Georgiou* teaches the method of claim 8 at Section III(J)(3). Thus, for the same reasons above, *Georgiou* in view of *Kranich* renders obvious the method of claim 8, wherein step (d) comprises providing a queue for communication between at least one of the domains.

IV. CONCLUSION

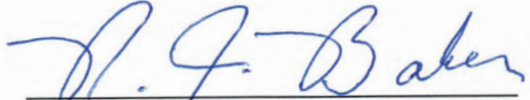
236. In summary, it is my opinion that the references discussed in this Declaration disclose or suggest all of the features recited in claims 1, and 3-12 of the '443 Patent. Thus, it is my opinion that every one of claims 1, and 3-12 of the '443 Patent is rendered obvious by the prior art grounds as set forth herein.

237. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the

Declaration of R. Jacob Baker, P.E., Ph.D.
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like so made are punishable by fine or imprisonment, or both, under Section 1001 of
Title 18 of the United States Code.

Dated: 7/29/2024

By: 
R. Jacob Baker, Ph.D.

Appendix A

R. JACOB BAKER, PH.D., P.E.

professor emeritus of electrical and computer engineering

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PROFESSIONAL SUMMARY

Russel Jacob Baker (R. Jacob Baker), Ph.D., P.E. (IEEE Student Member 1983, Member 1988, Senior Member 1997, and Fellow 2013) was born in Ogden, Utah, on October 5, 1964. He received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas (UNLV) in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno (UNR) in 1993. His Google Scholar profile is [here](#) and his ResearchGate profile is [here](#).

From 1981-1987 he served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division). From 1985-1993 he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada Test Site. During this time he designed, and oversaw the fabrication and the electrical/mechanical manufacture of, over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs for high-speed imaging, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1991-1993 he was an adjunct faculty member in the Departments of Electrical Engineering at UNLV and UNR. From 1993-2000 he served on the faculty in the Department of Electrical Engineering at the University of Idaho (UI), first as an untenured assistant professor and then from 1998 as a tenured associate professor. In 2000 he joined a new electrical and computer engineering (ECE) program at Boise State University (BSU) where he was promoted to professor in 2002. He then served as the ECE department chair from 2004-2007. At BSU he helped establish graduate programs in ECE including, in 2006, the university's second PhD degree. In 2012 he rejoined the faculty at UNLV as a tenured full professor of ECE. During his tenure at the UI, BSU, and UNLV he has been the major professor to more than [100 graduate students](#).

Dr. Baker has done consulting for over [200 companies](#). His [research/development](#) activities are in: photonics, circuit design for wireless and wired communications, analog-to-digital/digital-to-analog data conversion and transmission, optoelectronics (imagers, displays, LIDARs, APDs, SiPMs, and associated electronics), analog and digital integrated circuit design and fabrication, design of diagnostic electrical and electro-optic instrumentation for scientific research, integrated electrical/biological circuits and systems, array (memory, imagers, and displays) fabrication and design, design of digital processors for signal processing, CAD tool development and online tutorials, low-power interconnect and packaging (electrical and optical) techniques, design of wired/wireless communication and interface circuits, circuit design for the use and storage of renewable energy, power electronics and power supply design, and the delivery of [online engineering education](#). As a result of this work, he is the named inventor on over [150 US patents](#) and the author of over [100 publications](#).

He is a member of the honor societies Eta Kappa Nu and Tau Beta Pi, a licensed Professional Engineer, a popular lecturer that has delivered over [50 invited talks](#) around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation, CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the 2000 Best Paper Award from the IEEE Power Electronics Society,

the 2007 Frederick Emmons Terman Award, the 2011 IEEE Circuits and Systems Education Award, and the 2021 Wiley-IEEE Press Textbook Award for the 4th Edition of his book CMOS Circuit Design, Layout, and Simulation.

His service activities include the IEEE Press Editorial Board (1999-2004), editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015), the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), Distinguished Lecturer for the SSCS (2012-2015), Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the IEEE Solid-State Circuits Magazine, IEEE Kirchhoff Award Committee (2020-2023), and advisor for the student branch of the IEEE at UNLV (2013-2024).

INDUSTRY EXPERIENCE

2008 - present: Expert witness in intellectual property disputes in electrical, electro-optic, and computer engineering matters for: 1) district court and ITC patent disputes, 2) inter partes reviews at the PTAB, and 3) arbitrations and mediations.

2013 - 2022: Worked with Freedom Photonics, Santa Barbara, CA, on the integration, fabrication and design, of optoelectronics with CMOS integrated circuits. Work includes the design of compact optical transceivers for range finding applications, high-efficiency integrated silicon avalanche photodetectors for quantum key receivers, Geiger mode SiGe receivers for long-range communications, cryptography, and the fabrication of near-infrared focal plane arrays. Packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies using LEDs, ILDs, PIN, APDs, and ROICs.

2017 - 2019: Worked with Vorpel Research Systems, Las Vegas, NV on the design of integrated circuit electronics and optoelectronics for optical transceivers used in LIDARs/LADARs.

2016 - 2019: Worked with Attollo Engineering on the design of transient digitizers for the capture of high-speed signals for range finders using LEDs and lasers in compact optical transceivers.

2013 - 2018: Working with Mission Support and Test Services, LLC (MSTS, formerly National Security Technologies, LLC, [NSTec]) on the Design and Fabrication of Integrated electrical/photonics application specific integrated circuit (ASIC) design for use in the implementation of diagnostic instrumentation.

2013 - 2015: Consultant for OmniVision. Working on integrating CMOS image sensors (CIS) with memory for very high-speed consumer imager products. Design specialty DRAM, high-speed interfaces between CIS and DRAM, packaging techniques to pair the CIS with DRAM.

2010 - 2013: Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2013: Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

2012: Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design and fabrication for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, high-speed interfaces between image processors and imaging systems, and infrared imaging systems.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

2009 - 2010: Sun Microsystems, Inc. (and then Oracle) VLSI research group. Provided consulting on memory circuit design/fabrication and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power, 3D packaging, for memory modules and controllers implemented with FPGAs and custom ASICs.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

1994 - 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs, PLLs for embedded processors, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), SRAMs, RFIDs, CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project

between Micron and HP labs in magnetic memory fabrication and design using the MTJ memory cell. Worked on numerous technologies ranging from LED lighting to medical imaging using CMOS image sensors (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line from fabrication to test. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing.

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1999: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips, interfaces, and serial buses including USB circuits, charging circuits based upon power up/down circuits using an MOS or bandgap reference, pre-amplifiers, comparators, etc.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and processors.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television. Worked on the fabrication and design of video peripheral circuits for these displays.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns rise-time and 8 ns fall-time for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant while finishing up my Ph.D.), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing and fabricating over 30 electronic and electro-optic instruments including: CCD camera design, communication networks, fiber optic transmitters employing high speed laser drive electronics, receivers employing envelop tracking for DC voltage restoration and regeneration of received information, receiver low noise amplifier design, frame synchronizers for re-assembling transmitted images, high-speed SRAM memory system design with battery back-up, calibration equipment design such as a tunnel diode pulse generator for testing compensation of oscilloscopes and DAC design for calibrating CCD readout electronics, power supply and battery charger designs, sweep circuits for streak cameras, Pockel's cell drive electronics, vertical amplifier design using HBTs for analog oscilloscopes used at the Nevada Test Site, and 10 kV ramp designs using a planar triode to name some of the designs.

This position provided considerable fundamental grounding in EE with a broad exposure ranging from the design of PC boards to, for example, the design of cable equalizers. Summarizing, gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuit fabrication and design, GaAs (high speed logic and HBTs), Mach-Zehnder interferometers, Pockels cells, krytrons, power MOSFETs, microwave techniques, power supplies, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble-shooting electric motors on mining equipment.

ACADEMIC EXPERIENCE

January 1991 – present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho:** Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998 - 2000). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit fabrication and design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, Army, DMEA, Navy, and the AFRL.
- Current and past research and development interests are:
 - Design and packaging of electrical/optical systems (e.g., LiDARs/LADARs) using LEDs, semiconductor lasers, lens for focusing and directing light, integrated circuits, and associated control and communication systems/circuits.
 - Capacitive sensing techniques using delta-sigma modulation and interfacing to sensors
 - Design of high-voltage and energy switching circuits
 - Circuit design and fabrication for the control, use, and storage of renewable energy using thermoelectric generators
 - Design of electrical/biological/optical circuits and systems using electrowetting on dielectric for automating and controlling biological experiments
 - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
 - Heterogeneous integration of III-V photonic devices (e.g., FPAs and VCSELs) with CMOS
 - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories, memory modules, and digital systems using custom and non-custom (e.g., FPGAs) implementations
 - Analog and mixed-signal circuit fabrication and design for communication systems, synchronization, energy storage, data conversion, and interfaces
 - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g., magnetic, chalcogenide)
 - Reconfigurable electronics design and fabrication using nascent memory technologies such as the memristor to implement FPGAs
 - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
 - Power electronics circuit design for consumers and consumer electronics including power management and adaptive control to reduce power consumption
 - Design of bandpass delta-sigma modulators for IQ demodulation in wireless communication systems in OFDM, WiFi, 802.11, Bluetooth, 3G, 4G, etc.
 - University prototyping, fabricating, and packaging of integrated circuits
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI design and fabrication, fiber optics, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

EDUCATION

- Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*
- M.S. and B.S. in Electrical Engineering; May 1986 and May 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge.*

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)
Member of the honor societies Eta Kappa Nu and Tau Beta Pi
Licensed Professional Engineer

HONORS AND AWARDS

- Consolidated Students of the University of Nevada, Las Vegas (CSUN) Faculty Award, 2017
- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013, 2014, 2015 and 2016
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2012 - 2015
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Master's graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as a Distinguished Lecturer for the SSCS (2012-2015), as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015, as advisor for the student branch of the IEEE at UNLV (2013-2023), and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the *IEEE Solid-State Circuits Magazine*, and IEEE Kirchhoff Award Committee (2020-2023).

ARMED FORCES

From 1981 to 1987 served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge. Military Occupational Specialty (MOS) was Machine Gunner (MOS 0331)

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Fourth Edition" *Wiley-IEEE Press*, 1234 pages. ISBN 9781119481515 (2019) **Over 50,000 copies of this book in print.** (Third Edition published in 2010, Revised Second Edition published in 2008, and Second Edition Published in 2005)

Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 9780471227540 (First Edition published in 2002)

Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, 201 pages. ISBN: 9780470184752

Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, 201 pages. ISBN 0780360141

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 9780780334168

BOOKS, OTHER (edited, chapters, etc.)

Saxena, V. and Baker, R. J., "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 2000. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 22 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

INVITED TALKS AND SEMINARS

Have given over 50 invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICSEng Keynote, ICySSS keynote, IEEE Computing and Communication Workshop (CCWC), IEEE Electron Devices Conference (NVMETS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Lockheed-Martin, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING

In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. J., (2023-2024) "Silicon Germanium (SiGe) Avalanche Photo Diode (APD) Chip," Department of Energy, Mission Support and Test Services (MSTS), LLC, \$120,000
- Baker, R. Jacob, (2017-2023) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit," NASA, \$29,999 (Phase I), \$225,238 (Phase II), and \$79,697 (Phase IIE)
- Goldman, J., Menezes, J., and Baker, R. J., (2021-2022) "Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling," UNLV Sports Research & Innovation Initiative. Proof of Concept Grant Program, \$50,000
- Baker, R. Jacob, (2019-2021) "Dual-Mode, Extended Near-Infrared, Focal Plane Arrays Fabricated with CMOS Compatible GeSiSn Alloy Materials," DARPA, \$149,998
- Baker, R. Jacob, (2018-2020) "Geiger Mode SiGe Receiver for Long-Range Optical Communications," NASA, \$99,996

- Baker, R. Jacob, (2019) "Improved Quantum Efficiency Photo-Detector," Navy, \$29,999
- Baker, R. Jacob, (2018-2019) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit – Phase I," NASA, \$29,999
- Baker, R. Jacob, (2017-2019) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), \$266,029
- Baker, R. Jacob, (2017-2019) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, \$299,605
- Baker, R. Jacob, (2016-2018) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, \$299,665

DOCTORAL STUDENT SUPERVISION

10. Sachin Namboodiri – A Multi-channel MCP-PMT based Readout Integrated Circuit for LiDAR Applications (2020)
9. Wenlan Wu – High-Speed Radhard Mega-Pixel CIS Camera for High-Energy Physics (2019)
8. Kostas Moutafis – A Highly-Sensitive Global-Shutter CMOS Image Sensor with On-Chip Memory for Hundreds of kilo-frames per second Scientific Experiments (2019)
7. Yiyan Li – Portable High Throughput Digital Microfluidics and On-Chip Bacteria Cultures (2016)
6. Yacouba Moumouni – Designing, Building, and Testing a Solar Thermoelectric Generation, STEG, for Energy Delivery to Remote Residential Areas in Developing Regions (2015)
5. Qawi IbnZayd Harvard – Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design (2011)
4. Vishal Saxena – K-Delta-1-Sigma Modulators for Wideband Analog-to-Digital Conversion (2010)
3. Robert Russell Hay – Digitally-Tunable Surface Acoustic Wave Resonator (2009)
2. Xiangli Li (the first Boise State University College of Engineering PhD graduate) – MOSFET Modulated Dual Conversion Gain CMOS Image Sensors (2008)
1. Feng Lin, Research and Design of Low Jitter, Wide Locking-Range Phase-Locked and Delay-Locked Loops (2000)

MASTERS STUDENT SUPERVISION

91. Jazmine Bloor – Survey of how Irregular Pathways in the Electrical System of the Human Heart Link to Different Heart Arrhythmias (2023)
90. Abraham Lopez – An Avalanche-Transistor-Based Pulse Generator Design For Infrared Laser Applications (2023)
89. David Santiago – Development of an Automated GPIB System for Characterization of SiGe Avalanche Photodiodes (2023)
88. Minsung Cho – Studies of Forward Projection Algorithms and Implementation on PC and FPGA (2023)
87. Armani Alvarez – A Control Integrated Circuit for a Hysteretic Flyback Power Converter (2022)
86. Francisco Mata-carlos – A Wearable Electronic Monitoring Device for Low Pressure Garment Applications and Temperature Analysis for Prevention of Ulceration and Infection (2022)
85. Daniel Senda – Designs and Outcomes of Transcranial Magnetic Stimulation (TMS) and Repetitive Transcranial Magnetic Stimulation (rTMS) Circuits (2021)
84. James Skelly – Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling (2021)
83. Gonzalo Arteaga – Current-mode photon-counting circuit with SiGe BiCMOS input stage (2020)
82. Jason Silic – Design and Fabrication of a 6-bit Current-Mode ADC for Lidar and High-Speed Applications (2020)
81. Brandon Wade (2020)
80. Mario Valles Montenegro – Front-End CMOS Transimpedance Amplifiers on a Silicon Photomultiplier Resistant to Fast Neutron Fluence (2020)
79. Jonathan DeBoy (2018)
78. Dane Gentry – Design, Layout, and Testing of SiGe APDs Fabricated in a BiCMOS Process (2018)
77. James Mellot – Variable Transition Time Inverters in a Digital Delay Line with Analog Storage for Processing Fast Signals and Pulses (2018)
76. Eric Monahan – High Speed Fast Transient Digitizer Design and Simulation (2018)
75. Shada Sharif – Design and Analysis of First and Second Order K-Delta-1-Sigma Modulators in Multiple Fabrication Processes (2018)
74. Vikas Vinayaka – Analysis and Design of Analog Front-End Circuitry for Avalanche Photodiodes (APD) and Silicon Photo-Multipliers (SiPM) in Time-of-Flight Applications (2018)

73. Claire Tsagkari – Design, Fabrication and Testing of a Capacitive Sensor Using Delta-Sigma Modulation (2017)
72. Kevin Buck – Fast Transient Digitizer and PCB Interface (2015)
71. Marzieh Sharbat Maleki (2015)
70. Angsuman Roy – Design, Fabrication and Testing of Monolithic Low-Power Passive Sigma-Delta Analog-to-Digital Converters (2015)
69. Daniel Anderson – Design and Implementation of an Instruction Set Architecture and Instruction Execution Unit for the RZ9 Coprocessor System (2014)
68. Jared Gordon – Design and Fabrication of an Infrared Optical Pyrometer ASIC (2013)
67. Justin Butterfield (2012)
66. Adam Johnson – Methods and Considerations for Testing Resistive Memories (2012)
65. Ben Millemon – CMOS Characterization, Modeling, and Circuit Design in the Presence of Random Local Variation (2012)
64. Justin Wood (2012)
63. Chamunda Ndinawe Chamunda (2011)
62. Gary VanAckern – Design Guide for CMOS Process On-Chip 3D Inductors using Thru-Wafer Vias (2011)
61. Lucien Jan Bissey – High-Voltage Programmable Delta-Sigma Modulation Voltage-Control Circuit (2010)
60. Kaijun Li (2010)
59. Yingting Li (co-supervised with Maria Mitkova) (2010)
58. Lael Matthews (co-supervised with Said Ahmed-Zaid) (2010)
57. Priyanka Mukeshbhai Parikh (2010)
56. Todd Plum (co-supervised with Jeff Jessing) – Design and Fabrication of a Chemicapacitive Sensor for the Detection of Volatile Organic Compounds (2010)
55. Rahul Srikonda (2010)
54. Avani Falgun Trivedi (2010)
53. Kuang Ming Yap – Gain and Offset Error Correction for CMOS Image Sensors using Delta-Sigma Modulation (2010)
52. Mahesh Balasubramanian – Phase Change Memory - Array Development and Sensing Circuits using Delta-Sigma Modulation (2009)
51. Lincoln Bollschweiler (2009)
50. Shantanu Gupta (2009)
49. Qawi Harvard – Wide I/O DRAM Architecture Utilizing Proximity Communication (2009)
48. Avinash Rajagiri (2009)
47. Ramya Ramarapu (2009)
46. Harikrishna Rapole (2009)
45. Aruna Vadla (2009)
44. Hemanth Ande (2008)
43. Curtis Cahoon – Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References (2008)
42. Prashanth Busa (2008)
41. John McCoy III (2008)
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INVITED TALKS (PARTIAL LISTING)

- Harvard, Q. I. and Baker, R. J., "Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design," a presentation covering semiconductor packaging, DRAM architectures, and I/O circuits. The goal of this work is to investigate replacing the currently used dual in-line memory modules (DIMMs) with a smaller and a lower power memory module, a "Nano-Module."
- Baker, R. J., and Campbell, K. A., "Reconfigurable Analog Electronics using the Memristor."
- Baker, R. J., and Saxena, V., "A K-Delta 1-Sigma Modulator for Wideband Analog-to-Digital Conversion."
- Li, K., Saxena, V., and Baker, R. J., "The Baker ADC: An Overview,"
- Saxena, V., and Baker, R. J., "High-Speed Op-Amp Design: Compensation and Topologies for Two and Three Stage Designs,"
- Baker, R. J., "Circuit Design for MLC Flash: Towards a Semiconductor Replacement for the Hard Disk Drive."
- Baker, R. J., Terman Award Acceptance Speech, given at the Frontiers in Education Conference (FIE 2007), Milwaukee, WI, October 11, 2007.
- Baker, R. J., "The One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM), and its Impact on Society," presented at the Franklin Institute, in the symposium honoring Dr. Robert H. Dennard and his receipt of the 2007 Benjamin Franklin Medal in Electrical Engineering, April 25, 2007.
- Baker, R. J. and Saxena, V., "Design of Bandpass Delta-Sigma Modulators: Avoiding Common Mistakes."
- Baker, R. J., "Sensing Circuits for Resistive Memory."
- Hadrick, M. and Baker, R. J., "Sensing in CMOS Imagers using Delta-Sigma Modulation."

- Baker, R. J., "Design of High-Speed CMOS Op-Amps for Signal Processing," IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), April, 2005
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EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services in electrical and computer engineering are listed below. I have been deposed 105 times, given expert testimony at 14 trials (7 USITC, 2 D. Del., 1 Arbitr., 1 S.D. Cal., 1 N.D. Ga., 1 D. Ore., and 1 E.D. Tex.), and participated in 1 mediation.

DLA Piper LLP (Palo Alto, CA and Austin, TX)

Case – BOE Technology Group Co., Ltd. v. Optronics Sciences LLC

Case Numbers – IPR2024-01130, IPR2024-01133, and IPR2024-01134. Petitions filed on July 5, 2024

Case Subject Matter – Imaging pixels, layout, and fabrication. Light emitting devices, including packaging, covers, and structures.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Dentons US LLP (Washington, DC)

Case – Reolink Digital Technology Co., Ltd. v. KT Imaging US, LLC

Case Numbers – IPR2024-01154 and IPR2024-01155. Petitions filed on July 3, 2024

Case Subject Matter – Image sensor structure and package with integrated lens module for digital image products such as digital cameras, camera phones, video phones, fingerprint readers and so on.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/019,560, 90/019,962, and 90/019,964. Requests filed on July 1, 2024

Case Numbers – 90/019,556, 90/019,557, and 90/019,558. Requests filed on June 28, 2024.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for ex parte reviews.

Banner Witcoff (Chicago, IL and Washington, DC)

Case – ZF Friedrichshafen AG, ZF Active Safety and Electronics US LLC, and Nissan Motor Company, Ltd. v. Foras Technologies, Ltd.

Case Number – IPR2024-00969. Petition filed on June 24, 2024.

Case Subject Matter – Detecting loss of lockstep between pairs of processors and loss of lockstep recovery

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Fish & Richardson P.C. (San Diego, CA and Boston, MA)

Case – Vicor Corporation v. Delta Electronics, Inc.

Case Numbers – IPR2024-00704, IPR2024-00705, IPR2024-00706, and IPR2024-00715. Petitions filed on March 25, 2024.

Case Subject Matter – Power converters including design, packaging, heatsinking and manufacturing. Resonant converters with overcurrent protection.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Winston & Strawn LLP (Los Angeles, CA and Redwood City, CA)

Case – Silicon Motion, Inc. v. Unification Technologies LLC

Case Number – IPR2024-00199. Petition filed on December 18, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Garlick & Markison, LLC (Austin, TX)

Case – NXP USA, Inc. v. Bell Semiconductor, LLC

Case Numbers – IPR2024-00167 and IPR2024-00168. Petitions filed on November 9, 2023.

Case Subject Matter – Semiconductor manufacturing processes, fabrication and packaging of integrated circuits, layout and routing of signal lines.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019288. Request filed on October 20, 2023.

Case Subject Matter – Power conversion device to drive an alternating-current motor for an electric vehicle.

Work Performed – Provided expert consulting services and wrote declaration.

Haynes and Boone, LLP (Dallas, TX)

Case – Western Digital Technologies, Inc. v. Longitude Licensing LTD.

Case Number – IPR2023-01200. Petition filed on July 14, 2023.

Case Subject Matter – Communications between a memory controller and memory.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Samsung Electronics Co., Ltd. v. Mojo Mobility, Inc.

Case Numbers – IPR2023-01094, IPR2023-01095, IPR2023-01096, IPR2023-01097, IPR2023-01098, IPR2023-01099, IPR2023-01100, and IPR2023-01124. Petitions filed on June 30, 2023.

Case Numbers – IPR2023-01101 and IPR2023-01102. Petitions filed on June 29, 2023.

Case Numbers – IPR2023-01091, IPR2023-01092, and IPR2023-01093. Petitions filed on June 28, 2023.

Case Numbers – IPR2023-01086, IPR2023-01087, IPR2023-01088, IPR2023-01089, and IPR2023-01090. Petitions filed on June 27, 2023.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Winston & Strawn LLP (Los Angeles, CA, Redwood City, CA, Chicago, IL, and Houston, TX)

Case – Unification Technologies LLC v. Silicon Motion, Inc.

Case Number – Texas, ED (Marshall) 2:23-cv-00267. Complaint filed June 2, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services.

Norton Rose Fulbright LLP (Austin, TX and Dallas, TX)

Case – Current Lighting Solutions, LLC d/b/a GE Current v. Jiaying Super Lighting Electric Appliance Co., Ltd.

Case Numbers – IPR2023-00979 and IPR2023-00980. Petitions filed on May 31, 2023.

Case Number – IPR2023-00270. Petition filed on December 19, 2022.

Case Number – IPR2023-00271. Petition filed on December 14, 2022.

Case Subject Matter – LED lighting, lamps, tube lamps, assembly, and associated circuits and electronics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes review.

Baker Botts LLP (Dallas, TX)

Case – Lennox Industries Inc. v. Rosen Technologies LLC

Case Numbers – IPR2023-00715, IPR2023-00716, IPR2023-00717, IPR2023-00718, and IPR2023-00719. Petitions filed on March 29, 2023.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Cooley LLP (Palo Alto, CA)

Case – Nintendo Co., Ltd. and Nintendo of America Inc. v. Polaris PowerLED Technologies, LLC

Case Number – IPR2023-00778. Petition filed on March 28, 2023.

Case Subject Matter – Visual displays, circuit design, and related technologies.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Bracewell LLP (New York, NY and Seattle, WA)

Case – Kioxia America, Inc. and Kioxia Corporation v. BitMICRO LLC

Case Numbers – IPR2023-00741, IPR2023-00742, and IPR2023-00743. Petitions filed on March 23, 2023.

Case Subject Matter – Solid-state storage devices utilizing multi-profile memory controllers. Optimizing memory operations in a memory system suitable for use in an electronic storage device. Supplying energy to a cache memory using a super capacitor.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Bookoff McAndrews, PLLC (Washington, DC)

Case – Lenovo Inc. and Motorola Mobility LLC v. Theta IP, LLC

Case Numbers – IPR2023-00694, IPR2023-00697, and IPR2023-00698. Petitions filed on March 7, 2023.

Case Subject Matter – Power in wireless communication circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA)

Case – Semiconductor Design Technologies LLC v. Cadence Design Systems, Inc.

Case Number – California, ND 3:23-cv-01001. Complaint filed March 6, 2023.

Case Subject Matter – Semiconductor design support device/method and manufacturing method for semiconductor integrated circuit.

Work Performed – Provided expert consulting services.

McDermott Will & Emery LLP (Chicago, IL and Austin, TX)

Case – Xilinx, Inc. v. Polaris Innovations Limited

Case Numbers – IPR2023-00513 and IPR2023-00514. Petitions filed on February 6, 2023.

Case Subject Matter – Methods for terminating a memory chip with various termination resistances and output drivers for integrated circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Willkie Farr & Gallagher LLP (San Francisco, CA)

Case – Bell Semiconductor, LLC. v. Synopsys, Inc.

Case Number – California, SD 3:22-cv-00594. Complaint filed on January 31, 2023.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services and wrote expert reports.

Fish & Richardson P.C. (Washington, DC, Atlanta, GA, and Boston, MA)

Case – Element Capital Commercial Company PTE. LTD v. BOE Technology Group Co. LTD and Motorola (Wuhan) Mobility

Case Number – Texas, ED (Marshall) 2:22-cv-00118. Complaint filed January 11, 2023.

Case Subject Matter – Display technology, layout, circuit design, pixel design and fabrication.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Baker Botts LLP (San Francisco, CA and New York, NY) and O'Melveny & Myers LLP (Los Angeles, CA)

Case – Polaris PowerLED, LLC v. Samsung Electronics and Samsung Display

Case Number – Texas, ED (Marshall) 2:22-cv-00469. Complaint filed December 12, 2022.

Case Subject Matter – active matrix organic light-emitting diode (AMOLED) displays, controlling the intensity of light-emitting diodes in backlights of displays, control circuits for adjusting current delivery based upon temperature.

Work Performed – Provided expert consulting services including writing a declaration for claim construction.

Arnold & Porter (Los Angeles and Palo Alto, CA) and Willkie Farr & Gallagher LLP (San Francisco, CA)

Case – Synopsys, Inc. and Cadence Design Systems, Inc. v. Bell Semiconductor, LLC.

Case Number – Delaware, 1:22-cv-01512. Complaint filed on November 18, 2022.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/015155 and 90/015156. Requests filed on November 7, 2022.

Case Number – 90/015134. Request filed on October 14, 2022.

Case Number – 90/015130. Request filed on September 30, 2022.

Case Subject Matter – Packaging and fabrication of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declaration.

Russ August & Kabat (Los Angeles, CA)

Case – Resonant Systems, Inc. v. Sony

Case Number – Texas, ED (Marshall) 2:22-cv-00424. Complaint filed on October 26, 2022.

Case Subject Matter – Linear vibration modules and linear-resonant vibration modules.

Work Performed – Provided expert consulting services and wrote claim construction disclosure.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA) and Willkie Farr & Gallagher LLP (San Francisco, CA)

Case – Bell Semiconductor, LLC v. NXP, SMC, Micron, Nvidia, Advanced Micro Devices (AMD), Acer, Infineon, Qualcomm, Motorola Mobility, and Western Digital

Case Number – ITC Investigation No. 337-TA-1340. Complaint filed October 6, 2022.

Case Subject Matter – Electronic devices, semiconductor devices, and components.

Work Performed – Provided expert consulting services.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Daedalus Prime LLC v. Samsung Electronics and Qualcomm Inc.

Case Number – ITC Investigation No. 337-TA-1335. Complaint filed September 12, 2022.

Case Subject Matter – Semiconductor devices, mobile devices, and components.

Work Performed – Provided expert consulting services.

Fish & Richardson P.C. (Boston, MA, Houston, TX, and Washington, DC)

Case – Sonrai Memory LTD. v. Micron Technology, Inc.

Case Number – Texas, WD (Waco) 6:22-cv-00855 and Texas, WD (Waco) 1:23-cv-01407. Complaint filed August 16, 2022.

Case Subject Matter – Portable RAM drive and variable charge pump circuit with dynamic load.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Russ August & Kabat (Los Angeles, CA and New York, NY)

Case – NextGen Innovations, LLC v. Infinera, Fujitsu, AT&T, and Nokia

Case Number – Texas, ED (Marshall) 2:22-cv-00306, Texas, ED (Marshall) 2:22-cv-00307, Texas, ED (Marshall) 2:22-cv-00308, and Texas, ED (Marshall) 2:22-cv-00309. Complaints filed on August 9, 2022.

Case Subject Matter – optical transmission systems including optical components for encoding, transmission (fiber optic transmitters and receivers), and decoding of data and related standards and concepts.

Work Performed – Provided expert consulting services, wrote claim construction disclosure, wrote expert reports, and was deposed twice.

DLA Piper (Chicago, IL and Washington, DC)

Case – Ampt, LLC v. SolarEdge Technologies, Inc.

Case Number – ITC Investigation No. 337-TA-1327. Complaint filed July 28, 2022.

Case Subject Matter – Solar power optimizers, inverters, and components.

Work Performed – Provided expert consulting services including writing declarations for claim construction, expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Signify North America Corporation v. Shenzhen Intellirocks Tech Co.

Case Number – Texas, WD (Waco) 6:22-cv-00760. Complaint filed on July 8, 2022.

Case Subject Matter – LED packaging, circuits, and systems.

Work Performed – Provided expert consulting services including writing declaration for claim construction. Was deposed.

Baker Botts LLP (Dallas, TX)

Case – Rosen Technologies LLC v. Lennox Industries Inc.

Case Number – Texas, ND (Dallas) 3:22-cv-00732. Complaint filed on June 7, 2022.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung Electronics Co., Ltd. v. Scramoge Technology Ltd.

Case Numbers – IPR2022-01052, IPR2022-01053, and IPR2022-01058. Petitions filed on May 26, 2022.

Case Numbers – IPR2022-01054, IPR2022-01055, IPR2022-01056, and IPR2022-01057. Petitions filed on May 24, 2022.

Case Number – IPR2022-00939. Petition filed on April 29, 2022.

Case Subject Matter – An antenna that supports wireless charging using switching power supplies such as flyback converters.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Ex Parte Reexaminations

Case Number – 90/015020. Request filed on May 2, 2022.

Case Number – 90/014906. Request filed on November 12, 2021.

Case Number – 90/014899. Request filed on November 10, 2021.

Case Number – 90/014888. Request filed on October 21, 2021.

Case Numbers – 90/014886 and 90/014887. Requests filed on October 20, 2021.

Case Number – 90/014885. Request filed on October 19, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging.

Work Performed – Provided expert consulting services and wrote declarations.

DLA Piper (Chicago, IL, Austin, TX, and Washington, DC)

Case – SolarEdge Technologies, Inc. v. Fronius International GMBH

Case Number – IPR2022-00849. Petition filed on April 14, 2022.

Case Subject Matter – Mechanical assembly and enclosure whereby an upper housing part is detached from a lower housing part using a “rotate-and-lift” feature.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Kirkland & Ellis LLP (New York, NY)

Case – Samsung Electronics Co. v. Sonrai Memory Ltd.

Case Numbers – IPR2022-00305 and IPR2022-00306. Petitions filed on December 10, 2021.

Case Subject Matter – USB devices and circuits for saving power.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews.

Haynes and Boone, LLP (Washington, DC)

Case – Unified Patents, LLC v. Arigna Technology Limited

Case Number – IPR2022-00285. Petition filed on December 9, 2021.

Case Subject Matter – High voltage driver circuit for driving power devices such as insulated gate bipolar transistors (IGBTs).

Work Performed – Provided expert consulting services, wrote declaration for inter partes review and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Samsung Electronics Co., Ltd. v. Lynk Labs, Inc.

Case Numbers – IPR2022-00149 and IPR2022-00150. Petitions filed on November 12, 2021

Case Numbers – IPR2022-00100 and IPR2022-00101. Petitions filed on October 28, 2021.

Case Numbers – IPR2022-00051, IPR2022-00052, and IPR2022-00098. Petitions filed on October 27, 2021.

Case Numbers – IPR2021-01575 and IPR2021-01576. Petitions filed on October 1, 2021.

Case Numbers – IPR2021-01299, IPR2021-01300, IPR2021-01345, IPR2021-01346, and IPR2021-01347. Petitions filed on September 7, 2021.

Case Subject Matter – Circuit design, including switching power supply design (e.g., flyback), rectifiers, power factor correction, etc. for lighting and displays using light emitting diodes (LEDs).

Work Performed – Provided expert consulting services, wrote declarations, and was deposed ten times.

Haynes and Boone, LLP (Plano, TX)

Case – Pure Storage, Inc. v. Digital Cache, LLC

Case Number – IPR2022-00121. Petition filed on October 29, 2021.

Case Subject Matter – Non-volatile memory (NVM) devices capable of retaining stored data in case of a power failure.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Banner Witcoff (Washington, DC)

Case – SolarEdge Technologies Ltd. v. Koolbridge Solar, Inc.

Case Numbers – IPR2022-00007, IPR2022-00008, IPR2022-00009, IPR2022-00010, IPR2022-00011, and IPR2022-00012. Petitions filed on October 11, 2021.

Case Numbers – IPR2022-00013, IPR2022-00014, and IPR2022-00015. Petitions filed on October 8, 2021.

Case Subject Matter – DC-to-AC converters using full-bridges, multi-level conversion for power systems, and other electronics for harvesting solar energy.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung Electronics Co., Ltd. v. LED Wafer Solutions LLC

Case Number – IPR2021-01554. Petition filed on September 20, 2021.

Case Number – IPR2021-01526. Petition filed on September 10, 2021.

Case Number – IPR2021-01506. Petition filed on September 7, 2021.

Case Number – IPR2021-01491. Petition filed on September 3, 2021.

Case Subject Matter – Packaging of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declarations.

Paul Hastings, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/014,846. Request filed on August 30, 2021.

Case Subject Matter – Wireless power transmission and ways to wirelessly charge and/or discharge a battery.

Work Performed – Provided expert consulting services and wrote declaration.

Jones Day (San Diego, CA and Pittsburgh, PA)

Case – SOLiD, Inc. v. CommScope Technologies LLC

Case Numbers – IPR2021-01390, IPR2021-01391, IPR2021-01392, IPR2021-01393, and IPR2021-01394. Petitions filed on August 12, 2021.

Case Subject Matter – Digital antenna system that enables extension of radio frequency (RF) analog signals from base stations to areas (e.g., inside of buildings) where access to such signals is inhibited.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019,015. Request filed on July 20, 2021.

Case Subject Matter – Voltage-controlled oscillator (VCO) temperature compensation.

Work Performed – Provided expert consulting services and wrote declaration.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC v. Unification Technologies LLC

Case Numbers – IPR2021-00940, IPR2021-00941, and IPR2021-00942. Petitions filed on June 4, 2021.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Kaijet Technology v. Sanho Corporation

Case Number – IPR2021-00886. Petition filed on April 30, 2021.

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services for inter partes review, wrote declaration, was deposed.

O'Melveny & Myers LLP (Los Angeles, CA and New York, NY)

Case – Solas OLED LTD. v. Samsung Electronics Co. LTD.

Case Number – Texas, ED (Marshall) 2:21-cv-00105. Complaint filed March 22, 2021.

Case Subject Matter – Touch-sensors for gesture recognition and signal processing for capacitive touch displays.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

O'Melveny & Myers LLP (San Francisco, CA)

Case – Super Interconnect Technologies LLC v. Google LLC

Case Number – Texas, ED (Marshall) 2:18-cv-00463 (complaint filed November 2, 2018) and Texas, WD (Waco) 6:21-cv-00259 (complaint filed March 15, 2021).

Case Subject Matter – Transmission of data and clock signals. Serial signals such as transition minimized differential signaling. Communications between processors and non-volatile storage such as Universal Flash Storage (UFS) and embedded MultiMedia Controller (eMMC).

Work Performed – Provided expert consulting services and wrote expert reports.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Fundamental Innovation Systems International LLC v. Anker Innovations and Fantasia Trading LLC d/b/a Ankerdirect

Case Number – Delaware, 1:21-cv-00339. Complaint filed on March 5, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – TCT Mobile Inc. and TCL Communication, Inc. v. Fundamental Innovation Systems International LLC

Case Numbers – IPR2021-00597, IPR2021-00598, and IPR2021-00599. Petitions filed on February 26, 2021.

Case Number – IPR2021-00428. Petition filed on January 13, 2021.

Case Number – IPR2021-00410. Petition filed on January 11, 2021.

Case Number – IPR2021-00395. Petition filed on December 31, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews. Was deposed twice.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung, Inc. v. Pictos Technologies, Inc.

Case Number – IPR2021-00557. Petition filed on February 18, 2021.

Case Number – IPR2021-00436. Petition filed on January 19, 2021.

Case Numbers – IPR2021-00437 and IPR2021-00438. Petitions filed on January 15, 2021.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

O'Melveny & Myers LLP (San Francisco, CA) and DLA Piper (New York, NY)

Case – Solas OLED Ltd. v. BOE Technology Group Co. Ltd. and Samsung Electronics

Case Number – ITC Investigation No. 337-TA-1243. Complaint filed January 5, 2021.

Case Subject Matter – Active matrix OLED display devices and components

Work Performed – Provided expert consulting services, wrote expert reports, was deposed, and testified at trial.

Paul Hastings LLP (Washington, DC)

Case – Samsung, Inc. v. Garrity Power Services LLC

Case Number – IPR2021-00389. Petition filed on December 31, 2020.

Case Subject Matter – Power electronics including full-bridge PWM modules for wireless power transmission using magnetic coupling via antennas and transformers. Design of inductors and coils.

Work Performed – Provided expert consulting services and wrote declaration for inter partes reviews.

Morgan, Lewis & Bockius LLP (Palo Alto, CA and Shanghai, CN)

Case – Monolithic Power Systems, Inc. v. Meraki Integrated Circuit Technology, Inc. and Promate Electronic Company, LTD.

Case Number – Texas, WD (Waco) 6:20-cv-00876. Complaint filed on December 24, 2020.

Case Subject Matter – Design of switching power supplies including synchronous rectification.

Work Performed – Provided expert consulting services including declaration for claim construction, trade secret analysis and declaration, and Markman tutorial.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC; Dell Technologies Inc.; Dell Inc.; and HP Inc. v. Unification Technologies LLC

Case Numbers – IPR2021-00343, IPR2021-00344, and IPR2021-00345. Petitions filed on December 22, 2020.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews, wrote declarations, and was deposed.

Jones Day (Chicago, IL and Dallas, TX)

Case – WSOU Investments, LLC d/b/a Brazos Licensing and Development v. Xilinx, Inc.

Case Numbers – Delaware, 1:20-cv-01231 and Delaware, 1:20-cv-01233. Complaints filed on November 23, 2020 and September 16, 2020.

Case Subject Matter – Controlling power cycles in communication devices and transferring multiple asynchronous clock signals.

Work Performed – Provided expert consulting services, wrote claim construction declaration, wrote expert reports, and was deposed.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Cosemi Technologies, Inc. v. EverPro Technologies, Fibbr Technologies, Logitech, Inc., and Facebook Technologies

Case Number – ITC Investigation No. 337-TA-1233. Complaint filed October 28, 2020.

Case Subject Matter – Data cables, including HDMI, Display Port, and USB Type A, USB Type C and USB Type A/C data cables.

Work Performed – Provided expert consulting services.

Kirkland & Ellis LLP (Boston, MA and New York, NY)

Case – Pictos Technologies, Inc. v. Samsung Electronics Co., LTD. and Samsung Semiconductor, Inc.

Case Number – ITC Investigation No. 337-TA-1231. Complaint filed September 25, 2020.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, correction of bad pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote expert report.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Fundamental Innovation Systems International LLC v. TCT Mobile Inc. and TCL Communication, Inc.

Case Number – Delaware, 1:20-cv-00552. Complaint filed on September 11, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations, expert report on invalidity, and was deposed.

Walters Wilson LLP (Redwood City, CA)

Case – Western Digital Corporation and SanDisk, LLC v. Martin Kuster

Case Numbers – IPR2020-01410 and IPR2020-01411. Petitions filed on August 3, 2020.

Case Subject Matter – Computer connectors such as universal serial bus (USB) that connect to peripheral devices such as mice, keyboards, displays, printers, external storage, etc.

Work Performed – Provided expert consulting services for inter partes review, wrote declarations and was deposed.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Advanced Micro Devices, Inc. v. Monterey Research, LLC

Case Number – IPR2020-01315. Petition filed on July 16, 2020.

Case Number – IPR2020-00985. Petition filed on May 26, 2020.

Case Subject Matter – Reading and writing to semiconductor memory such as SRAM and double data rate (DDR) DRAM. Buffer circuits with variable current supplies for controlling the rise and fall times of output signals.

Work Performed – Provided expert consulting services for inter partes review, wrote declarations and was deposed twice.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Unification Technologies LLC v. Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC

Case Number – Texas, WD (Waco) 6:20-cv-00500. Complaint filed June 5, 2020.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, and was deposed.

Ari Law, P.C. (Palo Alto, CA) and Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Sanho Corporation v. Kaijet Technology, Magic Control Technology, and Star View Global

Case Numbers – Georgia, ND (Atlanta) 1:18-cv-05385 (third amended complaint filed November 14, 2019) and Georgia, ND (Atlanta) 1:20-cv-02150 (filed May 19, 2020).

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, and expert reports. Was deposed and testified at trial.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Fundamental Innovation Systems International LLC v. Coolpad Group Limited, Coolpad Technologies, Inc., and Yulong Computer Telecommunication Scientific Co. Ltd.

Case Number – Texas, ED (Marshall) 2:20-cv-00117. Complaint filed on April 23, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA and Shanghai, China)

Case – SMIC, Americas v. Innovative Foundry Technologies LLC

Case Numbers – IPR2020-00837 and IPR2020-00839. Petitions filed on April 14, 2020.

Case Subject Matter – Methods of manufacturing a semiconductor component, such as a short-channel MOS device, including forming graded-junctions using spacers along the sidewalls of a transistor's gate.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Russ August & Kabat (Los Angeles, CA)

Case – Oyster Optics, LLC v. Ciena Corporation

Case Number – California, ND (Oakland) 3:20-cv-02354. Complaint filed on April 7, 2020.

Case Subject Matter – Fiber optic telecommunication systems.

Work Performed – Provided expert consulting services, wrote claim construction declaration, and was deposed.