

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court **Western District of Texas** on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 6:23-cv-307	DATE FILED 4/26/2023	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF Intellectual Ventures I LLC and Intellectual Ventures II LLC		DEFENDANT Lenovo Group Limited
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,325,140	1/29/2008	Intellectual Ventures II LLC
2 8,474,016	6/25/2013	Intellectual Ventures II LLC
3 7,089,443	8/8/2006	Intellectual Ventures I LLC
4 7,623,439	11/24/2009	Intellectual Ventures I LLC
5 7,646,835	1/12/2010	Intellectual Ventures II LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
1			
2			
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
-------	-------------------	------

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:23-cv-293	DATE FILED 4/20/2023	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF Intellectual Ventures I and Intellectual Ventures II		DEFENDANT TCL Electronics Holdings Ltd. and TCL Industries Holdings Co., Ltd.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,089,443	8/8/2006	Intellectual Ventures II
2 7,623,439	11/24/2009	Intellectual Ventures I
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court **Western District of Texas** on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:23-cv-309	DATE FILED 4/26/2023	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF Intellectual Ventures I LLC		DEFENDANT TCL Electronics Holdings Ltd. and TCL Industries Holdings Co., Ltd.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,089,443	8/8/2006	Intellectual Ventures I
2 7,623,439	11/24/2009	Intellectual Ventures I
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
-------	-------------------	------

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,089,443 B2
APPLICATION NO. : 10/762550
DATED : August 8, 2006
INVENTOR(S) : Albonesi et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 17, line 9, in Claim 1, delete “multiple-clock-domain” and insert -- multiple clock domain --.

Column 17, line 9, in Claim 1, delete “microprpcessor” and insert -- microprocessor --.

Column 18, line 25, in Claim 10, delete “one” and insert -- two --.

Column 18, line 33, in Claim 11, delete “Emply” and insert -- Empty --.

Signed and Sealed this
Fourteenth Day of June, 2011

A handwritten signature in black ink that reads "David J. Kappos". The signature is written in a cursive, flowing style with a large initial "D" and a stylized "K".

David J. Kappos
Director of the United States Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : 7,089,443 B2
APPLICATION NO.: 10/762,550
ISSUE DATE : August 8, 2006
INVENTOR(S) : Albonesi et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 17, line 9, in Claim 1, delete "multiple-clock-domain" and insert - - multiple clock domain - -.

Column 17, line 9, in Claim 1, delete "microprpcessor" and insert - - microprocessor - -.

Column 18, line 25, in Claim 10, delete "one" and insert - - two - -.

Column 18, line 33, in Claim 11, delete "Empty" and insert - - Empty - -.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	10762550			
Filing Date:	23-Jan-2004			
Title of Invention:	MULTIPLE CLOCK DOMAIN MICROPROCESSOR			
First Named Inventor/Applicant Name:	David Albonesi			
Filer:	Blayne Donnis Green/Lindsey Hunt			
Attorney Docket Number:	2493-0010			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of correction	1811	1	100	100
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				100

Electronic Acknowledgement Receipt

EFS ID:	10108284
Application Number:	10762550
International Application Number:	
Confirmation Number:	3210
Title of Invention:	MULTIPLE CLOCK DOMAIN MICROPROCESSOR
First Named Inventor/Applicant Name:	David Albonesi
Customer Number:	73552
Filer:	Blayne Donnis Green/Lindsey Hunt
Filer Authorized By:	Blayne Donnis Green
Attorney Docket Number:	2493-0010
Receipt Date:	17-MAY-2011
Filing Date:	23-JAN-2004
Time Stamp:	15:11:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 100
RAM confirmation Number	1522
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Request for Certificate of Correction	CoC_7089443.pdf	80889 3c946efb4ad3958cc6c7be5ea9cbd555c2409f95	no	2
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	30191 841d1069a4eb93eeefb191fae38e0223c1f2aac	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			111080		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/762,550

Patent No: 7,089,443

Filed: 1/23/2004

Issued: 8/8/2006

Confirmation No.: 3210

For: MULTIPLE CLOCK DOMAIN MICROPROCESSOR

FILED VIA EFS
COMMISSIONER FOR PATENTS

**NOTIFICATION OF LOSS OF ENTITLEMENT TO SMALL ENTITY STATUS
UNDER 37 CFR 1.27(g)(2)**

Applicant hereby notifies the U.S. Patent and Trademark Office of the loss of entitlement to small entity status.

Customer No. 73552

Respectfully submitted,

STOLOWITZ FORD COWGER LLP

/Graciela G. Cowger/

Graciela G. Cowger

Reg. No. 42,444

STOLOWITZ FORD COWGER LLP
621 SW Morrison Street, Suite 600
Portland, OR 97205
(503) 224-2170

Date: November 4, 2008

Electronic Acknowledgement Receipt

EFS ID:	4231125
Application Number:	10762550
International Application Number:	
Confirmation Number:	3210
Title of Invention:	MULTIPLE CLOCK DOMAIN MICROPROCESSOR
First Named Inventor/Applicant Name:	David Albonesi
Customer Number:	73552
Filer:	Stephen Scott Ford/Heather Kulin
Filer Authorized By:	Stephen Scott Ford
Attorney Docket Number:	2493-0010
Receipt Date:	04-NOV-2008
Filing Date:	23-JAN-2004
Time Stamp:	16:49:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2493-0010_Loss_of_Entity.pdf	54929 d07ae6232129040067ad1497a14411a441563fc7	no	1

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/762,550	01/23/2004	David Albonesi	2493-0010

73552
Stolowitz Ford Cowger LLP
621 SW Morrison St
Suite 600
Portland, OR 97205

CONFIRMATION NO. 3210
POA ACCEPTANCE LETTER



Date Mailed: 10/29/2007

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/18/2007.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/sibrahim/

Office of Initial Patent Examination (571) 272-4000 or 1-800-PTO-9199

PATENT APPLICATION
Docket. No. 2493-0010**TRANSMITTAL LETTER - POWER OF ATTORNEY**

In re application of: ALBONESI DAVID H., SEMERARO GREG, MAGKLIS
GRIGORIOS, SCOTT MICHAEL L., BALASUBRAMONIAN RAJEEV and
DWARKADAS SANDHYA

**RECEIVED
CENTRAL FAX CENTER**

OCT 18 2007

Application No.: 10/762,550

Filing Date: 1/23/2004

Patent No. 7,089,443

Issue Date: 8/8/2006

Title: MULTIPLE CLOCK DOMAIN MICROPROCESSOR

COMMISSIONER FOR PATENTS
VIA FAX 571-273-8300

TOTAL PAGES (including this cover sheet): 3

Attached are:

- ☒ Power of Attorney to Prosecute Applications Before the PTO.
- ☒ Statement Under 37 CFR 3.73b.

Respectfully submitted,

STOLOWITZ FORD COWGER LLP

/Graciela G. Cowger/
Graciela G. Cowger
Reg. No. 42,444

STOLOWITZ FORD COWGER LLP
621 SW Morrison Street, Suite 600
Portland, Oregon 97205

Customer No. 73552

Page 1 of 3

PATENT APPLICATION
Docket. No. 2493-0010

STATEMENT UNDER 37 CFR 3.73 (b)

In re application of: ALBONESI DAVID H., SEMERARO GREG, MAGKLIS GRIGORIOS,
SCOTT MICHAEL L., BALASUBRAMONIAN RAJEEV and DWARKADAS SANDHYARECEIVED
CENTRAL FAX CENTER

OCT 18 2007

Application No.: 10/762,550

Filing Date: 1/23/2004

Patent No. 7,089,443

Issue Date: 8/8/2006

Title: MULTIPLE CLOCK DOMAIN MICROPROCESSOR

University of Rochester, whose principal place of business is located at 518 Hylan Building, Box 270140,
Rochester NY 14627-0140, states that it is:

1. ☒ the assignee of the entire right, title and interest; or
2. ☐ an assignee of less than the entire right, title and interest
The extent (by percentage) of its ownership is _____%

in the patent application/patent identified above by virtue of either:

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 016031, Frame 0516

OR

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

1. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____.
2. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____.
3. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____.

☐ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.
[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is empowered to sign this statement on behalf of the assignee.

Date: 10/18/2007 Signature /Graciela G. Cowger/
GRACIELA G. COWGER, PTO Reg. No. 42,444
Attorney for Assignee

RECEIVED
CENTRAL FAX CENTER

OCT 18 2007

PTO/SB/90 (01-08)

Approved for use through 12/31/2008. OMB 0951-0035

U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☒ Practitioners associated with the Customer Number:

73552

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☒

The address associated with Customer Number:

73552

OR

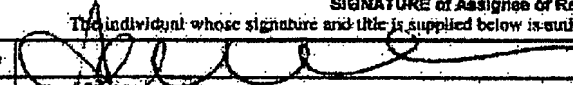
☐ Firm or Individual Name:			
Address			
City	State	Zip	
Country			
Telephone	Email		

Assignee Name and Address: University of Rochester
518 Hylan Building
Box 370140
Rochester, NY 14627-0140

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/90 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

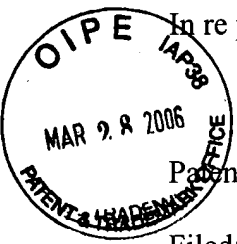
Signature: 	Date: 10/11/2007
Name: Gail Morris	Telephone: 585-275-5370
Title: Director, Office of Technology Transfer	

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.31 and 1.34. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Times will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1480. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1480, Alexandria, VA 22313-1480.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

ZZW
DAG
\$

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re patent application of	)	
David Albonesi et al.	)	Art Unit: 2115
Patent Application No.: 10/762,550	)	Examiner: Dennis Butler
Filed: January 23, 2004	)	Docket No.: 000687-00324
Confirmation No. 3210	)	Allowed: May 19, 2005
Title: Multiple Clock Domain Microprocessor	)	Issue Fee Paid: August 19, 2005
	)	Date: March 28, 2006

PAYMENT OF FEE DEFICIENCY UNDER 37 C.F.R. §1.28(c)(1) AND (2)

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

University of Rochester, the Assignee of the above-identified patent application, through undersigned counsel, hereby submits a check in the amount of \$700.00 to cover the deficiency in the Issue Fee that were incorrectly paid in good faith at the small entity rate on August 19, 2005:

Issue Fee:

Large Entity Issue Fee: \$1,400.00

Amount of Issue Fee paid on August 25, 2005: \$ 700.00

Deficiency owed:

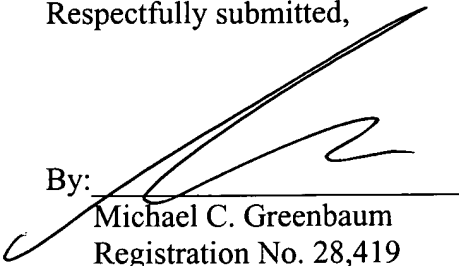
Total deficiency owed:

Adjustment date: 03/30/2006 MREYENE2
08/23/2005 SDENB082 00000013 10762550
01 FC:2501 \$ 700.00 -700.00 OP

03/30/2006 MREYENE2 00000002 10762550
01 FC:1501 1400.00 OP

It is believed that no additional fee is required in connection with this application. However, if such a fee is required, the Commissioner is authorized to charge Blank Rome LLP, Deposit Account No. 23-2185 (000687-00324).

Respectfully submitted,

By: 

Michael C. Greenbaum
Registration No. 28,419

BLANK ROME LLP
The Watergate
600 NEW HAMPSHIRE AVENUE, NW
Washington, D.C. 20037
(202) 772-5800 (Phone)
(202) 572-8398 (Facsimile)



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of	)	
	)	
David Albonesi et al.	)	Art Unit: 2115
	)	
Patent Application No.: 10/762,550	)	Examiner: Dennis Butler
	)	
Filed: January 23, 2004	)	Docket No.: 000687-00324
	)	
Confirmation No. 3210	)	Allowed: May 19, 2005
	)	Issue Fee Paid: August 19, 2005
Title: Multiple Clock Domain Microprocessor	)	
	)	Date: March 28, 2006

COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

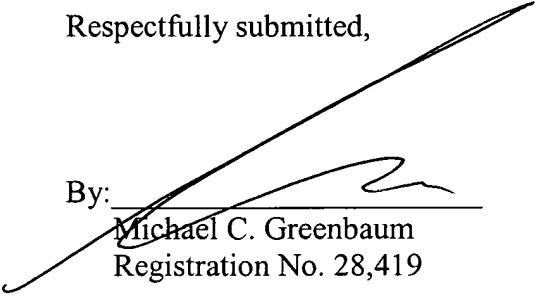
It is respectfully requested that the following comments on Statement for Reasons for Allowance be entered into the record for the above-referenced patent application.

The Examiner's Statements of Reasons for Allowance are hereby acknowledged by Assignee. Assignee agrees that the claimed subject matter is patentably distinct from the documents cited by the Examiner; however, Assignee takes no position regarding the reasons for allowance presented by the Examiner, other than the positions previously taken during prosecution of the above-referenced patent application. Therefore, the Examiner's reasons for allowance should not be attributed to Assignee as an indication of the basis for Assignee's belief that the claims are patentably distinct. Furthermore, it is respectfully asserted that there may also be additional reasons for patentability of the claimed subject matter not explicitly stated in this

record. While in accordance with 37 C.F.R. §1.104(e), a failure by the Assignee to disagree with the Examiner, or file more detailed comments, does not give rise to any implication that the Assignee agrees with or acquiesces in the reasoning of the Examiner, here, by this document, Assignee is expressly making clear that no such agreement or acquiesce is present.

If the Examiner has any questions, he is invited to contact the undersigned. It is believed that no fee is due in connection with this filing. However, if such a fee is due, the Commissioner if authorized to charge any additional fee to Deposit Account number 23-2185 (000687-00324).

Respectfully submitted,

By: 

Michael C. Greenbaum
Registration No. 28,419

BLANK ROME LLP
The Watergate
600 NEW HAMPSHIRE AVENUE, NW
Washington, D.C. 20037
(202) 772-5800 (Phone)
(202) 572-8398 (Facsimile)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or Fax (703) 746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below. Otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27557 7590 05/19/2005

BLANK ROME LLP
 600 NEW HAMPSHIRE AVENUE, N.W.
 WASHINGTON, DC 20037

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,550	01/23/2004	David Albonesi	000687-00324	3210

TITLE OF INVENTION: MULTIPLE CLOCK DOMAIN MICROPROCESSOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$300	\$1000	08/19/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
BUTLER, DENNIS	2115	713-500000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Blank Rome LLP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

University of Rochester

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Rochester, New York

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

- ☒ A check in the amount of the fee(s) is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 23-2185 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously applied fees to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

08/23/2005 08:00:00 0000013 10/762550
 01 FC:2501 700.00 OP
 02 FC:1504 300.00 OP

Authorized Signature

Date August 19, 2005

Typed or printed name Michael C. Greenbaum

Registration No. 28,419

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number

10762550

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	3	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	3 minus 20 =	*
INDEPENDENT CLAIMS	2 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	3	20	=
Independent	2	3	= 1
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total			=
Independent			=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total			=
Independent			=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

- * If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 - ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
 - *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
- The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY TYPE ☐

OR OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	385.00
X\$ 9=	
X43=	
+145=	
TOTAL	385

RATE	FEE
BASIC FEE	770.00
X\$18=	
X86=	
+290=	
TOTAL	

SMALL ENTITY

OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
X\$ 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$ 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$ 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27557 7590 05/19/2005

BLANK ROME LLP
600 NEW HAMPSHIRE AVENUE, N.W.
WASHINGTON, DC 20037

EXAMINER

BUTLER, DENNIS

ART UNIT

PAPER NUMBER

2115

DATE MAILED: 05/19/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,550	01/23/2004	David Albonesi	000687-00324	3210

TITLE OF INVENTION: MULTIPLE CLOCK DOMAIN MICROPROCESSOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$300	\$1000	08/19/2005

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
- B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
- B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail**

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27557 7590 05/19/2005

**BLANK ROME LLP
600 NEW HAMPSHIRE AVENUE, N.W.
WASHINGTON, DC 20037**

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,550	01/23/2004	David Albonesi	000687-00324	3210

TITLE OF INVENTION: MULTIPLE CLOCK DOMAIN MICROPROCESSOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$300	\$1000	08/19/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
BUTLER, DENNIS	2115	713-500000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
 1 _____
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
 NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,550	01/23/2004	David Albonesi	000687-00324	3210
27557	7590	05/19/2005	EXAMINER	
BLANK ROME LLP 600 NEW HAMPSHIRE AVENUE, N.W. WASHINGTON, DC 20037			BUTLER, DENNIS	
			ART UNIT	PAPER NUMBER
			2115	

DATE MAILED: 05/19/2005

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571) 272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

Notice of Allowability

Application No.

10/762,550

Examiner

Dennis M. Butler

Applicant(s)

ALBONESI ET AL

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment received on March 4, 2005.
2. ☒ The allowed claim(s) is/are 4-15.
3. ☒ The drawings filed on 23 January 2004 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 - * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date 03042005
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Art Unit: 2115

1. This action is in response to the amendment that was received on March 4, 2005. Claims 4-15 are pending. Claims 1-3 have been canceled. Claims 4-15 have been added.

2. The following is an examiner's statement of reasons for allowance:

The cited prior art describe systems that change the voltage and frequency of components in data processing systems. Gary et al (2004/0025069) describe that voltage and clock domains are known in Table 1 at the top of page 2. Gary et al does not describe the domains in a microprocessor and does not describe dynamically controlling the clock frequency and voltage in each domain independently of the clock frequencies and voltages in each of the other domains. Tam et al describe dynamically varying clock frequency to adapt to changes in Vcc. Tam et al does not describe a plurality of domains in a microprocessor or using their system in a microprocessor having a plurality of domains.

The claimed invention is allowable over the art of record because the art of record does not teach or suggest a method or apparatus for dynamically controlling the clock frequency and voltage in a microprocessor having a plurality of domains comprising a microprocessor having a plurality of domains, each domain having a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independent of the clock frequencies in each of the other domains and each domain having a voltage input for receiving a voltage that is dynamically changeable independent

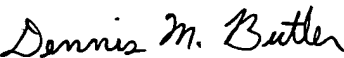
Art Unit: 2115

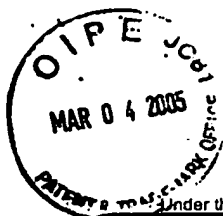
of the voltage applied to each of the other domains as claimed in independent claims 4 and 11.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 571-272-3663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Dennis M. Butler
Primary Examiner
Art Unit 2115



PTO/SB/08a
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	10/762,550 (Conf. No. 3210)
Filing Date	January 23, 2004
First Named Inventor	David Albonesi
Art Unit	2115
Examiner Name	Not yet assigned
Attorney Docket Number	000687-00324

Sheet

1

of

1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
DmB		US-6,487,675 B2	11-26-2002	Sager et al	Fig. 4; col. 4, lines 3-20; col. 5, lines 7-50; col. 6, lines 9-25
		US-6,463,547 B1	10-08-2002	Bailey et al	
		US-6,047,382 A	04-04-2000	Maley et al	
		US-5,796,995 A	08-18-1998	Nasserbakht et al	Fig. 4; col. 7, lines 28-62
		US-5,710,910 A	01-20-1998	Kehl et al	Col. 3, line 13-col. 5, line 50
DmB		US-5,309,561 A	05-03-1994	Overhouse et al	Col. 2, line 53-col. 4, line 59
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

Examiner
Signature

Dennis M. Butler

Date
Considered

5-13-05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Notice of References Cited	Application/Control No. 10/762,550	Applicant(s)/Patent Under Reexamination ALBONESI ET AL	
	Examiner Dennis M. Butler	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2004/0017234	01-2004	Tam et al.	327/141
	B	US-2004/0025069	02-2004	Gary et al.	713/300
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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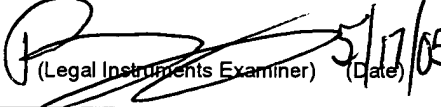
NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification 	Application/Control No.		Applicant(s)/Patent under Reexamination	
	10/762,550		ALBONESI ET AL	
	Examiner		Art Unit	
	Dennis M. Butler		2115	

ISSUE CLASSIFICATION										
ORIGINAL					CROSS REFERENCE(S)					
CLASS		SUBCLASS			CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
713		501			713	322	600			
INTERNATIONAL CLASSIFICATION										
G	0	6	F	1/04						
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_____ (Assistant Examiner) (Date)		Dennis M. Butler Primary Examiner <i>Dennis M. Butler</i> 5-13-05 (Primary Examiner) (Date)		Total Claims Allowed: 12	
 (Legal Instruments Examiner) (Date)				O.G. Print Claim(s) 1	O.G. Print Fig. 1

☐ Claims renumbered in the same order as presented by applicant										☐ CPA		☐ T.D.		☐ R.1.47		
Final	Original		Final	Original		Final	Original		Final	Original		Final	Original		Final	Original
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	2			32			62			122			152			182
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3	6			36			66			126			156			186
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	29			59			89			149			179			209
	30			60			90			150			180			210

Search Notes

Application/Control No.

10/762,550

Examiner

Dennis M. Butler

Applicant(s)/Patent under
Reexamination

ALBONESI ET AL

Art Unit

2115

SEARCHED

Class	Subclass	Date	Examiner
713	322,500, 501,600	11/8/2004	DMB
713	322,500	5/13/2005	DMB
713	320,501	5/13/2005	DMB
713	600	5/13/2005	DMB

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner
713	501,600	5/13/2005	DMB
713	322	5/13/2005	DMB

**SEARCH NOTES
(INCLUDING SEARCH STRATEGY)**

	DATE	EXMR
EAST searh for related case PCT/US2004/001700	5/13/2005	DMB
EAST	5/13/2005	DMB

Index of Claims



Application/Control No.

10/762,550

Examiner

Dennis M. Butler

Applicant(s)/Patent under Reexamination

ALBONESI ET AL

Art Unit

2115

✓	Rejected
=	Allowed

—	(Through numeral) Cancelled
+	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date						
Final	Original	5/13/05						
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UNITED STATES PATENT AND TRADEMARK OFFICE

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 www.uspto.gov



Bib Data Sheet

CONFIRMATION NO. 3210

SERIAL NUMBER 10/762,550	FILING DATE 01/23/2004 RULE	CLASS 713	GROUP ART UNIT 2115	ATTORNEY DOCKET NO. 000687-00324
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APPLICANTS

David Albonesi, Rochester, NY;

Greg Semeraro, Fairport, NY;
 Grigorios Magklis, Barcelona, SPAIN; Michael L. Scott, Rochester, NY;
 Rajeev Balasubramonian, Rochester, NY;
 Sandhya Dwarkadas, Rochester, NY;

** CONTINUING DATA ***** DMB
 This appln claims benefit of 60/441,759 01/23/2003

** FOREIGN APPLICATIONS ***** DMB
 none

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
 ** 12/07/2004

Foreign Priority claimed 35 USC 119 (a-d) conditions met	☐ yes ☒ no ☐ yes ☒ no ☐ Met after Allowance	STATE OR COUNTRY NY	SHEETS DRAWING 8	TOTAL CLAIMS 3	INDEPENDENT CLAIMS 2
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Verified and Acknowledged Dennis M. Butler
 Examiner's Signature Initials

ADDRESS
 27557
 BLANK ROME LLP
 600 NEW HAMPSHIRE AVENUE, N.W.
 WASHINGTON , DC
 20037

TITLE
 Multiple clock domain microprocessor

FILING FEE	FEES: Authority has been given in Paper	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of
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	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	563126	processor or microprocessor	US-PGPUB; USPAT	2005/05/13 16:50
2	BRS	L2	2207	clock adj2 domain	US-PGPUB; USPAT	2005/05/13 16:51
3	BRS	L3	2367	voltage near5 domain	US-PGPUB; USPAT	2005/05/13 16:51
4	BRS	L4	483	1 same 2	US-PGPUB; USPAT	2005/05/13 16:52
5	BRS	L5	100	1 same 3	US-PGPUB; USPAT	2005/05/13 16:52
6	BRS	L6	6	4 and 5	US-PGPUB; USPAT	2005/05/13 16:55
7	BRS	L7	11	4 and 3	US-PGPUB; USPAT	2005/05/13 16:55
8	BRS	L8	5	7 not 6	US-PGPUB; USPAT	2005/05/13 17:08
9	BRS	L9	6523	local\$2 adj3 clock\$1	US-PGPUB; USPAT	2005/05/13 17:13
10	BRS	L10	51	4 and 9	US-PGPUB; USPAT	2005/05/13 17:14
11	BRS	L11	1330	713/500.ccls. 713/501.ccls.	US-PGPUB; USPAT	2005/05/13 17:15
12	BRS	L12	2087	713/600.ccls. 713/320.ccls. 713/322.ccls.	US-PGPUB; USPAT	2005/05/13 17:15
13	BRS	L13	3135	11 or 12	US-PGPUB; USPAT	2005/05/13 17:16
14	BRS	L14	6	10 and 13	US-PGPUB; USPAT	2005/05/13 17:23
15	BRS	L15	215958	(block section module) same 1	US-PGPUB; USPAT	2005/05/13 17:25

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L16	75063	(block section module) near5 (speed clock)	US-PGPUB; USPAT	2005/05/13 17:31
17	BRS	L17	56603	(block section module) near5 voltage	US-PGPUB; USPAT	2005/05/13 17:31
18	BRS	L18	2460	15 and 16 and 17	US-PGPUB; USPAT	2005/05/13 17:32
19	BRS	L19	8050	clock near5 distribut\$3	US-PGPUB; USPAT	2005/05/13 17:32
20	BRS	L20	19530	voltage near5 distribut\$3	US-PGPUB; USPAT	2005/05/13 17:32
21	BRS	L21	36	18 and 19 and 20	US-PGPUB; USPAT	2005/05/13 17:33
22	BRS	L22	3	13 and 21	US-PGPUB; USPAT	2005/05/13 17:38
23	BRS	L23	33	21 not 22	US-PGPUB; USPAT	2005/05/13 17:38

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number

10762550

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	3	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	3 minus 20 =	*
INDEPENDENT CLAIMS	2 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY
TYPE ☐

OR OTHER THAN
SMALL ENTITY

RATE	FEE
BASIC FEE	385.00
X\$ 9=	
X43=	
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TOTAL	385

RATE	FEE
BASIC FEE	770.00
X\$18=	
X86=	
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TOTAL	

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	3 Minus	20 =
	Independent	2 Minus	3 = 1
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐		

SMALL ENTITY OR

OTHER THAN
SMALL ENTITY

RATE	ADDITIONAL FEE
X\$ 9=	
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+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
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+290=	
TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
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	Independent	Minus	=
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TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
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+290=	
TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
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	Independent	Minus	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐		

RATE	ADDITIONAL FEE
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+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

- * If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 - ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
 - *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
- The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Patent and Trademark Office U.S. DEPARTMENT OF COMMERCE



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of	)	
	)	
David Albonesi et al.	)	Art Unit: 2115
	)	
Patent Application No. 10/762,550	)	Examiner: Not yet known
	)	
Filed: January 23, 2004	)	Attorney Docket No.:
	)	000687-00324
Confirmation No. 3210	)	
	)	
Title: Multiple Clock Domain Microprocessor	)	

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Before examination on the merits, please amend the above-captioned patent application
as follows.

Amendments to the claims begin on page 2 of the present Amendment.

Remarks begin on page 5 of the present Amendment.

In the claims:

Please amend the claims as follows:

1-3. (Canceled)

4. (New) A multiple-clock-domain microprocessor comprising:

a plurality of domains;

for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and

for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

5. (New) The microprocessor of claim 4, wherein each said clock comprises a phase-locked loop, and wherein the microprocessor further comprises means for receiving an externally generated clock signal and for supplying the externally generated clock signal to each said phase-locked loop.

6. (New) The microprocessor of claim 4, wherein there are at least four of said domains.

7. (New) The microprocessor of claim 4, wherein the microprocessor is programmed to determine a slack in processing in one of the domains and to reduce the clock frequency and the voltage in said one of the domains to reduce the slack.

8. (New) The microprocessor of claim 4, further comprising a queue for communication between at least two of the domains.

9. (New) The microprocessor of claim 8, wherein the queue has a *Full* flag and an *Empty* flag, and wherein the microprocessor is programmed to prevent a write to the queue when

the *Full* flag is asserted, until the *Full* flag is deasserted; and to prevent a read from the queue when the *Empty* flag is asserted, until the *Empty* flag is deasserted.

10. (New) The microprocessor of claim 9, wherein the queue is implemented as a dual-ported SRAM.

11. (New) A method of operating a microprocessor, the method comprising:

(a) providing a plurality of domains in the microprocessor;

(b) clocking each of the domains separately at a clock frequency;

(c) applying a voltage to each of the domains separately;

(d) operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another; and

(e) dynamically controlling the clock frequency and the voltage in each of the plurality of domains independently of the clock frequencies and the voltages in others of the plurality of domains.

12. (New) The method of claim 11, wherein step (e) comprises:

(i) determining a slack in processing in one of the domains; and

(ii) reducing the clock frequency and the voltage in said one of the domains to reduce the slack.

13. (New) The method of claim 11, wherein step (d) comprises providing a queue for communication between at least two of the domains.

14. (New) The method of claim 13, wherein the queue has a *Full* flag and an *Empty* flag, and wherein step (d) further comprises:

preventing a write to the queue when the *Full* flag is asserted, until the *Full* flag is deasserted; and

preventing a read from the queue when the *Empty* flag is asserted, until the *Empty* flag is deasserted.

15. (New) The method of claim 11, wherein there are at least four of said domains.

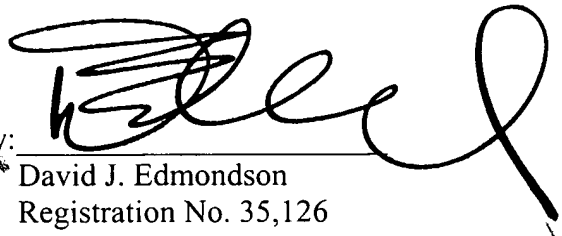
REMARKS

The present Preliminary Amendment has been submitted to improve claim coverage. No new matter has been added.

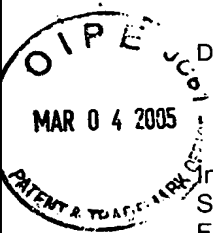
If there are any questions about the Preliminary Amendment or about the application in general, the Office is invited to contact the undersigned at the telephone number set forth below.

Please charge any deficiency in fees, or credit any overpayment thereof, to the deposit account of Blank Rome LLP, Deposit Account No. 23-2185 (000687-00324).

Respectfully submitted,

By: 
David J. Edmondson
Registration No. 35,126

BLANK ROME LLP
The Watergate
600 NEW HAMPSHIRE AVENUE, NW
Washington, D.C. 20037
(202) 772-5800 (Phone)
(202) 572-8398 (Facsimile)



Docket No. 000687-00324

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: David Albonesi et al
Serial No: 10/762,550
Filed: January 23, 2004
For: Multiple clock domain microprocessor

GAU: 2115
Confirmation No. 3210
Examiner: Not yet assigned

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ☐ Attached is a copy of applicant's pending application(s) or issued patent(s) which may be related to the present application. These documents are listed on form PTO-1449, also attached.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☒ Each item of information contained in this information disclosure statement was cited for the first time in any communication from a foreign patent office in any counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited for the first time in any communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.
- ☐ This Information Disclosure Statement is being filed within three months of the filing date of the subject patent application.
- ☒ This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits.

PETITION

- ☐ Applicant(s) hereby request consideration of the attached information. A check is attached in the amount of the Petition fee required under 37 CFR §1.17(i)(1).

DEPOSIT ACCOUNT

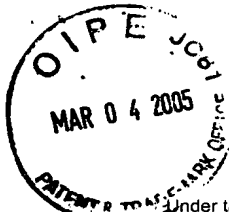
- ☒ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 23-2185. A duplicate copy of this sheet is enclosed.

Blank Rome LLP
600 New Hampshire Avenue, N.W.
Washington, DC 20037
Tel: (202) 772-5800
Fax (202) 572-8398
Customer No.: 27557

Date: March 4, 2005

Respectfully submitted,

David J. Edmondson
Attorney of Record
Registration No. 35,126



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known

Application Number	10/762,550 (Conf. No. 3210)
Filing Date	January 23, 2004
First Named Inventor	David Albonesi
Art Unit	2115
Examiner Name	Not yet assigned
Attorney Docket Number	000687-00324

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US-6,487,675 B2	11-26-2002	Sager et al	Fig. 4; col. 4, lines 3-20; col. 5, lines 7-50; col. 6, lines 9-25
		US-6,463,547 B1	10-08-2002	Bailey et al	
		US-6,047,382 A	04-04-2000	Maley et al	
		US-5,796,995 A	08-18-1998	Nasserbakht et al	Fig. 4; col. 7, lines 28-62
		US-5,710,910 A	01-20-1998	Kehl et al	Col. 3, line 13-col. 5, line 50
		US-5,309,561 A	05-03-1994	Overhouse et al	Col. 2, line 53-col. 4, line 59
		US-			
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		US-			
		US-			

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ Kind Code ⁵ (if known)				

Examiner Signature

Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Docket No. 000687-00324

JPW



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: David Albonesi, et al.

GAU: 2115

SERIAL NO: 10/762,550

EXAMINER: UNASSIGNED

FILED: January 23, 2004

FOR: MULTIPLE CLOCK DOMAIN MICROPROCESSOR

COMMISSIONER FOR PATENTS

P.O. BOX 1450

ALEXANDRIA, VA. 22313-1450

SIR:

Transmitted herewith is an amendment in the above-identified application.

- ☒ No additional fee is required
- ☐ This application qualifies for small entity status. 37 C.F.R. §1.27.
- ☐ Additional documents filed herewith:

Claims	Claims Remaining	Highest Number Prev. Paid		Number of Extra Claims	Rate	Fee
Total	12	20	-20	0	\$50	\$0.00
Independent	2	3	-3	0	\$200	\$0.00
		☐ Multiple Dependent Claims			\$360	\$0.00
		TOTAL OF ABOVE CALCULATIONS				\$0.00
		☐ Reduction by 50% for filing by Small Entity				\$0.00
		☐ Recordation of Assignment			\$40.00	\$0.00
		TOTAL				\$0.00

☐ A check in the amount of is attached.

☒ Please charge any additional Fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit Account No. 23-2185. A duplicate copy of this sheet is enclosed.

☒ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 23-2185. A duplicate copy of this sheet is enclosed.

Blank Rome LLP
600 NEW HAMPSHIRE AVENUE, N.W.
WASHINGTON, DC 20037
TEL (202) 944-3000
FAX (202) 572-8398

Customer No. 27557

Date: March 4, 2005

BLANK ROME LLP

Michael C. Greenbaum
Registration No. 28,419

by David Edmundson
35126

MAR 04 2005

PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
to a collection of information unless it displays a valid OMB control number

Under the Paperwork Reduction Acts of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	(\$)
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Complete if Known

Application Number	10/762,550
Filing Date	January 23, 2004
First Named Inventor	David Albonesi, et al.
Examiner Name	Unassigned
Art Unit	2115
Attorney Docket No.	000687-00324

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____
☐ Deposit Account Deposit Account Number: 23-2185 Deposit Account Name: Blank Rome LLP
 For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)
☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**
☐ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☐ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description

Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

<u>Total Claims</u>	<u>Extra Claims</u>	<u>Fee (\$)</u>	<u>Fee Paid (\$)</u>	<u>Multiple Dependent Claims</u>
-20 or HP =	x	=		<u>Fee (\$)</u> <u>Fee Paid (\$)</u>

HP=highest number of total claims paid for, if greater than 20

<u>Indep. Claims</u>	<u>Extra Claims</u>	<u>Fee (\$)</u>	<u>Fee Paid (\$)</u>
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$$\text{---} -3 \text{ or HP} = \text{---} \times \text{---} = \text{---}$$

HP=highest number of independent claims paid for, if greater than 3

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

<u>Total Sheets</u>	<u>Extra Sheets</u>	<u>Number of each additional 50 or fraction thereof</u>	<u>Fee (\$)</u>	<u>Fee Paid (\$)</u>
-100 =	/ 50 =	(round up to a whole number) x	-	

4. OTHER FEE(S)		Fees Paid (\$)

Non-English Specification,	\$130 fee (no small entity discount)
-----------------------------------	---

Other:

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 28,419	Telephone 202-772-5836
Name (Print/Type)	Michael C. Greenbaum		Date March 4, 2005

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, 1-800-PTO-9199 and select option 2.

If you need assistance in completing the form, 1-800-PTO-9

4 David Edwards
35126

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number

10 762 550

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	3	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	3 minus 20 =	*
INDEPENDENT CLAIMS	2 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 3	Minus ** 20	=
Independent	* 2	Minus *** 3	= 1
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

- * If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 - ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
 - *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
- The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY TYPE ☐ OR

OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	385.00
X\$ 9=	
X43=	
+145=	
TOTAL	385

RATE	FEE
BASIC FEE	770.00
X\$18=	
X86=	
+290=	
TOTAL	

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
X\$ 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$ 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$ 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re patent application of

David Albonesi et al.

Patent Application No. 10/762,550

Filed: January 23, 2004

Confirmation No. 3210

Title: Multiple Clock Domain Microprocessor

Art Unit: 2115

Examiner: Not yet known

Attorney Docket No.:
000687-00324

TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: November 29, 2004
(November 27, 2004 was a Saturday)

Sir:

Responsive to the *Notice to File Missing Parts of NonProvisional Application* mailed April 27, 2004, enclosed are the following documents to complete the formal filing requirements in the above-identified application:

- ☒ Transmittal (herewith).
- ☒ Fee Transmittal (in dupl.) with check \$1,265.00 to cover the filing fee, late submission of Declaration fee, Extension of Time and Assignment fee.
- ☒ Petition for Four Month Extension of Time (in dupl.)
- ☒ A copy of the Notice to File Missing Parts of Application .
- ☒ Executed Declaration
- ☒ Submission of Declaration
- ☒ Executed Assignment
- ☒ Assignment Recordation Cover Sheet
- ☒ The Commissioner is hereby authorized to charge any additional fees or credit any

payment to Deposit Account No. 23-2185 (000687-00324). **A duplicate copy of this letter is attached.**

Respectfully submitted,

By:

Michael C. Greenbaum
Registration No. 28,419

BLANK ROME LLP
The Watergate
600 NEW HAMPSHIRE AVENUE, NW
Washington, D.C. 20037
(202) 944-3000 (Phone)
(202) 572-8398 (Facsimile)

FEE TRANSMITTAL
for FY 2005

Effective 10/01/2003. Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT

(\$) 1,265.00.00

Complete If Known

Application Number	0/862,550
Filing Date	January 23, 2004
First Named Inventor	David Albonesi et al.
Examiner Name	TBD
Art Unit	2115
Attorney Docket No.	000687-00324

METHOD OF PAYMENT (check all that apply)☒ Check ☐ Credit card ☐ Money ☐ other ☐ None☐ Deposit Account:

Deposit

Account

Number

Deposit

Account

Name

23-2185

Blank Rome LLP

The Director is authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☒ Credit any overpayments☒ Charge any additional fee(s) or any underpayment of fee(s)☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.**FEE CALCULATION****1. BASIC FILING FEE**

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1001	790	2001	395	Utility filing fee	395
1002	350	2002	170	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	
SUBTOTAL (1)					(\$) 395.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1202	18	2202	9	Claims in excess of 20	
1201	88	2201	44	Independent claims in excess of 3	
1203	300	2203	150	Multiple dependent claim, if not paid	
1204	88	2204	44	** Reissue independent claims over original patent	
1205	18	2205	9	** Reissue claims in excess of 20 over original patent	
SUBTOTAL (2)					(\$) .00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1051	130	2051	65	Surcharge - late filing fee or oath	65
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for <i>ex parte</i> reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	430	2252	215	Extension for reply within second month	
1253	980	2253	490	Extension for reply within third month	
1254	1,530	2254	765	Extension for reply within fourth month	765
1255	2,080	2255	1,040	Extension for reply within fifth month	
1401	340	2401	170	Notice of Appeal	
1402	340	2402	170	Filing a brief in support of an appeal	
1403	340	2403	170	Request for oral hearing	
1501	1,510	1501	1,510	Petition to institute a public use proceeding	
1502	110	2452	55	Petition to revive - unavoidable	
1503	1,370	2453	685	Petition to revive - unintentional	
1501	1,370	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	40
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR 1.129(b))	
1801	790	2810	395	Request for Continued Examination (RCE)	
1802	90	1802	900	Request for expedited examination of a design application	
Other fee (Specify) _____					
SUBTOTAL (3)					(\$) 870.00

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3)**(\$) 870.00****SUBMITTED BY**

(Complete (if applicable))

Name (Print/Type)	Michael C. Greenbaum	Registration No. (Attorney/Agent)	28,419	Telephone	202-772-5800
Signature				Date	November 29, 2004
Correspondence Address:	Blank Rome LLP 600 New Hampshire Avenue, N.W. Washington, D.C. 20037 Fax: 202-572-8398 Customer No.: 27557				



PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2005

Effective 10/01/2003. Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT

(\$ 1,265.00.00)

Complete If Known

Application Number	0/862,550
Filing Date	January 23, 2004
First Named Inventor	David Albonesi et al.
Examiner Name	TBD
Art Unit	2115
Attorney Docket No.	000687-00324

METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit card ☐ Money ☐ other ☐ None
☐ Deposit Account:

Deposit Account Number: 23-2185
Deposit Account Name: Blank Rome LLP

The Director is authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☒ Credit any overpayments
☐ Charge any additional fee(s) or any underpayment of fee(s)
☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1001	790	2001	395	Utility filing fee	395
1002	350	2002	170	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	
SUBTOTAL (1)					(\$ 395.00)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Total Claims	Extra Claims	Fee from below	Fee Paid
8	20	X	0
2	3	X	0
Multiple Dependent			0

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1202	18	2202	9	Claims in excess of 20	
1201	88	2201	44	Independent claims in excess of 3	
1203	300	2203	150	Multiple dependent claim, if not paid	
1204	88	2204	44	** Reissue independent claims over original patent	
1205	18	2205	9	** Reissue claims in excess of 20 over original patent	
SUBTOTAL (2)					(\$) .00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1051	130	2051	65	Surcharge - late filing fee or oath	65
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for <i>ex parte</i> reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	430	2252	215	Extension for reply within second month	
1253	980	2253	490	Extension for reply within third month	
1254	1,530	2254	765	Extension for reply within fourth month	765
1255	2,080	2255	1,040	Extension for reply within fifth month	
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1402	340	2402	170	Filing a brief in support of an appeal	
1403	340	2403	170	Request for oral hearing	
1501	1,510	1501	1,510	Petition to institute a public use proceeding	
1502	110	2452	55	Petition to revive - unavoidable	
1503	1,370	2453	685	Petition to revive - unintentional	
1501	1,370	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	40
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR 1.129(b))	
1801	790	2810	395	Request for Continued Examination (RCE)	
1802	90	1802	900	Request for expedited examination of a design application	
Other fee (Specify) _____					
SUBTOTAL (3)					(\$ 870.00)

*Reduced by Basic Filing Fee Paid

SUBMITTED BY

(Complete (if applicable))

Name (Print/Type)	Michael C. Greenbaum	Registration No. (Attorney/Agent)	28,418	Telephone	202-772-5800
Signature				Date	November 29, 2004
Correspondence Address:	Blank Rome LLP 600 New Hampshire Avenue, N.W. Washington, D.C. 20037 Fax: 202-572-8398 Customer No.: 27557				



Docket No. 000687-00324

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: David Albonesi et al.

CONFIRMATION NO: 3210

SERIAL NO: 10/762,550

GAU: 2115

FILED: January 23, 2004

EXAMINER: TBD

FOR: Multiple Clock Domain Microprocessor

FILING OF DECLARATION UNDER 37 CFR 1.53(f)

MAIL STOP: MISSING PARTS
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ARLINGTON, VA 22313-1450

ATTN: APPLICATION BRANCH

SIR:

Responsive to the notification dated April 27, 2004, and in accordance with the provisions of 37 CFR 1.53(f), Applicants submit herewith a Declaration in accordance with 37 C.F.R. 1.63.

- ☐ The required fee was paid at the time of filing the application.
- ☒ A check is attached to cover the required fee (\$65.00) for the late filing of the executed declaration.
- ☒ A copy of the notification is also submitted herewith.

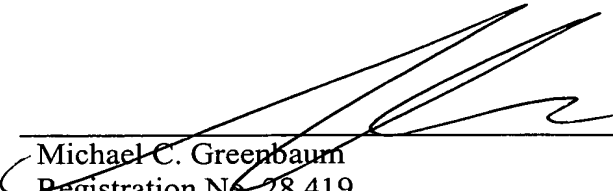
The Declaration enclosed herewith adequately identifies the above-identified application in accordance with 37 CFR 1.63, as set forth in MPEP Section 601.01.

In light of the foregoing, this application is deemed to be in proper condition for examination and such favorable action is earnestly solicited.

Please charge any underpayment of fees or credit any overpayment of fees to Deposit Account No. 23-2185. A duplicate copy of this paper is attached.

BLANK ROME LLP

THE WATERGATE BUILDING
SUITE 1100
600 NEW HAMPSHIRE AVENUE
WASHINGTON, DC 20037
TEL (202) 772-5838
FAX (202) 572-1438


Michael C. Greenbaum
Registration No. 28,419

Date: November 29, 2004



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/762,550	01/23/2004	David Albonesi	000687.00324

27557
 BLANK ROME LLP
 600 NEW HAMPSHIRE AVENUE, N.W.
 WASHINGTON, DC 20037



CONFIRMATION NO. 3210

FORMALITIES LETTER



OC000000012460712

Date Mailed: 04/27/2004

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

*Filing Date Granted***Items Required To Avoid Abandonment:**

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
Applicant must submit \$ 385 to complete the basic filing fee for a small entity.
- The oath or declaration is missing.
A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of \$65 for a small entity in compliance with 37 CFR 1.27, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$450** for a Small Entity

- **\$385** Statutory basic filing fee.
- **\$65** Late oath or declaration Surcharge.

Replies should be mailed to: Mail Stop Missing Parts
 Commissioner for Patents
 P.O. Box 1450
 Alexandria VA 22313-1450

11/30/2004 EABUDAK1 00000071 10762550

01 FC:2001
 02 FC:2051

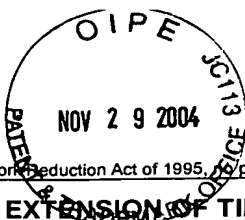
395.00 OP
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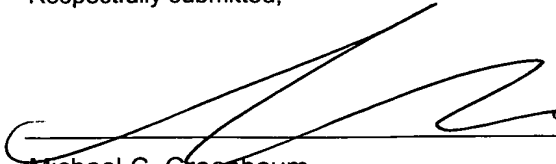
A copy of this notice MUST be returned with the reply.



Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 2 - COPY TO BE RETURNED WITH RESPONSE



PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)		Docket Number: 000687-00324
Serial Number: 10/762,550	Confirmation Number: 3210	Filed: January 23, 2004
Inventor(s): David Albonesi et al.		
For: Multiple Clock Domain Microprocessor		
Art Unit: 2115	Examiner: TBD	
This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.		
The requested extension and fees are as follows (check time period desired and enter the appropriate fee below):		
	<u>Fee</u>	<u>Small Entry Fee</u>
☐ One month (37 CFR 1.17(a)(1))	\$110	\$55 \$ _____
☐ Two months (37 CFR 1.17(a)(2))	\$430	\$215 \$ _____
☐ Three months (37 CFR 1.17(a)(3))	\$980	\$490 \$ _____
☒ Four months (37 CFR 1.17(a)(4))	\$1530	\$765 \$ <u>765.00</u>
☐ Five months (37 CFR 1.17(a)(5))	\$2080	\$1040 \$ _____
☒ Applicant claims small entity status. See 37 CFR 1.27.		
☒ A check in the amount of the fee is enclosed.		
☐ Payment by credit card. Form PTO-2038 is attached.		
☐ The Director has already been authorized to charge fees in this application to a Deposit Account.		
☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number <u>23-2185</u>		
WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.		
I am the ☐ applicant/inventor.		
☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96)		
☒ attorney or agent of record. Registration Number <u>28,419</u>		
☐ attorney or agent under 37 CFR 1.34: Registration number if acting under 37 CFR 1.34 _____		
Blank Rome LLP 600 New Hampshire Avenue, N.W. Washington, DC 20037 Tel: (202) 772-5800 Fax: (202) 572-8398 Customer No.: 27557		
Respectfully submitted,  Michael C. Greenbaum		
Date: November 29, 2004		
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.		
☒ Total <u>2</u> forms are submitted.		

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



Attorney Docket: 000687-00324

DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: MULTIPLE CLOCK DOMAIN MICROPROCESSOR

the specification of which

☐ is attached hereto

☒ was filed on January 23, 2004 as United States Application Number or PCT International

Application Number 10/762,550 and (if applicable) was amended on

I hereby authorize our attorneys to insert the serial number assigned to this application.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 USC §119

APPLICATION NO.	COUNTRY	DAY/MONTH/YEAR FILED	PRIORITY CLAIMED

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

PROVISIONAL APPLICATION(S) UNDER 35 U.S.C. §119(e)

APPLICATION NUMBER	FILING DATE
60/441,759	January 23, 2003

I hereby claim the benefit under 35 U.S.C. §120 of any United States application, or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. §112.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

PRIOR U.S./PCT INTERNATIONAL APPLICATION(S) DESIGNATED FOR BENEFIT UNDER 35 U.S.C. §120

APPLICATION NO.	FILING DATE	STATUS — PATENTED, PENDING, ABANDONED

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith: Victor M. Wigman, Reg. No. 25,201; George C. Myers, Jr., Reg. No. 27,040; Donald R. Greene, Reg. No. 22,470; Michael C. Greenbaum, Reg. No. 28,419; Charles R. Wolfe, Jr., Reg. No. 28,680; Michael D. White, Reg. No. 32,795; Brian C. Jones, Reg. No. 37,857; David J. Edmondson, Reg. No. 35,126; Denise C. Lane, Reg. No. 42,780; Peter Weissman, Reg. No. 40,220; Brian WM. Higgins, Reg. No. 48,443; Minh-Quan K. Pham, Reg. No. 50,594; Thomas L. Willis Jr., Reg. No. 53,778 and Tara Hoffman, Reg. No. 46,510.

Correspondence Address:

BLANK ROME LLP
600 New Hampshire Avenue, N.W.
Washington, DC 20037
TEL (202) 944-3000 FAX (202) 572-8398



27557

PATENT & TRADEMARK OFFICE

000687.00324/35626421v1

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

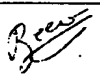
Full Name of sole or first inventor (given name, family name) David Albonesi	
Signature <i>David H Albonesi</i>	Date 7/27/04
Residence Rochester, NY	Citizenship US
Mailing Address 2389 Doran Road, Rochester, NY 14485 <i>Uma</i>	
Full Name of additional joint inventor (given name, family name) Greg Semeraro	
Signature <i>Greg Semeraro</i>	Date 25 May 04
Residence Fairport, NY	Citizenship US
Mailing Address 112 Harvest Road, Fairport, NY 14450	
Full Name of additional joint inventor (given name, family name) Grigorios Magklis	
Signature	Date
Residence Rochester, NY	Citizenship US
Mailing Address 60 Crittenden Blvd., Apart. 429, Rochester, NY 14620	
Full Name of additional joint inventor (given name, family name) Michael L. Scott	
Signature <i>Michael L. Scott</i>	Date 2 June 04
Residence Rochester, NY	Citizenship US
Mailing Address 54 Laconia Pkwy, Rochester, NY 14618	
Full Name of additional joint inventor (given name, family name) Rajeev Balasubramonian	
Signature	Date
Residence Rochester, NY	Citizenship US
Mailing Address 50 S. Central Campus Drive, Rm. 3190J, Salt Lake City, UT 84112	
☒ Additional joint inventors are named on separately numbered sheets attached hereto.	

Attorney Docket: 000687-00324

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of sole or first inventor (given name, family name) David Albonesi	
Signature	Date
Residence Rochester, NY	Citizenship US
Mailing Address University of Rochester, RC Box 270226, Computer Studies 411, Rochester, NY 14627	
Full Name of additional joint inventor (given name, family name) Greg Semeraro	
Signature	Date
Residence Fairport, NY	Citizenship US
Mailing Address 112 Harvest Road, Fairport, NY 14450	
Full Name of additional joint inventor (given name, family name) Grigorios Magklis	
Signature 	Date 10/6/2004
Residence Barcelona Spain	Citizenship Greece
Mailing Address Intel Labs Barcelona, Jordi Girona, 29-3A, 08024, Barcelona, SPAIN	
Full Name of additional joint inventor (given name, family name) Michael L. Scott	
Signature	Date
Residence Rochester, NY	Citizenship US
Mailing Address University of Rochester, RC Box 270226, Computer Studies 715, Rochester, NY 14627	
Full Name of additional joint inventor (given name, family name) Rajeev Balasubramonian	
Signature	Date
Residence Rochester, NY	Citizenship US
Mailing Address 216-A Conant Road, Rochester, NY 14623	
☒ Additional joint inventors are named on separately numbered sheets attached hereto.	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of sole or first inventor (given name, family name) David Albonesi	
Signature	Date
Residence Rochester, NY	Citizenship US
Mailing Address ~~2389 Doran Road, Rochester, NY 14485~~	
Full Name of additional joint inventor (given name, family name) Greg Semeraro	
Signature	Date
Residence Fairport, NY	Citizenship US
Mailing Address 112 Harvest Road, Fairport, NY 14450	
Full Name of additional joint inventor (given name, family name) Grigorios Magklis	
Signature	Date
Residence Rochester, NY	Citizenship US
Mailing Address 60 Crittenden Blvd., Apart. 429, Rochester, NY 14620	
Full Name of additional joint inventor (given name, family name) Michael L. Scott	
Signature	Date
Residence Rochester, NY	Citizenship US
Mailing Address ~~54 Laconia Pkwy, Rochester, NY 14618~~	
Full Name of additional joint inventor (given name, family name) Rajeev Balasubramonian	
Signature 	Date <u>7/8/2004</u>
Residence Rochester, NY	Citizenship ~~US~~ INDIA
Mailing Address ~~50 S Central Campus Drive, Rm 3190, Salt Lake City, UT 84112~~	
☒ Additional joint inventors are named on separately numbered sheets attached hereto.	

Full Name of sole or first inventor (given name, family name) Sandhya Dwarkadas	
Signature <i>Sandhya Dwarkadas</i>	Date 1 st June, 2004
Residence Rochester, NY	Citizenship India
Mailing Address University of Rochester, RC Box 270226, Computer Studies 411, Rochester, NY 14627	
Full Name of additional joint inventor (given name, family name)	
Signature	Date
Residence	Citizenship
Mailing Address	
Full Name of additional joint inventor (given name, family name)	
Signature	Date
Residence	Citizenship
Mailing Address	
Full Name of additional joint inventor (given name, family name)	
Signature	Date
Residence	Citizenship
Mailing Address	
Full Name of additional joint inventor (given name, family name)	
Signature	Date
Residence	Citizenship
Mailing Address	
☐ Additional joint inventors are named on separately numbered sheets attached hereto.	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
1	BRS	L1	486275	processor or microprocessor	USPAT; US-PGP UB	2004/11/08 20:30		
2	BRS	L2	1516	clock adj2 domain	USPAT; US-PGP UB	2004/11/08 20:31		
3	BRS	L3	269	1 same 2	USPAT; US-PGP UB	2004/11/08 20:31		
4	BRS	L4	8355	multi\$3 adj3 clock\$1	USPAT; US-PGP UB	2004/11/08 20:32		
5	BRS	L5	6003	local\$2 adj3 clock\$1	USPAT; US-PGP UB	2004/11/08 20:32		
6	BRS	L6	144130	1 same (block or section)	USPAT; US-PGP UB	2004/11/08 20:33		
7	BRS	L7	185	3 and 6	USPAT; US-PGP UB	2004/11/08 20:33		
8	BRS	L8	54	4 and 7	USPAT; US-PGP UB	2004/11/08 21:06		
9	BRS	L9	22	5 and 7	USPAT; US-PGP UB	2004/11/08 21:06		
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13	BRS	L13	2177	11 or 12	USPAT; US-PGP UB	2004/11/08 21:18		
14	BRS	L14	25	3 and 13	USPAT; US-PGP UB	2004/11/08 21:43		
15	BRS	L15	35381	(block or section or module) near5 speed	USPAT; US-PGP UB	2004/11/08 21:44		
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17	BRS	L17	30	13 and 16	USPAT; US-PGP UB	2004/11/08 21:44		
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19	BRS	L19	7164	clock near5 distribut\$3	USPAT; US-PGP UB	2004/11/08 21:55		
20	BRS	L20	76	3 and 19	USPAT; US-PGP UB	2004/11/08 21:55		

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
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22	BRS	L22	16	3.ab.	USPAT; US-PGP UB	2004/11/08 22:08		
23	BRS	L23	1673	clock near3 ring	USPAT; US-PGP UB	2004/11/08 22:09		
24	BRS	L24	118	1 same 23	USPAT; US-PGP UB	2004/11/08 22:10		
25	BRS	L25	14	13 and 24	USPAT; US-PGP UB	2004/11/08 22:10		



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
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 Alexandria, Virginia 22313-1450
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10/762,550	01/23/2004	David Albonesi	000687.00324

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 BLANK ROME LLP
 600 NEW HAMPSHIRE AVENUE, N.W.
 WASHINGTON, DC 20037

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Applicant must submit \$ 385 to complete the basic filing fee for a small entity.
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SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$450** for a Small Entity

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- **\$65** Late oath or declaration Surcharge.

Replies should be mailed to: Mail Stop Missing Parts
 Commissioner for Patents
 P.O. Box 1450
 Alexandria VA 22313-1450

*A copy of this notice **MUST** be returned with the reply.*

A handwritten signature in black ink, appearing to be 'CM' followed by a stylized name, is written over a horizontal line.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	000687.00324
	First Inventor or Application Identifier	David Albonesi et al.
	Title	MULTIPLE CLOCK DOMAIN MICROPROCESSOR

00727 U.S. PTO
107762550



APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents	ADDRESS TO: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450
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1. ☐ Fee Transmittal Form (e.g. PTO/SB/17) (Submit an original and a duplicate for fee processing) 2. ☒ Applicant claims small entity status. See 37 CFR 1.27 3. ☒ Specification Total Pages 33 4. ☒ Drawing(s) (35 U.S.C. 113) Total Sheets 8 5. ☐ Oath or Declaration Total Pages a. ☐ Newly executed (original or copy) b. ☐ Copy from a prior application (37 C.F.R. §1.63(d)) (for continuation / divisional w/ box 18 completed) i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §1.63(d)(2) and 1.33(b). 6. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program <i>(Appendix)</i> 7. ☐ Application Data Sheet. See 37 CFR 1.76 8. ☐ Nucleotide and/or Amino Acid Sequence Submission <i>(if applicable, all necessary)</i> a. ☐ Computer Readable Form (CRF) b. ☐ Specification or Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies	ACCOMPANYING APPLICATION PARTS 9. ☐ Assignment Papers (cover sheet & document(s)) 10. ☐ 37 C.F.R. §3.73(b) Statement ☐ Power of Attorney <i>(when there is an assignee)</i> 11. ☐ English Translation Document <i>(if applicable)</i> 12. ☐ Information Disclosure ☐ Copies of IDS Statement (IDS)/PTO-1449 Citations 13. ☐ Preliminary Amendment 14. ☒ White Advance Serial No. Postcard 15. ☐ Certified Copy of Priority Document(s) <i>(if foreign priority is claimed)</i> 16. ☐ Request and Certification under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent. 17. ☐ Other:
---	---

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below:

☐ Continuation
 ☐ Divisional
 ☐ Continuation-in-part (CIP)
 of prior application no.:

Prior application information: Examiner: Group Art Unit:

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b is considered a part of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. Amend the specification by inserting before the first line the sentence:

☐ This application is a ☐ Continuation
 ☐ Division
 ☐ Continuation-in-part (CIP)
 of application Serial No. Filed on

☒ This application claims priority of provisional application Serial No. 60/441,759 Filed January 23, 2003

20. CORRESPONDENCE ADDRESS	
BLANK ROME LLP 600 NEW HAMPSHIRE AVENUE, N.W. WASHINGTON, DC 20037 TEL (202) 944-3000 FAX (202) 572-8398	 27557 PATENT TRADEMARK OFFICE

Name: Michael C. Greenbaum	Registration No.: 28,419
Signature:	Date: January 23, 2004

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	000687.00324
	First Inventor or Application Identifier	David Albonesi et al.
	Title	MULTIPLE CLOCK DOMAIN MICROPROCESSOR

00727 U.S. PTO
107762550



APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents	ADDRESS TO: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450
---	---

1. ☐ Fee Transmittal Form (e.g. PTO/SB/17) (Submit an original and a duplicate for fee processing) 2. ☒ Applicant claims small entity status. See 37 CFR 1.27 3. ☒ Specification Total Pages 33 4. ☒ Drawing(s) (35 U.S.C. 113) Total Sheets 8 5. ☐ Oath or Declaration Total Pages a. ☐ Newly executed (original or copy) b. ☐ Copy from a prior application (37 C.F.R. §1.63(d)) (for continuation / divisional w/ box 18 completed) i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §1.63(d)(2) and 1.33(b). 6. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (<i>Appendix</i>) 7. ☐ Application Data Sheet. See 37 CFR 1.76 8. ☐ Nucleotide and/or Amino Acid Sequence Submission (<i>if applicable, all necessary</i>) a. ☐ Computer Readable Form (CRF) b. ☐ Specification or Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies	ACCOMPANYING APPLICATION PARTS 9. ☐ Assignment Papers (cover sheet & document(s)) 10. ☐ 37 C.F.R. §3.73(b) Statement ☐ Power of Attorney (<i>when there is an assignee</i>) 11. ☐ English Translation Document (<i>if applicable</i>) 12. ☐ Information Disclosure ☐ Copies of IDS Statement (IDS)/PTO-1449 Citations 13. ☐ Preliminary Amendment 14. ☒ White Advance Serial No. Postcard 15. ☐ Certified Copy of Priority Document(s) (<i>if foreign priority is claimed</i>) 16. ☐ Request and Certification under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent. 17. ☐ Other:
---	---

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application no.:

Prior application information: Examiner: Group Art Unit:

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b is considered a part of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. Amend the specification by inserting before the first line the sentence:

☐ This application is a ☐ Continuation ☐ Division ☐ Continuation-in-part (CIP)
 of application Serial No. Filed on

☒ This application claims priority of provisional application Serial No. 60/441,759 Filed January 23, 2003

20. CORRESPONDENCE ADDRESS	
BLANK ROME LLP 600 NEW HAMPSHIRE AVENUE, N.W. WASHINGTON, DC 20037 TEL (202) 944-3000 FAX (202) 572-8398	 27557 PATENT TRADEMARK OFFICE

Name: Michael C. Greenbaum	Registration No.: 28,419
Signature:	Date: January 23, 2004

MULTIPLE CLOCK DOMAIN MICROPROCESSOR

Statement of Government Interest

This work was supported in part by NSF grants CCR-9701915, CCR-9702466, CCR-9705594, CCR-9811929, EIA-9972881, CCR-9988361, and EIA-0080124; by DARPA/ITO under AFRL contract F29601-00-K-0182. The government has certain rights in the invention.

Reference to Related Application

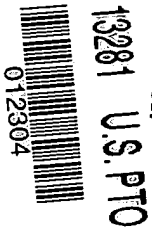
The present application claims the benefit of U.S. Provisional Patent Application No. 60/441,759, filed January 23, 2003, whose disclosure is hereby incorporated by reference in its entirety into the present disclosure.

Field of the Invention

The present invention is directed to microprocessors and more particularly to microprocessors having multiple clock domains.

Description of Related Art

The continuing push for higher microprocessor performance has led to unprecedented increases in clock frequencies in recent years. While the Pentium III microprocessor broke the 1GHz barrier in 2000, the Pentium IV is currently shipping at 2GHz. At the same time, due to issues of reliability and performance, wire dimensions have been scaled in successive process generations more conservatively than transistor dimensions. The result of these frequency and dimensional trends is that microprocessor clock speeds have become increasingly limited by wire delays, so much so that some of the more recent microprocessors, e.g., the Pentium IV [14], have pipeline stages solely dedicated to moving signals across the chip. Furthermore, a growing challenge in future systems will be to distribute the clock across a progressively larger die to increasing numbers of latches while meeting a decreasing clock skew budget. The inevitable



conclusion reached by industrial researchers is that in order to continue the current pace of clock frequency increases, microprocessor designers will eventually be forced to abandon singly-clocked globally synchronous systems in favor of some form of asynchrony [8, 24].

Although purely asynchronous systems have the potential for higher performance and lower power compared to their synchronous counterparts, major corporations have been reluctant to fully migrate to asynchronous design methodologies. Two major reasons for this reluctance are the immaturity of asynchronous design tools relative to those in the synchronous domain, and the cost and risk of moving away from the mature design infrastructures that have been successfully used to create many generations of microprocessor products. Yet many existing synchronous designs do incorporate a limited amount of asynchrony. For example, several multiprocessor systems run the memory bus off of a different clock than the processor core in order to allow a single system to accommodate processors of different frequencies. In such dual clock domain systems, the logic in each of the two clock domains is designed using conventional synchronous design methodologies. Well-known and highly-reliable techniques are used to synchronize communication between the two domains, albeit at the cost of extra delay.

An additional trend due to the wire scaling dilemma is to replace microarchitectural techniques requiring long global wires with alternatives requiring only local wiring. This approach improves both clock frequency and the scalability of the design in future process generations. For example, in several microprocessors including the Alpha 21164 and 21264 [11, 20] and the UltraSPARC III [17], the use of global wires to stall early pipeline stages has been replaced by the use of replay traps that cancel instructions and restart the pipeline. Although flushing the pipeline in this manner requires additional cycles for reloading, it results in a higher clock frequency and more scalable implementation due to the elimination of global wires. The

designers of the UltraSPARC III fully embraced this approach by creating six functional blocks that run relatively independently of one another, with most long wires eliminated between units [17].

Reference numerals in brackets refer to the following references:

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Summary of the Invention

It is an object of the invention to overcome the above-noted deficiencies of the prior art. It is another object of the invention to provide an approach that allows for aggressive future frequency increases, maintains a synchronous design methodology, and exploits the trend
5 towards making functional blocks more autonomous.

To achieve the above and other objects, the present invention is directed to a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain
10 communication. Thus, fully synchronous design practices are used in the design of each domain. Although the inter-domain synchronization increases the number of clock cycles required to run a given application, an MCD microprocessor affords a number of potential advantages over a singly clocked design:

- The global clock distribution network is greatly simplified, requiring only the distribution
15 of the externally generated clock to the local Phase Lock Loop (PLL) in each domain. The independence of each local domain clock implies no global clock skew requirement, permitting potentially higher frequencies within each domain and greater scalability in future process generations.
- The designers of each domain are no longer constrained by the speeds of critical paths in
20 other domains, affording them greater freedom in each domain to optimize the tradeoffs among clock speed, latency, and the exploitation of application parallelism via complex hardware structures.

- Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain allows for finer grained dynamic voltage and frequency scaling, and thus lower energy, than can be achieved with single clock, single-core-voltage systems.

- 5
- With the ability to dynamically resize structures and alter the clock speed in each domain, the IPC/clock rate tradeoff can be tailored to application characteristics within each individual domain [1], thereby improving both performance and energy efficiency.

In the present application, we describe an initial implementation of an MCD microprocessor that is a straightforward extension of a singly-clocked synchronous dynamic superscalar design. By accurately modeling inter-domain synchronization, we characterize the performance and energy costs of the required synchronization circuitry. We then explore the potential benefits of per-domain dynamic voltage and frequency scaling. Our results demonstrate a 20% average improvement in energy-delay product for a set of benchmarks that includes both compute and memory-bound applications. Unlike rate-based multimedia applications, these benchmarks have not traditionally been candidates for voltage and frequency scaling.

10

15

We disclose a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style along with dynamic voltage and frequency scaling in order to maximize performance and energy efficiency for a given application. Our design uses existing queue structures in a superscalar processor core to isolate the different clock domains in a way that minimizes the need for inter-domain synchronization.

20

Performance results for applications drawn from standard benchmark suites suggest that the division of the processor into multiple domains incurs an average baseline performance cost of less than 4%. At the same time, by scaling frequency and voltage in different domains

dynamically and independently, we can achieve an average improvement in energy-delay product of nearly 20%. By contrast, global voltage scaling to achieve comparable performance degradation in a singly clocked microprocessor achieves an average energy-delay improvement of only 3%.

5 Our current analysis uses an off-line algorithm to determine the points in the program at which different domains should change frequency and voltage. Variations within the scope of the invention include effective on-line algorithms, including approaches for effective scaling of the front end, as well as the ability to deliver tunable on-chip voltage and frequency with low latency.

10 The following paper describes the invention and is hereby incorporated by reference in its entirety into the present disclosure: Semeraro et al, "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," *High Performance Computer Architecture (HPCA)*, February 2, 2002.

Brief Description of the Drawings

A preferred embodiment of the present invention will be disclosed in detail with reference to the drawings, in which:

Fig. 1 shows a multiple clock domain processor block diagram;

5 Fig. 2 shows a queue structure;

Fig. 3 shows a full flag;

Fig. 4 shows synchronization timing;

Fig. 5 shows performance degradation results;

Fig. 6 shows energy saving results;

10 Fig. 7 shows energy-delay improvement results;

Figs. 8A and 8B show frequency changes for *art* generated by our off-line algorithm for the dynamic 1% configuration for Transmeta and XScale, respectively; and

Figs. 9A and 9B show summary statistics for intervals chosen by the off-line tool for the dynamic 5% configuration for Transmeta and XScale reconfiguration data, respectively.

15

Detailed Description of the Preferred Embodiment

Matzke has estimated that as technology scales down to a 0.1 μ m feature size, only 16% of the die will be reachable within a single clock cycle [24]. Assuming a chip multiprocessor with two processors per die, each processor would need to have a minimum of three equal-size clock domains. The preferred embodiment uses four domains, one of which includes the L2 cache, so that domains may vary somewhat in size and still be covered by a single clock. In effect, we treat the main memory interface as a fifth clock domain, external to the MCD processor, and always running at full speed.

In choosing the boundaries between domains, we attempted to identify points where (a) there already existed a queue structure that served to decouple different pipeline functions, or (b) there was relatively little inter-function communication. Our four chosen domains, shown in the architecture 100 of Figure 1, comprise the front end 110 (including instruction cache 112, fetch unit 114, and branch prediction, rename, and dispatch 116); integer issue/execute 120 (including integer issue queue 122 and integer arithmetic logic units and register file 124); floating point issue/execute 130 (including floating point issue queue 132 and floating point arithmetic logic units and register file 134); and load/store issue/execute 140 (including load/store unit 142, L1 D-cache 144, and L2 cache 146 in communication with the main memory interface 150 as well as with the cache 112 of the front end 110). Although we were initially concerned about the performance impact of implementing separate load/store and integer domains, we discovered that the additional synchronization penalty did not significantly degrade performance. Furthermore, because we discovered no energy savings from decoupling instruction fetch from rename/dispatch, we combined these regions into a single fetch/rename/dispatch domain to eliminate their inter-domain synchronization overhead. Finally, execution units of the same type

(e.g., integer units) were combined into a single domain to avoid the high cost of synchronizing the bypass and register file datapaths among these units. As a result of these divisions, there were no explicit changes to the pipeline organization of the machine. We also believe that these divisions would result in a physically realizable floorplan for an MCD processor.

5 The primary disadvantage of an MCD processor is the performance overhead due to inter-domain synchronization. In this section, we discuss the circuitry required to perform this synchronization. We discuss how to model its performance cost below.

Some synchronization schemes restrict the phase relationship and relative frequencies of the clocks, thereby eliminating the need for hardware arbitration [27]. Unfortunately, these
10 schemes impose significant restrictions on the possible choices of frequencies. In addition, the need to control the phase relationships of the clocks means that global clock synchronization is required. Our design specifically recognizes the overhead associated with independent clocks with no known phase relationship. We believe this overhead to be unavoidable in an MCD processor: one of the motivating factors for the design is the recognition that traditional global
15 clock distribution will become increasingly difficult in the future.

The issue queues in the integer, floating point, and load/store domains (the Load/Store Queue within the Load/Store Unit), together with the Reorder Buffer (ROB) in the front end domain, serve to decouple the front and back ends of a conventional processor. Choosing these queues as inter-domain synchronization points has the advantage of hiding the synchronization
20 cost whenever the queue is neither full nor empty (as described below).

The general queue structure that we use for inter-domain communication is shown in Figure 2. The assertion of the *Full* flag indicates to the producer that it can no longer write to the queue until the flag is deasserted ($\overline{Full}$), while the *Empty* flag when asserted indicates that there

is no valid data for the consumer to read from the queue. The consumer waits until *Empty* is deasserted before reading again.

The use of a full handshake protocol for this interface requires that the producer/consumer check the *Full/Empty* flag after every operation in order to avoid queue overruns on writes or reads from an empty queue. This requirement significantly slows down the interface, thereby degrading performance. Rather, we assume that the *Full* and *Empty* flags are generated far enough in advance such that writes and reads can occur every clock cycle without over- or underflowing the queue. In other words, the *Full* flag is generated early enough such that a burst of writes every cycle will terminate (due to recognition by the producer of the assertion of the *Full* flag) just as the last remaining queue entry has been written. An analogous situation exists for the consumer side of the queue, although our particular queues are different in this regard as we discuss later. Note that this scheme may result in underutilization of the queue under particular conditions. For example, if the write that initiates assertion of the *Full* flag is at the end of a burst, then there will be empty but unusable entries in the queue (because the *Full* flag will have been asserted) the next time the producer has data to write into the queue.

In order to avoid underutilization of the queues, we assume extra queue entries to buffer writes under worst-case conditions so that the original number of queue entries can be fully utilized. In the MCD design, the worst-case situation occurs when the producer is operating at the maximum frequency (*max_freq*) and the consumer at the minimum frequency (*min_freq*). An additional complication occurs due to the need to compare queue head and tail pointers from different clock domains in order to generate the *Full* and *Empty* flags. Under these conditions, and assuming an additional cycle for the producer to recognize the *Full* signal,

$(\max_freq/\min_freq)+1$ additional entries are required. Our results do not account for the performance advantage nor the energy cost of these additional entries.

Even with completely independent clocks for each interface, the queue structure is able to operate at full speed for both reading and writing under certain conditions. This concurrency
5 requires a dual-ported SRAM structure where simultaneous read and write cycles are allowed to different SRAM cells. As long as the interfaces are designed to adhere to the protocol associated with the *Full* and *Empty* flags, the queue structure does not need to support simultaneous read and write access to the same SRAM cell. As long as the queue is not full (as described above) the producer can continue to write data on every rising edge of $Clock_w$ (Figure 3). Similarly, so long
10 as the queue is not empty, the consumer can continue reading on every rising edge of $Clock_r$. Therefore, both interfaces operate at full speed so long as the queue is partially full, although newly written entries may not be recognized by the consumer until after a synchronization period. Once the queue becomes full, the queue state of $\overline{Full}$ can only result from data being read out of the queue on the read interface. When this event occurs, the queue pointer in the read
15 domain must get synchronized with the write domain clock ($Clock_w$) in order to deassert *Full*. A similar desynchronization delay occurs with the generation of the $\overline{Empty}$ condition due to a write to an empty queue.

Many of the queues that we use as synchronization points have a different interface than that described above. For the issue queue for example, each entry has *Valid* and *Ready* flags that
20 the scheduler uses to determine whether an entry should be read (issued). The scheduler by design will never issue more than the number of valid and ready entries in the queue. Note, however, that due to synchronization, there is a delay before the scheduler sees newly written

queue data. The delay associated with crossing a clock domain interface is a function of the following:

- The synchronization time of the clock arbitration circuit, T_S , which represents the minimum time required between the source and destination clocks in order for the signal to be successfully latched at the destination. We assume the arbitration and synchronization circuits developed by Sjogren and Myers [28] that detect whether the source and destination clock edges are sufficiently far apart (at minimum, T_S) such that a source-generated signal can be successfully clocked at the destination. The destination clock is enabled only under these conditions. We assume a T_S of 30% of the period of the highest frequency.
- The ratio of the frequencies of the interface clocks.
- The relative phases of the interface clocks.

This delay can best be understood by examining a timing diagram (Figure 4), which shows source clock F_1 and destination clock F_2 . Consider the case when the queue is initially empty. Data is written into the queue on the rising edge of F_1 (edge 1). Data can be read out of the queue as early as the next rising edge of F_2 . If $T \leq T_S$, the earliest that the data can be read is one F_2 period later (edge 3). This extra delay represents one source of performance degradation due to synchronization. The value of T is determined by the relative frequency and phases of F_1 and F_2 , as well as the relative jitter of the clock sources, and may well change over time. The cost of synchronization is controlled by the relationship between T and T_S , and to a lesser degree by the magnitude of T_S . The analogous situation exists when the queue is *Full*, replacing *Empty* with *Full*, edge 1 with edge 2, and edge 3 with edge 4 in the above discussion.

Our simulator, described below, accurately accounts for the inter-domain overhead.

Our simulation testbed is based on the SimpleScalar toolset [6] with the Wattch [5] power estimation extensions. The original SimpleScalar model supports out of order execution using a centralized Register Update Unit (RUU) [29]. We have modified this structure to more closely model the microarchitecture of the Alpha 21264 microprocessor [20]. Specifically, we split the RUU into separate reorder buffer (ROB), issue queue, and physical register file structures. A summary of our simulation parameters appears in Table 1.

Table I: Architectural parameters for simulated processor

Branch predictor: comb. of bimodal and 2-level PAg	
Level1	1024 entries, history 10;
Level2	1024 entries;
Bimodal predictor size	1024;
Combining predictor size	4096;
BTB	4096 sets, 2-way
Branch Mispredict Penalty	7
Decode Width	4
Issue Width	6
Retire Width	11
L1 Data Cache	64KB, 2-way set associative
L1 Instruction Cache	64KB, 2-way set associative
L2 Unified Cache	1MB, direct mapped
L1 cache latency	2 cycles
L2 cache latency	12 cycles
Integer ALUs	4 + 1 mult/div unit
Floating-Point ALUs	2 + 1 mult/div/sqrt unit
Integer Issue Queue Size	20 entries
Floating-Point Issue Queue Size	15 entries
Load/Store Queue Size	64
Physical Register File Size	72 integer, 72 floating-point
Reorder Buffer Size	80

We selected a mix of compute-bound, memory-bound, and multimedia applications from the MediaBench, Olden, and SPEC2000 benchmark suites. Table 2 specifies the benchmarks used along with the window of instructions simulated. We show combined statistics for the

encode and decode phases of adpcm, epic, and g721, and for the mipmap, osdemo, and texgen phases of mesa.

Table 2: Benchmarks

Bench- mark	Suite	Datasets	Simulation window (instructions)
adpcm	Media- Bench	ref	entire program
epic		ref	entire program
g721		ref	0–200M
mesa		ref	entire program
em3d	Olden	4K nodes, arity 10	70M–119M
health		4 levels, 1K iters	80M–127M
mst		1K nodes	entire program 199M
power		ref	0–200M
treeadd		20 levels, 1 iter	entire program 189M
tsp		ref	0–200M
bzip2	SPEC 2000 Int	input.source	1000M–1100M
gcc		166.i	1000M–1100M
mcf		ref	1000M–1100M
parser		ref	1000M–1100M
art	SPEC	ref	300M–400M
swim	2000 FP	ref	1000M–1100M

For the baseline processor, we assume a 1GHz clock and 1.2V supply voltage, based on that projected for the forth-coming CL010LP TSMC low-power 0.1 μm process [30]. For configurations with dynamic voltage and frequency scaling, we assume 32 frequency points spanning a linear range from 1GHz down to 250MHz. Corresponding to these frequency points is a linear voltage range from 1.2V down to 0.65V. In Wattch, we simulate the effect of a 1.2–0.65V voltage range by using a range of 2.0–1.0833V because Wattch assumes a supply voltage of 2.0V. Our voltage range is tighter than that of XScale (1.65–0.75V), reflecting the compression of voltage ranges in future generations as supply voltages continue to be scaled aggressively relative to threshold voltages. In addition, the full frequency range is twice that of the full voltage range. As we demonstrate below, these factors limit the amount of power savings that can be achieved with conventional dynamic voltage and frequency scaling.

We assume two models for dynamic voltage and frequency scaling: an *XScale* model and a *Transmeta* model, both of which are based on published information from the respective companies [10, 13]. For both of these models, we assume that the frequency change can be initiated immediately when transitioning to a lower frequency and voltage, while the desired voltage must be reached first before increasing frequency. For the *Transmeta* model, we assume a total of 32 separate voltage steps, at 28.6mV intervals, with a voltage adjustment time of 20 μ s per step. Frequency changes require the PLL to re-lock. Until it does the domain remains idle. We model the PLL as a normally distributed locking circuit with a mean time of 15 μ s and a range of 10–20 μ s. For the *XScale* model, we assume that frequency changes occur as soon as the voltage changes, i.e., as the voltage is changed, the frequency is changed accordingly. There is no penalty due to a domain being idle waiting for the PLL: circuits execute through the change. To approximate a smooth transition, we use 320 steps of 2.86mV each, with 0.1718 μ s required to transition from one step to the next. Traversing the entire voltage range requires 640 μ s under the *Transmeta* model and 55 μ s under the *XScale* model.

Processor reconfiguration decisions (choices of times, frequencies, and voltages) could in principle be made in hardware, software, or some combination of the two, using information gathered from static analysis, on-line statistics, or feedback-based profiling. For the purposes of the current study we have attempted to identify the energy savings that might be achieved with good quality control algorithms, without necessarily determining what those algorithms should look like. More concretely, we employ an off-line tool that analyzes a trace collected during a full-speed run of an application in an attempt to determine the minimum frequencies and voltages that could have been used by various domains during various parts of the run without significantly increasing execution time. A list of these frequencies and voltages—and the times

they should be applied—is then fed back into our processor simulator in the course of a second, dynamic scaling run, to obtain accurate estimates of energy and performance.

It is unclear whether this experimental methodology will overestimate or underestimate the benefits that might be achieved by realistic on-line control algorithms: our feedback-based system can in principle use future knowledge, but it is not provably optimal: a good on-line strategy might conceivably do better. What the methodology does provide is an existence proof: with the frequencies and voltages chosen by our analysis tool one could expect to realize the energy savings described below.

The two subsections that follow describe, respectively, our multiple clock domain simulator and the analysis tool used to choose reconfiguration points.

The disadvantage of multiple clock domains is that data generated in one domain and needed in another must cross a domain boundary, potentially incurring synchronization costs as described in Section 2. In order to accurately model these costs, we account for the fact that the clocks driving each domain are independent by modeling independent jitter, the variation in the clock, on a cycle-by-cycle basis. Our model assumes a normal distribution of jitter with a mean of zero. The standard deviation is 110ps, consisting of an external Phase Lock Loop (PLL) jitter of 100ps (based on a survey of available ICs) and 10ps due to the internal PLL. These values assume a 1GHz on-chip clock generated from a common external 100MHz clock source. Despite the common use of the external clock, because the local clock sources are independent, the clock skew within individual domains is not a factor when calculating inter-domain penalties.

Our simulator tracks the relationships among all of the domain clocks on a cycle-by-cycle basis based on their scaling factors and jitter values. Initially, all the clocks are randomized in terms of their starting times. To determine the time of the next clock pulse in a domain, the

domain cycle time is added to the starting time, and the jitter for that cycle (which may be a positive or negative value) is obtained from the distribution and added to this sum. By performing this calculation for all domains on a cycle by cycle basis, the relationship between all clock edges is tracked. In this way, we can accurately account for synchronization costs due to violations of the $T > T_S$ relationship or to inter-domain clock rate differences.

For all configurations, we assume that all circuits are clock gated when not in use. We do not currently estimate the power savings or clock frequency advantage (due to reduced skew) from the absence of a conventional global clock distribution tree that supplies a low-skew clock to all chip latches.

To select the times and values for dynamic scaling in a given application, our reconfiguration tool begins by running the application on the simulator, at maximum speed. During this initial run we collect a trace of all primitive events (temporally contiguous operations performed on behalf of a single instruction by hardware in a single clock domain), and of the functional and data dependences among these events. For example, a memory instruction (load/store) is broken down into five events: fetch, dispatch, address calculation, memory access, and commit. Data dependences link these events in temporal order. Functional dependences link each event to previous and subsequent events (in different instructions) that use the same hardware units. Additional functional dependences capture the limited size of structures such as the fetch queue, issue queues, and reorder buffer. In the fetch queue, for example, event n depends on event $n-k$, where k is the size of the queue.

We use our trace information to construct a dependence directed acyclic graph (DAG) for each 50K cycle interval. (The length of this interval is chosen to be the maximum for which the DAG will fit in cache on our simulation servers.) Once the DAG has been constructed, we

proceed through two additional analysis phases. The first phase uses the DAG as input, and confines its work to a single interval. Its purpose is to “stretch” (scale) individual events that are not on the application’s critical execution path, as if they could, on an instruction-by-instruction basis, be run at a lower frequency. The final phase uses summary statistics from the first phase in order to cluster intervals into larger contiguous periods of time, with a uniform clock rate for each.

Whenever an event in the dependence DAG has two or more incoming arcs, it is possible—in fact likely—that one arc will constitute the critical path and that the others will have “slack”. This slack indicates that the previous operation completed earlier than necessary. If all of the outgoing arcs of an event have slack, then we have an opportunity (assuming zero-cost scaling) to save energy by performing the event at a lower frequency and voltage. With each event in the DAG we associate a power factor whose initial value is based on the relative power consumption of the corresponding clock domain, as determined by parameters in Wattch. When we stretch an event we scale its power factor accordingly. Calculations are made on a relative basis, on the assumption that energy is proportional to the square of the clock frequency. The stretching phase of our reconfiguration tool uses a “shaker” algorithm to distribute slack and scale edges as uniformly as possible. Since SimpleScalar, like any real processor, executes events as soon as possible subject to dependences and hazards, slack always appears at the ends of non-critical paths in the original execution trace. The shaker algorithm thus begins at the end of its 50K cycle interval and works backwards through the DAG. When it encounters an event whose outgoing edges all have slack, the shaker checks to see whether the power factor of the event exceeds a certain threshold, originally set to be slightly below the maximum power of any event in the graph. If so (this is a high-power event), the shaker scales the event until either it

consumes all the available slack or its power factor drops below the current threshold. If any slack remains, the event is moved later in time, so that as much slack as possible is moved to its incoming edges. When it reaches the beginning of the DAG, the shaker reverses direction, reduces its power threshold by a small amount, and makes a new pass forward through the DAG, scaling high-power events and moving slack to outgoing edges. It repeats this process, alternately passing forward and backward over the DAG, reducing its power threshold each time, until all available slack has been consumed, or until all events adjacent to slack edges have been scaled down to one quarter of their original frequency. When it completes its work for a given 50K cycle interval, the shaker constructs a summary histogram for each clock domain. Each histogram indicates, for each of the 320 frequency steps in the XScale model (being the maximum of the number of steps for the two models), the total number of cycles for the events in the domain and interval that have been scaled to run at or near that frequency.

Unfortunately, it turns out to be difficult to capture the behavior of the front end in terms of dependences among events. Unlike the time between, say, the beginning and the end of an add in the floating-point domain, the time between fetch and dispatch is not a constant number of cycles. In addition, experiments with manually selected reconfiguration points suggested that scaling of the front was seldom as beneficial as scaling of other domains. As a result, we have chosen to run the front at a steady 1GHz, and to apply the shaker algorithm to events in the other 3 domains only. Since the front end typically accounts for 20% of the total chip energy, this choice implies that any energy improvements we may obtain must come from the remaining 80%. Future attempts to address the front end may yield greater savings than are reported here.

The final, clustering phase of our off-line analysis tool recognizes that frequencies cannot change on an instantaneous, instruction-by-instruction basis. It also allows for a certain amount

of performance degradation. Using the histograms generated by the shaker, we calculate, for each clock domain and interval, the minimum frequency f that would permit the domain to complete its work with no more than d percent time dilation, where d is a parameter to the analysis. More specifically, we choose a frequency (from among 32 possible values for Transmeta and from among 320 possible values for XScale) such that the sum, over all events in higher bins of the histogram, of the extra time required to execute those events at the chosen frequency is less than or equal to d percent of the length of the interval. This calculation is by necessity approximate. It ignores ILP within domains: it assumes that the dilations of separate events in the same domain will have a cumulative effect. At the same time it ignores most dependences across domains: it assumes that the dilations of events in different domains will be independent. As an exception to this rule, we add the events of the load/store domain into the histogram of the integer domain. This special case ensures that effective address computations occur quickly when memory activity is high. For most applications the overall time dilation estimate turns out to be reasonably accurate: Figs. 5-7 and 8A-9B show performance degradation (with respect to the MCD baseline) that is roughly in keeping with d .

Whereas the shaker algorithm assumes that reconfiguration is instantaneous and free, the clustering algorithm must model reconfiguration times and costs. For each adjacent pair of intervals for a given domain, it merges histograms on a bin-by-bin basis and calculates the minimum frequency that would allow us to run the larger, combined interval at a single frequency. For the Transmeta power model we require that the time dilation of too-slow events together with the time required to reconfigure at interval boundaries not exceed d percent of total execution time. Since it eliminates one reconfiguration, merging intervals under the Transmeta model often allows us to run the combined interval at a lower frequency and voltage, thereby

saving energy. Most mergers under the XScale model occur when adjacent intervals have identical or nearly identical target frequencies. The clustering algorithm continues to perform mergers, recursively, so long as it is profitable from an energy standpoint to do so.

When it is done performing mergers, the clustering algorithm calculates the times at which reconfiguration must begin in order to reach target frequencies and voltages at target times. If reconfiguration is not possible, for example, because of a large swing in frequency that would take longer (because of the time to reduce or increase voltage) than the available interval, it is avoided. Since transitions in the Transmeta model take 20 μ s per voltage level, this results in the inability to accommodate short intervals with a large frequency variance. The algorithm completes its work by writing a log file that specifies times at which the application could profitably have requested changes in the frequencies and voltages of various domains. This file is then read by the processor simulator during a second, dynamic configuration run.

In this section, we compare the performance, energy, and energy-delay product of the MCD microarchitecture to that of a conventional singly clocked system. The base-line configuration is a single clock 1GHz Alpha 21264-like system with no dynamic voltage or frequency scaling. The baseline MCD configuration is split into four clock domains as described in Section 2 but with the frequency of all clocks statically set at 1GHz. This configuration serves to quantify the performance and energy cost of inter-domain synchronization. The dynamic 1% and dynamic 5% configurations are identical to baseline MCD except that they support dynamic voltage and frequency scaling within each clock domain. For the dynamic 1% case the clustering phase of our off-line reconfiguration tool uses a target of 1% performance degradation (beyond that of baseline MCD); for the dynamic 5% case it uses a target of 5%. Finally, the

global configuration models the baseline configuration with the addition of dynamic scaling of its single voltage and frequency, and serves to quantify the benefits of multiple clock domains.

The frequency for the global case is set so as to incur an overall performance degradation equal to that of the dynamic 5% configuration, and its voltage is correspondingly reduced. The energy savings of global is calculated by running each application under SimpleScalar and Wattch using the reduced frequency and voltage values. This approach permits the energy savings of the MCD approach to be compared to that of conventional voltage and frequency scaling for the same level of performance degradation. We performed a sanity check of the energy results of the global configuration by comparing the Wattch results against a simple calculation of the energy of the baseline configuration scaled relative to the square of the voltage ratios and found the results to agree to within 2%.

Figures 5, 6, and 7 display the performance degradation, energy savings, and change in energy $\times$ delay of the base-base-line MCD, dynamic 1%, dynamic 5%, and global configurations with respect to the baseline configuration, under the XScale model of voltage and frequency scaling. The Transmeta model produced far less promising results than the XScale model. Because of the roughly 15 μ s required to re-lock the PLL under the Transmeta model, reconfigurations are profitable much more rarely than they are under the XScale model, and energy improvements are much less. We will return to a comparison of the Transmeta and XScale models after discussing the XScale results in more detail.

The baseline MCD design, which simply uses multiple clock domains with no voltage or frequency scaling, shows an average performance degradation of less than 4%, with average energy cost of 1.5%. The resulting impact on energy-delay product approaches -10% for adpcm and -5% overall. Note that any overheads introduced by the algorithms add directly to this

baseline MCD overhead. For instance, the average dynamic 5% performance overhead is almost 10% or roughly what might be expected given the target degradation of 5% above the base-line MCD.

Our second observation is that the overall energy savings of the global approach is similar to its performance degradation, and averages less than 12% across the sixteen benchmarks. This result is somewhat counterintuitive, since when both frequency and voltage are reduced linearly by the same percentage, performance drops linearly with frequency, yet energy drops quadratically with voltage. Recall, however, that in our model a four-fold change in frequency (from 1GHz down to 250MHz) results in a less than two-fold change in voltage (from 1.2V down to 0.65V, modeled as 2.0V to 1.0833V in Wattch). As discussed above, this difference is due to the compression of voltage ranges relative to frequency ranges in successive process generations, as voltages are scaled down relative to threshold voltage, and frequencies are scaled up. The slope of the voltage curve has become much less steep than that of the frequency curve, greatly diminishing the quadratic effect on energy of a voltage reduction.

The MCD approaches, by contrast, achieve significant energy and energy $\times$ delay improvements with respect to the baseline configuration, with a comparatively minor overall performance degradation. For example, the dynamic 5% configuration achieves an average overall energy reduction of 27% and an energy $\times$ delay improvement of almost 20% relative to the baseline configuration, while incurring a performance degradation of less than 10% across the sixteen benchmarks under the XScale model. The dynamic 1% algorithm, which tries to more strictly cap the performance degradation at the expense of energy savings, trades off a significant energy savings to achieve this goal, resulting in an energy $\times$ delay improvement of

roughly 13%. Even so, this still far exceeds the 3% energy $\times$ delay improvement obtained with the global approach.

In several cases the opportunity to hide latency behind cache misses allows actual performance degradation to be significantly less than what one might expect from the frequencies chosen by the dynamic algorithm. In particular, the slack associated with L1 data cache misses often allows our reconfiguration tool to scale the integer and floating-point domains without significantly impacting overall performance (due to the fact that the available ILP is not sufficient to completely hide the miss latency), even when the utilization for these domains is high. The load/store domain, of course, must continue to operate at a high frequency in order to service the misses as quickly as possible, since the second level cache is in the same domain (unless we have a lot of level-two cache misses as well). The impact of misses can be seen in gcc (dynamic 1%), where the cache miss rate is high (12.5%) and the average frequency of the integer domain drops to approximately 920 MHz, but total performance degradation is less than 1%.

By contrast, branch mispredictions do not provide an opportunity for dynamic scaling: the dependence chain developed to resolve a branch precludes significant frequency reductions in the integer domain, and sometimes in the load/store domain as well. Applications that experience a high branch mispredict rate are likely to show performance degradation in accordance with frequency slowdown. This effect can be seen in swim, where the energy savings barely exceeds the performance degradation. (Here the floating point domain must also remain at a high frequency because of high utilization.)

The dynamic algorithm performs poorest with respect to global voltage scaling in g721. This is an integer benchmark with a well balanced instruction mix, high utilization of the integer

and load/store domains, a low cache miss rate, a low branch misprediction rate, and high baseline MCD overheads. Its IPC is relatively high (above 2), and the integer and load/store domains must run near maximum speed in order to sustain this. The floating point domain can of course be scaled back to 250MHz, but because of the high activity levels in the other domains, the resulting energy savings is a smaller fraction of total processor energy than it is in most of the other integer applications.

Comparing Figures 5–7 with corresponding results (not shown here) under the Transmeta scaling model, we found that the XScale model enables us to achieve significantly higher energy savings for a given level of performance degradation. The reasons for this result are illustrated in Figures 8A and 8B, which display the frequency settings chosen by our reconfiguration tool for a 30ms interval of the art benchmark, with a target performance degradation of 1%. In comparing Figs. 8A and 8B, note that under the XScale model (Fig. 8B) we are able both to make a larger number of frequency changes and to make those changes over a wider range of frequencies. In particular, while art is a floating-point intensive application, there are many instruction intervals during which we can safely scale back the floating-point domain. Because of its 10–20 μ s PLL relock penalty, the Transmeta model does not allow us to capture this comparatively short-term behavior.

Figures 9A and 9B present summary statistics for the intervals chosen by our off-line reconfiguration tool in all 16 applications, under both the Transmeta and XScale models. Those figures show summary statistics for intervals chosen by the off-line tool for the dynamic 5% configuration for Transmeta and XScale reconfiguration data, respectively. Solid bars indicate, for the integer, load-store, and floating-point domains, the number of reconfigurations requested per 1 million instructions. Points above the bars indicate the average frequencies chosen for

those domains. “Error bars”, where shown, indicate the range of dynamic frequencies for the domain. While the average frequencies chosen for the integer, load-store, and floating-point domains are similar in the two graphs, the total number of reconfigurations is much lower under the Transmeta model, and the frequency ranges are narrower.

5 Figures 8A through 9B all illustrate the value of using different frequencies in different clock domains: by controlling these frequencies independently we can maintain the required frequency in domains that are critical to performance, while aggressively scaling those domains that are less performance-critical. The floating-point domain in particular can be scaled back to the lowest available frequency in many applications, including some that include non-trivial
10 numbers of floating-point operations. Note, however, that due to clock gating, the floating point domain is often not the largest source of energy dissipation for integer programs: the integer domain often is the largest source and thus even modest adjustments of its domain voltage yield significant energy savings. Furthermore, although one would expect dynamic scaling to reduce static power as well, we have not quantified the corresponding contribution to the energy
15 savings. Dynamic voltage gating might achieve additional savings (given appropriate support for saving/restoring critical processor state), and would seem to be a promising avenue for future research.

Several manufacturers, notably Intel [21] and Transmeta [16], have developed processors capable of global dynamic frequency and voltage scaling. Since minimum operational voltage is
20 roughly proportional to frequency, and power is roughly proportional to the voltage squared, this dynamic scaling can be of major benefit in applications with real-time constraints for which the processor as a whole is over-designed: for example, video rendering. Marculescu [23] and Hsu et al. [18] evaluated the use of whole-chip dynamic voltage scaling with minimal loss of

performance using cache misses as the trigger [23]. Other work [7, 26] has also begun to look at steering instructions to pipelines or functional units running statically at different speeds so as to exploit scheduling slack in the program to save energy. Our contribution is to demonstrate that a microprocessor with multiple clock domains provides the opportunity to reduce power consumption on a variety of different applications without a significant performance impact by reducing frequency and voltage in domains that do not contribute significantly to the critical path of the current application phase.

Govil et al. [15] and Weiser et al. [31] describe interval-based strategies to adjust the CPU speed based on processor utilization. The goal is to reduce energy consumption by attempting to keep the processor 100% utilized without significantly delaying task completion times. A history based on the utilization in previous intervals is used to predict the amount of work and thereby adjust speed for maximum utilization without work backlog. Perring et al. [25] apply a similar principle to real-time and multimedia applications. Similarly, Hughes et al. [19] use instruction count predictions for frame based multimedia applications to dynamically change the global voltage and frequency of the processor while tolerating a low percentage of missed frame deadlines. Bellosa [2, 3] describes a scheme to associate energy usage patterns with every process in order to control energy consumption for the purposes of both cooling and battery life. Cache and memory behavior as well as process priorities are used as input in order to drive the energy control heuristics. Benini et al. [4] present a system that monitors system activity and provides information to an OS module that manages system power. They use this monitoring system in order to demonstrate how to set the threshold idle time used to place a disk in low-power mode. Our work differs in that we attempt to slow down only those parts of the processor that are not on an application's critical path.

Fields et al. [12] use a dependence graph similar to ours, but constructed on the fly, to identify the critical path of an application. Their goal is to improve instruction steering in clustered architectures and to improve value prediction by selectively applying it to critical instructions only. We use our graph off-line in order to slow down non-critical program paths. Li et al. [22] explore the theoretical lower bound of energy consumption assuming that both the program and the machine are fully adjustable. Assuming equal energy dissipation in all hardware components, they show that a program with balanced load on all components consumes less energy than one with significant variance.

Childers et al. [9] propose to trade IPC for clock frequency. The user requests a particular quality of service from the system (expressed in MIPS) and the processor uses an interval-based method to monitor the IPC and adjust the frequency and voltage accordingly. In their work, a process with high IPC will run at a low clock frequency while a process with low IPC will run at a high clock frequency, which is contrary to what is required for some applications (e.g., when low IPC is due to high miss rates). Our techniques work to achieve the exact opposite in order to provide maximum performance with minimum energy.

While a preferred embodiment of the present invention has been set forth above, those skilled in the art who have reviewed the present disclosure will readily appreciate that other embodiments can be realized within the scope of the invention. For example, numerical values and fabrication techniques are illustrative rather than limiting. Also, while four domains have been disclosed, it is possible to implement a processor with more or fewer domains and with different boundaries among the domains. Other possible variations of the invention have been noted above. Therefore, the present invention should be construed as limited only by the appended claims.

We claim:

1. A multiple-clock-domain microprocessor comprising:

a plurality of domains; and

for each of the plurality of domains, a clock for separately generating a clock signal for

5 that domain.

2. The microprocessor of claim 1, wherein each said clock comprises a phase-locked loop, and wherein the microprocessor further comprises means for receiving an externally generated clock signal and for supplying the externally generated clock signal to each said phase-locked loop.

10 3. A method of operating a microprocessor, the method comprising:

providing a plurality of domains in the microprocessor;

clocking each of the domains separately; and

operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another.

15

Abstract of the Disclosure

A multiple clock domain (MCD) microarchitecture uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-
5 domain communication. Thus, fully synchronous design practices are used in the design of each domain.

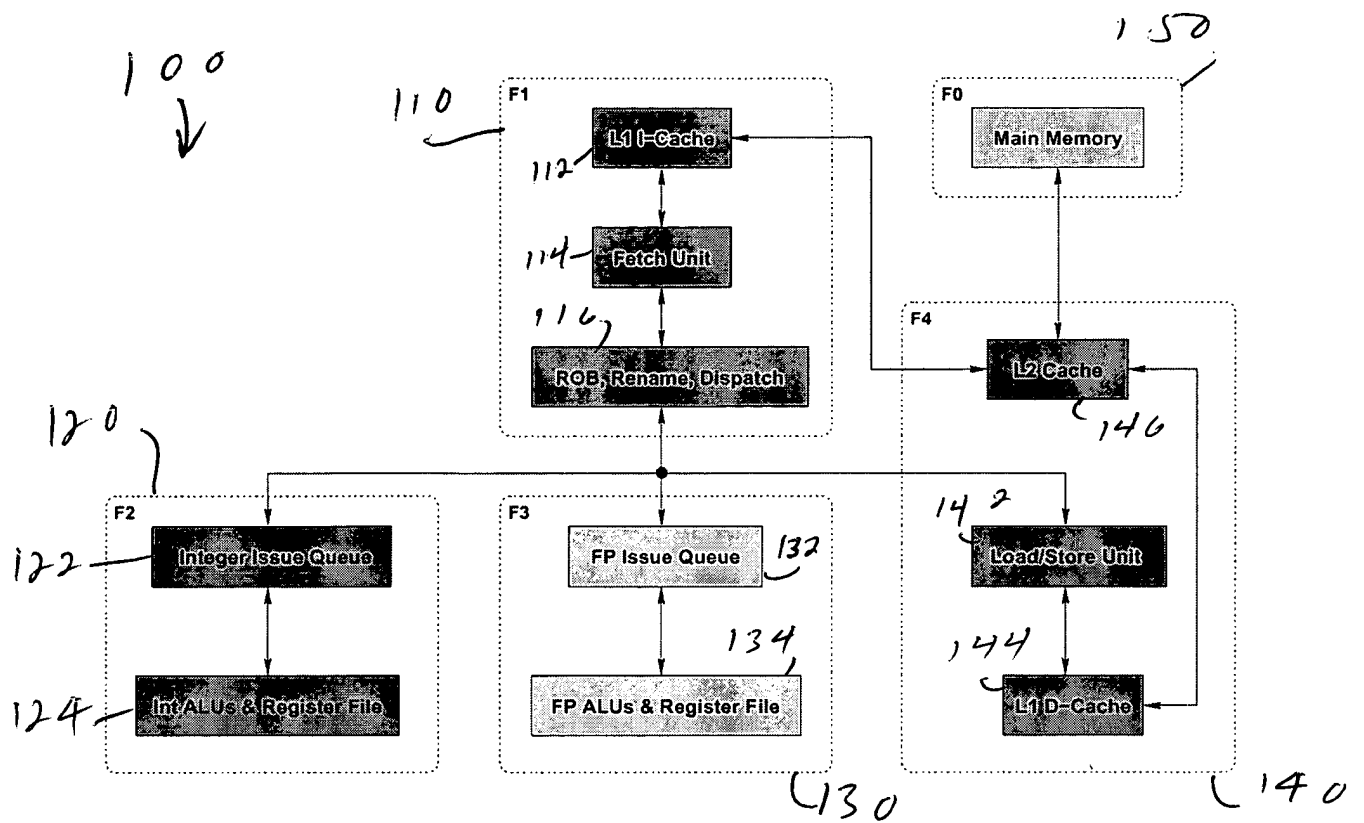


Figure 1

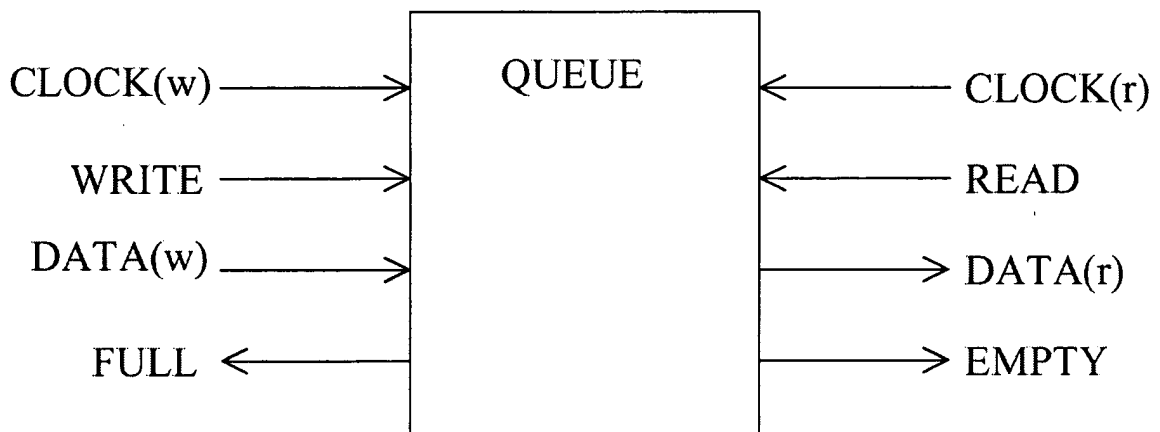


Figure 2

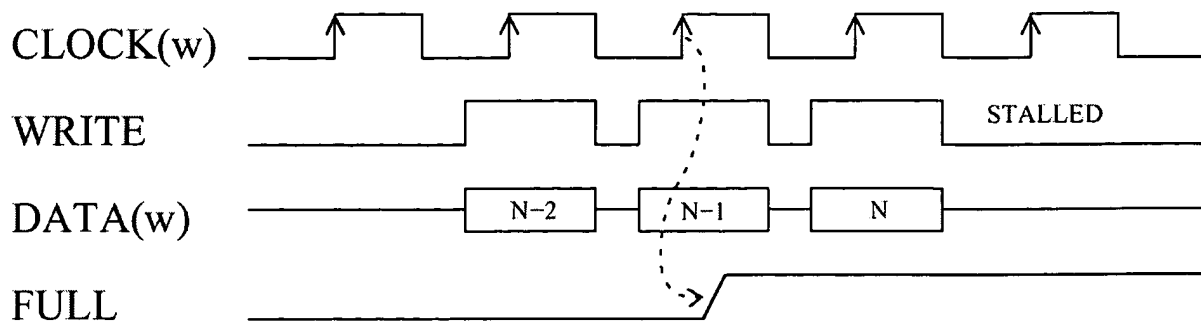


Figure 3

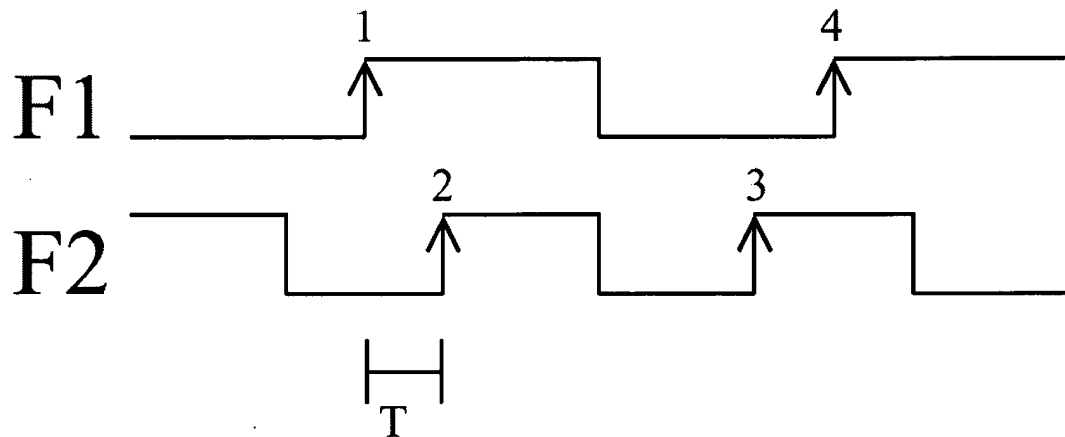


Figure 4

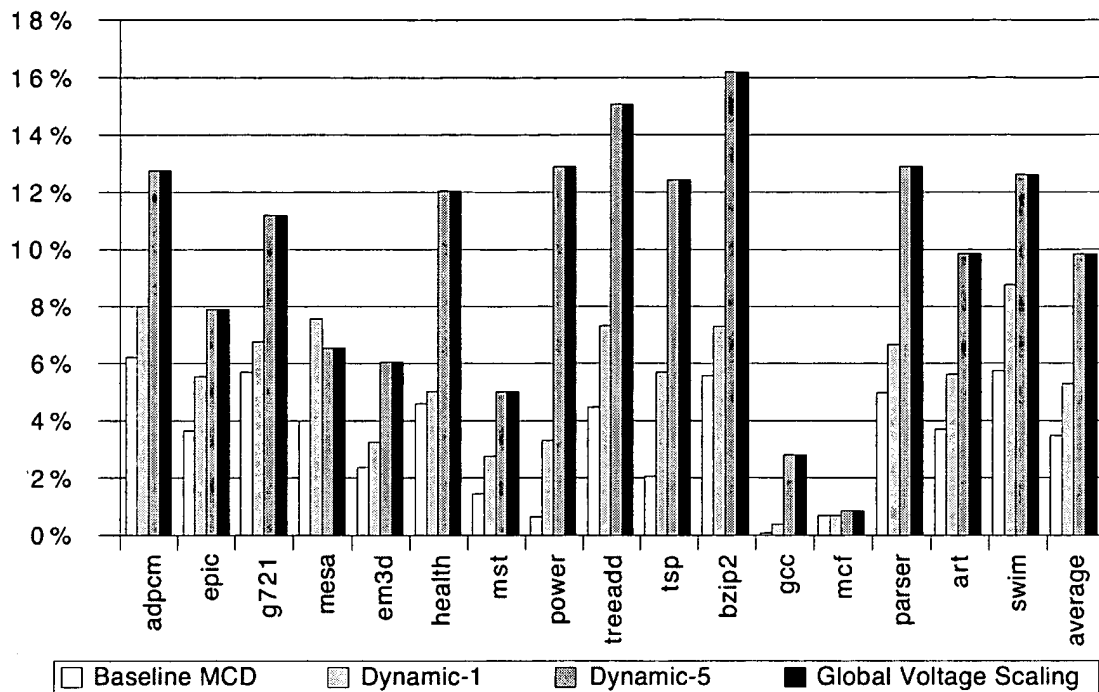


Figure 5

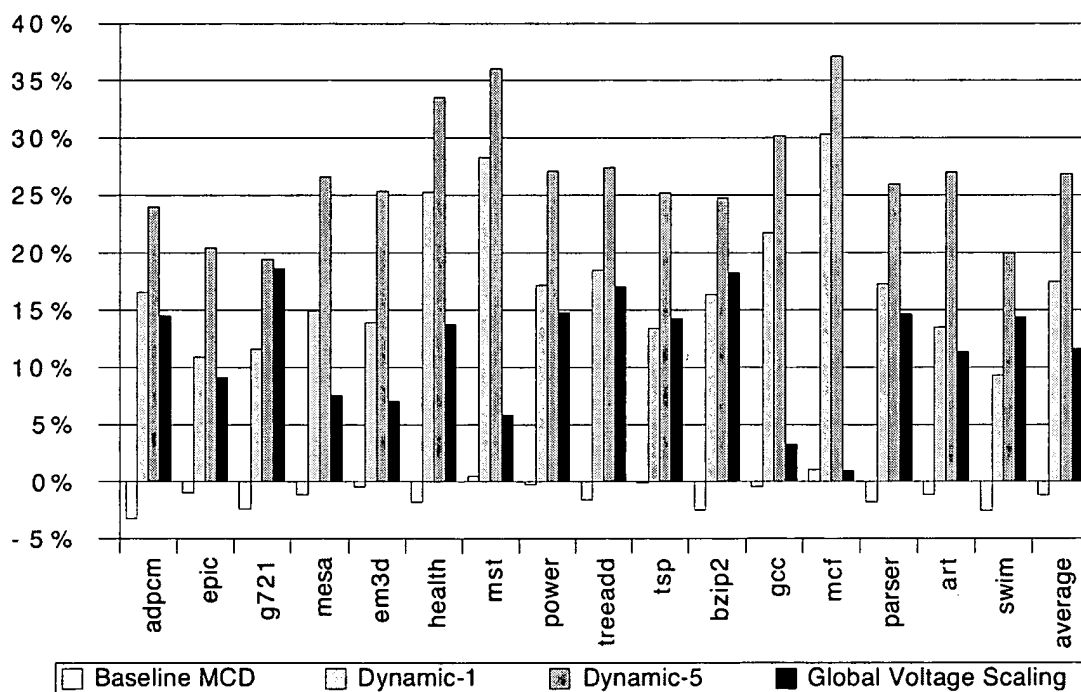


Figure 6

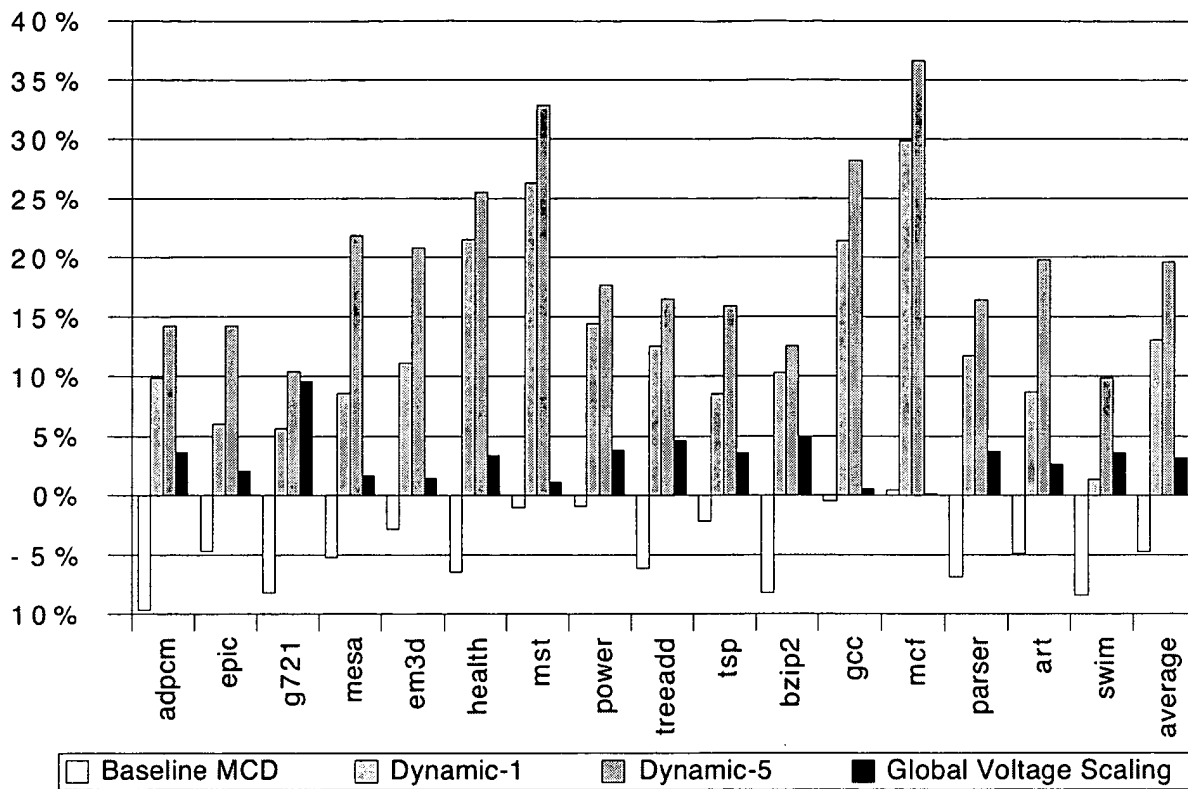


Figure 7

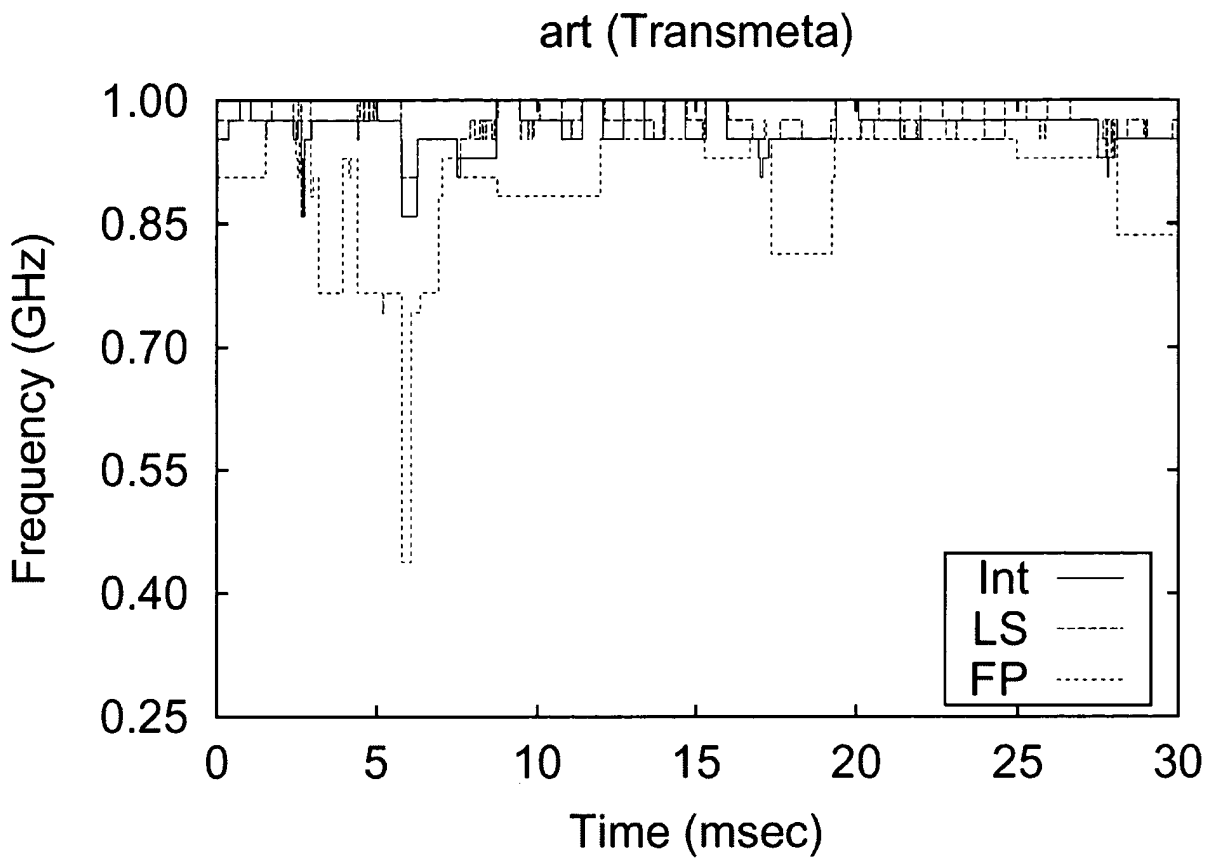


Figure 8A

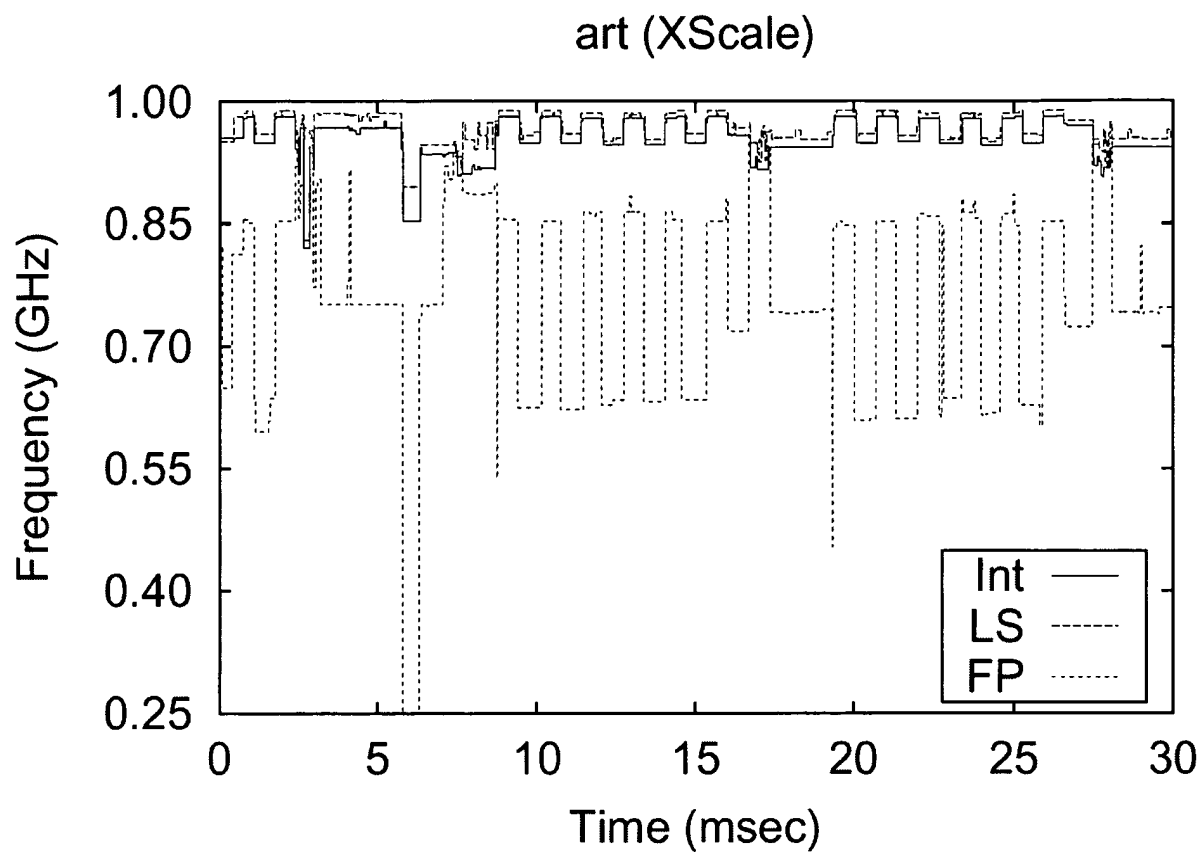


Figure 8B

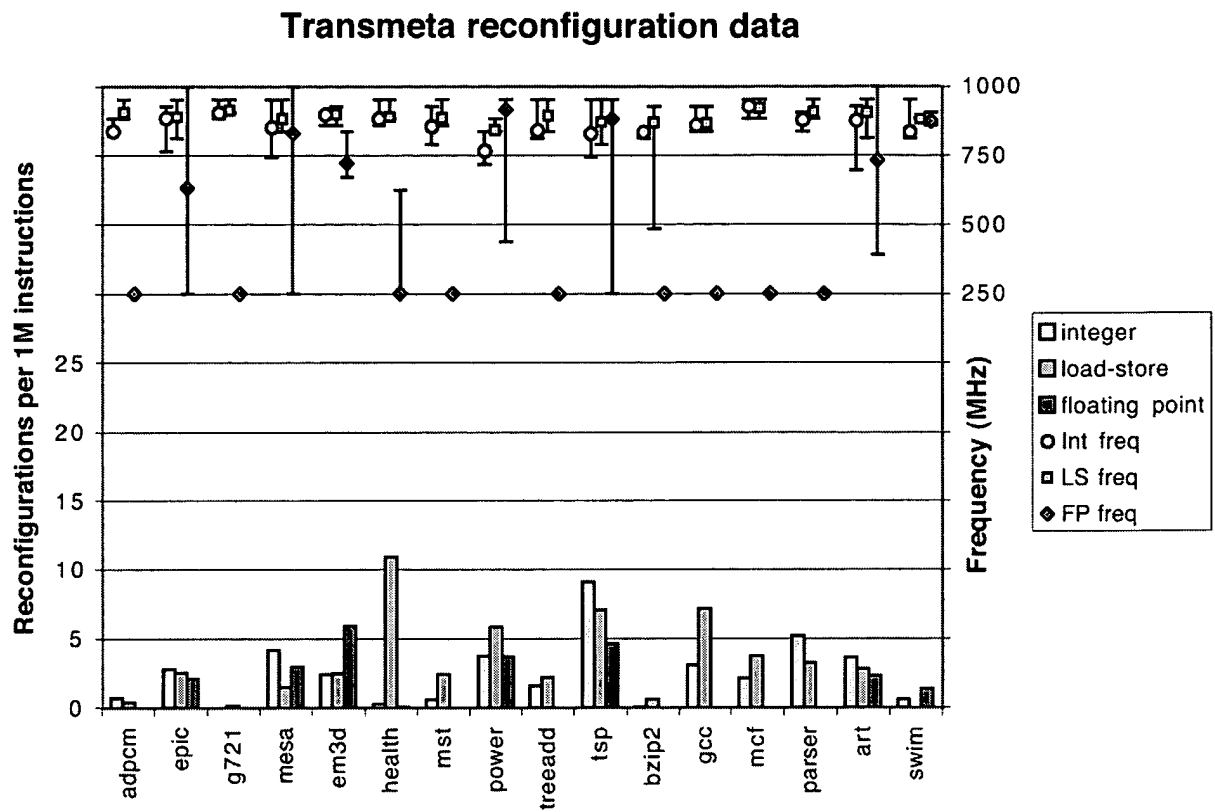


Figure 9A

X-Scale reconfiguration data

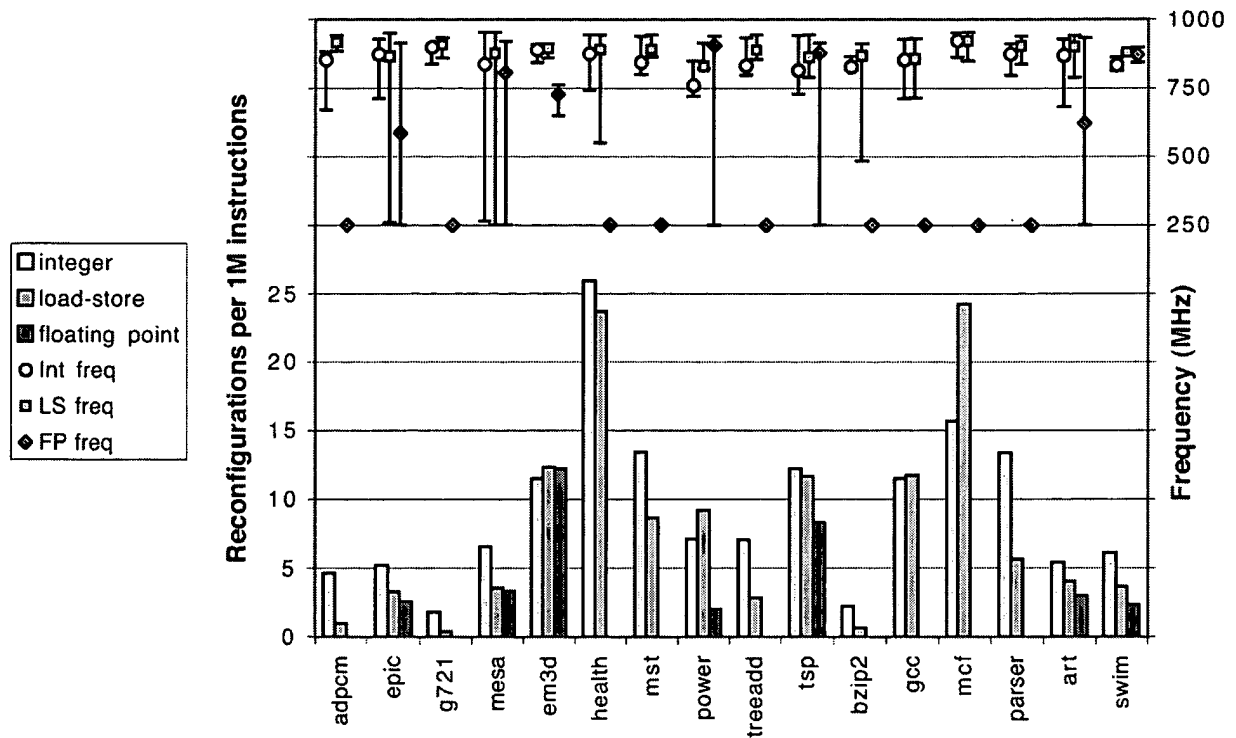


Figure 9B

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2003

Application or Docket Number

10 762 550

CLAIMS AS FILED - PART I

(Column 1) (Column 2)

TOTAL CLAIMS	3	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	3 minus 20=	*
INDEPENDENT CLAIMS	2 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

(Column 1) (Column 2) (Column 3)

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*		Minus	**	=
Independent	*		Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐					

(Column 1) (Column 2) (Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*		Minus	**	=
Independent	*		Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐					

(Column 1) (Column 2) (Column 3)

AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*		Minus	**	=
Independent	*		Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐					

SMALL ENTITY
TYPE ☐

OR OTHER THAN
SMALL ENTITY

RATE	FEE
BASIC FEE	385.00
X\$ 9=	
X43=	
+145=	
TOTAL	385

RATE	FEE
BASIC FEE	770.00
X\$18=	
X86=	
+290=	
TOTAL	

SMALL ENTITY

OR OTHER THAN
SMALL ENTITY

RATE	ADDI- TIONAL FEE
X\$ 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
X\$ 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
X\$ 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDI- TIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.