

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.
Petitioner

v.

UNIVERSITY OF ROCHESTER
Patent Owner

Case No. IPR2024-01225
Patent No. 7,089,443 B2

DECLARATION OF ANKIT AGGARWAL IN SUPPORT OF PETITION

I, Ankit Aggarwal, make the following declaration pursuant to 28 U.S.C.

§ 1746:

1. I am an attorney at the law firm of Bookoff McAndrews PLLC.
2. I provide this Declaration in connection with the above-identified *Inter Partes* Review proceeding requested at the United States Patent and Trademark Office by Lenovo (United States) Inc. against University of Rochester under 35 U.S.C. § 311, 37 C.F.R. § 42.104. Unless otherwise stated, the facts stated in this Declaration are based on my personal knowledge.
3. Exhibit 1010 is a true and correct copy of Webpage for Datamath Calculator Museum - archived by WayBackMachine on February 26, 2001, which I personally obtained online from the website <https://web.archive.org/web/20010424233617/http://datamath.org:80/Story/Intel.htm> on July 29, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.
4. Exhibit 1011 is a true and correct copy of Stanley Mazor, *The History of the Microcomputer-Invention and Evolution*, (1995), which I personally downloaded online from the website <https://people.engr.tamu.edu/djimenez/taco/utsa-www/cs5513-fall07/reader/mazor-microcomputer.pdf> on July 29, 2024. An exhibit

label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

5. Exhibit 1012 is a true and correct copy of William M. Johnson, *Super-Scalar Processor Design*, (1989), which I personally downloaded online from the website https://vlsiweb.stanford.edu/people/alum/pdf/8906_MikeJohnson_SuperScalar_Processor_Design.pdf on July 29, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

6. Exhibit 1013 is a true and correct copy of Altera Corporation, *Excalibur Arm-Based Hardware Reference Manual*, January 2001, which I personally downloaded online from the website https://cdrdv2-public.intel.com/655167/exc_arm_hwdref_mnl.pdf on July 29, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

7. Exhibit 1014 is a true and correct copy of Texas Instruments, *TMS320C64x Technical Overview*, January 2001, which I personally downloaded online from the website <https://www.ti.com/lit/ug/spru395b/spru395b.pdf?ts=1721933464110> on July 29, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

8. Exhibit 1015 is a true and correct copy of Kenneth C. Yeager, *The MIPS R100 Superscalar Microprocessor*, (1996), which I personally downloaded online from the website

<https://compas.cs.stonybrook.edu/~nhonarmand/courses/sp16/cse502/res/R10k.pdf>

on July 29, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

9. Exhibit 1016 is a true and correct copy of Texas Instruments, *FIFO Architecture, Functions, and Applications*, November 1999, which I personally downloaded online from the website

<https://www.ti.com/lit/an/scaa042a/scaa042a.pdf> on July 29, 2024. An exhibit label

on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

10. Exhibit 1017 is a true and correct copy of Eric Tune *et al.*, *Dynamic Prediction of Critical Path Instructions*, (2001), which I personally downloaded online from the website <https://cseweb.ucsd.edu/~tullsen/hpca00.pdf> on July 29, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

11. Exhibit 1019 is a true and correct copy of Anand Lal Shimpi, *AMD's K6-2+ in Notebooks – Evaluating Performance with PowerNow*, September 12, 2000

which I personally downloaded online from the website

<https://www.anandtech.com/show/620/3> on July 29, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

12. Exhibit 1020 is a true and correct copy of Anand Lal Shimpi, *AMD's K6-2+ in Notebooks – Evaluating Performance with PowerNow*, September 12, 2000, which I personally downloaded online from the website

<https://www.anandtech.com/show/620/5> on July 29, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

13. Exhibit 1021 is a true and correct copy of Bruce R. Childers *et al.*, *Adapting Processor Supply Volatage to Instruction-Level Parallelism*, (2001), which I personally downloaded online from the website

<https://people.cs.pitt.edu/~melhem/vita/doc/koolchips00.pdf> on July 29, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

14. Exhibit 1022 is a true and correct copy of Andrew Royal *et al.*, *GALS, Globally Asynchronous, Locally Synchronous Systems*, April 27th, 2001, which I personally downloaded online from the website

<https://cas.ee.ic.ac.uk/old/students/andy/gals.html> on July 29, 2024. An exhibit

label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

15. Exhibit 1026 is a true and correct copy of Actel Corporation, *3200DX Dual-Port Random Access Memory (RAM)*, September 1997, which I personally downloaded online from the website

https://ww1.microchip.com/downloads/aemdocuments/documents/fpga/ApplicationNotes/ApplicationNotes/3200dx_ram_an.pdf on July 15, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

16. Exhibit 1027 is a true and correct copy of Barr Group, *Types of Memory in Embedded Systems*, May 1, 2001, which I personally downloaded online from the website <https://barrgroup.com/blog/types-memory-embedded-systems> on July 27, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

17. Exhibit 1028 is a true and correct copy of Wavecrest corporation, *Understanding Jitter*, 2001, which I personally downloaded online from the website <https://www.hep.ucl.ac.uk/~mp/ELECTRONICS/Clock-Jitter-Understanding.pdf> on July 17, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

18. In signing this declaration, I understand that willful and false statements and the like are punishable by fine or imprisonment, or both.

19. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

I declare under penalty of perjury that the foregoing is true and correct. Executed this 30th day of July, 2024, at Washington, D.C.



By: _____
Ankit Aggarwal