

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.,

Petitioner,

v.

UNIVERSITY OF ROCHESTER
(INTELLECTUAL VENTURES I, LLC),

Patent Owner.

Case No. IPR2024-01225

U.S. Patent No. 7,089,443

PATENT OWNER'S PRELIMINARY RESPONSE

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PATENT OWNER'S EXHIBIT LIST

Ex. 2001	Declaration of Dr. David Kaeli
Ex. 2002	Resume of Dr. David Kaeli
Ex. 2003	Declaration of David H. Albonesi
Ex. 2004	L. F. G. Sarmenta, G. A. Pratt, and S. A. Ward. Rational Clocking. In Proceedings of the International Conference on Computer Design, Austin, Tex., October 1995
Ex. 2005	Semeraro et al, "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," High Performance Computer Architecture (HPCA), Feb. 2, 2002
Ex. 2006	Provisional Application No. 60/311,575, filed August 10, 2001
Ex. 2007	Provisional Application No. 60/337,837, filed November 5, 2001
Ex. 2008	Provisional Application No. 60/337,479, filed November 5, 2001
Ex. 2009	Provisional Application No. 60/338,510, filed November 5, 2001
Ex. 2010	SimpleScalar Tutorial

I. INTRODUCTION

The Petition (Paper #2) challenges claims 1 and 2-12 (“Challenged Claims”) of U.S. Patent No. 7,089,443 (“’443 Patent,” Ex. 1001) under seven grounds. Pet., 3-4. The Petition fails to present a reasonable likelihood of success in connection with any of the grounds.

The ’443 Patent describes the design and implementation of a microprocessor architecture utilizing a globally asynchronous, locally synchronous (GALS) clocking architecture in which each domain includes a separate clock for generating a clock signal at a frequency for that domain. Ex. 1001, 4:13-16; 40-45. Among other features, the frequency in each domain is dynamically changeable independently of the frequencies of the clock signals generated for other domains. *Id.*, claim 1. The transformative nature of this architecture has been widely recognized, including the receipt of a prestigious Test of Time Award in 2023. Ex. 2003, ¶9.

On the merits, the Petition is deficient because the invention’s novel features, including a globally-asynchronous, locally-synchronous architecture with separate and independently adjustable clock domains, are clearly distinguished from the prior art, such as Shenai and Georgiou, that relied on restrictive synchronization techniques such as “rational factor” frequency relationships.

On the issue of discretionary denial, Petitioner waited almost a full year after service of the complaint in parallel patent infringement litigation to file this

challenge. As a result, the parallel litigation (in which Petitioner is advancing the same prior art relied on in the Petition) has already reached an advanced stage, with a trial scheduled to occur long before any Final Written Decision would be issued in these proceedings. Based on these facts, and as explained more fully below, all of the *Fintiv* factors favor a discretionary denial of the Petition.

II. SPECIFICATION OF '443 PATENT

A. Summary Of The Invention

As explained in the Summary of the Invention of the '443 Patent:

... the present invention is directed to a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. Ex. 1001, 4:13-19 (emphasis added).

As explained next in the Summary of the Invention, the inventors identified several "potential" advantages of the MCD design, including "lower energy:"

Although the inter-domain synchronization increases the number of clock cycles required to run a given application, an MCD microprocessor affords a number of potential advantages over a singly clocked design: ...

The independence of each local domain clock implies no global skew requirement...

Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain

allows for finer grained dynamic voltage and frequency scaling, and thus lower energy, than can be achieved with single clock, single-core-voltage systems. Ex. 1001, 6:22-45. (emphasis added).

Next, in the Summary of the Invention, the inventors explained that they implemented their MCD design and found that it achieved significant performance advantages:

In the present application, we describe an initial implementation of an MCD microprocessor that is a straightforward extension of a singly-clocked synchronous dynamic superscalar design. By accurately modeling inter-domain synchronization, we characterize the performance and energy costs of the required synchronization circuitry. We then explore the potential benefits of per-domain dynamic voltage and frequency scaling. Our results demonstrate a 20% average improvement in energy-delay product for a set of benchmarks that includes both compute and memory-bound applications. ...

Performance results for applications drawn from standard benchmark suites suggest that the division of the processor into multiple domains incurs an average baseline performance cost of less than 4%. At the same time, by scaling frequency and voltage in different domains dynamically and independently, we can achieve an average improvement in energy-delay product of nearly 20%. By contrast, global voltage scaling to achieve comparable performance degradation in a singly clocked microprocessor achieves an average energy-delay improvement of only 3%. Ex. 1001, 4:51-5:14 (emphasis added).

At the end of the Summary of The Invention, the inventors noted that "the invention" was described in an earlier paper by the inventors:

The following Paper describes the invention and is hereby incorporated by reference in its entirety into the present disclosure: Semeraro et al, "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," *High Performance Computer Architecture (HPCA)*, Feb. 2, 2002. Ex. 1001, 5:22-27.

The above-referenced Paper is referred to hereinafter as "the Paper," and attached hereto as Ex. 2005. As explained more fully in Section III, *infra*, the salient portions of the '443 Patent specification were lifted almost verbatim from the Paper. The findings of the inventors set forth in the Paper and reproduced in the '443 Patent were nothing short of groundbreaking. In 2023, this work was awarded the Technical Committee on Computer Architecture's 2022 Test of Time Award at the 29th IEEE International Symposium on High-Performance Computer Architecture. Ex. 2003, ¶9. The Test of Time Award "recognizes the most influential papers published in prior sessions of the International Symposium of High Performance Computer Architecture (HPCA) each of whom have had significant impact in the field." Ex. 2003, ¶10. The Paper has been cited 575 times since it was published.

B. Detailed Description

The Detailed Description of '443 Patent distinguished the MCD processor disclosed in the '443 Patent from prior synchronization schemes that restricted the relative frequencies of the clocks:

Some synchronization schemes restrict the ... relative frequencies of the clocks, thereby eliminating the need for hardware arbitration [27]. Unfortunately, these schemes impose significant restrictions on the possible choices of frequencies. ... Ex. 1001, 6:32-36 (emphasis added).

As discussed more fully below, reference [27] referred to in the above quotation corresponded to a paper by Sarmenta (Ex. 2004) that described systems that placed

significant restrictions on the possible choices of frequencies. As Dr. Kaeli explains, “[t]he ‘443 invention overcomes these limitations, offering independence in clock frequency generation, allowing each frequency domain to adopt their own independent frequency, offering near infinite resolution in terms of the clock frequency selected for each domain.” Ex. 2003, ¶38.

III. THE CLAIMED INVENTION HAD BEEN CONCEIVED AND ACTUALLY REDUCED TO PRACTICE BY FEBRUARY 2002

A. Legal Principles

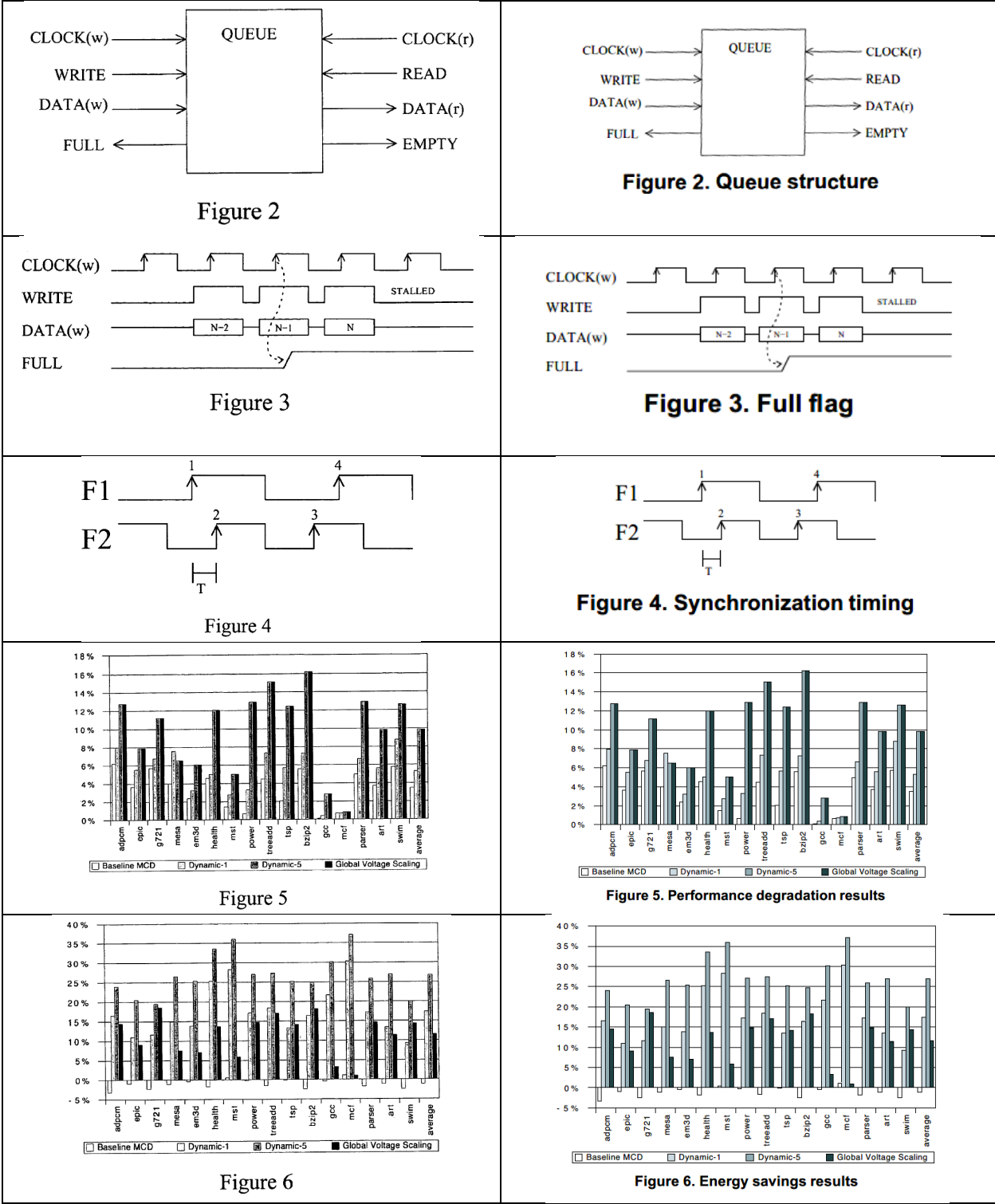
A patent owner can antedate an asserted prior art reference by showing conception and actual reduction to practice prior to the date of the reference. *Medtronic, Inc. v. Teleflex Life Scis. Ltd.*, 86 F.4th 902, 906 (Fed. Cir. 2023). “Conception can be proven with evidence that a full description,” of the invention existed “in written materials disclosed to persons,” in the United States. *Scott v. Koyama*, 281 F. 3d 1243, 1247 (Fed. Cir. 2002). “Reduction to practice in the United States requires that the invention be embodied in tangible form in the United States,” and “that the invention, as conceived, was shown to work for its intended purpose.” *Id.*; *In re Steed*, 802 F. 3d 1311, 1316 (Fed. Cir. 2015). In connection with the requirement that the invention be embodied in a tangible form, it is well-settled that a computer program with executable instructions stored in memory (e.g., on a

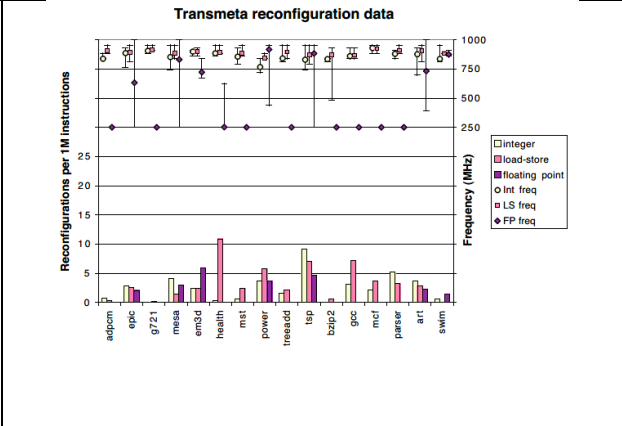
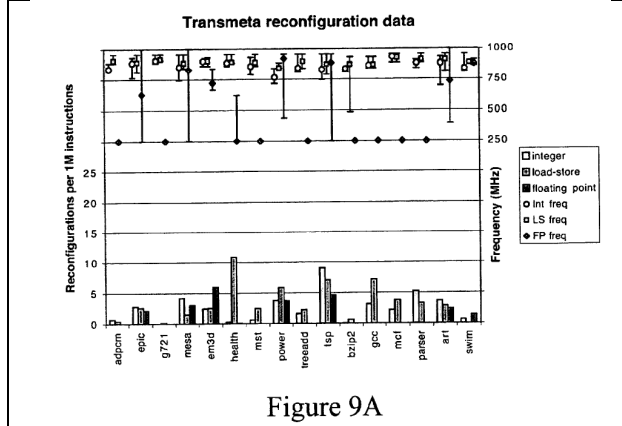
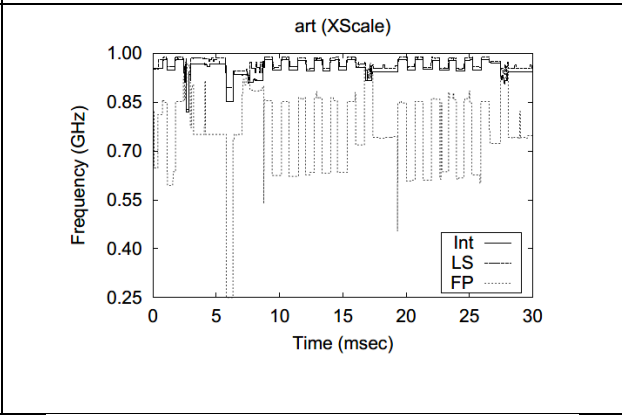
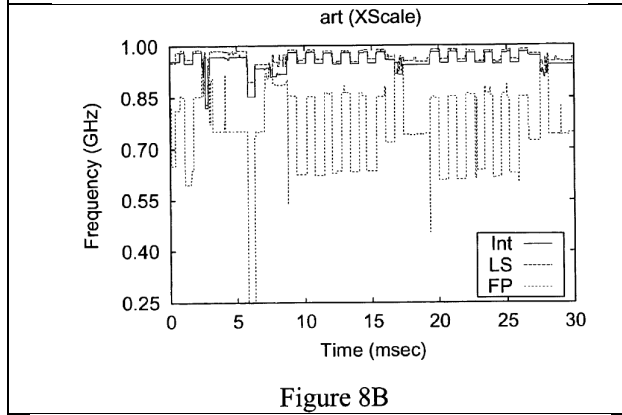
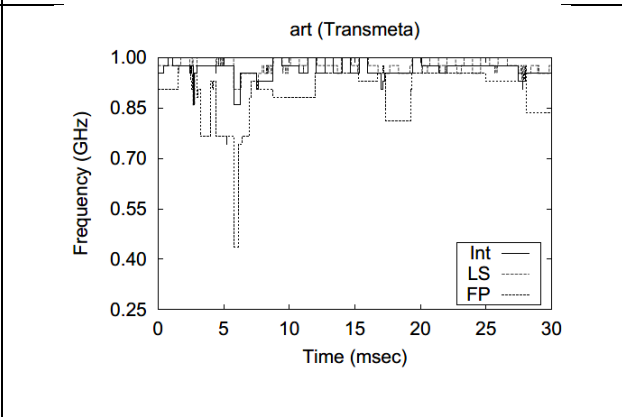
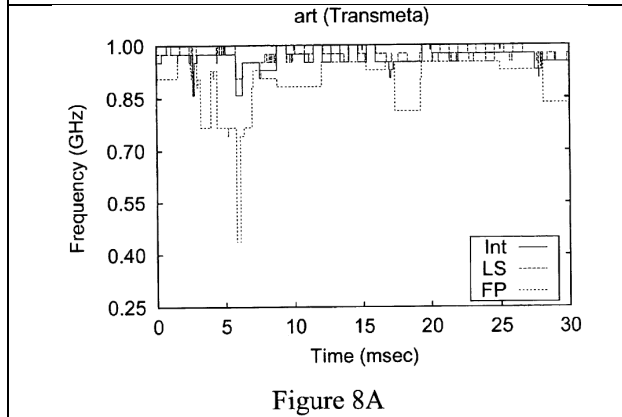
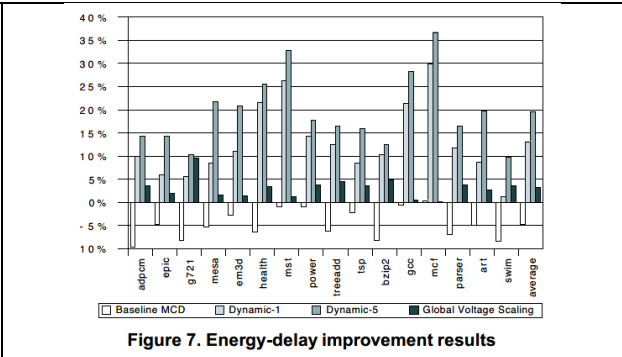
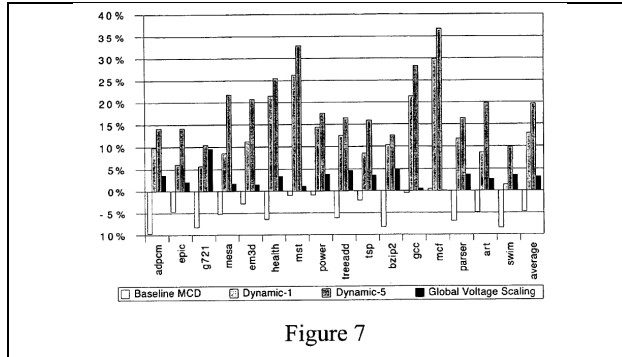
computer disk) is embodied in a tangible form. *In re Beauregard*, 53 F.3d 1583 (Fed. Cir.1995).

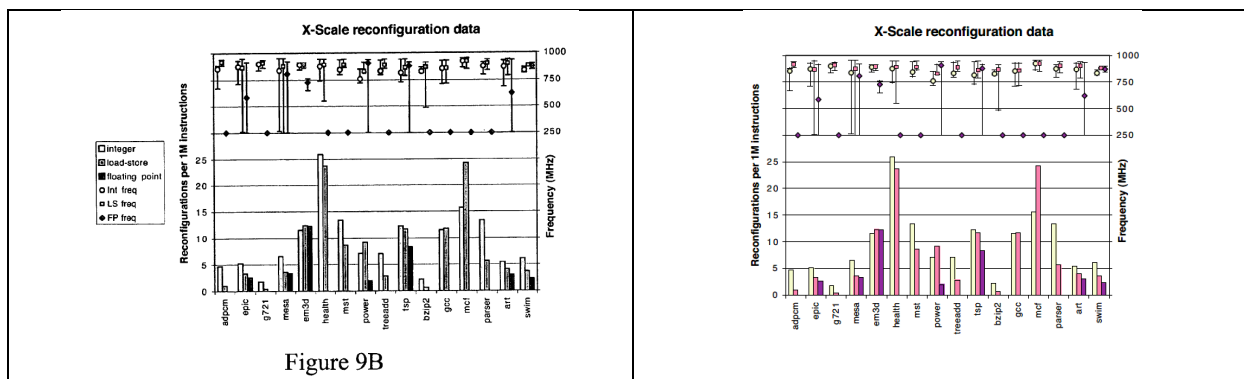
B. The Paper Authored By The Inventors And Published In February 2002 Demonstrates Conception By Providing A Full Written Description Of The Claimed Invention

As noted above, the '443 Patent cited and incorporated by reference the Paper (i.e., Semeraro et al, “Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling,” High Performance Computer Architecture (HPCA), Feb. 2, 2002). Ex. 1001, 5:22-27; Ex. 2005. The Paper was published in *Proceedings Eighth International Symposium on High Performance Computer Architecture*, pp. 29-40 in February, 2002. Ex. 2003, ¶5. The authors of the Paper coincide identically with the named inventors on the '443 Patent. *Id.* As shown below, with the exception of reference numerals, all of the figures contained in the '443 Patent are substantively identical to corresponding figures in the Paper. Ex. 2003, ¶8.

Figure from '443 Patent	Corresponding Figure in Paper
Figure 1	Figure 1. Multiple clock domain processor block diagram







Given the overlap in the figures, it should not be surprising that the wording of the '443 Patent closely tracks that of the Paper. For example, the first three paragraphs of the Introduction section of the Paper are reproduced virtually verbatim as the first three paragraphs in the Background of the '443 Patent (Ex. 1001 , 1:25-2:14; Ex. 2005, at 1-2), and the 31 references listed at the end of the Paper are listed identically at the end of the Background of the '443 Patent. Ex. 1001, 2:17-4:4; Ex. 2005, at 11-12). In addition, as shown below, the salient aspects of the Summary of the Invention of the '443 Patent (Ex. 1001, 4:6-5:21) are taken verbatim from the Introduction section of the Paper (Ex. 2005, 2):

Summary of Invention of '443 Patent	Corresponding Language In Introduction of Paper
It is another object of the invention to provide an approach that allows for aggressive future frequency increases, maintains a synchronous design methodology, and exploits the trend towards making functional blocks more autonomous.	An approach that allows for aggressive future frequency increases, maintains a synchronous design methodology, and exploits the trend towards making functional blocks more autonomous, is ...

To achieve the above and other objects, the present invention is directed to a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. Thus, fully synchronous design practices are used in the design of each domain. Although the inter-domain synchronization increases the number of clock cycles required to run a given application, an MCD microprocessor affords a number of potential advantages over a singly clocked design: ... Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain allows for finer grained dynamic voltage and frequency scaling, and thus lower energy, than can be achieved with single clock, single-core-voltage systems. ... In the present application, we describe an initial implementation of an MCD microprocessor that is a straightforward extension of a singly-clocked synchronous dynamic superscalar design.	a <i>multiple clock domain (MCD)</i> microarchitecture, which uses a <i>globally-asynchronous, locally-synchronous (GALS)</i> clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. Thus, fully synchronous design practices are used in the design of each domain. Although the inter-domain synchronization increases the number of clock cycles required to run a given application, an MCD microprocessor affords a number of potential advantages over a singly clocked design: ... Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain allows for finer grained dynamic voltage and frequency scaling, and thus lower energy, than can be achieved with single clock, single-core-voltage systems. ... In this Paper, we describe an initial implementation of an MCD microprocessor that is a straightforward extension of a singly-clocked synchronous dynamic superscalar design.
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Below is a mapping demonstrating a description of each element of claims 1-7 of the '443 Patent in the Paper. While not shown, the mappings for claims 8, 9, 10, 11 and 12 of the '443 Patent correspond to the mappings below for claims 1, 4, 5, 6 and 3, respectively.

Claim 1

<u>Claim Element</u>	<u>Disclosure in Paper</u>
A multiple-clock-domain microprocessor comprising:	"An approach that allows for aggressive future frequency increases, maintains a synchronous design methodology, and exploits the trend towards making functional blocks more autonomous, is a <u>multiple clock domain</u> (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an <u>MCD microprocessor</u> each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. ... In this Paper, we describe an initial implementation of an MCD microprocessor ..." Ex. 2005, 2 (emphasis added).
a plurality of domains;	"We describe an alternative approach, which we call a Multiple Clock Domain (MCD) processor, in which the chip is divided into <u>several (coarse-grained) clock domains</u> , within which independent voltage and frequency scaling can be performed." Ex. 2005, Abstract (emphasis added).

for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and	"We describe an alternative approach, which we call a Multiple Clock Domain (MCD) processor, in which the chip is divided into several (coarse-grained) clock domains, <u>within which independent voltage and frequency scaling can be performed</u>." PEx. 2005, Abstract (emphasis added). "Figures 8 and 9 both illustrate the value of using <u>different frequencies in different clock domains: by controlling these frequencies independently</u> we can maintain the required frequency in domains that are critical to performance, while aggressively scaling those domains that are less performance-critical." Ex. 2005, 10 (emphasis added).
for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.	"We describe an alternative approach, which we call a Multiple Clock Domain (MCD) processor, in which the chip is divided into several (coarse-grained) clock domains, <u>within which independent voltage and frequency scaling can be performed</u>." Ex. 2005, Abstract (emphasis added). "[B]y <u>scaling frequency and voltage in different domains dynamically and independently</u>, we can achieve an average improvement in energy-delay product of nearly 20%." Ex. 2005, 11 (emphasis added).

Claim 2

<u>Claim Element</u>	<u>Disclosure in Paper</u>
2. The microprocessor of claim 1, wherein each said clock comprises a phase-locked loop,	"The global clock distribution network is greatly simplified, requiring only the distribution of the externally generated clock to <u>the local Phase Lock Loop (PLL) in each domain</u> ." Ex. 2005, 2 (emphasis added).
and wherein the microprocessor further comprises means for receiving an externally generated clock signal and for supplying the externally generated clock signal to each said phase-locked loop.	"The global clock distribution network is greatly simplified, requiring only the <u>distribution of the externally generated clock to the local Phase Lock Loop (PLL) in each domain</u> ." Ex. 2005, 2 (emphasis added).

Claim 3

<u>Claim Element</u>	<u>Disclosure in Paper</u>
3. The microprocessor of claim 1, wherein there are at least four of said domains.	"We propose <u>four clock domains</u> , corresponding to the front end (including L1 instruction cache), integer units, floating point units, and load-store units (including L1 data cache and L2 cache)." Ex. 2005, Abstract (emphasis added).

Claim 4

<u>Claim Element</u>	<u>Disclosure in Paper</u>
4. The microprocessor of claim 1, wherein the microprocessor is programmed to determine a slack in processing in one of the domains and to reduce the clock frequency and the	"Whenever an event in the dependence DAG has two or more incoming arcs, it is possible—in fact likely—that one arc will constitute the critical path and that the others will have “slack”. This slack

voltage in said one of the domains to reduce the slack.	indicates that the previous operation completed earlier than necessary. If all of the outgoing arcs of an event have <u>slack</u>, then we have an opportunity (assuming zero-cost scaling) to save energy by performing the event at a <u>lower frequency and voltage</u>." Ex. 2005, 6 (emphasis added). "In particular, the slack associated with L1 data cache misses often allows our reconfiguration tool to scale the integer and floating point domains without significantly impacting overall performance (due to the fact that the available ILP is not sufficient to completely hide the miss latency), even when the utilization for these domains is high." Ex. 2005, 9.
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Claim 5

<u>Claim Element</u>	<u>Disclosure in Paper</u>
5. The microprocessor of claim 1, further comprising a queue for communication between at least two of the domains.	"The general <u>queue structure that we use for inter-domain communication</u> is shown in Figure 2." Ex. 2005, 3 (emphasis added).

Claim 6

<u>Claim Element</u>	<u>Disclosure in Paper</u>
6. The microprocessor of claim 5, wherein the queue has a Full flag and an Empty flag, and wherein the microprocessor is programmed to prevent a write to the queue when the Full flag is asserted, until the Full flag is	The general queue structure that we use for inter-domain communication is shown in Figure 2. The assertion of the <u>Full flag</u> indicates to the producer that it can <u>no longer write to the queue until the flag is deasserted</u> ..., while the

deasserted; and to prevent a read from the queue when the Empty flag is asserted, until the Empty flag is deasserted.	<u>Empty flag</u> when asserted indicates that there is no valid data for the consumer to read from the queue. The consumer <u>waits until <i>Empty</i> is deasserted before reading again.</u> " Ex. 2005, 3 (emphasis added).
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Claim 7

<u>Claim Element</u>	<u>Disclosure in Paper</u>
7. The microprocessor of claim 6, wherein the queue is implemented as a dual-ported SRAM.	"This concurrency requires a dual-ported SRAM structure where simultaneous read and write cycles are allowed to <i>different</i> SRAM cells." Ex. 2005, 4.

Given the significant overlap between the specification of the '443 Patent and the Paper, as well as explicit support in the Paper for each element recited in the claims, there can be no dispute that the Paper demonstrates conception by providing a full description of the invention. *Scott*, 281 F. 3d 1243, 1247; Ex. 2003, ¶17 ("The microarchitecture design described in the Paper is the same design implemented by the multiple-clock-domain microprocessor described and claimed in the '443 Patent") and ¶24 ("my Co-Inventors and I had conceived of the invention ... before the February 2002 publication of the Paper.")

C. The Simulation Described In The Paper Embodied The Invention In A Tangible Form

After describing in detail the claimed multiple clock domain microarchitecture (including all of the aspects set forth in the claim charts in Section III(B) above), the Paper described a detailed simulation that implemented the multiple clock domain microarchitecture prior to the publication of the Paper in February, 2002. *See*, Ex. 2005, 5-8; Ex. 2003, ¶16 ("The simulation described in the Paper was completed before publication of the Paper in February, 2002"). The simulation described in Paper used the SimpleScalar tool. As explained by Dr. Kaeli:

In 2002, SimpleScalar was a computer simulator that was commonly used by the computer architecture community to evaluate the performance and correctness of new architectural designs. Among other features, the SimpleScalar tool included a performance simulator that implemented the device at the microarchitecture level, including data paths, memory architecture and control units of the computer device. *See*, e.g., Paper at 5 (discussing use of SimpleScalar to implement modified "microarchitecture of the Alpha 21264 microprocessor" where the centralized Register Update Unit was split "into separate reorder buffer (ROB), issue queue, and physical register file structures.") The SimpleScalar tool provided for execution-driven simulations, where the device being implemented ran as an instrumented program on a host. Ex. 2001, ¶41 (emphasis added).

Significantly, "[w]hen the SimpleScalar tool executed the simulation described in the Paper on a host, the host executing the simulation embodied all of the elements of claim 1 in tangible form. The same can be said for each of the other claims in the '443 Patent, namely, that the host executing the simulation embodied

all of the elements of the claim in tangible form." Ex. 2001, ¶42. By embodying all of the elements of the claims in tangible perform, execution of the simulation described in the Paper constituted an actual reduction to practice of the claimed invention by February, 2002. *Scott*, 281 F. 3d 1243, 1247 ("[r]eduction to practice...requires that the invention be embodied in tangible form.")

Moreover, "separate and apart from the host used to implement the device during the simulation, the computer code (standing alone) used to implement the simulation embodied all of the elements of claim 1 (and the other claims of the '443 patent) in tangible form." Ex. 2001, ¶42; *see, e.g., In re Beauregard*, 53 F.3d 1583 (computer program with executable instructions stored in memory (e.g., on a computer disk) is embodied in a tangible form). Thus, the existence of the computer code used to run the simulation provides an independent basis for demonstrating that the invention claimed in the '443 was actually reduced to practice by February 2002.

D. The Simulation Described In The Paper Showed That The Invention Worked For Its Intended Purpose

The Introduction of the Paper described several "potential" advantages of the MCD design, including "lower energy." As explained in the Paper:

Although the inter-domain synchronization increases the number of clock cycles required to run a given application, an MCD microprocessor affords a number of potential advantages over a singly clocked design: ...

- Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain

allows for finer grained dynamic voltage and frequency scaling, and thus lower energy, than can be achieved with single clock, single-core-voltage systems. Ex. 2005, 2 (emphasis added).

As explained in the Paper, the performance results of the simulation demonstrated that the MCD design achieved the advantages that the inventors sought to recognize:

Performance results for applications drawn from standard benchmark suites suggest that the division of the processor into multiple domains incurs an average baseline performance cost of less than 4%. At the same time, by scaling frequency and voltage in different domains dynamically and independently, we can achieve an average improvement in energy-delay product of nearly 20%. By contrast, global voltage scaling to achieve comparable performance degradation in a singly clocked microprocessor achieves an average energy-delay improvement of only 3%. Ex. 2005, 11.

Thus, the simulation proved that the intended purpose of the MCD design—lower energy—had been achieved. In other words, the simulation results proved that the invention worked for its intended purpose. Ex. 2001, ¶43 ("[O]thers working in the field reading the Paper would have understood that the device implemented in the simulation was shown to work for its intended purpose"); *Scott*, 281 F. 3d 1243, 1247 (Fed. Cir. 2002) (reduction to practice requires "that the invention, as conceived, was shown to work for its intended purpose").

In summary, the Paper taken together with the declaration evidence included herewith, establishes that the invention claimed in the '443 Patent was conceived and

actually reduced to practice by the time the Paper was published in February, 2002.

Thus, any reference dated after that time is not prior art.

IV. CLAIMS OF '443 PATENT

The claims of the '443 Patent capture the MCD microprocessor architecture that the inventors designed and implemented. Claim 1 is representative and provides:

A multiple-clock-domain microprocessor comprising:
a plurality of domains;
for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and
for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

V. CLAIM CONSTRUCTION

The claim limitations at issue must be construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). Claim language is not read in isolation. *Phillips*, 415 F.3d at 1315. Rather, the claim language, when read in light of the specification, elucidates the meaning of the claim language.

A. The Specification Limits The Claims To Globally-Asynchronous Systems

When a patentee describes the features of the "present invention," it is well-settled that "this description limits the scope of the invention." *Pacing Techs., LLC*

v. *Garmin Int'l, Inc.*, 778 F.3d 1021 (Fed. Cir. 2015). In this regard, the "Summary of the Invention" of the '443 Patent states the "present invention" uses a globally-asynchronous clocking style:

... the present invention is directed to a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. ... an MCD microprocessor affords a number of potential advantages over a singly clocked design: ...

The independence of each local domain clock implies no global skew requirement... Ex. 1001, 4:13-31 (emphasis added).

Thus, the claim language reciting "for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains," requires that the separate clocks in the plurality of domains be globally-asynchronous. As. Dr. Kaeli explains, the "Patent '443 overcomes earlier limitations of GALS systems by developing novel methods to support using independent clock and independent voltage controls, overcoming issues related to inter-domain synchronization and communication." Ex. 2001, ¶39.

B. The Specification Disparages Systems That Impose Significant Restrictions On The Possible Choices Of Frequencies

The law is clear and well-settled that claims should not be read so broadly as to encompass a prior art structure distinguished or disparaged in the specification. *Indivior Inc. v. Dr. Reddy's Labs*, 752 Fed. Appx. 1024 (Fed. Cir. 2018) (finding that claims did not cover solely using conventional top air drying to produce films because the specification disclaimed such drying by disparaging its use); *SciMed Life Sys. v. Advanced Cardiovascular Sys.*, 242 F.3d 1337 (Fed. Cir. 2001), *citing*, *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1159 (Fed. Cir. 1998) (Specification distinguished prior art as inferior and touted advantages of a conical shaped cup for use in an artificial hip device; “such statements make clear that the '589 patent discloses *only* conical shaped cups and nothing further”); *Ekchian v. Home Depot, Inc.*, 104 F.3d 1299, 1304, 41 U.S.P.Q.2D (BNA) 1364, 1368 (Fed. Cir. 1997) (“Since, by distinguishing the claimed invention over the prior art, an applicant is indicating what the claims do not cover, he is by implication surrendering such protection.”).

As recognized by the Federal Circuit, even “where the language of the claims, read without reference to the specification, might be considered broad enough to encompass a feature, that feature is deemed to be outside the reach of the claims where the specification makes clear that the invention does not include the particular

feature.” *Chi. Bd. Options Exch., Inc. v. Int’l Sec. Exch., LLC*, 677 F.3d 1361 (Fed. Cir. 2012), *citing*, *Honeywell Int’l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1319 (Fed. Cir. 2005) (quoting *SciMed*, 242 F.3d 1337, 1341).

Here, the specification of the '443 Patent disparages prior art synchronization schemes that restrict the relative frequencies of the clocks:

Some synchronization schemes restrict the ... relative frequencies of the clocks, thereby eliminating the need for hardware arbitration [27]. Unfortunately, these schemes impose significant restrictions on the possible choices of frequencies. ... Ex. 1001, 6:32-36 (emphasis added).

The specification explains that Reference [27] is “L. F. G. Sarmenta, G. A. Pratt, and S. A. Ward. Rational Clocking. In Proceedings of the International Conference on Computer Design, Austin, Tex., October 1995.” Ex. 1001 3:54-56. (Ex. 2004) (hereinafter, “Sarmenta”).

Sarmenta describes an “approach [that] maintains a known phase relationship between clocks whose frequencies are related by a rational factor, and exploits the predictability of their relative phases to algorithmically time communications without run-time arbitration contests.” Ex. 2004, Abstract. The “rational factor” refers to the ratio of two small integers (M/N), representing the relationship between the clock frequencies of two clocked digital subsystems. Ex. 2001, ¶36. This rational relationship ensures periodic alignment of the clocks, creating predictable moments when the active edges of both clocks coincide (and are therefore synchronized). Ex. 2001, ¶36. For instance, if one clock operates at

frequency (f_m) and the other at other at (f_n), their frequencies satisfy the relationship ($f_m/f_n = M/N$). This periodic alignment defines a “coincidence cycle,” during which the relative positions of clock edges are synchronized, enabling efficient transfers between subsystems. Ex. 2001, ¶36.

The specification makes clear that Sarmenta is an example of synchronization scheme that imposes "significant restrictions" on the possible choices of frequencies, and clearly disparages and disclaims/disavows these types of restrictive schemes. Ex. 1001, 6:32-36. To overcome the limitations of systems like Sarmenta, the '443 Patent explains that the invention provides “[t]he designers of each domain [to be] no longer constrained by the speeds of critical paths in other domains, affording them greater freedom in each domain to optimize the tradeoffs among clock speed, latency, and the exploitation of application parallelism via complex hardware structures.” Ex. 1001, 6:34-39. As Dr. Kaeli explains, “The ‘443 invention overcomes these limitations, offering independence in clock frequency generation, allowing each frequency domain to adopt their own independent frequency, offering near infinite resolution in terms of the clock frequency selected for each domain.” Ex. 2001, ¶38.

Accordingly, the claims should not be read to cover schemes like Sarmenta’s, where frequencies are related by a “rational factor” that significantly restricts the possible choices of frequencies to those related by the "rational factor." In addition

to being expressly disavowed, such systems are outside of the scope of the "present invention" which is limited to systems that use a globally-asynchronous clocking style (*id.*, Ex. 1001, 4:13-19), because in systems like Sarmeta where the frequencies are related by a "rational factor," there will be a periodic alignment during which the relative positions of clock edges are synchronized. Ex. 2001, ¶37. Thus, the claim language reciting "for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains," does not cover synchronized systems like Sarmenta that maintain global synchronization by restricting the possible choice of frequencies to those related by a "rational factor."

C. The Claims Are Limited To Microprocessors

Claim 1 begins as follows:

*A multiple-clock-domain microprocessor comprising:
a plurality of domains; ...*

The specification makes clear that the "present invention" is directed to a microprocessor. *See*, Ex. 1001, Title ("Multiple Clock Domain Microprocessor"); 4:14-17 (Summary of the Invention) ("the present invention is directed to a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor ..."). Thus,

it is clear that the claims are limited to microprocessors, and that the "plurality of domains" are domains within a microprocessor.

The Petition (at 21) begins its analysis of claim 1 with the statement: "If the preamble is limiting." Based on the statements in the specification that the invention is directed to a microprocessor, the recitation of a multiple-clock-domain microprocessor is limiting and a requirement of the claim.

VI. PRIOR ART RELIED ON IN THE PETITION

A. Shenai

Shenai is the sole reference cited in Ground 1. Shenai, titled "Distributed Power and Supply Architecture," discloses a power management system designed to provide power and clock signals to multiple loads. The system includes a clock distribution controller capable of adjusting voltages, currents, and clock frequencies for the loads, as illustrated in Figure 4. The clock and voltage distribution network supports various clock frequencies derived from a common reference clock, enabling synchronous communication between loads. Ex. 1004, [0036]; Ex 2001, ¶46-49.

B. Georgiou

Georgiou is the sole reference cited in Gound 5. Georgiou, titled "Performance-Temperature Optimization by Cooperatively Varying the Voltage and Frequency of a Circuit," describes a system that uses thermal feedback to adjust

voltage and frequency cooperatively to manage circuit heating while maintaining synchronization. The system employs a master clock divided into dependent clock signals that drive functional units through multiplexers, as illustrated in Figure 4. Synchronization across the circuit is ensured by constraining clock frequencies to fixed fractions of the master clock, enabling efficient thermal and performance optimization. Ex 2001, ¶58-60.

VII. THE PETITION FAILS TO DEMONSTRATE A REASONABLE LIKELIHOOD OF SUCCESS ON THE MERITS

A. Ground 1 Is Deficient

1. Shenai Is Not Prior Art

As explained above, the invention claimed in the '443 Patent was conceived and actually reduced to practice by February, 2002. The Petitioner asserts “Shenai was filed 08/12/2002, published 02/13/2003, and is prior art at least under Section 102(e).” Pet., 9. Accordingly, since the August 12 2002 date asserted by the Petitioner is after February, 2002, Shenai cannot render the claims obvious under 35 U.S.C. §103.

The Petitioner does not allege that the relied upon disclosures Shenai should be afforded an earlier date. In fact, while Shenai claims priority to Provisional Application Nos. 60/311,575, filed August 10, 2001 (Ex. 2006), 60/337,837, filed November 5, 2001 (Ex. 2007), 60/337,479, filed November 5, 2001 (Ex. 2008) and

60/338,510, filed November 5, 2001 (Ex. 2009) (collectively, the Provisional Applications), the passages from Shenai (Ex. 1004) relied on in the Petition are not entitled to the benefit of the filing date of the Provisional Applications because the subject matter was not disclosed in the manner provided by 35 U.S.C. § 112.

“A reference patent is only entitled to claim the benefit of the filing date of its provisional application if the disclosure of the provisional application provides support,” in compliance with § 112 for both the claims in the reference patent and the disclosures from the reference patent relied upon for invalidity. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1382 (Fed. Cir. 2015). In order to satisfy the written description requirement of §112, “one skilled in the art, reading the original disclosure, must immediately discern” the material at issue. *Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1323 (Fed. Cir. 2000) (emphasis added). “[A] description that merely renders the invention obvious does not satisfy the [written description] requirement.” *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1352 (Fed. Cir. 2010) (*en banc*); *see also Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1571-72 (Fed. Cir. 1997).

The Petition does not argue that the portions of Shenai (Ex. 1004) relied on in the Petition are supported by the Provisional Applications, nor does the Petitioner argue that at least one of the claims of Shenai is supported by the Provisional Applications as required under *Dynamic Drinkware*. In fact, it is clear that numerous

portions of Shenai (Ex. 1004) relied on in the Petition are not supported by the Provisional Applications. For example:

- At page 21, the Petition cites Shenai at [0030] and states: “Shenai is directed to the architecture of a microprocessor where ‘certain processing activities of software running on a microprocessor may utilize various subsystems more heavily.’” Ex.-1004, [0030] (emphasis added). However, none of the Provisional Applications mention the implementation of techniques on a “microprocessor.” The quoted passage relied on from [0030] was only introduced into the disclosure when the Shenai utility application was filed.
- At pages 21-22, the Petition cites to Shenai at [0025] and [0028] and states: “Shenai’s loads are ‘components or subsystems of a microprocessor ... [such as] arithmetic logic units (ALU), integer units,” “nonvolatile memory units,” a “floating point unit,” or even an “integer unit.” Id., [0025], [0028] (emphasis added). However, none of the Provisional Applications mention implementation of techniques on a “microprocessor,” “arithmetic logic units,” “integer units,” a “floating point unit,” or an “integer unit.” Again, applications of techniques on these specific units was only introduced into the disclosure when the Shenai utility application was filed.

In short, since material portions of Shenai (Ex. 1004) relied on the Petition are not fully supported under §112, the relied on portions of Shenai (Ex. 1004) are only

entitled to a priority date of August 12, 2002, which is after the invention date of the '443 Patent which occurred by February, 2002. See, Section III, *supra*.

Accordingly, Shenai cannot render the Challenged Claims obvious under 35 U.S.C. §103 because Shenai is not a valid prior art reference.

2. Ground 1 Is Deficient Because Shenai’s Reliance on Rational Frequency Relationships Fails to Teach or Render Obvious the Independent Clock Frequency Generation Required by the Challenged Claims

Unlike the globally-asynchronous system that is the subject of the '443 Patent, both the prior art systems disparaged in the '443 Patent and Shenai utilize rational frequency relationships to achieve synchronization. Ex. 1004, [0036] (noting that the disclosed configurations may “allow for synchronous communication between loads.”) (emphasis added). Specifically, Shenai relies on a “rational factor” relationship, where clock signals are generated as integer or fractional multiples or divisions of a reference clock. Moreover, like prior art systems disparaged in the specification, Shenai imposes significant restrictions on frequency selection—which the '443 Patent disparages. See, Section VI(B), *supra*. Shenai’s disclosures failed to provide the independently dynamic frequency control across clock domains required by the Challenged Claims.

The Federal Circuit has held that “[t]he patentee may demonstrate intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification expressions of manifest exclusion or restriction, representing a

clear disavowal of claim scope." *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012) (Internal Citation Omitted). In the situation where the inventor's intention is to disavow the scope, "the inventor's intention, as expressed in the specification, is regarded as dispositive." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005). For example, "an inventor may disavow claims lacking a particular feature when the specification distinguishes or disparages prior art based on the absence of that feature." *Poly-America, L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136-37 (Fed. Cir. 2016). In the present case, the specification deliberately and unambiguously disavows an embodiment that imposes a "rational factor" requirement on selection of the frequencies.

The '443 Patent states, "[s]ome synchronization schemes restrict the phase relationship and relative frequencies of the clocks, thereby eliminating the need for hardware arbitration [27]." Ex 1001, 6:33-35. In the '443 Patent, citation [27] corresponds to Sarmenta (Ex. 2004). Sarmenta describes an "approach maintains [that] a known phase relationship between clocks whose frequencies are related by a rational factor, and exploits the predictability of their relative phases to algorithmically time communications without run-time arbitration contests." Ex. 2004, Abstract.

The "rational factor" in the Paper refers to the relationship between the clock frequencies of two independently clocked digital subsystems. These frequencies are

related by the ratio of two integers, (M/N) , where (M) and (N) are small integers. This rational relationship ensures that the clocks align periodically, creating predictable points in time where the active edges of both clocks coincide. Ex. 2001, ¶36

For example, in Sarmenta, if one clock operates at a frequency (f_m) and the other at (f_n) , their frequencies satisfy the relationship $(f_m/f_n = M/N)$. This periodic alignment allows the system to define a “coincidence cycle,” during which the relative positions of the clock edges are predictable. This predictability is key to scheduling safe and efficient data transfers between subsystems without introducing run-time synchronization delays or relying on more restrictive synchronous designs that demand integer frequency ratios. Ex. 2001, ¶36.

However, as the ‘443 Patent observes when discussing Sarmenta, “these schemes impose significant restrictions on the possible choices of frequencies.” Ex 1001 6:35-37. To overcome the limitations of systems like Sarmenta, the ‘443 Patent explains that invention provides “[t]he designers of each domain [to be] no longer constrained by the speeds of critical paths in other domains, affording them greater freedom in each domain to optimize the tradeoffs among clock speed, latency, and the exploitation of application parallelism via complex hardware structures.” Ex. 1001 2:34-39. Accordingly, while Sarmenta introduces a synchronization approach leveraging rational frequency relationships, it imposes significant restrictions on

frequency selection, as acknowledged in the ‘443 Patent. Dr. Kaeli explains, “The ‘443 invention overcomes these limitations, offering independence in clock frequency generation, allowing each frequency domain to adopt their own independent frequency, offering near infinite resolution in terms of the clock frequency selected for each domain.” Ex. 2001, ¶36

The Petitioner’s expert “provided an annotated version of Shenai’s Figure 4 below to assist in illustrating the relationship between the clock/shifters and corresponding loads.” Ex. 1002, ¶110 (a copy of the annotated figure is reproduced below).

“for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains”

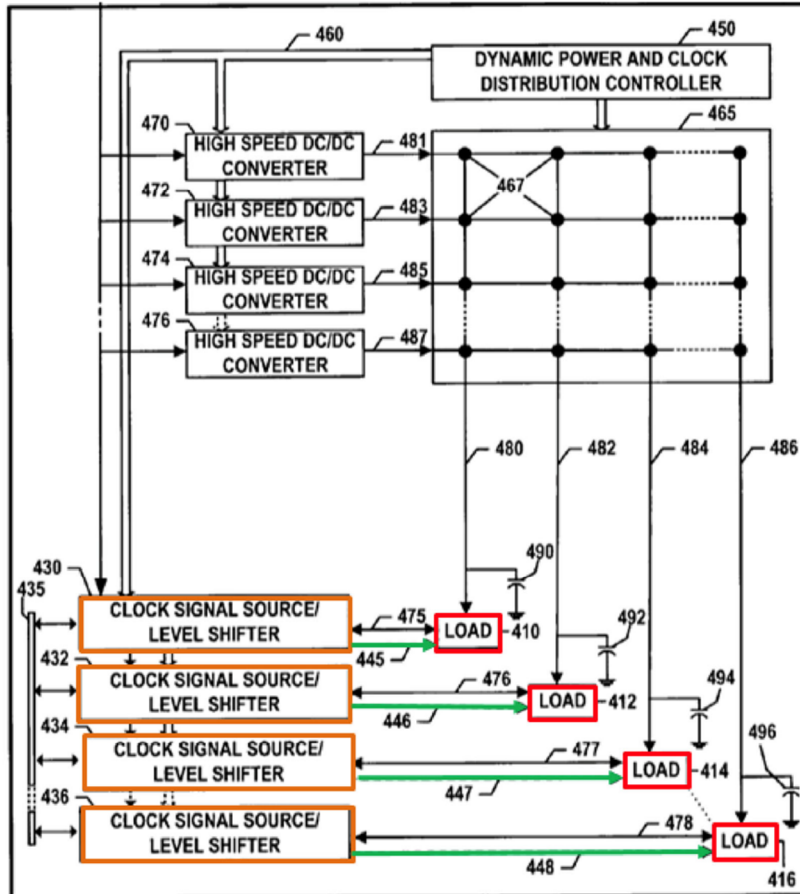


FIGURE 4

Petitioner’s expert further alleged that “[a]s Shenai’s clock/shifter dynamically generates a clock signal for a given load at a frequency based on that load’s respective needs, the clock signal for each load is generated independent of the clock signal for each other load.” Ex. 1002, ¶113.

However, the clocks are not generated independently of the clock signal for each other load. Instead, Shenai relies upon Sarmenta’s “rational factor” for

synchronization. As the Petition observes, Shenai describes, “clock/shifters 430-436 may comprise, phase-locked-loop circuits, delay-locked-loop circuits, or combinational logic circuits that generate clock signals for loads 410-416 by, for example, operating at [sic] at an integer multiplication, a half-integer multiplication or a quarter-integer multiplication of a reference clock signal.” Pet., 28.

Specifically, Par. [0036] of Shenai explains:

[0036] Additionally, clock/shifters 430-436 may comprise, phase-locked-loop circuits, delay-locked-loop circuits, or combinational logic circuits for supplying clock signals to loads 410-416. These circuits may operate **at an integer multiplication, a half-integer multiplication or a quarter-integer multiplication of a reference clock signal.** Controller 450 may provide the reference clock signal, though the invention is not so limited. Alternatively, these circuits may operate **at an integer division, a half-integer division and a quarter-integer division of the reference clock signal.** Such configurations may allow for synchronous communication between loads 410-416, as opposed to asynchronous communication, which may be undesirable.¹

Accordingly, as Dr. Kaeli explains, “[t]he clock frequency control described in Shenai generates a clock frequency that is based on a rational multiple of a reference clock signal.” Ex. 2001, ¶64. Therefore, like in Sarmenta, there is a “rational factor” relationship in Shenai between the clock signal provided to each of the loads that ensures that the clocks align periodically, creating predictable points

¹ Shenai's characterization of systems requiring asynchronous communications as "undesirable" would not motivate a POSITA to implement a globally-asynchronous architecture as required by the Challenged Claims. Ex. 2001, ¶47.

in time where the active edges of both clocks coincide. See, Ex. 1004, [0036] (noting that the disclosed configurations may “allow for synchronous communication between loads.”) (emphasis added). This approach fundamentally contradicts the independence in frequency generation required by the challenged claims. The ‘443 Patent explicitly identifies these limitations and emphasizes that the claimed invention overcomes them by enabling the dynamic and independent generation of clock signals for each domain, unconstrained by the frequencies of other domains. Ex. 1001, 6:34-39 (the invention provides “[t]he designers of each domain [to be] no longer constrained by the speeds of critical paths in other domains, affording them greater freedom in each domain to optimize the tradeoffs among clock speed, latency, and the exploitation of application parallelism via complex hardware structures.”). This freedom is critical to achieving the design flexibility and performance optimization described in the ‘443 Patent. Ex. 2001, ¶39 (“The ‘443 invention overcomes these limitations, offering independence in clock frequency generation, allowing each frequency domain to adopt their own independent frequency, offering near infinite resolution in terms of the clock frequency selected for each domain.”).

As such, the Petitioner has not demonstrated that Shenai discloses or renders obvious the claimed feature of “separately generating a clock signal...the frequency being dynamically changeable independently of the frequencies of the clock signals

generated for others of the plurality of domains.” Therefore, the Petitioner has failed to meet its burden of proving obviousness for the challenged claims under Ground 1.

B. Ground 2 Is Deficient Because Halepete Does Not Cure the Shortcomings of Shenai

The Petition does not allege, nor does Halepete teach, “separately generating a clock signal...the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” as recited in the independent Challenged Claims. Accordingly, the Petitioner has failed to meet its burden with regard to Ground 2 for at least the reasons discussed with regard to Ground 1 above.

C. Ground 3 Is Deficient Because Sherburne Does Not Cure the Shortcomings of Shenai

The Petition does not allege, nor does Sherburne teach, “separately generating a clock signal...the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” as recited in the independent Challenged Claims. Accordingly, the Petitioner has failed to meet its burden with regard to Ground 3 for at least the reasons discussed with regard to Ground 1 above.

D. Ground 4 Is Deficient Because Traylor Does Not Cure the Shortcomings of Sherburne and Shenai

The Petition does not allege, nor does Traylor teach, “separately generating a clock signal...the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” as recited in the independent Challenged Claims. Accordingly, the Petitioner has failed to meet its burden with regard to Ground 4 for at least the reasons discussed with regard to Ground 1 above.

E. Ground 5 Is Deficient Because Georgiou’s “Rational Factor” Relationship Fails to Disclose or Render Obvious the Claimed Independent and Dynamically Changeable Clock Frequencies

Georgiou (Ex. 1008) does not disclose the claimed feature of “separately generating a clock signal...the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains.” Similar to Shenai, Georgiou explicitly relies on a “rational factor” relationship, wherein clock signals are generated as integer or fractional multiples or divisions of a reference clock. As Dr. Kaeli explains “[a] POSITA would understand the clocking structure taught by Georgiou would lack the flexibility and precision of the independent clocks that are taught in the ‘443 patent.” Ex. 2001, ¶78. Therefore, the Petitioner has failed to demonstrate that Shenai renders the challenged claims obvious under Ground 5.

The Petition states, “[i]n Georgiou’s Figure 4, it can be seen that clock dividers can manipulate the master clock frequency by an integer value, such as divide-by-2 or divide-by-n.” Pet., 69. As shown in the Petitioner’s annotated version of Figure 4 (reproduced below), the clock divider provides the functional unit with an integer fraction of the master clock.

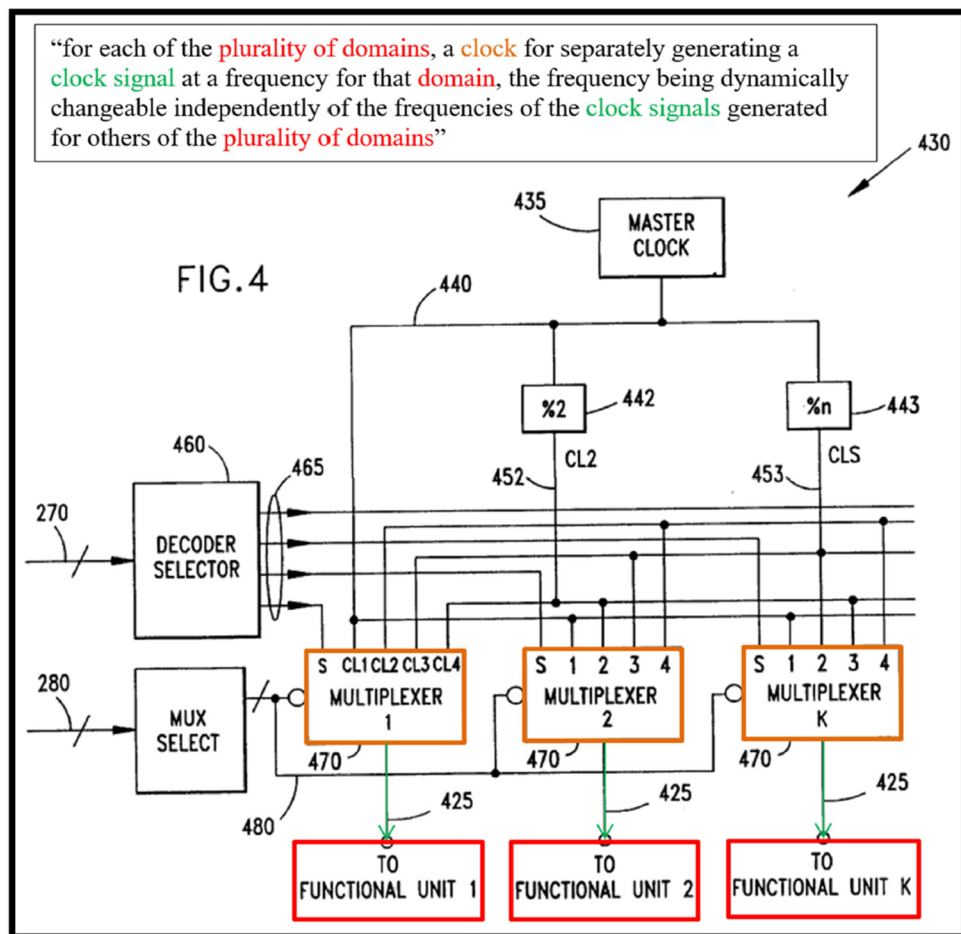


Figure 4 of *Georgiou*

Accordingly, Georgiou teaches a system that operates a given functional unit at M integers (e.g., 2) of the master clock and another at N integers (e.g., N) of the

master clock. Therefore, Georgiou teaches a system that requires the same “rational factor” as Sarmenta and, thus, like Sarmenta, “impose[s] significant restrictions on the possible choices of frequencies.” Ex 1001, 6:35-37.

Accordingly, the arguments and evidence presented by Petitioner fail to establish that Georgiou discloses or renders obvious the claimed feature of “separately generating a clock signal...the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains.” Georgiou, like Shenai and Sarmenta, relies on a “rational factor” relationship, wherein clock signals are generated as integer or fractional multiples or divisions of a master clock. This approach inherently imposes significant restrictions on frequency selection, ensuring periodic alignment of clock edges but failing to provide the independence required by the Challenged Claims.

Accordingly, the Petitioner has not met its burden of demonstrating that Georgiou renders the challenged claims obvious under Ground 5.

F. Ground 6 Is Deficient Because Halepete Does Not Cure the Shortcomings of Georgiou.

The Petition does not allege, nor does Halepete teach, “separately generating a clock signal...the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” as recited in the independent Challenged Claims. Accordingly, the Petitioner has failed

to meet its burden with regard to Ground 6 for at least the reasons discussed with regard to Ground 5 above.

G. Ground 7 Is Deficient Because Kranich Does Not Cure the Shortcomings of Georgiou.

The Petition does not allege, nor does Kranich teach, “separately generating a clock signal...the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” as recited in the independent Challenged Claims. Accordingly, the Petitioner has failed to meet its burden with regard to Ground 7 for at least the reasons discussed with regard to Ground 5 above.

VIII. SUMMARY OF ARGUMENTS ON THE MERITS

The Petition falls well short of demonstrating a reasonable likelihood of success in establishing the invalidity of the Challenged Claims. Each Ground advanced by the Petitioner suffers from critical deficiencies, including reliance on inapplicable or insufficiently supported prior art, mischaracterizations of the references, and a failure to address key technical distinctions and legal requirements. The Petitioner has not provided persuasive evidence to overcome the invention's demonstrated novelty and non-obviousness. For these reasons, the Board should find that the Petitioner has not met its burden on the merits, and the institution of the IPR should be denied.

IX. Conclusion

For the above reasons, Patent Owner respectfully requests that the Board deny institution of the Petition.

Respectfully submitted,

Dated: November 19, 2024

By: /Brandon R. Theiss/
Brandon R. Theiss
Registration No. 70,507
Counsel for Patent Owner
University of Rochester
(Intellectual Ventures I LLC)

CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Patent Owner Preliminary Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 8,101 words, excluding the parts of this Patent Owner's Preliminary Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Preliminary Response.

Respectfully submitted,

Dated: November 19, 2024

By: /Brandon R. Theiss/
Brandon R. Theiss
Registration No. 70,507
Counsel for Patent Owner
University of Rochester
(Intellectual Ventures I LLC)

CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a copy of the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** was served via email (as consented to by counsel) on November 19, 2024 to lead and backup counsel of record for Petitioners as follows:

Dinesh Melwani
dmelwani@bomcip.com

Ankit Aggarwal
aaggarwal@bomcip.com

William Uhr
wuhr@bomcip.com

Bookoff McAndrews, PLLC
2000 Pennsylvania Avenue NW
Suite 4001
Washington, D.C. 20006
Service email: docketing@bomcip.com

Dated: November 19, 2024

By: /Brandon R. Theiss/
Brandon R. Theiss
Registration No. 70,507
Counsel for Patent Owner
University of Rochester
(Intellectual Ventures I LLC)