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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Krishna	Shenai	Naperville, Illinois

☐ Additional inventors are being named on the _____ separately numbered sheets attached hereto**TITLE OF THE INVENTION (280 characters max)**

Dynamic Power and Performance Management Architecture

Direct all correspondence to:

CORRESPONDENCE ADDRESS☐ Customer Number Place Customer Number
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ENCLOSED APPLICATION PARTS (check all that apply)

☒ Specification	Number of Pages	10	☐ CD(s), Number	
☒ Drawing(s)	Number of Sheets	5	☒ Other (specify)	
☒ Application Data Sheet. See 37 CFR 1.76				

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☒ Applicant claims small entity status. See 37 CFR 1.27.	FILING FEE AMOUNT (\$) \$75.00
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Respectfully submitted,

SIGNATURE

Date

08-10-01

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REGISTRATION NO.

34,137

(if appropriate)

Docket Number:

6455-83476

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Application Number	
Filing Date	concurrently herewith
First Named Inventor	Krishna SHENAI
Examiner Name	
Group/Art Unit	
Attorney Docket Number	6455-83476

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Small Entity

Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	75.00

SUBTOTAL (1)

(\$ 75.00

2. EXTRA CLAIM FEES

	Extra Claims	Fee from below	Fee Paid
Total Claims	-20**=	x	=
Independent Claims	-3**=	x	=
Multiple Dependent Claims		=	

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Large Entity Small Entity

Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2)

(\$

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FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Small Entity

Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description	Fee Paid
105	130	205	65	Surcharge-late filing fee or oath	
127	50	227	25	Surcharge-late provisional filing fee or cover sheet	
139	130	139	130	Non-English Specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a Brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify)

SUBTOTAL (3)

(\$

*Reduced by Basic Filing Fee Paid

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Signature

Date

August 10, 2001

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Application Data Sheet

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Application Information

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Title Line Two:: Management Architecture
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Formal Drawings?: No
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Docket Number:: 6455-83476

Representative Information

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Registration Number Five::	25,060
Registration Number Six::	22,053
Registration Number Seven::	27,466
Registration Number Eight::	29,434
Registration Number Nine::	29,054
Registration Number Ten::	29,381
Registration Number Eleven::	34,044
Registration Number Twelve::	27,600
Registration Number Thirteen::	34,137
Registration Number Fourteen::	39,724
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Registration Number Sixteen::	37,135
Registration Number Seventeen::	40,604
Registration Number Eighteen::	37,435

Dynamic Power and Performance Management Architecture (CS65)

[23 claims]

References Cited

U.S. PATENT DOCUMENTS

5,485,127	1/1996	Bertoluzzi et al
5,548,763	8/1996	Combs et al
5,586,308	12/1996	Hawkins et al
5,586,332	12/1996	Jain et al
5,628,020	5/1997	O'Brien
5,630,143	5/1997	Maher et al
5,630,148	5/1997	Norris
5,632,037	5/1997	Maher et al
5,646,572	7/1997	Masleid
5,696,953	12/1997	Wong et al
5,724,249	3/1998	Kodali et al
5,727,193	3/1998	Takeuchi
5,729,720	3/1998	Kau et al
5,754,436	5/1998	Walsh et al
5,768,602	6/1998	Dhuey
5,771,373	6/1998	Kau et al
5,799,198	8/1998	Fung
5,845,138	12/1998	Nowlin, Jr.
5,894,579	3/1999	Fujihara
5,905,901	5/1999	Klein
5,910,930	6/1999	Dieffenderfer et al
5,913,067	6/1999	Klein
5,954,820	9/1999	Hetzler
5,958,058	9/1999	Barrus
5,959,439	9/1999	Shenai et al
5,974,557	10/1999	Thomas et al
5,978,923	11/1999	Kou
5,983,357	11/1999	Sun
5,987,244	11/1999	Kau et al
5,987,614	11/1999	Mitchell et al
5,996,084	11/1999	Watts
6,000,035	12/1999	Matsushima et al
6,016,071	1/2000	Shay
6,065,122	5/2000	Wunderlich et al
6,065,124	5/2000	Lee
6,105,139	8/2000	Dey et al
6,105,142	8/2000	Goff et al

6,115,823	9/2000	Velasco et al
6,128,745	10/2000	Anderson et al
6,151,681	11/2000	Roden et al
6,158,012	12/2000	Watts, Jr.
6,163,845	12/2000	Zhao et al
6,167,330	12/2000	Linderman
6,182,232	1/2001	Klein
6,192,479	2/2001	Ko
6,195,755	2/2001	Webster et al
6,212,645	3/2001	Tjandrasuwita
6,260,149	7/2001	Baweja

OTHER PUBLICATIONS

- L. Casey et al, "CMOS drive and control circuitry for 1–10 MHz power conversion," *IEEE Trans. Power Electronic.*, vol. 6, no. 4, pp. 749-758, 1991.
- J. Titus et al, "Characterization of a fully resonant, 1-MHz, 25-W DC/DC converter fabricated in a rad-hard BiCMOS/high-voltage process," *IEEE Trans. Nucl. Sci.*, vol. 42, no. 6 Part I, pp. 2143-2149, 1995.
- D. Maksimovic and B. Arbetter, "Feedforward pulse-width modulator for boost DC-DC power converters," *Electron. Lett.*, vol. 31, no. 7, pp. 513-514, 1995.
- S. Reynolds, "A DC-DC converter for short-channel CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 32, no. 1, pp. 111-113, 1997.
- J.-M. Chang and M. Pedram, "Energy minimization using multiple supply voltages," *IEEE Trans. VLSI Syst.*, vol. 5, no. 4, pp. 436-443, 1997.
- T. Kuroda et al, "Variable supply-voltage scheme for low-power high-speed CMOS digital design," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 454-462, 1998.
- M. Takahashi et al, "A 60-mW MPEG4 video codec using clustered voltage scaling with variable supply-voltage scheme," *IEEE J. Solid-State Circuits*, vol. 33, no. 11, pp. 1772-1780, 1998.
- J. Goodman et al, "An energy/security scalable encryption processor using an embedded variable voltage DC/DC converter," *IEEE J. Solid-State Circuits*, vol. 33, no. 11, pp. 1799-1809, 1998.
- S. Raje and M. Sarrafzadeh, "Scheduling with multiple voltages under resource constraints," in *Proc. IEEE Int. Conf. Circuits Systems (ISCAS)*, 1999, pp. 350-353.
- G.-Y. Wei and M. Horowitz, "A fully digital, energy-efficient, adaptive power-supply regulator," *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 520-528, 1999.
- E. McShane and K. Shenai, "Monolithic DC power supplies for wireless telecommunications and multimedia systems," in *Proc. IEEE Int. Telecommunications Energy Conf. (INTELEC)*, 2000, pp. 733-740.
- T. Kuroda and M. Hamada, "Low-power CMOS digital design with dual embedded adaptive power supplies," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 652-655, 2000.
- T. Burd et al, "A dynamic voltage scaled microprocessor system," *IEEE J. Solid-State Circuits*, vol. 35, no. 11, pp. 1571-1580, 2000.
- G.-Y. Wei et al, "A variable-frequency parallel I/O interface with adaptive power-supply regulation," *IEEE J. Solid-State Circuits*, vol. 35, no. 11, pp. 1600-1610, 2000.

E. McShane and K. Shenai, "A CMOS monolithic 5-MHz, 5-V, 250-mA, 56% efficiency DC/DC switch-mode boost converter with dynamic PWM for embedded power management," to be presented at *IEEE Industry Applications Society (IAS) Ann. Mtg.*, 2001.

ABSTRACT

A dynamic power and performance management architecture which is comprised of five subsystems. First is a collection of m clusters of subsystems to be managed, also referred to as load clusters, each serviced by an independent clock generator. Second is a collection of n high-speed DC/DC voltage converters, also referred to as power sources. Third is a cross-bridge network which permits arbitrary connections between the power sources and loads. Fourth is a controller circuit which dynamically specifies the connections to be made by the cross-bridge network between the power sources and loads. Fifth is voltage level-shifting logic and latches associated with inter-cluster signals. The significance of the architecture is its ability to exploit high-frequency DC/DC voltage converters to dynamically and rapidly adjust the supply voltage of each subsystem cluster in conjunction with frequency scaling such that the power consumed by each subsystem cluster is minimized in response to time-varying performance levels.

FIELD OF THE INVENTION

The field of the invention is power management circuits and technology and in particular dynamic and adaptive power minimization.

BACKGROUND OF THE INVENTION

Power minimization is recognized as a primary objective in the design of most electronics systems but most especially in systems which are portable, battery-operated, or otherwise especially sensitive to power efficiency in terms of size, weight, operating lifetime, or cost. Although power consumption can be reduced arbitrarily by limiting the system performance (as measured by clock frequency or number of operations performed in unit time), this is an undesirable method. The unsuitability of performance limitations to ensure power efficiency is emphasized by emerging applications (e.g. enhanced wireless telecommunications protocols, streaming multimedia, etc) which require higher performance.

Historically, power minimization has been accomplished by technology scaling—that is reducing the dimensions of transistors and their supply voltage. This technique is now producing diminishing returns for two reasons. Firstly, system power is related to capacitance, voltage, and frequency by $P = CV^2f$. A reduction in supply voltage from 5 V to 1.5 V leads to dramatically lower power; further reduction to 1.25 V or 1 V produces considerably less power savings. Secondly, semiconductor chips and electronic systems have become extremely complex and also may contain replicated components; the growing power consumption of these complex systems is outpacing the incremental improvements to power efficiency offered by technology scaling.

A more recent approach to minimizing power consumption is to disable any logic gates that are idle during the execution of an operation. The disabling is typically accomplished either by halting the clock signal to the gates or by removing the power source to the gates. This technique can be applied at the chip- or system-level. Although effective, this method is simply a binary on-off control of power and performance. It provides no mechanism for a continual tuning between peak performance and minimum power.

A recent approach which balances performance (as measured by clock frequency) and power consumption is simple frequency scaling. This approach yields roughly linear scaling in performance and power. However, in terms of power it is nonoptimal since the propagation delay of logic gates is proportional to C/V^2 . If frequency is simply reduced then the internal logic gates are much faster than is necessary. It is more optimal to also reduce the supply voltage. Related techniques such as clock cycle skipping or inserting sleep cycles into a steady instruction stream do reduce both the average clock frequency and the average power consumption, but these methods as above are binary on-off control. Rather than alternating between off and fully-on states, it is more power efficient to operate continuously at a lower clock frequency and a lower supply voltage.

Performance/power management to date has been accomplished using combined voltage and frequency scaling. To further improve the optimization, semiconductor chips and electronic systems have also been divided into partitions with individual voltage scaling per partition. In most implementations, the scaling is nearly static (quasi-static) such that a clock frequency is almost constant and the supply voltage is automatically reduced to an optimally low potential. More recently (Burd, *IEEE J. Solid-State Circuits*, 2000), the scaling has been performed dynamically at a rate of approximately 15 kHz. Both the quasi-static and dynamic methods rely on the conventional system configuration in which the power source has a low switching rate (less than 1 MHz) and utilizes large reactive components ($>1 \mu\text{F}$ and $>1 \mu\text{H}$).

When the activity levels (and hence the required clock frequency) of the load clusters are nearly constant, both methods yield good improvement to power efficiency. Further improvement is possible however if more clusters are produced since the balance of performance versus power can be made more precisely. When the activity levels (and hence the required clock frequency) of the load clusters are changing rapidly, however, state-of-the-art quasi-static and dynamic frequency-voltage scaling methods do very poorly in minimizing the instantaneous power consumption.

Extremely rapid frequency-voltage scaling can be accomplished by the present invention, which utilizes fully high-frequency power sources. As mentioned previously, state-of-the-art power sources are slow-switching and hence require large reactive components. Technology exists, however, to achieve very high-speed switching ($>150 \text{ MHz}$) power sources (as in U.S. Patent #5,959,439), which can consequently utilize very small-valued reactive components ($<100 \text{ nF}$ and $<100 \text{ nH}$). Using a high-speed switching power source it is possible to employ very small external (discrete) reactive components or even to integrate the reactive components monolithically with the power source. State-of-the-art technology exists which can permit small-valued reactive components with characteristics comparable to those achieved with high-quality discrete parts. By switching at a very high rate it is possible to tune performance/power with very good temporal resolution; by achieving a compact monolithic implementation it is possible to support tuning of multiple load clusters with good spatial resolution.

The unique capability of the present invention is its management of the performance and power consumption of integrated or distributed load clusters using high-frequency power converters and dynamic mapping of power sources to load clusters. Each load cluster can comprise any degree of complexity ranging from a single logic gate, to IC subsystems, to an entire IC, up to an entire electronics system consisting of a multiplicity of components and chips.

A brief review of prior art power and performance management techniques follows.

Localized clock gating or power source gating is limited to binary on-off control. It does not permit a continuous tuning of performance and power characteristics. Software-based progressive sleep modes can be viewed as an extension of clock gating or power source gating.

Frequency scaling, which is generally universally applied to a complex system, does permit a continuous tuning of performance and power characteristics. However, its power efficiency is still poor without also applying voltage scaling. Moreover, applied universally the technique fails to exploit fine-grained performance and power tuning of possible using small load clusters.

Reported techniques for combined frequency and voltage scaling improve power efficiency under quasi-static conditions, but have poor power optimization under dynamic load activity. This limitation is fundamentally caused by the low switching frequency of the power source and the use of only one or two load clusters.

SUMMARY

A dynamic power and performance management architecture which is comprised of five subsystems. First is a collection of m clusters of subsystems to be managed, also referred to as load clusters, each serviced by an independent clock generator. Second is a collection of n high-speed DC/DC voltage converters, also referred to as power sources. Third is a cross-bridge network which permits arbitrary connections between the power sources and loads. Fourth is a controller circuit which dynamically specifies the connections to be made by the cross-bridge network between the power sources and loads. Fifth is voltage level-shifting logic and latches associated with inter-cluster signals. The significance of the architecture is its ability to exploit high-frequency DC/DC voltage converters to dynamically and rapidly adjust the supply voltage of each subsystem cluster in conjunction with frequency scaling such that the power consumed by each subsystem cluster is minimized in response to time-varying performance levels.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features, and advantages of the present invention will become more apparent from the following detailed description taken with the accompanying drawings in which:

FIG. 1 is an illustration of normalized power consumption of a digital circuit versus its normalized clock frequency considering frequency scaling and combined frequency-voltage scaling;

FIG. 2 is a schematic view of a dynamic power and performance management architecture in accordance with an embodiment of the invention;

FIG. 3 is a schematic view of a conventional quasi-static frequency-scaling architecture;

FIG. 4 is a schematic view of a conventional quasi-static combined frequency-voltage scaling architecture; and

FIG. 5 is a schematic view of a conventional dynamic slow combined frequency-voltage scaling architecture.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a comparison of the power consumption of a digital logic gate at a given clock frequency when using either frequency scaling or combined frequency-voltage scaling. Clearly combined frequency-voltage scaling is more optimal. If the clock frequency of a particular load cluster varies rapidly then optimal power efficiency is achieved only if the supply voltage can be varied just as rapidly; this motivates the need for high-speed power sources. If many load clusters exist then a precise tuning of performance versus power within the processor is possible; this motivates the need for multiple load clusters.

FIG. 2 is a schematic diagram of the dynamic performance and power management architecture in accordance with an embodiment of the invention. It is contemplated that each power source could be implemented in one of several fashions. First, it could be integrated monolithically along with the load clusters using existing integrated circuit (IC) fabrication techniques (e.g. CMOS, BiCMOS, etc.). Second, it could be fashioned as an independent IC that is integrated with a load cluster in a compound package such as a multi-chip module (MCM). Third, it could be fashioned as an independent IC that is integrated with a load cluster on a conventional printed circuit board (PCB). The power source also can employ a variety of manifestations of the reactive components. First, the reactive components can be integrated monolithically with the power source. Second, the reactive components can be fashioned as an independent chip that is integrated with the converter in an MCM. Third, conventional discrete components can be used. It is envisioned that each power source will operate at a switching frequency of 1 to 500 MHz and utilize reactive components with values of 1 nF to 10 μ F and 1 nH to 10 μ H.

The architecture is constructed such that a system (e.g. a complex IC or an electronics system) is partitioned into m load clusters. Each load cluster receives an independent clock frequency from a unique clock generator. The clock generator may be implemented by any method known to the art (e.g. a phase-locked loop). It is envisioned that all clock generators will utilize multiplication/division from a single master clock frequency on an integer, half-integer, or quarter-integer basis as is known to the art. The use of a single master clock frequency facilitates synchronization of logic signals between load clusters.

The supply voltages generated by the n power sources are connected to the m load clusters through a cross-bridge network. The cross-bridge network may be implemented by any method known to the art (e.g. analog transistor switches). To stabilize the supply voltage delivered to each load cluster, each load cluster is supported by a local charge-buffering capacitor C . Additionally, logic signals which propagate between clusters are propagated through

dedicated voltage level-shifting latches. The latches ensure that all communications conducted on the logic bus have consistent noise margins.

Finally, to control the cross-bridge network, to specify dynamically the voltage output by each of n power sources, and to specify the clock frequency delivered to each of m load clusters, a dynamic controller is provided. It is envisioned that the dynamic controller will operate with the cooperation of scheduling software, operating system prioritization, or dynamic performance and power optimization algorithms as known to the art.

It is envisioned that under quasi-static load cluster activity conditions, the present invention will reduce load cluster power dissipation to 10% to 50% of that delivered by the present state-of-the-art.

It is envisioned that under dynamic load cluster activity conditions, the present invention will reduce load cluster power dissipation to 10% to 50% of that delivered by the present state-of-the-art.

Five significant features of the architecture of the present invention are noted.

First, the architecture permits combined frequency and voltage scaling with very fine spatial and temporal resolution.

Second, the architecture accommodates a variety of mapping algorithms and strategies in the cross-bridge network between the power sources and the load clusters to permit optimization of power, control complexity, or size.

Third, the architecture accommodates both static and dynamic mapping algorithms and strategies in the cross-bridge network between the power sources and the load clusters to permit optimization of power, control complexity, or size.

Fourth, the architecture complements state-of-the-art techniques for power scheduling, instruction reordering, and progressive sleep modes. The architecture also provides additional sophistication to each of the aforementioned techniques.

Fifth, the architecture is generic and scalable in application to systems of arbitrary complexity. Therefore a managed load cluster could be a single logic gate, an IC subsystem, an entire IC, up to an entire electronics system consisting of a multiplicity of components and chips.

The architecture of the present invention is next contrasted with similar prior art as shown in FIGS. 3, 4, and 5.

FIG. 3 is a conventional quasi-static frequency-scaling architecture. Its use of only a single load cluster creates poor spatial resolution of performance and power tuning. Its use of quasi-static frequency scaling creates poor temporal resolution of performance and power tuning. Finally, its omission of voltage scaling creates very nonoptimal power efficiency.

FIG. 4 is a conventional quasi-static combined frequency-voltage scaling architecture. Its use of only one or two load clusters results in improved, but still poor, spatial resolution of performance and power tuning. Its use of quasi-static frequency-voltage scaling creates poor temporal resolution of performance and power tuning.

FIG. 5 is a conventional dynamic slow combined frequency-voltage scaling architecture. Its use of only a single load cluster creates poor spatial resolution of performance and power tuning. Its use of dynamic frequency-voltage scaling results in improved, but still poor, temporal resolution of performance and power tuning.

CLAIMS

What is claimed is:

1. A generic dynamic performance and power management architecture for performing rapid adjustments of both supply voltage and clock frequency, said architecture comprising:

up to m partitions of independent load clusters to be managed;

up to n power sources;

an n by m cross-bridge network to connect dynamically the n power sources to the m load clusters in response to control signals; and

a control circuit to generate and deliver the control signals to the cross-bridge network as necessary to perform dynamic mapping of the n power sources to the m load clusters.

2. The architecture as claimed in claim 1, wherein up to m clock generators are included to specify and deliver the clock signal of each load cluster.

3. The architecture as claimed in claims 1 and 2, wherein up to m charge-buffering capacitors are included to stabilize the supply voltage of each load cluster.

4. The architecture as claimed in claims 1, 2, and 3, wherein up to m level-shifting latches are included to ensure consistent logic noise margins and proper synchronization of all inter-cluster signals produced by each load cluster.

5. The architecture as claimed in claims 1, 2, 3, and 4, wherein a clock generator delivers an integer, half-integer, or quarter-integer multiplication or division of a reference clock signal input using a phase-locked loop implementation.

6. The architecture as claimed in claims 1, 2, 3, and 4, wherein a clock generator delivers an integer, half-integer, or quarter-integer multiplication or division of a reference clock signal input using a delay-locked loop implementation.

7. The architecture as claimed in claims 1, 2, 3, and 4, wherein a clock generator delivers an integer, half-integer, or quarter-integer multiplication or division of a reference clock signal input using simple combinational logic.

8. The architecture as claimed in claims 1, 2, 3, and 4, wherein a clock generator delivers an integer, half-integer, or quarter-integer division of a reference clock signal input using simple combinational logic.

9. The architecture as claimed in claims 1, 2, 3, and 4, wherein a power source delivers a regulated output side voltage from a single input side voltage in response to a control signal using a switch-mode inductor-based step-up converter as is known to the art.

10. The architecture as claimed in claims 1, 2, 3, and 4, wherein a power source delivers a regulated output side voltage from a single input side voltage in response to a control signal using a switch-mode inductor-based step-down converter as is known to the art.

11. The architecture as claimed in claims 1, 2, 3, and 4, wherein a power source delivers a regulated output side voltage from a single input side voltage in response to a control signal using a switch-mode inductor-based combined step-up/step-down converter as is known to the art.

12. The architecture as claimed in claims 1, 2, 3, and 4, wherein a power source delivers a regulated output side voltage from a single input side voltage in response to a control signal using a switch-mode charge-pump converter as is known to the art.

13. The architecture as claimed in claims 1, 2, 3, and 4, wherein a power source delivers a regulated output side voltage from a single input side voltage in response to a control signal using a switch-mode switched-capacitor converter as is known to the art.

14. The architecture as claimed in claims 1, 2, 3, and 4, wherein the control circuit is implemented only in electronic hardware.

15. The architecture as claimed in claims 1, 2, 3, and 4, wherein the control circuit is implemented in electronic hardware and cooperates and coordinates with software control (e.g. power scheduling, instruction reordering, and progressive sleep modes).

16. A method of controlling the mapping of power sources to load clusters using the architecture as claimed in claims 1, 2, 3, and 4, wherein the mapping is performed once (is static).

17. A method of controlling the mapping of power sources to load clusters using the architecture as claimed in claims 1, 2, 3, and 4, wherein the mapping is performed continually (is dynamic).

18. A method of controlling the mapping of power sources to load clusters using the architecture as claimed in claims 1, 2, 3, and 4, wherein the mapping is performed such that each power source services an approximately equal number of load clusters.

19. A method of controlling the mapping of power sources to load clusters using the architecture as claimed in claims 1, 2, 3, and 4, wherein the mapping is performed such that each power source services load clusters with approximately equal clock frequency.

20. A method of controlling the mapping of power sources to load clusters using the architecture as claimed in claims 1, 2, 3, and 4, wherein the mapping is performed such that each power source delivers an approximately equal average power.

21. A method of tuning the supply voltage applied to a load cluster using the architecture as claimed in claims 1, 2, 3, and 4, wherein the supply voltage is controlled to adjust the performance and/or power dissipation of the load cluster.

22. A method of tuning the clock frequency applied to a load cluster using the architecture as claimed in claims 1, 2, 3, and 4, wherein the clock frequency is controlled to adjust the performance and/or power dissipation of the load cluster.

23. A method of tuning the supply voltage and clock frequency applied to a load cluster using the architecture as claimed in claims 1, 2, 3, and 4, wherein the supply voltage and the clock frequency is controlled to adjust the performance and/or power dissipation of the load cluster.

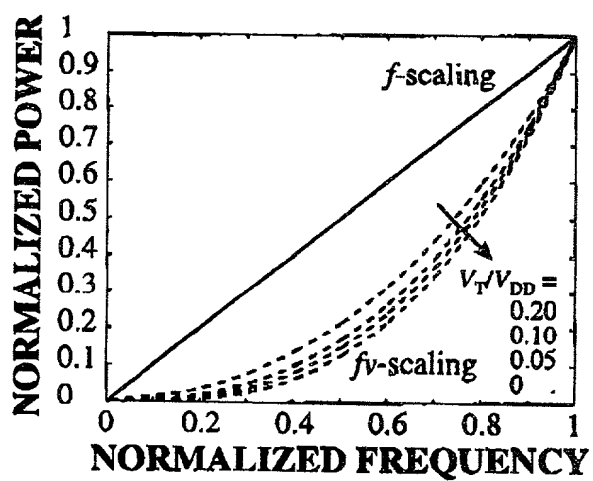


FIGURE 1

CS 65



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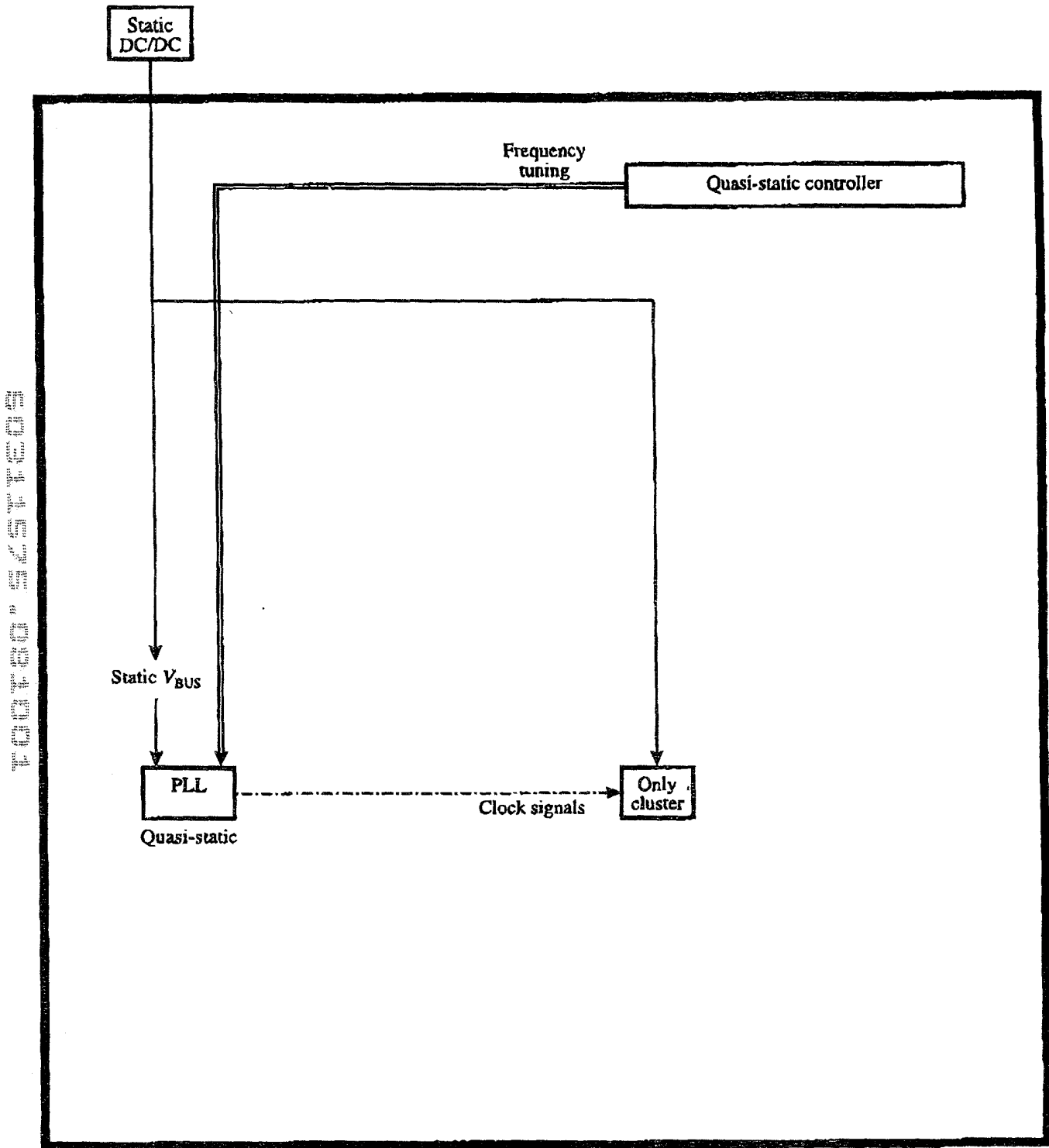


FIGURE 3

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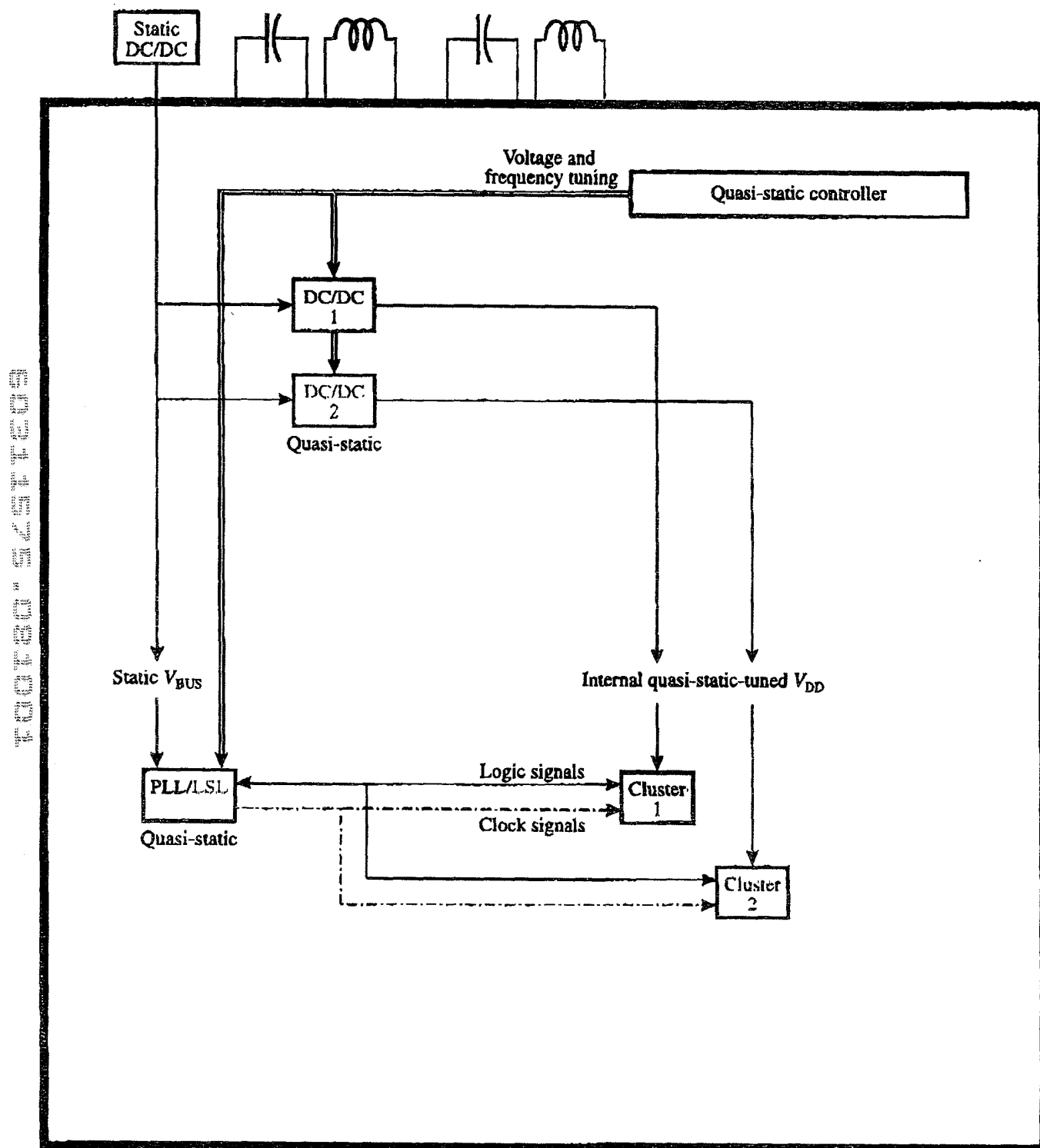
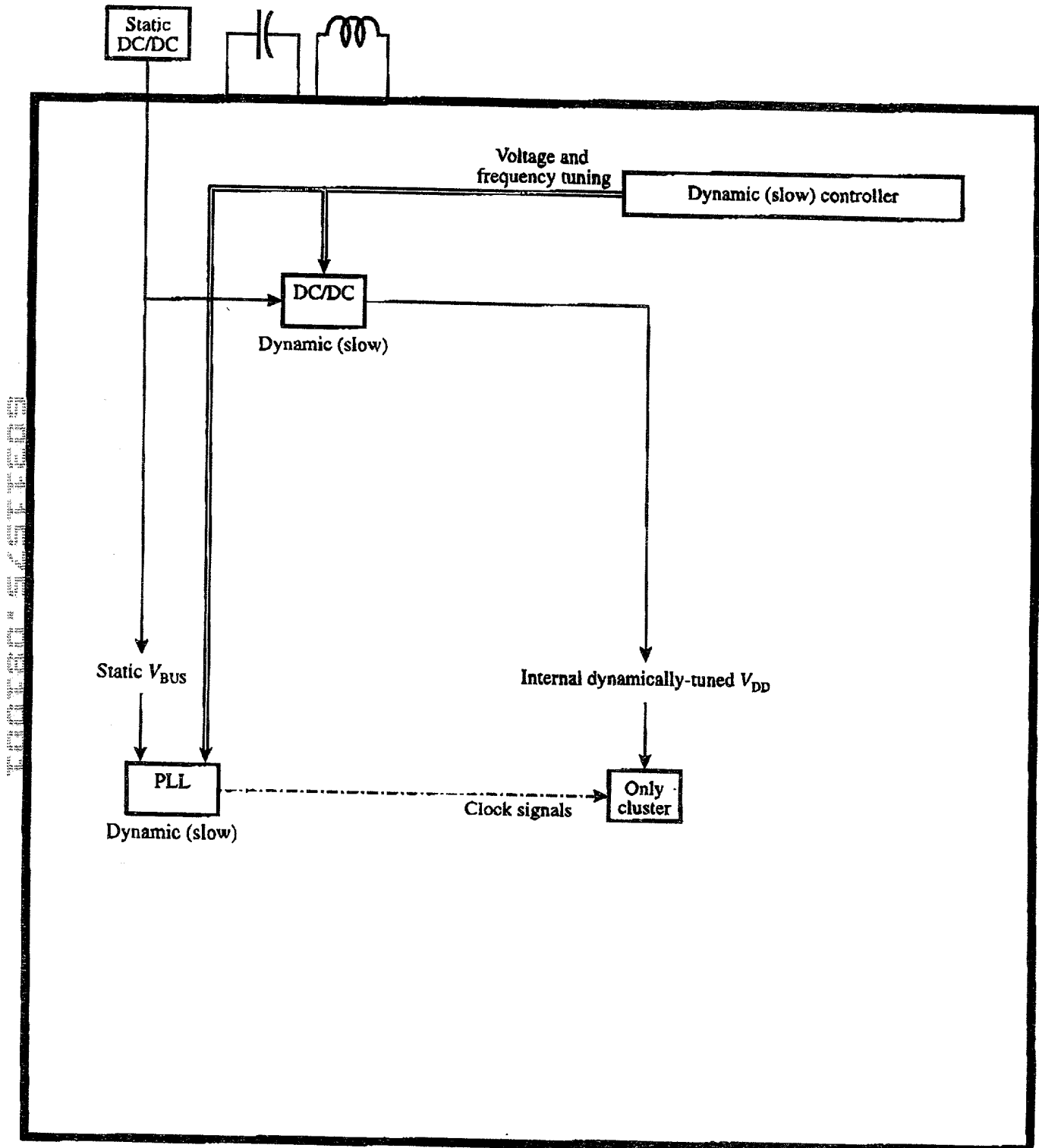


FIGURE 4

C 8 65

**FIGURE 5**