J1064 U.S. PTO
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APPROV

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PTO/SB/16 (8-00)
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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Krishna Siamak	**Shenai Abedinpour**	**Naperville, Illinois**

☐ *Additional inventors are being named on the ____ separately numbered sheets attached hereto*

TITLE OF THE INVENTION (280 characters max)

Monolithic Multi-Slice Synchronous Buck Converter

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

☐ Customer Number [ ] → *Place Customer Number Bar Code Label here*

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☒ Firm or Individual Name	**Jon P. Christensen**				
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ENCLOSED APPLICATION PARTS *(check all that apply)*

☒ Specification *Number of Pages* **7**
☒ Drawing(s) *Number of Sheets* **3**
☒ Application Data Sheet. See 37 CFR 1.76
☐ CD(s), Number [ ]
☒ Other (specify) **Postcard receipt**

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT *(check one)*

☒ Applicant claims small entity status. See 37 CFR 1.27.
☒ A check or money order is enclosed to cover the filing fees
☒ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number **23-0920**
☐ Payment by credit card. Form PTO-2038 is attached.

FILING FEE AMOUNT ($) **$80.00**

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.
☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

Respectfully submitted,

SIGNATURE _____

TYPED or PRINTED NAME **Jon P. Christensen**

TELEPHONE **312-655-1500**

Date **11-05-01**

REGISTRATION NO. *(if appropriate)* **34,137**

Docket Number: **6455-84073**

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Washington, D.C.

P19SMALL/REV05

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FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 80.00

Complete if Known	
Application Number	
Filing Date	concurrently herewith
First Named Inventor	Krishna SHENAI
Examiner Name	
Group/Art Unit	
Attorney Docket Number	6455-84073

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	80.00

SUBTOTAL (1) ($) 80.00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below		Fee Paid
Total Claims		-20**=		x =	
Independent Claims		-3** =		x =	
Multiple Dependent Claims				=	

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge-late filing fee or oath	
127	50	227	25	Surcharge-late provisional filing fee or cover sheet	
139	130	139	130	Non-English Specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a Brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a)	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b)	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

SUBTOTAL (3) ($)

*Reduced by Basic Filing Fee Paid

SUBMITTED BY

Complete *(if applicable)*

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Signature				Date	November 5, 2001

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Date of Deposit: November 5, 2001

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Signature of Person Mailing Paper or Fee

P.05.0574.00

Application Data Sheet

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Electronic Patent Application Fee Transmittal

Application Information

Title Line One::	Monolithic Multi-Slice
Title Line Two::	Synchronous Buck Converter
Total Drawing Sheets::	3
Formal Drawings?::	No
Application Type::	Provisional
Docket Number::	6455-84073

Representative Information

Registration Number One::	24,003
Registration Number Two::	22,839
Registration Number Three::	28,903
Registration Number Four::	27,429
Registration Number Five::	25,060
Registration Number Six::	22,053
Registration Number Seven::	27,466
Registration Number Eight::	29,434
Registration Number Nine::	29,054
Registration Number Ten::	29,381
Registration Number Eleven::	34,044
Registration Number Twelve::	27,600
Registration Number Thirteen::	34,137
Registration Number Fourteen::	39,724
Registration Number Fifteen::	37,963
Registration Number Sixteen::	37,135
Registration Number Seventeen::	40,604
Registration Number Eighteen::	37,435
Registration Number Nineteen::	38,110
Registration Number Twenty::	39,021

PTO/SB/15 (07-05)

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Monolithic Multi-Slice Synchronous Buck Converter
[11 claims]

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ABSTRACT

A novel monolithic step-down dc-dc buck converter is proposed that uses two or more parallel slices to achieve a high output current with a smaller filter capacitor. The n slices are operated with a phase difference of $360°/n$. Each of the converter slices is based on a synchronous rectifier topology to avoid the excessive power losses introduced by the diode component of conventional step-down buck converters. Hysteretic control is used to provide both pulse-width modulation and pulse-frequency modulation of the internal gate-drive waveform without the need to provide a dedicated clock signal or oscillator circuit. The hysteretic control is further refined using digital control techniques to enforce a brief dead time between the activation of each slice such that undesirable circulating currents are prevented. A significant advantage of the proposed multi-slice step-down dc-dc buck converter and its associated control is that the semiconductor switches, filter inductors and capacitor, and the control circuit are fabricated as part of a single monolithic integrated circuit.

FIELD OF THE INVENTION

The field of the invention is related to dc-dc converters and more particularly to voltage step-down dc-dc converters.

BACKGROUND OF THE INVENTION

The diversity of VLSI chips often results that a chip utilize a supply voltage that is not available within its target platform. Therefore, a voltage converter is required to translate an available voltage into one suitable for the VLSI chip. Often this involves a voltage step-down or buck operation. Since many of these platforms require high efficiency, compact dimensions, rapid response to load conditions, and high power output, several modifications of conventional switching DC/DC converters are necessary. The most common solution to date is to create n multiple parallel step-down buck converters (i.e. a multi-slice converter) such that the aggregate output current is n times higher than with a single converter. Efficiency over 80% can be achieved with this solution, but the construction of such converters requires a hybrid solution that combines VLSI control chips, external passive (filtering) components, and external power

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semiconductor switches. Also, the switching frequency is generally low, such that the responsiveness of the step-down buck converter to load conditions has large granularity.

The significant improvement of the technology of the present patent is the application of very high-speed control circuitry. Unlike conventional control, which requires a clock signal or oscillator circuit to generate a reference frequency, the control of the present invention is oscillator-less and internally generates its own switching impulses. The result is a highly adaptive and dynamic switching pattern. Conventional control (pulse-width and/or pulse-frequency modulation) is limited to the tuning of the single reference frequency. The control of the present invention has no fixed frequency and can very rapidly and accurate adjust both the frequency and the duty cycle of the pulse. The control of the present invention is further refined using digital techniques to ensure that a dead time is inserted between the activation of each successive converter slice. This dead time prevents undesirable circulating currents.

Using the high-speed control of the present invention, all of its components (semiconductor switches, filter inductors and capacitor, and the control circuit) are fabricated as part of a single monolithic integrated circuit.

Application Publication

SUMMARY

A novel monolithic step-down dc-dc buck converter is proposed that uses two or more parallel slices to achieve a high output current with a smaller filter capacitor. The n slices are operated with a phase difference of $360°/n$. Each of the converter slices is based on a synchronous rectifier topology to avoid the excessive power losses introduced by the diode component of conventional step-down buck converters. Hysteretic control is used to provide both pulse-width modulation and pulse-frequency modulation of the internal gate-drive waveform without the need to provide a dedicated clock signal or oscillator circuit. The hysteretic control is further refined using digital control techniques to enforce a brief dead time between the activation of each slice such that undesirable circulating currents are prevented. A significant advantage of the proposed multi-slice step-down dc-dc buck converter and its associated control is that the semiconductor switches, filter inductors and capacitor, and the control circuit are fabricated as part of a single monolithic integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view of a dc-dc voltage converter in accordance with an embodiment of the invention;

FIG. 2 is a schematic view of a dc-dc voltage converter in accordance with a second embodiment of the invention; and

FIG. 3 is a schematic view of a dc-dc voltage converter in accordance with a third embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a schematic diagram of a dc-dc step-down voltage converter in accordance with an embodiment of the invention. The converter would be fabricated as an integral part of a multifunction chip by use of the existing chip fabrication techniques. The step-down converter is fabricated using CMOS technology. A well-known fabrication design and a construction technique referred to as MOSIS is used to fabricate the step-down converter with a 0.5-μm minimum feature. The synchronous recfitier uses a pMOSFET in the main current path, and an nMOSFET to divert the inductor current when the pMOSFET is turned off. The resonant gate-drive for each device operates out-of-phase and accounts for different polarity of the two switches. This is accomplished by the circuit configuration in FIG. 1. A control circuit, based on feedback of output voltage determines the switching sequence. Out-of-phase signals are provided to the two switches.

The step-down converter accomplishes a voltage step-down through the interaction of the supply voltage, SOURCE, the NMOS switch, and the PMOS switch. One NMOS and one PMOS are used per slice. The "chopped" output voltage is then filtered using the low-pass filter (LC). One inductor is used per slice; a single filter capacitor is shared by all slices.

The operation of the multi-slice converter is described in the context of a single slice next. When the NMOS switch is closed, the voltage of the internal node is at ground potential; when the PMOS switch is closed, the voltage of the internal node is at the supply voltage potential. The NMOS and PMOS switches are closed alternately. By adjusting the duty cycle of the NMOS closing, the average voltage at the internal node can be controlled between 0 and the supply voltage. This square wave signal is then filtered to a DC level by the low-pass filter. Output current (represented by the load resistor R) is then drawn from the output filter capacitor.

By adding parallel slices of identical converters, the total output current is increased.

The control circuit operates in a manner such that the output voltage is continuously compared to a desired potential. If the output voltage is higher than the nominal (reference) voltage, then the NMOS switch is activated. If the output voltage is lower than the nominal (reference) voltage, then the PMOS switch is activated. Operation of multiple slices is interleaved in time such that only one converter slice is active at a time. That is, for n slices, each slice is operated $360°/n$ out of phase.

Each slice can be integrated monolithically by choosing a sufficiently high switching frequency to ensure low values of passive components. A typical switching frequency of 100 MHz will result in inductor values less than 100 nH and capacitance around 1 nF. Such values can be provided on-chip. However, presently available on-chip inductors have poor quality

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factor, restricted less than 15. Using such practical components, efficiency improvement up to 10% is expected from the use of this topology over the conventional multi-slice synchronous rectifier.

A specific embodiment of a method and apparatus of dc voltage conversion according to the present invention has been described for the purpose of illustrating the manner in which the invention is made and used. It should be understood that the implementation of other variations and modifications of the invention is not limited by the specific embodiments described. Therefore it is contemplated to cover the present invention any and all modifications, variations, or equivalents that fall within the true spirit and scope of the basic underlying principles disclosed and claimed herein.

CLAIMS

We claim:

1. A dc-dc voltage converter comprising:

a series synchronous rectifier connection of two main switches that operate as a voltage step-down device,

an inductor connected to the common point of the series switch configuration, which provides an output of the dc-dc voltage converter;

a step-down switch configuration operating at a load-dependent switching frequency,

an oscillator-less control circuit that monitors the output voltage of the voltage step-down device and triggers the switches each time the output of the dc-dc converter falls below a threshold voltage to produce a dynamic pulse-width and pulse-frequency modulation,

a capacitor connected between the output of the inductor and ground potential to provide filtering of the output voltage waveform.

2. The dc-dc converter as in claim 1 further wherein multiple (*n*) slices are connected in parallel to provide a higher output current.

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3. The dc-dc converter as in claim 1 further wherein the voltage step-down device further comprises a power supply connected in series with the synchronous rectifier configuration.

4. The dc-dc converter as in claim 1 further comprising a capacitor coupled across an output of the dc-dc step-down converter.

5. The dc-dc converter as in claim 1 wherein both the switches comprising the synchronous rectifier are implemented using MOSFET devices.

6. The dc-dc converter as in claim 1 further comprising a feedback and startup circuit, the output of which controls the switching of the synchronous rectifier switches.

7. The dc-dc converter as in claim 6, with the control signal for the two main switches being out of phase with each other.

8. The dc-dc converter as in claim 7, with the control signal for each of the n slices being $360°/n$ phase-shifted.

9. The dc-dc converter as in claim 7, with the control signal to the synchronous switch being generated by the use of an inverter.

10. The dc-dc converter as in claim 8, wherein the voltage regulator further comprises an LC filter providing the regulated output voltage at the output of the LC filter.

11. A monolithic multi-slice step-down dc-dc converter for improved performance comprising:

a series switch with the first end of the switch connected in series with a positive side of a power supply, the power supply also having a negative side,

another series switch with the first end of the switch connected in series with the first switch, the second end being connected to the negative side of the power supply,

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an inductor, with the first end of the inductor connected to the common connection point of the two switches,

a capacitor with a first end of the capacitor connected between a second end of the inductor and the negative side of the power supply and the voltage across the capacitor defining an output of the monolithic dc-dc converter,

a control feedback and startup circuit receiving an output of the dc-dc converter, and a reference voltage as input, generating the required switching signals for the step-up switch,

multiple slices of the above switches and synchronous switches, and output filters, such that multiple identical slices appear in parallel, sharing a single common input voltage terminal and a single common output voltage terminal,

with the two main switches, one auxiliary switch, control feedback and start-up circuit, filter inductor, filter capacitor, resonant inductor and resonant capacitor all being fabricated within a substrate of an integrated circuit forming the monolithic dc-dc voltage step-up converter.

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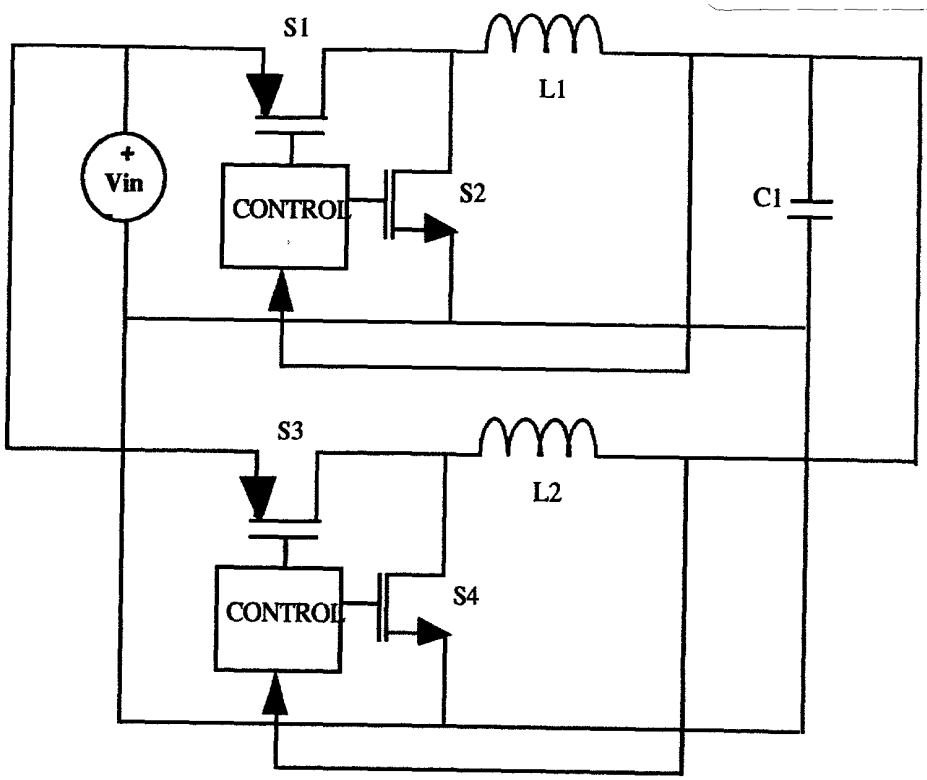

FIGURE 1

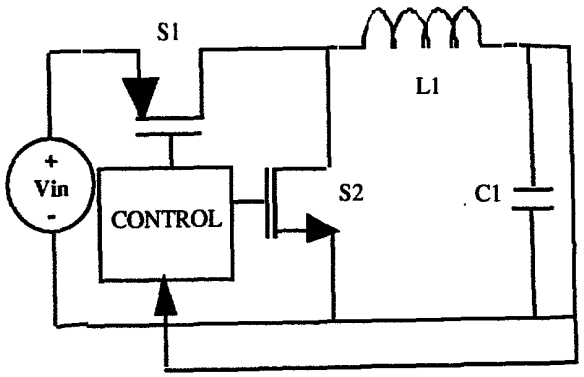

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FIGURE 2

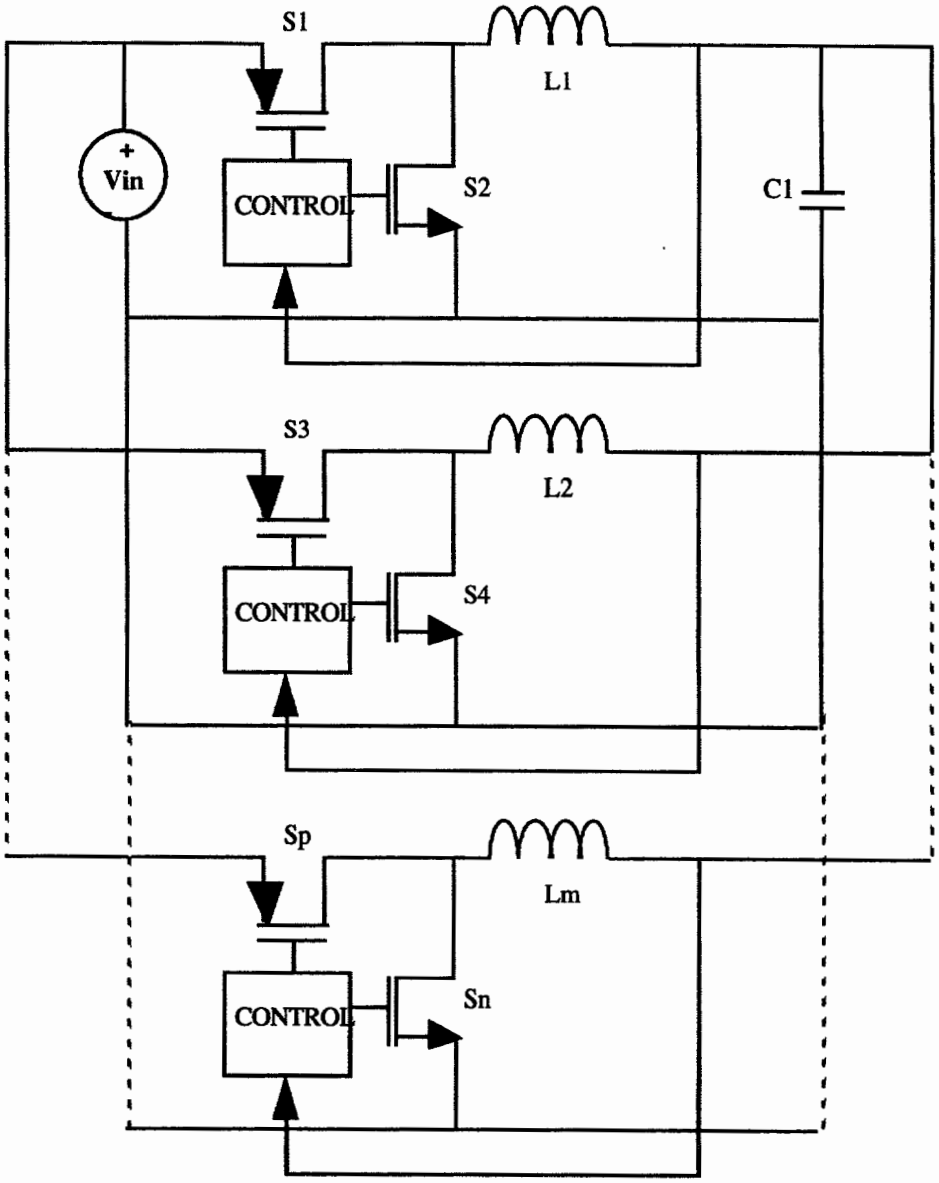

FIGURE 3