

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES), INC.,
Petitioner,

v.

UNIVERSITY OF ROCHESTER
(INTELLECTUAL VENTURES I LLC),
Patent Owner.

IPR2024-01225
Patent 7,089,443 B2

Before JAMESON LEE, THU A. DANG, and HYUN J. JUNG,
Administrative Patent Judges.

DANG, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background*

Lenovo (United States), Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1 and 3–12 (the “challenged claims”) of U.S. Patent No. 7,089,443 B2 (Ex. 1001, “the ’443 patent”). Paper 2 (“Pet.”). University of Rochester¹ (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 7 (“Prelim. Resp.”). With the Board’s authorization, Petitioner filed a Reply to Patent Owner’s Preliminary Response (Paper 9, “Prelim. Reply”), and Patent Owner filed a Sur-reply to Petitioner’s Reply (Paper, 10, “Prelim. Sur-reply”).

Under 37 C.F.R. § 42.4(a), the Board has authority to determine whether to institute an *inter partes* review. Applying the standard set forth in 35 U.S.C. § 314(a), which requires demonstration of a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim, we grant Petitioner’s request and institute an *inter partes* review of all challenged claims.

B. *Real Parties-in-Interest*

Petitioner identifies itself as the real party-in-interest. Pet. 1. Patent Owner identifies itself and Intellectual Venture I LLC, each as the real party-in-interest. Paper 5, 2.

¹ Patent Owner states that University of Rochester owns the patent and Intellectual Ventures I LLC is an exclusive licensee. Paper 5, 2 (Patent Owner’s mandatory notices). Patent Owner represents that Intellectual Ventures I LLC has all substantial rights to the ’443 patent. *Id.*

C. Related Proceedings

The parties identify the '443 patent as the subject of the following related district court matters: (i) *Intellectual Ventures I LLC v. Lenovo Group Ltd.*, No. 6:23-cv-00307 (W.D. Tex.); (ii) *Intellectual Ventures I LLC v. TCL Electronics Holdings Ltd.*, No. 6:23-cv-00309 (W.D. Tex.); (iii) *Intellectual Ventures I LLC v. TCL Electronics Holdings Ltd. f/k/a/ TCL Multimedia Technology Holdings, Ltd.*, No. 6:23-cv-00293 (W.D. Tex.); and (iv) *Intellectual Ventures II LLC v. Lenovo Group Limited*, No. 6:23-cv-00068 (W.D. Tex.). Pet. 1–2; Paper 5, 2; Paper 8, 1–2.

The '443 patent also is challenged by a different petitioner in IPR2024-01245. *TCL Electronics Holdings Ltd. v. University of Rochester*, IPR2024-01245, Paper 2.

D. The '443 Patent

The '443 patent, titled “Multiple Clock Domain Microprocessor,” issued on August 8, 2006, from Application No. 10/762,550, with a filing date of January 23, 2004, and claiming the benefit of provisional Application No. 60/441,759, filed on January 23, 2003. Ex. 1001, codes (54), (45), (21), (22), (60). The '443 patent observes “that in order to continue the current pace of clock frequency increases, microprocessor designers will eventually be forced to abandon singly-clocked globally synchronous systems in favor of some form of asynchrony.” *Id.* at 1:42–45.

The '443 patent describes a multiple clock domain (MCD) microarchitecture for a microprocessor which uses a globally-asynchronous, locally-synchronous (GALS) clocking style where each functional block operates with a separately generated clock. *Id.* at code (57); *see also id.* at 4:16–19. The '443 patent reports that “by scaling frequency and voltage in

different domains dynamically and independently, we can achieve an average improvement in energy-delay product of nearly 20%.” *Id.* at 5:8–11. The ’443 patent further describes that “[t]he independence of each local domain clock implies no global clock skew requirement, permitting potentially higher frequencies within each domain and greater scalability in future process generations.” *Id.* at 4:29–32. “Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain allows for finer grained dynamic voltage and frequency scaling, and thus lower energy, than can be achieved with single clock, single-core-voltage systems.” *Id.* at 4:40–45.

Figure 1 of the ’443 patent is a block diagram of an MCD processor, and is reproduced below. Ex. 1001, 5:32–33.

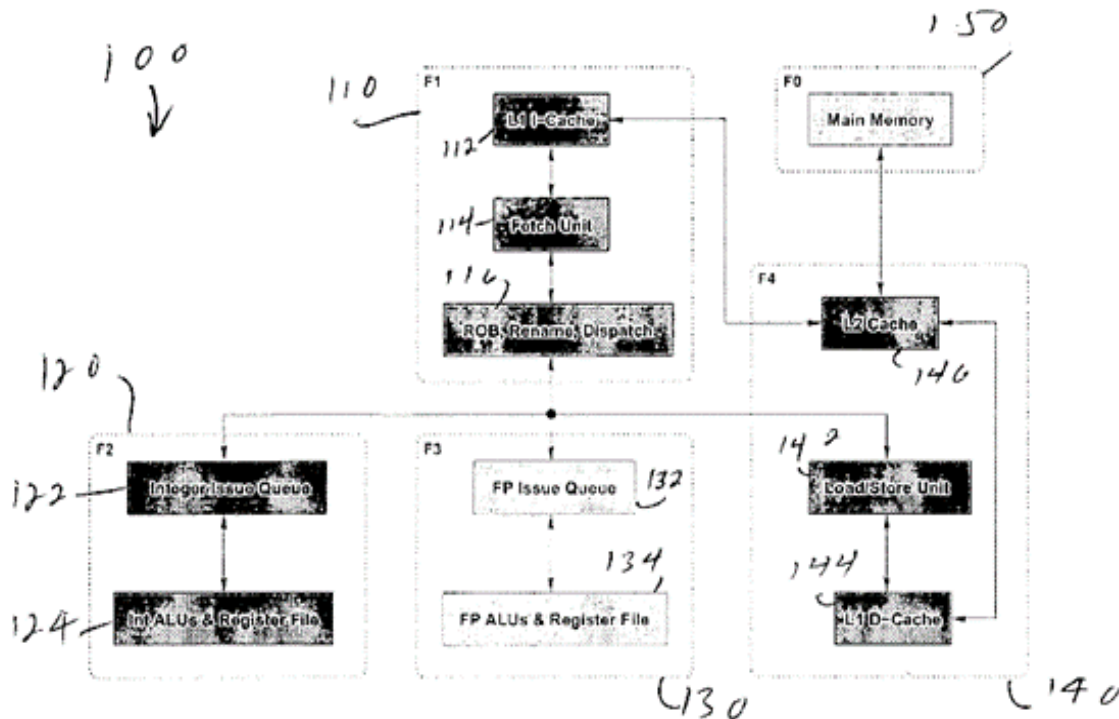


Figure 1

Figure 1 depicts architecture 100 with four domains consisting of front end 110, integer issue/execute 120, floating point issue/execute 130, and load/store issue/execute 140. *Id.* at 5:67–6:11. Front end 110 includes instruction cache 112, fetch unit 114, and branch prediction, rename, and dispatch 116. *Id.* Integer issue/execute 120 includes integer issue queue 122 and integer arithmetic logic units and register file 124. *Id.* Floating point issue/execute 130 includes a floating point issue queue 132 and floating point arithmetic logic units and register file 134. *Id.* Load/store issue/execute 140 includes load/store unit 142, L1 D-cache 144, and L2 cache 146, where L2 cache 146 is in communication with main memory interface 150 as well as with cache 112 of front end 110. *Id.*

Although the '443 patent “recognizes the overhead associated with independent clocks with no known phase relationship” in an MCD processor, the '443 patent provides a “general queue structure that we use for inter-domain communication” that “minimizes the need for inter-domain synchronization.” Ex. 1001, 6:39–41, 6:54–55, 5:2–4. In particular, the '443 patent’s selection of certain “queues as interdomain synchronization points has the advantage of hiding the synchronization cost whenever the queue is neither full nor empty.” *Id.* at 6:50–53.

E. Challenged Claims

Of the challenged claims (1 and 3–12), claims 1 and 8 are the independent claims. Claims 3–7 depend from claim 1, and claims 9–12 depend from claim 8. Independent claim 1 is illustrative and is reproduced below:

1. A multiple clock domain microprocessor comprising:
a plurality of domains;

for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and

for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

Ex. 1001, 17:9–19.²

F. Evidence

Petitioner relies on the references listed below.

Reference		Date	Exhibit No.
Shenai	US 2003/0030326 A1	Feb. 13, 2003	1004
Halepete	WO 01/53921 A1	July 26, 2001	1005
Sherburne	US 2002/0169990 A1	Nov. 14, 2002	1006
Traylor	US 5,473,756	Dec. 5, 1995	1007
Georgiou	US 6,047,248	Apr. 4, 2000	1008
Kranich	WO 01/33352 A1	May 10, 2001	1009

Petitioner also relies on the Declaration of R. Jacob Baker, Ph.D.

Ex. 1002.

G. The Asserted Grounds of Unpatentability

Petitioner contends that the challenged claims are unpatentable under the following grounds. Pet. 3–4.

² The text set forth above reflects corrections made by way of a certificate of correction of June 14, 2011.

Claim(s) Challenged	35 U.S.C. § ³	Reference(s)/Basis
1, 3, 8, 12	103(a)	Georgiou
4, 9	103(a)	Georgiou, Halepete
5, 10	103(a)	Georgiou, Kranich
1, 3–5, 8, 9, 12	103(a)	Shenai
4, 9	103(a)	Shenai, Halepete
5–7, 10, 11	103(a)	Shenai, Sherburne
7	103(a)	Shenai, Sherburne, Traylor

II. ANALYSIS

A. Claim Construction

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b) (2024). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art (POSITA) at the time of the invention and in the context of the entire patent disclosure. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc).

Petitioner asserts “that no construction of the claims is necessary to assess whether the prior art reads on the Challenged Claims.” Pet. 20–21. Patent Owner also does not propose a construction for any claim term. Prelim. Resp. 19–25. However, Patent Owner argues that “[w]hen a patentee describes the features of the ‘present invention,’ it is well-settled that ‘this description limits the scope of the invention.’” *Id.* at 19–20

³ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. Because the ’443 patent was filed before March 16, 2013, the effective date of the relevant amendment, the pre-AIA version of § 103 applies.

(quoting *Pacing Techs., LLC v. Garmin Int'l, Inc.*, 778 F.3d 1021 (Fed. Cir. 2015)). Thus, Patent Owner argues:

the claim language reciting “for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” requires that the separate clocks in the plurality of domains be globally-asynchronous.

Prelim. Resp. 20. Patent Owner notes that the '443 patent includes a reference to a publication that “describes an ‘approach [that] maintains a known phase relationship between clocks whose frequencies are related by a rational factor’” *Id.* at 22 (quoting Ex. 2004 (“Sarmenta”), Abstract). According to Patent Owner, “the claims should not be read to cover schemes like Sarmenta’s, where frequencies are related by a ‘rational factor’ that significantly restricts the possible choices of frequencies to those related by the ‘rational factor.’” *Id.* at 23 (quoting Ex. 1001, 6:32–36).

In addition, Patent Owner proposes that the claims should be limited to covering microprocessors. Specifically, Patent Owner argues that “[t]he specification [of the '443 patent] makes clear that the ‘present invention’ is directed to a microprocessor,” that “it is clear that the claims are limited to microprocessors, and that the ‘plurality of domains’ are domains within a microprocessor.” Prelim. Resp. 24–25 (citing Ex. 1001, code (54), 4:14–17).

At this stage of the proceeding, we do not perceive a need to construe any claim terms of the '443 patent for purposes of determining whether to institute trial. *See, e.g., Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the

controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that “only those terms need to be construed that are in controversy, and only to the extent necessary to resolve the controversy”)); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

B. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, “would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

C. Level of Skill in the Art

The level of skill in the art is a factual determination that provides a primary guarantee of objectivity in an obviousness analysis. *See Al-Site Corp. v. VSI Int’l Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999) (citing *Graham*, 383 U.S. at 17–18 (1966); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991)). Generally, it is easier to establish obviousness under a higher level of ordinary skill in the art. *See Innovention Toys, LLC v. MGA Entm’t, Inc.*, 637 F.3d 1314, 1323 (Fed. Cir. 2011) (“A less

sophisticated level of skill generally favors a determination of nonobviousness . . . while a higher level of skill favors the reverse.”).

Petitioner, relying on the testimony of Dr. Baker, contends that a person of ordinary skill in the art (POSITA) “would have had a bachelor’s degree in electrical engineering, computer engineering, or the equivalent, and 2–3 years of experience designing computing circuits and systems,” wherein “[m]ore practical experience could offset the aforementioned education and vice-versa.” Pet. 4 (citing Ex. 1002 ¶¶ 29–31). At this stage in the proceeding, Patent Owner does not contest Petitioner’s proposal or offer an alternative. On this record, we are persuaded that Petitioner’s proposal is consistent with the technology described in the Specification and the cited prior art. For purposes of this Decision, we adopt Petitioner’s proposed level of skill.

D. Claims 1, 3, 8, and 12 as obvious over Georgiou; Claims 4 and 9 as obvious over Georgiou and Halepete; and Claims 5 and 10 as obvious over Georgiou and Kranich

Petitioner contends that Georgiou renders obvious claims 1, 3, 8, and 12 of the ’443 patent. Pet. 61–76. Petitioner also contends that Georgiou, in further view of Halepete, renders obvious claims 4 and 9 of the ’443 patent. *Id.* at 76–78. Petitioner further contends that Georgiou, in further view of Kranich, renders obvious claims 5 and 10 of the ’443 patent. *Id.* at 78–81.

In response, Patent Owner contends that Petitioner has failed to show that Georgiou teaches or suggests every limitation of challenged claims 1, 3, 8, and 12, and that Halepete and Kranich fail to cure the shortcomings of Georgiou. *See* Prelim. Resp. 37–40.

We briefly summarize Georgiou, Halepete and Kranich below.

1. Georgiou (Ex. 1008)

Georgiou, titled “Performance-Temperature Optimization by Cooperatively Varying the Voltage and Frequency of a Circuit,” discloses a “[a] system and method using thermal feedback to cooperatively vary a voltage and frequency of a circuit to control heating while maintaining synchronization.” Ex. 1008, codes (54), (57). More specifically, Georgiou’s disclosure applies, in a preferred embodiment, to “a multi-functional unit processor such as a superscalar microprocessor,” and describes “[u]sing thermal sensors for feedback, the voltage swing and operating frequency of the circuit [being] cooperatively varied (also called voltage-frequency pairs) to reduce the power dissipation without comprising reliability of system synchronization.” *Id.* at 2:21–26, 3:48–52.

Figure 1, reproduced below, illustrates a block diagram of a superscalar processing system.

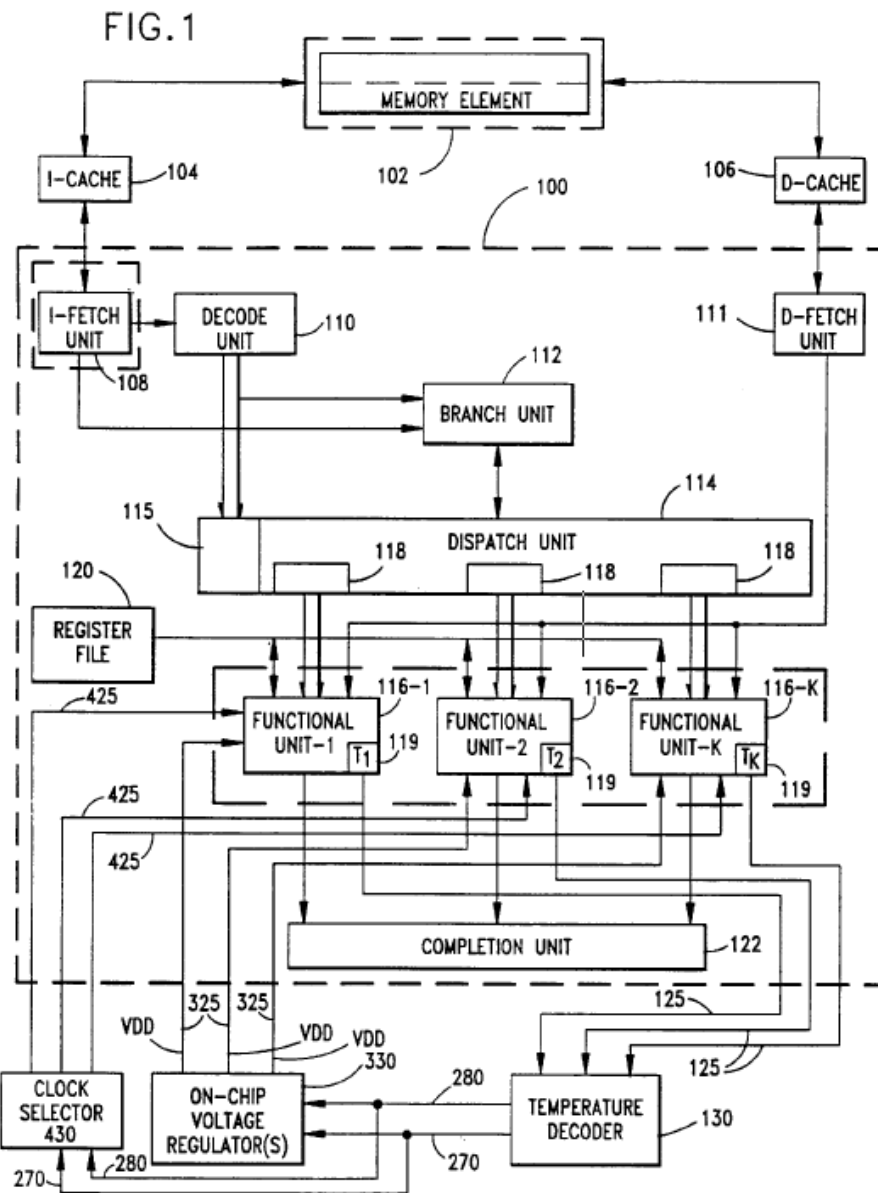
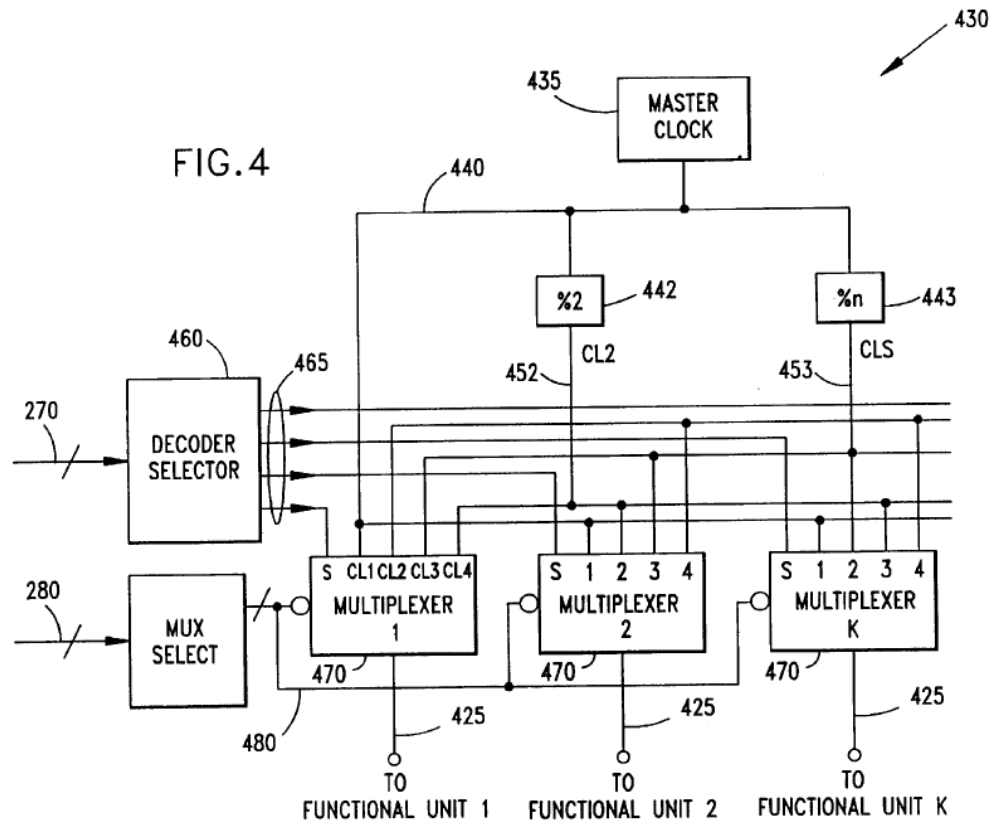


Figure 1 shows processor unit 100, which includes components for fetching instructions from memory and “analyz[ing] dependencies among pending instructions, and schedul[ing] execution of instructions, one on each of functional units 116-1 through 116-K.” Ex. 1008, 5:16–38. Georgiou provides that “[e]xamples of well known functional units are: fixed-point units, floating point units, load/store units, and branch units found in typical general purpose and superscalar microprocessors.” *Id.* at 3:58–61. In the

Figure 1 embodiment, “each functional unit 116-1 . . . 116-K may include an on-chip thermal sensor 119 mechanism,” the output of which is periodically sampled by temperature decoder 130. *Id.* at 6:43–53. “The decoder 130 decodes and compares the thermal sensor output with a predetermined threshold to provide current/clock control signals 270 respectively to an adjustable on-chip voltage regulator 330 (described in FIG. 3) and to a clock selector 430 (described in FIG. 4).” *Id.* at 6:54–59. “[S]ignals 270 operate to control the current sources to voltage regulator 330 to adjust the regulator output voltage 325,” as well as “to select a predetermined corresponding clock frequency via clock selector 430.” *Id.* at 6:59–63. This resulting voltage-frequency pair maintains critical timing paths within design specifications and is provided to the functional units via paths 325 and 425. *Id.* at 6:63–66.

Clock selector 430 is shown in detail in Figure 4, reproduced below.



As shown in Figure 4, “master clock 435 running at a master clock frequency 440 [] is used as the common source and provides a common clock reference for a number of clock dividers whose output is some predetermined fraction of the master clock frequency 440.” Ex. 1008, 8:37–42. For example, “clock divider 442 may be a divide-by-two clock divider whose output frequency 452 is one-half that of the master clock frequency 440, and clock divider 443 may be a divide-by-n clock divider whose output frequency 453 is one-nth that of the master clock frequency 440.” *Id.* at 8:43–47.

2. Halepete (Ex. 1005)

Halepete, titled “Adaptive Power Control,” relates to “controlling the power used by a computer” by “determining when the operating characteristics of the central processor are significantly different than required by the operations being conducted” and “changing the operating characteristics of the central processor,” such as by increasing or decreasing the frequency and voltage. Ex. 1005, codes (54), (57). In particular, Halepete describes a computer system with processor 10, wherein processing unit 16 includes master control unit 18 “for monitoring the operating characteristics of the processor” and “accomplishing clock and voltage control.” *Id.* at 5:5–17, Fig. 1.

3. Kranich (Ex. 1009)

Kranich, titled “Fast Multithreading for Closely Coupled Multiprocessors,” relates to “[a] processor architecture containing multiple closely coupled processors” interconnected via thread control device 300, which includes first-in-first-out buffers 310A-310B and synchronization logic 314. Ex. 1009, codes (54), (57), 10:6–11, Fig. 3A.

4. Independent claim 1 as obvious over Georgiou

a) *Preamble, “A multiple clock domain microprocessor comprising”*

Petitioner contends that Georgiou teaches a system with multiple functional units, such as in a superscalar microprocessor, where the functional units may be independently controllable such that each unit operates with a different voltage and frequency combination. Pet. 62 (citing Ex. 1002 ¶¶ 192–194; Ex. 1008, 3:49–63, 5:2–6, 8:37–67). In particular, Petitioner contends that “a POSITA would have recognized that *Georgiou’s* functional units correspond to the claimed ‘domains,’” and, in the

alternative, that “a POSITA would have known that applying *Georgiou*’s functional units as the claimed ‘domains’ would have been a simple substitution of one known element (*Georgiou*’s functional units) for another (domains) to obtain predictable results.” *Id.* at 63 (citing Ex. 1002, ¶¶ 192–194; *KSR*, 550 U.S. at 415–421).

At this stage of the proceeding, Patent Owner does not present arguments in the Preliminary Response addressing the specific merits of Petitioner’s contentions with respect to the preamble. *See generally* Prelim. Resp. 37–39.

Having reviewed all of Petitioner’s assertions regarding the limitations in the preamble, as well as all supporting evidence, we determine on this record that Petitioner has made a sufficient showing that *Georgiou* teaches a “multiple clock domain microprocessor,” as recited in claim 1.⁴

b) “a plurality of domains”

Petitioner contends that *Georgiou* teaches the claimed “plurality of domains” for the reasons detailed above regarding the language of the preamble. Pet. 64 (citing Ex. 1002 ¶¶ 195–196). Specifically, Petitioner asserts that *Georgiou*’s functional units 116-1 through 116-K teach the claimed domains. *Id.*

At this stage of the proceeding, Patent Owner does not present arguments in the Preliminary Response addressing the specific merits of Petitioner’s contentions with respect to this claim limitation. *See generally* Prelim. Resp. 37–39.

⁴ Because Petitioner has shown that the recitation in the preamble is satisfied by *Georgiou*, there is no need at this time to determine whether the preamble is limiting. *See Realtime Data*, 912 F.3d at 1375.

Having reviewed all of Petitioner's assertions regarding this claim limitation, as well as all supporting evidence, we determine on this record that Petitioner has made a sufficient showing Georgiou teaches "a plurality of domains," as recited in claim 1.

- c) *"for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains"*

Petitioner contends that Georgiou discloses clock frequencies 425 applied to the clock inputs of respective functional units. Pet. 67 (citing Ex. 1002 ¶¶ 197–198; Ex. 1008, 4:61–62). Specifically, Petitioner asserts that within Georgiou's clock selector 430 are multiplexers 470, each of which "corresponds to the claimed 'clock' for separately generating a clock signal at a frequency for a corresponding functional unit." *Id.* at 68 (citing Ex. 1002 ¶¶ 193, 197–201). Petitioner provides annotated versions of Figures 1 and 4 of Georgiou, reproduced below, to supports its contentions:

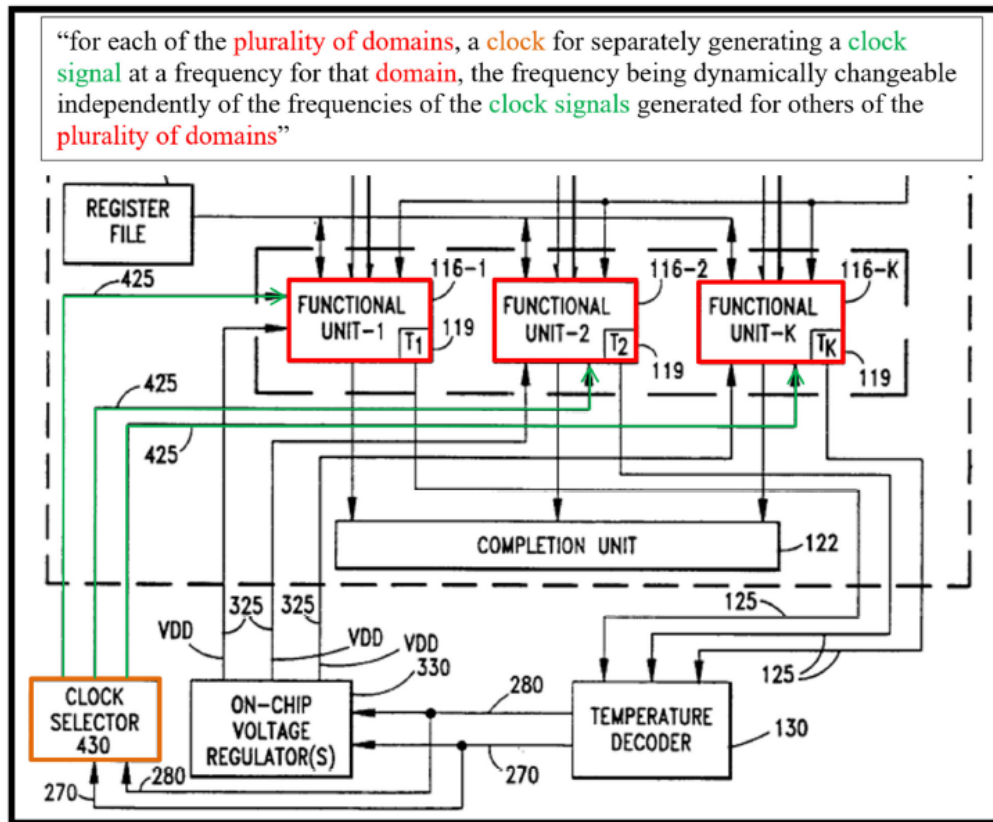


Figure 1 of Georgiou (Excerpted)

The above annotated Figure 1 of Georgiou in the Petition shows a data processing system comprising functional units 116 (red), and clock selector 430 (orange) providing clock signal 425 (green) to a respective one of functional units 116. Pet. 66.

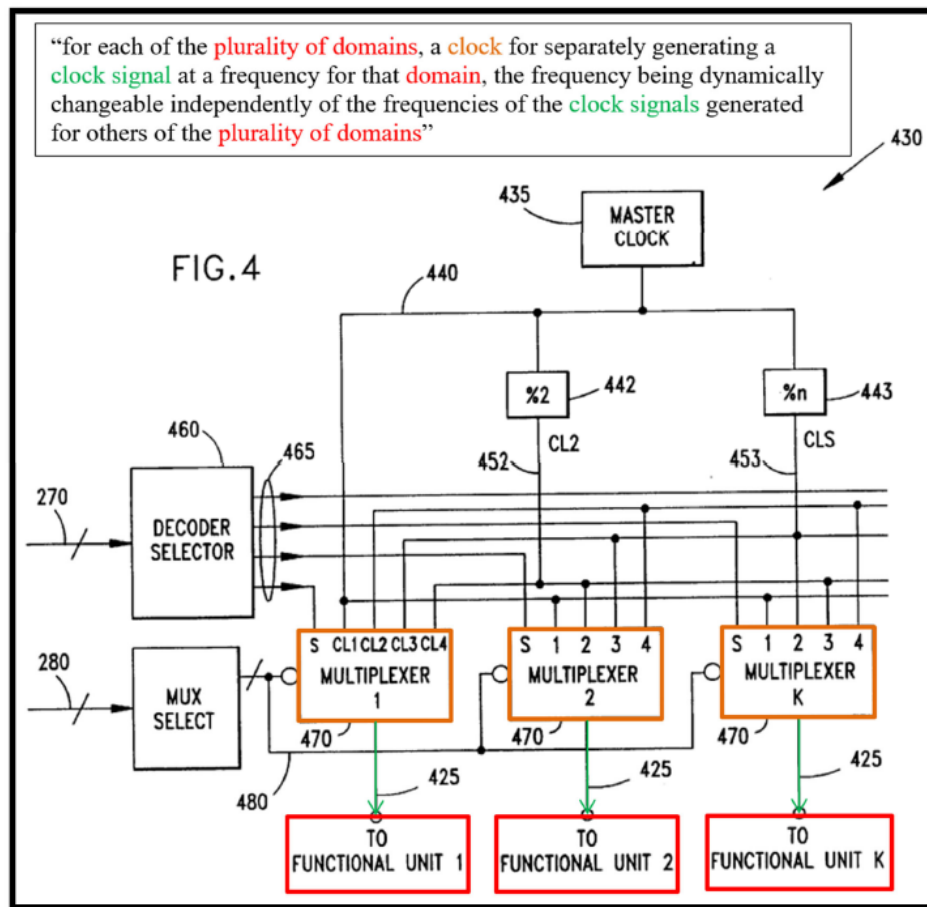


Figure 4 of Georgiou

The above annotated Figure 4 of Georgiou in the Petition shows data clock selector 430 in further detail. Pet. 68. As shown in annotated Figure 4, data clock selector 430 comprises multiplexers 470 (orange) providing clock signal 425 (green) to a respective one of functional units (red). *Id.*

Petitioner asserts that, as shown in annotated Figure 4 of Georgiou, clock selector 430 also includes “master clock 435 running at master clock frequency 440,” wherein “clock dividers can manipulate the master clock frequency by an integer value, such as divide-by-2 or divide-by-n.” *Id.* at 69 (citing Ex. 1002 ¶¶ 199–201; Ex. 1008, 8:37–48). Accordingly, according to Petitioner, “[e]ach multiplexor 470 provides a clock signal to its respective

functional unit independent of the other clock signals, and the clock signals are dynamically changed depending on the individual needs of each functional unit at a given time.” *Id.* (citing Ex. 1002 ¶¶ 197–201).

Patent Owner responds that Georgiou does not disclose, for a given domain, “separately generating a clock signal . . . the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” as recited in claim 1. Prelim. Resp. 37. In particular, Patent Owner argues that Georgiou “relies on a ‘rational factor’ relationship, wherein clock signals are generated as integer or fractional multiples or divisions of a master clock.” *Id.* at 39. This, according to Patent Owner, “inherently imposes significant restrictions on frequency selection, ensuring periodic alignment of clock edges but failing to provide the independence required by the Challenged Claims.” *Id.*

We find unavailing Patent Owner’s arguments, which turn on the contention that Georgiou’s clock signals are generated as integer or fractional multiples or divisions of a master clock, and thus, Georgiou “fail[s] to provide the independence required by the Challenged Claims.” Prelim. Resp. 39. In particular, we find unavailing Patent Owner’s argument that clock signals generated based on *a master clock* are not generated independently of the clock signals generated *for others of the plurality of domains*.

Although Patent Owner points to Figure 4 of Georgiou to support its contention that Georgiou’s clock signals are generated based on the master clock and thus that Georgiou “fails to provide the independence” claimed (Prelim. Resp. 38–39), Figure 4 merely shows that clock signals are dependent on master clock, but does not show that the clock signals are

dependent on the clock signals of the other functional units (domains). *See* Ex. 1008, Fig. 4.

As Petitioner points out, in Georgiou’s Figure 4, “[e]ach multiplexer 470 outputs the selected clock frequency which is coupled to the **particular functional unit** via the appropriate one of paths 425.” Pet. 69 (citing Ex. 1008, 8:61–67). We find persuasive Dr. Baker’s testimony relied upon by Petitioner, wherein Dr. Baker testified that, “[t]herefore, not only are the clock signals provided independent to the other generated clock signals,” but “the clock signals are also dynamically changeable depending on the individual operating conditions of each functional unit at a given time.” Ex. 1002 ¶¶ 197–201; *see also* Pet. 69. Although Dr. Baker acknowledged that Georgiou discloses a clock selector with a master clock running at a master clock frequency, Dr. Baker pointed out that is similar to the ’443 Patent. Ex. 1002 ¶ 200 (citing Ex. 1008, 8:37–41; Ex. 1001, 5:7–9 (“The preferred embodiment uses four domains, . . . so that domains may vary somewhat in size and still be covered by a single clock.”))).

Having reviewed all of Petitioner’s assertions, Patent Owner’s responsive arguments, as well as all supporting evidence, we determine that Petitioner has made a sufficient showing that Georgiou teaches “for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” as recited in claim 1.

- d) *“for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains”*

Petitioner contends that supply voltage 325 output from on-chip voltage regulator(s) 330 “provides separate voltages to the inputs of functional unit 116-1, 116-2, . . . 116-K.” Pet. 70–71 (Ex. 1002 ¶ 202; Ex. 1008, 4:38–41). Petitioner asserts that to the extent “*Georgiou’s* voltage supply is found not to correspond to a ‘voltage input,’ it was known in the art for microprocessors to use input pins to receive a voltage.” *Id.* at 71–72 (citing Ex. 1002 ¶¶ 203–204; Ex. 1011, 6; Ex. 1013, 138, 175).

Petitioner further asserts that “[c]urrent/clock signal 270, as seen in Figure 1, is coupled to ‘adjustable on-chip voltage regulators 330 to reduce the supply voltage 325,’” such that “‘the **modulated voltage** and frequency **are applied to the functional unit to dynamically control heating** while maintaining synchronization and reliability.’” Pet. 72 (citing Ex. 1002 ¶¶ 202–204; Ex. 1008, 4:35–36, 10:48–51). Petitioner contends that “[e]ach functional unit is provided a separate voltage that changes depending on the thermal feedback received from that functional unit,” and that “the voltages supplied are independent from one another, and are dynamically changeable (e.g., based on thermal feedback of each functional unit).” *Id.* (citing Ex. 1002 ¶¶ 202–204; Ex. 1008, 5:5–7).

At this stage of the proceeding, Patent Owner does not present arguments in the Preliminary Response addressing the specific merits of Petitioner’s contentions with respect to this claim limitation. *See generally* Prelim. Resp. 37–39.

Having reviewed all of Petitioner’s assertions regarding this claim limitation, as well as all supporting evidence, we determine on this record

that Petitioner has made a sufficient showing Georgiou teaches “for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains,” as recited in claim 1.

f) Conclusion

For the foregoing reasons, we determine the evidence and arguments presented show a reasonable likelihood Petitioner would prevail in establishing that claim 1 would have been obvious over Georgiou.

5. Independent claim 8, claim 3 depending from claim 1, and claim 12 depending from claim 8, as obvious over Georgiou

Petitioner contends Georgiou teaches or renders obvious claims 3, 8, and 12. Pet. 72–76 (citing Ex. 1002 ¶¶ 53–56, 205–221; Ex. 1008, 2:21–26, 3:19–21, 3:58–61, 9:4–11). At this stage of the proceeding, Patent Owner does not provide arguments for claims 3, 8, and 12 separate from claim 1. *See* Prelim. Resp. 37–39.

Having reviewed all of Petitioner’s assertions regarding the limitations in these claims, as well as all supporting evidence, we determine on this record that Petitioner has made a sufficient showing that Georgiou teaches the limitations of claims 3, 8, and 12. For the foregoing reasons, we determine the evidence and arguments presented show a reasonable likelihood Petitioner would prevail in establishing that claim 3, 8, and 12 would have been obvious over Georgiou.

6. Claims 4 and 9 as obvious over Georgiou and Halepete; Claims 5 and 10 as obvious over Georgiou and Kranich

Petitioner contends Georgiou in combination with Halepete teaches or renders obvious claims 4 and 9. Pet. 76–78 (citing Ex. 1002 ¶¶ 222–227;

Ex. 1008, 1:49–54, 2:28–29). Petitioner then contends Georgiou in view of Kranich teaches or renders obvious claims 5 and 10. *Id.* at 78–80 (citing Ex. 1002 ¶¶ 41–44, 228–235; Ex. 1008, 3:48–53; Ex. 1009, 9:4–5, 10:6–13, Fig. 3A).

At this stage of the proceeding, Patent Owner merely contends that the Petition does not allege, and neither Halepete nor Kranich teaches, the “separately generating a clock signal” limitation, and thus, neither Halepete nor Kranich cures the shortcomings of Georgiou. *See generally* Prelim. Resp. 39–40. But we have already determined above that the limitation is met by Georgiou.

Having reviewed all of Petitioner’s assertions regarding the limitations in these dependent claims, as well as all supporting evidence, we determine on this record that Petitioner has made a sufficient showing that the combination of Georgiou and Halepete teaches the limitations of claims 4 and 9, and that the combination of Georgiou and Kranich teaches the limitations of claims 5 and 10.

For the foregoing reasons, we determine the evidence and arguments presented show a reasonable likelihood Petitioner would prevail in establishing that claims 4 and 9 would have been obvious over Georgiou and Halepete; and that claims 5 and 10 would have been obvious over Georgiou and Kranich.

F. Claims 1, 3–5, 8, 9, and 12 as obvious over Shenai; Claims 4 and 9 as obvious over Shenai and Halepete; Claims 5–7, 10, and 11 as obvious over Shenai and Sherburne; and Claim 7 as obvious over Shenai, Sherburne, and Traylor

Petitioner contends that Shenai renders obvious claims 1, 3–5, 8, 9, and 12 of the '443 patent. Pet. 21–43. Petitioner also contends that Shenai in further view of Halepete renders obvious claims 4 and 9 of the '443 patent. *Id.* at 43–47. Petitioner further contends that Shenai in further view of Sherburne renders obvious claims 5–7, 10, and 11 of the '443 patent. *Id.* at 47–59. Finally, Petitioner contends that Shenai and Sherburne in further view of Traylor render obvious claim 7 of the '443 patent. *Id.* at 59–61.

In response, Patent Owner contends that Shenai is not prior art to the '443 patent. Prelim. Resp. 26–29. Patent Owner also contends that “Shenai relies on a ‘rational factor’ relationship, where clock signals are generated as integer or fractional multiples or divisions of a reference clock,” and thus fails to teach “the independently dynamic frequency control across clock domains required by the Challenged Claims.” *Id.* at 29. Patent Owner further contends that Halepete, Sherburne, and Traylor fail to cure the shortcomings of Shenai. *Id.* at 36–37.

Resolving the issue of whether Shenai is prior art, particularly Patent Owner’s assertion of conception and actual reduction to practice by February 2002, would be better after the parties’ positions have been developed further at trial.

III. CONCLUSION

Because we determine that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing at least one of the challenged claims is unpatentable, we institute *inter partes* review as to all challenged

claims and grounds presented in the Petition. At this stage of the proceeding, we have not made a final determination as to the patentability of any of these challenged claims.

IV. ORDER

For the reasons given, it is

ORDERED that pursuant to 35 U.S.C. § 314, an *inter partes* review is instituted as to claims 1 and 3–12 of the '443 patent to determine whether:

1) claims 1, 3, 8, and 12 are unpatentable under 35 U.S.C. § 103(a) as obvious over Georgiou;

2) claims 4 and 9 are unpatentable under 35 U.S.C. § 103(a) as obvious over Georgiou and Halepete;

3) claims 5 and 10 are unpatentable under 35 U.S.C. § 103(a) as obvious over Georgiou and Kranich;

4) claims 1, 3–5, 8, 9, and 12 are unpatentable under 35 U.S.C. § 103(a) as obvious over Shenai;

5) claims 4 and 9 are unpatentable under 35 U.S.C. § 103(a) as obvious over Shenai and Halepete;

6) claims 5–7, 10, and 11 are unpatentable under 35 U.S.C. § 103(a) as obvious over Shenai and Sherburne; and

7) claim 7 is unpatentable under 35 U.S.C. § 103(a) as obvious over Shenai, Sherburne, and Traylor; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this Decision.

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