

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.,

Petitioner,

v.

UNIVERSITY OF ROCHESTER
(INTELLECTUAL VENTURES I, LLC),

Patent Owner.

Case No. IPR2024-01225

U.S. Patent No. 7,089,443

PATENT OWNER'S RESPONSE

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PATENT OWNER'S EXHIBIT LIST

EX2001	Declaration of Dr. David Kaeli
EX2002	Resume of Dr. David Kaeli
EX2003	Declaration of David H. Albonesi
EX2004	L. F. G. Sarmenta, G. A. Pratt, and S. A. Ward. Rational Clocking. In Proceedings of the International Conference on Computer Design, Austin, Tex., October 1995
EX2005	Semeraro et al, "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," High Performance Computer Architecture (HPCA), Feb. 2, 2002
EX2006	Provisional Application No. 60/311,575, filed August 10, 2001
EX2007	Provisional Application No. 60/337,837, filed November 5, 2001
EX2008	Provisional Application No. 60/337,479, filed November 5, 2001
EX2009	Provisional Application No. 60/338,510, filed November 5, 2001
EX2010	SimpleScalar Tutorial
EX2011	U.S. Patent No. 5,634,041 "Rationally clocked communication interface" by Pratt et al. ("Pratt").
EX2012	A. Chakraborty and M. R. Greenstreet, "Efficient self-timed interfaces for crossing clock domains," Ninth International Symposium on Asynchronous Circuits and Systems, 2003. Proceedings., Vancouver, BC, Canada, 2003, pp. 78-88.
EX2013	Declaration of Dr. David Kaeli

I. INTRODUCTION

The Petition (Paper #2) challenges claims 1 and 2-12 (“Challenged Claims”) of U.S. Patent No. 7,089,443 (“‘443 Patent,” EX1001) under seven grounds. Pet., 3-4.

The ‘443 Patent claims a breakthrough in energy-efficient processor design: a multiple-clock-domain (MCD) microprocessor architecture in which each functional domain operates with an independently generated clock that is dynamically controllable without regard to the clocks of other domains. As the patent explains, this globally-asynchronous, locally-synchronous (GALS) design allows for fine-grained dynamic voltage and frequency scaling (DVFS) on a per-domain basis, enabling significant improvements in energy-delay product with minimal performance overhead.

Petitioner’s challenge fails because it relies on prior art references—such as Shenai and Georgiou—that fundamentally diverge from the independently clocked architecture claimed in the ‘443 Patent. These references describe systems in which clock signals across domains are derived from a common master clock and constrained to fixed integer ratios—a “rational factor” relationship expressly disavowed in the ‘443 specification. As shown below, such rational clocking schemes inherently restrict frequency choices to small integer multiples of a common clock to preserve global synchronization through deterministic phase

alignment cycles (e.g., “coincidence cycles” or “beating periods”), in stark contrast to the invention’s architectural independence. Because Petitioner’s cited references do not render obvious the claimed per-domain autonomy in clock generation, and because key references are not prior art in view of the inventors’ earlier reduction to practice, the Petition fails to establish that any challenged claim is unpatentable.

II. SPECIFICATION OF ‘443 PATENT

A. Summary Of The Invention

As explained in the Summary of the Invention of the ‘443 Patent:

... the *present invention* is directed to a multiple clock domain (MCD) microarchitecture, which uses a *globally-asynchronous*, locally-synchronous (GALS) clocking style. In an MCD microprocessor *each functional block operates with a separately generated clock*, and synchronizing circuits ensure reliable inter-domain communication. EX1001, 4:13-19 (emphasis added).

As explained next in the Summary of the Invention, the inventors identified several “*potential*” advantages of the MCD design, including “lower energy:”

Although the inter-domain synchronization increases the number of clock cycles required to run a given application, an MCD microprocessor affords a number of *potential* advantages over a singly clocked design: ...

The *independence* of each *local domain clock* implies no global skew requirement...

Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain allows for finer grained dynamic voltage and frequency scaling, and thus *lower energy*, than can be achieved with single clock, single-core-voltage systems. EX1001, 6:22-45. (emphasis

added).

Next, in the Summary of the Invention, the inventors explained that they implemented their MCD design and found that it achieved significant performance advantages:

In the present application, we describe an initial implementation of an MCD microprocessor that is a straightforward extension of a singly-clocked synchronous dynamic superscalar design. By accurately modeling inter-domain synchronization, we characterize the performance and energy costs of the required synchronization circuitry. We then explore the potential benefits of per-domain dynamic voltage and frequency scaling. Our results demonstrate a 20% average improvement in energy-delay product for a set of benchmarks that includes both compute and memory-bound applications. ...

Performance results for applications drawn from standard benchmark suites suggest that the division of the processor into multiple domains incurs an average baseline performance cost of less than 4%. At the same time, by scaling frequency and voltage in different domains dynamically and independently, we can achieve an average improvement in energy-delay product of nearly 20%. By contrast, global voltage scaling to achieve comparable performance degradation in a singly clocked microprocessor achieves an average energy-delay improvement of only 3%. EX1001, 4:51-5:14 (emphasis added).

At the end of the Summary of The Invention, the inventors noted that “the invention” was described in an earlier paper by the inventors:

The following Paper describes the invention and is hereby incorporated by reference in its entirety into the present disclosure: Semeraro et al, “Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling,” *High Performance Computer Architecture* (HPCA), Feb. 2, 2002. EX1001, 5:22-27.

The above-referenced Paper is referred to hereinafter as “the Paper,” and

attached hereto as EX2005. As explained more fully in Section III, *infra*, the salient portions of the ‘443 Patent specification were lifted almost verbatim from the Paper. The findings of the inventors set forth in the Paper and reproduced in the ‘443 Patent were nothing short of *groundbreaking*. In 2023, this work was awarded the Technical Committee on Computer Architecture’s 2022 Test of Time Award at the 29th IEEE International Symposium on High-Performance Computer Architecture. EX2003, ¶9. The Test of Time Award “recognizes the most influential papers published in prior sessions of the International Symposium of High Performance Computer Architecture (HPCA) each of whom have had significant impact in the field.” EX2003, ¶10. The Paper has been cited 575 times since it was published.

B. Detailed Description

The Detailed Description of ‘443 Patent distinguished the MCD processor disclosed in the ‘443 Patent from prior synchronization schemes that restricted the relative frequencies of the clocks:

Some synchronization schemes restrict the ... relative frequencies of the clocks, thereby eliminating the need for hardware arbitration [27]. Unfortunately, these schemes impose *significant restrictions* on the possible choices of frequencies. ... EX1001, 6:32-36 (emphasis added).

As discussed more fully below, reference [27] referred to in the above quotation corresponded to a paper by Sarmenta (EX2004) that described systems that placed significant restrictions on the possible choices of frequencies. As Dr. Kaeli explains, “[t]he ‘443 invention overcomes these limitations, offering independence in clock

frequency generation, allowing each frequency domain to adopt their own independent frequency, offering near infinite resolution in terms of the clock frequency selected for each domain.” EX2013, ¶34.

III. THE CLAIMED INVENTION HAD BEEN CONCEIVED AND ACTUALLY REDUCED TO PRACTICE BY FEBRUARY 2002

A. Legal Principles

A patent owner can antedate an asserted prior art reference by showing conception and actual reduction to practice prior to the date of the reference. *Medtronic, Inc. v. Teleflex Life Scis. Ltd.*, 86 F.4th 902, 906 (Fed. Cir. 2023). “Conception can be proven with evidence that a full description,” of the invention existed “in written materials disclosed to persons,” in the United States. *Scott v. Koyama*, 281 F. 3d 1243, 1247 (Fed. Cir. 2002). “Reduction to practice in the United States requires that the invention be embodied in tangible form in the United States,” and “that the invention, as conceived, was shown to work for its intended purpose.” *Id.*; *In re Steed*, 802 F. 3d 1311, 1316 (Fed. Cir. 2015). In connection with the requirement that the invention be embodied in a tangible form, it is well-settled that a computer program with executable instructions stored in memory (e.g., on a computer disk) is embodied in a tangible form. *In re Beauregard*, 53 F.3d 1583 (Fed. Cir.1995).

B. The Paper Authored By The Inventors And Published In February 2002 Demonstrates Conception By Providing A Full Written Description Of The Claimed Invention

As noted above, the ‘443 Patent cited and incorporated the Paper by reference (i.e., Semeraro et al, “Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling,” High Performance Computer Architecture (HPCA), Feb. 2, 2002). EX1001, 5:22-27; EX2005. The Paper was published in *Proceedings Eighth International Symposium on High Performance Computer Architecture*, pp. 29-40 in February, 2002. EX2003, ¶5. The authors of the Paper coincide identically with the named inventors on the ‘443 Patent. *Id.* As shown below, with the exception of reference numerals, all of the figures contained in the ‘443 Patent are substantively identical to corresponding figures in the Paper. EX2003, ¶8.

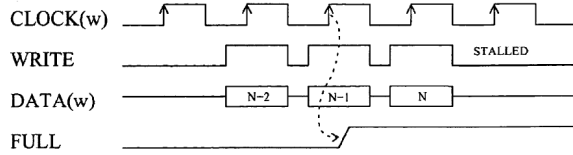


Figure 3

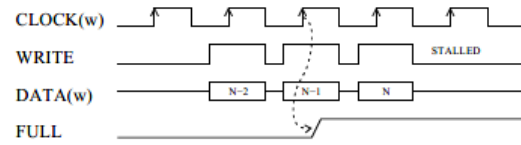


Figure 3. Full flag

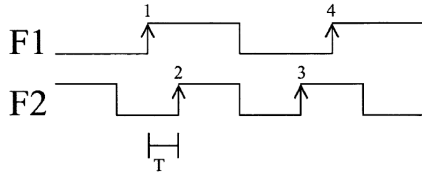


Figure 4

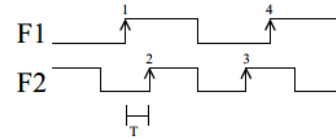


Figure 4. Synchronization timing

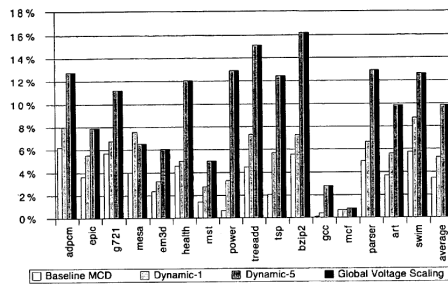


Figure 5

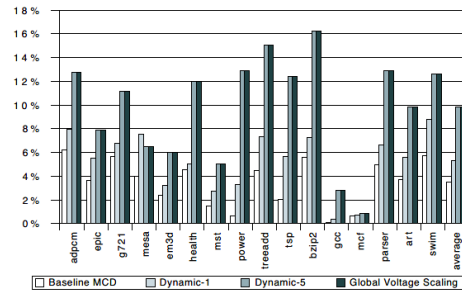


Figure 5. Performance degradation results

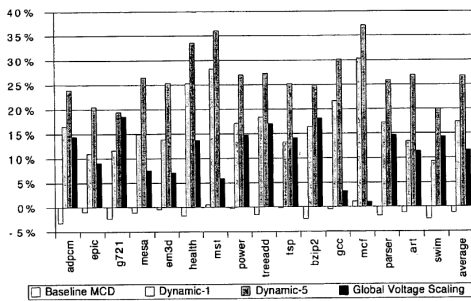


Figure 6

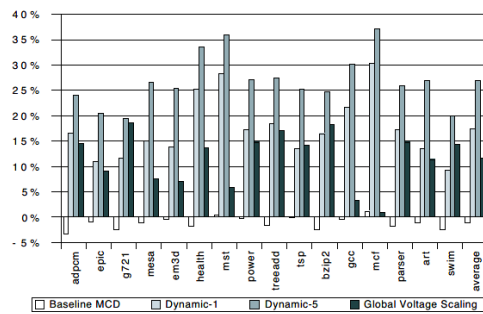


Figure 6. Energy savings results

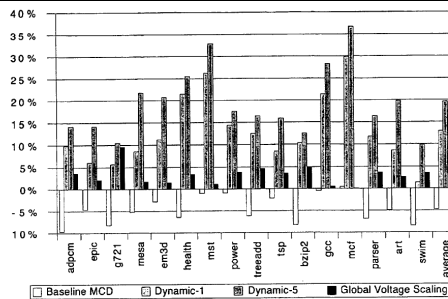


Figure 7

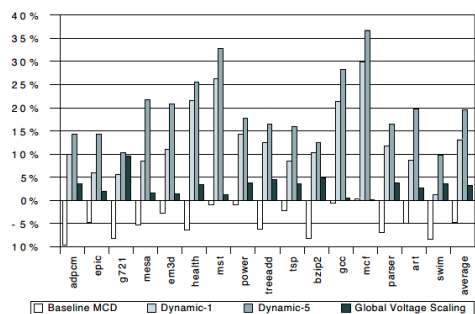


Figure 7. Energy-delay improvement results

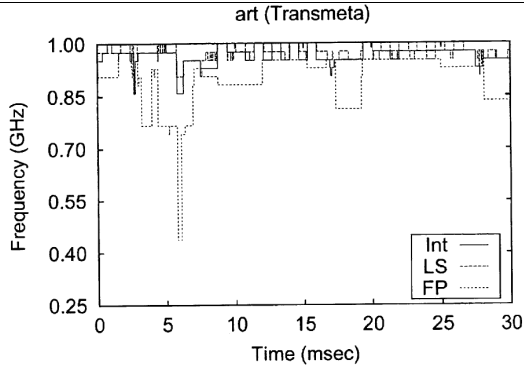


Figure 8A

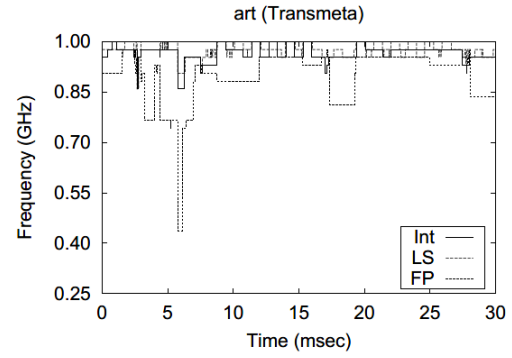


Figure 8B

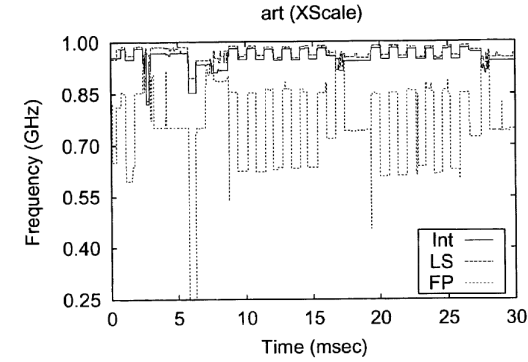


Figure 9A

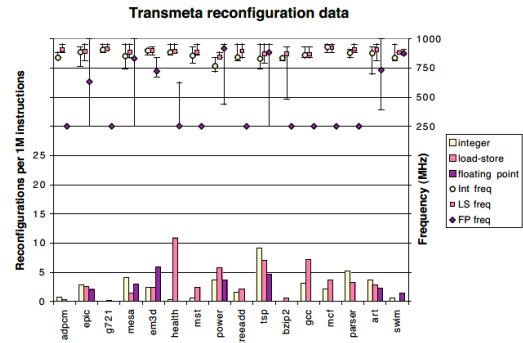


Figure 9B

Given the overlap in the figures, it should not be surprising that the wording of the ‘443 Patent closely tracks that of the Paper. For example, the first three paragraphs of the Introduction section of the Paper are reproduced virtually verbatim as the first three paragraphs in the Background of the ‘443 Patent (EX1001, 1:25-2:14; EX2005, at 1-2), and the 31 references listed at the end of the Paper are listed identically at the end of the Background of the ‘443 Patent. EX1001, 2:17-4:4; EX2005, at 11-12). In addition, as shown below, the salient aspects of the Summary of the Invention of the ‘443 Patent (EX1001, 4:6-5:21) are taken verbatim from the Introduction section of the Paper (EX2005, 2):

Summary of Invention of ‘443 Patent	Corresponding Language In the Introduction of Paper
<p>It is another object of the invention to provide an approach that</p> <p>allows for aggressive future frequency increases, maintains a synchronous design methodology, and exploits the trend towards making functional blocks more autonomous.</p> <p>To achieve the above and other objects, the present invention is directed to</p> <p>a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable</p>	<p>An approach that</p> <p>allows for aggressive future frequency increases, maintains a synchronous design methodology, and exploits the trend towards making functional blocks more autonomous, is ...</p> <p>a <i>multiple clock domain (MCD)</i> microarchitecture, which uses a <i>globally-asynchronous, locally-synchronous (GALS)</i> clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable</p>

<p>inter-domain communication. Thus, fully synchronous design practices are used in the design of each domain. Although the inter-domain synchronization increases the number of clock cycles required to run a given application, an MCD microprocessor affords a number of potential advantages over a singly clocked design: ...</p> <p>Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain allows for finer grained dynamic voltage and frequency scaling, and thus lower energy, than can be achieved with single clock, single-core-voltage systems. ...</p> <p>In the present application,</p> <p>we describe an initial implementation of an MCD microprocessor that is a straightforward extension of a singly-clocked synchronous dynamic superscalar design.</p>	<p>inter-domain communication. Thus, fully synchronous design practices are used in the design of each domain. Although the inter-domain synchronization increases the number of clock cycles required to run a given application, an MCD microprocessor affords a number of potential advantages over a singly clocked design: ...</p> <p>Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain allows for finer grained dynamic voltage and frequency scaling, and thus lower energy, than can be achieved with single clock, single-core-voltage systems. ...</p> <p>In this Paper,</p> <p>we describe an initial implementation of an MCD microprocessor that is a straightforward extension of a singly-clocked synchronous dynamic superscalar design.</p>
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Below is a mapping demonstrating a description of each element of claims 1-7 of the '443 Patent in the Paper. While not shown, the mappings for claims 8, 9, 10, 11 and 12 of the '443 Patent correspond to the mappings below for claims 1, 4, 5, 6 and 3, respectively.

Claim 1

<u>Claim Element</u>	<u>Disclosure in Paper</u>
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<p>A multiple-clock-domain microprocessor comprising:</p>	<p>“An approach that allows for aggressive future frequency increases, maintains a synchronous design methodology, and exploits the trend towards making functional blocks more autonomous, is a <u>multiple clock domain</u> (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an <u>MCD microprocessor</u> each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. ... In this Paper, we describe an initial implementation of an MCD microprocessor ...” EX2005, 2 (emphasis added).</p>
<p>a plurality of domains;</p>	<p>“We describe an alternative approach, which we call a Multiple Clock Domain (MCD) processor, in which the chip is divided into <u>several (coarse-grained) clock domains</u>, within which independent voltage and frequency scaling can be performed.” EX2005, Abstract (emphasis added).</p>
<p>for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and</p>	<p>“We describe an alternative approach, which we call a Multiple Clock Domain (MCD) processor, in which the chip is divided into several (coarse-grained) clock domains, <u>within which independent voltage and frequency scaling can be performed.</u>” EX2005, Abstract (emphasis added).</p>

	<p>“Figures 8 and 9 both illustrate the value of using <u>different frequencies in different clock domains: by controlling these frequencies independently</u> we can maintain the required frequency in domains that are critical to performance, while aggressively scaling those domains that are less performance-critical.” EX2005, 10 (emphasis added).</p>
<p>for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.</p>	<p>“We describe an alternative approach, which we call a Multiple Clock Domain (MCD) processor, in which the chip is divided into several (coarse-grained) clock domains, <u>within which independent voltage and frequency scaling can be performed.</u>” EX2005, Abstract (emphasis added).</p> <p>“[B]y <u>scaling frequency and voltage in different domains dynamically and independently</u>, we can achieve an average improvement in energy-delay product of nearly 20%.” EX2005, 11 (emphasis added).</p>

Claim 2

<u>Claim Element</u>	<u>Disclosure in Paper</u>
<p>2. The microprocessor of claim 1, wherein each said clock comprises a phase-locked loop,</p>	<p>“The global clock distribution network is greatly simplified, requiring only the distribution of the externally generated clock to <u>the local Phase Lock Loop (PLL) in each domain.</u>” EX2005, 2 (emphasis added).</p>

and wherein the microprocessor further comprises means for receiving an externally generated clock signal and for supplying the externally generated clock signal to each said phase-locked loop.	“The global clock distribution network is greatly simplified, requiring only the <u>distribution of the externally generated clock to the local Phase Lock Loop (PLL) in each domain.</u> ” EX2005, 2 (emphasis added).
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Claim 3

<u>Claim Element</u>	<u>Disclosure in Paper</u>
3. The microprocessor of claim 1, wherein there are at least four of said domains.	“We propose <u>four clock domains</u> , corresponding to the front end (including L1 instruction cache), integer units, floating point units, and load-store units (including L1 data cache and L2 cache).” EX2005, Abstract (emphasis added).

Claim 4

<u>Claim Element</u>	<u>Disclosure in Paper</u>
4. The microprocessor of claim 1, wherein the microprocessor is programmed to determine a slack in processing in one of the domains and to reduce the clock frequency and the voltage in said one of the domains to reduce the slack.	“Whenever an event in the dependence DAG has two or more incoming arcs, it is possible—in fact likely—that one arc will constitute the critical path and that the others will have “slack”. This slack indicates that the previous operation completed earlier than necessary. If all of the outgoing arcs of an event have <u>slack</u> , then we have an opportunity (assuming zero-cost scaling) to save energy by performing the event at a <u>lower frequency and voltage.</u> ” EX2005, 6 (emphasis added).

	<p>“In particular, the slack associated with L1 data cache misses often allows our reconfiguration tool to scale the integer and floating point domains without significantly impacting overall performance (due to the fact that the available ILP is not sufficient to completely hide the miss latency), even when the utilization for these domains is high.” EX2005, 9.</p>
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Claim 5

<u>Claim Element</u>	<u>Disclosure in Paper</u>
5. The microprocessor of claim 1, further comprising a queue for communication between at least two of the domains.	<p>“The general <i>queue structure that we use for inter-domain communication</i> is shown in Figure 2.” EX2005, 3 (emphasis added).</p>

Claim 6

<u>Claim Element</u>	<u>Disclosure in Paper</u>
6. The microprocessor of claim 5, wherein the queue has a Full flag and an Empty flag, and wherein the microprocessor is programmed to prevent a write to the queue when the Full flag is asserted, until the Full flag is deasserted; and to prevent a read from the queue when the Empty flag is asserted, until the Empty flag is deasserted.	<p>The general queue structure that we use for inter-domain communication is shown in Figure 2. The assertion of the <i>Full flag</i> indicates to the producer that it can <i>no longer write to the queue until the flag is deasserted</i> ..., while the <i>Empty flag</i> when asserted indicates that there is no valid data for the consumer to read from the queue. The consumer <i>waits until Empty is deasserted before reading again.</i>” EX2005, 3 (emphasis added).</p>

Claim 7

<u>Claim Element</u>	<u>Disclosure in Paper</u>
7. The microprocessor of claim 6, wherein the queue is implemented as a dual-ported SRAM.	“This concurrency requires a dual-ported SRAM structure where simultaneous read and write cycles are allowed to <i>different</i> SRAM cells.” EX2005, 4.

Given the significant overlap between the specification of the ‘443 Patent and the Paper, as well as explicit support in the Paper for each element recited in the claims, there can be no dispute that the Paper demonstrates conception by providing a full description of the invention. *Scott*, 281 F. 3d 1243, 1247; EX2003, ¶17 (“The microarchitecture design described in the Paper is the same design implemented by the multiple-clock-domain microprocessor described and claimed in the ‘443 Patent”) and ¶24 (“my Co-Inventors and I had conceived of the invention ... before the February 2002 publication of the Paper.”)

C. The Simulation Described In The Paper Embodied The Invention In A Tangible Form

After describing in detail the claimed multiple clock domain microarchitecture (including all of the aspects set forth in the claim charts in Section III(B) above), the Paper described a detailed simulation that implemented the multiple clock domain microarchitecture prior to the publication of the Paper in February, 2002. *See*, EX2005, 5-8; EX2003, ¶16 (“The simulation described in the

Paper was completed before publication of the Paper in February, 2002”). The simulation described in the Paper used the SimpleScalar tool. As explained by Dr.

Kaeli:

In 2002, SimpleScalar was a computer simulator that was commonly used by the computer architecture community to evaluate the performance and correctness of new architectural designs. Among other features, the SimpleScalar tool included a performance simulator that implemented the device at the microarchitecture level, including data paths, memory architecture and control units of the computer device. See, e.g., Paper at 5 (discussing use of SimpleScalar to implement modified “microarchitecture of the Alpha 21264 microprocessor” where the centralized Register Update Unit was split “into separate reorder buffer (ROB), issue queue, and physical register file structures.”) The SimpleScalar tool provided for execution-driven simulations, where the device being implemented ran as an instrumented program on a host. EX2013, ¶43 (emphasis added).

Significantly, “[w]hen the SimpleScalar tool executed the simulation described in the Paper on a host, the host executing the simulation embodied all of the elements of claim 1 in tangible form. The same can be said for each of the other claims in the ‘443 Patent, namely, that the host executing the simulation embodied all of the elements of the claim in tangible form.” EX2013, ¶44. By embodying all of the elements of the claims in tangible form, execution of the simulation described in the Paper constituted an actual reduction to practice of the claimed invention by February, 2002. *Scott*, 281 F. 3d 1243, 1247 (“[r]eduction to practice...requires that the invention be embodied in tangible form.”)

Moreover, “separate and apart from the host used to implement the device during the simulation, the computer code (standing alone) used to implement the simulation embodied all of the elements of claim 1 (and the other claims of the ‘443 patent) in tangible form.” EX2013, ¶44; *see, e.g., In re Beauregard*, 53 F.3d 1583 (computer program with executable instructions stored in memory (e.g., on a computer disk) is embodied in a tangible form). Thus, the existence of the computer code used to run the simulation provides an independent basis for demonstrating that the invention claimed in the ‘443 was actually reduced to practice by February 2002.

D. The Simulation Described In The Paper Showed That The Invention Worked For Its Intended Purpose

The Introduction of the Paper described several “potential” advantages of the MCD design, including “lower energy.” As explained in the Paper:

Although the inter-domain synchronization increases the number of clock cycles required to run a given application, an MCD microprocessor affords a number of potential advantages over a singly clocked design: ...

- Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain allows for finer grained dynamic voltage and frequency scaling, and thus lower energy, than can be achieved with single clock, single-core-voltage systems. EX2005, 2 (emphasis added).

As explained in the Paper, the performance results of the simulation demonstrated that the MCD design achieved the advantages that the inventors sought to realize:

Performance results for applications drawn from standard benchmark suites suggest that the division of the processor into multiple domains incurs an average baseline performance cost of less than 4%. At the same time, by scaling frequency and voltage in different domains dynamically and independently, we can achieve an average improvement in energy-delay product of nearly 20%. By contrast, global voltage scaling to achieve comparable performance degradation in a singly clocked microprocessor achieves an average energy-delay improvement of only 3%. EX2005, 11.

Thus, the simulation proved that the intended purpose of the MCD design—lower energy—had been achieved. In other words, the simulation results proved that the invention worked for its intended purpose. EX2013, ¶45 (“[O]thers working in the field reading the Paper would have understood that the device implemented in the simulation was shown to work for its intended purpose”); *Scott*, 281 F. 3d 1243, 1247 (Fed. Cir. 2002) (reduction to practice requires “that the invention, as conceived, was shown to work for its intended purpose”).

In summary, the Paper, taken together with the declaration evidence included herewith, establishes that the invention claimed in the ‘443 Patent was conceived and actually reduced to practice by the time the Paper was published in February, 2002. Thus, any reference dated after that time is not prior art.

IV. CLAIMS OF ‘443 PATENT

The claims of the ‘443 Patent capture the MCD microprocessor architecture that the inventors designed and implemented. Claim 1 is representative and provides:

A multiple-clock-domain microprocessor comprising:

a plurality of domains;
for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and
for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

V. CLAIM CONSTRUCTION

The Patent Owner maintains that the Challenged Claims should have their plain and ordinary meaning. However, a determination that a claim term “needs no construction” or has the “plain and ordinary meaning” may be inadequate when a term has more than one “ordinary” meaning or when reliance on a term’s “ordinary” meaning does not resolve the parties’ dispute.” *O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008). Instead, “[t]he terms used in the claims bear a presumption that they mean what they say and have the ordinary meaning that would be attributed to those words by persons skilled in the relevant art.” *Honeywell Int’l, Inc. v. ITC*, 341 F.3d 1332, 1338 (Fed. Cir. 2003). Accordingly, “Properly viewed, the ‘ordinary meaning’ of a claim term is its meaning to the ordinary artisan after reading the entire patent.” *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1358 (Fed. Cir. 2017).

A. The Specification Limits The Claims To Globally-Asynchronous Systems

When a patentee describes the features of the “present invention,” it is well-settled that “this description limits the scope of the invention.” *Pacing Techs., LLC v. Garmin Int’l, Inc.*, 778 F.3d 1021 (Fed. Cir. 2015). In this regard, the “Summary of the Invention” of the ‘443 Patent states that the “present invention” uses a globally-asynchronous clocking style:

... the present invention is directed to a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. ... an MCD microprocessor affords a number of potential advantages over a singly clocked design: ...

The independence of each local domain clock implies no global skew requirement... EX1001, 4:13-31 (emphasis added).

Thus, the claim language reciting “for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” requires that the separate clocks in the plurality of domains be globally-asynchronous. As Dr. Kaeli explains, the “Patent ‘443 overcomes earlier limitations of GALS systems by developing novel methods to support using independent clock and independent voltage controls, overcoming issues related to inter-domain synchronization and communication.” EX2013, ¶30.

B. The Specification Disparages Systems That Impose Significant Restrictions On The Possible Choices Of Frequencies

The Patent Owner maintains that the Challenged Claims should have their plain and ordinary meaning. However, a determination that a claim term “needs no construction” or has the “plain and ordinary meaning” may be inadequate when a term has more than one “ordinary” meaning or when reliance on a term’s “ordinary” meaning does not resolve the parties’ dispute.” *O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008). Accordingly, “Properly viewed, the ‘ordinary meaning’ of a claim term is its meaning to the ordinary artisan after reading the entire patent.” *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1358 (Fed. Cir. 2017).

C. When Viewed From The Perspective Of A POSITA Reading The Entirety Of The ‘443 Patent, The Plain And Ordinary Meaning Of The Separately Generated Clock Signals In Claim 1 Corresponds To Globally-Asynchronous Clock Signals

A POSITA reading the entirety of the ‘443 Patent would have understood that when the patentee described the features of the “present invention” in the Summary of the Invention, the patentee was equating such features with the claims. See, e.g., *Pacing Techs., LLC v. Garmin Int’l, Inc.*, 778 F.3d 1021 (Fed. Cir. 2015). Here, the “Summary of the Invention” of the ‘443 Patent states that the “present invention” uses a globally-asynchronous clocking style:

... the present invention is directed to a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-

synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. ... an MCD microprocessor affords a number of potential advantages over a singly clocked design: ...

The independence of each local domain clock implies no global skew requirement... EX1001, 4:13-31 (emphasis added).

Thus, a POSITA reading the entirety of the ‘443 Patent would have understood that the “the present invention” was directed to globally-asynchronous clocks and would have equated the plain and ordinary meaning of the claim language reciting “for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” to “require that each domain generate its clock signal independently, and that the frequency of each domain’s clock be dynamically changeable without being constrained by the frequencies of other domains. That is, each domain must be free to generate and change its clock frequency without being tethered to small integer multiples of the other domains.” EX2013, ¶114. As Dr. Kaeli explains, the “Patent ‘443 overcomes earlier limitations of GALS systems by developing novel methods to support using independent clock and independent voltage controls, overcoming issues related to inter-domain synchronization and communication.” EX2013, ¶30.

D. POSITA Would Understand the Claims to Require Unrestricted Per-Domain Clock Frequency Control

It would have been readily apparent to a POSITA reading the entirety of the ‘443 Patent that the specification criticized prior synchronization systems—such as those described in Sarmenta (EX2004), Pratt (EX2011), and Chakraborty (EX2012)—that restricted the freedom to select clock frequencies by requiring a rational relationship between clock domains to enable synchronized communication.¹ The criticized systems relied on predetermined, fixed frequency ratios to establish deterministic timing intervals for data transfer, inherently imposing design constraints. To overcome the limitations of such systems, the ‘443 Patent explained that the invention provides “[t]he designers of each domain [to be] *no longer constrained* by the speeds of critical paths in other domains, affording them greater *freedom in each domain* to optimize the tradeoffs among clock speed, latency, and the exploitation of application parallelism via complex hardware structures.” EX1001, 4:34-39.

¹ As explained in the ‘443 Patent: “Some synchronization schemes *restrict the phase relationship and relative frequencies of the clocks*, thereby eliminating the need for hardware arbitration [27]. *Unfortunately, these schemes impose significant restrictions on the possible choices of frequencies*. In addition, the need to control the phase relationships of the clocks means that global clock synchronization is required. *Our design specifically recognizes the overhead associated with independent clocks with no known phase relationship*. We believe this overhead to be *unavoidable* in an MCD processor ... EX1001, 6:32-42.

It would have been apparent to a POSITA reading the criticisms set forth in the specification of systems that restricted the freedom to select clock frequencies, that the intent of the invention set forth in the ‘443 Patent was to eliminate such constraints in favor of techniques that afforded designers freedom in each domain. Given this context, a POSITA reading the entirety of the ‘443 Patent would have understood that the plain and ordinary meaning of “dynamically controlling the clock frequency ... in each of the plurality of domains independently of the clock frequencies” in claim 8 did not cover prior art techniques that restricted the freedom to select clock frequencies by requiring a rational relationship between clock domains. Similarly, a POSITA reading the entirety of the ‘443 Patent would have understood that the plain and ordinary meaning of “for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains” in claim 1 did not cover prior art techniques that restricted the freedom to select clock frequencies by requiring a rational relationship between clock domains. Instead, a POSITA reading the entirety of the ‘443 Patent would have understood that the plain and ordinary meaning of the claims is limited to systems that permit each domain to operate at independently selected, dynamically changeable frequencies without global synchronization constraints.

Simply put, a POSITA reading the entirety of the ‘443 Patent would have understood that the plain and ordinary meaning of the claims did not cover prior art structures disparaged in the specification. See, e.g., *Indivior Inc. v. Dr. Reddy’s Labs*, 752 Fed. Appx. 1024 (Fed. Cir. 2018)(finding that claims did not cover solely using conventional top air drying to produce films because the specification disclaimed such drying by disparaging its use); *SciMed Life Sys. v. Advanced Cardiovascular Sys.*, 242 F.3d 1337 (Fed. Cir. 2001), *citing*, *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1159 (Fed. Cir. 1998) (Specification distinguished prior art as inferior and touted advantages of a conical shaped cup for use in an artificial hip device; “such statements make clear that the ’589 patent discloses *only* conical shaped cups and nothing further”); *Ekchian v. Home Depot, Inc.*, 104 F.3d 1299, 1304, 41 U.S.P.Q.2D (BNA) 1364, 1368 (Fed. Cir. 1997) (“Since, by distinguishing the claimed invention over the prior art, an applicant is indicating what the claims do not cover, he is by implication surrendering such protection”).

As Dr. Kaeli explains, “The ‘443 invention overcomes these limitations [or frequency-restricted systems], offering independence in clock frequency generation, allowing each frequency domain to adopt its own independent frequency, offering near infinite resolution in terms of the clock frequency selected for each domain.” EX2013, ¶34. A POSITA reading the entirety of the specification of the ‘443 Patent

would therefore have understood that the invention (and, hence the claims) excluded rational clocking restrictions imposed by systems like Sarmenta. EX2013, ¶60.

1. Sarmenta Relies on a Rational Frequency Relationship and a Deterministic Coincidence Cycle to Enable Synchronized Communication

The specification of the ‘443 Patent disparages prior art synchronization schemes that restrict the relative frequencies of the clocks:

Some synchronization schemes restrict the ... relative frequencies of the clocks, thereby eliminating the need for hardware arbitration [27]. Unfortunately, these schemes impose significant restrictions on the possible choices of frequencies. ... EX1001, 6:32-36 (emphasis added).

Specifically, the specification explains that Reference [27] is “L. F. G. Sarmenta, G. A. Pratt, and S. A. Ward. Rational Clocking. In Proceedings of the International Conference on Computer Design, Austin, Tex., October 1995.” EX1001 3:54-56. (EX2004) (“Sarmenta”).

Sarmenta describes a restriction that “maintains a known phase relationship between clocks whose frequencies are related by a rational factor, and exploits the predictability of their relative phases to algorithmically time communications without run-time arbitration contests.” EX2004, Abstract. Specifically, Sarmenta and its corresponding patent (U.S. Patent No. 5,634,041) address systems with multiple clock domains, synchronizing communication between subsystems operating at different clock frequencies, particularly when the clocks are not integer multiples of one another by exploiting a special class of frequency relationships—

those governed by a *rational factor*. When the clock frequencies of two systems are related by a rational ratio, such as $f_m / f_n = M / N$, where M and N are integers, their clock edges periodically realign. This rational relationship defines a deterministic interval—referred to as the coincidence cycle in the paper and the beating period in the patent—during which the relative positions of clock edges from both domains repeat predictably. EX2013, ¶32.

A *coincidence cycle* refers to the periodic interval during which the active (typically rising) edges of two independently clocked systems realign. These systems, referred to as system m and system n , operate at different clock frequencies, but their frequencies are related by a rational ratio $f_m / f_n = M / N$, where M and N are small integers. This means that the period of system m 's clock (T_m) and system n 's clock (T_n) are also related such that $T_n / T_m = M / N$. The key insight of rational clocking is that, despite the systems running at different rates, the relative phase relationship between their clocks is predictable and periodic. Specifically, every M clock cycles of system m and N clock cycles of system n , the two clocks' active edges coincide again. This recurring alignment defines the *coincidence cycle*. EX2013, ¶32.

For example, Sarmenta states:

“Given the frequency ratio M/N , we can predict the relative positions of the systems' clock edges within a coincidence cycle and generate a schedule of safe and unsafe cycles for data transfers. **This makes it possible to ensure reliable**

communication by synchronously inhibiting data transfers during the predetermined unsafe cycles. Since the clock interactions are periodic, the same schedule can be applied every M clock cycles on system m and N clock cycles on system n .” EX2004, 1

Accordingly, this duration of a coincidence cycle is the least common multiple (LCM) of the two clock periods, and during this interval, system m completes exactly MM cycles while system n completes NN cycles. The significance of the coincidence cycle is that within it, the relative timing of all active edges of both clocks is fixed and can therefore be analyzed and used to precompute which moments are safe for data transfers between the two systems. This allows the use of lookup tables or runtime scheduling algorithms to avoid unsafe transfers that would otherwise require handshaking or cause metastability.

As Dr. Kaeli explains:

For example, if $M=5$ and $N=6$, the coincidence cycle would span 30 ticks of the global clock which corresponds to 5 clock cycles of system m and 6 clock cycles of system n , and the safe and unsafe transfer opportunities can be determined once and reused in every repetition of the cycle. Thus, the coincidence cycle serves as the basic scheduling unit that enables reliable and high-throughput communication between rationally-clocked systems. EX2013, ¶33

In sum, Sarmenta’s use of small integer ratios of frequencies and the resulting deterministic coincidence cycle enables synchronized communication between independently clocked systems without requiring traditional synchronization mechanisms. By leveraging the periodic re-alignment of clock edges, the system can

precompute and reuse safe data transfer schedules, ensuring both reliability and efficiency. However, Sarmenta cannot support a situation where a coincidence point does not exist (e.g., multiple clock domains running at that same clock frequency but starting at different times) or the coincidence point is unknown in advance (e.g., multiple clock domains that can each independently change its respective clock frequency without constraint). EX2013, ¶34.

2. Pratt Formalizes the Rational Clocking Approach by Using a Predictable Beating Period to Precompute Valid Communication Cycles Between Clock Domains

Sarmenta states, “A U.S. patent application has been filed on behalf of MIT covering portions of this work.” EX2004, 1. The U.S. patent application referenced is US07/929,879, which matured into U.S. Patent No. 5,634,041 “Rationally clocked communication interface” (“Pratt”) (EX2011). Pratt was granted to the Massachusetts Institute of Technology on behalf of Gill Pratt and Stephen Ward, the co-authors of Sarmenta.

Pratt explains that the term “beating period” refers to the recurring interval over which two clocks—operating at rationally related frequencies—return to the same relative phase alignment. Fig. 2 (reproduced below) illustrates the “beat period” when the two independent clock signals will periodically align, which corresponds to the “coincidence cycle” in Sarmenta. EX2013, ¶36.

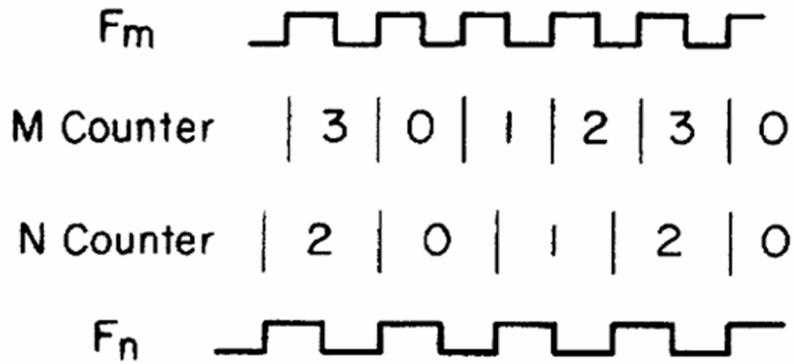


Fig. 2

For example, Pratt explains that, if the frequencies of two clocks are related by a rational ratio $F_m / F_n = M / N$ where M and N are integers, then the beating period is the least common multiple of the two clock periods, expressed as $M \times T_m = N \times T_n$, where T_m and T_n are the periods of the respective clocks. This beating period defines the interval over which the phase relationship between the two clocks repeats, enabling a deterministic communication schedule. EX2013, ¶37.

Specifically, Pratt states:

“The slave clock source may be generated from the master clock source by a M/N phase locked loop. The M/N phase locked loop defines a rational frequency relationship between the processing units. This allows the present invention to generate one clock from the other. The clock frequencies, F_m and F_n , are related by the ratio of two integers M and N . From this relationship, the beating period or locking phase of the clocks is used to schedule a precompiled set of valid

and invalid communication clock cycles for transmitting and receiving data between the processing units. Since phase interaction is periodic, this pattern of valid and invalid cycles repeats itself every M clocks for processor M and every N clocks for processor N.”

EX2011

As a result, Pratt exploits this periodicity to precompute a schedule of valid and invalid communication cycles for both the transmitting and receiving systems. Within each beating period, certain transmitter clock cycles are deemed invalid because previously transmitted data has not yet been received, while certain receiver cycles are invalid because the data has not remained stable long enough to satisfy setup and hold time constraints. By using the beating period to predefine these valid and invalid cycles, the system ensures that data transfers occur only during times that are safe from metastability, without requiring asynchronous handshake mechanisms or complex flow control circuitry. Thus, the beating period serves as the core temporal framework around which the entire synchronization method is organized. EX2013, ¶38-39.

Therefore, the “coincidence cycle” described in Sarmenta —referred to as the “beating period” in the corresponding Pratt—requires that the clock frequencies of two systems be related by a rational ratio of integers. This rational relationship ensures that the relative phases of the two clocks realign periodically, creating a repeatable timing interval over which the positions of all clock edges are fixed and

predictable. Within this interval—spanning exactly M clock cycles of one system and N clock cycles of the other—it becomes possible to determine with precision which cycles are safe and which are unsafe for data transfer, based on timing constraints like setup, hold, contamination, and propagation delays. EX2013, ¶40.

This predictable structure enables a powerful result: the system can precompute a schedule of valid and invalid transmission and reception windows because the child clocks will always synchronize at a known point. This avoids metastability and eliminates the need for asynchronous handshaking or dynamic arbitration. Communication can therefore occur deterministically and with high throughput, even between independently clocked systems operating at different speeds. The coincidence cycle, or beating period, thus serves as the enabling mechanism that transforms a traditionally asynchronous problem into a synchronously solvable one, through rational timing and deterministic scheduling. EX2013, ¶41.

3. Chakraborty Confirms That Rational Clocking Systems—Defined by Known Integer Frequency Ratios—Are Fundamentally Distinct from Systems with Arbitrary Clock Frequencies

“[R]ational clocking, that allows data to be transferred reliably and efficiently between two systems whose clock frequencies are related by the ratio of two small integers” was not only explored by Sarmenta and Pratt. EX2004, 1. For example, “Efficient Self-Timed Interfaces for Crossing Clock Domains” by Chakraborty

(“Chakraborty”) describes a system that “take[s] advantage of knowing the exact relationship between the various clocks to implement an interface that operates with low latency and without synchronization.” EX2012, 2.

Specifically, Figure 1(b) (reproduced below), Chakraborty illustrates a chip architecture in which different regions operate at distinct clock frequencies that are rationally related—that is, their frequencies are integer multiples or ratios of one another—and all clocks are derived from a common source. Chakraborty explains that this configuration is typical in system-on-chip (SoC) and multi-rate digital signal processing designs, where different IP blocks are optimized to run at different rates based on performance or power requirements. EX2013, ¶55.

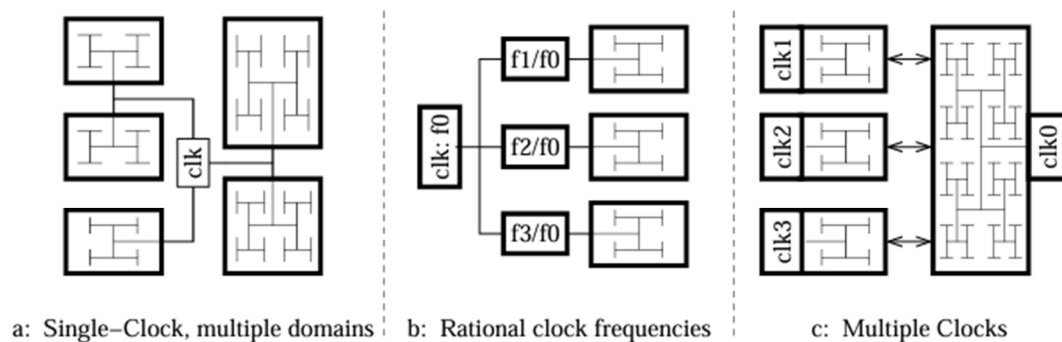


Figure 1. Chips with Multiple Clock Domains

EX2012, 2

Chakraborty expressly states:

Although different domains operate at different frequencies, these frequencies are all rational multiples of each other, and these ratios are typically known in advance or are determined by pre-designed operating

modes of the design. In this case, we can take advantage of knowing the exact relationship between the various clocks to implement an interface that operates with low latency and without synchronization. EX2012, 2.

Chakraborty makes clear that systems that utilize rational clock frequencies are different than systems that use arbitrary frequencies. EX2013, ¶57. Specifically, Chakraborty describes several different, separate approaches:

As described above, we present designs when the sender and receiver operate at exactly the same frequency; **at frequencies that are rational multiples of each other**; at closely matched frequencies; and **at arbitrary, relatively stable frequencies**. EX2012, 2.

To further highlight that systems that utilize rational clock frequencies are fundamentally different than systems that use arbitrary frequencies, Chakraborty contains completely separate sections for “Rational Clock Frequency Multiples” (see EX2012, 6) and “Arbitrary Clock Frequencies” (see EX2012, 9).

Therefore, Chakraborty makes clear that rational clocking systems—where clock frequencies are related by a known ratio of small integers—are fundamentally different from systems that operate with arbitrary or unrelated clock frequencies. In rational clocking, the known relationship between clocks enables the design of interfaces that operate with low latency and without synchronization, leveraging the predictability of clock phase alignment. This stands in contrast to arbitrary clocking

systems, which do not rely on any predefined frequency relationship and therefore must account for unknown or drifting phase differences, typically requiring more complex synchronization mechanisms. Chakraborty expressly distinguishes between these two classes of systems, devoting separate sections of the paper to “Rational Clock Frequency Multiples” and “Arbitrary Clock Frequencies,” thereby underscoring that rational clocking is not simply a special case within a broader asynchronous framework, but rather a distinct and recognized approach that depends on a known, rational frequency relationship between clock domains. EX2013, ¶59.

4. The Claims Exclude Rational Clocking Schemes That Impose Frequency Constraints Disparaged in the Specification

The intrinsic evidence in the ‘443 Patent makes clear that the invention is not merely an incremental improvement on rational clocking schemes, but a departure from them. The specification explicitly disparages synchronization schemes that impose “significant restrictions on the possible choices of frequencies”—a clear reference to rational clocking systems like those described in Sarmenta, Pratt, and Chakraborty. These systems rely on a known, rational frequency ratio between clocks to precompute communication schedules, inherently requiring designers to constrain clock frequencies to maintain a predetermined phase relationship. In contrast, the ‘443 Patent expressly advances a different approach: one that eliminates the need for such constraints and grants each frequency domain independence to

optimize its own tradeoffs. This disavowal of rational clocking is unequivocal and consistent throughout the intrinsic record.

Accordingly, as explained by Dr. Kaeli “a person of ordinary skill in the art would understand the claim language—particularly the phrases “independently of the frequencies” (claims 1 and 12)—to require that each domain’s frequency be selectable and dynamically changeable without being tethered to, derived from, or constrained by the frequencies of other domains.” EX2013, ¶60. Thus, the claim language reciting “for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains” (claim 1) and “dynamically controlling the clock frequency ... in *each* of the plurality of domains *independently* of the clock frequencies” (Claim 12) do not cover synchronized systems like Sarmenta, and Pratt that maintain global synchronization by restricting the possible choice of frequencies to those related by a “rational factor” in order to utilize a “coincidence cycle” for synchronization. EX2013, ¶60.

Instead, as explained by Dr. Kaeli, “and based on the plain and ordinary meaning as understood by a person of ordinary skill in the art, the claims of the ‘443 Patent require that each domain generate its clock signal independently, and that the frequency of each domain’s clock be dynamically changeable without being

constrained by the frequencies of other domains. That is, each domain must be free to generate and change its clock frequency without being tethered to small integer multiples of the other domains.” EX2013, ¶114.

E. The Claims Are Limited To Microprocessors

Claim 1 begins as follows:

A multiple-clock-domain microprocessor comprising:
a plurality of domains; ...

The specification makes clear that the “present invention” is directed to a microprocessor. *See*, EX1001, Title (“Multiple Clock Domain Microprocessor”); 4:14-17 (Summary of the Invention) (“the present invention is directed to a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor ...”). Thus, it is clear that the claims are limited to microprocessors, and that the “plurality of domains” are domains within a microprocessor.

The Petition (at 21) begins its analysis of claim 1 with the statement: “If the preamble is limiting.” Based on the statements in the specification that the invention is directed to a microprocessor, the recitation of a multiple-clock-domain microprocessor is limiting and a requirement of the claim.

VI. THE PETITION FAILS TO DEMONSTRATE ANY OF THE CHALLENGED CLAIMS ARE INVALID

A. Ground 1 Is Deficient

1. Shenai Is Not Prior Art

As explained above, the invention claimed in the ‘443 Patent was conceived and actually reduced to practice by February, 2002. The Petitioner asserts “Shenai was filed 08/12/2002, published 02/13/2003, and is prior art at least under Section 102(e).” Pet., 9. Accordingly, since the August 12, 2002 date asserted by the Petitioner is after February, 2002, Shenai cannot render the claims obvious under 35 U.S.C. §103.

The Petitioner does not allege that the disclosures relied upon in Shenai should be afforded an earlier date. In fact, while Shenai claims priority to Provisional Application Nos. 60/311,575, filed August 10, 2001 (EX2006), 60/337,837, filed November 5, 2001 (EX2007), 60/337,479, filed November 5, 2001 (EX2008) and 60/338,510, filed November 5, 2001 (EX2009) (collectively, the Provisional Applications), the passages from Shenai (EX1004) relied on in the Petition are not entitled to the benefit of the filing date of the Provisional Applications because the subject matter was not disclosed in the manner provided by 35 U.S.C. § 112.

a) Claim 1 Of Shenai Is Unsupported By The Provisional

“A reference patent is only entitled to claim the benefit of the filing date of its provisional application if the disclosure of the provisional application provides support for the claims in the reference patent in compliance with § 112.” *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1382 (Fed. Cir. 2015). Here,

the Petitioner has failed to show that the Provisional Applications support claim 1 (or any other claim).

Claim 1 of Shenai (Ex. 1004) recites in pertinent part,

“a power and clock distribution *controller capable of determining voltage, current and clock signal frequency targets for the plural loads ...*”

The Provisional Application (Ex. 2006) fails to mention a controller that determines current targets for plural loads. Rather, the controller in the Provisional Application only determines voltage and frequency targets. Ex. 2006, 12 (characterizing permitting “combined frequency and voltage scaling,” without mentioning control of current). The Reply (at 2) cites the following from the Provisional Application as allegedly supporting determining current targets:

... Fourth is a controller circuit which dynamically specifies the connections to be made by the cross-bridge network between the power sources and loads. (Ex. 2006, 8)

* * *

[T]o control the cross-bridge network, to specify dynamically the voltage output by each of n power sources, and to specify the clock frequency delivered to each of m load clusters, a dynamic controller is provided. It is envisioned that the dynamic controller will operate with the cooperation of [] power optimization algorithms ... (Ex. 2006, 12) (emphasis added).

* * *

[T]he architecture accommodates ... strategies in the cross-bridge network between the power sources and the load clusters to permit optimization of power, control complexity, or size. (Ex. 2006, 12)

These passages do not disclose determining current targets for plural loads. Rather, the disclosure regarding the determination of current targets was first introduced in Shenai’s utility application, which disclosed in part:

Power and clock distribution controller 450 may be capable of determining voltage, current and clock signal frequency targets for the plural loads. Ex. 1004, [0026] (emphasis added).

... DC/DC converters 470-476 may be responsive to controller 450, such that they are selectively coupled with loads 410-416 to provide the respective target voltages and currents to the loads. *Id.*, [0031] (emphasis added).

Since the Provisional Applications fail to disclose a controller that determines current targets for plural loads, it fails to provide written description support for claim 1 as required by *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1382 (Fed. Cir. 2015); *see also, Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1323 (Fed. Cir. 2000) (to meet the written description requirement, “one skilled in the art, reading the original disclosure, must immediately discern” the material); *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1352 (Fed. Cir. 2010) (*en banc*) (“[A] description that merely renders the invention obvious does not satisfy the [written description] requirement.”)

b) The Provisional Lacks Written Description Support For A Microprocessor

As clarified by the Federal Circuit, “[e]ven if one demonstrates that a provisional application provides written description support for one claim of the non-provisional application or patent, the provisional application must also provide written description support for the specific portions of the patent specification

identified and relied on in the prior art rejection.” *In re Riggs*, 131 F.4th 1377, 1384 (Fed. Cir. 2025)

Claim 1 of the ‘443 Patent recites the domains of a “multiple-clock-domain microprocessor,” and Ground 1 relies solely on Shenai (Ex. 1004) for this aspect of Claim 1. However, the Provisional Application (Ex. 2006) lacks written description support for a microprocessor. The Reply (at 3) argues :

Ex. 2006’s “controller circuit” and power sources “integrated monolithically along with the load clusters using existing integrated circuit (IC) fabrication techniques” would be understood to provide written description for a “microprocessor.”

The Provisional Application does not say that its “controller circuit”/power sources/load clusters are a microprocessor, nor do such components provide inherent support for a “microprocessor.” The Reply does not explain why a controller circuit/power sources/load clusters must be “capable of receiving and executing coded instructions” -- because there is no such requirement.”[W]hen an explicit limitation . . . is not present in the written description whose benefit is sought it must be shown that ... the description requires that limitation.” *Hyatt v. Boone*, 146 F.3d 1348, 1353 (Fed. Cir. 1998) (emphasis added). Here, nothing in the Provisional Application requires that the “load clusters” be a microprocessor.²

² The subsequent utility application, added the loads may comprise other circuitry including “an analog to digital converter utilizing comparators, ... RF power amplifiers, ... LCD displays, TFT displays, ... non-volatile memory units, or circuitry clusters.” Ex. 1004, [0025].

Therefore, the *generic* disclosure of “load clusters” in the Provisional Application fails to provide written description support for a *specific* implementation where the “load clusters” are a microprocessor. See *In re Smith*, 458 F.2d 1389, 1395, (CCPA 1972). (description of a genus failed to support claims to a species within the genus).

As made clear by the Federal Circuit, “to claim priority to provisional filing date, the portion of the application relied on by the [Challenges] as prior art must be supported by the provisional application.” *In re Riggs*, 131 F.4th 1377, 1384 (Fed. Cir. 2025). Since the Petition does not identify how the portion relied upon is supported by the Provisional, Shenai cannot render the Challenged Claims obvious under 35 U.S.C. §103.

2. Ground 1 Is Deficient Because Shenai’s Reliance on Rational Frequency Relationships Fails to Teach or Render Obvious the Independent Clock Frequency Generation Required by the Challenged Claims

Unlike the globally-asynchronous system that is the subject of the ‘443 Patent, both the prior art systems disparaged in the ‘443 Patent and Shenai utilize rational frequency relationships to achieve synchronization. EX1004, ¶0036 (noting that the disclosed configurations may “allow for *synchronous* communication between loads.”) (emphasis added). Specifically, Shenai relies on a “rational factor” relationship, where clock signals are generated as integer or fractional multiples or divisions of a reference clock. Moreover, like prior art systems disparaged in the specification, Shenai imposes significant restrictions on frequency selection—which

the ‘443 Patent disparages. See, Section V (B), *supra*. Shenai’s disclosures failed to provide the independently dynamic frequency control across clock domains required by the Challenged Claims.

The Federal Circuit has held that “[t]he patentee may demonstrate intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.” *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012) (Internal Citation Omitted). In the situation where the inventor’s intention is to disavow the scope, “the inventor’s intention, as expressed in the specification, is regarded as dispositive.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005). For example, “an inventor may disavow claims lacking a particular feature when the specification distinguishes or disparages prior art based on the absence of that feature.” *Poly-America, L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136-37 (Fed. Cir. 2016). In the present case, the specification deliberately and unambiguously disavows an embodiment that imposes a “rational factor” requirement on selection of the frequencies.

The ‘443 Patent states, “[s]ome synchronization schemes restrict the phase relationship and relative frequencies of the clocks, thereby eliminating the need for hardware arbitration [27].” EX1001, 6:33-35. In the ‘443 Patent, citation [27] corresponds to Sarmenta (EX2004). Sarmenta describes an “approach [that]

maintains a known phase relationship between clocks whose frequencies are related by a rational factor, and exploits the predictability of their relative phases to algorithmically time communications without run-time arbitration contests.” EX2004, Abstract.

The “rational factor” in the Paper refers to the relationship between the clock frequencies of two independently clocked digital subsystems. These frequencies are related by the ratio of two integers, (M/N) , where (M) and (N) are small integers. This rational relationship ensures that the clocks align periodically, creating predictable points in time where the active edges of both clocks coincide. EX2013, ¶32.

For example, in Sarmenta, if one clock operates at a frequency (f_m) and the other at (f_n) , their frequencies satisfy the relationship $(f_m/f_n = M/N)$. This periodic alignment allows the system to define a “coincidence cycle,” during which the relative positions of the clock edges are predictable. This predictability is key to scheduling safe and efficient data transfers between subsystems without introducing run-time synchronization delays or relying on more restrictive synchronous designs that demand integer frequency ratios. EX2013, ¶32.

However, as the ‘443 Patent observes when discussing Sarmenta, “these schemes impose significant restrictions on the possible choices of frequencies.” EX1001, 6:35-37. To overcome the limitations of systems like Sarmenta, the ‘443

Patent explains that invention provides “[t]he designers of each domain [to be] no longer constrained by the speeds of critical paths in other domains, affording them greater freedom in each domain to optimize the tradeoffs among clock speed, latency, and the exploitation of application parallelism via complex hardware structures.” EX1001, 2:34-39. Accordingly, while Sarmenta introduces a synchronization approach leveraging rational frequency relationships, it imposes significant restrictions on frequency selection, as acknowledged in the ‘443 Patent. Dr. Kaeli explains, “The ‘443 invention overcomes these limitations, offering independence in clock frequency generation, allowing each frequency domain to adopt their own independent frequency, offering near infinite resolution in terms of the clock frequency selected for each domain.” EX2013, ¶34

The Petitioner’s expert “provided an annotated version of Shenai’s Figure 4 below to assist in illustrating the relationship between the clock/shifters and corresponding loads.” EX1002, ¶110 (a copy of the annotated figure is reproduced below).

“for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains”

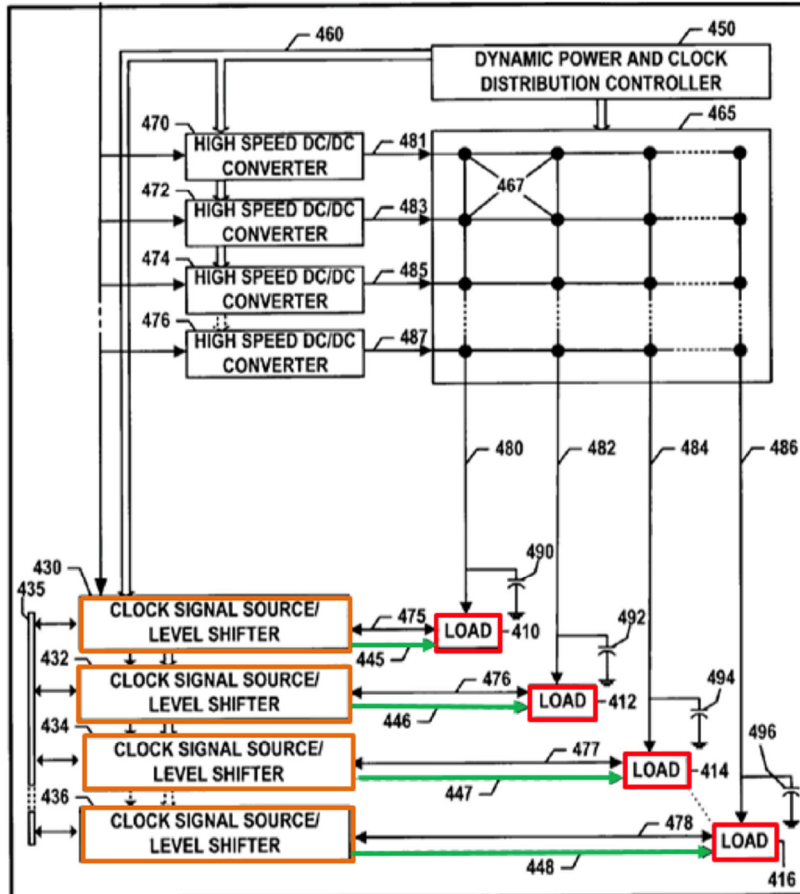


FIGURE 4

Petitioner’s expert further alleged that “[a]s Shenai’s clock/shifter dynamically generates a clock signal for a given load at a frequency based on that load’s respective needs, the clock signal for each load is generated independent of the clock signal for each other load.” EX1002, ¶113.

However, the clocks are not generated independently of the clock signal for each other’s load. Instead, Shenai relies upon Sarmenta’s “rational factor” for

synchronization. As the Petition observes, Shenai describes, “clock/shifters 430-436 may comprise, phase-locked-loop circuits, delay-locked-loop circuits, or combinational logic circuits that generate clock signals for loads 410-416 by, for example, operating at [sic] at an integer multiplication, a half-integer multiplication or a quarter-integer multiplication of a reference clock signal.” Pet., 28.

Specifically, ¶[0036] of Shenai explains:

Additionally, clock/shifters 430-436 may comprise, phase-locked-loop circuits, delay-locked-loop circuits, or combinational logic circuits for supplying clock signals to loads 410-416. These circuits may operate **at an integer multiplication, a half-integer multiplication or a quarter-integer multiplication of a reference clock signal.** Controller 450 may provide the reference clock signal, though the invention is not so limited. Alternatively, these circuits may operate **at an integer division, a half-integer division and a quarter-integer division of the reference clock signal.** Such configurations may allow for synchronous communication between loads 410-416, as opposed to asynchronous communication, which may be undesirable.³

Accordingly, as Dr. Kaeli explains, “[t]he clock frequency control described in Shenai generates a clock frequency that is based on a rational multiple of a reference clock signal.” EX2013, ¶99. Therefore, like in Sarmenta, there is a “rational factor” relationship in Shenai between the clock signal provided to each of the loads that ensures that the clocks align periodically, creating predictable points

³ Shenai’s characterization of systems requiring asynchronous communications as “undesirable” would not motivate a POSITA to implement a globally-asynchronous architecture as required by the Challenged Claims. EX2013, ¶66.

in time where the active edges of both clocks coincide. See, EX1004, [0036] (noting that the disclosed configurations may “allow for synchronous communication between loads.”) (emphasis added). This approach fundamentally contradicts the independence in frequency generation required by the challenged claims. The ‘443 Patent explicitly identifies these limitations and emphasizes that the claimed invention overcomes them by enabling the dynamic and independent generation of clock signals for each domain, unconstrained by the frequencies of other domains. EX1001, 6:34-39 (the invention provides “[t]he designers of each domain [to be] no longer constrained by the speeds of critical paths in other domains, affording them greater freedom in each domain to optimize the tradeoffs among clock speed, latency, and the exploitation of application parallelism via complex hardware structures.”). This freedom is critical to achieving the design flexibility and performance optimization described in the ‘443 Patent. EX2013, ¶34 (“The ‘443 invention overcomes these limitations, offering independence in clock frequency generation, allowing each frequency domain to adopt its own independent frequency, offering near infinite resolution in terms of the clock frequency selected for each domain.”).

As such, the Petitioner has not demonstrated that Shenai discloses or renders obvious the claimed feature of “separately generating a clock signal...the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains.” Therefore, the Petitioner has failed

to meet its burden of proving obviousness for the challenged claims under Ground 1.

B. Grounds 2-4 Are Deficient Because Halepete, Sherburne, and/or Traylor Do Not Cure the Shortcomings of Shenai

The Petition does not allege, nor do Halepete, Sherburne, and/or Traylor, teach, “separately generating a clock signal...the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” as recited in the independent Challenged Claims. Accordingly, the Petitioner has failed to meet its burden with regard to Grounds 2-4 for at least the reasons discussed with regard to Ground 1 above.

C. Ground 5 Is Deficient Because Georgiou’s “Rational Factor” Relationship Fails to Disclose or Render Obvious the Claimed Independent and Dynamically Changeable Clock Frequencies

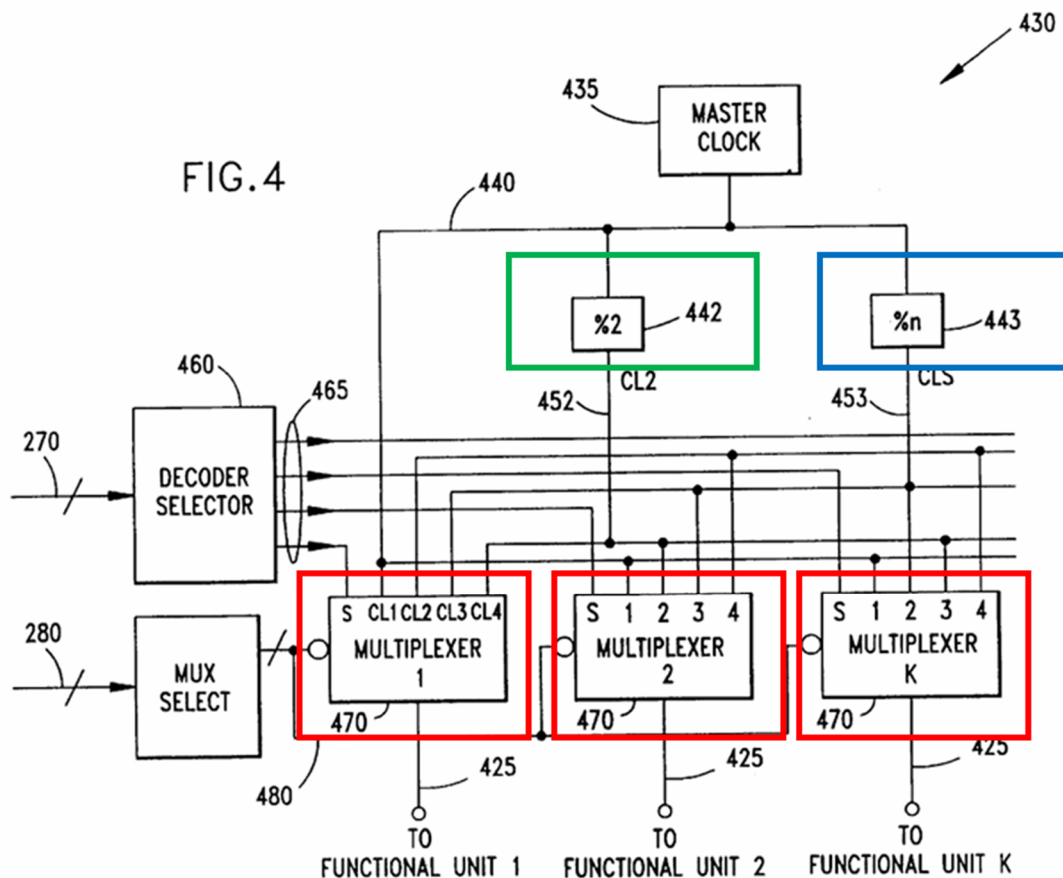
Georgiou discloses a clocking architecture in which all domain clocks are derived from a shared master clock through predetermined rational dividers, inherently imposing interdependent relationships that enable synchronized operation through predictable phase alignment. This structure necessarily imposes a small integer relationship among the domain clocks—precisely the “rational factor” (M/N) criticized in the ‘443 specification and exemplified in Sarmenta and Pratt.

1. The Board Misconstrues Georgiou’s Disclosure by Overlooking the Rational Interdependence Among Domain Clocks Inherent in Its Master-Clock-Derived Architecture

The Board errs in concluding that Georgiou’s Figure 4 fails to show any interdependence between the clock signals of different functional units, asserting that the signals are merely dependent on a shared master clock without implying synchronization across domains. This interpretation overlooks the full import of Georgiou’s disclosure. As detailed below, Georgiou’s clock selector 430—including its clock dividers and multiplexers—imposes a fixed, “rational relationship” (i.e., related by the ratio of two small integers, (M/N)), among those signals by outputting predetermined fractional frequencies (e.g., $\frac{1}{2}$) of a common master clock. This architecture necessarily results in globally synchronized operation across domains, much like the “coincidence cycle” in Sarmenta or the “beating period” in Pratt.

Specifically, the Board stated that “Figure 4 merely shows that clock signals are dependent on [the] master clock, but does not show that the clock signals are dependent on the clock signals of the other functional units (domains).” Institution, 20-21. However, as shown in Figure 4 (annotated below), Georgiou’s clock selector (430) includes clock divider 442, clock divider 443, and multiplexers 470, where the master clock frequency 440 “is used as the common source and provides a common clock reference for a number of clock dividers whose output is some predetermined fraction of the master clock frequency 440.” EX1008, 8:39-42.

This configuration establishes a rational relationship between the clock domains—i.e., their frequencies are small integer-related fractions of the same master frequency—and thereby enables synchronized operation through a predictable phase relationship akin to the “coincidence cycle” described in Sarmenta and the “beating period” in Pratt. EX2013, ¶122.



Georgiou specifically states that “clock divider 442 may be a divide-by-two clock divider whose output frequency 452 is one-half that of the master clock frequency 440, and clock divider 443 may be divide-by-n clock divider whose output

frequency 453 is one-nth that of the master clock frequency 440.” EX1008, 8:42-47.

As Dr. Kaeli explains:

“The purpose of employing clock dividers in this manner is to enable discrete, hardware-efficient scaling of the clock frequency for a functional unit experiencing thermal stress. By selecting from a set of known, reliable frequency levels derived from the master clock, the system avoids the need for dynamically synthesizing new clocks, thereby reducing complexity and ensuring stability.

For example, if the master clock operates at 1 GHz, the system may utilize a divide-by-2 clock divider to output 500 MHz, or a divide-by-4 divider to output 250 MHz. The selected lower-frequency clock is then routed to the overheating functional unit to reduce power dissipation while maintaining synchronization with the rest of the system.

Further, the values of N must be relatively small because taking a large value of 1,000 would result in the 1GHz master clock in the above example outputting a 1 MHz clock which is not useful in a modern computing system.” EX2013, ¶119-121

Therefore, Georgiou requires a predetermined rational factor ($2/n$) between the clock output by clock divider 442 and clock divider 443. However, the specification expressly criticizes such prior art systems, explaining that “some synchronization schemes restrict the ... relative frequencies of the clocks ... [and] impose significant restrictions on the possible choices of frequencies.” EX1001, 6:32–36. The invention of the ‘443 Patent is a deliberate departure from such constrained architectures, and instead permits each domain to operate at a clock

frequency that is both separately generated and dynamically changeable independently of the other domains.

Georgiou fails to meet this limitation. Its clock selector 430 derives all domain clocks from a common master clock using clock dividers (e.g., divide-by-2, divide-by-n), resulting in domain clocks that are predetermined rational fractions of the same source frequency EX1008, 8:39–47. This architecture necessarily imposes a small integer relationship among the domain clocks—precisely the “rational factor” (M/N) criticized in the ‘443 specification and exemplified in Sarmenta and Pratt. The multiplexer 470 cannot select arbitrary or unrelated frequencies, but only from among the constrained outputs of the clock dividers tied to the master clock. EX1008, 8:39–67. As Dr. Kaeli explains, “Georgiou’s architecture allows for discrete scaling from a fixed set of fractional clock outputs, but does not permit domain clocks to be generated independently or to be dynamically varied beyond the bounds of the preselected small integer ratios.” EX2013, ¶95.

Petitioner nonetheless alleges that the output of multiplexer 470 satisfies the “separately generating” and “dynamically changeable independently” language of the Challenged Claims. However, this argument ignores the plain meaning of the claims from the perspective of the specification. The ‘443 Patent does not merely require that different clocks exist—it requires that they be generated independently and that each domain’s frequency be dynamically controllable without regard to the

clock frequencies of other domains. Georgiou's reliance on a common clock source and rational dividers forecloses such independence and dynamic control.

Therefore, contrary to the Board's suggestion, Georgiou does not merely show that domain clocks are dependent on a shared master clock—it expressly discloses a clocking architecture in which all domain frequencies are predetermined fractions of the same global source. By using fixed divide ratios, such as divide-by-2 or divide-by-n, Georgiou enforces rational relationships between clock domains that inherently enable synchronized communication through predictable phase alignment, akin to the “coincidence cycle” of Sarmenta or the “beating period” of Pratt. As Dr. Kaeli explains, “this configuration avoids the complexity of dynamic frequency generation by selecting from a constrained set of precomputed clock values derived from the master clock.” EX2013, ¶120.

Consequently, the Board's conclusion that Georgiou fails to show interdependence among domain clocks overlooks the fundamental structure of Georgiou's architecture, which imposes a rational relationship between clock signals by deriving them as fixed fractional outputs of a shared master clock. This configuration results in synchronized domain clocks whose frequencies are related by a ratio of small integers (M/N), thereby creating a predictable alignment of clock edges over a repeating interval—a structure directly analogous to the “coincidence cycle” described in Sarmenta and the “beating period” in Pratt. These deterministic

timing intervals enable synchronized communication between domains, but they do so by restricting each domain's clock frequency to a fixed rational ratio relative to the master clock. The '443 Patent expressly disclaims such constrained designs, criticizing synchronization schemes that "restrict the relative frequencies of the clocks" and "impose significant restrictions on the possible choices of frequencies." CITE. Properly understood in the context of the '443 Patent, the challenged claims require domain clocks that are generated independently and are dynamically changeable without regard to the frequencies of other domains—free from the small integer dependencies that define coincidence cycle-based systems. Because Georgiou's architecture depends on and exploits these rational phase relationships to enable synchronized communication, it cannot satisfy the limitations of the Challenged Claims.

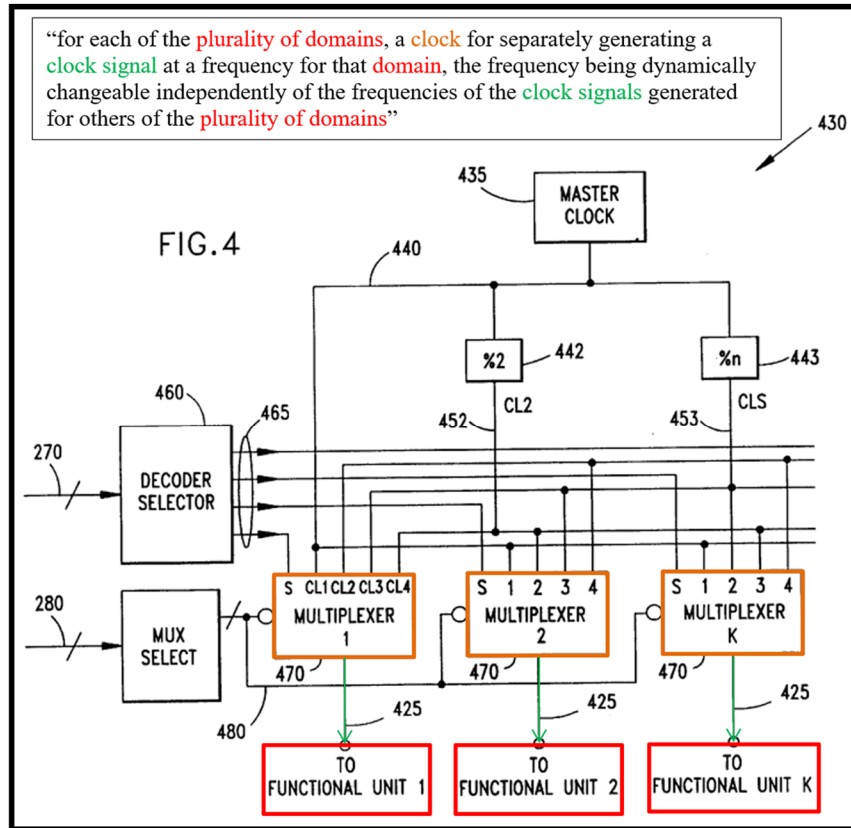
2. Georgiou's Use of a Multiplexer to Select Predetermined Fractions of a Master Clock Fails to Satisfy the '443 Patent's Requirement for Independently and Dynamically Generated Domain Frequencies.

Georgiou's clock selector 430, including multiplexer 470, does not meet the limitations of the challenged claims because it merely selects among predetermined fractions of a master clock, thereby restricting the available clock frequencies to those rationally related to a global source. This structure mirrors the rational clocking schemes criticized in the '443 Patent and exemplified by Sarmenta, Pratt, and Chakraborty, which rely on known integer ratios between frequencies to

maintain synchronization. In contrast, the ‘443 Patent expressly disclaims such constrained architectures and instead requires that each domain generate a clock frequency that is “dynamically changeable independently” of others, free from rational dependencies. Because Georgiou’s multiplexer cannot select an arbitrary or unrelated frequency and instead enforces a predetermined “rational factor” across domains, it falls outside the scope of the properly understood claims and fails to teach or suggest the independent and dynamic frequency generation required by the ‘443 invention.

Georgiou’s clock selector 430 is taught to utilize a multiplexer 470 that “outputs the selected clock frequency which is coupled to the particular functional unit via the appropriate one of paths 425.” EX1008, 8:65-67. As shown in Figure 4, the multiplexers 470 select the clock frequency from among “a number of clock dividers whose output is some predetermined fraction of the master clock frequency 440.” EX1008, 8:39-42. Therefore, multiplexers 470 can only cause Georgiou’s clock selector 430 to output predetermined small integer fractions of the master clock and cannot take a non-predetermined, arbitrary, unrelated value. EX2013, ¶116-117.

As shown below, the Petitioner alleges that the predetermined fractions of the master clock output by the multiplexer 470 is the clock frequency referenced in the challenged claims.



EX1007, 199.

However, the output of the multiplexer 470 does not satisfy the claim language reciting “for each of the plurality of domains, a clock for *separately* generating a clock signal at a frequency for that domain, the frequency being dynamically changeable *independently* of the frequencies of the clock signals generated for others of the plurality of domains” (claim 1) and “dynamically controlling the clock frequency ... in *each* of the plurality of domains *independently* of the clock frequencies” (Claim 12). Instead, Georgiou is describing a synchronized system like Sarmenta and Pratt that maintains global synchronization by restricting the possible choice of frequencies to those related by a “rational factor” (i.e., related

by the ratio of two small integers, (M/N) in order to utilize a “coincidence cycle” for synchronization. EX2013, ¶123-124.

Specifically, in Georgiou’s system, the multiplexer 470 can only select to output a signal that is at some predetermined fraction of the master clock frequency and cannot select any arbitrary value. As Chakraborty makes clear, systems where clock frequencies are related by a known ratio of small integers are fundamentally different from systems that operate with arbitrary or unrelated clock frequencies. (EX2012, 2)

Therefore, Georgiou’s reliance on a master clock and its use of a multiplexer 470 to select among predetermined fractional derivatives of that clock renders it fundamentally incompatible with the independent, dynamically changeable frequency generation required by the challenged claims of the ‘443 Patent. The claims are directed to architectures in which each domain operates at a frequency that is not only separately generated but also dynamically adjustable independent of the frequencies of other domains—a design that eliminates the global constraints imposed by rational clocking schemes. In contrast, Georgiou implements a globally synchronized structure in which all domain clocks remain rationally tied by small-integers divisions of a common source, precisely the type of restriction the ‘443 specification expressly criticizes and disclaims. Because Georgiou’s multiplexer is incapable of producing arbitrary or unrelated frequencies and instead enforces fixed

frequency relationships across domains, it cannot satisfy the limitations of claims 1 or 12, and fails to disclose the claimed invention. EX2013, ¶124

3. Petitioner’s Expert Mischaracterizes the ‘443 Patent by Misreading a Reference to Intra-Domain Clocking as Evidence of Global Synchronization

Petitioner’s expert mischaracterizes the ‘443 Patent by suggesting that its reference to “a single clock” supporting components such as the L2 cache implies a centralized clocking scheme akin to Georgiou’s clock selector 430. However, when read in its full context, the cited passage from the ‘443 Patent makes clear that the invention contemplates five distinct and independent clock domains—including three processor domains, one for the L2 cache, and one for memory—each operating separately. The specification does not suggest, let alone require, that these domains maintain a rational frequency relationship. In contrast, Georgiou explicitly discloses a clocking architecture in which multiple clock signals are derived from a master clock through predetermined dividers, inherently imposing a rational dependency between domain frequencies. Far from supporting the Petitioner’s position, the cited passage from the ‘443 Patent underscores the architectural divergence between the ‘443 invention—which enables each domain to operate at a dynamically changeable and independently generated frequency—and Georgiou’s globally synchronized system.

Specifically, Petitioner’s Expert alleges:

Figure 4 shows a clock selector 430 with a master clock 435 running at a master clock frequency 440 that is used “as the common source and provides a common clock reference for a number of clock dividers[.]” Id. at 8:37-41. This is similar to the ‘443 Patent: “The preferred embodiment uses four domains, one of which includes the L2 cache, so that domains may vary somewhat in size and still be covered by a single clock.” Ex. 1001 at 5:7-9⁴. EX1002, ¶200

However, when read in the full context, the portion of the ‘443 Patent cited by the Petitioner’s expert further highlights the contrast between Georgiou’s clock selector 430 and the present invention.

The ‘443 Patent states:

Matzke has estimated that as technology scales down to a 0.1 μm feature size, only 16% of the die will be reachable within a single clock cycle [24]. Assuming a chip multiprocessor with two processors per die, each processor would need to have a minimum of three equal-size clock domains. The preferred embodiment uses four domains, one of which includes the L2 cache, so that domains may vary somewhat in size and still be covered by a single clock. In effect, we treat the main memory interface as a fifth clock domain, external to the MCD processor, and always running at full speed. EX1001, 5:52-62

Accordingly, the passage describes a system where there are five independent clock domains: 3 for the processors themselves, one for the L2 cache, and one for the memory. The five domains are graphically depicted in Figure 1 (reproduced below) as 110, 120, 130, 140, and 150, respectively. EX2013, ¶125.

⁴ The Expert Declaration appears to contain a typographical error which was propagated into the institution decision. (see Institution, 21)

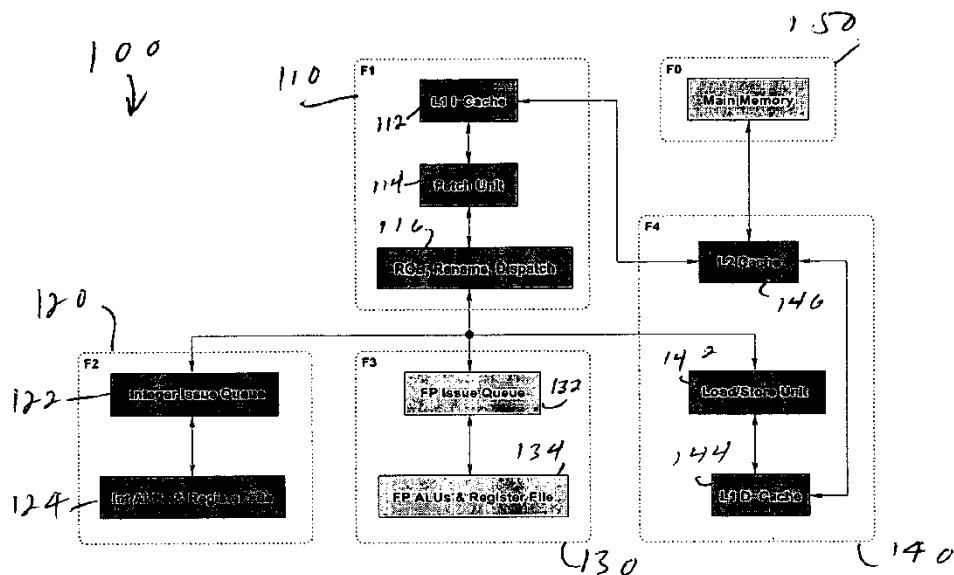


Figure 1

The passage is wholly silent with regard to any relationship between the five independent clock domains. Instead, Petitioner's expert seems to be misunderstanding that components within a given domain (e.g., the L2 cache) utilize the same clock.

As a result, when properly read in context, the '443 Patent describes a system comprising five distinct and independent clock domains—three for processor cores, one for the L2 cache, and one for memory—each capable of operating at its own dynamically changeable frequency. Petitioner's expert mischaracterizes the specification by suggesting that a reference to “a single clock” for components within a domain (e.g., the L2 cache) implies a globally synchronized architecture like that disclosed in Georgiou.

However, the cited passage is silent as to any relationship among the domains and instead confirms their independence. In contrast, Georgiou discloses a clock selector in which all domain clocks are derived from a shared master clock through fixed dividers, resulting in predetermined fractional frequencies that maintain a rational relationship across domains. This global synchronization structure mirrors the rational clocking schemes expressly criticized and disclaimed in the ‘443 Patent. Accordingly, Georgiou cannot meet the claim limitations requiring that, for each domain, the clock be “separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently” (claim 1) and “dynamically controlling the clock frequency ... independently of the clock frequencies” in other domains (claim 12). EX2013, ¶126.

4. Georgiou Fails to Render the Challenged Claims Obvious

When properly understood, Georgiou discloses a centralized clocking scheme fundamentally at odds with the architecture claimed in the ‘443 Patent. All domain clocks in Georgiou are derived from a shared master clock using fixed-ratio dividers (e.g., divide-by-2 or divide-by-n), creating predetermined rational relationships (M/N) among domains to maintain synchronization via predictable phase alignment—akin to the “coincidence cycle” in Sarmenta or the “beating period” in Pratt. The ‘443 Patent expressly rejects such rationally constrained architectures.

This dependency is not incidental but central to Georgiou’s design. The use of fixed dividers and multiplexer 470 limits each domain to a narrow set of outputs tied to the master clock, eliminating the possibility of truly independent or dynamically adjustable clock frequencies. In contrast, the ‘443 Patent requires that each domain generate its own clock signal independently, with frequencies that can be changed without regard to other domains—a key feature enabling the invention’s energy and performance benefits.

The Board’s suggestion that Georgiou does not imply interdependence ignores the structure of its system. Because each divider’s output is mathematically linked to the master clock, all domain clocks are inherently interdependent. This determinism enables synchronization but precludes the autonomy the claims require.

Petitioner’s reliance on the multiplexer as evidence of separate generation is misplaced. Selecting from rationally related options is not the same as independently generating arbitrary frequencies. Nor does the ‘443 Patent’s reference to a “single clock” within a domain—such as the L2 cache—support Petitioner’s centralized interpretation. Read in context, the Patent clearly discloses five distinct, independently controlled domains.

In sum, Georgiou cannot meet the limitations of the challenged claims. Its master-clock-based architecture, rational frequency constraints, and lack of true domain independence place it squarely within the category of prior art disclaimed

by the ‘443 Patent. Petitioner has thus failed to show that Georgiou renders the claims unpatentable.

D. Grounds 6-7 Are Deficient Because Halepete and/or Kranich Do Not Cure the Shortcomings of Georgiou.

The Petition does not allege, nor do Halepete and/or Kranich teach, “separately generating a clock signal...the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” as recited in the independent Challenged Claims. Accordingly, the Petitioner has failed to meet its burden with regard to Ground 6-7 for at least the reasons discussed with regard to Ground 5 above.

VII. SUMMARY OF ARGUMENTS ON THE MERITS

The Petition fails to demonstrate, by a preponderance of the evidence, that any of the challenged claims of the ‘443 Patent are unpatentable. Across all seven asserted grounds, Petitioner mischaracterizes the scope of the claims, overlooks controlling statements in the specification that disclaim particular synchronization techniques, and relies on prior art references that teach away from—rather than toward—the claimed invention. At its core, the ‘443 Patent claims a microprocessor in which each clock domain operates with a separately generated and independently controllable clock signal, free from any constraint imposed by small integer fractions/multiples of other domains. This architectural autonomy—reflected in the

claim language and emphasized throughout the specification—is entirely absent from the systems disclosed in Shenai, Georgiou, and the other cited references.

Grounds 1 through 4 rely on Shenai as the primary reference. However, Shenai is not prior art. As shown by contemporaneous documentation and sworn declarations, the inventors conceived and actually reduced the claimed invention to practice prior to Shenai’s August 2002 filing date. The multiple-clock-domain microprocessor disclosed in the ‘443 Patent was implemented, simulated, and described in detail in a paper published in February 2002. That paper—incorporated by reference into the patent and authored by the named inventors—provides a complete written description of the invention and documents a successful reduction to practice. Shenai, therefore, cannot be used to invalidate the claims under 35 U.S.C. §103.

Even if Shenai were prior art, it fails to teach or suggest the key limitation of “separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others.” Shenai relies on a common reference clock and generates all domain clocks as fixed integer or fractional multiples of that reference. This rational dependency—like those described in Sarmenta and Pratt—imposes significant restrictions on frequency selection and inherently couples the timing of all domains. The ‘443 Patent explicitly criticizes such synchronization schemes and disclaims

them in the specification. The system in Shenai, which achieves synchronization through rational frequency relationships, cannot reasonably be interpreted to support the type of asynchronous, per-domain clock generation required by the claims. Nor do the supplemental references in Grounds 2 through 4 (Halepete, Sherburne, and Traylor) cure this deficiency; none of them disclose independently generated, dynamically adjustable clocks untethered from a shared frequency source.

Grounds 5 through 7 are similarly deficient. In Ground 5, Petitioner relies on Georgiou, which discloses a thermal management scheme where domain clocks are derived from a master clock using fixed divide-by-n ratios and selected by a multiplexer. This architecture enforces a rational, small-integer relationship among clock domains, contrary to the independent and dynamically changeable clocks required by the ‘443 Patent. Because all domain clocks in Georgiou remain tethered to the master clock, frequency changes are limited to precomputed, rationally related values.

The Board’s preliminary view that Georgiou lacks interdependence overlooks that its clocking scheme ensures deterministic phase alignment—akin to the “coincidence cycle” in Sarmenta or “beating period” in Pratt—which the ‘443 Patent expressly criticizes for restricting frequency choice. Georgiou’s use of a multiplexer merely selects among constrained outputs and does not provide true per-domain independence in clock generation.

Petitioner’s attempt to equate this constrained design with the independently controlled domains in the ‘443 Patent is unavailing. The ‘443 Patent repeatedly emphasizes that each domain must be capable of operating with a clock that is both separately generated and dynamically adjustable, without being constrained by the frequencies of other domains. This requirement is not merely a design preference—it is a core feature of the invention and underlies its energy-efficiency and architectural flexibility. The fact that Georgiou allows thermal control through clock selection does not address or overcome the fundamental deficiency: all clocks in Georgiou are rationally tied by a small-integer ratio multiple to a shared master and thus cannot be changed independently.

In sum, Petitioner has failed to show that any of the cited references—either individually or in combination—disclose or render obvious the requirement that each domain in a microprocessor generate its own clock independently and dynamically.

For the above reasons, Patent Owner respectfully requests that the Board fail to find any of the challenged claims invalid.

Respectfully submitted,

Dated: May 9, 2025

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Patent Owner's Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 14,000 words, excluding the parts of this Patent Owner's Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Preliminary Response.

Respectfully submitted,

Dated: May 9, 2025

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CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a copy of the foregoing **PATENT OWNER'S RESPONSE** was served via email (as consented to by counsel) on May 9, 2025 to lead and backup counsel of record for Petitioners as follows:

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