Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.,
Petitioner,

v.

UNIVERSITY OF ROCHESTER
(INTELLECTUAL VENTURES I LLC),
Patent Owner.

Inter Partes Review No.
IPR2024-01225

Patent No. 7,089,443
Filing: January 23, 2004
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PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

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Exhibit 1002	Declaration of R. Jacob Baker, Ph.D., P.E.
Exhibit 1003	Prosecution History of U.S. Patent No. 7,089,443 B2
Exhibit 1004	U.S. Patent Publication No. 2003/0030326 A1 to Shenai *et al.* ("*Shenai")* published on February 13, 2003
Exhibit 1005	International Publication No. WO 01/53921 A1 to Halepete *et al.* ("*Halepete*") published on July 26, 2001
Exhibit 1006	U.S. Patent Publication No. 2002/0169990 A1 to Sherburne ("*Sherburne*") published on November 14, 2002
Exhibit 1007	U.S. Patent No. 5,473,756 to Traylor ("*Traylor*") issued on December 5, 1995
Exhibit 1008	U.S. Patent No. 6,047,248 to Georgiou *et al.* (*"Georgiou*") issued on April 4, 2000
Exhibit 1009	International Publication No. WO 01/33352 A1 to Kranich *et al.* ("*Kranich*") published on May 10, 2001
Exhibit 1010	Webpage for Datamath Calculator Museum - archived by WayBackMachine on February 26, 2001 ("*Datamath*")
Exhibit 1011	Stanley Mazor, *The History of the Microcomputer – Invention and Evolution* (1995) ("*Mazor*")
Exhibit 1012	William M. Johnson, *Super-Scalar Processor Design*, (1989) ("*Johnson*")
Exhibit 1013	Altera, *Excalibur Arm-Based Hardware Reference Manual*, January 2001 ("*Excalibur*")
Exhibit 1014	Texas Instruments, *TMS320C64x Technical Overview*,

	January 2001 ("*TMS*")
Exhibit 1015	Kenneth C. Yeager, *The MIPS R100 Superscalar Microprocessor,* (1996) ("*Yeager*")
Exhibit 1016	Texas Instruments, *FIFO Architecture, Functions, and Applications*, November 1999 ("FIFO")
Exhibit 1017	Eric Tune *et al.*, *Dynamic Prediction of Critical Path Instructions,* (2001) ("*Tune*")
Exhibit 1018	U.S. Patent No. 6,289,465 B1 to Kuermerle ("*Kuermerle*") issued on September 11, 2001
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Exhibit 1021	Bruce R. Childers *et al.*, *Adapting Processor Supply Voltage to Instruction-Level Parallelism*, (2001) ("*Childers*")
Exhibit 1022	Andrew Royal *et al.*, *GALS, Globally Asynchronous, Locally Synchronous Systems*, April 27th, 2001 ("*GALS*")
Exhibit 1023	U.S. Patent No. 6,141,762 to Nicol *et al.* issued on October 31, 2000 ("*Nicol*")
Exhibit 1024	*Reserved*
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Exhibit 1026	Actel Corporation, *3200DX Dual-Port Random Access Memory (RAM)*, September 1997 ("*3200DX*")
Exhibit 1027	Barr Group, *Types of Memory in Embedded Systems*, May 1, 2001

Exhibit 1028	Wavecrest corporation, *Understanding Jitter*, 2001
Exhibit 1029	U.S. Application No. 60/441,759 filed January 23, 2003
Exhibit 1030	U.S. Patent No. 7,739,537 to Albonesi *et al.* ("*Albonesi"*) issued on June 15, 2010
Exhibit 1031	Declaration of Ankit Aggarwal
Exhibit 1032	Declaration of R. Jacob Baker, Ph.D., P.E.
Exhibit 1033	Transcript of Cross-Examination of Dr. David Kaeli
Exhibit 1034	R. Jacob Baker et al., *CMOS Circuit Design, Layout, and Simulation*, 1998
Exhibit 1035	Graf, *Modern Dictionary of Electronics*, Seventh Ed., Aug. 11, 1999
Exhibit 1036	T. Burd et al, *A Dynamic Voltage Scaled Microprocessor System*, IEEE J. Solid-State Circuits, vol. 35, no. 11, pp. 1571-1580, 2000 ("Burd")

I. INTRODUCTION

The Petition provides detailed reasons, supported by evidence, that show how the challenged claims 1 and 3-12 of the ’443 patent would have been either anticipated or rendered obvious to a person of ordinary skill in the art (“POSITA”). None of Patent Owner’s arguments are supported by evidence and therefore fail to adequately refute the Petition. As discussed below, Patent Owner’s substantive arguments rely on an incorrect claim construction. Since Patent Owner has not presented alternative arguments for all the claims of the ’443 patent without applying its proposed claim construction, Patent Owner cannot succeed if the proposed claim construction is not adopted. Further, Patent Owner’s attempt to “swear behind” the *Shenai* reference (Ex. 1004) fails because the SimpleScalar simulation is not a reduction to practice. *Shenai* is entitled to the priority date of the provisional application which it claims benefit to. Accordingly, *Shenai* is prior art to the ’443 patent, and as laid out in the Petition, renders obvious the challenged claims of the ’443 patent. *Georgiou* provides an additional, overlapping challenge to claims of the ’443 patent and also renders the challenged claims obvious. Thus, the Board should thus find the challenged claims unpatentable in the final written decision.

II. CLAIM CONSTRUCTION

The Petition established that no construction of the claims is necessary to assess whether the prior art reads on the Challenged Claims. Paper 1, 20-21; *see also* Ex. 1002, ¶32. The Board correctly declined to construe the claims of the '443 patent in the Institution Decision. *See* Paper 11, 8-9. The record does not support a different result in the final written decision.

Patent Owner's obviousness arguments depend on an improper claim construction that relies on extrinsic evidence and excludes the preferred embodiment of the '443 patent. In particular, Patent Owner proposed narrowing the claims of the '443 patent by "requir[ing] that each domain generate its clock signal independently, [] that the frequency of each domain's clock be dynamically changeable without being constrained by the frequencies of other domains" and that "each domain must be free to generate and change its clock frequency without being tethered to small integer multiples of the other domains." Paper 14, 22. This claim construction represents a significant narrowing of the actual claim language reciting "the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains." Ex. 1001, 17:13-15 (claim 1).

A. Patent Owner's Claim Construction Is Based Entirely on Extrinsic Evidence and Ignores the Claims and Specification.

Neither the actual claim language nor the specification supports Patent

Owner's claim construction. See *Phillips v. AWH Corp*., 415 F.3d 1303, 1306 (Fed. Cir. 2005) ("the words of the claims themselves ... define the scope of the patented invention"); *Leibel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 904 (Fed. Cir. 2004) ("Claims must be read in view of the specification …. On the other hand, it is improper to read a limitation from the specification into the claims."). First, Patent Owner's proposed construction that "**each domain generate its clock signal** independently" is technically inaccurate and does not track the claim language. Paper 14, 22 (emphasis added).

Instead, the claims recite "for each of the plurality of domains, **a clock for separately generating a clock signal** at a frequency for that domain …". Ex. 1001, 17:11-13 (claim 1) (emphasis added). A domain itself does not "generate a clock signal," independently or otherwise. *See* Ex. 1033, 22:6-13 (Dr. Kaeli agreeing that "the domain includes a clock for separately generating a clock signal at a frequency for that domain.").

Similarly, the claim language does not support the requirement that "each domain must be free to generate and change its clock frequency without being tethered to small integer multiples of the other domains." Paper 14, 22; Ex. 1032, ¶8. As discussed above, a domain is not "free to generate and change its clock frequency" according to the claim language. Further, language excluding domains "being tethered to small integer multiples of the other domains" is nowhere to be

found in the claims of the ’443 patent. Instead, this language is based on extrinsic evidence. *See* Ex. 1033, 36:18-23 (“that particular language in my declaration is specific for how the prior art developed supported multiple clock domains”).

Support for Patent Owner’s construction is also absent from the specification of the ’443 patent. Ex. 1033, ¶¶8-9. The specification does not include any discussion of “integer multiples” of frequencies in any context, much less restricting domains “being tethered to small integer multiples of the other domains.” *Compare* Paper 7 *with* Ex. 1001. Instead, Patent Owner’s claim construction appears to be based on a single paragraph of the ’443 patent referring to preexisting “synchronization schemes [that] restrict the phase relationship and relative frequencies of the clocks,” which cites to the Sarmenta Paper (Ex. 1004). Paper 14, 23 (*citing* Ex. 1001, 6:32-42). This disclosure (including the Sarmenta Paper) does not describe how these synchronization schemes “restrict the phase relationship and relative frequencies” with any specificity, and would not inform a POSITA to specifically read “small integer relationships among the domain clocks” from out of the ’443 claims. Ex. 1032, ¶8.

The other references that Patent Owner relies on for support for this claim construction, namely the Pratt Paper (Ex. 2011) and the Chakraborty Paper (Ex. 2012), are not cited in the ’443 patent and, at best, represent extrinsic evidence. Ex. 1033, 59:17-19.

Thus, the Board correctly declined to construe the claims of the ’443 patent in the Institution Decision and should again reject Patent Owner’s construction.

B. Patent Owner’s Claim Construction Is Not Compatible with the Preferred Embodiment of the ’443 Patent.

Patent Owner’s claim construction excludes the preferred embodiment of the ’443 patent by “requir[ing] that each domain generate its clock signal independently,” and assigning independent “globally-asynchronous” clocks to each domain. Paper 14, 20, Ex. 1033, 25:16-18 (“The ’443 patent describes how each domain has … a separate clock at its own frequency, and also an associated voltage.”). The preferred embodiment of the ’443 patent itself does not have this architecture. Instead, the first paragraph under the heading “DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT” of the ’443 patent states: **“[t]he preferred embodiment** uses **four domains** […] so that domains may vary somewhat in size and still be **covered by a single clock**.” Paper 1, 40, Ex. 1001, 5:57-59; Ex. 1032, ¶9 (emphasis added). The ’443 patent touts the benefit of this configuration, stating that its “global clock distribution network is greatly simplified, requiring only the distribution of the **externally generated clock** to the local Phase Lock Loop (PLL) in each domain.” Ex. 1001, 4:25-28 (emphasis added). Thus, the preferred embodiment of the ’443 patent relies on a **single external master clock** that distributes a signal to the local PLL of each domain. Ex. 1032, ¶9. Accordingly, a POSITA would not have interpreted the

claims according to this claim construction. Ex. 1032, ¶9. "A [claim] construction that excludes the preferred embodiment 'is rarely, if ever, correct and would require highly persuasive evidentiary support.'" *Starhome GMBH v. AT&T Mobility LLC*, 743 F.3d 849, 857 (Fed Cir. 2014) (*citing Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996)). Patent Owner's reliance on extrinsic evidence cannot overcome this flaw in its construction. *Id*.

For this additional reason, Patent Owner's proposed claim construction is overly narrow and should be rejected.

III. *SHENAI* IS PRIOR ART TO THE '443 PATENT.

Patent Owner's attempt to swear behind *Shenai* (Ex. 1004) fails for two independent reasons: (1) Patent Owner has provided no evidence of an actual reduction to practice; and (2) *Shenai* predates the alleged conception and alleged reduction to practice by virtue of its priority claim.

A. The SimpleScalar Simulation Was Not a Reduction to Practice.

Even if the multiple clock domain microarchitecture was simulated as described in the Semeraro Paper (Ex. 2005), there is no evidence that any claim of the '443 patent was ever embodied in tangible form. As Patent Owner correctly recognizes, "[r]eduction to practice in the United States requires that the invention be embodied in tangible form." *Scott v. Koyama*, 281 F.3d 1243, 1247 (Fed. Cir. 2002); *see* Paper 14, 5.

Every challenged claim is directed to either a "microprocessor" or a "method of operating a microprocessor." Ex. 1001, 17:9-18:36 (claims 1, 3-12). Dr. Kaeli admitted that a microprocessor is a physical item. Ex. 1033, 83:21-84:4. Yet Patent Owner has presented no evidence and has not alleged that any physical microprocessor was ever produced or operated. *See* Paper 14, 15-17. Instead, Patent Owner relies on an alleged computer simulation of a microprocessor, "[t]he whole purpose" of which "is to avoid the cost of going through the fabrication process each time, which is both time-consuming and very expensive." *See* Paper 14, 15-17; Ex. 1033, 88:2-7. Dr. Kaeli confirmed that SimpleScalar was not used to fabricate anything, including a microprocessor. Ex. 1033, 88:11-23.

Simulations of the kind Patent Owner relies on for reduction to practice would have occurred before any physical prototyping in the circuit design process. Ex. 1032, ¶14-17. Only after a simulation showed feasibility might a physical prototype be fabricated. Ex. 1032, ¶¶10-18; Ex. 1033, 88:2-7; Ex. 1034, 26. The particular simulation Patent Owner relies on was supposedly generated by SimpleScalar, which was not industry standard. Ex. 1032, ¶¶12-13. The SimpleScalar simulation would have had limited value on its own because the simulation's accuracy would have had to be validated against a physical prototype. Ex. 1033, 103:23-105:1. Patent Owner has produced no evidence of any physical prototype of the claimed microprocessor that could have validated the simulation.

See Paper 14, 15-17. At most, the alleged SimpleScalar simulation demonstrated feasibility for prototyping of a microprocessor. *Standard Mfg. Co. v. United States*, 25 Cl. Ct. 1, 67 (1991) ("The feasibility of the optical alignment system may have been proven by the optical mock-up, but the optical mock-up was not a reduction to practice of the proposed MHU–145/M trailer.")

Patent Owner's reliance on *In re Beauregard* is misplaced. *See* Paper 14, 5, 17. *Beauregard* clarified that "computer programs embodied in a tangible medium, such as floppy diskettes, are patentable subject matter." 53 F.3d 1583, 1584 (Fed. Cir. 1995). *Beauregard* did not suggest that computer code can qualify as a tangible embodiment of a claim for a physical object or that computer code can qualify as a reduction to practice for a physical object. *See Beauregard*, 53 F.3d at 1584.

Patent Owner has therefore failed to prove a reduction to practice. For this reason alone, *Shenai* is not antedated and qualifies as prior art to the '443 patent.

B. *Shenai* Is Entitled to the August 10, 2001, Priority Date.

If the Board finds that the SimpleScalar simulation was a reduction to practice—it was not—*Shenai* still predates Patent Owner's alleged February 2002 critical date. *Shenai* properly claims priority under §119(e) to provisional App. No. 60/311,575 (Ex. 2006), which was filed on Aug. 10, 2001. *Shenai* was filed "not later than 12 months" after Ex. 2006 (noting per §119(e)(3) that Aug. 10, 2002,

was a Saturday and *Shenai* was filed on Monday) and *Shenai* explicitly claims priority to Ex. 2006. Both *Shenai* and Ex. 2006 identify Krishna Shenai as an inventor. As discussed in detail hereinafter, the priority claim is perfected because the "provisional application provides written description support for" *Shenai*'s claim 1 and "provide[s] written description support for the specific portions of the patent specification identified and relied on." *In re Riggs*, 131 F.4th 1377, 1384 (Fed. Cir. 2025); *see also Dynamic Drinkware v. Nat'l Graphics, Inc.* 800 F.3d 1375, 1380 (Fed. Cir. 2015).

1. Ex. 2006 Supports Claim 1 of *Shenai*.

The parties only dispute whether Ex. 2006 provides support for a "controller **capable** of determining […] **current** […] targets" as recited in *Shenai* claim 1. Ex. 1004, claim 1 (emphasis added); *compare* Paper 10, 1-2 *with* Paper 14, 38-40. There is no dispute that Ex. 2006 supports all other elements of claim 1, including a "controller capable of determining voltage […] and clock signal frequency targets." *Id.*

Patent Owner argues that Ex. 2006 "fails to mention a controller that determines *current* targets for plural loads." Paper 14, 39 (emphasis in original). Claim 1 of *Shenai*, however, does not require a controller that affirmatively determines current targets. Claim 1 instead recites a "controller **capable** of determining voltage, current and clock signal frequency targets." Ex. 1004, 11

(claim 1) (emphasis added). Claim 1 therefore requires only a controller that could determine current targets; the controller need not actually determine current targets. *See Intel Corp. v. U.S. Int'l Trade Comm'n*, 946 F.2d 821, 832 (Fed. Cir. 1991).

Ex. 2006 supports a controller **capable** of determining current targets. Ex. 2006 describes a "dynamic controller" that is provided to "specify dynamically the voltage output by each of *n* power sources, and to specify the clock frequency delivered to each of *m* load clusters." Ex. 2006, 12. Patent Owner admits that this "controller in [Ex. 2006] determines **voltage** and **frequency** targets." Paper 14, 39 (emphasis in original). There is therefore no dispute that the Ex. 2006 controller is **capable** of determining voltage and frequency targets. The Ex. 2006 controller is equally *capable* of determining other parameter targets, including current targets, and a POSITA would have understood as much from the text. Ex. 1032, ¶¶22-23. A POSITA, moreover, would have recognized based on the controller described in Ex. 2006 that *Shenai*'s inventors possessed a controller capable of determining current targets, as recited in *Shenai* claim 1. Ex. 1032, ¶¶22-23. No more is required for Ex. 2006 to support *Shenai* claim 1. *See Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc) ("[W]ritten description support" requires that the disclosure "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as

of the filing date.")

2. Ex. 2006 Supports a Microprocessor.

Patent Owner argues that because Ex. 2006 does not explicitly use the word "microprocessor" to describe its architecture, Ex. 2006 does not support *Shenai*'s use of the term. Paper 14, 40-42. Patent Owner's argument relies on a misconception of the written description requirement and ignores the content and context of Ex. 2006.

To satisfy the written description requirement, "the prior application need not describe the claimed subject matter in exactly the same terms as used in the claims; it must simply indicate to persons skilled in the art that as of the earlier date the applicant had invented what is now claimed." *Eiselstein v. Frank*, 52 F.3d 1035, 1038 (Fed. Cir. 1995). "The failure of the specification to specifically mention a limitation that later appears […] is not a fatal one when one skilled in the art would recognize upon reading the specification that the new language reflects what the specification shows has been invented." *All Dental Prodx, LLC v. Advantage Dental Prods., Inc.*, 309 F.3d 774, 779 (Fed. Cir. 2002).

Ex. 2006 is squarely directed to microprocessor architecture. As set forth in Petitioner's Preliminary Reply (Paper 10), a microprocessor is "an electronic integrated circuit, typically a single-chip package, capable of receiving and executing coded instructions." Ex. 1035, 6; Ex. 1032, ¶26. Ex. 2006 describes

arrangement of its architecture on an integrated circuit, explaining that the "architecture is constructed such that a system (e.g. a complex IC or an electronics system is partitioned into *m* load clusters." Ex. 2006, 11; Ex. 1032, ¶25. Ex. 2006 further describes power sources "integrated monolithically along with the load clusters using existing integrated circuit (IC) fabrication techniques." Ex. 2006, 11; Ex. 1032, ¶25. Patent Owner does not dispute that Ex. 2006 describes an integrated circuit. *See* Paper 14, 41-42.

Ex. 2006 also describes a "controller circuit," or "dynamic controller," provided to "control the cross-bridge network, to specify dynamically the voltage output by each of *n* power sources, and to specify the clock frequency delivered to each of *m* load clusters." Ex. 2006, 10, 12. Ex. 2006 specifies that the "dynamic controller will operate with the cooperation of scheduling software, operating system prioritization, or dynamic performance and power optimization algorithms." Ex. 2006, 12. A POSITA would have recognized when reading Ex. 2006 that at least the dynamic controller portion of the architecture would necessarily be "capable of receiving and executing coded instructions" to function with software, an operating system, and/or algorithms. Ex. 1032, ¶27.

A POSITA would have also recognized from Ex. 2006's background and statement of the problem addressed that Ex. 2006 describes a microprocessor. Ex. 1032, ¶¶28-29. Ex. 2006 describes minimizing power consumption while

maintaining performance in electronic systems using voltage scaling and/or frequency scaling. Ex 2006, 8-9. Describing the state of the art, Ex. 2006 specifically references a previous scaling technique developed by Thomas D. Burd and described in an IEEE paper titled "A Dynamic Voltage Scaled Microprocessor System."[1] Ex. 2006, 9; Ex. 1036. A POSITA would have concluded based on the recognition of Burd's earlier microprocessor work that Ex. 2006 would also be directed to microprocessor technology and describe a microprocessor. Ex. 1032, ¶28.

Patent Owner has provided no competing definition of a microprocessor, no evidence of what a microprocessor is, and no evidence of how a microprocessor could differ from what is described in Ex. 2006. *See* Paper 14, 40-42. Patent Owner's argument that a microprocessor is somehow unsupported by Ex. 2006 should therefore be rejected.

IV. THE CHALLENGED CLAIMS ARE OBVIOUS OVER *SHENAI.*

A. Patent Owner's Arguments Fail Because *Shenai* Discloses the Same Clock Architecture as the '443 patent.

Patent Owner argues that "Shenai relies on a 'rational factor' relationship … [and] failed to provide the independently dynamic frequency across clock domains

[1] The '443 Patent also cites an article by Burd titled "The Simulation and Evaluation of Dynamic Voltage Scaling Algorithms." Ex. 1001, 11.

required by the Challenged claims." Paper 14, 42-43. However, *Shenai* discloses a master clock with Phase Locked Loops in each domain in the same way as the preferred embodiment of the '443 patent. *See* Ex. 1001, 4:25-28, 5:57-59; Ex. 1004, 10; Ex. 1032, ¶31.

As discussed in the Petition, *Shenai* describes a microprocessor operating a plurality of loads at a plurality of independent frequencies and voltages. Paper 1, 39; Ex. 1002, ¶¶133-141; Ex. 1004, 9; Ex. 1032, ¶30. In particular, *Shenai*'s clock/shifters 430-436 provide signals separately to domains (*i.e*., loads 410-416) which function at frequencies dynamically changeable independently of other domains. Ex. 1032, ¶30; Ex. 1004, 9, 11. *Shenai*'s loads are disclosed as "individual components, functional blocks of a single component[,] or independent systems." Paper 1, 39; Ex. 1032, ¶30; Ex. 1004, 9. *Shenai* explicitly discloses independence between frequencies in each load: "each load of a partitioned (or dynamically partitioned) complex electronic system may function at voltage and frequency values that allow the load to realize [] power savings." Paper 1, 39; Ex. 1004, 11; Ex. 1032, ¶30.

Shenai also discloses that "clock/shifters 430-436 may comprise, **phase-locked-loop** circuits, delay-locked-loop circuits, or combination logic circuits for supplying clock signals to loads 410-416", similar to the architecture of the '443 patent. Ex. 1001, 4:25-28, 5:57-59; Ex. 1004, 10; Ex. 1032, ¶31. As discussed

above, the preferred embodiment of the '443 patent relies on a single external master clock that distributes a signal to the local PLL of each domain. *See* Ex. 1001, 4:25-28, 5:57-59; Ex. 1032, ¶31. The fact that *Shenai* and the '443 patent include the same type of timing architecture with a master clock and PLL in domains directly contradicts Patent Owner's arguments that "Shenai's disclosures failed to provide the independently dynamic frequency control across clock domains required by the Challenged Claims." Paper 14, 43; Ex. 1032, ¶31.

B. *Shenai*'s Domains Are Not Interdependent.

Patent Owner's arguments also fail when applied to embodiments of *Shenai* where clock/shifters 430-436 operate "at an integer multiplication, a half-integer multiplication or a quarter-integer multiplication of a reference clock signal." Ex. 1001, 28; Ex. 1004, 10; Ex. 1032, ¶32. Generation of clock signals using a master clock (*e.g.*, related at integer or sub-integer multiplication) does not impact the dependence of clock signals between various domains. *See* Paper 11, 20-21; Ex. 1032, ¶32. In particular, Patent Owner has not shown that integer or sub-integer relationships between reference clock signals imparted to different loads has any impact on frequencies being "dynamically changeable" or independent from other loads. *See* Ex. 1004, 9-11; Ex. 1032, ¶32.

Likewise, Patent Owner's argument that *Shenai*'s "multiplexer 470 limits each domain to a narrow set of outputs" has nothing to do with interdependence of

domains. Paper 14, 47-48; Ex. 1032, ¶33. That is, Patent Owner does not support an argument that a possible range of frequencies impacts independence between domains. Paper 14, 47-48; Ex. 1032, ¶33. To the contrary, *Shenai* teaches that even when clock/shifters 430-436 operate at some integer multiple of a reference clock signal, its loads are dynamically changeable and independently "function at voltage and frequency values that allow the load to realize [] power savings." Ex. 1001, 39; Ex. 1004, 11; Ex. 1032, ¶33.

Thus, as laid out in the Petition, *Shenai* teaches all the elements of independent claim 1, including "for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains." Paper 1, 21-29; Ex. 1032, ¶34. Patent Owner has not made any independent arguments regarding claims 3-12, which are obvious over *Shenai* alone and in view of *Halepete*, *Sherburne*, and *Traylor* as laid out in the Petition. Paper 1, 21-61.

Accordingly, all of the challenged claims are obvious in view of *Shenai* alone and in view of *Halepete*, *Sherburne*, and *Traylor*.

V. THE CLAIMS ARE OBVIOUS OVER *GEORGIOU*.

A. The Board Correctly Determined that *Georgiou*'s Clock Architecture Does Not Limit Independence Between Domains.

In the Institution Decision, the Board correctly rejected Patent Owner's

argument that *Georgiou*'s "clock signals generated based on *a master clock* are not generated independently of the clock signals generated *for others of the plurality of domains*." Paper 11, 20 (emphasis original). Patent Owner rehashed essentially the same arguments in its Response, arguing that *Georgiou*'s architecture "does not permit domain clocks to be generated independently or to be dynamically varied beyond the bounds of the preselected small integer ratios." Paper 14, 53. The Board should reject these arguments because *Georgiou*'s domain clocks are independent. Paper1, 69; Ex. 1008, 12.

As explained in the Petition, *Georgiou* teaches a thermal feedback system which allows for varying the voltage and operating frequency of functional units (*i.e.*, domains) to control heating. Paper 1, 70; Ex. 1008, 9; Ex. 1032, ¶35. *Georgiou* teaches a master clock connected to multiplexors 470 which each independently "output [a] selected clock frequency which is coupled to the particular functional unit." Paper 1, 69; Ex. 1008, 12; Ex. 1032, ¶35. These clock signals are provided to each functional unit independent of the other clock signals and are dynamically changeable depending on the individual needs of each functional unit at a given time. Paper 1, 69; Ex. 1008, 12; Ex. 1032, ¶35.

As the Board previously stated, *Georgiou* "shows that clock signals are dependent on master clock, but does not show that the clock signals are dependent on the clock signals of the other functional units (domains)." Paper 11, 20-21; Ex.

1008, 6 (Fig. 4), 12; Ex. 1032, ¶36. That is, Patent Owner has not established that independence between domains is limited by a possible number of frequencies. Ex. 1032, ¶36. Patent Owner has also failed to show how Georgiou's architecture limits the range of possible frequencies. Ex. 1032, ¶37.

B. *Georgiou*'s Clock Architecture Allows for Independence Between Domains Just as the '443 Patent's Clock Architecture.

Patent Owner also argued that "the Board's conclusion that *Georgiou* fails to show interdependence among domain clocks overlooks the fundamental structure of Georgiou's architecture, which imposes a rational relationship between clock signals by deriving them as fixed fractional outputs of a shared master clock." Paper 14, 54. This statement is incorrect as the Board did not find that *Georgiou* fails to show interdependence among domain clocks. To the contrary, the Board found Dr. Baker's statement persuasive that "not only are [*Georgiou*'s] clock signals provided independent from the other generated clock signals, but the clock signals are also dynamically changeable depending on the individual operating conditions of each functional unit at a given time." Paper 11, 21, (*citing* Ex. 1002, ¶¶197-210); Ex. 1032, ¶35. The Board should maintain this decision in the final written decision because *Georgiou*'s timing architecture provides for independent domains just as the timing architecture of the '443 patent.

Patent Owner attempts to distinguish the '443 patent as a "deliberate departure from such constrained architectures," referring to *Georgiou*. Paper 14,

52. This argument ignores the similarities between the clock architectures of the '443 patent and *Georgiou*. Ex. 1001, 4:25-28, 5:57-59; Ex. 1008, 12; Ex. 1032, ¶36. As discussed above, the '443 patent teaches that a single external master clock distributes a signal to the local PLL of each domain. Ex. 1001, 4:25-28, 5:57-59; Ex. 1032, ¶36. *Georgiou* similarly teaches a master clock connected to multiplexors 470, which each independently "output [a] selected clock frequency which is coupled to the particular functional unit." Paper 1, 69; Ex. 1008, 8:61-67; Ex. 1032, ¶36. While *Georgiou*'s clock dividers can manipulate the master clock frequency by an integer value, such as divide-by-2 or divide-by-n, this does not limit the independence of the functional units with respect to other clock signals. Paper 1, 69; Ex. 1008, 9; Ex. 1032, ¶36. In *Georgiou*'s scheme and the '443 patent alike, "the clock signals are dynamically changed depending on the individual needs of each functional unit (domain) at a given time." Paper 1, 69; Ex. 1002, ¶¶197-201; Ex. 1032, ¶36. Thus, the domains in both *Georgiou* and the '443 patent receive clock signals from a single master clock and function independently of each other. Ex. 1032, ¶36.

Further, Patent Owner has not substantiated its arguments that *Georgiou*'s architecture imposes a "coincidence cycle" or "beating period" between domains which "impose[s] significant restrictions on the possible choices of frequencies." Paper 11, 54-55; Ex. 1032, ¶37. First, these arguments discount the need for all

domains—including those in the ’443 patent—to be synchronized at some time to provide for communications. *See* Ex. 1001, 4:19-20 (discussing “synchronizing circuits [that] ensure reliable inter-domain communication”). The synchronization of domains necessarily requires alignment between the timing of different domains. Ex. 1001, 4:51-56; Ex. 1032, ¶37. However, this requirement for alignment to communicate is not related to the independence of the domains. Ex. 1032, ¶37. That is, the alignment between domains in both *Georgiou* and the ’443 patent can be selected to occur at various times, according to the requirements of the circuit. Ex. 1032, ¶37.

Last, Patent Owner has not substantiated in any way the “significant restrictions on the possible choice of frequencies” allegedly caused by *Georgiou*’s architecture. Paper 11, 54; Ex. 1032, ¶38. First, frequency choice is not related to the independence of domains. Ex. 1032, ¶38. Second, *Georgiou*’s functional units are completely independent of the others such that “each functional unit may be operating under a different voltage 325 and frequency 425 combination according to the thermal feedback from its associated thermal sensor 119.” Paper 1, 67; Ex. 1008, 11; Ex. 1032, ¶38. In this way, *Georgiou*’s timing architecture does not pose any significant restrictions on the possible choice of frequencies. Ex. 1032, ¶38.

Accordingly, the Board correctly recognized “that *Georgiou* teaches ‘for each of the plurality of domains, a clock for separately generating a clock signal at

a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains.'" Paper 11, 21. None of Patent Owner's arguments compel a different finding.

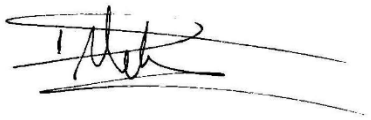
Thus, as laid out in the Petition, *Georgiou* teaches all the elements of independent claim 1. Paper 1, 61-73. Patent Owner has not made any independent arguments regarding claims 3-5, 8-10 and 12, which are obvious over *Georgiou* alone and in view of *Halepete* and *Kranich* as laid out in the Petition. Paper 1, 61-81.

This Reply is supported by the Declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1032, ¶¶1-40).

VI. CONCLUSION

For the reasons above, the Board should find all of the challenged claims 1 and 3-12 of the '443 patent unpatentable.

Respectfully submitted,



Dated: August 8, 2025

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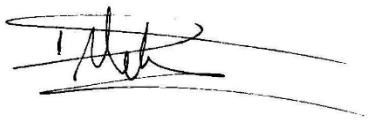
CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petitioner' Reply to Patent Owner's Response in IPR2024-01225 contains, as measured by the word-processing system used to prepare this paper, 4,776 words. This word count does not include the items excluded by 37 C.F.R. § 42.24.

Dated: August 8, 2025

Respectfully submitted,



By: _____
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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, the undersigned hereby certifies that this "PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE" was served by filing this document through the Patent Trial and Appeal Case Tracking System (P-TACTS) and via e-mail to the following attorneys of record for the Patent Owner listed below:

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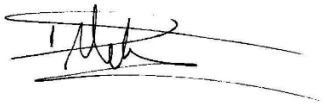

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