

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES), INC.,
Petitioner,

v.

UNIVERSITY OF ROCHESTER
(INTELLECTUAL VENTURES I LLC),
Patent Owner.

IPR2024-01225
Patent 7,089,443 B2

Tuesday, July 22, 2025

Remote Zoom Deposition of
DAVID Kaeli, Ph.D., taken with the witness
participating from his office at the Department
of Electrical and Computer Engineering,
Northeastern University, 333 Dana Research
Center, Boston, Massachusetts, beginning at
10:07 a.m., EST, before Ryan K. Black, Registered
Professional Reporter, Certified Livenote
Reporter and Notary Public in and for the
Commonwealth of Pennsylvania.

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I N D E X

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* * *

Whereupon,

DAVID Kaeli, PH.D.,
called to testify remotely via Zoom
videoconference, having been first duly sworn or
affirmed, was examined and testified as follows:

* * *

EXAMINATION

BY MR. MAUCOTEL:

Q. Good morning, Dr. Kaeli.

A. Good morning.

Q. My name is Jordan Maucotel. I represent
Petitioner Lenovo in this matter, and I'm joined
by my colleagues William Uhr and Dinesh Melwani.

Have you been deposed before?

A. Yes, I have.

Q. How many times?

A. I'm trying to -- probably less than 10,
but more than five.

Q. Okay. In that case, I think I can skip
some of the preliminaries. It sounds like you
have an idea of what to expect.

I do request that you allow me to
complete my question in full before you begin to
answer. I'll try to extend you the same

1 courtesy, as well, and do my best to allow you to
2 complete your full answer before I continue.

3 Counsel for patent owner may object to
4 questions from time to time. And if that's the
5 case and an objection is lodged, you're still
6 required to provide an answer, provided that
7 counsel has instructed you specifically -- has
8 not instructed you specifically not to answer.

9 Do you understand?

10 A. I do.

11 Q. Also, if you do not understand any of
12 my questions, feel free to ask me to repeat the
13 question. I'm happy to do so. And if you do not
14 ask for a question to be repeated, I'll assume
15 that it was understood. Is that fair?

16 A. Yeah. That's fair.

17 Q. Okay. I'll try to take breaks about
18 every-hour intervals, if that works for you.
19 If you need a break at any other time, let me
20 know, and I can finish up my question and then we
21 can proceed to take the break.

22 Does that sound fair?

23 A. Yes.

24 Q. Great.

25 Could you please state your full legal

1 name for the record?

2 A. David Richard Kaeli.

3 Q. Thank you.

4 Do you understand that you're testifying
5 under oath today?

6 A. Yes.

7 Q. Is there anything preventing you from
8 answering questions truthfully today?

9 A. No.

10 Q. Do you recognize the Case Number
11 IPR2024-01225?

12 A. Yes, I do.

13 Q. And this is the proceeding before us,
14 the Inter Partes Review of the U.S. Patent Number
15 7,089,443; is that correct?

16 A. Yes. I believe that is the correct
17 number.

18 Q. Okay. So when I refer to the '443
19 patent, I'll be referring to this patent number.
20 Is that understood?

21 A. Understood.

22 Q. Great.

23 Are you currently at your office?

24 A. I am at my office.

25 Q. Are there any other people in the office

1 there with you?

2 A. No.

3 Q. Okay. Great.

4 Does your internet connection seem to be
5 reliable so far?

6 A. It generally is. I'm connected to a
7 wireless router that's out in the hall, but
8 that's, you know, how we connect here on campus.

9 Q. Okay. In the case that communications
10 go down, we'll try to get you back up as quickly
11 as we can to answer all the questions, if that's
12 all right?

13 Other than Zoom on your computer in
14 which we are communicating, do you have any other
15 software open on your computer?

16 A. The only other window I have open is
17 a listing of the deposition files that we may
18 discuss today, --

19 Q. Okay.

20 A. -- which is Exhibits 1001 through 1009,
21 Exhibits 1001 through -- sorry, 2001 through
22 2013.

23 Q. Okay. And you can access those
24 exhibits?

25 A. I can.

1 Q. Okay. Are those clean exhibits? What I
2 mean is, do they have any notes on them?

3 A. They have no notes on them.

4 Q. Okay. That works fine. And when I
5 refer to an exhibit number, we can pull up that
6 exhibit that you have before you to refer to it.

7 A. Great.

8 Q. Can you affirm that you will not
9 communicate with anyone, electronically or
10 otherwise, while you're providing testimony on
11 the record?

12 A. Yes.

13 Q. Okay. And did you bring any other
14 documents or notes with you electronically --

15 A. No.

16 Q. -- or physically?

17 A. No.

18 Q. Great. Let's go ahead and pull up
19 Exhibit 2001.

20 A. I have it open.

21 Q. This is a copy of your Declaration
22 submitted with the Patent Owner's preliminary
23 response, correct?

24 A. Yes.

25 Q. This is -- we sometimes refer to this as

1 the First Declaration, for ease of discussion.

2 And turning to the very last page of
3 this, Page 40, that is your signature there; is
4 that correct?

5 A. That is correct.

6 Q. Are you aware of anything in this
7 Preliminary Response Declaration that needs to be
8 corrected or clarified?

9 A. No.

10 Q. So sitting here today, do you believe
11 the declaration before us, Exhibit 2001, is
12 complete and accurate?

13 A. So after this, I completed a second
14 declaration, later on. So I'd just qualify it
15 that my later declaration is a more complete and
16 full description of my opinions. So I don't -- I
17 want to make sure that that's understood when I
18 answer this question.

19 So at the time when I signed that
20 declaration, that was -- based on the information
21 and the analysis I had done at that point,
22 everything was factual.

23 Q. Okay. Let's go ahead and open up
24 Exhibit 2013. And if you could turn to the last
25 page of this one, as well, this exhibit.

1 A. Yes, I'm there.

2 Q. This is a copy of your Declaration that
3 was given with the Patent Owner's response; is
4 that correct?

5 A. That is correct.

6 Q. And that's your signature on the last
7 page, Page 16?

8 A. It is. Yep.

9 Q. Great.
10 Are you aware of anything in this
11 Declaration that needs to be corrected or
12 clarified?

13 A. No.

14 Q. Sitting here today, do you still believe
15 that this entire Declaration is complete and
16 accurate?

17 A. Yes.

18 Q. So from now on, I'll be referring to
19 this Declaration more since it's the most recent
20 one. This is what I'll be referring to as your
21 Declaration in our discussion.

22 If I refer to Exhibit 2001, I'll refer
23 to that as your First Declaration or Exhibit
24 2001, just so that's understood. Does that work?

25 A. Yes.

1 Q. Okay. At this point I'd like you to
2 open up Exhibit 1001. This is the '443 patent.

3 A. I have it open.

4 Q. Could you please turn to Column 17
5 starting at Line 9?

6 A. I'm there.

7 Q. Could you read this entire claim,
8 please?

9 A. The entire Claim 1?

10 Q. Claim 1, yes.

11 A. So at 9 it says, "We claim, one, a
12 multiple clock domain microprocessor," -- there's
13 a typo there -- "comprising a plurality of
14 domains. For each of the plurality of domains, a
15 clock for separately generating a clock signal at
16 a frequency for that domain, the frequency being
17 dynamically changeable independently of the
18 frequencies of the clock signals generated for
19 the others of the plurality of domains; and, for
20 each of the plurality of domains, a voltage input
21 for receiving a voltage, which is dynamically
22 changeable independently of the voltages applied
23 to the others of the plurality of domains."

24 Q. Thank you.

25 The first line of the claim after the

1 Preamble recites "a plurality of domains"; is
2 that correct?

3 A. The first line includes the term
4 "plurality of domains."

5 Q. How would you define the term "a
6 plurality of domains," as recited in this claim?

7 A. I'd look at the sentence construction.
8 It's referring to the multiple clock domain
9 processor, which has more than one -- plurality,
10 generally to me, means more than one -- clock
11 domain.

12 Q. And what's your definition of a
13 "domain"?

14 A. I think that's a well-understood term.
15 In the context of a clock domain, it refers to
16 those elements in that portion of, let's say, a
17 microprocessor, which is the context here, that
18 are under control of the same clock -- clock
19 frequency, I'll say in this context. And along
20 with that frequency, also an associated voltage
21 that is associated with that frequency for that
22 domain.

23 Q. Does this domain have a physical
24 architecture?

25 A. Sorry. I don't know what you mean by

1 "a physical architecture."

2 Q. Is this domain made up of physical
3 components?

4 A. The clock domain can -- is -- is, you
5 know, is based on when a clock -- a generated
6 clock signal is feeding the devices, some subset
7 of the devices, which will define the domain.

8 Is it physically separate? It may
9 or may not be separate. It will depend on the
10 individual design of that microprocessor.

11 Q. How is an individual domain defined, as
12 far as being separate from other domains?

13 A. I can answer that question in the
14 context of this patent, which is where there's a
15 frequency and a voltage feeding a subset of the
16 elements of the -- of the, you know, of the
17 digital elements in that domain that are under a
18 common clock and -- and -- sorry, frequency and
19 voltage control.

20 Q. Are there specific components associated
21 with these domains?

22 A. I'd like to understand your question
23 better. Are you talking about is this how it's
24 generally designed? Is this -- what is your
25 -- what -- can you be more specific in your

1 question?

2 Q. Sure.

3 Are these domains generally designed
4 with certain electronic components?

5 A. So a microprocessor, you know, has,
6 usually, you know, gates and latches of various
7 -- and -- and other elements, buses and -- that
8 make up the design.

9 Those elements that are controlled by a
10 clock, generally, will be under and in a domain
11 in the context of the '443 patent. That domain
12 -- that subset of elements that are clocked will
13 share a common clock at a frequency, and, then,
14 associated with that, an appropriate voltage.

15 Q. So according to what you've said, it
16 appears that the main definition of "domain" is
17 that it's under the control of a clock; is that
18 correct?

19 A. I'm responding specifically for the
20 context of the '443 patent, which that is how the
21 term "domain" is being used.

22 Q. As far as the claims of the '443 patent,
23 how does the clock in this context generate the
24 clock signal?

25 A. For a single domain, generally, there

1 is a crystal that generates at a known frequency
2 a clock signal, and that crystal would feed a
3 particular clock domain.

4 In the context of the '443 patent,
5 there will be multiple, you know, independent and
6 separate, you know, clock generation in terms of
7 -- and -- and so they're completely decoupled
8 from each other. There's no -- and so they're
9 -- they're each driving and feeding their own
10 individual domain.

11 Q. Does each clock have its own crystal, as
12 you mentioned?

13 I think you're referring to a crystal
14 oscillator; is that correct?

15 A. That's right. Mm-hmm.

16 Q. And each -- each domain -- or each clock
17 includes its own crystal oscillator?

18 A. That's one particular implementation.
19 There may be others. I haven't considered every
20 possible one.

21 Q. What would be another example?

22 A. So as de -- you know, in -- in
23 -- different than the '443 patent, and in a lot
24 of the cited art in this case, we could take a
25 single oscillator and take versions of it that

1 are at fixed multiples of the frequency of that
2 oscillator and feed different domains. That is
3 a -- but that's not what the '443 teaches.

4 Q. In that case, in the case that there
5 is a clock partitioning its timing to different
6 domains, in that case, does each clock have its
7 own crystal oscillator?

8 A. When they're feeding multiples? Is that
9 your question?

10 Q. That's my question, yes.

11 A. Yes. So the -- and, again, my
12 description with a crystal oscillator is, you
13 know, we have to have something that's generating
14 a clock signal that's then -- so we -- if we're
15 -- again, if we're creating a -- you know, we
16 have multiple clock domains, but they're not
17 independent -- they're dependent on a single
18 frequency, and then those frequencies are then
19 usually divided by some integer value and
20 they're done for a purpose, which is to allow
21 communication between domains to occur
22 synchronously and predictably.

23 And, again, the '443 patent teaches away
24 from that in that there's limitations for that
25 style of clock design, for a multiple clock

1 domain microprocessor.

2 Q. In the case that you have a multiple
3 clock domain processor, as you mentioned, there's
4 various different types. In any organization of
5 a clock feeding a signal to a domain, does that
6 clock have a crystal oscillator in it?

7 A. Say your question one more time.

8 Q. Sure.

9 In any example of a clock connected to a
10 domain to provide timing to that domain, does the
11 clock connected to the circuit have a crystal
12 oscillator in it?

13 A. So you're asking if -- sorry. Frog in
14 my throat.

15 So if there's a clock feeding a domain,
16 is there a -- is there a crystal oscillator
17 that's feeding that -- the -- the generation of
18 the signal to that domain? Is that the question?

19 Q. Yes.

20 A. Yes.

21 Q. Is there any other mechanism by which a
22 clock can generate a signal, beside a crystal
23 oscillator, that you're aware of?

24 A. As I mentioned before, as the '443
25 teaches away from, we can take versions of that

1 same signal -- that same clock signal, and divide
2 it down through a variety of techniques where,
3 then, the clocks are not independent.

4 The '443 teaches about having
5 independent -- independently changeable
6 frequencies in clock signals.

7 Q. Okay. Let's go ahead and turn to your
8 Declaration, Exhibit 2013.

9 I'd like to refer to Paragraph 114 of
10 Exhibit 2013, if you could open that up?

11 A. Sure. One second. 113, yes.

12 Q. Excuse me. Paragraph 114.

13 A. I'm on 114.

14 Q. Could you please read Paragraph 114 of
15 the your Declaration when you have it open?

16 A. Sure.

17 "In my opinion, based on the plain and
18 ordinary meaning as understood by a person of
19 ordinary skill in the art, the claims of the
20 '443 patent require that each domain" --

21 Oh, man. Hold on a second.

22 Give me just a second.

23 (Whereupon witness took a drink of
24 water.)

25 Once again, "In my opinion, and based on

1 the plain and ordinary meaning as understood by a
2 person of ordinary skill in the art, the claims
3 of the '443 patent require that each domain
4 generate its clock independently, and that the
5 frequency of each domain's clock be dynamically
6 changeable without being constrained by the
7 frequencies of other domains; that is, each
8 domain must be free to generate and change its
9 clock frequency without being tethered to small
10 integer multiples of other domains.

11 BY MR. MAUCOTEL:

12 Q. In referring to the first portion of
13 that paragraph you stated, "The claims of the
14 '443 patent require that each domain generate its
15 clock signal independently"; is that correct?

16 A. Yes.

17 Q. Referring to the language of Claim 1
18 that we read before, does Claim 1 recite
19 "a domain that generates a clock signal"?

20 A. So we read clock -- I'm sorry.
21 We read Claim 1. Basically, Claim 1, you know,
22 is a -- it's for a multiple clock domain
23 microprocessor that has multiple domains, where
24 each of the plurality of domains a clock for
25 separately generating a clock signal at a

1 frequency for the domain and the frequency being
2 dynamically changeable independently of the
3 frequencies of the clock signals generated for
4 the others of the plurality of domains.

5 And then for -- and then, similarly for
6 the voltage input, as well.

7 Q. Correct.

8 So my question is, does the actual
9 language of Claim 1 recite, "A domain that
10 generates a clock signal"?

11 A. So when you say does it in -- does it
12 int -- I want to be clear on your question --

13 Q. Sure.

14 A. -- and the scope of your question.

15 Q. Let me refer directly to your statement
16 in your Declaration on Paragraph 114. I'm
17 referring to the portion that states, each domain
18 generate -- "The claims of the '443 patent
19 require that each domain generate its clock
20 signal independently."

21 Is this language found in the '443
22 patent --

23 A. Yes.

24 Q. -- in the claims of the '443 patent?

25 A. Yes.

1 Q. Can you show me in Claim 1 where it
2 recites that each domain generates its clock
3 signal independently?

4 A. Okay. I'll read the -- read it again.

5 So, "A multiple clock domain
6 microprocessor comprising a plurality of domains.
7 For each of the plurality of domains, a clock
8 for separately generating a clock signal at a
9 frequency for that domain, that frequency being
10 dynamically changeable independently of the
11 frequencies of clock signals generated for the
12 others of the plurality of domains."

13 I think that's clear.

14 Q. Again, I'd -- I'd like to --
15 specifically the language, "a domain generating
16 a clock signal," is that found in Claim 1?

17 A. In Claim 1, "A clock for separately
18 generating a clock signal at a frequency." So
19 for each of the plurality of domains, the domains
20 include a clock for separately generating a clock
21 signal at a frequency for that domain. I don't
22 -- I -- I don't think that could be clearer.

23 Q. So you take that phrase in the claim to
24 be equivalent to a domain generating its clock
25 signal independently?

1 A. Again, I take the claim as a whole
2 that includes the frequency being dynamically
3 changeable independently of the frequencies of
4 clock signals generated for others of the
5 plurality of domains.

6 Q. I understand. I'm referring directly to
7 your language in Paragraph 114 where you state
8 that, "each domain generates its clock signal
9 independently." I'm unclear how a domain can
10 generate a clock signal.

11 A. So the domain includes a clock for
12 separately generating a clock signal at a
13 frequency for that domain.

14 I can't -- I'm -- I'm, you know -- the
15 language that's in the claim is pretty clear to
16 me.

17 Q. So you're referring to the clock in each
18 domain? Is that what you're saying?

19 A. Again, for each of the plurality of
20 domains, a clock for separately generating
21 -- "separately generating" -- a clock signal at a
22 frequency for that domain and the frequency being
23 dynamically changeable independently. These
24 are key -- key elements of the '443 -- of the
25 frequencies of the clock signals generated for

1 the others of the plurality of domains.

2 Q. Can a domain generate a clock signal
3 without a clock?

4 A. Can a domain generate a clock signal?
5 That's an odd question.

6 So as opposed to what's described in
7 the '443, we can have a clock that's generated
8 outside of a domain and then divided by -- as
9 -- as is done in -- in some of the cited art
10 that, basically, are versions of that same clock
11 and fed to domains.

12 That's an alternative. Not what's
13 described and not what's taught in the '443.

14 You know, I'm trying to understand your
15 question. I'm not trying to be obtuse.

16 Q. I understand.

17 Is it safe to assume that a -- the
18 statement, "Each domain generates its clock
19 signal independently," refers to the clock within
20 the domain that's generating a clock signal? Is
21 that fair to say?

22 A. Again, I can -- I'm -- I'm -- my opinion
23 here is, in reference to the '443, and the '443
24 clearly states that, for the plurality of domains
25 a clock for sep -- that the domain includes a

1 clock for separately generating a clock signal at
2 a frequency for that domain, and the frequency
3 being dynamically changeable independently of the
4 frequencies of other domains -- of the clock
5 signals for other domains.

6 So I think that's really clear.

7 Q. Is it your opinion that, in the context
8 of this claim, Claim 1 of the '443 patent, each
9 domain is assigned a separate clock?

10 A. In the context of the '443 Claim 1,
11 for each domain there's a clock for separately
12 generating a clock signal at a frequency for that
13 domain. That's what the language says. I
14 support that for the '443.

15 Q. In the context of the '443 patent, do
16 you consider a clock to be an integral part of
17 the domain?

18 A. What do you consider an "integral part"?

19 Q. Earlier you mentioned that a domain is
20 defined by receiving a clock signal; is that
21 correct?

22 A. Say it one more time.

23 Q. Earlier, I believe that your testimony
24 was that a domain is defined by an area that
25 receives a clock signal; is that correct?

1 A. I didn't say that it's "an area,"
2 because I think I was specific in suggesting
3 that these could be physically distributed or
4 overlapping, but that their individual components
5 are fed with a common clock, and that's what's
6 defining the domain.

7 Q. So would you consider that this clock is
8 an integral part of the domains?

9 A. In the context of the '443 patent,
10 it's clear that the domain includes a clock for
11 separately generating a clock signal at a
12 frequency for the domain.

13 Q. Okay. Is it your understanding that the
14 '443 patent is limited to embodiments where each
15 domain is assigned a separate clock?

16 A. The '443 describes how each domain has
17 its -- a separate -- has a separate clock at its
18 own frequency, and also an associated voltage.
19 And those are independent of other do -- of the
20 frequency and voltages for other domains.

21 That's what the '443 teaches.

22 Q. Is it your understanding that each
23 domain is assigned a clock with a separate
24 crystal oscillator for each domain?

25 A. I would assume that there's -- that is

1 one possible embodiment for -- for -- to achieve
2 separate clocks feeding individual domains; and
3 that for the context of '443, that is the
4 -- that's a -- a straight -- that's a straight
5 -- you know, that's the easiest, I think about
6 here, in terms of the context of what the '443
7 teaches.

8 If we -- you know, if -- if we want to
9 go to the other types of solutions that have been
10 -- that were proposed that, basically, take a
11 single clock and then divide it by some integral
12 value, then, again, that's not -- that's
13 different than the '443 patent.

14 Q. So let's take this example of the '443
15 patent that you've discussed where each domain
16 has a separate clock.

17 Are the phases of these different
18 domains related in any way?

19 A. When you say "the phases," can you be
20 more precise?

21 Q. Sure. As far as the timing of the
22 different domains. Is the timing of the
23 different domains related in any way in the
24 context of the '443 patent?

25 A. So the only -- so you're asking if the

1 -- the -- the multiple frequencies in the -- for
2 the '443 patent, for the multiple frequencies
3 that are generated, that are available, are they
4 -- do they have any relation to one another at
5 all? Is that your question?

6 Q. Yes. That's what I'm asking.

7 A. In general, they should be completely
8 independent, so they may be in some, you know,
9 changeable independently -- dynamically
10 changeable, independently, across a range that
11 may be -- that is -- that would allow for each
12 clock domain to run at its, I'll call it, optimal
13 power and frequency, or whatever the computation
14 happens to be.

15 Q. So if I'm understanding you right,
16 you're saying that the frequencies in each domain
17 are disconnected from each other in every way; is
18 that correct?

19 A. I wouldn't say "in every way."

20 Again, we're not gonna have something
21 running at 10 -- you know, two gigahertz and
22 something running at a hertz. That would be
23 somewhat -- you know, unless it really made sense
24 for whatever's running at one hertz to be running
25 that slow.

1 Q. So are you saying there's not gonna be
2 an extreme variation in frequency between the
3 domains?

4 A. I didn't say that. It will not be
5 -- for the example that I gave, which is probably
6 a -- one that has never been developed, I would
7 not be surprised to see that each domain has
8 ranges that may overlap.

9 Q. So even though the frequencies
10 are not related between the various domains, they
11 may have frequencies that may overlap -- or they
12 may have ranges that may overlap? Excuse me.

13 A. Again, though, they're dynamically
14 changeable independently of one another. So they
15 don't de -- they don't depend on each other.

16 Q. What's your understanding of what
17 "depending on each other" means as far as the
18 domains are concerned?

19 A. If I change the frequency in one
20 clock domain, that I don't need to give any
21 consideration, necessarily, to changing the
22 frequency in another domain in my design.

23 Q. So in such a case with independent
24 domains as you've defined, is there any --
25 can there be any problems that arise with

1 coordinating timing between the various domains?

2 A. So previous art before the '443 taught
3 that you want to have a -- if you have multiple
4 clocks that are generated off a single clock and
5 you're gonna take multiples of that, you're gonna
6 divide by 2 or 3 or 4, usually small integers,
7 to have a more synchronous design so that between
8 clock domains communication could occur simply.

9 With the '443, the '443 describes
10 language of utilizing Phase Lock Loops that allow
11 for two design -- two domains that are running at
12 different frequencies to sync up and be able to
13 pass information between the two domains.

14 Q. So it's my understanding that this
15 Phase Lock Loop process that you're talking about
16 avoids problems with not having synchronization
17 between the different domains; is that correct?

18 A. The Phase Lock Loop is one element for,
19 you know, buffering information be -- allowing
20 for two domains that are running at different
21 frequencies to sync up on passing information
22 from one to the other.

23 Q. Why do these domains need to sync up, as
24 you had just stated?

25 A. Well, I'll give maybe one of

1 the simplest designs possible, or one of the
2 simplest examples, which is, let's assume that
3 most of our processing pipeline is running at
4 one frequency and our memory is running at a
5 different -- in a different domain, so two
6 different domains. And I need to be able to
7 -- so the processing pipeline needs to access
8 memory to get operands to carry out, let's say,
9 an addition. So it needs to go off and request
10 those to the memory interface.

11 Now, they're running at different
12 frequencies. Typically, memory technology
13 is running slower than processing pipeline
14 technology. So they'll need to be able to -- you
15 know, for the passing of information, they'll
16 need to be able to sync up between them.

17 Q. From your understanding of the '443
18 patent, are there any examples in the '443 patent
19 where domains share a common clock?

20 A. (Brief pause.)

21 So in Column 6, the -- around
22 27 -- so -- the '443, particularly -- you know,
23 it emphasizes the -- and I'll read this, "The
24 primary disadvantage of a multiple clock domain
25 processor (an MCD processor) is performance

1 overhead due to interdomain synchronization."

2 And, you know, so, basically -- and
3 it says in the next paragraph at 32, some
4 synchronization screen -- schemes restrict the
5 phase relationship and relative frequencies of
6 the clocks thereby eliminating the need for
7 hardware arbitration, and it cites 27.

8 So in terms of your question, is
9 there anywhere in this patent description that
10 describes using -- where a single clock is used
11 to feed multiple domains, in this context, I
12 believe -- let's go to 27.

13 Let's see. 27 is the Sarmenta that,
14 basically, is titled Rational Clocking that was
15 published in ICCD 1995.

16 I think I was at that conference.

17 So the answer to your question, you
18 asked if there's any mention of using a single
19 clock to feed multiple domains, there is, but
20 the '443 is teaching us away from that design
21 because of various challenges.

22 Q. So referring to the solution proposed
23 by the '443 patent that you dis -- that you
24 discussed, does the solution of the '443 patent
25 include any examples of two domains sharing a

1 common clock?

2 A. So is it referencing paper -- you're
3 asking me does it reference papers and studies
4 that suggest it's easier to take a single clock
5 signal, divide it by some known value, some
6 integer value and then feed it to multiple
7 domains? It -- it does provide that, but it's,
8 basically, teaching away from that.

9 Q. I understand. I'm referring to
10 the solution proposed by the '443 patent. I
11 understand that the '443 patent refers to other
12 -- other papers and -- and -- and systems. But
13 as far as the system presented by the '443 patent
14 as a solution, does that include multiple domains
15 that share a common clock?

16 A. The claims of the '443 are teaching away
17 from sharing a common clock.

18 Does the whole patent -- I'd have to
19 read it to make sure that they didn't offer a --
20 you know, offer, but it's a possibility as it was
21 in previous art that they cite.

22 So they do acknowledge that you could
23 have a design that has a single clock and feed it
24 to multiple domains. But that's not what the
25 '443 is teaching, as the claims that we keep

1 reading, so . . .

2 Q. Okay. We're about 50 or 60 minutes in.
3 Do you want to stop for a break?

4 A. That would be fine with me.

5 MR. THEISS: That works for us, as well.

6 MR. MAUCOTEL: Do you want to say a
7 five-minute break? Does that work all right?

8 THE WITNESS: That will be fine with me.

9 MR. MAUCOTEL: How about a seven-minute
10 break, and come back at 11:05 Eastern.

11 Does that work?

12 THE WITNESS: Sounds great. Sounds
13 great.

14 MR. MAUCOTEL: Okay. We'll go off the
15 record. Thank you.

16 THE REPORTER: Okay. We're off the
17 record.

18 (Recess taken -- 10:58 a.m.)

19 (Resume testimony -- 11:06 a.m.)

20 BY MR. MAUCOTEL:

21 Q. Let's go ahead and open again to Exhibit
22 2013, Paragraph 114.

23 A. I am there.

24 Q. Could you read the last sentence of that
25 paragraph, Paragraph 114?

1 A. "That is, each domain must be free to
2 generate and change its clock frequency with"
3 -- "without being tethered to small integer
4 multiples of other domains."

5 Q. And do you have Claim 1 handy, as well?
6 It sounds like you've been able to refer to that.
7 And I know we're bouncing back and forth a lot
8 between exhibits here.

9 A. I understand.

10 Q. I just want you to take a look at the
11 claim language in Claim 1.

12 My question is does Claim 1 -- the
13 language in Claim 1 actually recite, "A domain
14 that is free to generate and change its clock
15 frequency"?

16 A. The Claim 1 states -- again, I'll -- I
17 can't say it clearer than the language that's
18 there: "For each of the plurality of domains, a
19 clock for separately generating a clock signal at
20 a frequency for that domain, the frequency being
21 dynamically changeable independently of the
22 frequencies of the clock signals generated for
23 the others of the plurality of domains."

24 I think it's consistent.

25 Q. So are you saying that -- that that

1 language that you referred to is equivalent to
2 your statement that this is a domain that is free
3 to generate and change its clock frequency?

4 A. Independently of the other clock domains
5 -- of the frequency in other clock domains.

6 The statement -- the sound byte from
7 114 that you asked me to recite is referring to,
8 specifically, an implementation from prior art
9 which, basically, changes the clock frequency and
10 other domains based on a small integer multiple
11 of a single clock.

12 Q. That -- that statement -- that specific
13 term "small integer multiples," does the language
14 of Claim 1 recite "small integer multiples"?

15 A. The language in Claim 1, basically, says
16 that the clocks for each domain are generated
17 independently.

18 Q. But does the actual language of Claim 1
19 state the term "small integer multiples"?

20 A. That particular language in my
21 declaration is specific for how the prior art
22 developed supported multiple clock domains.
23 So, no, it does not include it.

24 Q. Does the disclosure of the '443 patent
25 include the phrase, "small integer multiples of a

1 frequency"?

2 A. So the disclosure of the '443 does
3 reference the prior art, and, in the prior art,
4 they describe using small integer multiples of a
5 clock.

6 Q. And which prior art are you referencing
7 there?

8 A. I'm gonna go to -- let me just -- so if
9 I go to the Sarmenta, so this is Exhibit 2004,
10 titled Rational Clocking, so it talks about
11 "Synchronous solutions are more efficient and
12 reliable but have traditionally lacked
13 flexibility because they require clock
14 frequencies to be related to integer factors."

15 And later on it talks about that the
16 clock frequencies are related by the ratio of two
17 small integers.

18 Q. So is that the background of this
19 term, then, the small integer multiples that you
20 refer to here?

21 A. When I refer to, in 114, I'm basically
22 responding to the Georgiou publication, which was
23 coauthored by, actually, my previous manager at
24 IBM research.

25 But the point is that each of the

1 cited examples of generating multiple clocks are
2 generating versions of a single clock that are
3 dependent on one another because they're coming
4 off a single frequency and then are distributed
5 to each clock domain.

6 In the Georgiou patent it's doing this
7 based on formal feedback and doing this in a
8 -- and uses precomputed voltage and frequency
9 pairs to select, but, again, is working off of
10 the same context. Basically, it has, in the
11 Georgiou patent, a divide by two and a divide by
12 an element described in their figures.

13 Q. So going back to the '443 patent,
14 besides this Sarmenta reference which you have
15 discussed here, are you aware of the '443 patent
16 itself discussing small integer multiples of a
17 frequency?

18 A. Again, I think they're -- in terms of
19 the '443 by reference is using -- let me just
20 -- give me a second and let me take a quick look
21 just to make sure.

22 (Reviews document.)

23 (Pause in proceedings while witness
24 reviewed document.)

25 So in terms of using that exact

1 language, so that was -- those were my -- that
2 was my terminology for describing what is
3 presented in the prior art that was cited by
4 Lenovo. And, also, specifically -- and, again,
5 it's des -- it -- that -- that terminology is not
6 used directly in the '443, but by reference,
7 particularly, to the Sarmenta rational clocking.

8 The terminology, "rational clocking," as
9 a term, may not have been as well-understood as
10 my description of what actually is done, which is
11 by scaling by integer multiples.

12 But it's very clear from the '443 that,
13 you know, feeding different clock domains with a
14 clock that's, you know, divided by N, whether
15 that be 2, 3, 4 small integers, you know, that
16 was the prior art before the '443 and the '443
17 teaches away from that.

18 Q. I'm interested to hear your definition
19 of this term, "small integer relationships."
20 You've discussed here there can be various small
21 integers in the frequencies related by those; is
22 that correct?

23 A. Yes.

24 So let's say we're taking N to be 2, so
25 we're gonna divide the clock by 2 and we'll have

1 a clock running at, let's say, a gigahertz, and a
2 clock running at 500 megahertz. That would be an
3 example of -- and we use -- you know, you don't
4 want to use a value, probably, that's, let's say,
5 a thousand, because then you would be slowing
6 down one clock too much, even though you'd have a
7 synchronous design that would probably not make
8 as much sense in terms of scaling clocks in
9 multiple domains.

10 So -- and in most of the cited
11 literature by Lenovo, it's -- they're -- they're
12 talking about, "divide by 2 or divide by N," and,
13 again, where N is usually a small integer.

14 Q. So this term is as simple as dividing a
15 frequency by some small N or, in this case, some
16 small integer; is that correct?

17 A. Yes. And the -- the -- the goal is
18 that, after a certain number -- after -- let's
19 say we divide by three, after -- so after -- or
20 let's say 4. After 4 iterations of the faster
21 clock -- sorry, of the slower clock, they'll
22 -- the two clocks will be in phase so that
23 synchronization between domains and communication
24 will be eased.

25 Q. So are there other ways to keep the

1 various domains in phase without simply dividing
2 by an integer?

3 A. Well, that is part of what the '443
4 teaches us.

5 Q. What do you mean by that?

6 A. So if we go to the -- to Claim 2, which
7 builds on Claim 1 -- it's a dependent claim
8 -- that, basically, comprises a Phase Lock Loop
9 and means for receiving an externally generated
10 clock signal and for supplying the externally
11 clock -- generated clock signal to said Phase
12 Lock Loop.

13 And then later talking about the -- the
14 -- the term in the slack and the processing from
15 one domain to the other and then being able to,
16 using a, further described in the dependent
17 claims, ability to exchange information.

18 Q. I'm referring -- I'm referring
19 specifically to the term of "small integer
20 relationship." Does this term only refer to
21 dividing a frequency by an integer -- that's my
22 question -- or is there more involved?

23 A. In the related -- in the -- in
24 the cited exhibits that Lenovo provided, and
25 others, it's clear they're dividing that clock

1 by -- they're basically feeding a -- using a
2 common clock and then dividing it down.

3 Does each -- so one option is using a
4 integer multiple, and that's usually described
5 for understandability and simplicity. If we're
6 using -- there is the option that we could use a
7 different number, a different value, and as long
8 as there's still the ability to have those sync
9 up in the future dependably, which is, again,
10 they use divide by N and they usually describe
11 N as a small integer.

12 So is it the only? So again, you
13 know, in the -- as described in the literature,
14 it's generally described as N small integer. Is
15 it possible? I suspect there is a way to do it
16 and still have that ability to sync up. But,
17 again, each of those domains is not independent
18 of each other. Their frequencies are not
19 independent of each other. So they're -- and
20 that's, basically, what the '443 teaches away
21 from, is that dependency between domains to have
22 to have -- you know, or they're being fed by a
23 single clock frequency that gets conditioned.

24 Q. So wouldn't it be fair to say that your
25 term, "a small integer relationship," refers to

1 the ability to sync up over time as you were
2 saying?

3 A. So if we go to where I can -- so that's
4 in 114, correct?

5 Q. We were discussing your testimony at
6 Paragraph 114 of the Declaration earlier, yes.

7 A. Yes. And in 114, I'm specifically
8 addressing Georgiou, in particular, in that
9 context.

10 Q. So my question is, though, the idea of
11 a small integer relationship that you testified
12 about is related in some way to the frequencies
13 matching up over time; is that correct?

14 A. Again, I was describing how it's
15 described in Georgiou.

16 Q. But it's your opinion in Georgiou that
17 small integer relationships end up with domains
18 that match up over time?

19 A. When the division -- that is one
20 possible, "divide by 2, divide by N," as
21 described in Georgiou.

22 Q. In -- in -- in the example that you've
23 given here of domains that are related in some
24 way by small integers, is it possible to one
25 integer multiple of one domain without affecting

1 the other domain?

2 A. So you're saying -- so the only -- once
3 the -- so the -- that's a -- I see -- I see your
4 point.

5 You're gonna be still off of a single
6 frequency -- base frequency, so you're not truly
7 independent of the other domain. You're still
8 gonna be a -- so -- so you're still gonna be
9 dependent on the frequency of that other domain
10 because you're only gonna be dividing by a
11 different N. So you're not independent.

12 Q. So my question was, is it possible to
13 change the integer multiple of one domain without
14 changing the integer multiple of another domain?

15 A. It depends how you're changing that
16 -- each of the frequencies.

17 So can I change from dividing by 2 to
18 dividing by 3 for one domain and keep the other
19 domain as dividing by 4? Yes. But they're
20 still, basically, fed by a single source. And
21 you're only gonna be -- and you're dependent on
22 that source, so you are dependent on that other
23 frequency.

24 You know, independence includes, you
25 know, selecting your own frequency without any

1 consideration of the other domains. And, again,
2 you're only going to be able to divide a fixed
3 frequency or the freq -- you know, the -- the
4 -- the -- the one frequency, or whatever
5 -- however number you have -- by that -- a
6 fixed value.

7 Q. Okay. If we could turn to Paragraph 50
8 of your Declaration, --

9 A. Sure. Just a second.

10 Q. Sure.

11 A. Okay. I'm there.

12 Q. And this part of your declaration
13 actually discusses some of the disclosure of
14 the '443 patent that we disclosed -- that we
15 discussed earlier. In fact, I think you read
16 that section already of the patent. This is
17 columns -- excuse me --

18 A. Column 6.

19 Q. -- Column 6, correct.

20 Do you -- do you mind just reading, once
21 again, Column 6, Lines 32 through 36 of the '443
22 patent?

23 A. Mm-hmm.

24 So I'm gonna read the paragraph before
25 it, if you don't mind, as well, just so we have

1 the full context?

2 Q. Sure.

3 A. "The primary disadvantage of a
4 multiple clock domain processor is the
5 performance overhead due to interdomain
6 synchronization. In this section, we discuss
7 the circuitry required to perform the
8 synchronization. We discuss how to model its
9 performance cost below. Some synchronization
10 schemes restrict the phase relationship and
11 relative frequencies of the clocks thereby
12 eliminating the need for hardware arbitration,
13 cites 27" -- which we've talked about here
14 multiple times, which is the -- is it the
15 Sarmenta? Yeah. The Sarmenta --

16 Q. That's the Sarmenta.

17 A. -- paper.

18 Q. Right.

19 A. Right. That uses rational clocks.

20 Q. Okay. And so --

21 A. "Unfortunately, these schemes" --

22 Q. We can move back to your Declaration
23 which refers to that portion that you've read.

24 A. Yes.

25 Q. And the last sentence in Paragraph 50

1 of your declaration states, "These statements
2 clearly inform a POSITA that the invention is
3 designed to avoid architectures where clock
4 domains must maintain a small integer
5 relationship to each other; is that correct?

6 A. Yeah. I -- I believe -- I -- I feel
7 strongly that the invention teaches away from
8 using an architecture where the clock domains
9 must maintain this small integer relationship to
10 each other.

11 Q. Well, why should a POSITA avoid
12 these type of architectures, where clock domains
13 maintain a small integer relationship to each
14 other?

15 A. By having dependencies between clock
16 domains, you're restricting what frequency
17 each domain can run at to get its either optimal
18 performance, optimal power, whatever your
19 criteria is. And so by restricting them to be
20 multiples of a common frequency, we're going to
21 -- it's -- that -- that implementation will be
22 suboptimal.

23 And, again, having them as, you know,
24 as integer multiples will probably run one -- may
25 run one too fast or one -- I'm sorry, not too

1 fast, but one too slow, just for the sake of
2 simplifying syncing up between the domains.

3 Q. What do you mean by that, that one would
4 have to run too slow to sync up?

5 A. Well, let's say I divide by two, and I'm
6 doing that for a reason. Maybe it's because I'm
7 a little bit slower than the other domain. My
8 cert -- my -- my devices are a little bit slower.
9 But I -- I used N equal to 2, and that, basically
10 -- now I'm running at half speed, and I didn't
11 need to go quite that aggressively. But because
12 of my strategy for syncing up the clocks in the
13 multiple domains, I'm going to be limited here.

14 Q. Is it true that some of these systems
15 that you're referring to, where the frequencies
16 are related in some way, are related with a
17 number smaller than an integer?

18 A. Do you mean smaller than 1?

19 Q. Yeah. Smaller than 1.

20 A. So that they could speed up? So
21 if I doubled -- so I could use .5, which is --
22 basically, they are integer multiples. So I -- I
23 don't want to play that game.

24 Is that what you're getting at? I'm not
25 quite clear.

1 Q. No. I think --

2 A. You're looking for some
3 determinism --

4 Q. -- what I'm referring to is --

5 A. Yeah. You're looking for some
6 determinism between the frequencies of the two
7 clock domains so that they can -- there can be
8 some -- in the future, they can communicate more
9 simply due to being -- they'll be in phase at
10 that point.

11 Q. What I'm saying is it's not necessarily
12 one integer to another integer relationship; is
13 that correct? It can be some -- some -- some
14 smaller number than an -- some portion of an
15 integer to be related between the different
16 domains; is that correct?

17 A. I hadn't considered that in my analysis.
18 I'd have to think about that a little bit more
19 before I had an opinion.

20 Q. As far as the '443 patent teaches,
21 what reasons does it give for avoiding these
22 architectures where clock domains maintain a
23 small integer relationship to each other?

24 A. So as described -- I can read it again.
25 You -- you -- so in Column 6, you know, "Some of

1 the synchronization schemes restrict the phase
2 relationship and relatively frequencies of the
3 clocks thereby eliminating the need for hardware
4 arbitration. Unfortunately, these schemes impose
5 significant restrictions on the possible choices
6 of frequency."

7 So, in addition, the need to control
8 the -- to control the phase relationships of the
9 clocks means that global clock synchronization is
10 required.

11 And, again, the '443 says, "Our design,
12 specifically, recognized the overhead associated
13 with independent clocks with no known phase
14 relationship. We believe this overhead to be
15 unavoidable in a multiple-clock domain processor.
16 One of the motivating factors for the design is
17 the recognition that the traditional global
18 clock distribution will become increasingly
19 difficult in the future."

20 Q. So the first sentence of that paragraph
21 that you read discusses the need for hardware
22 arbitration. What's hardware arbitration?

23 A. So this is, again, I -- it's referencing
24 27, so let's go and look at 27.

25 I'm not sure if they use that

1 terminology.

2 Yeah. They do use that terminology.

3 So right in the abstract, basically --
4 I'll read the last line of the abstract -- "Our
5 approach maintains a known-phase relationship
6 between clocks whose frequencies are related by a
7 rational factor and exploits the predictability
8 of their relative phases to algorithmically timed
9 communications without runtime arbitration
10 contests."

11 So when we're trying to sync up, you
12 know, signals between two -- or values between
13 two clock domains or communication between those
14 domains.

15 I'd refer you to my example of the
16 processing pipeline and the memory system that
17 I referred to earlier as an example.

18 Q. So how does this restriction
19 of phase relationship and relative frequency
20 eliminate the need for hardware arbitration,
21 then?

22 A. Let's take the example of we're running
23 at a gigahertz and 500 megahertz in the two
24 domains.

25 After two cycles in the 500 megahertz

1 domain, I will be in phase with the gigahertz
2 -- I'm sorry. Opposite. The gigahertz will be
3 running twice as fast. So the gigahertz is
4 running twice as fast. After two cycles, it will
5 be in phase with the 500 megahertz. So in that
6 sense -- so then the communication is simpler.

7 That's what the Sarmenta paper's about.

8 Q. So just by virtue of them being
9 synchronized in some way, there doesn't need to
10 be a timing function; is that correct?

11 A. "There doesn't need to be a timing
12 function." I don't know what you mean by that.

13 By having a known phase relationship
14 between clocks whose frequencies are related by a
15 relational matter -- a factor, I'm sorry,
16 basically, they will be more predictable of
17 their relative phases and easier to sync up.

18 Q. Okay. We've been discussing the 2004
19 Sarmenta reference. I think that's just the
20 portion of it that you had just read recently; is
21 that correct?

22 A. That is correct.

23 Q. There is some testimony about the
24 Sarmenta reference in Paragraph 34 of your
25 Declaration I'd like to turn to.

1 A. Okay. I'm there.

2 Q. In the center of that Paragraph 34,
3 there's a line that starts with, "While Sarmenta
4 introduces." Could you read that sentence there?

5 A. "While Sarmenta introduces a
6 synchronization approach leveraging rational
7 frequency relationship, Sarmenta's scheme imposes
8 significant restrictions on frequency selection
9 as noted in the '443 patent."

10 Q. And what are these "significant
11 restrictions in frequency selection" that you're
12 referring to here?

13 A. There needs to be a rational
14 relationship between the frequencies in each of
15 the clock domains. And they're -- and they have
16 to -- and they're dependent on each other.

17 Q. And the rational relationship is related
18 by integers? Is that what you're referring to?

19 A. So a rational -- so, basically, I'll say
20 that there's a single -- there's a single clock
21 that's used for generating the frequencies for
22 each of the domains, and so they're not
23 independent.

24 The '443 teaches us we can have our
25 independence and clock frequency generation

1 and allow each domain to have their independent
2 frequency, thus optimizing execution.

3 Q. So in your opinion, these significant
4 restrictions boils down to the number of
5 different frequencies that are selectable
6 in each domain; is that correct?

7 A. No. Not the number you can select.
8 It's the independence between each domain being
9 able to use its own frequency independent of the
10 frequency used in other domains. That is the
11 novelty of the '443.

12 Q. And so how is that independence --

13 A. It's not just a number. It's not like,
14 "oh, we can three frequencies or four frequencies
15 or five." That's a different -- you know, I
16 don't think -- all we're -- all the -- the '443
17 allows for a plurality. It doesn't say exactly
18 how many, and so it allows for whatever number.

19 Q. Correct. I'm not talking about the
20 number of domains. I'm talking about the number
21 of available frequencies in each domain.

22 A. The number of available frequencies
23 in each domain? A domain is defined by its
24 frequency.

25 Q. Right. So my understanding of what we

1 are discussing here, it sounds like what you're
2 saying is that the significant restrictions
3 discussed in Sarmenta has to do with domains
4 being related by some integer number in their
5 frequencies; is that correct?

6 A. That's part of it. The other part is
7 that they are -- it's a single frequency that
8 -- and -- and therein lies the lack of
9 independence as described.

10 Q. Can you describe that: "A single
11 frequency therein lies the" --

12 A. So they're basically being -- so there's
13 a single base frequency that is then -- we use
14 the term "conditioned." Usually it's divided to
15 feed each of the frequencies in each domain.
16 That's the technique that Sarmenta is describing
17 and what the '443 is teaching away from.

18 Q. So how does that propose -- impose a
19 significant restriction?

20 A. Didn't we just go over that?

21 Q. Well, you mentioned there's a single
22 frequency that's conditioned in some way.
23 Does that -- in your -- in your --

24 A. So on Column 6, Line 32 -- I can read
25 it again -- it's pretty clear -- and, again, it

1 refers to how it's done in -- as well in -- in
2 Sarmenta, but, basically, I think it's providing
3 multiple reasons why you don't want to have, you
4 know, this dependency between clock domains.

5 Q. I think if we jump down to Paragraph 52,
6 there's also some more explanation here that
7 can maybe be helpful, so let's go to your
8 declaration in Paragraph 52.

9 Could you go ahead and read that once
10 you've got it in front of you?

11 A. 52?

12 So I'm gonna read 51, because 52 is
13 referring to -- is relative to 51. Is that okay?

14 Q. Okay.

15 A. So 51 recites, "The references cited in
16 the specification, particularly Sarmenta, and,
17 by extension, Pratt, reinforce this distinction.
18 As a POSITA, I recognize that Sarmenta and Pratt
19 describe systems that rely on rational clocking;
20 that is, systems where the clock frequencies of
21 different domains must maintain a ratio of
22 small integers. These systems exploit the
23 predictability of phase alignment over a fixed
24 interval, referred to as a coincidence cycle or
25 beating period, to schedule communication without

1 requiring one-time arbitration."

2 Paragraph 52, "From a technical
3 perspective, these rational clocking systems
4 necessarily impose frequency constraints on
5 each domain in order to maintain the fixed
6 alignment interval that enables deterministic
7 communication. Each domain's clock frequency
8 must be selected from a narrow set of permitted
9 values that satisfy the required rational ratio.
10 A POSITA reading Sarmenta and Pratt would have
11 understood that such constraints fundamentally
12 limit the system's ability to independently vary
13 domain frequencies."

14 Q. I'd like to focus on -- it's the second
15 sentence from the end of what you've just read --
16 "Each domain's clock frequency must be selected
17 from a narrow set of permitted values that
18 satisfy the required ratio."

19 Do you see that there?

20 A. Yes.

21 Q. What is this narrow set of permitted
22 values you're referring to here?

23 A. I'm referring to, as described in
24 Sarmenta and Pratt, the small integer values that
25 are referenced specifically in that prior art.

1 Q. So the small integer values is
2 equivalent to the narrow set of permitted values?

3 A. In the context of Sarmenta and Pratt,
4 they are.

5 Q. Is it possible to approximate the number
6 of permitted values referred to here?

7 A. To approximate the number of permitted
8 values?

9 The number of values has -- again,
10 the -- the -- given the ability to change -- I'm
11 confused by the question because you -- you
12 -- this is the second time you've asked "the
13 number of values." And the number of values is
14 the -- the four -- the -- the '443, basically,
15 allows for a -- has a plurality of clock domains
16 and doesn't put such restrictions on what -- what
17 the number of different clock frequencies are
18 used for individual domain.

19 With the prior art, they're going
20 to -- you'll -- you need to be able to -- you
21 have to go and check -- you have to talk to your
22 neighbors and see what other domains are running
23 at, and then this can tell you what you can run
24 at because, one, you're being fed by the same
25 base clock and you're just dividing it by some

1 value.

2 And -- and -- and so -- and you need to
3 be able to make sure that value was such that you
4 can predictably have your coincidence cycle, or
5 beating period, to sync up. And, again, without
6 it, it will complicate the design significantly.

7 So Sarmenta and Pratt are teaching us
8 something very different than what's in the -- in
9 the '443.

10 Q. So I'm really just referring
11 to your statement, "The narrow set of permitted
12 values." I understand your explanation there.
13 It's the narrow set of permitted values connected
14 to what you're talking about, that the domains
15 must be connected in some way, their frequencies
16 must be related in some way. Is that what that
17 statement is referring to, "a narrow set of
18 permitted values"?

19 A. The relationship between the clock
20 frequencies in the different domains, that's
21 what I'm referring to. And, again, specifically
22 talking in that context on Sarmenta and, by
23 extension, Pratt.

24 Q. Okay. We're about 50 minutes or so in.
25 Did you want to pause for a break again?

1 A. Sure.

2 MR. MAUCOTEL: Let's go off the record.

3 (Recess taken -- 11:56 a.m.)

4 (Resume testimony -- 12:05 p.m.)

5 BY MR. MAUCOTEL:

6 Q. So moving just a couple paragraphs down
7 from what we were talking about before, I'd like
8 to discuss Paragraph 54 of your exhibit -- of
9 your Declaration, Exhibit 2013. And this refers
10 to the Chakraborty reference; is that correct?

11 A. Yes.

12 Q. And that's a paper entitled Efficient
13 Self-time Interfaces Processing Clock Domains.
14 Is that correct, what the Chakraborty reference
15 is?

16 A. Yes.

17 Q. Is the Chakraborty paper cited in the
18 '443 patent?

19 A. No. No, it's not.

20 Q. Could you turn to Paragraph 58 of your
21 Declaration. This is continuing the discussion
22 of Chakraborty. If you could read Paragraph 58
23 when you have it up?

24 A. Well, again, 58 is referring to
25 something from the previous paragraph, which

1 I'll read 57. Is that okay?

2 Q. Sure. Please proceed.

3 A. Yeah. "Chakraborty also makes clear
4 that systems utilizing rational clock frequencies
5 are different from systems that operate at
6 arbitrary frequencies. Specifically, Chakraborty
7 explains, 'as described above, we present designs
8 when the sender and receiver operate at exactly
9 the same frequency, at frequencies that are
10 rational multiples of each other, at closely
11 matched frequencies and at arbitrarily relatively
12 stable frequencies.' To emphasize this point,
13 Chakraborty dedicates entire separate sections of
14 the paper to rational clock frequency multiples
15 and arbitrary clock frequencies reinforcing that
16 these are treated as distinct classes of
17 systems."

18 Q. So is it true that your testimony that
19 rational clock -- rational clock systems and
20 arbitrary clock systems are separate is based on
21 these being separated sections of Chakraborty?

22 A. I offer -- I selected Chakraborty as
23 an example of a -- you know, a description that
24 clearly differentiates between a rational clock
25 frequency domain, so, basically, the two examples

1 with rational clock frequency multiples and
2 arbitrary clock frequencies; that they are
3 treated separately and distinctly in that paper
4 is why I brought the Chakraborty paper into this
5 discussion.

6 Q. Okay. Let's go ahead and turn to a
7 few paragraphs earlier in your declaration to
8 Paragraph 41.

9 I'm most interested in the last sentence
10 of this paragraph, which you have in front of
11 you. If you could read that?

12 A. Well, this is referring to Pratt.
13 And, basically, I'm describing, I think,
14 some -- so in -- in Paragraph 40, just to give
15 it more context, "So in this way, Pratt provides
16 the detailed implementation of the theoretical
17 foundation that underpins the concept of the
18 coincidence cycle referenced in Sarmenta.
19 The coincidence cycle and beating period are
20 functionally synonymous terms for the reoccurring
21 alignment window of two rationally related
22 clocks, and both serve as a basis for the
23 synchronization stream described across both
24 documents. This predictable timing structure
25 yields a powerful architectural advantage. It

1 enables the system to precompute a schedule of
2 valid and invalid transmission and reception
3 intervals.

4 As a result, data" extensions --
5 "exchanges between independently clocked systems
6 can be precisely timed to occur only during safe
7 windows, thereby avoiding metastability and
8 eliminating the need for asynchronous handshaking
9 protocols or dynamic arbitration logic. The
10 communication proceeds deterministically and
11 With high throughput even across clock domains
12 operating at different speeds.

13 In this context, the coincidence
14 cycle, or beating period, serves as a fundamental
15 mechanism that transforms what would otherwise be
16 an asynchronous communication challenge into a
17 synchronously solvable problem achieved through
18 rational clocking and deterministic scheduling."

19 Q. Thank you for reading that.

20 So referring to the last sentence
21 of that paragraph, what is an "asynchronous
22 communication challenge" -- an example of "an
23 asynchronous communication challenge" referred to
24 here?

25 A. So when two clock domains need to pass

1 information between those domains, they need
2 to have the ability to in some way synchronize
3 the communication, such that we can
4 deterministically have a way of communicating
5 data from one domain to the other, even though
6 the speeds of those domains are different.

7 By using rational factors as described
8 in all of the examples that we're discussing, we,
9 basically, know that after a certain number of
10 cycles, they'll -- those two domains will be in
11 phase, and so will make that synchronization and
12 that passing of information, that communication,
13 easier to accomplish and be much more
14 deterministic in that sense.

15 Q. Well, that's the one example, is to have
16 the phases lineup as in the previous examples, as
17 we've talked about. What is the solution that
18 the '443 patent presents as a solution to the
19 asynchronous communication challenge?

20 A. So the '443 leverages a couple of
21 mechanisms.

22 First, it leverages a Phase Lock
23 Loop that basically will allow for, basically,
24 possible syncing, and, in addition, the
25 '443 describes the ability to -- and these are

1 independent claims -- the ability to have a -- a
2 queue between each of the domains with status of
3 empty and full described that, basically, allow
4 for that communication to happen even though
5 those are running asynchronously.

6 Q. So, in your opinion, do these solutions
7 offered by the '443 patent, the Phase Lock Loop
8 that you discussed, as well as the queue between
9 the different domains, do those result in
10 synchronizing the various domains?

11 A. They allow for deterministic
12 communications between the domains.

13 Q. And what does "deterministic
14 communication" refer to?

15 A. That I can -- when I have two
16 independently domain -- clock domains, running
17 at different frequencies, and I'm trying to
18 communicate information from one to another,
19 I have a mechanism for performing that
20 communication, and, again, that allows
21 for, you know, the decoupling of the two domains
22 and to allow them to run independently, as well.

23 That's -- that's part of the com -- you
24 know, part of, you know, what that enables. The
25 fact that they have completely separate clock

1 generation mechanisms is also the major benefit,
2 as well, for the '443.

3 So, again -- but I'll -- you know, that
4 -- so -- and -- and Claim 6, which is a dependent
5 claim on 5, which is a dependent claim on 1,
6 describes that.

7 Q. But it's your understanding that
8 these mechanisms allow for the domains to be
9 synchronized at a given time -- for a chosen
10 time; is that correct?

11 A. They allow for information to be
12 communicated between domains.

13 Q. And the domains are -- there's some
14 synchronization between the domains as well; is
15 that correct?

16 A. Is there a synchronization between
17 the domains? No. Not -- the clocks are not
18 synchronized. The communication is synchronized.

19 Q. So these -- the phase lock loop and the
20 queue system that you discussed allow the phases
21 of the various domains to be synchronized?

22 MR. THEISS: Objection. Misstates
23 testimony.

24 THE WITNESS: I said that -- so -- so
25 ask your question again.

1 BY MR. MAUCOTEL:

2 Q. So I'm -- I'm just interested in -- in
3 trying to understand what you're saying. The
4 solution by the '443 patent, which, as we've
5 discussed, are the Phase Lock Loop and the queue
6 system, result in the domains being synchronized
7 to send information; is that correct?

8 A. I -- the -- the -- basically, these are
9 the mechanisms that are being described in the
10 '443, and they're allowing for and supporting the
11 communication between the two clock domains --
12 for the communication to happen between the two
13 clock domains.

14 Q. Do these solutions allow the domains to
15 be synchronized in any way?

16 A. Only the communication is performed
17 in a way that provides us with deterministic
18 communication. There is no -- again, there's no
19 relationship between the clock frequencies of the
20 separate domains.

21 Q. Is it true that when the information is
22 sent, at the time the information is sent, the
23 domains are synchronized in their timing?

24 MR. THEISS: Objection. Asked and
25 answered.

1 THE WITNESS: Are you asking about the
2 '443 or some other art that the '443 teaches away
3 from?

4 I think you're talking about the -- the
5 art that the '443 teaches away from, which is
6 using synchronous -- using clocks that are
7 running off of replicas of some base clock.

8 BY MR. MAUCOTEL:

9 Q. I'm talking about the '443 examples that
10 we're discussing here.

11 You were talking about --

12 MR. THEISS: Objection.

13 BY MR. MAUCOTEL:

14 Q. -- deterministic communication.
15 I'm trying to understand your definition of this
16 term.

17 At the time of communication, is
18 the timing of the two domains communicating
19 synchronized?

20 A. No. The timing is independent of each
21 other. They're basically using a buffer for the
22 communication between the two domains.

23 Q. So there's no synchronization between
24 the domains even at the time of communication?

25 A. Again, the only aspect is the ability to

1 write to a queue and read from a queue, but no
2 dependency on the clocks of the frequencies of
3 those two domains.

4 Is that clear?

5 Q. So I'm not talking about clock
6 dependencies, I'm talking about synchronization
7 between the timing between domains. At the time
8 of communication is there any synchronization
9 between the --

10 A. You're talking timing -- you said timing
11 and synchronization. That's frequency. It's
12 just another term. So I want to be very clear
13 and careful that the two domains are reading and
14 writing to a buffer, to a queue. And that's how
15 information is passed from one domain to another,
16 as described in Claim 6.

17 Q. And, in your view, that communication is
18 not related to the domains being synchronized as
19 far as timing?

20 A. Again, each domain still runs at its
21 own individual frequency and they're -- and each
22 frequency is independent of other frequencies in
23 other domains, as taught by Claim 1.

24 Q. Okay. Let's go ahead and turn to
25 Paragraph 66 of your Declaration.

1 A. Sure.

2 I'm there.

3 Q. Could you just go ahead and read
4 Paragraph 66 when you've got it?

5 A. So this is in the context of the Shenai
6 reference, which is Exhibit 1004. And 66 says,
7 "It should be noted that Shenai is focused on
8 supplying a clock and vaulted source to an
9 analog-to-digital converter in contrast to the
10 microprocessor targeted in the '443 patent.
11 Further, Shenai's characterization of systems
12 requiring asynchronous communications as
13 undesirable would not motivate a POSITA to
14 implement a globally asynchronous architecture
15 as required by the '443 patent."

16 Q. The citation after the first sentence
17 says, Exhibit 1004, 3 comma -- or 3:0025. Do you
18 know what that cite is referring to there?

19 A. Let me go to that.

20 So that is -- should be Column 3.
21 It may be a typo.

22 Oh, 'cuz it's -- it's described
23 differently, yes. It's -- they're using
24 different numbering.

25 Page 3.

1 So it's referring to -- so they don't
2 use columns in this. They have, sort of, pages,
3 or I don't know what you want to call them. It's
4 on Page 9 of 13, but it's on -- I'm not sure what
5 we -- how we referred to the 3 that's at the top
6 of the page and then Paragraph 25.

7 Q. Okay. So it's referring to Paragraph 25
8 on Page 3?

9 A. Yes.

10 Q. Okay.

11 A. Yeah. I -- I was thrown off also by the
12 different way that this patent is structured.

13 Q. Okay. The -- the -- the disclosure
14 here, per your testimony, in -- involving this
15 section states, "It should be noted that Shenai
16 he's focusing on supplying a clock and voltage
17 source to an analog-to-digital converter in
18 contrast to the microprocessor targeted in
19 the '443 patent"; is that correct?

20 A. That is correct.

21 Q. Well, where is this analog-to-digital
22 converter that is referred to here in Shenai?

23 A. I believe -- let's see -- if we go
24 down -- again, I apologize that this reference,
25 though it's not mine, doesn't have line numbers.

1 So it's describing Figure 4. It
2 says, "Loads 410 through 416 may be individual
3 components, functional blocks of single component
4 or independent systems. Typical loads may
5 include an analog-to-digital converter utilizing
6 comparators as described in U.S. patent serial
7 number attorney docket hybrid data comparator."

8 So it's, in some sense, describing
9 applications that apply to analog-to-digital
10 conversion.

11 If we go to Figure 4, let me just take a
12 look real quick.

13 Q. Yeah. Paragraph 25 refers to Figure 4
14 as -- as -- as well, correct?

15 A. Yes. (Reviews document.)

16 So it has dynamic power and clock
17 distribution controller.

18 Q. The analog-to-digital converter you're
19 referring to, does that refer to the loads shown
20 in Figure 4, which are 410, 412, 414 and 416?

21 A. So it says loads -- so from that
22 Same Paragraph 25, "Loads 410 through 416 may be
23 individual components, functional blocks of a
24 single component or independent systems. Typical
25 loads may include an analog-to-digital converter

1 utilizing comparators," and, again, it's
2 described in some other document.

3 Q. Okay. Let's go ahead and --

4 A. And then they go on -- just let me
5 finish, please.

6 Q. Okay. Go ahead.

7 A. "Other loads may include RF power
8 amplifiers as used in cellular phones, LCD
9 displays, TFT displays, and are likely used in
10 cellular phones and personal digital assistants."

11 And so RF power amplifiers is analog
12 circuitry. So, again, it's talking about things
13 less akin to multiple clock domains and
14 microprocessor.

15 Q. Okay. We can go ahead and continue this
16 when we return from lunch and continue with this
17 questioning.

18 A. Very good.

19 Okay. Thanks.

20 MR. MAUCOTEL: We can go off record.

21 (Lunch recess -- 12:31 p.m.)

22 (Resume testimony -- 1:18 p.m.)

23 BY MR. MAUCOTEL:

24 Q. Okay. Let's go ahead and turn back to
25 Paragraph 66 of your declaration, Exhibit 2013.

1 This is kind of where we left off before lunch.

2 A. I am there.

3 Q. Okay. And the first sentence of
4 Paragraph 66 states, "It should be noted that
5 Shenai is focusing on supplying a clock and
6 voltage source to an analog-to-digital converter,
7 in contrast to the microprocessor targeted in the
8 '443 patent"; is that correct?

9 A. Yes.

10 Q. And is it -- is it true that the
11 analog-to-digital converter here is in reference
12 to the loads in Shenai?

13 A. Let me go back to Shenai, and let me
14 look at the language.

15 (Reviews document.)

16 So it says, "Loads 410 through 416 may
17 be individual components, functional blocks of a
18 single component or independent systems. Typical
19 loads may include analog-to-digital converter
20 utilizing comparators as described in whatever
21 patent. Other loads may include," and it gives
22 a laundry list with, like, our -- our power
23 amplifier. So certainly elements of analog and
24 digital, but it looks like a mix, which is
25 different than a microprocessor.

1 Q. So to clarify, though, this statement
2 in your testimony is referring to the loads?

3 A. Yes.

4 Q. Yeah. Let's continue reading in Shenai
5 the next few sentences as you were reading.

6 So one example of the loads, as you
7 stated, is an analog-to-digital converter. Can
8 you read the sentence that begins, "Other loads
9 may include"?

10 A. Other loads may include an RF power
11 amplifier as used in cellular phones, LCD
12 displays, TFT displays and the like used in
13 cellular phones and personal assistant devices,
14 digital cameras, et cetera.

15 Q. So is it --

16 A. So it's talking to a display which
17 usually involves, you know, some type of -- so
18 it's a -- you know, a different environment and
19 application and, generally, has both digital
20 and analog. But I'm -- I'm -- I was referring
21 to the typical loads comment that's specifically
22 written in that 0025 paragraph.

23 Q. Okay. Let's continue on to the
24 next sentence after the one that you read.
25 "Still further examples may include."

1 A. Sure. "Still further examples
2 may include components or subsystems of
3 microprocessor or microcontrollers such as
4 cache, register files, LUs, integer, and"
5 so -- "instruction pipeline circuitry hardware
6 multipliers, floating point circuits, nonvolatile
7 memory."

8 Q. So is it fair to say that there's kind
9 of a wide range of possible components that could
10 be a load, as far as Shenai is concerned?

11 A. Shenai is prime -- was prime -- you
12 know, initially focused on this class of
13 analog-to-digital, but does offer us a laundry
14 list of other types of devices.

15 Q. And it's true that those loads may
16 include components such as microprocessors and
17 microcontrollers; is that correct?

18 A. That's what it says.

19 Q. Would a microprocessor or a
20 microcontroller be implemented on an integrated
21 circuit?

22 A. Much of what I -- what do you mean
23 would a microprocessor or microcontroller be
24 implemented on an integrated circuit?

25 (Whereupon Mr. Theiss lost connection.)

1 That's a very broad question.

2 I'm trying to understand.

3 I mean, usually you're going to use, for
4 a microprocessor, most processors use a custom.
5 Usually today it's -- I'm not -- I think I've
6 lost track as to if it's CMOS recently, and,
7 basically, are very highly integrated. I'm not
8 sure I know what you're asking in your question.

9 Q. Sure. Are microprocessors or
10 microcontrollers suitable for being integrated on
11 an integrated circuit?

12 A. An integrated circuit?

13 I mean, what an ASIC is that's
14 referenced in this particular -- in the Shenai,
15 and what an integrated circuit is, in general,
16 are two -- so an Application-Specific Integrated
17 Circuit is something very specific to a
18 particular application and could be anything --

19 THE REPORTER: Excuse me. Excuse me.
20 I don't mean to interrupt. I think we lost
21 Mr. Theiss -- Theiss. It's looks like he's no
22 longer here.

23 MR. MAUCOTEL: Let's go off record.

24 (Recess taken -- 1:25 p.m.)

25 (Resume testimony -- 1:26 p.m.)

1 BY MR. MAUCOTEL:

2 Q. Okay. The question pending was are
3 microprocessors or microcontrollers suitable for
4 being implemented on an integrated circuit?

5 A. And, again, I was trying to understand
6 your context of the inter -- of an integrated
7 circuit. It could be as an ASIC, which,
8 generally, implements a very specialized type of
9 device in a circuit. Microprocessors use a more
10 custom-based design and layout technology for
11 implementing circuits -- implementing, you know,
12 devices.

13 If you're talking -- so talking about
14 integrated circuits, in general, that's a very
15 broad class. So I'm just trying to be -- maybe
16 if you could be more precise on what you're
17 asking.

18 Q. Well, isn't it true that some
19 microcontrollers or microprocessors can be
20 implemented in integrated circuits?

21 A. They could be integrated as an
22 integrated circuit, yes. They could be -- a
23 microprocessor could be implemented in a
24 field-programmable gate array. It could be
25 implemented in an ASIC.

1 Q. Okay. Let's go ahead and move down in
2 the Shenai reference. This is Exhibit 1004. We
3 were just reading in Paragraph 25. Paragraph 33
4 continues the description of Figure 4.

5 Could you read in Paragraph 33,
6 if you have that in front of you?

7 A. Yeah.

8 Q. Midway down Paragraph 33 there's
9 a sentence that begins, "Because DC-to-DC
10 converters 470 to 476." Do you see that?

11 A. Yeah.

12 Q. Could you read that sentence?

13 A. "Because DC-to-DC converters may
14 include smaller reactive components that may
15 be integrated monolithically, single die or
16 component with loads, such as 410 through 416,
17 such as on a common integrated circuit, for
18 example," --

19 Q. So --

20 A. -- "DC to DC converters may be placed
21 strategically with a large die near the specific
22 load clusters for which they provide power."

23 Q. Great.

24 So is it true that loads 410 through
25 416, which we've been discussing, can also be

1 integrated with DC-to-DC converters?

2 A. So Shenai is describing that they could
3 be integrated into a integrated circuit with
4 that, but they're -- again, the Figure 4 that we
5 referred to before was specifically showing us a
6 design that was targeted for A-to-D conversion,
7 so . . .

8 Q. And where is that in Figure 4 that
9 you're saying is specifically determined by
10 the --

11 A. Just by the design itself. Just by the
12 design itself.

13 Q. Can you explain what aspect of the
14 design lends itself to AC-to-DC conversion?

15 A. Hold on. I'm sorry.

16 Well, I have a -- because I have the
17 high-speed DC-to-DC converters, so let me -- you
18 know, they're basically servicing -- so -- so
19 they're -- how can I describe this?

20 (Reviews document.)

21 So just from the description that I
22 read on 0025 was my major indication that this
23 is -- that these loads are, basically, involved
24 in analog-to-digital conversion.

25 Q. Isn't it true that --

1 A. Again, this would be -- this would be a
2 block that you'd see in an A-to-D converter,
3 probably.

4 Q. Do you see a block that says A-to-D
5 converter in Figure 4?

6 A. No, just that that's described in 0025.

7 Q. Is it true that Paragraph 25 describes
8 that the loads can be analog-to-digital
9 converters?

10 A. Can you point me to somewhere in Shenai
11 where it says that?

12 Q. Paragraph 25.

13 A. So they're describing the loads
14 that they're controlling. And, again, they're
15 giving, as the major examples, analog-to-digital
16 conversion and also RF power amplifiers, which
17 -- and -- and elements that, typically, involve
18 analog-to-digital signals.

19 Q. Is it true that these loads can also be
20 microprocessors?

21 A. They -- so in -- in 0025, they mention
22 microprocessors, but they don't necessarily
23 describe how this particular circuit would need
24 to change to support anything relative to a
25 microprocessor or a microcontroller. It's much

1 more logical for a simpler element such as an
2 A-to-D converter.

3 Q. That may be, but it is possible that a
4 load can be a microprocessor in this paragraph;
5 is that correct?

6 A. The paragraph does state that, still,
7 further examples include components or subsystems
8 of a microprocessor.

9 So components or subsystems doesn't
10 sound like a full microprocessor or full
11 microcontroller. So I don't know. It's
12 somewhat vague.

13 Q. So what would be components or
14 subsystems of a microprocessor in that case?

15 A. I don't know what they're referring to
16 directly. They do talk about caches, memory
17 files -- register files -- sorry -- ALUs, so
18 different elements. But, again, how those
19 would be organized and work with this particular
20 circuit is unclear.

21 Q. Could analog-to-digital converters
22 be part of the components or subsystems of a
23 microprocessor that they're referring to here?

24 A. When I think of the major components of
25 a microprocessor, in terms of -- I don't -- I

1 don't -- you know, they're digitally controlled.
2 And while they do have analog elements for
3 driving buses and other interfaces, the majority
4 of the devices are digital.

5 Q. So if the majority of the devices
6 are digital, is it still possible that a
7 microprocessor has some analog-to-digital
8 components in it?

9 A. Yes, it's still possible. Again, how
10 Figure 4 -- how those loads would be the elements
11 of a microprocessor that are described here is
12 very unclear to me. And the -- the pat -- the
13 patent doesn't go into any further discussion on,
14 you know, how that's done for those types of
15 loads.

16 Q. Well, whether the patent goes into
17 it or not, is it true that Figure 4 can include
18 microprocessors as loads?

19 A. They offer a laundry list of examples
20 that may include components of a microprocessor
21 or components in subsystems of a microcontroller.

22 Q. Okay. Let's go ahead and turn back to
23 the '443 patent again. This is Exhibit 1001.

24 A. Sure.

25 Q. And let's go to the claims, again,

1 actually. Lets's go to Claim 1. It's on
2 Page 18.

3 A. Yep.

4 Q. And if you could read the Preamble of
5 the claim, the first line of the claim, when you
6 get to it.

7 A. The Preamble is? I'm not familiar with
8 what a Preamble of a claim is. It says, "We
9 claim"? Is that what you're --

10 Q. Correct. Yes?

11 A. So read Claim 1? Is that what you'd
12 like me to do?

13 Q. Sure. Yes. Just the first sentence of
14 Claim 1.

15 A. "A multiple clock domain microprocessor
16 comprising a plurality of domains."

17 Q. So what typ -- what materials are
18 typically used to make a microprocessor?

19 A. Are you talking about silicon and
20 copper.

21 Q. A microprocessor has a mass, correct?

22 A. Has a what?

23 Q. Has mass.

24 A. Oh, my gosh.

25 Sure. I think I have one in my closet

1 here. I can pull one out, yeah.

2 Q. And a microprocessor is a physical item.
3 Is that true?

4 A. Yes.

5 Q. Okay. Let's turn to Paragraph 42 of
6 your declaration.

7 And if you could read Paragraph 42 when
8 you get to it?

9 A. Sure.

10 "Counsel has asked me to discuss the
11 SimpleScalar tool that is mentioned in the
12 Samararo [phonetic] -- or however you say it
13 -- paper.

14 In the same time frame as the Samararo
15 paper, the computer architecture community,
16 including my own research group, was using the
17 SimpleScalar tool in our research.

18 Q. SimpleScalar is a software program; is
19 that correct?

20 A. It's a software simulator
21 used to evaluate design tradeoffs in
22 microprocessors/memory systems.

23 Q. What is the primary use of the
24 SimpleScalar system?

25 A. So at the time, the SimpleScalar offered

1 a number of different microarchitectural models
2 at different levels of abstraction that included
3 things like data paths, memory architectures,
4 control units and, basically, allowed you to
5 evaluate utilizing -- you would run actual
6 programs, workloads, benchmarks on the simulator
7 to evaluate the performance and power and other
8 benefits obtained by, you know, a particular
9 design feature that you're exploring in your
10 research.

11 Q. And what is the research group that
12 you're referring to here, your own research
13 group?

14 A. So at Northeastern, I have -- for, I
15 guess, some 33 years, I've led the Northeastern
16 University Computer Architecture Research Lab.
17 I've graduated over 50 Ph.Ds that -- or, sorry,
18 I've graduated 50 Ph.Ds. I'm mentoring more
19 students than that. But -- and many of them
20 have, you know, early on during this time frame,
21 used SimpleScalar in their research.

22 My group also develops simulators
23 of the same -- later -- you know, than the
24 SimpleScalar that, basically, allow you to
25 evaluate CPUs, GPUs, all types of devices.

1 Q. So what specifically did this research
2 group use SimpleScalar for?

3 A. When you say "this."

4 Q. This research group. The research group
5 that you're referring to.

6 A. My students? I'd have to go back to
7 the individual papers and find which ones were
8 -- most of them are using it for, I think -- I
9 think we were using SimpleScalar for our branch
10 prediction work, our cache simulation work early
11 on. So those are the ones that come to mind off
12 the top of my head.

13 Q. So, typically, when you're running a
14 simulation, what input do you put into this
15 -- what -- what input do you need to provide
16 for the SimpleScalar system?

17 A. So you provide a compiled binary.
18 So, basically, you have a benchmark program. You
19 have, usually, a suite of programs that are used
20 by the community to evaluate designs. We sort of
21 discussed this at our meetings and agree on what
22 those standards should be. And then everyone is
23 expected to, sort of, you know, when they're
24 comparing -- when they're evaluating a new design
25 feature, that they're able to demonstrate that,

1 on this set of workloads, this is one of the
2 performance benefits that we were getting. And
3 so it allows for some fairness, some comparisons,
4 some reproducibility.

5 Q. What is the output that the SimpleScalar
6 produces?

7 A. Oh, I haven't used it in quite a few
8 years, but as I remember, you would get cycles,
9 and, you know, you'd get -- depending on what
10 your assumptions were on frequency, you could
11 also couple this with other tools, such as the
12 watch simulator, that, basically, interfaced with
13 SimpleScalar to provide you with power.

14 And so there were a number of tools
15 that interfaced to SimpleScalar over the years.

16 Q. So SimpleScalar can interface with
17 various other systems; is that correct?

18 A. With other software-based simulators,
19 yes.

20 Q. Does the SimpleScalar system produce
21 anything physical; for instance, fabricating
22 hardware?

23 A. What SimpleScalar does is gives you
24 guidance on the potential benefits of -- and,
25 possibly, the guidance on sizing and dimensions

1 of what you might want to fabricate.

2 The whole purpose between, you
3 know, using a simulator like this is to avoid
4 the cost of going through the fabrication process
5 each time, which is both time-consuming and very
6 expensive, and provides you with, you know, a
7 good validation of your architectural idea.

8 And, again, simulators are used today.
9 I'm still working on simulators. My own group
10 continues to work on simulators.

11 Q. Is the simulation data produced as,
12 like, a file at the output of the SimpleScalar
13 system? Like a data file, is that what it
14 produces?

15 A. I forget the exact output format. It
16 could have been on a screen, or it could have
17 been in a file. And I'm sure you can write
18 what's on a screen to a file, because that's what
19 ends up happening, so . . .

20 Q. Okay. But it doesn't produce software
21 or fabricate anything like a 3D printer; is that
22 correct?

23 A. No.

24 Q. Okay. Turning to Paragraph 44 of your
25 declaration, that's two paragraphs down from what

1 we were discussing, could you read the sentence
2 that begins, "When the SimpleScalar tool
3 executed."

4 Do you see that there?

5 A. Paragraph 44 you said?

6 Q. Yes. It's the second paragraph
7 of -- second sentence of Paragraph 34.

8 A. Claim 1? Start off with can Claim 1?

9 Q. Yeah. You can start with Claim 1.
10 Yeah.

11 A. So Claim 1 on the '443 patent recites,
12 "A plurality of domains, each of which includes a
13 clock for separately generating a clock signal at
14 a frequency for that domain, and a clock input
15 for receiving a voltage which is dynamically
16 changeable.

17 When the SimpleScalar tool executed the
18 simulation described in the paper on a host, the
19 host executing the simulation embodied all of the
20 elements of Claim 1 in tangible form. The same
21 can be said for each of the other claims in the
22 '443 patent; namely, the host" --

23 Q. Okay. Let me turn back to "the host."
24 What is your definition of "the host" here?

25 A. Let me go back to the language.

1 (Reviews document.)

2 So in the paper they're describing
3 different processors that are being used.
4 So, basically, what they're im -- they have a
5 very detailed description. If we go to Exhibit
6 2005, and go through on Page 5, the simulation
7 methodology, they describe the actual processors,
8 hosts that they're implementing based on the
9 Xscale model and the Transmeta model and
10 describe how they were actually modeling the
11 implementation of the same concepts of generating
12 clock signals at a frequency for that domain. So
13 each having individual -- having a plurality of
14 clock domains and having separate adjustable
15 clocks that are, basically, available for those
16 domains that are independent of each other.

17 So that's what I'm describing there.

18 Q. So is it true that the host can include
19 a processor?

20 A. The -- you know, so -- so they're
21 modeling here two different processors.
22 They provide the actual details of each of them,
23 to a level of degree, and, basically, then go
24 through and describe how they've implemented,
25 basically, the Claim 1 of the '443 to be actually

1 evaluated its benefits.

2 So, yes, they're basically -- and
3 they're -- you know, they have -- they have two
4 different processor models, which is interesting.

5 Q. So am I correct in saying that the
6 SimpleScalar software uses one or two different
7 processors to provide simulations of a circuit?
8 Is that true?

9 A. They're not simulating a circuit.
10 They're simulating a microprocessor and its
11 execution. So it provides a level of extraction
12 from -- as -- you know, that's appropriate for
13 understanding the performance benefits of making
14 changes to the microarchitecture. In this sense,
15 they're basically dealing with how the individual
16 units are clocked and the control of those
17 clocks.

18 They're -- they're -- and they're
19 implementing that and simulating that within this
20 framework.

21 You know, I would just like to add that
22 this paper, this Samararo paper was presented at
23 HPCA in, I believe it was, 2005, if I'm correct.
24 I think that's the time frame.

25 And I was the general chair -- no. I

1 think it was 2002, right? And I was the general
2 chair of that meeting. It was presented at HPCA.
3 So I'm -- you know, I was at -- I was at this
4 talk, so . . .

5 Q. So you're very familiar with --

6 A. You know, HPCA is a highly competitive,
7 peer-reviewed conference environment where, you
8 know, only the best papers get selected.

9 So this is vetted by, you know, experts
10 in the field that, basically, deem this, you
11 know, very worthy and to be included. And the
12 acceptance rates for conferences in this field
13 are somewhere between 20 to 30 percent,
14 so . . .

15 Q. So turning back to your statement
16 in Paragraph 44, you stated, "When the
17 SimpleScalar tool executed the simulation
18 described in the paper on a host, the host
19 executing the simulation embodied all of the
20 elements of Claim 1 in tangible form."

21 Did I read that correctly?

22 A. Yes.

23 Q. So is it true that the host includes a
24 processor?

25 A. It includes one of the two processors

1 that's described in this paper, yes.

2 Q. As far as the simulation created by the
3 SimpleScalar software after being implemented on
4 the host, can the simulation of the processor be
5 used to control other circuits?

6 A. You're talking, like, different levels
7 of abstraction, and it's very confusing. Sorry.

8 So SimpleScalar is, basically, providing
9 you with -- it can be -- so it can -- it can
10 be, you know, running at different levels of
11 precision. And so here they're looking at both
12 -- they're looking at timing, so they're looking
13 at performance.

14 I forget, I'm trying to see if they
15 -- don't think they -- and they used Watch for
16 getting power estimation.

17 And so they're looking at how -- you
18 know, how they're saving both -- they're
19 improving performance but saving power. And
20 they're modeling things at a level of abstraction
21 to, you know, again, be able to provide this
22 capability of, you know, giving you the benefits
23 with and without the design feature.

24 And so when you ask if -- so in terms
25 of -- so this is a dynamic piece of software. It

1 can make changes to the frequency being used, if
2 that's what you're asking, dynamically while it's
3 running, because it's a piece of software that's
4 running dynamically. And, again, so, you know,
5 that's fully in the capabilities of SimpleScalar.

6 Q. So you mentioned that SimpleScalar can
7 be used at, in your words, different levels of
8 extraction; is that correct?

9 A. That's correct. That is true.

10 Q. You're referring to the possible -- the
11 possible types of simulations that can be run by
12 the SimpleScalar system. Is that true?

13 A. Yes. So if you -- I -- I believe
14 you have access to document Exhibit 2010, which
15 is a tutorial on SimpleScalar. And so it
16 describes the different microarchitectures that
17 are supported and levels of detail that you can
18 use.

19 So, let's see, if I can go down to -- so
20 I can -- let's see. Let's go to --

21 Q. Sure. Let's turn to Exhibit 2 --

22 A. Yeah. I'm trying to get to all the
23 options, because there are a lot of options
24 with this, in terms of -- I mean, as you can see,
25 basically, if I go to Page 23, this describes the

1 simulator structure.

2 So you have, you know, basically,
3 different types of -- so program binaries that
4 get compiled down to a binary at the highest
5 level that run on either targeting a SimpleScalar
6 ISA or a posit system call, which are emulated.
7 It's got a machine definition and also a system
8 call handler.

9 And then each of the different elements
10 -- this is the simulator core and the performance
11 core -- are, you know, elaborated for branch
12 prediction, caches, registers, all the things
13 that you would need that are in a typical
14 processor pipeline.

15 If you go to Page 25, it describes the
16 five different -- at least at that point in time,
17 the different simulators that, basically, you
18 know, were simulated. So it has some FAS, some
19 saves, some profile, in cache cheetah branch
20 prediction and sim out of order.

21 So these are allowing for different
22 levels of detail. And, you know, most of us were
23 using sim out of order, which was the -- the
24 -- and they had MIPS. They had Deluxe, which is
25 a MIPS-like architecture. They also had support

1 for the Alpha architecture.

2 So over time they added more support and
3 more -- you know, targeted more binaries.

4 So . . .

5 Q. So does each of these different suites
6 produce a different type of simulation?

7 A. Yeah. They add levels of detail or
8 they model some of the additional aspects for the
9 Semararo paper. They're doing -- they're
10 simulating an Alpha 21264, which is a DEC Alpha,
11 a state of the art microprocessor of the day, a
12 RISC processor. And that did sim out of order.

13 Q. Is it possible to use SimpleScalar to
14 generate different versions of the same circuit
15 at different levels of abstraction?

16 A. So in terms of the int -- I'd have to
17 go and look at the internal code. But, you know,
18 obviously, you can model any of the particular
19 subelements at a binder level of detail, if
20 that's what you're asking? Yes, you could do
21 that.

22 Q. Okay. Turning to Page 147, actually, of
23 this Exhibit 2010.

24 A. Yep. Which page?

25 Q. Page 147.

1 A. Wow.

2 Q. It's a long exhibit.

3 A. Yes.

4 Limitations . . .

5 Q. So this discusses some of the
6 limitations of the simulator structure. Is that
7 true?

8 A. This is of any type of simulator that,
9 you know, is, I think -- these -- these -- these
10 are the same kind of caveats.

11 Q. What other kind of simulators would have
12 a similar caveat that you're referring to?

13 A. My simulators. My simulators. You
14 know, basically, there's -- you know, in terms of
15 being -- correctness in timing, you know, you
16 are, basically, getting the -- the -- you're
17 -- you're not gonna -- so I'm gonna say a
18 simulator like SimpleScalar is cycle-relative
19 accurate versus being cycle accurate.

20 And I'll say the same for most
21 simulators. Whatever feature that you're
22 modeling or evaluating, you need to be able to
23 get the percent benefit of that feature. To get
24 the absolute number of cycles, that is really,
25 really difficult to do in a software simulator,

1 and no one really has ever done that.

2 This is an accepted limitation of
3 simulation, but also simulators are used
4 by industry, they're used by academics for
5 evaluating new architectural features all the
6 time.

7 Q. So the third bullet down on that
8 Page 147, I think, is relevant to what you're
9 saying here. And there's some speculation value
10 pred inaccurate.

11 A. No. That's talking about value
12 prediction and speculation. That's a
13 architectural feature. You can have value
14 prediction.

15 So -- and, again, unless you simulate
16 all of memory accurately, you may under or
17 overestimate slightly. But, again, that usually
18 is not a big impact on the performance.

19 Q. But is it safe to say that SimpleScalar
20 software predicts certain values that are in use
21 in simulation?

22 A. No. That's -- that's -- it predicts
23 values that may be in memory. That's all it does
24 sometimes.

25 Q. Can there be -- --

1 A. And they may have some implications on
2 those performance, but most of those things are
3 well-documented and well-understood.

4 Q. Can there be variation in the
5 predictions made by the SimpleScalar program?

6 A. No. When you run with the same binary,
7 you'll get the same predictable result. That's
8 what you should -- you should get repeatable
9 results.

10 Q. So what is the discussion here of
11 "inaccurate and speculation"? What does that
12 refer to here?

13 A. I didn't write these slides. It's -- I
14 believe that there is -- as with most simulators,
15 you don't always model all the data values that
16 are in memory.

17 And so in terms of assuming what
18 that value would -- that would be returned from
19 memory that may impact the number of cycles some
20 operation takes, there may be some speculation
21 that may have an impact on -- a minor -- very
22 minor impact. But, again, most of those things
23 are documented. I would have to go back to
24 some of the SimpleScalar papers to actually find
25 those. But the -- so I think that's what they're

1 talking about there.

2 They're also talking about the -- they
3 have -- they're doing value prediction, and so
4 value prediction is both something that we do in
5 microarchitecture. We have a functional unit
6 that's predicting values. And why do we predict
7 values? Because we want to get ahead in the
8 execution.

9 So if you're using value prediction
10 a lot, and I'd have to go and look at this
11 particular model -- I don't think they are,
12 only because it's through -- it's -- it's --
13 basically, their original model is based on the
14 Alpha 21264, which did not do value prediction.

15 I worked very closely with the Alpha
16 folks. They were a lot of fun.

17 Q. Well, when you're talking about
18 "predicting values within memory," are those
19 -- is that memory the memory of the simulated
20 circuit, or is it the memory of this SimpleScalar
21 system itself?

22 A. So think of what it takes to simulate
23 a micro -- like, a computer that's running a
24 program. You're gonna have the microprocessor.
25 You're gonna have the memory system. You're

1 gonna have the application that you compiled to
2 run on the system.

3 So all of those are what's -- all
4 -- they're all part of running a SimpleScalar
5 or any simulator when you're -- you're -- you're
6 doing -- these are -- you know, it's an
7 execution-driven simulation. You're running the
8 actual program that would run on a real physical
9 hardware system.

10 You are simulating the microprocessor
11 in the memory system and handling the I/O and
12 other things that need to happen.

13 Of the question is do you model all the
14 values that are being stored in memory, or do you
15 just know that this value is stored in this
16 address, but we're not going to model the actual
17 values.

18 That's -- and -- and that becomes
19 more of a critical thing when we're doing
20 value prediction as a functional unit. Value
21 prediction was trying to guess what the answer is
22 to a computation. And unless you model all
23 those data values, then you don't know if the
24 prediction was correct or not.

25 That's a microarchitectural feature

1 that are -- many people have tried but really it
2 hasn't panned out to be that useful.

3 So this comment, I believe, has no
4 bearing on -- on -- on the results that are
5 presented in this paper.

6 I don't see a -- so they're not
7 doing value prediction. I don't see it listed
8 in Table 1 in the paper.

9 They are doing branch mispredictions and
10 branches, and I can talk to you all day about
11 branches.

12 Q. Okay. So I think it's fair to say
13 that there is some amount of -- some amount of
14 inaccuracy that can result based on the input
15 software into the is SimpleScalar system. Is
16 that true?

17 A. I think you're mischaracterizing what I
18 said.

19 All simulators have some level of
20 inaccuracy, but it's -- cycle relative, they're
21 accurate. They need to be and they need to
22 prove that, or else they don't get adopted by
23 a community. And SimpleScalar was used by
24 companies, such as Intel and others, for guiding
25 their architectural decisions.

1 So, you know, the point that we just
2 discussed is not relevant to what your statement
3 was.

4 When you go off and look at value
5 prediction as a feature, there will be -- they're
6 saying because we don't model data values, there
7 may be some inaccuracies.

8 Is there -- overall, how accurate is
9 the simulator. That's been studied, you know, by
10 various researchers. Again, this -- at -- at the
11 time, this was the state-of-the-art simulator
12 that was being used by the community and by
13 industry.

14 That's all I can tell you.

15 You know, if you want to get
16 cycle-accurate, go build the hardware, but, you
17 know, maybe a couple million dollars later talk
18 to me.

19 Q. Is that generally how --

20 A. This is how -- this is how -- this is
21 how industry does their work, okay? You know,
22 this is not -- I'm very familiar with it.

23 Q. So once the simulation is created, how
24 is it validated?

25 A. It's validated against real hardware.

1 So they take, generally, a base -- you know,
2 couple base designs and do, sort of, a
3 back-to-back, cycle-by-cycle analysis and
4 they see how accurate it is.

5 Q. And what do you mean by "accurate" in
6 this context?

7 A. They're looking for, again, how -- you
8 know, in terms of -- of -- if they're really
9 interested in detailed cycles, usually what
10 they'll do is they'll take a small kernel, just,
11 maybe, a simple loop or a toy program, and use
12 that and run it on both systems and see if
13 they're getting the same results.

14 This is what I use to actually learn
15 what the hardware is doing of a particular
16 microprocessor as I'm trying to model it. It's
17 called reverse engineering. And this is how many
18 simulators are developed and debugged.

19 So we spend countless years in
20 performance debugging simulators and significant
21 effort and blood, sweat and tears is put into it.

22 So I -- you know, the -- you know,
23 simulators have their limitations, but simulators
24 are the state-of-the-art in terms of guiding
25 architectural decisions such as what's described

1 in our patents.

2 Q. Is there any other way to validate a
3 simulation, other than comparing it to the real
4 hardware version?

5 A. There are other options, but, again,
6 they tend to be quite costly.

7 Generally, you could have a -- you
8 could take your design and synthesize it to a
9 field-programmable gate array, but that also
10 comes with some limitations in terms etch
11 performance and accuracy and is much more
12 difficult to perform simulations and runs much
13 slower, to a certain degree.

14 So, again, you know, an industry, you
15 know, does have timing simulators. My first job
16 at IBM, I was working on a timing simulator for
17 an IBM mainframe. Worked on it for five years.
18 So I understand this domain very well.

19 Q. Okay. We've been going for about an
20 hour let's take another quick break, if that's
21 all right with you?

22 A. Great. That's fine.

23 MR. THEISS: Works for us.

24 (Recess taken -- 2:15 p.m.)

25 (Resume testimony -- 2:20 p.m.)

1 MR. MAUCOTEL: Thank you for your time,
2 Dr. Kaeli. That's all the questions that I have
3 at present. I'll turn it over to Patent Owner
4 counsel.

5 MR. THEISS: Jordan, would it be okay
6 if we just take five minutes? We have to do a
7 redirect. I just want to confer with Dawn for a
8 second.

9 MR. MAUCOTEL: Sure thing.
10 So could we come back at 2:25?

11 THE WITNESS: Sounds good.

12 (Recess taken -- 2:20 p.m.).

13 (Resume testimony -- 2:24 p.m.)

14 EXAMINATION

15 BY MR. THEISS:

16 Q. Professor, I apologize to hold you
17 longer than necessary, but I wanted to give you
18 an opportunity to clarify a couple points.

19 You were talking with opposing counsel
20 about the Gregory reference and the effect of
21 changing N in different domains.

22 Do you remember having that
23 conversation?

24 A. "Greg"? You mean the Georgiou?

25 Q. Yeah.

1 A. The Georgiou reference, yes.

2 Q. Specifically, counsel had asked you
3 questions about what would be the effect of
4 changing one domain -- N in one domain and the
5 other domain? Counsel provided an example with
6 one domain being three and one domain being four.

7 You remember that conversation?

8 A. I do.

9 Q. Okay. Great. Just wanted to orient you
10 there.

11 So if we have the example where Domain 1
12 is at 2N and Domain 3 -- domain -- the other
13 domain is at 3, where would the synchronization
14 point be?

15 A. Six.

16 Q. Great. And at the synchronization
17 point, what can happen?

18 A. Then communications can occur
19 synchronously.

20 Q. Great.

21 If we were to change the domain that
22 used to be at 3 to now be at 4, what would our
23 synchronization point be?

24 A. 12.

25 Q. So if we were to try to communicate at

1 the prior synchronization point, what would
2 happen?

3 A. We would get nondeterministic
4 behavior of the communication, and we may
5 lose information. So it wouldn't work.

6 Q. What would we have to do to make it
7 work?

8 A. We either would -- so we'd have to wait
9 until 12 cycles.

10 Q. Great.

11 So there was also a discussion about the
12 values that N could take.

13 A. Yes.

14 Q. And you gave an example where one of the
15 processors was working at one gigahertz -- or
16 1,000 megahertz; same thing -- and 500 megahertz,
17 and you said that's an example of a $2N$ system.

18 A. Yes.

19 Q. So wouldn't it be fair to characterize
20 that as a half N system if you were to use N
21 being the 1,000?

22 A. Sure. I think I gave that example as
23 well.

24 Q. Would they be mathematically equivalent?

25 A. Would they be math -- what do you mean

1 by "mathematically"?

2 Q. I apologize.

3 MR. MAUCOTEL: Objection. Calls for
4 speculation.

5 BY MR. THEISS:

6 Q. Poorly formulated question. I
7 apologize.

8 Would the synchronization point
9 calculation be the same?

10 A. The synchronization point would be the
11 same.

12 Q. Thank you.

13 So I just want to ask you a couple
14 questions about the SimpleScalar discussion that
15 you just had with opposing counsel.

16 A. Okay.

17 Q. You said that you've supervised a large
18 number of Ph.D students in your lab, right?

19 A. Yes.

20 Q. So if one of these -- and you said a lot
21 of your research deals with branch prediction.

22 If one of your Ph.D students were to
23 say, "I have this great branch prediction
24 algorithm that improves performance by 50
25 percent," what would you like to see them

1 prove to you.

2 MR. MAUCOTEL: Objection; leading.

3 BY MR. THEISS:

4 Q. You can answer the question, Professor.

5 A. So what I would like to see?

6 Q. Mm-hmm.

7 A. I'd like to see where they gen -- where
8 they got 50 percent.

9 Generally, if they're a student
10 working in my group, they would be using a
11 execution-driven or cycle-based simulator that
12 would, basically, be evaluating the particular
13 -- they'd have a baseline design and then they'd
14 simulate their design and evaluate how much a
15 performance changed. And I -- that would be
16 completely acceptable and publishable and
17 accepted by both academia and industry.

18 Q. So if they showed it to you, the
19 simulation results, you would think it worked?

20 A. I would -- again, they would have had
21 to demonstrate it across a representative set of
22 workloads that, basically, are deemed, you know,
23 appropriate for evaluating branch prediction, and
24 -- and -- and, you know, that their results are
25 repeatable and demonstrateable, yep.

1 MR. THEISS: Great. No further
2 questions.

3 Anything else, Jordan?

4 MR. MAUCOTEL: Nope. Nothing here.

5 MR. THEISS: Great. I think we can
6 close the deposition, then, and go off the
7 record. I assume the court reporter's going to
8 have some had paperwork stuff to do.

9 (Deposition concluded -- 2:31 p.m.)
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C E R T I F I C A T E

I do hereby certify that I am a Notary Public in good standing, that the aforesaid testimony was taken before me, pursuant to notice, at the time and place indicated; that said deponent was by me duly sworn to tell the truth, the whole truth, and nothing but the truth; that the testimony of said deponent was correctly recorded in machine shorthand by me and thereafter transcribed under my supervision with computer-aided transcription; that the deposition is a true and correct record of the testimony given by the witness; and that I am neither of counsel nor kin to any party in said action, nor interested in the outcome thereof.

WITNESS my hand and official seal this
29th day of July, 2025



Notary Public

1 Brandon R. Theiss, Esq.

2 btheiss@vklaw.com

3 July 29, 2025

4 RE: Lenovo (United States) Inc. v. University Of Rochester
(Intellectual Ventures I LLC)

5 7/22/2025, David Kaeli , PhD (#7473235)

6 The above-referenced transcript is available for
7 review.

8 Within the applicable timeframe, the witness should
9 read the testimony to verify its accuracy. If there are
10 any changes, the witness should note those with the
11 reason, on the attached Errata Sheet.

12 The witness should sign the Acknowledgment of
13 Deponent and Errata and return to the deposing attorney.
14 Copies should be sent to all counsel, and to Veritext at
15 cs-midatlantic@veritext.com.

16 Return completed errata within 30 days from
17 receipt of testimony.

18 If the witness fails to do so within the time
19 allotted, the transcript may be used as if signed.

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22 Yours,

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David Kaeli, PhD (#7473235)

E R R A T A S H E E T

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David Kaeli , PhD Date

1 Lenovo (United States) Inc. v. University Of Rochester
2 (Intellectual Ventures I LLC)

3 David Kaeli, PhD (#7473235)

4 ACKNOWLEDGEMENT OF DEPONENT

5 I, David Kaeli , PhD, do hereby declare that I
6 have read the foregoing transcript, I have made any
7 corrections, additions, or changes I deemed necessary as
8 noted above to be appended hereto, and that the same is
9 a true, correct and complete transcript of the testimony
10 given by me.

11 _____
12 David Kaeli, PhD

11 _____
12 Date

13 *If notary is required

14 SUBSCRIBED AND SWORN TO BEFORE ME THIS
15 _____ DAY OF _____, 20____.

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Federal Rules of Civil Procedure

Rule 30

(e) Review By the Witness; Changes.

(1) Review; Statement of Changes. On request by the deponent or a party before the deposition is completed, the deponent must be allowed 30 days after being notified by the officer that the transcript or recording is available in which:

(A) to review the transcript or recording; and

(B) if there are changes in form or substance, to sign a statement listing the changes and the reasons for making them.

(2) Changes Indicated in the Officer's Certificate. The officer must note in the certificate prescribed by Rule 30(f)(1) whether a review was requested and, if so, must attach any changes the deponent makes during the 30-day period.

DISCLAIMER: THE FOREGOING FEDERAL PROCEDURE RULES ARE PROVIDED FOR INFORMATIONAL PURPOSES ONLY.

THE ABOVE RULES ARE CURRENT AS OF APRIL 1, 2019. PLEASE REFER TO THE APPLICABLE FEDERAL RULES OF CIVIL PROCEDURE FOR UP-TO-DATE INFORMATION.

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COMPANY CERTIFICATE AND DISCLOSURE STATEMENT

Veritext Legal Solutions represents that the foregoing transcript is a true, correct and complete transcript of the colloquies, questions and answers as submitted by the court reporter. Veritext Legal Solutions further represents that the attached exhibits, if any, are true, correct and complete documents as submitted by the court reporter and/or attorneys in relation to this deposition and that the documents were processed in accordance with our litigation support and production standards.

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