

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.,
Petitioner,

v.

UNIVERSITY OF ROCHESTER
(INTELLECTUAL VENTURES I LLC),
Patent Owner.

Inter Partes Review No.
IPR2024-01225

Patent No. 7,089,443
Filing: January 23, 2004
Issue Date: August 8, 2006

PETITIONER'S UPDATED EXHIBIT LIST

LISTING OF EXHIBITS

Exhibit	Description
Exhibit 1001	U.S. Patent No. 7,089,443 B2
Exhibit 1002	Declaration of R. Jacob Baker, Ph.D., P.E.
Exhibit 1003	Prosecution History of U.S. Patent No. 7,089,443 B2
Exhibit 1004	U.S. Patent Publication No. 2003/0030326 A1 to Shenai <i>et al.</i> (“ <i>Shenai</i> ”) published on February 13, 2003
Exhibit 1005	International Publication No. WO 01/53921 A1 to Halepete <i>et al.</i> (“ <i>Halepete</i> ”) published on July 26, 2001
Exhibit 1006	U.S. Patent Publication No. 2002/0169990 A1 to Sherburne (“ <i>Sherburne</i> ”) published on November 14, 2002
Exhibit 1007	U.S. Patent No. 5,473,756 to Traylor (“ <i>Traylor</i> ”) issued on December 5, 1995
Exhibit 1008	U.S. Patent No. 6,047,248 to Georgiou <i>et al.</i> (“ <i>Georgiou</i> ”) issued on April 4, 2000
Exhibit 1009	International Publication No. WO 01/33352 A1 to Kranich <i>et al.</i> (“ <i>Kranich</i> ”) published on May 10, 2001
Exhibit 1010	Webpage for Datamath Calculator Museum - archived by WayBackMachine on February 26, 2001 (“ <i>Datamath</i> ”)
Exhibit 1011	Stanley Mazor, <i>The History of the Microcomputer – Invention and Evolution</i> (1995) (“ <i>Mazor</i> ”)
Exhibit 1012	William M. Johnson, <i>Super-Scalar Processor Design</i> , (1989) (“ <i>Johnson</i> ”)
Exhibit 1013	Altera, <i>Excalibur Arm-Based Hardware Reference Manual</i> , January 2001 (“ <i>Excalibur</i> ”)
Exhibit 1014	Texas Instruments, <i>TMS320C64x Technical Overview</i> ,

	January 2001 (“TMS”)
Exhibit 1015	Kenneth C. Yeager, <i>The MIPS R100 Superscalar Microprocessor</i> , (1996) (“Yeager”)
Exhibit 1016	Texas Instruments, <i>FIFO Architecture, Functions, and Applications</i> , November 1999 (“FIFO”)
Exhibit 1017	Eric Tune <i>et al.</i> , <i>Dynamic Prediction of Critical Path Instructions</i> , (2001) (“Tune”)
Exhibit 1018	U.S. Patent No. 6,289,465 B1 to Kuermerle (“Kuermerle”) issued on September 11, 2001
Exhibit 1019	Anand Lal Shimpi, <i>AMD’s K6-2+ in Notebooks – Evaluating Performance with PowerNow</i> , September 12, 2000 (“POWERNOW!”)
Exhibit 1020	Anand Lal Shimpi, <i>AMD’s K6-2+ in Notebooks – Evaluating Performance with PowerNow</i> , September 12, 2000 (“POWERNOW! Operating Modes”)
Exhibit 1021	Bruce R. Childers <i>et al.</i> , <i>Adapting Processor Supply Voltage to Instruction-Level Parallelism</i> , (2001) (“Childers”)
Exhibit 1022	Andrew Royal <i>et al.</i> , <i>GALS, Globally Asynchronous, Locally Synchronous Systems</i> , April 27 th , 2001 (“GALS”)
Exhibit 1023	U.S. Patent No. 6,141,762 to Nicol <i>et al.</i> issued on October 31, 2000 (“Nicol”)
Exhibit 1024	<i>Reserved</i>
Exhibit 1025	<i>Reserved</i>
Exhibit 1026	Actel Corporation, <i>3200DX Dual-Port Random Access Memory (RAM)</i> , September 1997 (“3200DX”)
Exhibit 1027	Barr Group, <i>Types of Memory in Embedded Systems</i> , May 1, 2001

Exhibit 1028	Wavecrest corporation, <i>Understanding Jitter</i> , 2001
Exhibit 1029	U.S. Application No. 60/441,759 filed January 23, 2003
Exhibit 1030	U.S. Patent No. 7,739,537 to Albonesi <i>et al.</i> (“Albonesi”) issued on June 15, 2010
Exhibit 1031	Declaration of Ankit Aggarwal
Exhibit 1032	Declaration of R. Jacob Baker, Ph.D., P.E.
Exhibit 1033	Transcript of Cross-Examination of Dr. David Kaeli
Exhibit 1034	R. Jacob Baker et al., <i>CMOS Circuit Design, Layout, and Simulation</i> , 1998
Exhibit 1035	Graf, <i>Modern Dictionary of Electronics</i> , Seventh Ed., Aug. 11, 1999
Exhibit 1036	T. Burd et al, <i>A Dynamic Voltage Scaled Microprocessor System</i> , IEEE J. Solid-State Circuits, vol. 35, no. 11, pp. 1571-1580, 2000 (“Burd”)
Exhibit 1037 (NEW)	Claim Construction Order and Memorandum in Support Thereof, <i>Intellectual Ventures I LLC v. TCL Electronics Holdings Ltd.</i> , No. 6-23-cv-00309 (W.D. Tex., Sep. 10, 2024), ECF No. 44.

Pursuant to the Board's General Order regarding Related Matters Updates (Paper 19) and the Board's September 29, 2025, email authorizing the parties to file a copy of the claim construction order issued in *Intellectual Ventures I LLC v. TCL Electronics Holdings Ltd.*, No. 6-23-cv-00309 (W.D. Tex.), Petitioner hereby submits this updated exhibit list identifying the claim construction order as new Exhibit 1037. Exhibit 1037 is filed concurrently herewith.

Respectfully submitted,



Dated: Oct. 3, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, the undersigned hereby certifies that this “PETITIONER’S UPDATED EXHIBIT LIST” and Exhibit 1037 were served by filing this document through the Patent Trial and Appeal Case Tracking System (P-TACTS) and via e-mail to the following attorneys of record for the Patent Owner listed below:

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