

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.,

Petitioner,

v.

UNIVERSITY OF ROCHESTER
(INTELLECTUAL VENTURES I, LLC),

Patent Owner.

Case No. IPR2024-01225
U.S. Patent No. 7,089,443

Patent Owner Demonstratives

Independent Claims of the '443 Patent

1. A multiple-clock-domain microprocessor comprising:

a plurality of domains;

for each of the plurality of domains, a clock for separately

generating a clock signal at a frequency for that domain, the frequency being **dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains**; and

for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

8. A method of operating a microprocessor, the method comprising:

(a) providing a plurality of domains in the microprocessor;

(b) **clocking** each of the domains separately at a clock frequency;

(c) applying a voltage to each of the domains separately;

(d) operating the microprocessor such that each domain operates synchronously, **while the domains operate asynchronously relative to one another**; and

(e) dynamically controlling the clock frequency and the voltage in each of the plurality of domains independently of the clock frequencies and the voltages in others of the plurality of domains.

Time Line of the '443 Invention

02/02/2002

Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling*

Greg Semeraro, Grigorios Magklis, Rajeev Balasubramanian,
David H. Albonesi, Sandhya Dwarkadas, and Michael L. Scott

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Abstract

As clock frequency increases and feature size decreases, clock distribution and wire delays present a growing challenge to the designers of singly-clocked, globally synchronous systems. We describe an alternative approach, in which the chip is divided into several (coarse-grained) clock domains, within which independent voltage and frequency scaling can be performed. Boundaries between domains are chosen to exploit existing queues, thereby minimizing inter-domain synchronization costs. We propose four clock domains, corresponding to the front end (including L1 instruction cache), integer units, floating point units, and load/store units (including L1 data cache and L2 cache). We evaluate this design using a simulation infrastructure based on SimpleScalar and Watch. In an attempt to quantify potential energy savings independent of any particular on-line control strategy, we use off-line analysis of traces from a single-speed run of each of our benchmark applications to identify profitable reconfiguration points for a subsequent dynamic scaling run. Dynamic runs incorporate a detailed model of inter-domain synchronization delays, with latencies for intra-domain scaling similar to the whole-chip scaling latencies of Intel XScale and Transmeta LongRun technologies. Using applications from the MediaBench, Olden, and SPEC2000 benchmark suites, we obtain an average energy-delay product improvement of 20% with MCD compared to a modest 3% savings from voltage scaling a single clock and voltage system.

*This work was supported in part by NSF grants CCR-9701915, CCR-9702466, CCR-9705594, CCR-9811929, EIA-9972881, CCR-9988361, and EIA-0080124; by DARPA/ITO under AFRL contract F29601-00-K-0182; and by an external research grant from DEC/Compaq.

EX2005, 1

01/23/2003

The following paper describes the invention and is hereby incorporated by reference in its entirety into the present disclosure: Semeraro et al, "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," *High Performance Computer Architecture (HPCA)*, February 2, 2002.

We claim:

1. A multiple-clock-domain microprocessor comprising:

a plurality of domains; and

for each of the plurality of domains, a clock for separately generating a clock signal for that domain.

2. The microprocessor of claim 1, wherein each said clock comprises a phase-locked loop, and wherein the microprocessor further comprises means for receiving an externally generated clock signal and for supplying the externally generated clock signal to each said phase-locked loop.

3. A method of operating a microprocessor, the method comprising:

providing a plurality of domains in the microprocessor;

clocking each of the domains separately; and

operating the microprocessor such that each domain operates synchronously, while the

domains operate asynchronously relative to one another.

US Provisional 60/441,759

01/23/2004

United States Patent Albonesi et al.

(10) Patent No.: US 7,089,443 B2
(45) Date of Patent: Aug. 8, 2006

(54) MULTIPLE CLOCK DOMAIN MICROPROCESSOR

(75) Inventors: David Albonesi, Rochester, NY (US);
Greg Semeraro, Fairport, NY (US);
Grigorios Magklis, Barcelona (ES);
Michael L. Scott, Rochester, NY (US);
Rajeev Balasubramanian, Rochester,
NY (US); Sandhya Dwarkadas,
Rochester, NY (US)

(73) Assignee: University of Rochester, Rochester,
NY (US)

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 164 days.

(21) Appl. No.: 10/762,550

(22) Filed: Jan. 23, 2004

(65) Prior Publication Data

US 2005/0060597 A1 Mar. 17, 2005

Related U.S. Application Data

(60) Provisional application No. 60/441,759, filed on Jan. 23,
2003.

(51) Int. Cl.
G06F 1/04 (2006.01)

(52) U.S. Cl. 713/501; 713/322; 713/600
(58) Field of Classification Search 713/322,
713/500, 501, 600, 320
See application file for complete search history.

(56) References Cited

U.S. PATENT DOCUMENTS

5,309,561 A 5/1994 Overhouse et al.
5,710,910 A 1/1998 Kohl et al.
5,796,995 A 8/1998 Nasserbakht et al.
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2004/0017234 A1 * 1/2004 Tam et al. 327/141
2004/0025069 A1 * 2/2004 Gary et al. 713/300

* cited by examiner

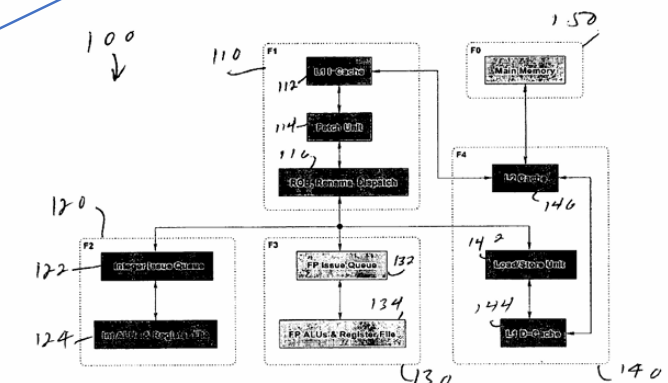
Primary Examiner—Dennis M. Butler

(74) Attorney, Agent, or Firm—Blank Rome LLP

(57) ABSTRACT

A multiple clock domain (MCD) microarchitecture uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. Thus, fully synchronous design practices are used in the design of each domain.

12 Claims, 8 Drawing Sheets



EX1001, 1

"DEMONSTRATIVE EXHIBIT - NOT EVIDENCE"

The Claimed Invention was Reduced to Practice Prior to February 2, 2002

I, David H. Albonesi, make the following declaration based on my own personal knowledge:

1. I am a named inventor of the above-identified patent (hereinafter, '443 Patent) along with my co-inventors Greg Semeraro, Grigorios Magklis, Michael L. Scott, Rajeev Balasubramonian, and Sandhya Dwarkadas. (hereinafter Co-Inventors).

EX2003, 1

20. The Paper also includes a section entitled "4. Results." This section contains the results compiled by my Co-inventors and me and shows the results of testing our invention.

21. The same results contained in "4. Results" is also included in the '443 Patent. (see Col. 13 Ll. 12- Col. 16 Ll. 14) The results described in the Paper and the '443 Patent are one and the same and, as stated above, these results were found before publication of the Paper in February, 2002.

d. "At the same time, by scaling frequency and voltage in different domains dynamically and independently, we can achieve an average improvement in energy-delay product of nearly 20%."

EX2003, 5

24. Accordingly, my Co-Inventors and I had conceived of the invention and actually reduced the invention to practice before the February 2002 publication of the Paper.

25. All statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and these statements are made with the knowledge that willful false statements are punishable by fine and/or imprisonment under 35 U.S.C. §1001, and may jeopardize the validity of this patent and related applications.

26. I Declare under penalty of perjury that the foregoing is true and correct.

Executed on 11/13/2024.

By: David H. Albonesi
David H. Albonesi

EX2003, 6

The Paper Described the Invention

A patent owner can antedate an asserted prior art reference by showing conception and actual reduction to practice prior to the date of the reference. *Medtronic, Inc. v. Teleflex Life Scis. Ltd.*, 86 F.4th 902, 906 (Fed. Cir. 2023). “Conception can be proven with evidence that a full description,” of the invention existed “in written materials disclosed to persons,” in the United States. *Scott v. Koyama*, 281 F. 3d 1243, 1247 (Fed. Cir. 2002). “Reduction to practice in the United States requires that the invention be embodied in tangible form in the United States,” and “that the invention, as conceived, was shown to work for its intended purpose.” *Id.*; *In re Steed*, 802 F. 3d 1311, 1316 (Fed. Cir. 2015). In connection with the requirement that the invention be embodied in a tangible form, it is well-settled that a computer program with executable instructions stored in memory (e.g., on a computer disk) is embodied in a tangible form. *In re Beauregard*, 53 F.3d 1583 (Fed. Cir.1995).

POR, 5

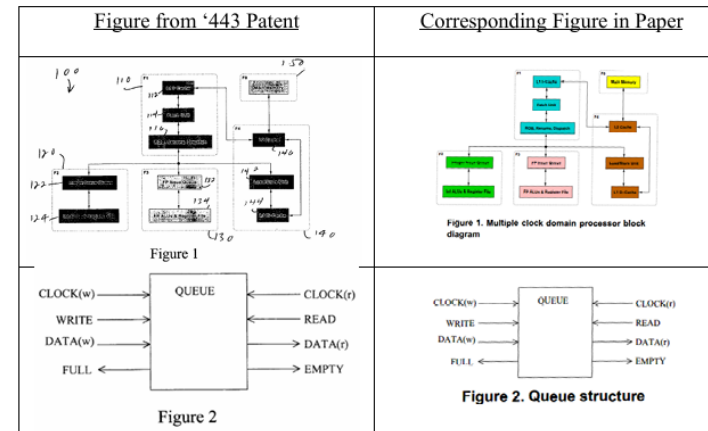
The following paper describes the invention and is hereby incorporated by reference in its entirety into the present disclosure: Semeraro et al, “Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling,” *High Performance Computer Architecture* (HPCA), Feb. 2, 2002. 25

EX1001, 5:22-25

The Paper Described Embodiments Meeting the Claimed Limitations

Actual Reduction to Practice (RTP) requires (1) an embodiment meeting the limitations and (2) proof the invention works for its intended purpose. The Federal Circuit is explicit that the second prong “need not” be proven under “conditions of actual, commercial use.” *Taskett v. Dentlinger*, 344 F.3d 1337, 1341 (Fed. Cir. 2003) (citing *Scott v. Finney*, 34 F.3d 1058, 1063 (Fed. Cir. 1994)). The court approved laboratory proof tailored to the technology, including simulation for a satellite attitude control system—“Thus, it found the simulation adequate.” *Taskett*, 344 F.3d at 1341 (discussing *Williams v. Adm’r of NASA*, 463 F.2d 1391, 1399 (CCPA 1972)). Requiring more would impermissibly demand a “viable commercial embodiment”— “[t]his the law does not require.” *Taskett*, 344 F.3d at 1342.

Sur Reply, 13



Summary of Invention of '443 Patent	Corresponding Language In the Introduction of Paper
It is another object of the invention to provide an approach that	An approach that
allows for aggressive future frequency increases, maintains a synchronous design methodology, and exploits the trend towards making functional blocks more autonomous.	allows for aggressive future frequency increases, maintains a synchronous design methodology, and exploits the trend towards making functional blocks more autonomous, is ...
To achieve the above and other objects, the present invention is directed to	
a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable	a <i>multiple clock domain (MCD)</i> microarchitecture, which uses a <i>globally-asynchronous, locally-synchronous (GALS)</i> clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable

A multiple-clock-domain microprocessor comprising:	“An approach that allows for aggressive future frequency increases, maintains a synchronous design methodology, and exploits the trend towards making functional blocks more autonomous, is a <u>multiple clock domain</u> (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an <u>MCD microprocessor</u> each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. ... In this Paper, we describe an initial implementation of an MCD microprocessor ...” EX2005, 2 (emphasis added).
a plurality of domains;	“We describe an alternative approach, which we call a Multiple Clock Domain (MCD) processor, in which the chip is divided into <u>several (coarse-grained) clock domains</u>, within which independent voltage and frequency scaling can be performed.” EX2005, Abstract (emphasis added).
for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and	“We describe an alternative approach, which we call a Multiple Clock Domain (MCD) processor, in which the chip is divided into several (coarse-grained) clock domains, <u>within which independent voltage and frequency scaling can be performed.</u>” EX2005, Abstract (emphasis added).
for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.	“Figures 8 and 9 both illustrate the value of using <u>different frequencies in different clock domains; by controlling these frequencies independently</u> we can maintain the required frequency in domains that are critical to performance, while aggressively scaling those domains that are less performance-critical.” EX2005, 10 (emphasis added). “We describe an alternative approach, which we call a Multiple Clock Domain (MCD) processor, in which the chip is divided into several (coarse-grained) clock domains, <u>within which independent voltage and frequency scaling can be performed.</u>” EX2005, Abstract (emphasis added). “[B]y <u>scaling frequency and voltage in different domains dynamically and independently</u>, we can achieve an average improvement in energy-delay product of nearly 20%.” EX2005, 11 (emphasis added).

The Paper Provided Proof it Worked for It's Intended Purposes

Ex. 1033, 103:23-105:1. Patent Owner has produced no evidence of any physical prototype of the claimed microprocessor that could have validated the simulation. See Paper 14, 15-17. At most, the alleged SimpleScalar simulation demonstrated feasibility for prototyping of a microprocessor. *Standard Mfg. Co. v. United States*, 25 Cl. Ct. 1, 67 (1991) (“The feasibility of the optical alignment system may have been proven by the optical mock-up, but the optical mock-up was not a reduction to practice of the proposed MHU-145/M trailer.”)

Reply, 13-14

“The defendant has stipulated that no actual prototype of the MHU-145/M loader was ever built. In actuality, design work was less than 50 percent complete, and no manufacturing drawings existed from which a prototype could have been constructed.”

[Std. Mfg. Co. v. United States, 25 Cl. Ct. 1, 65](#)

20. The Paper also includes a section entitled “4. Results.” This section contains the results compiled by my Co-inventors and me and shows the results of testing our invention.

21. The same results contained in “4. Results” is also included in the ‘443 Patent. (see Col. 13 Ll. 12- Col. 16 Ll. 14) The results described in the Paper and the ‘443 Patent are one and the same and, as stated above, these results were found before publication of the Paper in February, 2002.

24. Accordingly, my Co-Inventors and I had conceived of the invention and actually reduced the invention to practice before the February 2002 publication of the Paper.

26. I Declare under penalty of perjury that the foregoing is true and correct.

Executed on 11/13/2024.

By: David H. Albonesi
David H. Albonesi

EX2003, 6

RTP does not Require a “viable commercial embodiment”

Petitioner’s refrain that “a microprocessor is a physical item” (Reply, 14–15) cannot raise the bar: the Federal Circuit confirms the “works for intended purpose” prong “need not” be proven under commercial conditions and expressly approves laboratory proof, including simulation; demanding a tape-out would improperly require a “viable commercial embodiment.” *Taskett v. Dentlinger*, 344 F.3d 1337, 1341–42 (Fed. Cir. 2003). On this record, the apparatus of claims 1–7 was reduced to practice prior to the critical date.

Sur-Reply, 15-16

For the method claims (e.g., claim 8), the antedation inquiry is whether the claimed steps were performed—not whether a chip was fabricated. The record shows they were. First, the inventors implemented the offline analysis that computes per-domain frequency/voltage schedules and feeds them back for a second, dynamic run, i.e., executing the method’s per-domain DVFS control in operation. EX1001, 12:27–35. Second, the simulation models independent clocks with independent jitter to capture asynchronous inter-domain crossings and their timing/CDC costs, matching the claim requirement that domains operate synchronously within and asynchronously across domains. EX1001, 12:51–63; 17:63–18:1. Third, the specification describes the queue/flag boundary behavior used at domain interfaces and characterizes the overall methodology as an “existence proof” of the invention’s intended energy/performance benefits—i.e., the method, as performed, worked for its intended purpose. EX1001, 12:41–44; 17:55–18:8. See also POR, 22–23 (actual RTP on a host; “worked for intended purpose”).

Sur-Reply, 16

As Dr. Kaeli explained during his Deposition:

“Q. If one of your Ph.D students were to say, “I have this great branch prediction algorithm that improves performance by 50 percent,” what would you like to see the prove to you.

A. I’d like to see where they gen – where they got 50 percent. Generally, if they’re a student 10 working in my group, they would be using an execution-driven or cycle-based simulator that would, basically, be evaluating the particular they’d have a baseline design and then they’d 14 simulate their design and evaluate how much a performance changed. And I -- that would be completely acceptable and publishable and accepted by both academia and industry.

Q. So if they showed it to you, the simulation results, you would think it worked?

A. I would -- again, they would have had to demonstrate it across a representative set of workloads that, basically, are deemed, you know, appropriate for evaluating branch prediction, and -- and -- and, you know, that their results are repeatable and demonstrateable, yep.”

EX1033, 109:22-110:-25

Sur-Reply, 14

Shenai is not Prior Art

Shenai Time Line

8/10/2001

11/5/2001

11/5/2001

11/5/2001

8/12/2002

08-13-01 A/PREV

PROVISIONAL APPLICATION FOR PATENT COVER SHEET
This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(a).

INVENTORS
Name: Shenai, Shunai
Residence: Naperville, Illinois
City and other State or Foreign Country: Naperville, Illinois

ADDITIONAL INVENTORS
Name: Shenai, Shunai
Residence: Naperville, Illinois
City and other State or Foreign Country: Naperville, Illinois

TITLE OF THE INVENTION
Distributed Power and Supply Architecture

REFERENCE TO PRIOR APPLICATIONS
This application is a continuation-in-part of U.S. Patent Application No. 09/000,000, filed on 08/10/2001.

ABSTRACT
A power distribution management apparatus for supplying power to two or more loads includes a power and clock distribution controller capable of determining voltage, current and clock signal frequency targets for the loads. The apparatus also includes two or more power sources responsive to the controller so as to be selectively coupled with the loads to provide the target voltage and current to the loads. The power sources have switching frequencies of at least one megahertz. The apparatus further includes two or more clock signal sources responsive to the controller and coupled with the loads so as to provide clock signals to the loads at the target frequencies.

CLAIMS
1. A power distribution management apparatus for supplying power to two or more loads, comprising:
a power and clock distribution controller capable of determining voltage, current and clock signal frequency targets for the loads;
two or more power sources responsive to the controller so as to be selectively coupled with the loads to provide the target voltage and current to the loads;
two or more clock signal sources responsive to the controller and coupled with the loads so as to provide clock signals to the loads at the target frequencies.

FIGURES
FIG. 1 is a block diagram of a power distribution management apparatus in accordance with the present invention. The apparatus includes a power and clock distribution controller 100, a static converter 120, a quad-static frequency controller 140, a clock signal source 130, and a load 110. The controller 100 is connected to the static converter 120, the quad-static frequency controller 140, the clock signal source 130, and the load 110. The static converter 120 is connected to the quad-static frequency controller 140. The quad-static frequency controller 140 is connected to the clock signal source 130. The clock signal source 130 is connected to the load 110.

12-10-01 A/PREV

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12-10-01 A/PREV

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12-11-01 A/PREV

PROVISIONAL APPLICATION FOR PATENT COVER SHEET
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INVENTORS
Name: Shenai, Shunai
Residence: Naperville, Illinois
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ADDITIONAL INVENTORS
Name: Shenai, Shunai
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CLAIMS
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(19) United States
(12) Patent Application Publication
Shenai et al.

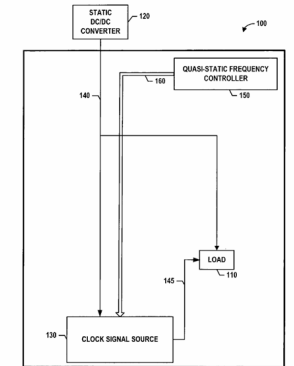
(109) Pub. No.: US 2003/0030326 A1
(43) Pub. Date: Feb. 13, 2003

(54) DISTRIBUTED POWER AND SUPPLY ARCHITECTURE
(57) Abstract
A power distribution management apparatus for supplying power to two or more loads includes a power and clock distribution controller capable of determining voltage, current and clock signal frequency targets for the loads. The apparatus also includes two or more power sources responsive to the controller so as to be selectively coupled with the loads to provide the target voltage and current to the loads. The power sources have switching frequencies of at least one megahertz. The apparatus further includes two or more clock signal sources responsive to the controller and coupled with the loads so as to provide clock signals to the loads at the target frequencies.

(73) Inventors: Krishna Shenai, Naperville, IL (US); Erik A. McShane, Lockport, IL (US)

(75) Assignee: Shakti Systems, Inc.
(21) Appl. No.: 10/217,840
(22) Filed: Aug. 12, 2002

(60) Provisional application No. 60/311,575, filed on Aug. 10, 2001. Provisional application No. 60/337,837, filed on Nov. 5, 2001. Provisional application No. 60/338,510, filed on Nov. 5, 2001.



EX2006

EX2007

EX2008

EX2009

Shenai Provisionals

Shenai
(EX1004)

02/02/2002

"DEMONSTRATIVE EXHIBIT - NOT EVIDENCE"

Shenai's Claims are Not Supported by the Provisionals Therefore are Not Entitled to the Filing Date

1. A power distribution management apparatus for supplying power to a plurality of loads, the apparatus comprising:

a power and clock distribution controller capable of determining voltage, current and clock signal frequency targets for the plural loads;

plural power sources responsive to the controller so as to be selectively coupled with the loads to provide the target voltage and current to the loads, wherein the power sources have switching frequencies of at least one megahertz; and

plural clock signal sources responsive to the controller and coupled with the loads so as to provide clock signals to the loads at the target frequencies.

EX1004, Claim 1

30. An electronic system comprising:

a plurality of loads;

a power and clock distribution controller capable of determining voltage, current and clock signal frequency targets for the loads;

plural power sources responsive to the controller and coupled with the plural loads so as to provide the target voltages and currents to the loads; and

plural clock signal sources responsive to the controller and coupled with the plural loads so as to provide clock signals to the loads at the target frequencies.

EX1004, Claim 30

35. A power distribution management apparatus for supplying power to a plurality of loads, the apparatus comprising:

a power and clock distribution controller capable of determining voltage, current and clock signal frequency targets for the plural loads;

plural regulated power sources coupled with at least one static power supply, the regulated power sources being responsive to the controller so as to be selectively coupled with the loads to provide the target voltage and current to the loads, wherein the power sources have switching frequencies of at least one megahertz;

plural clock signal sources responsive to the controller and coupled with the loads so as to provide clock signals to the loads at the target frequencies;

EX1004, Claim 35

“A reference patent is only entitled to claim the benefit of the filing date of its provisional application if the disclosure of the provisional application provides support for the claims in the reference patent in compliance with § 112.” *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1382 (Fed. Cir. 2015). Here, the Petitioner has failed to show that the Provisional Applications support claim 1 (or any other claim).

POR, 38-39

Shenai's Claims are Not Supported by the Provisionals Therefore are Not Entitled to the Filing Date

The Provisional Application (Ex. 2006) fails to mention a controller that determines current targets for plural loads. Rather, the controller in the Provisional Application only determines voltage and frequency targets. Ex. 2006, 12 (characterizing permitting “combined frequency and voltage scaling,” without mentioning control of current). The Reply (at 2) cites the following from the Provisional Application as allegedly supporting determining current targets:

... Fourth is a controller circuit which dynamically specifies the connections to be made by the cross-bridge network between the power sources and loads. (Ex. 2006, 8)

[T]o control the cross-bridge network, to specify dynamically the voltage output by each of n power sources, and to specify the clock frequency delivered to each of m load clusters, a dynamic controller is provided. It is envisioned that the dynamic controller will operate with the cooperation of [] power optimization algorithms ... (Ex. 2006, 12) (emphasis added).

[T]he architecture accommodates ... strategies in the cross-bridge network between the power sources and the load clusters to permit optimization of power, control complexity, or size. (Ex. 2006, 12)

These passages do not disclose determining current targets for plural loads. Rather, the disclosure regarding the determination of current targets was first introduced in Shenai's utility application, which disclosed in part:

Power and clock distribution controller 450 may be capable of determining voltage, current and clock signal frequency targets for the plural loads. Ex. 1004, [0026] (emphasis added).

... DC/DC converters 470-476 may be responsive to controller 450, such that they are selectively coupled with loads 410-416 to provide the respective target voltages and currents to the loads. *Id.*, [0031] (emphasis added).

Since the Provisional Applications fail to disclose a controller that determines current targets for plural loads, it fails to provide written description support for claim 1 as required by *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1382 (Fed. Cir. 2015); *see also, Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1323 (Fed. Cir. 2000) (to meet the written description requirement, “one skilled in the art, reading the original disclosure, must immediately discern” the material); *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1352 (Fed. Cir. 2010) (*en banc*) (“[A] description that merely renders the invention obvious does not satisfy the [written description] requirement.”)

Shenai's Provisionals Never Mention a Microprocessor Therefore are Not Entitled to the Filing Date

Claim 1 of the '443 Patent recites the domains of a "multiple-clock-domain microprocessor," and Ground 1 relies solely on Shenai (Ex. 1004) for this aspect of Claim 1. However, the Provisional Application (Ex. 2006) lacks written description support for a microprocessor. The Reply (at 3) argues :

Ex. 2006's "controller circuit" and power sources "integrated monolithically along with the load clusters using existing integrated circuit (IC) fabrication techniques" would be understood to provide written description for a "microprocessor."

POR, 41

As made clear by the Federal Circuit, "to claim priority to provisional filing date, the portion of the application relied on by the [Challenges] as prior art must be supported by the provisional application." *In re Riggs*, 131 F.4th 1377, 1384 (Fed. Cir. 2025). Since the Petition does not identify how the portion relied upon is supported by the Provisional, Shenai cannot render the Challenged Claims obvious under 35 U.S.C. §103.

POR, 42

The Provisional Application does not say that its "controller circuit"/power sources/load clusters are a microprocessor, nor do such components provide inherent support for a "microprocessor." The Reply does not explain why a controller circuit/power sources/load clusters must be "capable of receiving and executing coded instructions" -- because there is no such requirement." [W]hen an explicit limitation . . . is not present in the written description whose benefit is sought it must be shown that ... the description requires that limitation." *Hyatt v. Boone*, 146 F.3d 1348, 1353 (Fed. Cir. 1998) (emphasis added). Here, nothing in the Provisional Application requires that the "load clusters" be a microprocessor.² Therefore, the generic disclosure of "load clusters" in the Provisional Application fails to provide written description support for a specific implementation where the "load clusters" are a microprocessor. See *In re Smith*, 458 F.2d 1389, 1395, (CCPA 1972). (description of a genus failed to support claims to a species within the genus).

POR, 41-42

Shenai Teaches a “Rational Factor”

Problem to Be Solved Time Line

8/1992

United States Patent [19]
Pratt et al.

[11] Patent Number: 5,634,041
[45] Date of Patent: May 27, 1997

[54] **RATIONALLY CLOCKED COMMUNICATION INTERFACE**
[75] Inventors: Gill A. Pratt, Wellesley; Stephen A. Ward, Chestnut Hill, both of Mass.
[73] Assignee: Massachusetts Institute of Technology, Cambridge, Mass.
[21] Appl. No.: 929,879
[22] Filed: Aug. 11, 1992
[51] Int. Cl. G06F 1/12
[52] U.S. Cl. 395/553
[58] Field of Search 395/550, 650, 395/700

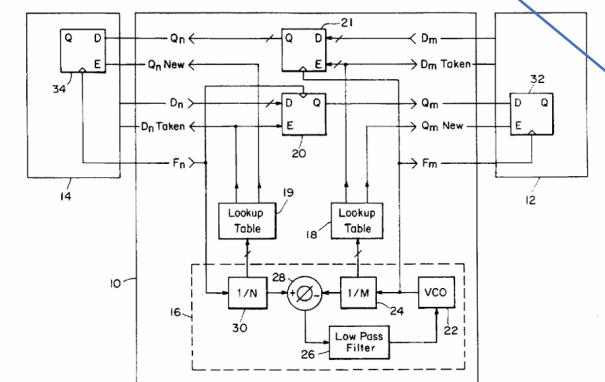
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Primary Examiner—Kevin A. Kriess
Assistant Examiner—John Q. Chavis
Attorney, Agent, or Firm—Hamilton, Brook, Smith & Reynolds, P.C.

ABSTRACT
An interface controlling digital communication between synchronous systems of unequal clock frequency. A phase locked loop generates one clock F_n from the other F_m by locking the phase of the two clocks at a beating period. Within the beating period, a precompiled set of valid and invalid communication clock cycles for each direction of communication are scheduled into lookup tables. The lookup tables generate outputs to a Set of registers for communicating data between the systems of unequal clock frequency.

14 Claims, 5 Drawing Sheets



EX2011, 1

10/1995

Rational Clocking

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Abstract

Communication between independently clocked digital subsystems typically involves a finite probability of synchronization failure whose minimization introduces delays and consequent performance costs. This paper explores a technique that eliminates both the inherent unreliability of such communication and the performance overhead it implies. Our approach maintains a known phase relationship between clocks whose frequencies are related by a rational factor, and exploits the predictability of their relative phases to algorithmically time communications without run-time arbitration contests.

1 Introduction

The designer of a digital system is often confronted with the need to establish communication between synchronous subsystems operating at different clock speeds. This problem occurs in heterogeneous multiprocessor systems, and in uniprocessor systems where the processor and bus are clocked independently.

Asynchronous solutions to this problem, which assume the systems' clocks to be completely independent, are typically inefficient because they must allow for sufficiently long synchronization delays to attain acceptable levels of reliability [1, 2, 3, 4]. Synchronous solutions are more efficient and reliable, but have traditionally lacked flexibility because they require the clock frequencies to be related by integer factors [6, 7].

In this paper, we present an efficient and flexible solution, called *rational clocking*, that allows data to be transferred reliably and efficiently between two systems whose clock frequencies are related by the ratio of two small integers. This rational frequency constraint allows a wide variety of frequencies to be used, while assuring a periodic relationship between the two clocks that can be used to determine a schedule for transferring data between the two systems.

* A U.S. patent application has been filed on behalf of MIT covering portions of this work.

1063-6404/95 \$4.00 © 1995 IEEE

2 Basic Implementation

In rational clocking, we use two clocks, Clk_m and Clk_n , with frequencies f_m and f_n , such that

$$\frac{f_m}{f_n} = \frac{M}{N} \quad (1)$$

where M and N are integers, and such that their active edges are known to coincide at some point in time. The active edges of such clocks will coincide periodically with a coincidence period, T_{MN} , equal to:

$$T_{MN} = MT_M = NT_N \quad (2)$$

where T_M and T_N are the two clocks' periods, and will define coincidence cycles equal in length to an integer number of cycles on each system (i.e., M cycles on system m , and N cycles on system n).

Given the frequency ratio M/N , we can predict the relative positions of the systems' clock edges within a coincidence cycle and generate a *schedule* of safe and unsafe cycles for data transfers. This makes it possible to ensure reliable communication by synchronously inhibiting data transfers during the predetermined unsafe cycles. Since the clock interactions are periodic, the same schedule can be applied every M clock cycles on system m and N clock cycles on system n .

2.1 Hardware Implementation

Figure 1 shows a simple circuit implementing this idea. In this circuit, a phase-locked loop (PLL) and two frequency-dividing counters are used to obtain Clk_n from Clk_m , while ensuring the desired phase and frequency relationships. (The characteristics of the PLL may limit the operational range of this circuit. However, this problem is orthogonal to the present discussion, and will not be discussed in this paper.) The values in the frequency-dividing counters indicate the current clock cycle (within the coincidence cycle) of their respective systems, and are used to index two lookup tables. Each lookup table produces two control signals per clock cycle number: TE (Transmit Enable), which controls the transmitting register, and RE (Receive Enable), which controls the receiving

02/02/2002

Some synchronization schemes restrict the phase relationship and relative frequencies of the clocks, thereby eliminating the need for hardware arbitration [27]. Unfortunately, these schemes impose significant restrictions on the possible choices of frequencies. In addition, the need to control the phase relationships of the clocks means that global clock synchronization is required. Our design specifically recognizes the overhead associated with independent clocks with no known phase relationship. We believe this overhead to be unavoidable in an MCD processor: one of the motivating factors for the design is the recognition that traditional global clock distribution will become increasingly difficult in the future.

The issue queues in the integer, floating point, and load/store domains (the Load/Store Queue within the Load/Store Unit), together with the Reorder Buffer (ROB) in the front end domain, serve to decouple the front and back ends of a conventional processor. Choosing these queues as inter-domain synchronization points has the advantage of hiding the synchronization cost whenever the queue is neither full nor empty (as described later in this section).

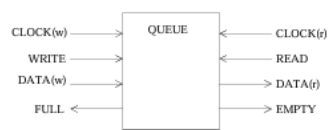


Figure 2. Queue structure

EX2004, 1

EX2005, 3

POSITA's Appreciated Rational Clocking was Different than Non-Constrained Clocking

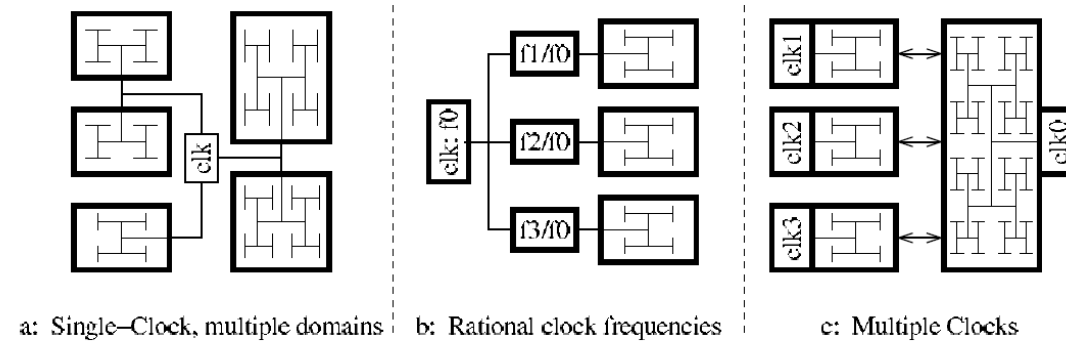


Figure 1. Chips with Multiple Clock Domains

EX2012, 2

Figure 1.b depicts a design where different portions of the chip operate at different frequencies, and the various clocks are derived from a common source. This commonly occurs in system-on-chip designs where different IP blocks operate at different clock frequencies or in multi-rate digital-signal-processing designs. Although multiple clock frequencies are used, these frequencies are exact rational multiples of each other, and these ratios are typically known in advance or are determined by pre-designed operating modes of the design. Knowing the exact relationship between the various clock frequencies enables the design of an interface that operates with low latency and without synchronization. Section 6 describes our design for this scenario.

The essential observation behind our designs is that clocks for synchronous systems are designed to be extremely stable. Thus, we can design STARI style interfaces that provide moderate amounts of skew tolerance and dynamically compensate for any long-term drift. As described above, we present designs when the sender and receiver operate at exactly the same frequency; at frequencies that are rational multiples of each other; at closely matched frequencies; and at arbitrary, relatively stable frequencies. In the remainder of the paper, we show that these designs are small and can operate at high clock frequencies with low latencies.

EX2012, 2

The Patent Specifically Overcomes Limits of Constrained Clocks

When a patentee describes the features of the “present invention,” it is well-settled that “this description limits the scope of the invention.” *Pacing Techs., LLC v. Garmin Int’l, Inc.*, 778 F.3d 1021 (Fed. Cir. 2015). In this regard, the “Summary of the Invention” of the ‘443 Patent states that the “present invention” uses a globally-asynchronous clocking style:

... the *present invention* is directed to a multiple clock domain (MCD) microarchitecture, which uses a *globally-asynchronous*, locally-synchronous (GALS) clocking style. In an MCD microprocessor *each functional block operates with a separately generated clock*, and synchronizing circuits ensure reliable inter-domain communication. ... an MCD microprocessor affords a number of potential advantages over a singly clocked design: ...

The *independence* of each *local domain clock* implies no global skew requirement... EX1001, 4:13-31 (emphasis added).

Thus, the claim language reciting “for each of the plurality of domains, a clock for *separately* generating a clock signal at a frequency for that domain, the frequency being dynamically changeable *independently* of the frequencies of the clock signals generated for others of the plurality of domains,” requires that the separate clocks in the plurality of domains be globally-asynchronous. As Dr. Kaeli explains, the “Patent ‘443 overcomes earlier limitations of GALS systems by developing novel methods to support using independent clock and independent voltage controls, overcoming issues related to inter-domain synchronization and communication.”

EX2013, ¶30.

POR, 20

It would have been readily apparent to a POSITA reading the entirety of the ‘443 Patent that the specification criticized prior synchronization systems—such as those described in Sarmenta (EX2004), Pratt (EX2011), and Chakraborty (EX2012)—that restricted the freedom to select clock frequencies by requiring a rational relationship between clock domains to enable synchronized communication.¹ The criticized systems relied on predetermined, fixed frequency ratios to establish deterministic timing intervals for data transfer, inherently imposing design constraints. To overcome the limitations of such systems, the ‘443 Patent explained that the invention provides “[t]he designers of each domain [to be] no longer constrained by the speeds of critical paths in other domains, affording them greater freedom in each domain to optimize the tradeoffs among clock speed, latency, and the exploitation of application parallelism via complex hardware structures.” EX1001, 4:34-39.

POR, 23

¹ As explained in the ‘443 Patent: “Some synchronization schemes *restrict the phase relationship and relative frequencies of the clocks*, thereby eliminating the need for hardware arbitration [27]. *Unfortunately, these schemes impose significant restrictions on the possible choices of frequencies*. In addition, the need to control the phase relationships of the clocks means that global clock synchronization is required. *Our design specifically recognizes the overhead associated with independent clocks with no known phase relationship*. We believe this overhead to be *unavoidable* in an MCD processor ... EX1001, 6:32-42.

The Constraints of Prior Art Systems

A *coincidence cycle* refers to the periodic interval during which the active (typically rising) edges of two independently clocked systems realign. These systems, referred to as system m and system n , operate at different clock frequencies, but their frequencies are related by a rational ratio $f_m / f_n = M / N$, where M and N are small integers. This means that the period of system m 's clock (T_m) and system n 's clock (T_n) are also related such that $T_n / T_m = M / N$. The key insight of rational clocking is that, despite the systems running at different rates, the relative phase relationship between their clocks is predictable and periodic. Specifically, every M clock cycles of system m and N clock cycles of system n , the two clocks' active edges coincide again. This recurring alignment defines the *coincidence cycle*.

EX2013, ¶32.

POR, 27

For example, Sarmenta states:

“Given the frequency ratio M/N , we can predict the relative positions of the systems' clock edges within a coincidence cycle and generate a schedule of safe and unsafe cycles for data transfers. **This makes it possible to ensure reliable communication by synchronously inhibiting data transfers during the predetermined unsafe cycles.** Since the clock interactions are periodic, the same schedule can be applied every M clock cycles on system m and N clock cycles on system n .” EX2004, 1

POR, 27-28

"DEMONSTRATIVE EXHIBIT - NOT EVIDENCE"

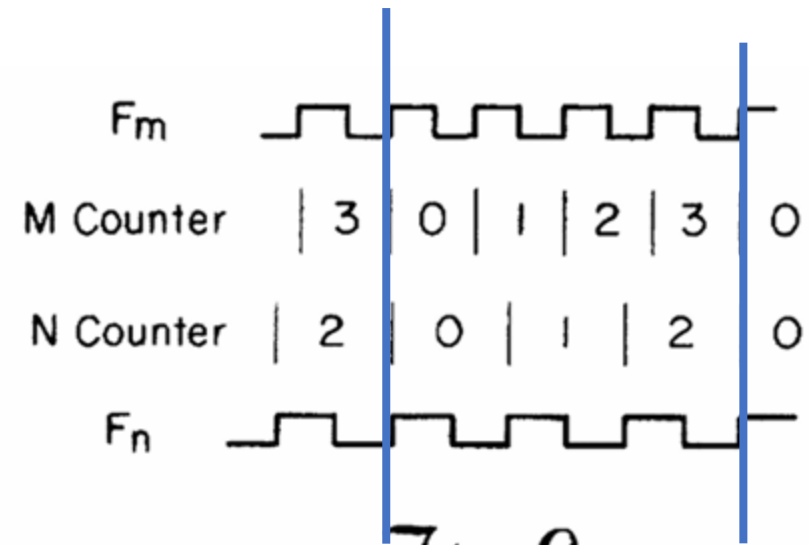


Fig. 2

POR, 30

“The slave clock source may be generated from the master clock source by a M/N phase locked loop. The M/N phase locked loop defines a rational frequency relationship between the processing units. This allows the present invention to generate one clock from the other. The clock frequencies, F_m and F_n , are related by the ratio of two integers M and N . **From this relationship, the beating period or locking phase of the clocks is used to schedule a precompiled set of valid and invalid communication clock cycles for transmitting and receiving data between the processing units. Since phase interaction is periodic, this pattern of valid and invalid cycles repeats itself every M clocks for processor M and every N clocks for processor N .**”

EX2011

POR, 30-31

Shenai Teaches Rational Factors of a Common Clock

Specifically, ¶[0036] of Shenai explains:

Additionally, clock/shifters 430-436 may comprise, phase-locked-loop circuits, delay-locked-loop circuits, or combinational logic circuits for supplying clock signals to loads 410-416. These circuits may operate **at an integer multiplication, a half-integer multiplication or a quarter-integer multiplication of a reference clock signal.** Controller 450 may provide the reference clock signal, though the invention is not so limited. Alternatively, these circuits may operate **at an integer division, a half-integer division and a quarter-integer division of the reference clock signal.** Such configurations may allow for synchronous communication between loads 410-416, as opposed to asynchronous communication, which may be undesirable.³

Accordingly, as Dr. Kaeli explains, “[t]he clock frequency control described in Shenai generates a clock frequency that is based on a rational multiple of a reference clock signal.” EX2013, ¶99. Therefore, like in Sarmenta, there is a “rational factor” relationship in Shenai between the clock signal provided to each of the loads that ensures that the clocks align periodically, creating predictable points in time where the active edges of both clocks coincide. See, EX1004, [0036] (noting that the disclosed configurations may “allow for *synchronous* communication between loads.”) (emphasis added). This approach fundamentally contradicts the

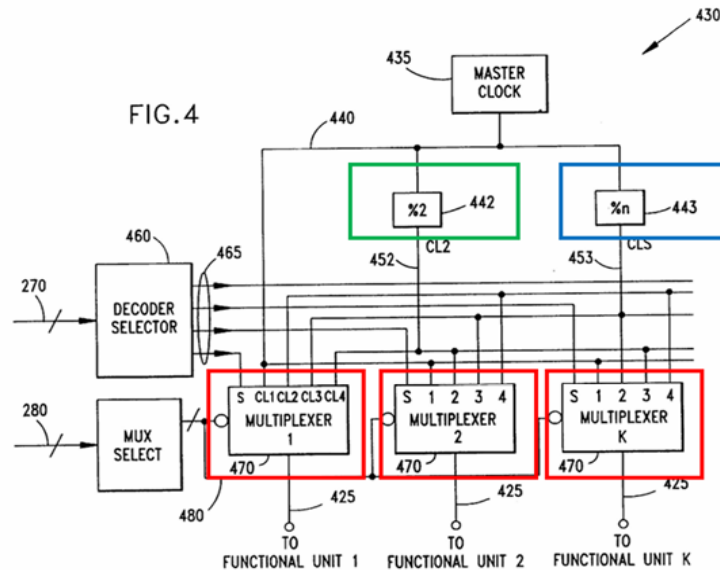
POR, 47-48

However, as the ‘443 Patent observes when discussing Sarmenta, “these schemes impose significant restrictions on the possible choices of frequencies.” EX1001, 6:35-37. To overcome the limitations of systems like Sarmenta, the ‘443 Patent explains that invention provides “[t]he designers of each domain [to be] no longer constrained by the speeds of critical paths in other domains, affording them greater freedom in each domain to optimize the tradeoffs among clock speed, latency, and the exploitation of application parallelism via complex hardware structures.” EX1001, 2:34-39. Accordingly, while Sarmenta introduces a synchronization approach leveraging rational frequency relationships, it imposes significant restrictions on frequency selection, as acknowledged in the ‘443 Patent. Dr. Kaeli explains, “The ‘443 invention overcomes these limitations, offering independence in clock frequency generation, allowing each frequency domain to adopt their own independent frequency, offering near infinite resolution in terms of the clock frequency selected for each domain.” EX2013, ¶34

POR, 44-45

Georgiou Teaches a “Rational Factor”

Georgiou Teaches Rational Factors of a Common Clock



Georgiou specifically states that “clock divider 442 may be a divide-by-two clock divider whose output frequency 452 is one-half that of the master clock frequency 440, and clock divider 443 may be divide-by-n clock divider whose output frequency 453 is one-nth that of the master clock frequency 440.” EX1008, 8:42-47.

POR, 51-52

However, the output of the multiplexer 470 does not satisfy the claim language reciting “for each of the plurality of domains, a clock for *separately* generating a clock signal at a frequency for that domain, the frequency being dynamically changeable *independently* of the frequencies of the clock signals generated for others of the plurality of domains” (claim 1) and “dynamically controlling the clock frequency ... in *each* of the plurality of domains *independently* of the clock frequencies” (Claim 12). Instead, Georgiou is describing a synchronized system like Sarmenta and Pratt that maintains global synchronization by restricting the possible choice of frequencies to those related by a “rational factor” (i.e., related by the ratio of two small integers, (M/N) in order to utilize a “coincidence cycle” for synchronization. EX2013, ¶123-124.

POR, 57-58

domain frequencies in each domain is constrained, and the relative frequencies across domains are similarly limited to a fixed set of relationships. Changing the master frequency rescales every available fraction; and the relative relationships among domains are fixed to the same rational set. That is the antithesis of “independently changeable” domain frequencies as required by the ‘443 Patent.

EX1008, 8:37-47; EX1001, 17:19-27; POR, 54-57.

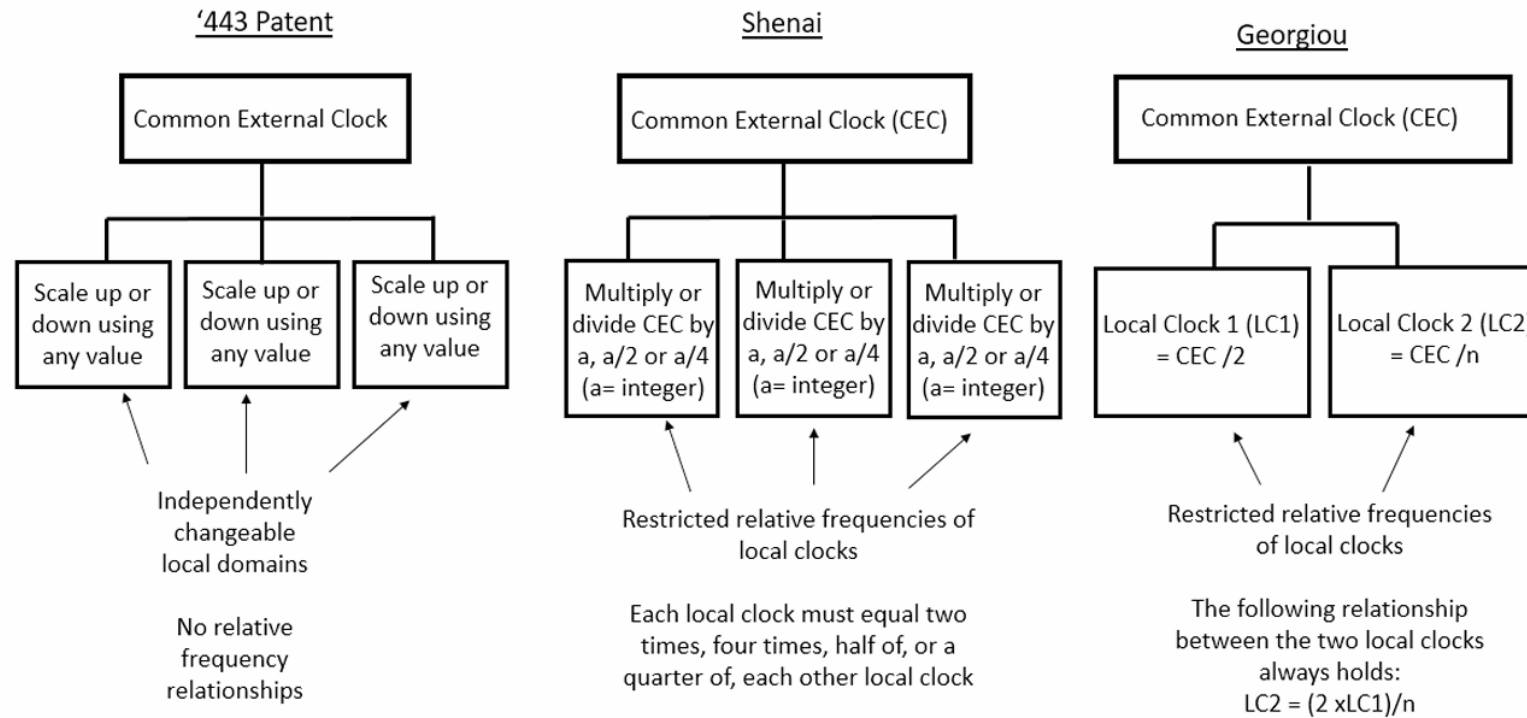
Sur-Reply, 10

“Independence” means freedom from other domain constraints—not merely “not literally derived from another domain’s clock”

Petitioner’s gloss reduces “independent” to “not directly derived from another domain’s clock.” Reply, 24–26. The ‘443 patent doesn’t use the terms “derive” or “derived” anywhere, let alone in connection with its discussion of independent domain clocks. Instead, the ‘443 Patent explains that independently changeable clocks are ones that do not “restrict the ... relative frequencies of the clocks” or “impose significant restrictions on the possible choices of frequencies.” EX1001, 6:32-36. The intrinsic evidence makes clear that such schemes are outside the scope of domains with clocks that are “changeable independently” from the frequencies of the clock signals in the other domains, as claimed.

Sur-Reply 7-8

The '443 is Fundamentally Different than Shenai and Georgiou



Sur-Reply 6

Conclusion

Grounds I-IV Fail for the following reasons:

- Shenai is not entitled to the earlier filing dates of the provisional
 - Provisionals do not provide support for all of the elements for at least claim
 - Provisionals never disclose a microprocessor
- The '443 was reduced to practice prior to February 2, 2020
 - Semeraro describes the claimed invention
 - No legal requirement for “commercial availability”
 - The simulation shows that the invention worked for its intended purposes
- Shenai imposes a “rational factor” requirement which is the exact problem the inventors were trying to avoid.

Ground V-VI Fails for the following reasons:

- Georgiou imposes a “rational factor”
- Limits frequencies to a limited number of preconfigured frequencies