

LENOVO (UNITED STATES) INC.

v.

UNIVERSITY OF ROCHESTER
(INTELLECTUAL VENTURES I LLC)

IPR2024-01225 (Patent No. 7,089,443 B2)

Petitioner's Demonstrative Exhibit

November 17, 2025

Roadmap

Overview

- '443 Patent
- *Shenai* Prior Art Reference
- *Georgiou* Prior Art Reference

Disputes

- Challenged Claims do not require construction
- *Shenai* is prior art to the '443 patent
- *Shenai* teaches domains with independently changeable frequencies
- *Georgiou* teaches domains with independently changeable frequencies

Overview of the '443 Patent


US007089443B2

(12) **United States Patent**
Albonesi et al.

(10) **Patent No.:** **US 7,089,443 B2**
(45) **Date of Patent:** **Aug. 8, 2006**

(54) **MULTIPLE CLOCK DOMAIN MICROPROCESSOR**

(75) **Inventors:** **David Albonesi**, Rochester, NY (US); **Greg Semeraro**, Fairport, NY (US); **Grigoris Magklis**, Barcelona (ES); **Michael L. Scott**, Rochester, NY (US); **Rajeev Balasubramanian**, Rochester, NY (US); **Sandhya Dwarkadas**, Rochester, NY (US)

(73) **Assignee:** **University of Rochester**, Rochester, NY (US)

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 164 days.

(21) **Appl. No.:** **10/762,550**
(22) **Filed:** **Jan. 23, 2004**
(65) **Prior Publication Data**
US 2005/0060597 A1 Mar. 17, 2005

Related U.S. Application Data
(60) Provisional application No. 60/441,759, filed on Jan. 23, 2003.

(51) **Int. CL**
G06F 1/04 (2006.01)

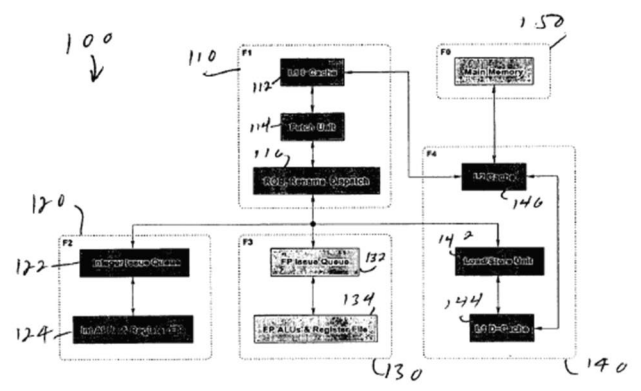
(52) **U.S. CL** **713/501; 713/522; 713/600**
(58) **Field of Classification Search** **713/500, 501, 600, 320**
See application file for complete search history

(56) **References Cited**
U.S. PATENT DOCUMENTS
5,309,561 A 5/1994 Overhouse et al.
5,710,910 A 1/1998 Kehl et al.
5,796,995 A 8/1998 Nasserbakht et al.
6,047,382 A 4/2000 Maley et al.
6,403,547 B1 10/2002 Bailey et al.
6,487,675 B1 11/2002 Sager et al.
2004/0017234 A1 * 1/2004 Tam et al. 327/141
2004/0025069 A1 * 2/2004 Gary et al. 713/300
* cited by examiner

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(57) **ABSTRACT**
A multiple clock domain (MCD) microarchitecture uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. Thus, fully synchronous design practices are used in the design of each domain.

12 Claims, 8 Drawing Sheets



1 of 19

Petitioner Lenovo (United States) Inc. - Ex. 1001

- US 7,089,443 B2
- “Multiple Clock Domain Microprocessor”
- Claims priority to a provisional application filed **January 23, 2003**

Claims 1 and 8 of the '443 Patent

1. A multiple-clock-domain microprocessor comprising:
a plurality of domains;
for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and
for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

8. A method of operating a microprocessor, the method comprising:
(a) providing a plurality of domains in the microprocessor;
(b) clocking each of the domains separately at a clock frequency;
(c) applying a voltage to each of the domains separately;
(d) operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another; and
(e) dynamically controlling the clock frequency and the voltage in each of the plurality of domains independently of the clock frequencies and the voltages in others of the plurality of domains.

Overview of Grounds

IPR 2024-01225 – Instituted Grounds

Grounds	Claim	Reference(s)
Ground 1: § 103	1, 3-5, 8-9, 12	<i>Shenai</i>
Ground 2: § 103	4, 9	<i>Shenai, Halepete</i>
Ground 3: § 103	5-7, 10, 11	<i>Shenai, Sherburne</i>
Ground 4: § 103	7	<i>Shenai, Sherburne, Traylor</i>
Ground 5: § 103	1, 3, 8, 12	<i>Georgiou</i>
Ground 6: § 103	4, 9	<i>Georgiou, Halepete</i>
Ground 7: § 103	5, 10	<i>Georgiou, Kranich</i>

* All disputes relate to *Shenai* and *Georgiou*.

Roadmap

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- *Georgiou* teaches domains with independently changeable frequencies

Overview of Shenai



US 20030030326A1

(19) **United States**
 (12) **Patent Application Publication** (10) **Pub. No.: US 2003/0030326 A1**
 Shenai et al. (43) **Pub. Date: Feb. 13, 2003**

(54) **DISTRIBUTED POWER AND SUPPLY ARCHITECTURE**

(75) Inventors: Krishna Shenai, Naperville, IL (US);
 Erik A. McShane, Lockport, IL (US)

filed on Nov. 5, 2001. Provisional application No. 60/337,479, filed on Nov. 5, 2001. Provisional application No. 60/338,510, filed on Nov. 5, 2001.

Publication Classification

(51) **Int. Cl.**⁷ **H02J 1/12**
 (52) **U.S. Cl.** **307/21; 307/29**

ABSTRACT

A power distribution management apparatus for supplying power to two or more loads includes a power and clock distribution controller capable of determining voltage, current and clock signal frequency targets for the loads. The apparatus also includes two or more power sources responsive to the controller so as to be selectively coupled with the loads to provide the target voltage and current to the loads. The power sources have switching frequencies of at least one megahertz. The apparatus further includes two or more clock signal sources responsive to the controller and coupled with the loads so as to provide clock signals to the loads at the target frequencies.

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(73) Assignee: Shakti Systems, Inc.

(21) Appl. No.: 10/217,840

(22) Filed: Aug. 12, 2002

Related U.S. Application Data

(60) Provisional application No. 60/311,575, filed on Aug. 10, 2001. Provisional application No. 60/337,837,

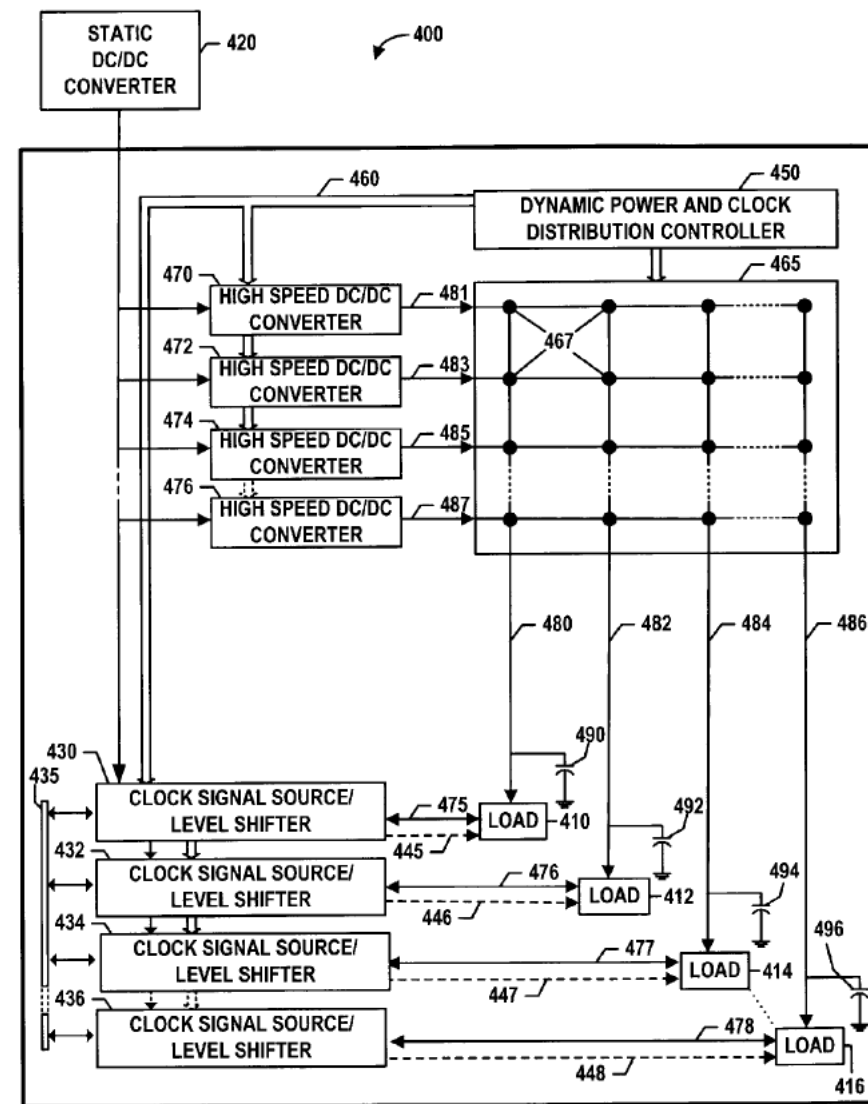


FIGURE 4

Ex. 1004, pp. 1, 5

Roadmap

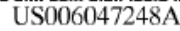
Overview

- '443 Patent
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- *Georgiou* teaches domains with independently changeable frequencies

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



[11] **Patent Number:** 6,047,248
[45] **Date of Patent:** Apr. 4, 2000

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

[75] Inventors: **Christos John Georgiou**, White Plains;
Edward Scott Kirkpatrick,
Croton-on-Hudson; **Thor Arne Larsen**,
Hopewell Junction, all of N.Y.

OTHER PUBLICATIONS

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

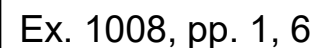
(List continued on next page.)

[21] Appl. No.: 09/226,097

[22] Filed: **Oct. 19, 1998**

Related U.S. Application Data

[63] Continuation of application No. 08/639,586, Apr. 29, 1996, Pat. No. 5,940,785.

[57] **ABSTRACT**

Roadmap

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1. The Challenged Claims Do Not Require Construction

“The Patent Owner maintains that the Challenged Claims should have their plain and ordinary meaning.”

Paper 14, p. 19

1. A multiple-clock-domain microprocessor comprising:
a plurality of domains;
for each of the plurality of domains, a clock for separately
generating a clock signal at a frequency for that
domain, the frequency being dynamically changeable
independently of the frequencies of the clock signals
generated for others of the plurality of domains; and
for each of the plurality of domains, a voltage input for
receiving a voltage which is dynamically changeable
independently of the voltages applied to said others of
the plurality of domains.

Ex. 1001, claim 1

1. The Challenged Claims Do Not Require Construction

Patent Owner nevertheless offers various limiting constructions.

- Claim 1 allegedly “requires that the separate clocks in the plurality of domains be globally-asynchronous.”
- Claim 1 allegedly “does not cover synchronized systems like Sarmenta that maintain global synchronization by restricting the possible choice of frequencies to those related by a ‘rational factor’.”
- Claims are allegedly “limited to systems that permit each domain to operate at independently selected, dynamically changeable frequencies without global synchronization constraints.”

Paper 7, p. 20;
Paper 14, p. 20

Paper 7, p. 24

Paper 14, p. 24

1. The Challenged Claims Do Not Require Construction

Patent Owner offers various limiting constructions.

- Claims allegedly require that “each domain must be free to generate and change its clock frequency without being tethered to **small integer multiples** of the other domains.”
- Claims allegedly “require domain-local clocks without **rational-ratio tethering**, and **GALS operation** that is **synchronous** within a domain and **asynchronous** across domains.”
- Claims allegedly “require that each domain generate its clock signal independently, and that the frequency of each domain’s clock be dynamically changeable without being constrained by the frequencies of other domains.”

Paper 18, p. 18

Paper 14, pp. 36-37

Paper 14, pp. 36-37

1. The Challenged Claims Do Not Require Construction

**Limitations alleged by Patent Owner are contrary to the
“plain and ordinary meaning.”**

1. A multiple-clock-domain microprocessor comprising:
a plurality of domains;
for each of the plurality of domains, a clock for separately
generating a clock signal at a frequency for that
domain, the frequency being dynamically changeable
independently of the frequencies of the clock signals
generated for others of the plurality of domains; and
for each of the plurality of domains, a voltage input for
receiving a voltage which is dynamically changeable
independently of the voltages applied to said others of
the plurality of domains.

Claim 1 does not recite any of:

- “small integer multiples”
- “GALS” / “synchronization”
- “rational factor” / “rational ratio”

Paper 17, pp. 8-11; Ex. 1001, claim 1 (annotated)

1. The Challenged Claims Do Not Require Construction

Limitations alleged by Patent Owner are unsupported by the specification.

To achieve the above and other objects, the present invention is directed to a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. Thus, fully synchronous design practices are used in the design of each domain. Although the inter-domain synchronization increases the number of clock cycles required to run a given application, an MCD microprocessor affords a number of potential advantages over a singly clocked design:

The global clock distribution network is greatly simplified, requiring only the distribution of the externally generated clock to the local Phase Lock Loop (PLL) in each domain.

The independence of each local domain clock implies no global clock skew requirement, permitting potentially higher frequencies within each domain and greater scalability in future process generations.

While a preferred embodiment of the present invention has been set forth above, those skilled in the art who have reviewed the present disclosure will readily appreciate that other embodiments can be realized within the scope of the invention. For example, numerical values and fabrication techniques are illustrative rather than limiting. Also, while four domains have been disclosed, it is possible to implement a processor with more or fewer domains and with different boundaries among the domains. Other possible variations of the invention have been noted above. Therefore, the present invention should be construed as limited only by the appended claims.

Paper 17, pp. 8-11; Paper 14, pp. 19-22; Ex. 1001, 4:13-33, 16:63-17:7 (annotated)

1. The Challenged Claims Do Not Require Construction

Limitations alleged by Patent Owner are unsupported by the specification.

The primary disadvantage of an MCD processor is the performance overhead due to inter-domain synchronization. In this section, we discuss the circuitry required to perform this synchronization. We discuss how to model its performance cost below.

Some synchronization schemes restrict the phase relationship and relative frequencies of the clocks, thereby eliminating the need for hardware arbitration [27]. Unfortunately, these schemes impose significant restrictions on the possible choices of frequencies. In addition, the need to control the phase relationships of the clocks means that global clock synchronization is required. Our design specifically recognizes the overhead associated with independent clocks with no known phase relationship. We believe this overhead to be unavoidable in an MCD processor: one of the motivating factors for the design is the recognition that traditional global clock distribution will become increasingly difficult in the future.

[27] L. F. G. Sarmenta, G. A. Pratt, and S. A. Ward. Rational Clocking. In *Proceedings of the International Conference on Computer Design*, Austin, Tex., October 1995.

Specification includes no “clear and unmistakable statement of disavowal of claim scope.”

See Mercedes-Benz USA, LLC v. Carucel Investments, LP, IPR2019-01404, Paper 38, 19-20 (Jan. 15, 2021) (distinguishing *Pacing Technologies*).

Paper 17, pp. 8-11; Paper 14, pp. 19-22; Ex. 1001, 6:27-44 (annotated)

1. The Challenged Claims Do Not Require Construction

The claims cannot be construed to exclude the Preferred Embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Matzke has estimated that as technology scales down to a 0.1 μm feature size, only 16% of the die will be reachable within a single clock cycle [24]. Assuming a chip multiprocessor with two processors per die, each processor would need to have a minimum of three equal-size clock domains. The preferred embodiment uses four domains, one of which includes the L2 cache, so that domains may vary somewhat in size and still be covered by a single clock. In effect, we treat the main memory interface as a fifth clock domain, external to the MCD processor, and always running at full speed.

To achieve the above and other objects, the present invention is directed to a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. Thus, fully synchronous design practices are used in the design of each domain. Although the inter-domain synchronization increases the number of clock cycles required to run a given application, an MCD microprocessor affords a number of potential advantages over a singly clocked design:

The global clock distribution network is greatly simplified, requiring only the distribution of the externally generated clock to the local Phase Lock Loop (PLL) in each domain.

Ex. 1001, 4:13-29, 5:49-62 (annotated); Paper 17, pp. 11-12

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2. *Shenai* is Prior Art

Shenai is prior art for either of the following reasons:

- 1) Patent Owner did not reduce claims to practice; or
- 2) *Shenai* predates the alleged reduction to practice.

8/10/2001

8/12/2002

Alleged Simulation
(2/2002)

'443 Earliest Priority
Claim (1/20/2003)

US 20030030326A1

(19) **United States**
(12) **Patent Application Publication**
Shenai et al.

(10) Pub. No.: US 2003/0030326 A1
(43) Pub. Date: Feb. 13, 2003

(54) **DISTRIBUTED POWER AND SUPPLY ARCHITECTURE**

(75) Inventors: Krishna Shenai, Naperville, IL (US);
Erik A. McShane, Lockport, IL (US)

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(21) Appl. No.: 10/217,840
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Related U.S. Application Data
(60) Provisional application No. 60/311,575, filed on Aug. 10, 2001; Provisional application No. 60/357,857, filed on May 10, 2002.

filed on Nov. 5, 2001. Provisional application No. 60/337,479, filed on Nov. 5, 2001. Provisional application No. 60/338,510, filed on Nov. 5, 2001.

Publication Classification

(51) Int. Cl.⁷ H02J 1/12
(52) U.S. Cl. 307/21; 307/29

(57) **ABSTRACT**
A power distribution management apparatus for supplying power to two or more loads includes a power and clock distribution controller capable of determining voltage, current and clock signal frequency targets for the loads. The apparatus also includes two or more power sources responsive to the controller so as to be selectively coupled with the loads to provide the target voltage and current to the loads. The power sources have switching frequencies of at least one megahertz. The apparatus further includes two or more clock signal sources responsive to the controller and coupled with the loads so as to provide clock signals to the loads at the target frequencies.

Paper 17, pp. 12-19; Ex. 1004, p. 1 (annotated)

2. Patent Owner Has Not Proved Reduction to Practice

All claims recite a microprocessor.

1. A multiple-clock-domain microprocessor comprising:
a plurality of domains;
for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and
for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

8. A method of operating a microprocessor, the method comprising:
(a) providing a plurality of domains in the microprocessor;
(b) clocking each of the domains separately at a clock frequency;
(c) applying a voltage to each of the domains separately;
(d) operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another; and
(e) dynamically controlling the clock frequency and the voltage in each of the plurality of domains independently of the clock frequencies and the voltages in others of the plurality of domains.

2. Patent Owner Has Not Proved Reduction to Practice

The alleged SimpleScalar simulation did not embody any claim in “tangible form.”

Q. And a microprocessor is a physical item.
Is that true?
A. Yes.

Q. Is the simulation data produced as, like, a file at the output of the SimpleScalar system? Like a data file, is that what it produces?
A. I forget the exact output format. It could have been on a screen, or it could have been in a file. And I'm sure you can write what's on a screen to a file, because that's what ends up happening, so . . .
Q. Okay. But it doesn't produce software or fabricate anything like a 3D printer; is that correct?
A. No.

Ex. 1033, 84:2-4, 88:11-23 (annotated)

2. Patent Owner Has Not Proved Reduction to Practice

The alleged SimpleScalar simulation preceded any tangible embodiment.

Q. Does the SimpleScalar system produce anything physical; for instance, fabricating hardware?

A. What SimpleScalar does is gives you guidance on the potential benefits of -- and, possibly, the guidance on sizing and dimensions of what you might want to fabricate.

The whole purpose between, you know, using a simulator like this is to avoid the cost of going through the fabrication process each time, which is both time-consuming and very expensive, and provides you with, you know, a good validation of your architectural idea.

You know, if you want to get cycle-accurate, go build the hardware, but, you know, maybe a couple million dollars later talk to me.

Q. Is that generally how --

A. This is how -- this is how -- this is how industry does their work, okay? You know, this is not -- I'm very familiar with it.

Q. So once the simulation is created, how is it validated?

A. It's validated against real hardware.

Ex. 1033, 87:20-88:7, 103:15-25 (annotated)

2. Patent Owner Has Not Proved Reduction to Practice

None of the cases on which Patent Owner relies held that a simulation qualifies as a reduction to practice of a physical device.

- *Taskett v. Dentlinger* – third-party institution not required for step of “obtaining financial authorization”
- *Williams v. Adm’r of NASA* – lab testing of a physical satellite
- *Scott v. Finney* – demonstration in a human patient of a physical prosthetic implant

2. *Shenai* is Entitled to the Filing Date of the Provisional

The Provisional supports claim 1.

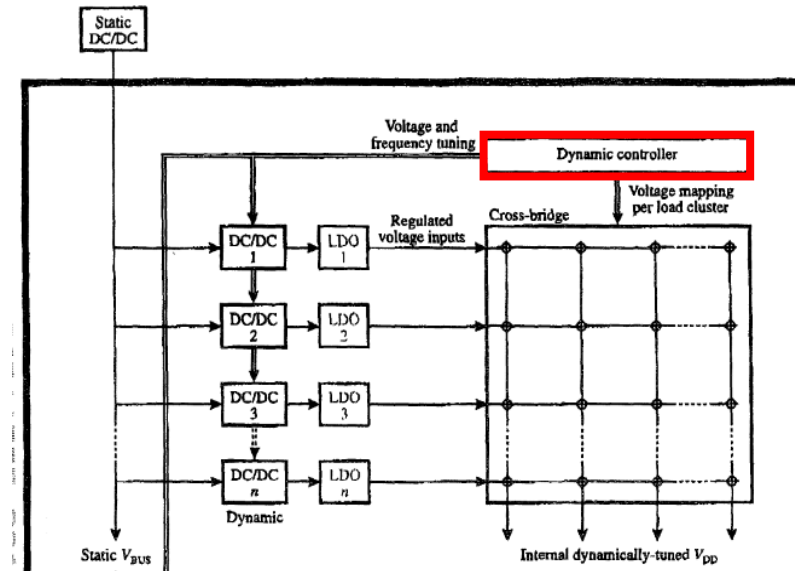
1. A power distribution management apparatus for supplying power to a plurality of loads, the apparatus comprising:

a power and clock distribution controller capable of determining voltage, current and clock signal frequency targets for the plural loads;

plural power sources responsive to the controller so as to be selectively coupled with the loads to provide the target voltage and current to the loads, wherein the power sources have switching frequencies of at least one megahertz; and

plural clock signal sources responsive to the controller and coupled with the loads so as to provide clock signals to the loads at the target frequencies.

Ex. 1004, claim 1 (annotated)



Ex. 2006, p. 17 (annotated)

Finally, to control the cross-bridge network, to specify dynamically the voltage output by each of n power sources, and to specify the clock frequency delivered to each of m load clusters, a dynamic controller is provided. It is envisioned that the dynamic controller will operate with the cooperation of scheduling software, operating system prioritization, or dynamic performance and power optimization algorithms as known to the art.

Ex. 2006, p. 12 (annotated)

2. *Shenai* is Entitled to the Filing Date of the Provisional

Dr. Baker's testimony as to support for claim 1 stands unrebutted.

A. Current

21. Ex. 2006 explains that the “dynamic controller” shown in the top right corner of Figure 2 is provided to “specify dynamically the voltage output by each of n power sources, and to specify the clock frequency delivered to each of m load clusters.” Ex. 2006, 12. Ex. 2006 further states that the “dynamic controller will operate with the cooperation of scheduling software, operating system prioritization, or dynamic performance and power optimization algorithms.” *Id.* According to Ex. 2006, the architecture “will reduce load cluster power dissipation to 10% to 50% of that delivered by the present state-of-the-art.” *Id.*

22. Power (P) is related to voltage (V) and (I) by the following equation:

$$P = V * I$$

23. To reduce load cluster power dissipation as in Ex. 2006, the dynamic controller would also specify current. By specifying both current through the n power sources and voltage, the dynamic controller would be able to manage power dissipation, which is proportional to both current and voltage. Without specifying the current, the dynamic controller could not effectively manage power dissipation, at least because power dissipation would vary proportionally with current. A POSITA reading Ex. 2006 would have immediately recognized this at least because

the proportional relationship of power to both voltage and current is an elementary principle of electronic circuits.

24. Further, the dynamic controller described in Ex. 2006 would also be capable of specifying circuit parameters other than voltage and frequency, including current. Configuring the dynamic controller to specify current in addition to voltage and frequency would be a routine matter of adjusting the scheduling software, operating system prioritization, and/or optimization algorithms used with the dynamic controller. A POSITA reading Ex. 2006 would have recognized that the dynamic controller could be configured to perform simple calculations.

25. A POSITA would have therefore recognized that the inventors of Ex. 2006 possessed a controller both capable of specifying currents and, more specifically, configured to specify currents.

Ex. 1032, ¶¶ 21-25; see *also* Paper 18, pp. 17-18

2. *Shenai* is Entitled to the Filing Date of the Provisional

The Provisional supports a microprocessor.

- Microprocessor = “an electronic integrated circuit, typically a single-chip package, capable of receiving and executing coded instructions.”
- No dispute that Ex. 2006 discloses an integrated circuit.

Ex. 1035, p. 6, Ex. 1032, ¶ 26

See Paper 14, pp. 40-42; Paper 18, pp. 17-18

Finally, to control the cross-bridge network, to specify dynamically the voltage output by each of n power sources, and to specify the clock frequency delivered to each of m load clusters, a dynamic controller is provided. It is envisioned that the dynamic controller will operate with the cooperation of scheduling software, operating system prioritization, or dynamic performance and power optimization algorithms as known to the art.

Ex. 2006, p. 12; Ex. 1032, ¶ 27 (annotated)

2. *Shenai* is Entitled to the Filing Date of the Provisional

Dr. Baker's testimony as to support for a microprocessor stands unrebutted.

27. As previously mentioned, Ex. 2006 states that the “dynamic controller will operate with the cooperation of scheduling software, operating system prioritization, or dynamic performance and power optimization algorithms.” *Id.* For “cooperation” with software, an OS, or optimization algorithms, the dynamic controller would necessarily receive and execute instructions to perform computations as directed by the software, OS, and/or algorithms. As this was an ordinary application of a controller in August 2001, a POSITA would have recognized from Ex. 2006 that at least the dynamic controller portion of the architecture would have to be “capable of receiving and executing coded instructions.”

28. Based on the foregoing, a POSITA would have recognized that the architecture described in Ex. 2006 would meet the accepted definition of a “microprocessor.”

29. Additionally, Ex. 2006 is directed to solutions for minimizing power consumption while maintaining performance in electronic systems using voltage scaling and/or frequency scaling. Ex 2006, 8-9. In the “Background of the Invention” section, where the state of the art is typically described in similar papers, Ex. 2006 references earlier research by Thomas D. Burd that was documented in an IEEE paper titled “A Dynamic Voltage Scaled Microprocessor System.” Ex. 2006, 9. Burd’s paper describes a voltage scaling and frequency scaling approach implemented specifically on microprocessors. By Ex. 2006’s reference to Burd’s microprocessor research in the background section, a POSITA would have concluded that the subject matter of Ex. 2006 improves upon or otherwise modifies Burd’s microprocessor research. A POSITA would have also concluded that Ex. 2006 is directed to microprocessor technology, as was Burd’s research, and describes a microprocessor.

Ex. 1032, ¶¶ 27-29; see also Paper 18, pp. 17-18

Roadmap

Overview

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- *Georgiou* Prior Art Reference

Disputes

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- *Shenai* is prior art to the '443 patent
- *Shenai* teaches domains with independently changeable frequencies
- *Georgiou* teaches domains with independently changeable frequencies

3. *Shenai* Teaches Independent Domain Frequencies

There is no dispute that *Shenai* teaches the highlighted claim language without Patent Owner's limiting construction.

1. A multiple-clock-domain microprocessor comprising:
a plurality of domains;
for each of the plurality of domains, a clock for separately
generating a clock signal at a frequency for that
domain, the frequency being dynamically changeable
independently of the frequencies of the clock signals
generated for others of the plurality of domains; and
for each of the plurality of domains, a voltage input for
receiving a voltage which is dynamically changeable
independently of the voltages applied to said others of
the plurality of domains.

Paper 17, pp. 8-11; Paper 14, pp. 19-22; Paper 18, pp. 11-12; Ex. 1001, claim 1 (annotated)

3. *Shenai* Teaches Independent Domain Frequencies

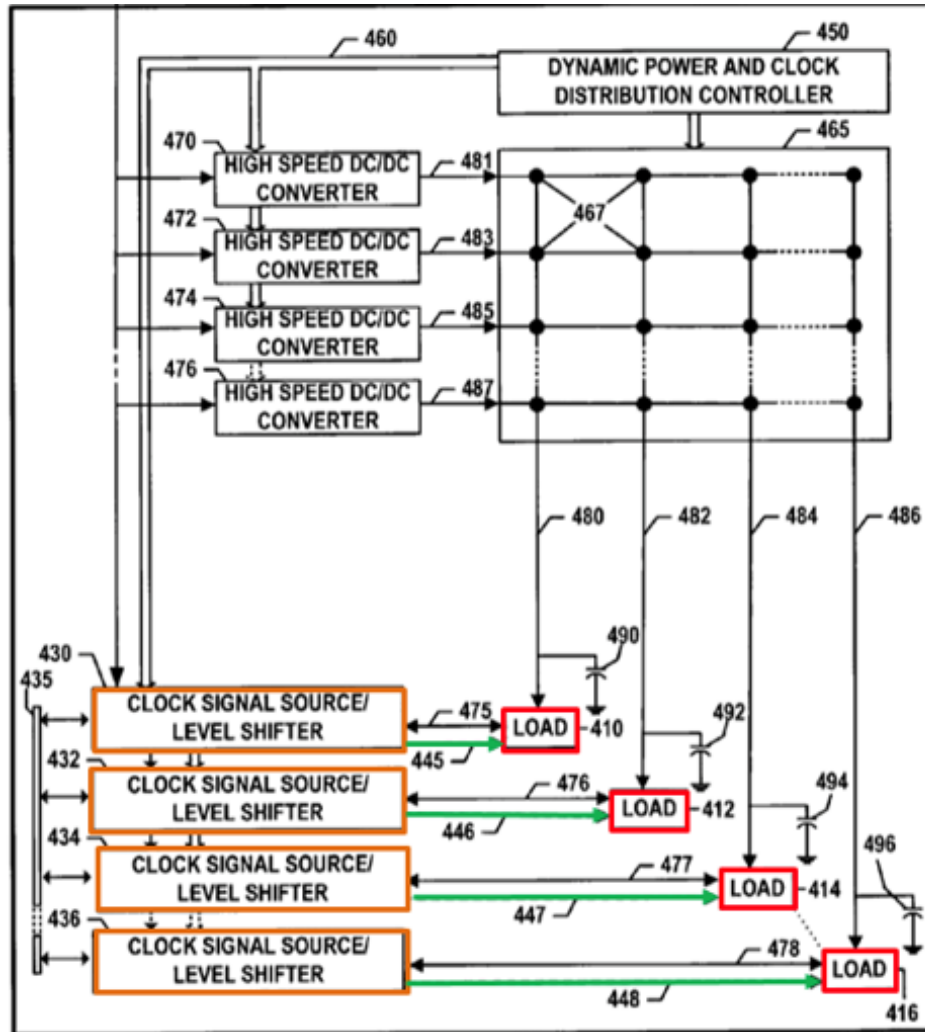


FIGURE 4

“for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains”

3. *Shenai* Teaches Independent Domain Frequencies

***Shenai* teaches independent clock signals at target frequencies.**

[0035] Circuit 400 may further include plural clock signal sources/level shifters (clock/shifters) 430, 432, 434 and 436, which may be coupled with a logic bus 435 for communication with other devices or components. Clock/shifters 430-436 may also be responsive to controller 450 and coupled with loads 410-416 so as to provide clock signals via clock signal buses 445, 446, 447 and 448 to the loads at the target frequencies, which may be determined by controller 450, as has been previously described. As was previously discussed, clock/shifters 430-436 may also include circuitry that allows electrical signal communication between loads operating at varying target voltages via signal buses 475, 476, 477 and 478. Such an approach may

3. *Shenai* Teaches Independent Domain Frequencies

***Shenai* does not require use of integer multiples.**

[0036] Additionally, clock/shifters 430-436 may comprise, phase-locked-loop circuits, delay-locked-loop circuits, or combinational logic circuits for supplying clock signals to loads 410-416. These circuits may operate at an integer multiplication, a half-integer multiplication or a quarter-integer multiplication of a reference clock signal. Controller 450 may provide the reference clock signal, though the invention is not so limited. Alternatively, these circuits may operate at an integer division, a half-integer division and a quarter-integer division of the reference clock signal. Such configurations may allow for synchronous

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Both *Shenai* and the '443 patent describe distribution of a clock to PLLs.

The global clock distribution network is greatly simplified, requiring only the distribution of the externally generated clock to the local Phase Lock Loop (PLL) in each domain.

Paper 17, pp. 19-20; Ex. 1001, 4:25-29 (annotated)

Additionally, information from DC/DC converters and clock circuits, such as those described below, may also be communicated to controller 450 via bus 460. Such information may include circuit activity information, as described herein, information from clock circuits regarding lock state, such as for phase-locked-loop circuits, for example, or any other information controller 450 might employ when managing power and clock distribution.

Paper 17, pp. 19-20; Ex. 1004, ¶ 29 (annotated)

3. *Shenai* Teaches Independent Domain Frequencies

***Shenai* teaches independence of domains.**

[0025] Referring now to **FIG. 4**, an embodiment of a power distribution management circuit **400** in accordance with the invention is shown. Circuit **400** may for be used to balance power consumption and performance for plural loads **410**, **412**, **414** and **416**, though the invention is not so limited and fewer or additional loads may be included with circuit **400**. Loads **410-416** may be individual components, functional blocks of a single component or independent systems. Typical loads may include an analog to digital

Paper 17, p. 20; Ex. 1004, ¶ 25 (annotated)

[0042] For embodiments of the invention, such as illustrated in **FIG. 4**, such loads may be partitioned. With the use of high-speed, regulated DC/DC converters, as previously described, each load of a partitioned (or dynamically partitioned) complex electronic system may function at voltage and frequency values that allow the load to realize the power savings shown in **FIG. 5** by line **520**. That is, some non-critical components may be provided with clock and voltage settings that allow them to operate lower down (further to the left on curve **520**), while only those load clusters that must operate at a higher level of performance operate at a higher point on curve **520**. In this respect, the aggregate power savings realized by embodiments of the invention may be substantially greater than prior bulk and quasi-static approaches.

Paper 17, p. 22; Ex. 1004, ¶ 42 (annotated)

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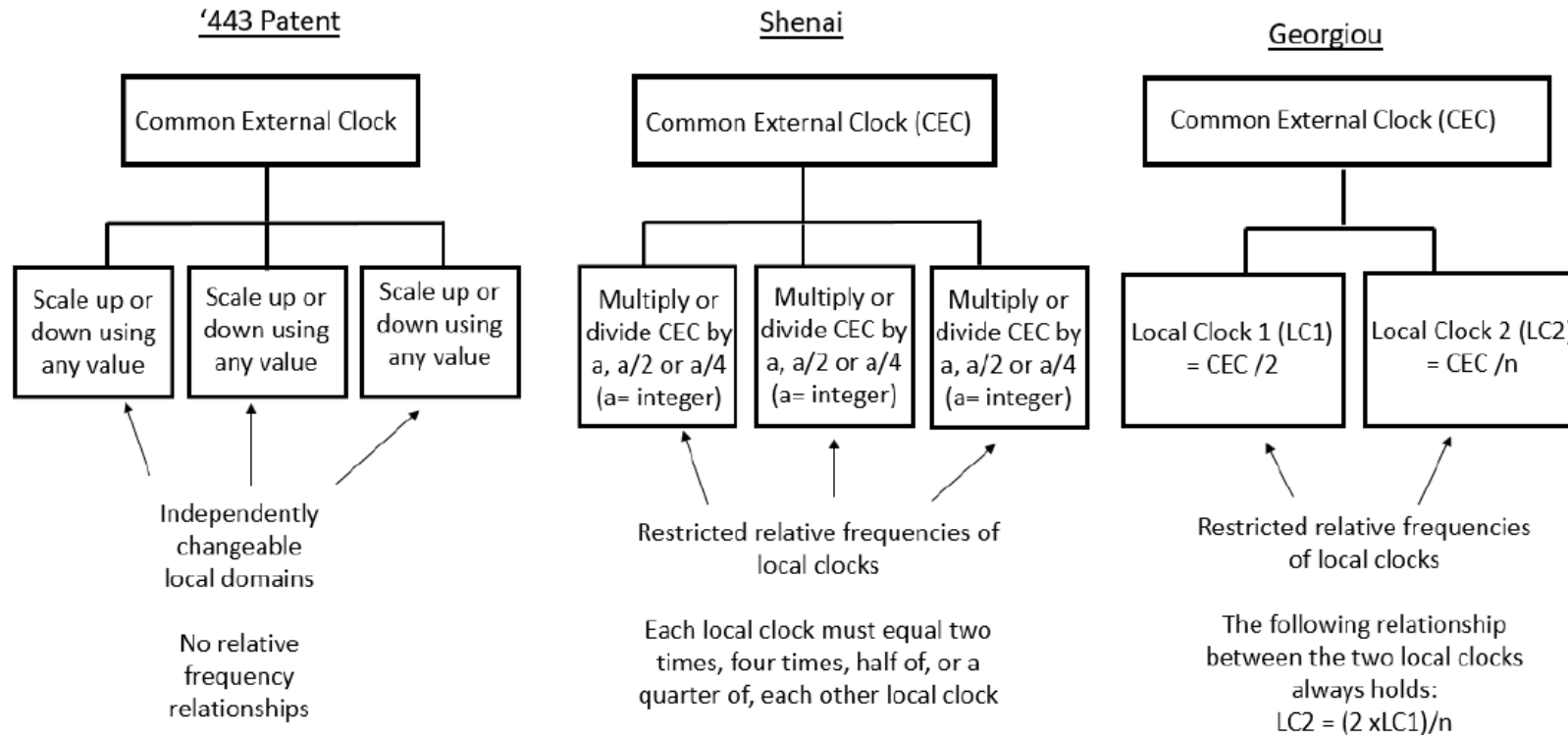
***Shenai* teaches independence of domains.**

eters for use by controller **450**. Preferably, the parameters provided by the software may still be regarding as guidelines or initial parameter settings, and the controller preferably still measures actual subsystem performance and makes dynamic determinations of actual performance versus required performance, and further adapts voltage and frequency parameters of the various subsystems.

[0028] Therefore, controller **450** may communicate with DC/DC converters and clock signal source/level shifters associated with each “load” and establish appropriate operating voltage and frequency values. Other applications, such

Paper 17, p. 22; Ex. 1004, ¶¶ 27-28 (annotated)

3. *Shenai* Teaches Independent Domain Frequencies



Roadmap

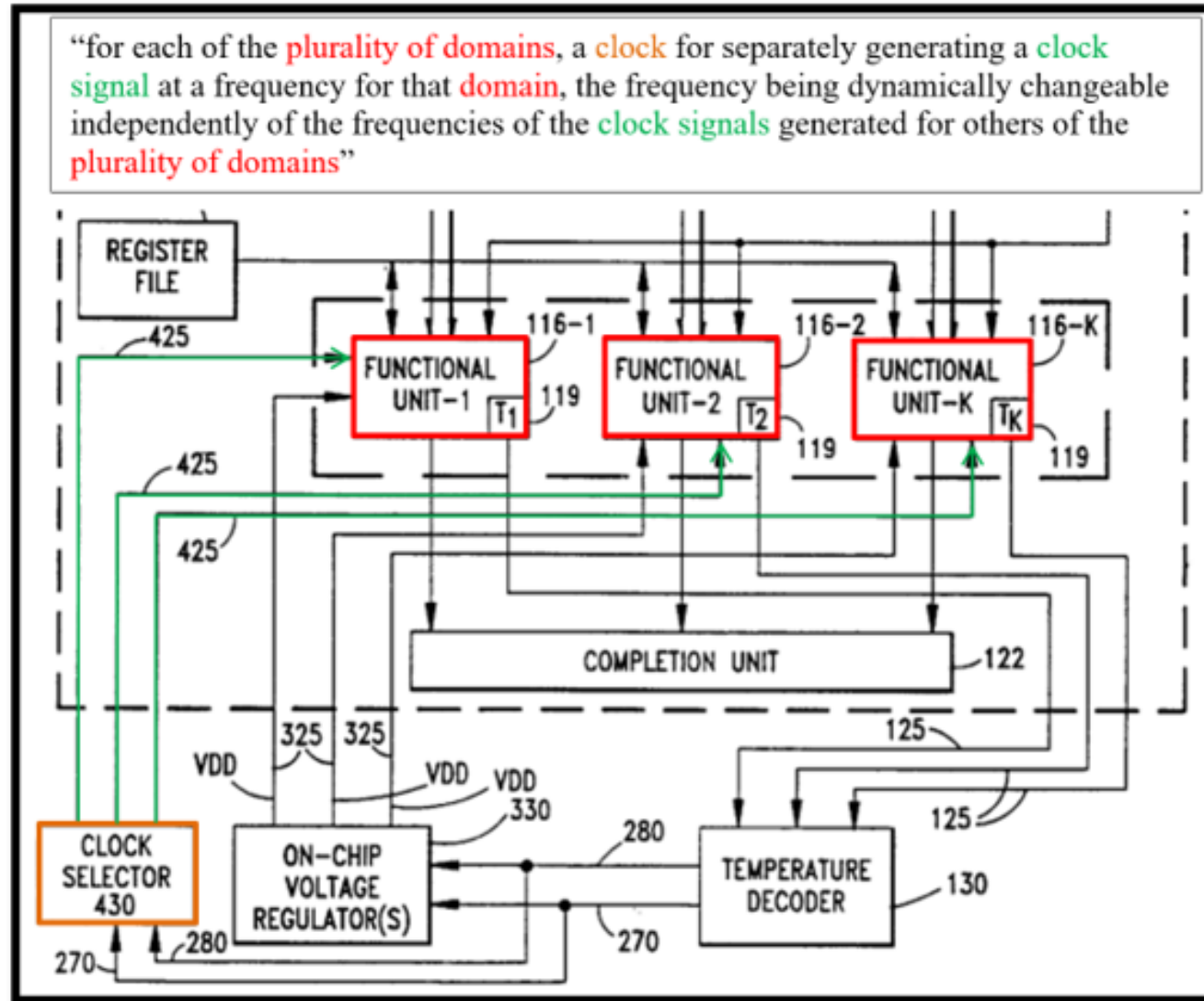
Overview

- '443 Patent
- *Shenai* Prior Art Reference
- *Georgiou* Prior Art Reference

Disputes

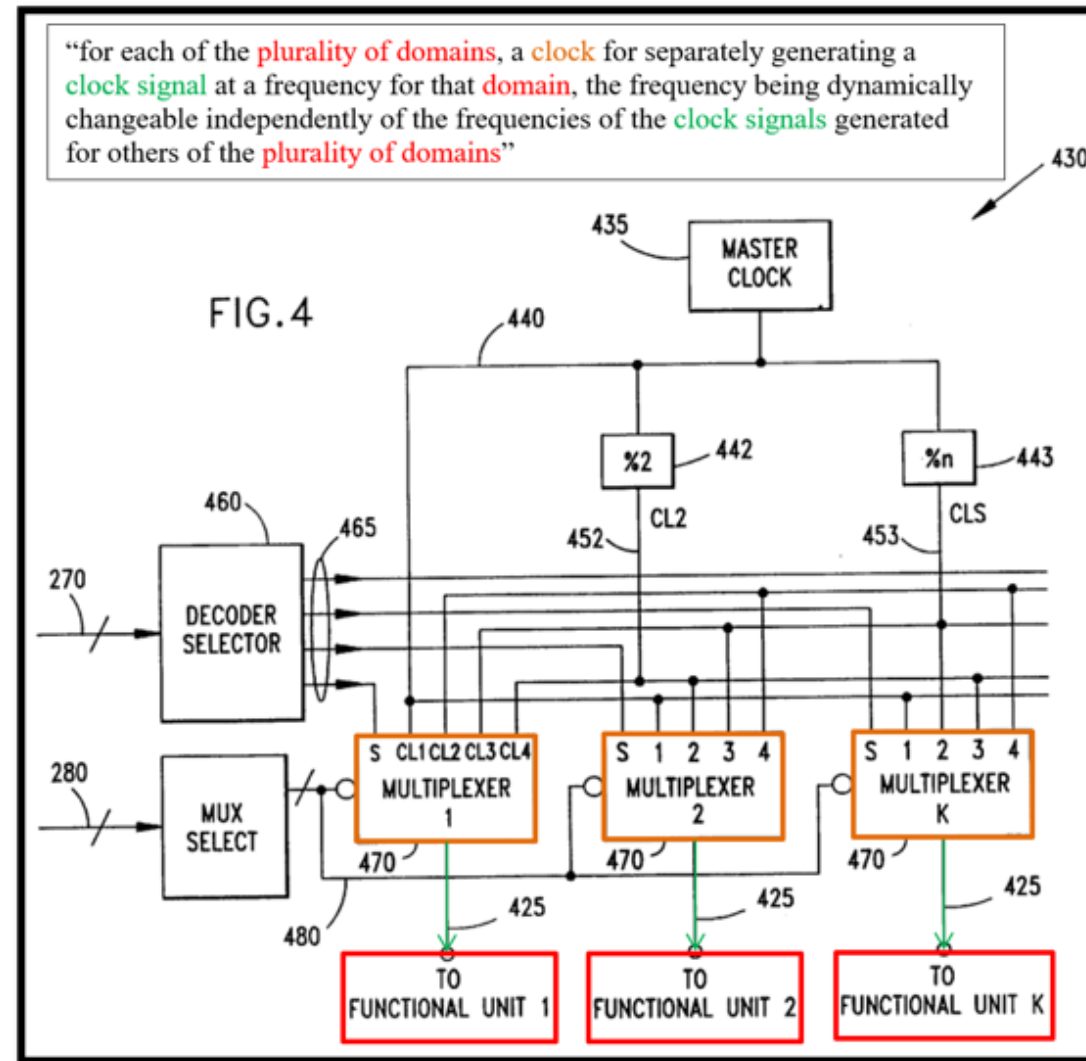
- Challenged Claims do not require construction
- *Shenai* is prior art to the '443 patent
- *Shenai* teaches domains with independently changeable frequencies
- *Georgiou* teaches domains with independently changeable frequencies

4. Georgiou Teaches Independent Domain Frequencies



Paper 2, p. 66; Ex. 1008, p. 3 (annotated)

4. Georgiou Teaches Independent Domain Frequencies



Paper 2, p. 68; Ex. 1008, p. 6 (annotated)

4. *Georgiou* Teaches Independent Domain Frequencies

***Georgiou* teaches separately generated clock signals.**

1. A multiple-clock-domain microprocessor comprising:
a plurality of domains;
for each of the plurality of domains, a clock for separately
generating a clock signal at a frequency for that
domain, the frequency being dynamically changeable
independently of the frequencies of the clock signals
generated for others of the plurality of domains; and
for each of the plurality of domains, a voltage input for
receiving a voltage which is dynamically changeable
independently of the voltages applied to said others of
the plurality of domains.

4. *Georgiou* Teaches Independent Domain Frequencies

Dr. Baker's testimony as to *Georgiou's* disclosure of "a clock for separately generating a clock signal" stands unrebutted.

198. As can be seen, current/clock control signal 270 is coupled to the "clock selector 430 to cooperatively modulate the clock frequency[.]" *Id.* at 4:37-39. As shown in annotated Figure 4 below, a respective modulated clock frequency 425 is generated by a multiplexer corresponding to a respective functional unit, and the respective modulated clock frequency 425 is then applied to each clock input of a corresponding functional unit. Thus, the "clock frequency of the functional unit is modulated[.]" *Id.* at 4:61-62. The multiplexers 470 of clock selector 430 are associated with each "independently controllable functional unit" such that "each functional unit may be operating under a different voltage 325 and frequency 425 combination according to the thermal feedback from its associated thermal sensor 119." *Id.* at 5:2-6, emphases added.

199. Additionally, as shown in annotated Figure 4 below, *Georgiou* describes a clock generator for each of the plurality of domains consisting of the dividers 442, 443, etc., decoder selector 460, and the multiplexers 470. Thus, multiplexers 470 are each a separate *clock*, capable of outputting a certain output clock frequency for a specific functional unit. As indicated, Figure 4 shows components within clock selector 430.

201. The "technology associated with each functional unit has been characterized at a series of voltage-frequency pairs which satisfy critical timing paths over expected manufacturing process and operating conditions. Each multiplexer 470 outputs the selected clock frequency which is coupled to the particular functional unit via the appropriate one of paths 425." *Id.* at 61-67, emphasis added. Therefore, not only are the clock signals provided independent to the other generated clock signals, but the clock signals are also dynamically changeable depending on the individual operating conditions of each functional unit at a given time. For these reasons, *Georgiou* teaches for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains.

Ex. 1002, ¶¶ 198-199, 201 (annotated); see also Paper 18, pp. 8-10

4. *Georgiou* Teaches Independent Domain Frequencies

There is otherwise no dispute that *Georgiou* teaches the highlighted claim language without Patent Owner's limiting construction.

1. A multiple-clock-domain microprocessor comprising:
a plurality of domains;
for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and
for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

Paper 17, pp. 8-11; Paper 14, pp. 19-22; Ex. 1001, claim 1

4. *Georgiou* Teaches Independent Domain Frequencies

***Georgiou* teaches independence of domains.**

The clock selector includes a decoder **460** which receives signal **270** associated with a particular functional unit via its thermal sensor **119** and the temperature decoder **130**. The decoder **460** decodes the signal **270** and outputs a clock select signal **465** to a select input (S) to the multiplexer associated with the particular functional unit. The clock select signal **465** is used to select the clock frequency corresponding to the voltage output by voltage regulator **330** according to signal **270**. The clock selector also includes a multiplexor selector which selects and latches signal **465** into the appropriate multiplexor **470** according to functional unit address **280**. Recall that the technology associated with each functional unit has been characterized at a series of voltage-frequency pairs which satisfy critical timing paths over expected manufacturing process and operating conditions. Each multiplexer **470** outputs the selected clock frequency which is coupled to the particular functional unit via the appropriate one of paths **425**.

Paper 2, p. 69; Ex. 1008, 8:50-67 (annotated)

In a preferred embodiment, the present invention is directed to an improved thermal feedback system and method for cooperatively varying the voltage and operating frequency of a functional unit in a multi-functional unit processor such as a superscalar microprocessor, to control heating. Those skilled in the art will appreciate however, that

Paper 2, p. 66; Ex. 1008, 1:48-53 (annotated)

