

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES), INC.,
Petitioner,

v.

UNIVERSITY OF ROCHESTER,
Patent Owner.

IPR2024-01225
Patent 7,089,443 B2

Before JAMESON LEE, THU A. DANG, and HYUN J. JUNG,
Administrative Patent Judges.

DANG, *Administrative Patent Judge.*

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. *Background*

In response to a Petition (Paper 2, “Pet.”) filed by Lenovo (United States), Inc. (“Petitioner”), we instituted *inter partes* review of claims 1 and 3–12 (the “challenged claims”) of U.S. Patent No. 7,089,443 B2 (Ex. 1001, “the ’443 patent”). See Paper 11 (“Dec. Inst.”). During trial, University of Rochester¹ (“Patent Owner”) filed a Response to the Petition (Paper 14 (“PO Resp.”)), to which Petitioner filed a Reply (Paper 17 (“Pet, Reply”)). In turn, Patent Owner filed a Sur-reply. Paper 18 (“PO Sur-Reply”). An oral hearing was held with the parties on November 17, 2025. A transcript of the hearing has been entered into the record. Paper 26 (“Tr.”)

We have jurisdiction under 35 U.S.C. § 6. This Decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the claims on which we instituted trial. Based on the record before us, Petitioner has shown by a preponderance of the evidence that claims 1 and 3–7 of the ’443 patent are unpatentable, but has not shown by a preponderance of the evidence that claims 8–12 are unpatentable.

B. *Real Parties-in-Interest*

Petitioner identifies itself as the real party-in-interest. Pet. 1. Patent Owner identifies itself and Intellectual Venture I LLC, each as the real party-in-interest. Paper 5, 2.

¹ Patent Owner states that the University of Rochester owns the patent and Intellectual Ventures I LLC is an exclusive licensee. Paper 5, 2 (Patent Owner’s mandatory notices). Patent Owner represents that Intellectual Ventures I LLC has all substantial rights to the ’443 patent. *Id.*

C. Related Proceedings

The parties identify the '443 patent as the subject of the following related district court matters: (i) *Intellectual Ventures I LLC v. Lenovo Group Ltd.*, No. 6:23-cv-00307 (W.D. Tex.); (ii) *Intellectual Ventures I LLC v. TCL Electronics Holdings Ltd.*, No. 6:23-cv-00309 (W.D. Tex.); (iii) *Intellectual Ventures I LLC v. TCL Electronics Holdings Ltd. f/k/a/ TCL Multimedia Technology Holdings, Ltd.*, No. 6:23-cv-00293 (W.D. Tex.); and (iv) *Intellectual Ventures II LLC v. Lenovo Group Limited*, No. 6:23-cv-00068 (W.D. Tex.). Pet. 1–2; Paper 5, 2; Paper 8, 1–2.

D. The '443 Patent

The '443 patent, titled “Multiple Clock Domain Microprocessor,” issued on August 8, 2006, from Application No. 10/762,550, with a filing date of January 23, 2004, and claiming the benefit of provisional Application No. 60/441,759, filed on January 23, 2003. Ex. 1001, codes (54), (45), (21), (22), (60). The '443 patent observes “that in order to continue the current pace of clock frequency increases, microprocessor designers will eventually be forced to abandon singly-clocked globally synchronous systems in favor of some form of asynchrony.” *Id.* at 1:42–45.

The '443 patent describes a multiple clock domain (MCD) microarchitecture for a microprocessor which uses a globally-asynchronous, locally-synchronous (GALS) clocking style where each functional block operates with a separately generated clock. *Id.* at code (57); *see also id.* at 4:16–19. The '443 patent reports that “by scaling frequency and voltage in different domains dynamically and independently, we can achieve an average improvement in energy-delay product of nearly 20%.” *Id.* at

5:8–11. The '443 patent further describes that “[t]he independence of each local domain clock implies no global clock skew requirement, permitting potentially higher frequencies within each domain and greater scalability in future process generations.” *Id.* at 4:29–32. “Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain allows for finer grained dynamic voltage and frequency scaling, and thus lower energy, than can be achieved with single clock, single-core-voltage systems.” *Id.* at 4:40–45.

Figure 1 of the '443 patent is a block diagram of an MCD processor, and is reproduced below. Ex. 1001, 5:32–33.

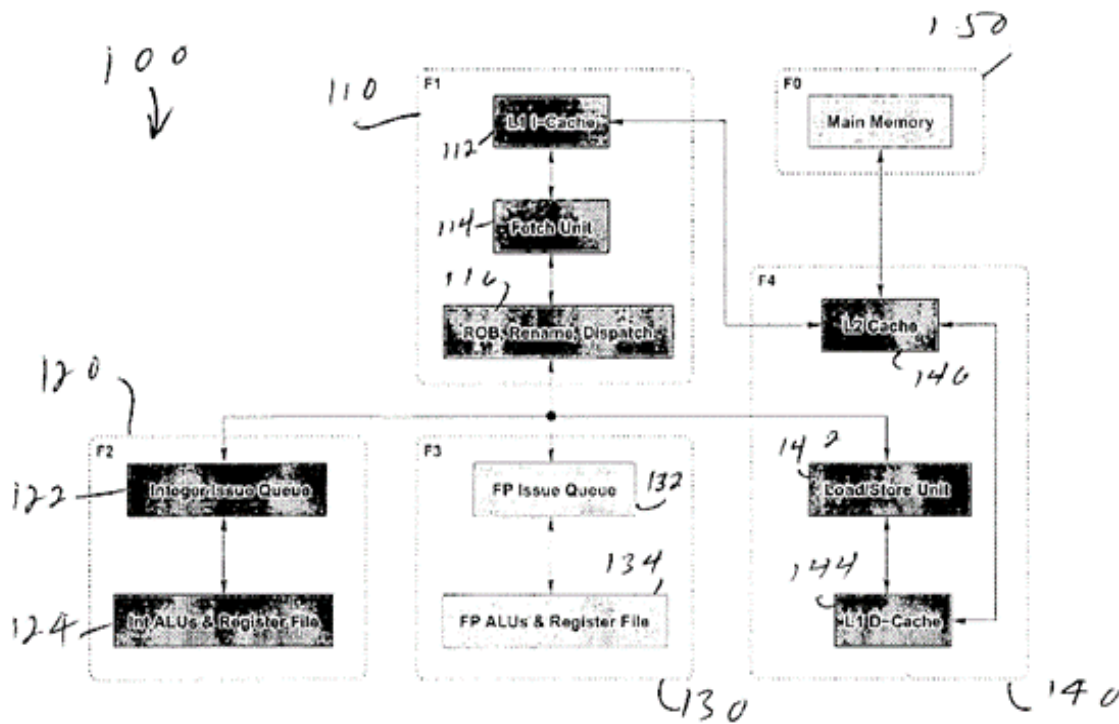


Figure 1

Figure 1 depicts architecture 100 with four domains consisting of front end 110, integer issue/execute 120, floating point issue/execute 130, and load/store issue/execute 140. *Id.* at 5:67–6:11. Front end 110 includes

instruction cache 112, fetch unit 114, and branch prediction, rename, and dispatch 116. *Id.* Integer issue/execute 120 includes integer issue queue 122 and integer arithmetic logic units and register file 124. *Id.* Floating point issue/execute 130 includes a floating point issue queue 132 and floating point arithmetic logic units and register file 134. *Id.* Load/store issue/execute 140 includes load/store unit 142, L1 D-cache 144, and L2 cache 146, where L2 cache 146 is in communication with main memory interface 150 as well as with cache 112 of front end 110. *Id.*

Although the '443 patent “recognizes the overhead associated with independent clocks with no known phase relationship” in an MCD processor, the '443 patent provides a “general queue structure that we use for inter-domain communication” that “minimizes the need for inter-domain synchronization.” Ex. 1001, 6:39–41, 6:54–55, 5:2–4. In particular, the '443 patent’s selection of certain “queues as interdomain synchronization points has the advantage of hiding the synchronization cost whenever the queue is neither full nor empty.” *Id.* at 6:50–53.

E. Challenged Claims

Of the challenged claims (1 and 3–12), claims 1 and 8 are independent. Claims 3–7 depend from claim 1, and claims 9–12 depend from claim 8. Claims 1 and 8 are reproduced below:

1. A multiple clock domain microprocessor comprising:

a plurality of domains;

for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and

for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

Ex. 1001, 17:9–19.²

8. A method of operating a microprocessor, the method comprising:

- (a) providing a plurality of domains in the microprocessor;
- (b) clocking each of the domains separately at a clock frequency;
- (c) applying a voltage to each of the domains separately;
- (d) operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another, and
- (e) dynamically controlling the clock frequency and the voltage in each of the plurality of domains independently of the clock frequencies and the voltages in others of the plurality of domains.

Ex. 1001, 18:5–18.

F. Evidence

Petitioner relies on the references listed below.

Reference		Date	Exhibit No.
Shenai	US 2003/0030326 A1	Feb. 13, 2003	1004
Halepete	WO 01/53921 A1	July 26, 2001	1005
Sherburne	US 2002/0169990 A1	Nov. 14, 2002	1006

² The text set forth above reflects corrections made by way of a certificate of correction of June 14, 2011.

Reference		Date	Exhibit No.
Traylor	US 5,473,756	Dec. 5, 1995	1007
Georgiou	US 6,047,248	Apr. 4, 2000	1008
Kranich	WO 01/33352 A1	May 10, 2001	1009

Petitioner relies on the Declarations of R. Jacob Baker, Ph.D. in support of its unpatentability contentions. Exs. 1002, 1032. Patent Owner relies on the Declarations of David Kaeli, Ph.D. Exs. 2001, 2013. Dr. Kaeli was cross-examined by Petitioner, and a transcript of his deposition was entered into the record. Ex. 1033.

G. The Asserted Grounds of Unpatentability

Petitioner contends that the challenged claims are unpatentable under the following grounds. Pet. 3–4.

Claim(s) Challenged	35 U.S.C. § ³	Reference(s)/Basis
1, 3, 8, 12	103(a)	Georgiou
4, 9	103(a)	Georgiou, Halepete
5, 10	103(a)	Georgiou, Kranich
1, 3–5, 8, 9, 12	103(a)	Shenai
4, 9	103(a)	Shenai, Halepete
5–7, 10, 11	103(a)	Shenai, Sherburne
7	103(a)	Shenai, Sherburne, Traylor

³ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. Because the ’443 patent was filed before March 16, 2013, the effective date of the relevant amendment, the pre-AIA version of § 103 applies.

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claims are construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). This standard includes “construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b).

“In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). Extrinsic evidence is “less significant than the intrinsic record in determining ‘the legally operative meaning of claim language.’” *Phillips*, 415 F.3d at 1317 (citations omitted).

“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Petitioner asserts “that no construction of the claims is necessary to assess whether the prior art reads on the Challenged Claims.” Pet. 20–21. Patent Owner contends that “a determination that a claim term ‘needs no construction’ or has the ‘plain and ordinary meaning’ may be inadequate when a term has more than one ‘ordinary’ meaning or when reliance on a

term's 'ordinary' meaning does not resolve the parties' dispute.'" PO Resp. 19 (citing *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008)). Patent Owner then argues that "[w]hen a patentee describes the features of the 'present invention,' it is well-settled that 'this description limits the scope of the invention.'" *Id.* at 20 (quoting *Pacing Techs., LLC v. Garmin Int'l, Inc.*, 778 F.3d 1021 (Fed. Cir. 2015)).

According to Patent Owner:

the claim language reciting "for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains," requires that the separate clocks in the plurality of domains be globally-asynchronous.

PO Resp. 20.

Patent Owner points out that the "'Summary of the Invention' of the '443 Patent states that the 'present invention' uses a globally-asynchronous clocking style," and thus, contends that a POSITA reading the entirety of the '443 patent "would have understood that the '[] present invention' was directed to globally-asynchronous clocks." PO Resp. 21. Thus, Patent Owner contends that a POSITA would have equated the plain and ordinary meaning of the claim language "to 'require that each domain generate its clock signal independently, and that the frequency of each domain's clock be dynamically changeable without being constrained by the frequencies of other domains.'" PO Resp. 21–22. Further, according to Patent Owner, it would have been readily apparent to a POSITA reading the entirety of the '443 patent that "the specification criticized prior synchronization systems . . . that restricted the freedom to select clock frequencies by requiring a rational relationship between clock domains," and thus, the POSITA would

have understood that the plain and ordinary meaning of such claim language did not cover such prior art techniques. *Id.* at 23–25 (citing *Indivior Inc. v. Dr. Reddy’s Labs*, 752 Fed. Appx. 1024 (Fed. Cir. 2018); *SciMed Life Sys. v. Advanced Cardiovascular Sys.*, 242 F.3d 1337 (Fed. Cir. 2001); *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1159 (Fed. Cir. 1998); *Ekchian v. Home Depot, Inc.*, 104 F.3d 1299, 1304 (Fed. Cir. 1997)).

In its Reply, Petitioner argues that “[n]either the actual claim language nor the specification supports Patent Owner’s claim construction.” Pet. Reply 8–9 (citing *Phillips*, 451 F.3d at 1306; *Leibel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 904 (Fed. Cir. 2004)). In particular, Petitioner contends that “the claim language does not support the requirement that ‘each domain must be free to generate and change its clock frequency without being tethered to small integer multiples of the other domains.’” *Id.* at 9 (citing PO Resp. 22). Petitioner points out that “language excluding domains ‘being tethered to small integer multiples of the other domains’ is nowhere to be found in the claims of the ’443 patent,” whereas “[t]he specification does not include any discussion of ‘integer multiples’ of frequencies in any context, much less restricting domains [as asserted].” *Id.* at 9–10.

In light of the parties’ arguments and evidence, we find that it is necessary to construe the terms “a clock for separately generating a clock signal at a frequency for that domain,” wherein the frequency is “dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains” recited in claim 1, but only to the extent necessary to resolve the controversy. *See Realtime Data*, 912 F.3d at 1375. As for the other claim limitations, for the reasons

set forth below, the explicit requirements set forth in claims themselves sufficiently limit the claims without requiring further construction.

As the parties agree, claim 1 recites that each clock of the plurality of domains separately generate a clock signal at a frequency that is dynamically “changeable independently of the frequencies of the clock signals generated for others” of the domains. Ex. 1001, 17:11–20. We find unavailing Patent Owner’s arguments that the separate clocks being “changeable independently” of the other domains “requires that the separate clocks in the plurality of domains be globally-asynchronous.” PO Resp. 20.

We begin with the language of the claims. *See Phillips*, 415 F.3d at 1314. Although claim 1 recites that the separate clocks are changed independently of each other, it does not recite any requirement that they be globally-asynchronous to one another. *See* Ex. 1001, 17:11–20. That is, although Patent Owner argues during the oral hearing that the prior art discloses a “known synchronization point,” and thus, cannot be “asynchronous” (Tr. 46:17–25), such argument does not focus on the language in claim 1. *See* Ex. 1001, 17:11–20. As Petitioner points out during the oral hearing, claim 1 “simply says that the frequencies have to be changeable independently,” and “do[es] not use any specific language excluding rational factor or integer multiplication.” *Id.* at 18:14–16.

Furthermore, we note that independent claim 8 separately recites “operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another,” *in addition* to reciting “dynamically controlling the clock frequency and the voltage in each of the plurality of domains independently of the clock frequencies and the voltages in others of the plurality of domains.” *See* Ex. 1001, 18:12–18. That is, claim 8 recites dynamically

controlling the separate clock frequencies independently of the of the others ***as a separate limitation*** from the limitation of “asynchronously” operating the plurality of domains. *Id.* Thus, by separately claiming the limitations in claim 8, the Applicant in the prosecution of the ’443 patent acknowledges that “independently” controlling the clock frequencies in the plurality of domains is different from “asynchronously” operating the plurality of domains.

We turn next to the Specification of the ’443 patent. “The specification is the ‘single best guide to the meaning of a disputed term,’ . . . and ‘is, thus, the primary basis for construing the claims.’” *Trs. of Columbia Univ. in City of New York v. Symantec Corp.*, 811 F.3d 1359, 1362 (Fed. Cir. 2016) (citations omitted). Although Patent Owner contends that the Specification disparages systems that impose significant restrictions on the possible choices of frequencies (PO Resp. 21), we find availing Petitioner’s contention that “[s]upport for Patent Owner’s construction is absent from the specification.” Pet. Reply 10. As Petitioner points out, Patent Owner’s claim construction “appears to be based on a single paragraph of the ’443 patent referring to preexisting ‘synchronization schemes [that] restrict the phase relationship and relative frequencies of the clocks.” *Id.* That is, the only reference by Patent Owner to the Specification is that the Specification states that “Some synchronization schemes restrict the . . . relative frequencies of the clocks, thereby eliminating the need for hardware arbitration [27]. Unfortunately, these schemes impose significant restrictions on the possible choices of frequencies.” PO Resp. 26 (citing Ex. 1001, 6:32–36). We agree with Petitioner that such disclosure in the Specification “does not describe how these synchronization schemes ‘restrict the phase relationship and relative frequencies’ with any specificity.” Pet.

Reply 10 (citing Ex. 1032 ¶ 8). That is, we agree that a mere statement in the Specification that some schemes impose restrictions on the possible choices of frequency is not a disparagement of any system that has limited choices of frequency or would preclude the claims from covering such prior art techniques.

Instead, as Petitioner points out, the Specification of the '443 patent states “[t]he **preferred embodiment** uses **four domains** [...] so that domains may vary somewhat in size and still be **covered by a single clock**.” *Id.* (citing Ex. 1001, 5:57–59). As Dr. Baker testified in support of Petitioner’s contention, “the preferred embodiment of the '443 patent relies on a **single external master clock** that distributes a signal to the local PLL of each domain.” *See* Ex. 1032 ¶ 9. Thus, although Patent Owner contends that clock signals generated based on a master clock cannot be interpreted to be generated independently of the clock signals generated for others of the plurality of domains (PO Resp. 49), we agree with Petitioner that such claim construction would “exclude[] the preferred embodiment of the '443 patent,” which is disfavored. Pet. Reply 11.

For the reasons discussed above, we conclude that “changeable independently” of the other domains does not require that the separate clocks in the plurality of domains be globally-asynchronous.

B. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, “would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406

(2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

C. Level of Skill in the Art

The level of skill in the art is a factual determination that provides a primary guarantee of objectivity in an obviousness analysis. *See Al-Site Corp. v. VSI Int’l Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999) (citing *Graham*, 383 U.S. at 17–18 (1966); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991)). Generally, it is easier to establish obviousness under a higher level of ordinary skill in the art. *See Innovention Toys, LLC v. MGA Entm’t, Inc.*, 637 F.3d 1314, 1323 (Fed. Cir. 2011) (“A less sophisticated level of skill generally favors a determination of nonobviousness . . . while a higher level of skill favors the reverse.”).

Petitioner, relying on the testimony of Dr. Baker, contends that a person of ordinary skill in the art (POSITA) “would have had a bachelor’s degree in electrical engineering, computer engineering, or the equivalent, and 2–3 years of experience designing computing circuits and systems,” wherein “[m]ore practical experience could offset the aforementioned education and vice-versa.” Pet. 4 (citing Ex. 1002 ¶¶ 29–31). Patent Owner does not contest Petitioner’s proposal or offer an alternative. *See generally* PO Resp. On this record, we are persuaded that Petitioner’s proposal is consistent with the technology described in the Specification and the cited prior art.

D. Claims 1, 3, 8, and 12 as allegedly obvious over Georgiou; Claims 4 and 9 as obvious over Georgiou and Halepete; and Claims 5 and 10 as obvious over Georgiou and Kranich

Petitioner contends that Georgiou renders obvious claims 1, 3, 8, and 12 of the '443 patent. Pet. 61–76. Petitioner also contends that Georgiou, in further view of Halepete, renders obvious claims 4 and 9 of the '443 patent. *Id.* at 76–78. Petitioner further contends that Georgiou, in further view of Kranich, renders obvious claims 5 and 10 of the '443 patent. *Id.* at 78–81.

In response, Patent Owner contends that Georgiou fails to disclose or render obvious the claimed independent and dynamically changeable clock frequencies, and that Halepete and Kranich fail to cure the shortcomings of Georgiou. *See* PO Resp. 49–64.

We briefly summarize Georgiou, Halepete and Kranich below.

1. Georgiou (Ex. 1008)

Georgiou, titled “Performance-Temperature Optimization by Cooperatively Varying the Voltage and Frequency of a Circuit,” discloses a “[a] system and method using thermal feedback to cooperatively vary a voltage and frequency of a circuit to control heating while maintaining synchronization.” Ex. 1008, codes (54), (57). More specifically, Georgiou’s disclosure applies, in a preferred embodiment, to “a multi-functional unit processor such as a superscalar microprocessor,” and describes “[u]sing thermal sensors for feedback, the voltage swing and operating frequency of the circuit [being] cooperatively varied (also called voltage-frequency pairs) to reduce the power dissipation without compromising reliability or system synchronization.” *Id.* at 2:21–26, 3:48–52.

Figure 1, reproduced below, illustrates a block diagram of a superscalar processing system.

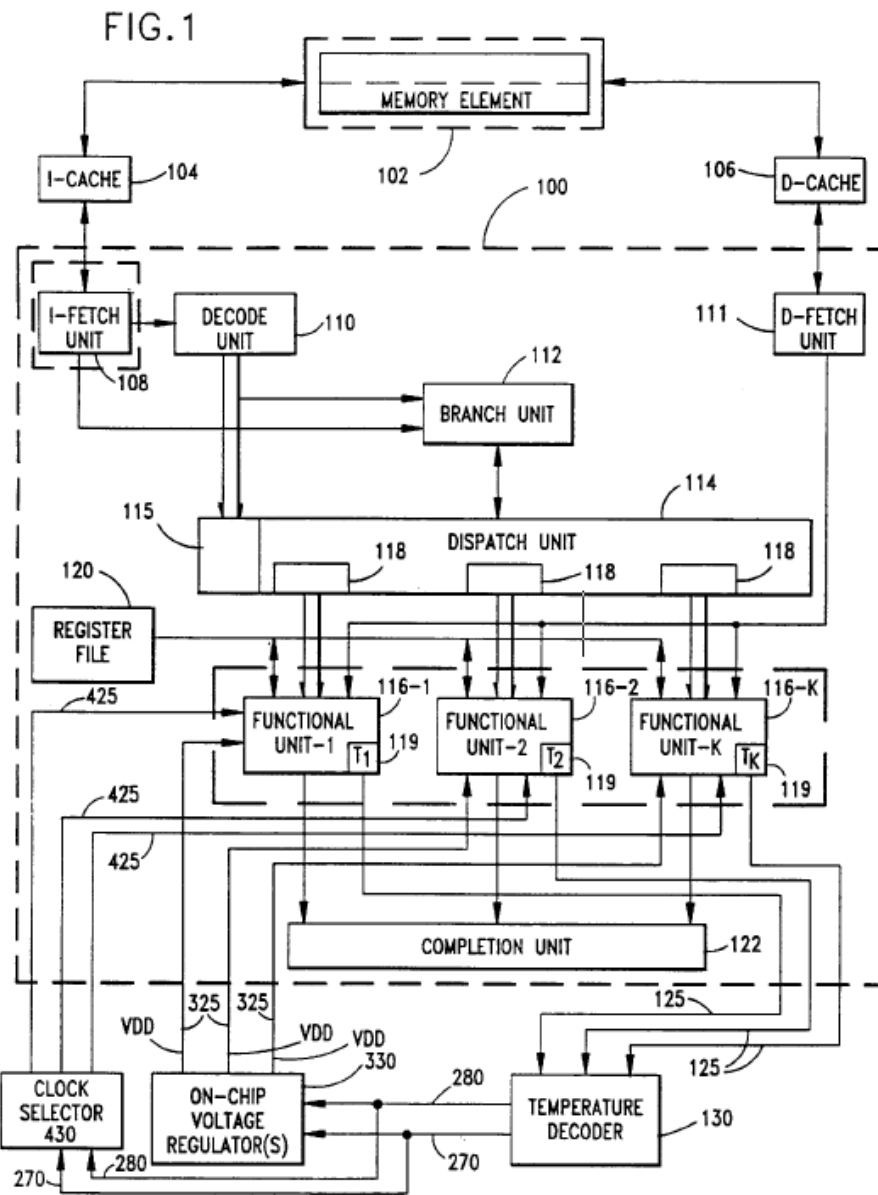
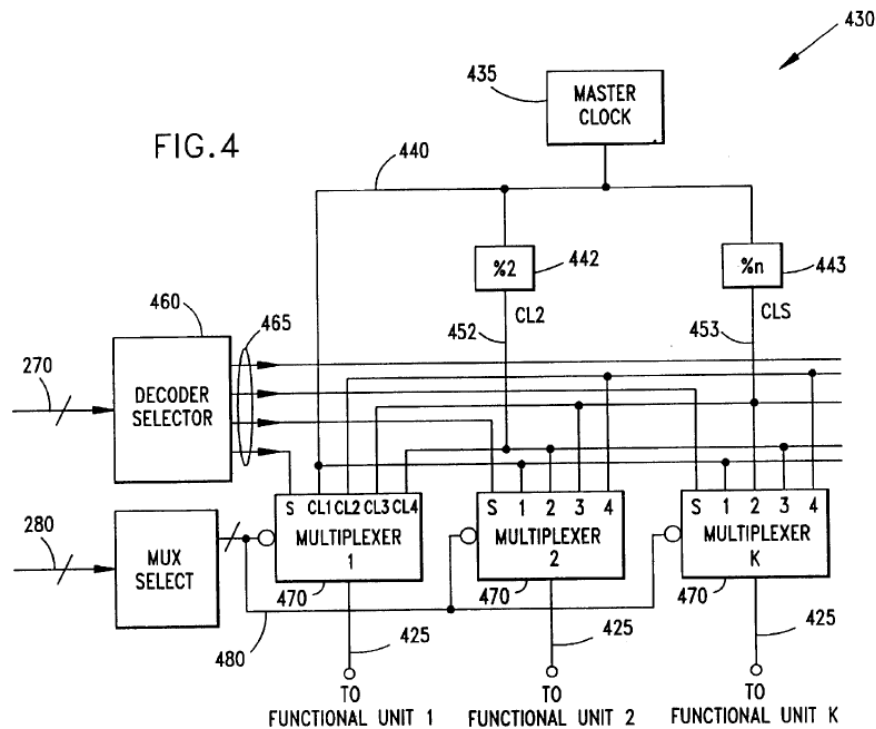


Figure 1 shows processor unit 100, which includes components for fetching instructions from memory and “analyz[ing] dependencies among pending instructions, and schedul[ing] execution of instructions, one on each of functional units 116-1 through 116-K.” Ex. 1008, 5:16–38. Georgiou provides that “[e]xamples of well known functional units are: fixed-point units, floating point units, load/store units, and branch units found in typical general purpose and superscalar microprocessors.” *Id.* at 3:58–61. In the

Figure 1 embodiment, “each functional unit 116-1 . . . 116-K may include an on-chip thermal sensor 119 mechanism,” the output of which is periodically sampled by temperature decoder 130. *Id.* at 6:43–53. “The decoder 130 decodes and compares the thermal sensor output with a predetermined threshold to provide current/clock control signals 270 respectively to an adjustable on-chip voltage regulator 330 (described in FIG. 3) and to a clock selector 430 (described in FIG. 4).” *Id.* at 6:54–59. “[S]ignals 270 operate to control the current sources to voltage regulator 330 to adjust the regulator output voltage 325,” as well as “to select a predetermined corresponding clock frequency via clock selector 430.” *Id.* at 6:59–63. This resulting voltage-frequency pair maintains critical timing paths within design specifications and is provided to the functional units via paths 325 and 425. *Id.* at 6:63–66.

Clock selector 430 is shown in detail in Figure 4, reproduced below.



As shown in Figure 4, “master clock 435 running at a master clock frequency 440 [] is used as the common source and provides a common clock reference for a number of clock dividers whose output is some predetermined fraction of the master clock frequency 440.” Ex. 1008, 8:37–42. For example, “clock divider 442 may be a divide-by-two clock divider whose output frequency 452 is one-half that of the master clock frequency 440, and clock divider 443 may be a divide-by-n clock divider whose output frequency 453 is one-nth that of the master clock frequency 440.” *Id.* at 8:43–47.

2. Halepete (Ex. 1005)

Halepete, titled “Adaptive Power Control,” relates to “controlling the power used by a computer” by “determining when the operating characteristics of the central processor are significantly different than required by the operations being conducted” and “changing the operating characteristics of the central processor,” such as by increasing or decreasing the frequency and voltage. Ex. 1005, codes (54), (57). In particular, Halepete describes a computer system with processor 10, wherein processing unit 16 includes master control unit 18 “for monitoring the operating characteristics of the processor” and “accomplishing clock and voltage control.” *Id.* at 5:5–17, Fig. 1.

3. Kranich (Ex. 1009)

Kranich, titled “Fast Multithreading for Closely Coupled Multiprocessors,” relates to “[a] processor architecture containing multiple closely coupled processors” interconnected via thread control device 300, which includes first-in-first-out buffers 310A-310B and synchronization logic 314. Ex. 1009, codes (54), (57), 10:6–11, Fig. 3A.

4. Independent claim 1 as allegedly obvious over Georgiou

Having reviewed Petitioner's and Patent Owner's contentions and supporting evidence in the complete record, we determine Petitioner has demonstrated by a preponderance of the evidence that claim 1 would have been obvious over Georgiou. As an initial matter, we address in detail Petitioner's contentions and Patent Owner's arguments with respect to the limitations of independent claim 1.

a) *Preamble, "A multiple clock domain microprocessor comprising"*

Petitioner contends that Georgiou teaches a system with multiple functional units, such as in a superscalar microprocessor, where the functional units may be independently controllable such that each unit operates with a different voltage and frequency combination. Pet. 62 (citing Ex. 1002 ¶¶ 192–194; Ex. 1008, 3:49–63, 5:2–6, 8:37–67). In particular, Petitioner contends that "a POSITA would have recognized that *Georgiou's* functional units correspond to the claimed 'domains,'" and, in the alternative, that "a POSITA would have known that applying *Georgiou's* functional units as the claimed 'domains' would have been a simple substitution of one known element (*Georgiou's* functional units) for another (domains) to obtain predictable results." *Id.* at 63 (citing Ex. 1002 ¶¶ 192–194; *KSR*, 550 U.S. at 415–421).

Patent Owner does not present arguments addressing the specific merits of Petitioner's contentions with respect to the preamble. *See generally* PO Resp. 49–64.

Based on the complete record presented, we determine that Petitioner has persuasively shown that Georgiou teaches a “multiple clock domain microprocessor,” as recited in claim 1.⁴

b) *“a plurality of domains”*

Petitioner contends that Georgiou teaches the claimed “plurality of domains” for the reasons detailed above regarding the language of the preamble. Pet. 64 (citing Ex. 1002 ¶¶ 195–196). Specifically, Petitioner asserts that Georgiou’s functional units 116-1 through 116-K teach the claimed domains. *Id.*

Patent Owner does not present arguments addressing the specific merits of Petitioner’s contentions with respect to this claim limitation. *See generally* PO Resp. 49–64.

Based on the complete record presented, we determine that Petitioner has persuasively shown that Georgiou teaches “a plurality of domains,” as recited in claim 1.

c) *“for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains”*

Petitioner contends that Georgiou discloses clock frequencies 425 applied to the clock inputs of respective functional units. Pet. 67 (citing Ex. 1002 ¶¶ 197–198; Ex. 1008, 4:61–62). Specifically, Petitioner asserts that within Georgiou’s clock selector 430 are multiplexers 470, each of

⁴ Because Petitioner has shown that the recitation in the preamble is satisfied by Georgiou, there is no need to determine whether the preamble is limiting. *See Realtime Data*, 912 F.3d at 1375.

which “corresponds to the claimed ‘clock’ for separately generating a clock signal at a frequency for a corresponding functional unit.” *Id.* at 68 (citing Ex. 1002 ¶¶ 193, 197–201). Petitioner provides annotated versions of Figures 1 and 4 of Georgiou, reproduced below, to supports its contentions:

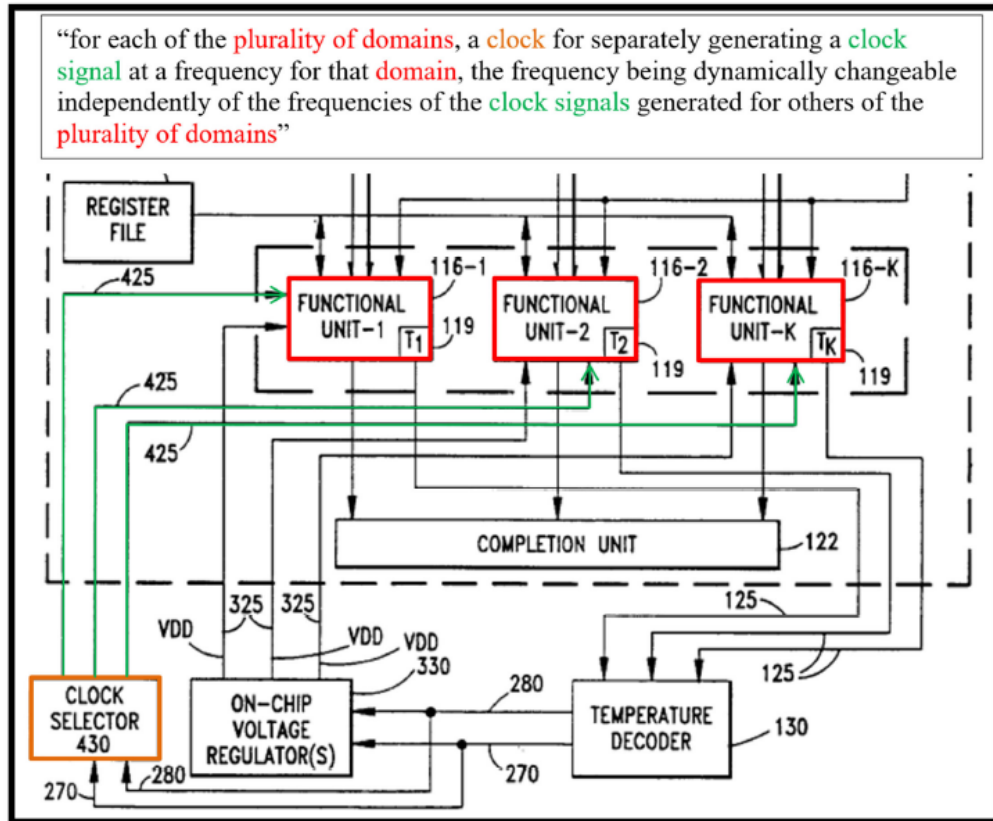


Figure 1 of Georgiou (Excerpted)

The above annotated Figure 1 of Georgiou in the Petition shows a data processing system comprising functional units 116 (red), and clock selector 430 (orange) providing clock signal 425 (green) to a respective one of functional units 116. Pet. 66.

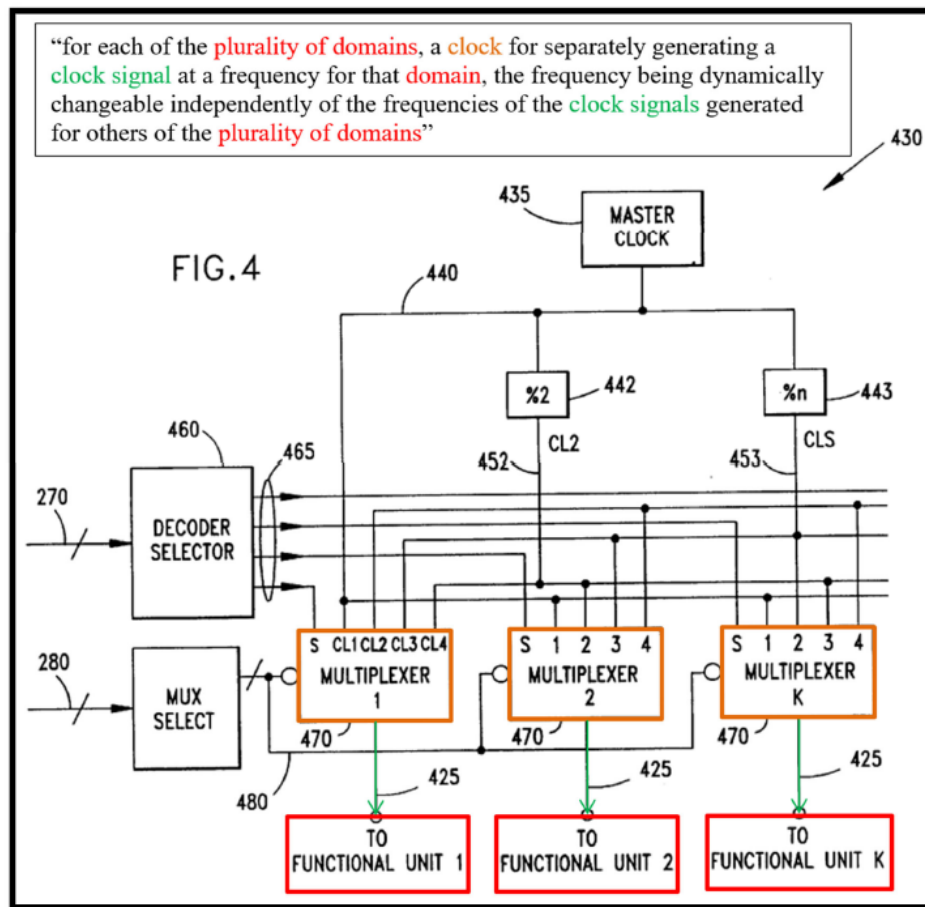


Figure 4 of Georgiou

The above annotated Figure 4 of Georgiou in the Petition shows data clock selector 430 in further detail. Pet. 68. As shown in annotated Figure 4, data clock selector 430 comprises multiplexers 470 (orange) providing clock signal 425 (green) to a respective one of functional units (red). *Id.*

Petitioner asserts that, as shown in annotated Figure 4 of Georgiou, clock selector 430 also includes “master clock 435 running at master clock frequency 440,” wherein “clock dividers can manipulate the master clock frequency by an integer value, such as divide-by-2 or divide-by-n.” *Id.* at 69 (citing Ex. 1002 ¶¶ 199–201; Ex. 1008, 8:37–48). Accordingly, according to Petitioner, “[e]ach multiplexor 470 provides a clock signal to its respective

functional unit independent of the other clock signals, and the clock signals are dynamically changed depending on the individual needs of each functional unit at a given time.” *Id.* (citing Ex. 1002 ¶¶ 197–201).

Patent Owner responds that Georgiou’s “Rational Factor” relationship fails to disclose or render obvious the claimed independent and dynamically changeable clock frequencies. PO Resp. 49. In particular, Patent Owner argues that Georgiou discloses a clocking architecture in which “all domain clocks are derived from a shared master clock through predetermined rational dividers, inherently imposing interdependent relationships that enable synchronized operation through predictable phase alignment. *Id.* This, according to Patent Owner, “necessarily imposes a small integer relationship among the domain clocks—precisely the ‘rational factor’ (M/N) criticized in the ’443 specification.” *Id.* Thus, Patent Owner contends that Georgiou “expressly discloses a clocking architecture in which all domain frequencies are predetermined fractions of the same global source.” *Id.* at 54.

We find unavailing Patent Owner’s arguments, which turn on the contention that Georgiou does not disclose the claimed invention because Georgiou’s clock signals are generated as integer or fractional multiples or divisions of a master clock. PO. Resp. 49. That is, Patent Owner is relying on its proposed claim construction of “dynamically changeable independently of the frequencies . . . generated for others of the plurality of domains” as excluding integer or factional multiples or divisions of a master clock, with which, as discussed above in Section II(A), we do not agree. We find unavailing Patent Owner’s argument that clock signals generated based on a master clock are not generated independently of the clock signals generated *for others of the plurality of domains*. Although Georgiou’s clock

signals are dependent on master clock, Patent Owner fails to show Georgiou's clock signals are also dependent on the clock signals of the other functional units (domains). *See* Ex. 1008, Fig. 4.

As Petitioner explained during the oral hearing, in Georgiou, “domain B could be changed as many times as needed based on the multiples, without touching . . . domain A,” and thus “domain A could remain at a static frequency while the frequency for domain B could be moving all around, multiples or not.” Tr. 24:8–12. In other words, “to the extent that they’re related at birth, . . . They have to start at some value, but otherwise, they are independently controlled.” *Id.* at 24:19–22. That is, although Georgiou’s clock frequencies in the plurality of domains are changeable to a fraction of the same master clock, which fraction a particular domain clock obtains does not depend on the fraction of the master clock frequency in the other domains. *See* Ex. 1008, Fig. 4.

As Petitioner points out, in Georgiou’s Figure 4, “[e]ach multiplexer 470 outputs the selected clock frequency which is coupled to the **particular functional unit** via the appropriate one of paths 425.” Pet. 69 (citing Ex. 1008, 8:61–67). We find persuasive Dr. Baker’s testimony relied upon by Petitioner, wherein Dr. Baker testified that, “[t]herefore, not only are the clock signals provided independent to the other generated clock signals,” but “the clock signals are also dynamically changeable depending on the individual operating conditions of each functional unit at a given time.” Ex. 1002 ¶¶ 197–201; *see also* Pet. 69. Although Dr. Baker acknowledged that Georgiou discloses a clock selector with a master clock running at a master clock frequency, Dr. Baker pointed out that is similar to the ’443 Patent. Ex. 1002 ¶ 200 (citing Ex. 1008, 8:37–41; Ex. 1001, 5:7–9 (“The

preferred embodiment uses four domains, . . . so that domains may vary somewhat in size and still be covered by a single clock.”)).

We do not find availing Patent Owner’s contention during the oral hearing that Georgiou’s multiplexer “can only select from known values,” and have a “known synchronization point,” wherein “[i]t’s not going to be able to take any arbitrary value.” Tr. 39: 7–22. Instead, we agree with Petitioner’s position that nothing in the claims or Specification excludes configurations in Georgiou in which the “individual domain clocks . . . , whether they are changeable based on integer multiples or integer division,” because “they’re still independent” of the other domain clocks. Tr. 18:24–20:7. That is, in the prior art, “what happens in the neighboring domain is not mentioned and wouldn’t need to be mentioned because each one essentially operates independently,” wherein each clock is derived “from the common external clock, and that common external clock is adjusted according to the particular needs of the domain.” *Id.* at 19:16–21.

Based on the complete record presented, we determine that Petitioner has persuasively shown that Georgiou teaches “for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” as recited in claim 1.

d) *“for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains”*

Petitioner contends that supply voltage 325 output from on-chip voltage regulator(s) 330 “provides separate voltages to the inputs of functional unit 116-1, 116-2, . . . 116-K.” Pet. 70–71 (citing Ex. 1002 ¶ 202;

Ex. 1008, 4:38–41). Petitioner asserts that to the extent “*Georgiou’s* voltage supply is found not to correspond to a ‘voltage input,’ it was known in the art for microprocessors to use input pins to receive a voltage.” *Id.* at 71–72 (citing Ex. 1002 ¶¶ 203–204; Ex. 1011, 6; Ex. 1013, 138, 175).

Petitioner further asserts that “[c]urrent/clock signal 270, as seen in Figure 1, is coupled to ‘adjustable on-chip voltage regulators 330 to reduce the supply voltage 325,’” such that “‘the **modulated voltage** and frequency **are applied to the functional unit to dynamically control heating** while maintaining synchronization and reliability.’” Pet. 72 (citing Ex. 1002 ¶¶ 202–204; Ex. 1008, 4:35–36, 10:48–51). Petitioner contends that “[e]ach functional unit is provided a separate voltage that changes depending on the thermal feedback received from that functional unit,” and that “the voltages supplied are independent from one another, and are dynamically changeable (e.g., based on thermal feedback of each functional unit).” *Id.* (citing Ex. 1002 ¶¶ 202–204; Ex. 1008, 5:5–7).

Patent Owner does not present arguments addressing the specific merits of Petitioner’s contentions with respect to these claim limitations. *See generally* PO Resp. 49–64.

Based on the complete record presented, we determine that Petitioner has persuasively shown that *Georgiou* teaches “for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains,” as recited in claim 1.

f) Claim 1 conclusion

Based on the complete record presented, we determine that Petitioner has persuasively shown that claim 1 would have been obvious over *Georgiou*.

5. Independent claim 8 as allegedly obvious over Georgiou

Similar to claim 1, claim 8 recites, *inter alia*, “dynamically controlling the clock frequency and the voltage in each of the plurality of domains independently of the clock frequencies and the voltages in others of the plurality of domains.” Ex. 1001, 18:15–18. Furthermore, claim 8 recites “operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another.” *Id.* at 18:12–14.

Petitioner repeats its contention with respect to claim 1 (Pet. 73–75), and adds that the limitation “operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another” would have been obvious to a POSITA “since the microprocessor described by Georgiou operates its functional units using a plurality of respective independent frequencies at the same time.” *Id.* at 74 (citing Ex. 1002 ¶¶ 211–219). According to Petitioner, a POSITA would have recognized that “the functional units of Georgiou operate asynchronously since they have different clocks.” *Id.* (citing Ex. 1002 ¶¶ 53–56, 211–219). Petitioner contends that a POSITA would have known “to apply known techniques for inter-unit synchronization (e.g., an asynchronous protocol, a synchronization schema, etc.) to improve the system synchronization of Georgiou’s functional units to yield predictable result.” *Id.* at 75 (citing Ex. 1002 ¶¶ 53–56, 213, 215–219).

Although “[a] person of ordinary skill in the art is also a person of ordinary creativity, not an automaton” (*KSR*, 550 U.S. at 421), there may be limits in a particular case as to how much gap-filling may be based on such creativity. *See Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361 (Fed. Cir. 2016); *DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F.3d 1367, 1374–75 (Fed.

Cir. 2018) (reliance on ordinary creativity to supply a missing limitation requires same “searching” inquiry as reliance on common sense).

Here, we find that Petitioner has not met its burden to prove that one of ordinary skill in the art would have recognized that “the functional units of Georgiou operate asynchronously since they have different clocks.” Pet. 74 (citing Ex. 1002 ¶¶ 53–56, 211–219). Specifically, although Petitioner relies on Georgiou for teaching different clocks, Petitioner’s conclusory statement that such application would operate asynchronously requires gap-filling. *Id.* As Patent Owner points out, Georgiou discloses a clocking architecture in which “all domain clocks are derived from a shared master clock through predetermined rational dividers.” PO Resp. 49. Petitioner concedes during the oral hearing that, in systems such as Georgiou, each domain clock is set a fraction of a master clock, and thus, the various domain clocks are “possibly” synchronous with each other. Tr. 59:4–14 (JUDGE DANG: . . . would being fractions of the master, wouldn’t they be synchronized with each other? MR UHR: They may be, . . . the answer is possibly.”) Thus, we find Petitioner’s contention that a POSITA would have recognized that the functional units of Georgiou operate “asynchronously” lacks sufficient support in the record.

We find the testimony of Dr. Baker insufficient to support Petitioner’s position. Ex. 1002 ¶¶ 53–56, 213, 215–219. In his declaration, Dr. Baker testified that he “provided several references . . . that explain operating domains asynchronous to one another while the domains operate synchronously.” *Id.* ¶¶ 215–219. However, although such references explain “globally asynchronous, local synchronous (GALS) systems” (*id.* ¶ 216), Dr. Baker does not explain why a POSITA “would have known that a functional unit of Georgiou also operates asynchronous with respect to

other functional units” just because “the functional units of Georgiou operate at different frequencies.” *Id.* ¶ 217. Without evidentiary support, we are left with speculation and impermissible hindsight. *See in Re Wagner*, 379 F.2d 1011, 1017 (CCPA 1967). We decline to engage in speculation. *See, e.g., In re Vaidyanathan*, 381 F. App’x 985, 993 (Fed. Cir. 2010); *In re Wallen*, 565 F. App’x 867, 869 (Fed. Cir. 2014), both citing *In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001) ([T]he Board must point to some concrete evidence in the record in support of these findings.”).

In sum, based on our review of the record, we find Petitioner’s showing is insufficient. Thus, based on the complete record presented, we determine that Petitioner has not persuasively shown that Georgiou teaches “operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another,” as recited in claim 8.

6. Claims 3 and 12 as allegedly obvious over Georgiou

Petitioner contends that Georgiou teaches the limitations of claim 3 because Georgiou describes “numerous functional units,” wherein “functional units 116-1 and 116-2 are shown,” and “functional unit 116-K is provided with variable K indicating more than three functional units.” Pet. 73 (citing Ex. 1008, 3:58–61). Similarly, Petitioner contends that Georgiou also teaches the limitations of claim 12 because Georgiou discloses at least four loads. *Id.* at 76.

Patent Owner does not present arguments addressing the specific merits of Petitioner’s contentions with respect to the limitations of claims 3 and 12. *See generally* PO Resp. 49–64.

As we have determined above in section II(D)(4), the limitations of claim 1 are met by Georgiou. Having reviewed Petitioner’s arguments and

supporting evidence in the complete record, we conclude Petitioner has demonstrated by a preponderance of the evidence that Georgiou further teaches the limitations of claim 3 depending from claim 1.

However, as we have determined above in section II(D)(5), the limitations of claim 8 are not met by Georgiou. Having reviewed Petitioner's arguments and supporting evidence in the complete record, we conclude Petitioner has also failed to demonstrate by a preponderance of the evidence that Georgiou teaches the limitations of claim 12 depending from claim 8.

7. Claims 4 and 9 as allegedly obvious over Georgiou and Halepete; Claims 5 and 10 as allegedly obvious over Georgiou and Kranich

Petitioner contends Georgiou in combination with Halepete teaches or renders obvious claims 4 and 9. Pet. 76–78 (citing Ex. 1002 ¶¶ 222–227; Ex. 1008, 1:49–54, 2:28–29). Petitioner then contends Georgiou in view of Kranich teaches or renders obvious claims 5 and 10. *Id.* at 78–81 (citing Ex. 1002 ¶¶ 41–44, 228–235; Ex. 1008, 3:48–53; Ex. 1009, 9:4–5, 10:6–13, Fig. 3A). Patent Owner contends Halepete and/or Kranich do not cure the shortcomings of Georgiou. *See generally* PO Resp. 64.

As we have determined above in section II(D)(4), the limitations of claim 1 are met by Georgiou. Having reviewed Petitioner's arguments and supporting evidence in the complete record, we conclude Petitioner has demonstrated by a preponderance of the evidence that the combination of Georgiou and Halepete teaches the limitations of claim 4 depending from claim 1, and that the combination of Georgiou and Kranich teaches the limitations of claim 5 depending from claim 1.

Furthermore, as we have determined above in section II(D)(5), the limitations of claim 8 are not met by Georgiou. Petitioner does not rely on Halepete or Kranich to cure the deficiencies of Georgiou. *See* Pet. 76–80. Having reviewed Petitioner’s arguments and supporting evidence in the complete record, we conclude Petitioner has also failed to demonstrate by a preponderance of the evidence that the combination of Georgiou and Halepete teaches the limitations of claim 9 depending from claim 8, and that the combination of Georgiou and Kranich teaches the limitations of claim 10 depending from claim 8.

F. Claims 1, 3–5, 8, 9, and 12 as allegedly obvious over Shenai; Claims 4 and 9 as obvious over Shenai and Halepete; Claims 5–7, 10, and 11 as obvious over Shenai and Sherburne; and Claim 7 as obvious over Shenai, Sherburne, and Traylor

Petitioner contends that Shenai renders obvious claims 1, 3–5, 8, 9, and 12 of the ’443 patent. Pet. 21–43. Petitioner also contends that Shenai in further view of Halepete renders obvious claims 4 and 9 of the ’443 patent. *Id.* at 43–47. Petitioner further contends that Shenai in further view of Sherburne renders obvious claims 5–7, 10, and 11 of the ’443 patent. *Id.* at 47–59. Finally, Petitioner contends that Shenai and Sherburne in further view of Traylor render obvious claim 7 of the ’443 patent. *Id.* at 59–61.

In response, Patent Owner contends that Shenai is not prior art to the ’443 patent. PO Resp. 38–42. Patent Owner also contends that Shenai relies on a “rational frequency” relationship, where “clock signals are generated as integer or fractional multiples or divisions of a reference clock,” and thus fails to teach the independent clock frequency generation required by the challenged claims. *Id.* at 42–49. Patent Owner further contends that

Halepete, Sherburne, and Traylor fail to cure the shortcomings of Shenai.
Id. at 349–37.

We briefly summarize Shenai, Sherburne, and Traylor below.

1. Shenai (Ex. 1004)

Shenai, titled “Distributed Power and Supply Architecture,” discloses “[a] power distribution management apparatus,” which includes “a power and clock distribution controller capable of determining voltage, current and clock signal frequency targets for the loads.” Ex. 1004, codes (54), (57). In particular, Shenai discloses a power distribution management circuit which balances power consumption and performance for a plurality of loads, wherein the loads can be “components or subsystems of a microprocessor or microcontroller such as cache memory, register files, arithmetic logic units (ALU), integer units, instruction pipeline circuitry, hardware multipliers, floating point circuits, non-volatile memory units, or circuitry clusters.” *Id.* ¶ 25. Figure 4 of Shenai, reproduced below, illustrates a power distribution management apparatus.

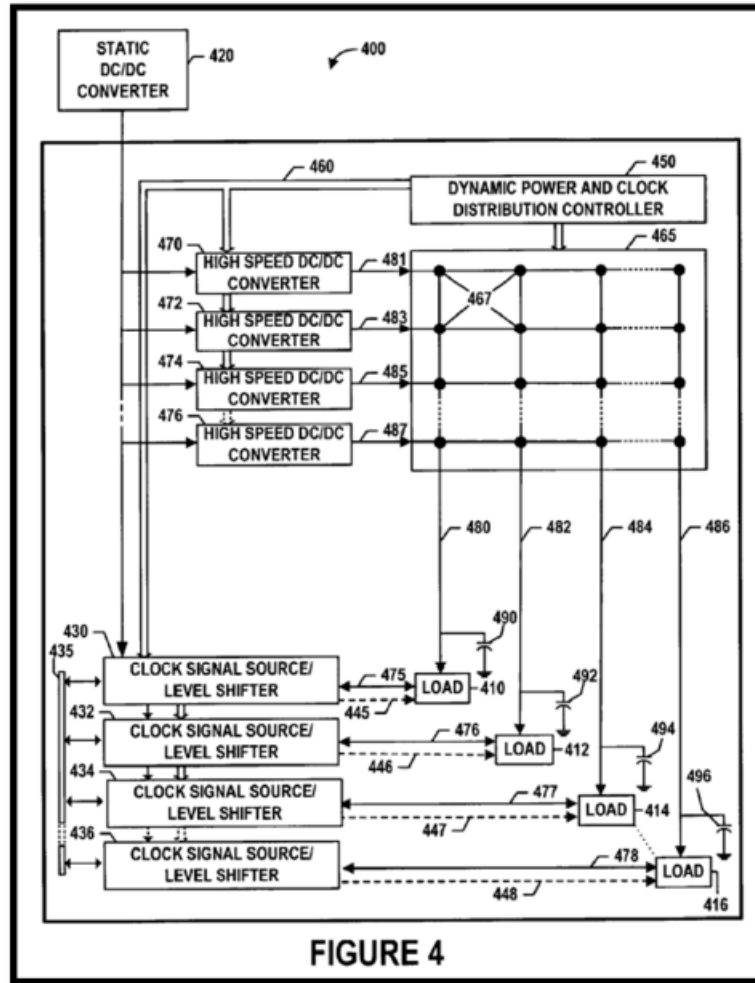


Figure 4 of Shenai shows power distribution management circuit 400 comprising controller 450, which uses clock signal sources/level shifters 430, 432, 434, 436 to provide clock signals to loads at target frequencies. Ex. 1004 ¶ 35. Further, DC/DC converters 470, 472, 474, 476 generate target voltages to the respective loads. *Id.* ¶¶ 34, 36. Clock signal sources/level shifters 430–436 are “coupled with loads 410–416 so as to provide clock signals via clock signal buses 445, 446, 447 and 448 to the loads at the target frequencies, which may be determined by controller 450.” *Id.* ¶ 35. Similarly, controller 450 selectively couples “DC/DC converters 470–476 with loads 410–416 via connection network 465’s nodes 467 and

voltage supply lines [480-487].” *Id.* ¶ 37. As “certain processing activities of software running on a microprocessor may utilize various subsystems more heavily,” controller 450 determines voltage, current, and frequency targets for the various loads. *Id.* ¶ 30.

2. Sherburne (Ex. 1006)

Sherburne, titled “Low Power Clocking Systems and Methods,” discloses “one or more processing units, each unit having a clock input that controls the performance of the unit;” “one or more clock controllers having clock outputs coupled to the clock inputs of the processing units, the controller operating [by] varying the clock frequency of each processing unit to optimize speed and processing power for a task;” and “a high-density memory array core coupled to the processing units.” Ex. 1006, codes (54), (57). In Sherburne, the output of a first buffer is provided to a processor, and a second buffer accepts data generated by the processor and provides a buffer fill level feedback signal to the controller, wherein the feedback signals include “BUFFER_FULL, BUFFER_EMPTY, or in between.” *Id.* ¶ 29. The controller, in response, varies the clock signal to the processor to increase or decrease the processing speed of the processor, thereby adjusting the fill rate to the buffer. *Id.*

3. Traylor (Ex. 1007)

Traylor, titled “FIFO Buffer with Full/Empty Detection by Comparing Respective Registers in Read and Write Circular Shift Registers,” teaches “generating control signals for a high speed First In First Out (FIFO) buffer” that “limits the instances where signal glitches may occur.” Ex. 1007, codes (54), (57). Traylor discloses flag and comparator logic blocks used for generating FULL and EMPTY control signals. *Id.* at 5:38-42. Traylor discloses that, “[g]enerally, a FIFO [device] is comprised of a memory

device, e.g. a Static Random Access Memory (SRAM), and FIFO controller.” *Id.* at 1:19-21. “EMPTY and FULL signals are used to avoid reading from an empty FIFO or writing to a full FIFO.” *Id.* at 5:44-46.

4. Claim 1 as allegedly obvious over Shenai

As an initial matter, we address in detail Petitioner’s contentions and Patent Owner’s arguments with respect to Shenai.

a) *Whether Shenai is prior art*

Patent Owner contends that the ’443 patent “was conceived and actually reduced to practice by . . . February 2002,” and thus, “any reference [such as Shenai] dated after that time is not prior art.” PO Resp. 18.

i) *Whether there was actual reduction to practice*

Patent Owner contends that, in the “Summary of the Invention” of ’443 patent, the inventors noted that “the invention” was described in an earlier paper (“the Paper”) by the inventors. PO Resp. 3 (citing Ex. 1001, 5:22–27). Citing to the Paper, Patent Owner contends that, after describing “in detail the claimed multiple clock domain microarchitecture . . . , the Paper described a detailed simulation that implemented the multiple clock domain microarchitecture prior to the publication of the Paper.” *Id.* at 15 (citing Ex. 2005 (“the Paper”), 5–8). Patent Owner then references the Declaration of inventor David H. Albonesi (Ex. 2003), who testified that “The simulation described in the Paper was completed before publication of the Paper in February, 2002.” PO Resp. 15–16 (citing Ex. 2003 ¶ 16).

Patent Owner further contends that the simulation described in the Paper used the “SimpleScalar” tool, and then relies on Dr. Kaeli’s testimony that “the Simple Scalar tool executed the simulation described in the Paper on the host,” wherein “the host executing the simulation embodied all of the

elements of claim 1 in tangible form.” PO Resp. 16 (citing Ex. 2013 ¶ 44). Thus, according to Patent Owner, “[b]y embodying all of the elements of the claims in tangible form, execution of the simulation described in the Paper constituted an actual reduction to practice of the claimed invention by February, 2002.” *Id.* Patent Owner then contends that, as the Paper explained, the performance results of the simulation demonstrate that the invention “achieved the advantages that the inventors sought to realize.” *Id.* at 17–18 (citing Ex. 2005, 11). According to Patent Owner, the simulation proved that the intended purpose of the invention, i.e., “lower energy,” “had been achieved.” *Id.* at 18 (citing Ex. 2013 ¶ 45).

Petitioner argues that the SimpleScalar simulation is not an actual reduction to practice. Pet. Reply 12. According to Petitioner, even if the multiple clock domain microarchitecture was simulated as described in the Paper, “there is no evidence that any claim of the ’443 patent was ever embodied in tangible form.” *Id.* Petitioner points out that every challenged claim “is direct to either a ‘microprocessor’ or a ‘method of operating a microprocessor,’” but “Patent Owner has presented no evidence and has not alleged any physical microprocessor was ever produced or operated.” *Id.* at 13 (citing PO Resp. 15–17). Petitioner points to Dr. Kaeli’s deposition, and contends that he “admitted that a microprocessor is a physical item,” but “confirmed that SimpleScalar was not used to fabricate anything, including a microprocessor,” as claimed. *Id.* (citing Ex. 1033, 88:11–23).

As both parties recognize, (PO Resp. 5; Pet. Reply 12), “[actual] [r]eduction to practice in the United States requires that the invention be embodied in tangible form.” *Scott v. Koyama*, 281 F.3d 1243, 1247 (Fed. Cir. 2002). In particular, actual reduction to practice requires a showing of the invention in a physical or tangible form that shows every element.

Westmore v. Quick, 536 F.2d 937, 942 (CCPA 1976). Conception alone is not sufficient. *See Kimberly-Clark v. Johnson & Johnson*, 745 F.2d 1437, 1445 (Fed. Cir. 1984).

Here, Patent Owner does not provide any evidence showing every element of the claims in physical or tangible form, as required, but rather contends that the Specification refers to the Paper, wherein the Paper stated that simulation using a software, SimpleScalar, was performed. PO Resp. 16. We are persuaded by Petitioner’s contention that the SimpleScalar simulation was not an actual reduction to practice of the claimed invention. Pet. Reply 12. As Petitioner points out, claim 1, for example, is directed to a “microprocessor,” wherein “Patent Owner has presented no evidence and has not alleged that any physical microprocessor was ever produced or operated.” *Id.* at 13; *see* PO Resp. 15–17. And as Petitioner points out, “Patent Owner has produced no evidence of any physical prototype of the claimed microprocessor that could have validated the simulation.” Pet. Reply 13–14. We agree with Petitioner that, at most, such simulation “demonstrated feasibility for prototyping of a microprocessor,” but not a tangible form of the microprocessor itself as required for an actual reduction to practice. *Id.* at 14; *see also Standard Mfg. Co. v. United States*, 25 Cl. Ct. 1, 67 (1991) (“The feasibility of the optical alignment system may have been proven by the optical mock-up, but the optical mock-up was not a reduction to practice of the proposed MHU–145/M trailer.”).

Although Patent Owner points to *Beauregard* to contend that a “computer program with executable instructions stored in memory (e.g., on a computer disk) is embodied in a tangible form” (PO Resp. 17 (citing *In re Beauregard*, 53 F.3d 1583 (Fed. Cir.1995))), we agree with Petitioner that such reliance on *Beauregard* is “misplaced” as *Beauregard* merely clarified

that computer programs embodied in a tangible medium are patentable subject matter. Pet. Reply 14. That is, determining whether or not computer programs embodied in a tangible medium can qualify as patentable subject matter is not determining that running a simulation of a microprocessor architecture using computer codes can qualify as an actual reduction to practice. *See Beauregard*, 53 F.3d at 1584.

On this record, we are unpersuaded that, by relying on the Paper referenced in the “Summary of the Invention” of the ’443 patent for a description of “a detailed simulation that implemented the multiple clock domain microarchitecture” and contending that the simulation used the “SimpleScalar” software tool (PO Resp. 16) is sufficient showing of an actual reduction to practice of the claimed microprocessor comprising the multiple clock domain microarchitecture as claimed.

ii) Whether Shenai predates the ’443 patent

Patent Owner argues that the ’443 is entitled to the February 2002 priority date because it was reduced to practice before February 2002, predating Shenai. PO Resp. 15. However, as discussed, we are persuaded by Petitioner’s arguments that the ’443 patent is not entitled to the February 2002 priority date because the claimed invention was not actually reduced to practice in tangible form before February 2002. Without the benefit of the February 2002 priority date, the ’443 patent does not predate Shenai. Accordingly, based on the record before us, we are persuaded that Shenai is prior art.

b) Whether claim 1 would have been obvious over Shenai

Petitioner contends that Shenai renders obvious claim 1 of the ’443 patent. Pet. 21–32. In particular, Petitioner contends that Shenai is directed

to the architecture of a microprocessor where “certain processing activities of software running on a microprocessor may utilize various subsystems more heavily. *Id.* at 21 (quoting Ex. 1004 ¶ 30; citing Ex. 1002 ¶¶ 104, 107). Patent Owner argues that, like Georgiou, Shenai’s reliance on rational frequency relationships fails to teach or render obvious the independent clock frequency generation required by the challenged claims. PO Resp. 42–49. We address the parties’ arguments below.

- i) *“for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains”*

Referring to Figure 4 of Shenai, Petitioner contends that Shenai’s clock signal sources/level shifters 430–436 are coupled with loads 410–416 so as to “provide clock signals via clock signal buses 445, 446, 447, and 448 to the loads at target frequencies,” wherein each clock include circuits “generating clock signals for loads 410–416” by, for example, operating “at an integer multiplication, a half-integer multiplication or a quarter-integer multiplication of a reference clock signal.” Pet. 25–26 (citing Ex. 1004 ¶¶ 35–36; Ex. 1002 ¶¶ 110–111). Petitioner provides annotated versions of Figure 4 of Shenai, reproduced below, to supports its contentions:

“for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains”

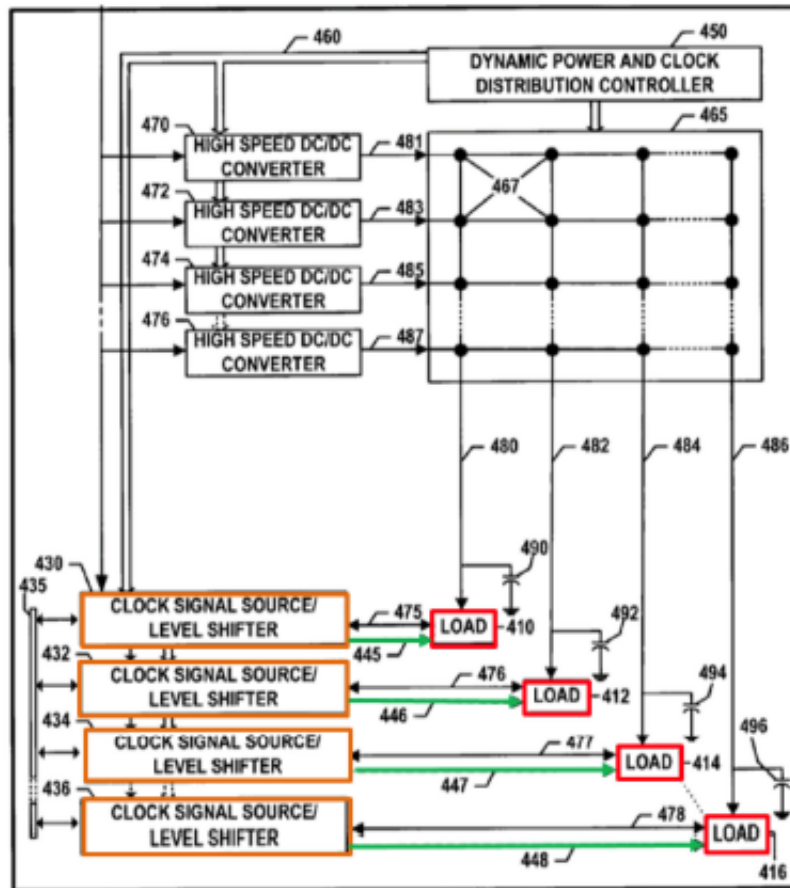


FIGURE 4

The above annotated Figure 4 of Shenai in the Petition shows a data processing system comprising clock signal sources/level shifters 430–436 (orange) providing clock signal 445–448 (green) to a respective one of loads 410–416 (red). Pet. 27. Petitioner contends that, in Shenai, the controller communicates with clock signal sources/level shifters 430–436 “associated with each [respective load]” to “**establish appropriate** operating voltage and **frequency values**” as it makes “**dynamic determinations** of actual performance versus required performance, and **further adapts** voltage and **frequency parameters** of the various subsystems.” *Id.* at 28 (quoting

Ex. 1004 ¶¶ 27–28; Ex. 1002 ¶¶ 110–11). According to Petitioner, such “dynamic determination and corresponding adaptation of ‘frequency parameters of the various subsystem,’ based on required performance for each respective load,” correspond to the claimed “dynamically changeable independently” limitation. *Id.* (citing Ex. 1002 ¶¶ 110–113).

Patent Owner responds with similar arguments it provides for the Georgiou grounds, in particular, that Shenai’s reliance on “Rational Factor” relationships fails to disclose or render obvious the claimed independent clock frequency generation required by the challenged claims. PO Resp. 42. In particular, Patent Owner argues that, in Shenai, “clock signals are generated as integer or fractional multiples or divisions of a reference clock,” and thus, like prior art systems, “Shenai imposes significant restrictions on frequency selection,” disparaged in the ’443 patent’s Specification. *Id.* Thus, Patent Owner contends that, in Shenai, “the clocks are not generated independently of the clock signal for each other’s load.” *Id.* at 46.

We find unavailing Patent Owner’s arguments, which turn on the contention that Shenai’s clock signals are generated as integer or fractional multiples or divisions of a reference clock. PO Resp. 42. That is, Patent Owner is again relying on its proposed claim construction of “dynamically changeable independently,” with which, as discussed above in Section II(A), we do not agree. Although Shenai’s clock signals are dependent on a reference clock, Patent Owner fails to show Shenai’s clock signals are also dependent on the clock signals for the other loads (domains). *See* Ex. 1004, Fig. 4. That is, like Georgiou’s clock frequencies, although Shenai’s clock frequencies in the various domains are changeable to a fraction of the same reference clock, which fraction a particular domain clock obtains does not

depend on the fraction of the reference clock frequency in the other domains.
Id.

Based on the complete record presented, we determine that Petitioner has persuasively shown that Shenai teaches “for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” as recited in claim 1.

ii) Remaining limitations of claim 1

Petitioner contends that Shenai teaches a multiple clock domain microprocessor (Pet. 21–23 (citing Ex. 1004 ¶¶ 25–26, 28, 30, 35, Fig. 4; Ex. 1002 ¶¶ 104–107)), comprising a plurality of domains. *Id.* at 24–25 (citing Ex. 1004, Fig. 4; Ex. 1002 ¶¶ 104–109). According to Petitioner, Shenai teaches “receiving an ‘appropriate operating voltage’ for each load,” wherein “DC/DC converters are ‘responsive to controller 450, such that they are selectively coupled with loads 410–416 to provide the respective target voltages and currents to the loads,’” and “[t]he controller communicates with the converters to ‘establish appropriate operating voltage[s]’ as it ‘makes dynamic determinations of actual performance versus required performance, and further adapts voltage and frequency parameters of the various subsystems.’” *Id.* at 29–32 (citing Ex. 1004 ¶¶ 26–28, 31, 37, 43, Fig. 4; Ex. 1002 ¶¶ 114–119).

Patent Owner does not present arguments addressing the specific merits of Petitioner’s contentions with respect to these claim limitations. *See generally* PO Resp. 42–49.

Based on the complete record presented, we determine that Petitioner has persuasively shown that Shenai further teaches the remaining limitations of claim 1.

c) Claim 1 conclusion

Based on the complete record presented, we determine that Petitioner has persuasively shown that claim 1 would have been obvious over Shenai.

5. Independent claim 8, as obvious over Shenai

With respect to claim 8, Petitioner repeats its contention with respect to claim 1 (Pet. 37–42), and adds that the limitation “operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another” would have been obvious to a POSITA since “[t]he circuitry of *Shenai* allows for a microprocessor to operate a plurality of loads at a plurality of independent frequencies and voltages,” which “would cause the loads of the microprocessor to operate asynchronous relative to one another.” *Id.* at 38 (citing Ex. 1004 ¶ 35; Ex. 1002 ¶¶ 133–141). According to Petitioner, “[g]lobally asynchronous, locally synchronous (GALS) systems . . . were known in the art prior to the ’443 Patent,” wherein it would have been obvious to a POSITA “to apply a known technique (e.g., globally asynchronous, locally synchronous communication) to known devices (e.g., Shenai’s loads that may be independent systems) ready for improvement to yield predictable results.” *Id.* at 39–40 (citing Ex. 1002 ¶¶ 53–56, 137, 139, 141). Petitioner contends that a POSITA would have “applied known synchronization techniques” to “Shenai’s inter-load communication to yield predictable results” for “improved synchronized communication such by improving ‘the noise tolerance of such electrical signal communication.’” *Id.* at 41–42 (citing Ex. 1002 ¶¶ 53–56, 133–141).

We find that Petitioner has not met its burden to prove that one of ordinary skill in the art would have recognized that Shenai's circuit, in which the microprocessor operates a plurality of loads at a plurality of independent frequencies and voltages, "would cause the loads of the microprocessor to operate asynchronously relative to one another." Pet. 38. Specifically, although Petitioner contends that GALS systems were known in the art prior to the '443 patent, Petitioner's conclusory statement that it would have been obvious to a POSITA to apply GALS systems to Shenai's loads requires gap-filling. *Id.* As Petitioner concedes during the oral hearing, in Shenai's system where each domain clock is set to a fraction of a master clock, the various domain clocks are "possibly" synchronous with each other. *See* Tr. 58:4–14. Thus, we find Petitioner's contention that a POSITA would have recognized that Shenai's various loads would operate "asynchronously relative to one another" (Pet. 38) lacks sufficient support in the record.

We find the testimony of Dr. Baker insufficient to support Petitioner's position. Ex. 1002 ¶¶ 53–56, 133–141. Although Dr. Baker stated that GALS was well-known (*id.* ¶¶ 137), he does not explain why a POSITA would have found it obvious to apply GALS systems to Shenai's loads. *Id.* Without evidentiary support, we are left with speculation and impermissible hindsight. *Wagner*, 379 F.2d at 1017.

Based on our review of the record, we find Petitioner's showing is insufficient. Thus, based on the complete record presented, we determine that Petitioner has not persuasively shown that Shenai teaches "operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another," as recited in claim 8.

6. Claims 3–5, 9, and 12 as allegedly obvious over Shenai

Petitioner contends that Shenai teaches the limitations of claim 3–5 because Shenai includes “loads 410, 412, 414, 416” (Pet. 32–33 (citing Ex. 1004 ¶ 25, Fig. 4)), and teaches “determining slack” (*id.* at 33–35 (citing Ex. 1004 ¶¶ 26, 30)), wherein a POSITA would have recognized that “Shenai’s circuitry allowing communication between loads would have been improved by implementing a queue.” *Id.* at 35–36 (citing Ex. 1004 ¶¶ 29, 35). Similarly, Petitioner contends that, “[a]s discussed for claim 4, Shenai determines load having non-critical paths” recited in claim 9, and “[a]s discussed in claim 3, Shenai discloses at least four loads” recited in claim 12. *Id.* at 42–43.

Patent Owner does not present arguments addressing the specific merits of Petitioner’s contentions with respect to the limitations of claims 3–5, 9, and 12. *See generally* PO Resp. 42–49.

As we have determined above in section II(F)(4), the limitations of claim 1 are met by Shenai. Having reviewed Petitioner’s arguments and supporting evidence in the complete record, we conclude Petitioner has demonstrated by a preponderance of the evidence that Shenai further teaches the limitations of claim 3–5 depending from claim 1.

Although Petitioner references its arguments with respect to claims 3 and 4 for claims 9 and 12, as we have determined above in section II(F)(5), the limitations of claim 8 from which claims 9 and 12 depend are not met by Shenai. Having reviewed Petitioner’s arguments and supporting evidence in the complete record, we conclude Petitioner has also failed to demonstrate by a preponderance of the evidence that Shenai teaches the limitations of claims 9 and 12 depending from claim 8.

7. Claims 4 and 9 as allegedly obvious over Shenai and Halepete; Claims 5–7, 10, and 11 as allegedly obvious over Shenai and Sherburne; Claim 7 as allegedly obvious over Shenai, Sherburne and Traylor

Petitioner contends Shenai in combination with Halepete teaches or renders obvious claims 4 and 9. Pet. 43–47 (citing Ex. 1004 ¶ 26; Ex. 1005, 5:5–14, 7:1–5, 7:8–25, 6:11–13, 8:11–15, 11:5–7, 11:114–16, 15:6–12; Ex. 1002 ¶¶ 45–52, 147–158). Petitioner also contends Shenai in view of Sherburne teaches or renders obvious claims 5–7, 10, and 11. *Id.* at 47–59 (citing Ex. 1004 ¶¶ 2, 4; Ex. 1006 ¶¶ 4, 13, 21–22, 26, 28–31, 35, 39–40, Fig. 3; Ex. 1002 ¶¶ 34–44, 159–186). Petitioner then contends Shenai in view of Sherburne and Traylor teaches or renders obvious claim 7. *Id.* at 59–61 (citing Ex. 1006 ¶ 26; Ex. 1007, 1:19–21, 4:59–62; Ex. 1002 ¶¶ 187–191).

Patent Owner contends Halepete, Sherburne and/or Traylor do not cure the shortcomings of Shenai. *See generally* PO Resp. 49.

As we have determined above in section II(F)(4), the limitations of claim 1 are met by Shenai. Having reviewed Petitioner’s arguments and supporting evidence in the complete record, we conclude Petitioner has demonstrated by a preponderance of the evidence that the combination of Shenai and Halepete teaches the limitations of claim 4 depending from claim 1, that the combination of Shenai and Sherburne teaches the limitations of claims 5–7 depending from claim 1, and that the combination of Shenai, Sherburne and Traylor teaches the limitations of claim 7 depending from claim 1.

Furthermore, as we have determined above in section II(F)(5), the limitations of claim 8 are not met by Shenai. Petitioner does not rely on

Halepete, Sherburne or Traynor to cure the deficiencies of Shenai. *See* Pet. 43–61. Having reviewed Petitioner’s arguments and supporting evidence in the complete record, we conclude Petitioner has also failed to demonstrate by a preponderance of the evidence that the combination of Shenai and Halepete teaches the limitations of claim 9 depending from claim 8, and that the combination of Shenai and Sherburne teaches the limitations of claims 10 and 11 depending from claim 8.

III. CONCLUSION⁵

For the foregoing reasons, we determine on the record at hand that Petitioner has demonstrated by a preponderance of the evidence that challenged claims 1 and 3–7 of the ’443 patent are unpatentable, but has not demonstrated by a preponderance of the evidence that challenged claims 8–12 and of the ’443 patent are unpatentable.

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 3, 8, 12	103	Georgiou	1, 3	8, 12
4, 9	103	Georgiou, Halepete	4	9

⁵ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

5, 10	103	Georgiou, Kranich	5	10
1, 3–5, 8, 9, 12	103	Shenai	1, 3–5	8, 9, 12
4, 9	103	Shenai, Halepete	4	9
5–7, 10, 11	103	Shenai, Sherburne	5–7	10, 11
7	103	Shenai, Sherburne, Traynor	7	
Overall Outcome			1, 3–7	8–12

IV. ORDER

For the reasons given, it is

ORDERED that, based on the preponderance of the evidence, claims 1 and 3–7 of the '443 patent have been shown to be unpatentable;

ORDERED that, based on the preponderance of the evidence, claims 8–12 of the '443 patent have not been shown to be unpatentable; and

FURTHER ORDERED that, because this is a final written decision, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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