AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 **Director of the U.S. Patent and Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313-1450**	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:23-cv-307	4/26/2023	Western District of Texas

PLAINTIFF	DEFENDANT
Intellectual Ventures I LLC and Intellectual Ventures II LLC	Lenovo Group Limited

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,325,140	1/29/2008	Intellectual Ventures II LLC
2	8,474,016	6/25/2013	Intellectual Ventures II LLC
3	7,089,443	8/8/2006	Intellectual Ventures I LLC
4	7,623,439	11/24/2009	Intellectual Ventures I LLC
5	7,646,835	1/12/2010	Intellectual Ventures II LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1			
2			
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

Petitioner Lenovo (United States) Inc. - Ex. 1003

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:23-cv-290	4/20/2023	Western District of Texas

PLAINTIFF	DEFENDANT
Intellectual Ventures I and Intellectual Ventures II	OnePlus Technology (Shenzen) Co., Ltd.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,623,439	11/24/2009	Intellectual Ventures I
2	7,646,835	1/12/2010	Intellectual Ventures II
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1			
2			
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,646,835 B1
APPLICATION NO. : 10/716320
DATED : January 12, 2010
INVENTOR(S) : Guillermo J. Rozas

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page:

The first or sole Notice should read --

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 938 days.

Signed and Sealed this

Sixteenth Day of November, 2010

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

IV (TRANSMETA)
C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

Mail Date: 04/21/2010

Applicant	: Guillermo J. Rozas	: DECISION ON REQUEST FOR
Patent Number	: 7646835	: RECALCULATION of PATENT
Issue Date	: 01/12/2010	: TERM ADJUSTMENT IN VIEW
Appliction No	: 10/716,320	: OF WYETH AND NOTICE OF INTENT TO
Filed	: 11/17/2003	: ISSUE CERTIFICATE OF CORRECTION
		:

The Request for Recalculation is **GRANTED** to the extent indicated.

The patent term adjustment has been determined to be **938** days. The USPTO will *sua sponte* issue a certificate of correction reflecting the amount of PTA days determined by the recalculation.

Prior to the issuance of the certificate of correction, the USPTO will afford patentee an opportunity to be heard and request reconsideration. Accordingly, patentee has **one month or thirty (30) days**, whichever is longer, to file a request for reconsideration of this patent term adjustment calculation. See 35 U.S.C. 154(b)(3)(B)(ii) and 37 CFR 1.322(a)(4). No extensions of time will be granted under 37 CFR 1.136.

Patentee should use document code PET.OP if electronically filing a request for reconsideration of this patent term adjustment calculation. The patentee must also include the information required by 37 CFR 1.705(b)(2) and the fee required by 37 CFR 1.18(e). If patentee does not file a timely request for reconsideration of this patent term adjustment calculation including the information required by 37 CFR 1.705(b)(2) and the fee required by 37 CFR 1.18(e), the USPTO will issue a certificate of correction reflecting the PTA determination noted above.

Patentee should be aware that in order to preserve the right to review in the United States District Court for the District of Columbia of the USPTO patent term adjustment determination, patentee must ensure that he or she also take the steps required under 35 U.S.C. 154(b)(4)(A) in a timely manner. Nothing in the request for recalculation should be construed as providing an alternative time frame for commencing a civil action under 35 U.S.C. 154(b)(4)(A).

Any questions concerning this decision should be directed to the Office of Patent Legal Administration at 571-272-7702.

PTO/SB/131 (01-10)
Approved for use through 02/28/2011. OMB 0651-0020
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST FOR RECALCULATION OF PATENT TERM ADJUSTMENT IN VIEW OF *WYETH**

Attorney Docket Number: TRAN-P156	Patent Number: 7646835
Filing Date (or 371(b) or (f) Date): 11-17-2003	Issue Date: 01-12-2010
First Named Inventor: Guillermo J. Rozas	
Title: METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE	

PATENTEE HEREBY REQUESTS RECALCULATION OF THE PATENT TERM ADJUSTMENT (PTA) UNDER 35 USC 154(b) INDICATED ON THE ABOVE-IDENTIFIED PATENT. THE PATENTEE'S SOLE BASIS FOR REQUESTING THE RECALCULATION IS THE USPTO'S PRE-*WYETH* INTERPRETATION OF 35 U.S.C. 154(b)(2)(A).

Note: This form is only for requesting a recalculation of PTA for patents issued before March 2, 2010, if the sole basis for requesting the recalculation is the USPTO's pre-*Wyeth* interpretation of 35 U.S.C. 154(b)(2)(A). See Instruction Sheet on page 2 for more information.

Patentees are reminded that to preserve the right to review in the United States District Court for the District of Columbia of the USPTO's patent term adjustment determination, a patentee must ensure that he or she also takes the steps required under 35 U.S.C. 154(b)(3) and (b)(4) and 37 CFR 1.705 in a timely manner.

**Wyeth v. Kappos*, No. 2009-1120 (Fed. Cir., Jan. 7, 2010).

Signature /Jose S. Garcia/	Date 2-16-2010
Name (Print/Typed) Jose S. Garcia	Registration Number 43628

Note: *Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the form of the signature. If necessary, submit multiple forms for more than one signature, see below**.

☐ *Total of _____ forms are submitted.

The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	7038874
Application Number:	10716320
International Application Number:	
Confirmation Number:	5239
Title of Invention:	METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	Jose S. Garcia/Missy Isaac
Filer Authorized By:	Jose S. Garcia
Attorney Docket Number:	TRAN-P156
Receipt Date:	18-FEB-2010
Filing Date:	17-NOV-2003
Time Stamp:	15:28:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition for review by the Office of Petitions.	TRAN-P156_PTA_Wyeth_form.pdf	126031 10dcc07d1642d423c9af9b3b7565793fbf92c0cc	no	1

Warnings:	
Information:	

Total Files Size (in bytes):	126031

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	01/12/2010	7646835	TRAN-P156	5239

45590 7590 12/23/2009

TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 644 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Guillermo J. Rozas, Los Gatos, CA;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Mina Oliveri	(Depositor's name)
/Mina Oliveri/	(Signature)
11-30-09	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$0	$1510	11/30/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_ 3_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☑ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☑ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-4160 .

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Anthony C. Murabito/ Date 11-30-2009

Typed or printed name Anthony C. Murabito Registration No. 35,295

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	10716320
Filing Date:	17-Nov-2003
Title of Invention:	METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Filer:	Anthony C. Murabito/Mina Oliveri
Attorney Docket Number:	TRAN-P156

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**1510**

Electronic Acknowledgement Receipt

EFS ID:	6540048
Application Number:	10716320
International Application Number:	
Confirmation Number:	5239
Title of Invention:	METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	Anthony C. Murabito/Mina Oliveri
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	TRAN-P156
Receipt Date:	30-NOV-2009
Filing Date:	17-NOV-2003
Time Stamp:	16:26:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$1510
RAM confirmation Number	7671
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Issue Fee Payment (PTO-85B)	TRAN-P156_IssueFee_Trans_11-30-09.pdf	234645 fa7e43adf5cc210f29c685c72da336cf9700273d	no	2
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	30307 207115e94e0dcdd34b795abbaaa67c2202bacd64	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	264952	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

45590 7590 08/31/2009

TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
ODOM, CURTIS B	
ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 08/31/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

TITLE OF INVENTION: METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$0	$0	$1510	11/30/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

45590 7590 08/31/2009

TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

TITLE OF INVENTION: METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$0	$0	$1510	11/30/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
ODOM, CURTIS B	2611	375-354000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_____ 3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

45590 7590 08/31/2009

TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
ODOM, CURTIS B	
ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 08/31/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 644 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 644 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	CURTIS B. ODOM	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filed on 8/14/2009*.

2. ☒ The allowed claim(s) is/are *1-20,22,25 and 26*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on 8/14/2009 and 8/19/2009 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Allowable Subject Matter

2. The following is an examiner's statement of reasons for allowance: Claims 1-20, 22, and 25, and 26 are allowable over prior art references because related references do not disclose altering inter-cycle timing relationships between signals by altering a phase shift of command signals, a phase shift of data signals, and a phase shift of sampling to determine a valid operation range of an integrated circuit device (DRAM or DDR DRAM).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CURTIS B. ODOM whose telephone number is (571)272-3046. The examiner can normally be reached on Monday- Friday, 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Curtis B. Odom/
Primary Examiner, Art Unit 2611
August 22, 2009

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10716320	ROZAS, GUILLERMO J.
	Examiner	Art Unit
	CURTIS B ODOM	2611

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/20/2008	12/07/2008	05/08/2009	08/22/2009					
	1	✓	✓	=	=					
	2	✓	✓	=	=					
	3	✓	✓	=	=					
	4	✓	✓	=	=					
	5	✓	✓	=	=					
	6	✓	✓	=	=					
	7	✓	✓	=	=					
	8	✓	✓	=	=					
	9	✓	✓	=	=					
	10	✓	✓	=	=					
	11	✓	✓	=	=					
	12	✓	✓	=	=					
	13	✓	✓	=	=					
	14	✓	✓	=	=					
	15	✓	✓	=	=					
	16	✓	✓	=	=					
	17	✓	✓	=	=					
	18	✓	✓	=	=					
	19	✓	✓	=	=					
	20	✓	✓	=	=					
	21	-	-	-	-					
	22	✓	✓	=	=					
	23		✓	-	-					
	24		✓	-	-					
	25			=	=					
	26			=	=					

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10716320	ROZAS, GUILLERMO J.
	Examiner	**Art Unit**
	CURTIS B ODOM	2611

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
375	354	H 0 4 L 7 / 00 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
375	371	372	373	374	375
375	376				
714	767	768	769	770	771
714	772	773			
365	194				

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	19	17												
2	2	20	18												
3	3	21	19												
4	4	22	20												
5	5		21												
6	6	23	22												
7	7		23												
8	8		24												
9	9	14	25												
10	10	15	26												
11	11														
12	12														
13	13														
16	14														
17	15														
18	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 23	
/CURTIS B ODOM/ Primary Examiner.Art Unit 2611 (Primary Examiner)	8/22/2009 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination
10/716,320	ROZAS, GUILLERMO J.
Examiner	**Art Unit**
CURTIS B. ODOM	2611

SEARCHED			
Class	Subclass	Date	Examiner
UPDATED		8/22/2009	CBO

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
375	**354**	8/22/2009	**CBO**
375	371-376	8/22/2009	CBO

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
UPDATED	8/22/2009	CBO

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	173	((phase or timing) near3 (command or address$4)) and ((phase or timing) near3 (data or "DQ" or information)) and ((phase or timing) near3 (sampl$5 or "DQS")) and (phase same ((range or point) near2 operat$4))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/08/22 16:06
L2	144	((phase or timing) near3 (command or address$4)) and ((phase or timing) near3 (data or "DQ" or information)) and ((phase or timing) near3 (sampl$5 or "DQS")) and (phase same (region near2 (operat$4 or valid)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/08/22 16:06
L3	136	L2 not L1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/08/22 16:06
L4	3	((714/767-773.ccls. or 375/354.ccls. or 375/371-376.ccls.) or (365/194.ccls. or 365/233.ccls.)) and L3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/08/22 16:06
L5	19	("20010045779" | "20020113622" | "5568350" | "5745375" | "5757172" | "6025737" | "6304824" | "6448815" | "6947865").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/08/22 16:06
L6	6	("6772352" | "6832177" | "7191088").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/08/22 16:07

L7	25	L5 or L6	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/08/22 16:07
S1	7	(714/767-773.ccls. or 375/354.ccls. or 371-376.ccls.) and (phase with (sampl$4 with (command or instruct $4) with (data or information)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:11
S2	13	((synchroniz$4 or align $4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40
S3	7	((adjust$4) near3 phase) same (sampl$4 adj2 signals) same ((command or instruct $4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:19
S4	1	((calibrat$4) near3 (phase or timing)) same (sampl$4 adj2 signals) same ((command or instruct $4 or address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S5	0	((synchroniz$4 or align $4) near3 phase) with (sampl$4 adj2 signals) with ((address) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S6	1	((synchroniz$4 or align $4) near3 phase) same (sampl$4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21

S7	3	"DRAM" same (sampl $4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21
S8	3	"DRAM" same (sampl $4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:23
S9	3	"DRAM" same (sampl $4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S10	325	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S11	66	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) same (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S12	2749	365/194.ccls. or 365/233.ccls. and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 10:47

S13	1453	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S14	318	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05
S15	13	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:13
S16	2	S15 and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:54
S17	1267	("DQ" and "DQS") same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:55
S18	13	S17 and ((phase or timing) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S19	10	S17 and ((delay$4) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:10

S20	47	S17 and ((phase or timing) same ((command or address) adj1 signals) same ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S21	11	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:18
S22	14	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S23	70	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S24	70	((phase or timing or synchroniz44) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22

S25	77	((phase or timing or synchroniz$4) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22
S26	965	S13 and "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S27	20	S26 and fine and coarse	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S28	1612	((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:08
S29	35	S28 and (fine same coarse)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:09
S30	0	Rozas.in. and ((synchroniz$4 or align $4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40
S31	0	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" near3 inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05

S32	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
S33	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
S34	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing or synchroniz44) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S35	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with (inoperable or inoperative))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:26
S36	3	(memory adj1 controller) same "DRAM" same coarse same fine	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:28
S37	10	((memory adj1 controller) same "DRAM") and ((memory adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:29

S38	11	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:45
S39	126	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) and (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:38
S40	87	(((memory or DRAM) adj1 controller) same "DRAM") and ((memory or DRAM) adj1 controller) and (coarse same fine same (address or command or data or clock))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:49
S41	1	"6016282".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S42	1	"6115318".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:44
S43	1	"6115318".pn. and (coarse same fine) and (coarse and fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S44	1	"6016282".pn. and (coarse same fine) and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S45	2	"6553472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/09/04 03:37
S46	2	"6553472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:50
S47	274	phase same (command same sampl $4 same data) same (adjust$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:52
S48	432	((adjust$4 or chang$4) with (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:53

S49	302	((adjust$4 or chang$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:54
S50	245	((adjust$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:54
S51	47	((calibrat$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:09
S52	1	((calibrat$4) near4 (phase or timing)) same (command adj1 signals) same (data adj1 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:10
S53	3	"20030131160".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:11
S54	3	"20030131160".pn. and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:12
S55	2	"20030131160".pn. and (sampl$4 same calibrat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:12
S56	1	"20030131160".pn. and (sampl$4 same calibrat$4) and (calibrat $4 same data same command)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:13
S57	2	"20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:35
S58	2	"20030122696".pn. and calibrat$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:36
S59	1	"20030122696".pn. and calibrat$4 and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:36

S60	2	"6553473".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/07/20 13:40
S61	4	"6553473".pn. or "20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/07/20 13:41
S62	4	"6553472".pn. or "20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/07/20 13:41
S63	1	"20030122696".pn. and (read$4 and writ $4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/12/05 10:56
S64	276	((calibrat$4 or synchroniz$4) near4 (phase or timing)) same (command same (sampl$4 or clock$4) same data) same (memory or RAM or DRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/05 11:11
S65	230	S64 and (read$4 and writ$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/05 11:12
S66	228	S64 and (read$4 and writ$5) and (operat$5 or inoperativ$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/05 11:26
S67	6	"6324171"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:08
S68	276	((calibrat$4 or synchroniz$4) near4 (phase or timing)) same (command same (sampl$4 or clock$4) same data) same (memory or RAM or DRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:37
S69	4	S68 and (inoperativ$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:37
S70	6	S68 and (operating adj2 point)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:39

S71	0	((DRAM or RAM or SDRAM) adj5 (inoperable or inoperative)) and ((DRAM or RAM or SDRAM) same ((calibrat $4 or synchroniz$4 or align) near4 (phase or timing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:52
S72	1	((DRAM or RAM or SDRAM) with (inoperable or inoperative)) and ((DRAM or RAM or SDRAM) same ((calibrat $4 or synchroniz$4 or align) near4 (phase or timing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:52
S73	32	((DRAM or RAM or SDRAM or memory) with (inoperable or inoperative)) and ((DRAM or RAM or SDRAM or memory) same ((calibrat$4 or synchroniz$4 or align) near4 (phase or timing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:53
S74	222	((DRAM or RAM or SDRAM or memory) with (inoperable or inoperative)) and ((DRAM or RAM or SDRAM or memory) same ((calibrat$4 or synchroniz$4 or align) same (read$4 or writ $4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:54
S75	199	S74 not S73	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:54
S76	38	((DRAM or RAM or SDRAM or memory) adj5 (inoperable or inoperative)) and ((DRAM or RAM or SDRAM or memory) same ((calibrat$4 or synchroniz$4 or align) same (read$4 or writ $4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:55

S77	30	S76 not S73	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:55
S78	1035	((DRAM or RAM or SDRAM or memory) adj5 (disabl$5)) and ((DRAM or RAM or SDRAM or memory) same ((calibrat$4 or synchroniz$4 or align) same (read$4 or writ $4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:58
S79	305	((DRAM or RAM or SDRAM) adj5 (disabl $5)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align $4) same (read$4 or writ$4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:58
S80	177	((DRAM or RAM or SDRAM) adj5 (disabl $5)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align $4) with (read$4 or writ$4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:59
S81	206	((DRAM or RAM or SDRAM) adj5 (disabl $5)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align $4) same (phase or timing))) and (command same (sampl$4 or clock$4) same data)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 16:03
S82	175	((DRAM or RAM or SDRAM) adj3 (disabl $5)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align $4) same (phase or timing))) and (command same (sampl$4 or clock$4) same data)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 16:04

S83	2	"20020078316".pn. and (disabl$4 or operat $4 or inoperative or inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 16:11
S84	1	"20020078316".pn. and (disabl$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 16:13
S85	1	"20030122696".pn. and (memory adj2 controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/12/06 17:41
S86	0	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) same ((range or point) near3 operat $54)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/03/27 21:22
S87	34	((phase or timing) same ((command$4 or address$4)) same ((sampling or "DQS")) same ((data or information))) same ((range or point) near3 operat$54)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/03/27 21:22
S88	147	((phase or timing) same ((command$4 or address$4 or control $5)) same ((sampling or "DQS")) same ((data or information))) same ((range or point) near3 operat$54)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/03/27 21:23
S89	169	((phase or timing) near3 (command or address$4)) and ((phase or timing) near3 (data or "DQ" or information)) and ((phase or timing) near3 (sampl$5 or "DQS")) and (phase same ((range or point) near2 operat$4))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 16:48

S90	0	(((phase or timing) near3 (command or address$4)) and ((phase or timing) near3 (data or "DQ" or information)) and ((phase or timing) near3 (sampl$5 or "DQS")) and ((range or point) near2 operat $4)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:26
S91	192	((phase or timing) near3 (command or address$4)) and ((phase or timing) near3 (data or "DQ" or information)) and ((phase or timing) near3 (sampl$5 or "DQS")) and (phase same (region near2 (operat$4 or region)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:26
S92	138	((phase or timing) near3 (command or address$4)) and ((phase or timing) near3 (data or "DQ" or information)) and ((phase or timing) near3 (sampl$5 or "DQS")) and (phase same (region near2 (operat$4 or valid)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:27
S93	130	S92 not S89	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:27
S94	0	((714/767-773.ccls. or 375/354.ccls. or 371-376.ccls.) or (365/194. ccls. or 365/233.ccls.)) and S93	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:30
S95	9	((phase or timing) near3 (command or address$4)) and ((phase or timing) near3 (data or "DQ" or information)) and ((phase or timing) near3 (sampl$5 or "DQS")) and ("DRAM" same ((range or point) near2 operat$4))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:36

S96	3	((714/767-773.ccls. or 375/354.ccls. or 375/371-376.ccls.) or (365/194.ccls. or 365/233.ccls.)) and S93	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:43

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(Not for submission under 37 CFR 1.99)

Application Number	10716320
Filing Date	2003-11-17
First Named Inventor	Guillermo J. Rozas
Art Unit	2611
Examiner Name	Odom, Curtis B.
Attorney Docket Number	TRAN-P156

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/CO/	1	5568350		1996-10-22	Brown	
/CO/	2	5745375		1998-04-28	Reinhardt, et al.	
/CO/	3	5757172		1998-05-26	Hunsdorf, et al.	
/CO/	4	6025737		2000-02-15	Patel, et al.	
/CO/	5	6304824		2001-10-16	Bausch, et al.	
/CO/	6	6448815		2002-09-10	Talbot, et al.	
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/CO/	1	20010045779		2001-11-29	Lee, et al.	
/CO/	2	20020113622		2002-08-22	Tang	

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/CO/	2	6832177		2004-12-14	Khandekar, et al.	
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	Examiner Name	Odom, Curtis B.
	Attorney Docket Number	TRAN-P156

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Glenn Barnes/	Date (YYYY-MM-DD)	2009-08-18
Name/Print	Glenn Barnes	Registration Number	42293

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	10716320
Filing Date	2003-11-17
First Named Inventor	Guillermo J. Rozas
Art Unit	2611
Examiner Name	Odom, Curtis B.
Attorney Docket Number	TRAN-P156

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6772352		2004-08-03	Williams, et al.	
	2	6832177		2004-12-14	Khandekar, et al.	
	3	7191088		2007-03-13	Reed, et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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	Application Number	10716320
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	First Named Inventor	Guillermo J. Rozas
	Art Unit	2611
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	Attorney Docket Number	TRAN-P156

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Application Number	10716320
	Filing Date	2003-11-17
	First Named Inventor	Guillermo J. Rozas
	Art Unit	2611
	Examiner Name	Odom, Curtis B.
	Attorney Docket Number	TRAN-P156

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Glenn Barnes/	Date (YYYY-MM-DD)	2009-08-18
Name/Print	Glenn Barnes	Registration Number	42293

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Electronic Acknowledgement Receipt

EFS ID:	5908679
Application Number:	10716320
International Application Number:	
Confirmation Number:	5239
Title of Invention:	METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	Glenn D. Barnes/Mina Oliveri
Filer Authorized By:	Glenn D. Barnes
Attorney Docket Number:	TRAN-P156
Receipt Date:	18-AUG-2009
Filing Date:	17-NOV-2003
Time Stamp:	14:34:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	TRAN-P156_IDS_Transmittal_8-18-09.pdf	779147 4de9754d5e3a0767bef693277a9a364751d26df7	no	4

Warnings:	
Information:	

Total Files Size (in bytes):	779147

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 10/716,320	Filing Date 11/17/2003	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	08/18/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 23	Minus	** 23	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DEBRA a. SAVOY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	10716320	Filing Date	2003-11-17	Docket Number (if applicable)	TRAN-P156	Art Unit	2611
First Named Inventor	Guillermo J. Rozas			Examiner Name	Odom, Curtis B.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 504160

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Signature of Registered U.S. Patent Practitioner			
Signature	/Glenn Barnes/	Date (YYYY-MM-DD)	2009-08-14
Name	Glenn Barnes	Registration Number	42293

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

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Filing Date	2003-11-17
First Named Inventor	Guillermo J. Rozas
Art Unit	2611
Examiner Name	Odom, Curtis B.
Attorney Docket Number	TRAN-P156

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5568350		1996-10-22	Brown	
	2	5745375		1998-04-28	Reinhardt, et al.	
	3	5757172		1998-05-26	Hunsdorf, et al.	
	4	6025737		2000-02-15	Patel, et al.	
	5	6304824		2001-10-16	Bausch, et al.	
	6	6448815		2002-09-10	Talbot, et al.	
	7	6947865		2005-09-20	Mimberg, et al.	

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Examiner Name	Odom, Curtis B.
Attorney Docket Number	TRAN-P156

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20010045779		2001-11-29	Lee, et al.	
	2	20020113622		2002-08-22	Tang	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10716320
	Filing Date	2003-11-17
	First Named Inventor	Guillermo J. Rozas
	Art Unit	2611
	Examiner Name	Odom, Curtis B.
	Attorney Docket Number	TRAN-P156

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10716320
	Filing Date	2003-11-17
	First Named Inventor	Guillermo J. Rozas
	Art Unit	2611
	Examiner Name	Odom, Curtis B.
	Attorney Docket Number	TRAN-P156

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Glenn Barnes/	Date (YYYY-MM-DD)	2009-08-14
Name/Print	Glenn Barnes	Registration Number	42293

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	10716320
Filing Date:	17-Nov-2003
Title of Invention:	METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Filer:	Glenn D. Barnes/Mina Oliveri
Attorney Docket Number:	TRAN-P156

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**810**

Electronic Acknowledgement Receipt

EFS ID:	5895807
Application Number:	10716320
International Application Number:	
Confirmation Number:	5239
Title of Invention:	METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	Glenn D. Barnes/Mina Oliveri
Filer Authorized By:	Glenn D. Barnes
Attorney Docket Number:	TRAN-P156
Receipt Date:	14-AUG-2009
Filing Date:	17-NOV-2003
Time Stamp:	20:21:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$810
RAM confirmation Number	4489
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Request for Continued Examination (RCE)	TRAN-P156_RCE_Transmittal_8-14-09.pdf	769168 a01bb5af0f322a38dda8b8f7be0a2020a3fcf7fe	no	3
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Filed (SB/08)	TRAN-P156_IDS_Transmittal_8-14-09.pdf	1062927 c5f12fd92e1b09e520863b23a7c7db26ecfcf1d0	no	5
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	30562 102cf8e206a7aa0955c922d1c088fec374f32805	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	1862657	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

45590 7590 05/14/2009

TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
ODOM, CURTIS B	
ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 05/14/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

TITLE OF INVENTION: METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$0	$0	$1510	08/14/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

45590 7590 05/14/2009

TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

TITLE OF INVENTION: METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$0	$0	$1510	08/14/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
ODOM, CURTIS B	2611	375-354000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_____ 3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

45590 7590 05/14/2009

TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
ODOM, CURTIS B	
ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 05/14/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 644 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 644 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	CURTIS B. ODOM	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdt filed on 3/12/2009*.

2. ☒ The allowed claim(s) is/are *1-20,22,25 and 26*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Allowable Subject Matter

1. The following is an examiner's statement of reasons for allowance: Claims 1-20, 22, and 25, and 26 are allowable over prior art references because related references do not disclose altering inter-cycle timing relationships between signals by altering a phase shift of command signals, a phase shift of data signals, and a phase shift of sampling to determine a valid operation range of an integrated circuit device (DRAM or DDR DRAM).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CURTIS B. ODOM whose telephone number is (571)272-3046. The examiner can normally be reached on Monday- Friday, 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Curtis B. Odom/
Primary Examiner, Art Unit 2611
May 8, 2009

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	169	((phase or timing) near3 (command or address$4)) and ((phase or timing) near3 (data or "DQ" or information)) and ((phase or timing) near3 (sampl$5 or "DQS")) and (phase same ((range or point) near2 operat$4))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 16:48
L2	0	(((phase or timing) near3 (command or address$4)) and ((phase or timing) near3 (data or "DQ" or information)) and ((phase or timing) near3 (sampl$5 or "DQS")) and ((range or point) near2 operat $4)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:26
L3	192	((phase or timing) near3 (command or address$4)) and ((phase or timing) near3 (data or "DQ" or information)) and ((phase or timing) near3 (sampl$5 or "DQS")) and (phase same (region near2 (operat$4 or region)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:26
L4	138	((phase or timing) near3 (command or address$4)) and ((phase or timing) near3 (data or "DQ" or information)) and ((phase or timing) near3 (sampl$5 or "DQS")) and (phase same (region near2 (operat$4 or valid)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:27

L5	130	L4 not L1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:27
L6	0	((714/767-773.ccls. or 375/354.ccls. or 371-376.ccls.) or (365/194.ccls. or 365/233.ccls.)) and L5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:30
L7	9	((phase or timing) near3 (command or address$4)) and ((phase or timing) near3 (data or "DQ" or information)) and ((phase or timing) near3 (sampl$5 or "DQS")) and ("DRAM" same ((range or point) near2 operat$4))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:36
L8	3	((714/767-773.ccls. or 375/354.ccls. or 375/371-376.ccls.) or (365/194.ccls. or 365/233.ccls.)) and L5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/08 17:43
S1	7	(714/767-773.ccls. or 375/354.ccls. or 371-376.ccls.) and (phase with (sampl$4 with (command or instruct $4) with (data or information)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:11
S2	13	((synchroniz$4 or align $4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40
S3	7	((adjust$4) near3 phase) same (sampl$4 adj2 signals) same ((command or instruct $4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:19

S4	1	((calibrat$4) near3 (phase or timing)) same (sampl$4 adj2 signals) same ((command or instruct $4 or address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S5	0	((synchroniz$4 or align $4) near3 phase) with (sampl$4 adj2 signals) with ((address) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S6	1	((synchroniz$4 or align $4) near3 phase) same (sampl$4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21
S7	3	"DRAM" same (sampl $4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21
S8	3	"DRAM" same (sampl $4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:23
S9	3	"DRAM" same (sampl $4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25

S10	325	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S11	66	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) same (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S12	2749	365/194.ccls. or 365/233.ccls. and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 10:47
S13	1453	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S14	318	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05

S15	13	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:13
S16	2	S15 and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:54
S17	1267	("DQ" and "DQS") same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:55
S18	13	S17 and ((phase or timing) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S19	10	S17 and ((delay$4) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:10
S20	47	S17 and ((phase or timing) same ((command or address) adj1 signals) same ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S21	11	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:18

S22	14	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S23	70	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S24	70	((phase or timing or synchroniz44) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22
S25	77	((phase or timing or synchroniz$4) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22
S26	965	S13 and "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S27	20	S26 and fine and coarse	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S28	1612	((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:08

S29	35	S28 and (fine same coarse)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:09
S30	0	Rozas.in. and ((synchroniz$4 or align $4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40
S31	0	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" near3 inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05
S32	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
S33	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06

S34	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing or synchroniz44) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S35	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with (inoperable or inoperative))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:26
S36	3	(memory adj1 controller) same "DRAM" same coarse same fine	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:28
S37	10	((memory adj1 controller) same "DRAM") and ((memory adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:29
S38	11	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:45
S39	126	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) and (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:38

S40	87	(((memory or DRAM) adj1 controller) same "DRAM") and ((memory or DRAM) adj1 controller) and (coarse same fine same (address or command or data or clock))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:49
S41	1	"6016282".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S42	1	"6115318".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:44
S43	1	"6115318".pn. and (coarse same fine) and (coarse and fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S44	1	"6016282".pn. and (coarse same fine) and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S45	2	"6553472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/09/04 03:37
S46	2	"6553472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:50
S47	274	phase same (command same sampl $4 same data) same (adjust$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:52
S48	432	((adjust$4 or chang $4) with (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:53
S49	302	((adjust$4 or chang$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:54

S50	245	((adjust$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:54
S51	47	((calibrat$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:09
S52	1	((calibrat$4) near4 (phase or timing)) same (command adj1 signals) same (data adj1 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:10
S53	3	"20030131160".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:11
S54	3	"20030131160".pn. and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:12
S55	2	"20030131160".pn. and (sampl$4 same calibrat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:12
S56	1	"20030131160".pn. and (sampl$4 same calibrat$4) and (calibrat$4 same data same command)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:13
S57	2	"20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:35
S58	2	"20030122696".pn. and calibrat$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:36
S59	1	"20030122696".pn. and calibrat$4 and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:36
S60	2	"6553473".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/07/20 13:40
S61	4	"6553473".pn. or "20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/07/20 13:41
S62	4	"6553472".pn. or "20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/07/20 13:41

S63	1	"20030122696".pn. and (read$4 and writ $4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/12/05 10:56
S64	276	((calibrat$4 or synchroniz$4) near4 (phase or timing)) same (command same (sampl$4 or clock$4) same data) same (memory or RAM or DRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/05 11:11
S65	230	S64 and (read$4 and writ$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/05 11:12
S66	228	S64 and (read$4 and writ$5) and (operat$5 or inoperativ$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/05 11:26
S67	6	"6324171"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:08
S68	276	((calibrat$4 or synchroniz$4) near4 (phase or timing)) same (command same (sampl$4 or clock$4) same data) same (memory or RAM or DRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:37
S69	4	S68 and (inoperativ$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:37
S70	6	S68 and (operating adj2 point)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:39
S71	0	((DRAM or RAM or SDRAM) adj5 (inoperable or inoperative)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align) near4 (phase or timing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:52

S72	1	((DRAM or RAM or SDRAM) with (inoperable or inoperative)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align) near4 (phase or timing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:52
S73	32	((DRAM or RAM or SDRAM or memory) with (inoperable or inoperative)) and ((DRAM or RAM or SDRAM or memory) same ((calibrat$4 or synchroniz$4 or align) near4 (phase or timing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:53
S74	222	((DRAM or RAM or SDRAM or memory) with (inoperable or inoperative)) and ((DRAM or RAM or SDRAM or memory) same ((calibrat$4 or synchroniz$4 or align) same (read$4 or writ $4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:54
S75	199	S74 not S73	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:54
S76	38	((DRAM or RAM or SDRAM or memory) adj5 (inoperable or inoperative)) and ((DRAM or RAM or SDRAM or memory) same ((calibrat$4 or synchroniz$4 or align) same (read$4 or writ $4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:55
S77	30	S76 not S73	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:55

S78	1035	((DRAM or RAM or SDRAM or memory) adj5 (disabl$5)) and ((DRAM or RAM or SDRAM or memory) same ((calibrat$4 or synchroniz$4 or align) same (read$4 or writ $4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:58
S79	305	((DRAM or RAM or SDRAM) adj5 (disabl $5)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align $4) same (read$4 or writ$4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:58
S80	177	((DRAM or RAM or SDRAM) adj5 (disabl $5)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align $4) with (read$4 or writ$4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:59
S81	206	((DRAM or RAM or SDRAM) adj5 (disabl $5)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align $4) same (phase or timing))) and (command same (sampl$4 or clock$4) same data)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 16:03
S82	175	((DRAM or RAM or SDRAM) adj3 (disabl $5)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align $4) same (phase or timing))) and (command same (sampl$4 or clock$4) same data)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 16:04
S83	2	"20020078316".pn. and (disabl$4 or operat $4 or inoperative or inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 16:11

S84	1	"20020078316".pn. and (disabl$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 16:13
S85	1	"20030122696".pn. and (memory adj2 controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/12/06 17:41
S86	0	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) same ((range or point) near3 operat $54)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/03/27 21:22
S87	34	((phase or timing) same ((command$4 or address$4)) same ((sampling or "DQS")) same ((data or information))) same ((range or point) near3 operat$54)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/03/27 21:22
S88	147	((phase or timing) same ((command$4 or address$4 or control $5)) same ((sampling or "DQS")) same ((data or information))) same ((range or point) near3 operat$54)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/03/27 21:23

5/8/09 6:10:19 PM
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10716320	ROZAS, GUILLERMO J.
	Examiner	Art Unit
	CURTIS B ODOM	2611

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/20/2008	12/07/2008	05/08/2009						
	1	✓	✓	=						
	2	✓	✓	=						
	3	✓	✓	=						
	4	✓	✓	=						
	5	✓	✓	=						
	6	✓	✓	=						
	7	✓	✓	=						
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	9	✓	✓	=						
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	13	✓	✓	=						
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	20	✓	✓	=						
	21	-	-	-						
	22	✓	✓	=						
	23		✓	-						
	24		✓	-						
	25			=						
	26			=						

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10716320	ROZAS, GUILLERMO J.
	Examiner	**Art Unit**
	CURTIS B ODOM	2611

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
375	354	H 0 4 L 7 / 00 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
375	371	372	373	374	375
375	376				
714	767	768	769	770	771
714	772	773			
365	194				

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	19	17												
2	2	20	18												
3	3	21	19												
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17	15														
18	16														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	23	
/CURTIS B ODOM/ Primary Examiner.Art Unit 2611	5/8/2009	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination
10/716,320	ROZAS, GUILLERMO J.
Examiner	**Art Unit**
CURTIS B. ODOM	2611

SEARCHED			
Class	Subclass	Date	Examiner
UPDATED		5/8/2009	CBO

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
375	**354**	5/8/2009	**CBO**
375	371-376	5/9/2009	CBO

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
UPDATED	5/8/2009	CBO
INTERFERENCE SEARCH	5/8/2009	CBO

S/N 10/716,320 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Rozas G. Examiner: Odom, C.

Serial No.: 10/716,320 Group Art Unit: 2611

Filed: 11/17/03 Docket No.: TRAN-P156

Title: A METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant has reviewed the Office Action mailed on December 12th, 2008.

Please consider the following amendments and remarks.

IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the method comprising:

generating command signals [[for]] to access[[ing]] an integrated circuit component;

accessing data signals [[for]] to convey[[ing]] data for the integrated circuit component;

accessing sampling signals [[for]] to control[[ling]] [[the]] sampling of the data signals; and

~~for both data write transactions and data read transactions, automatically adjusting a phase relationship between~~ systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals ~~to calibrate operation of~~ to determine a valid operation range of the integrated circuit device, wherein the~~ automatic adjusting is free of user input~~ valid operation range includes an optimal operation point for the integrated circuit device.

2. (Currently Amended) The method of claim 1, wherein the integrated circuit device [[is]] comprises a DRAM component.

3. (Currently Amended) The method of claim 2, wherein ~~the adjusting of the phase relationship~~ said altering is performed by a memory controller coupled to the DRAM component.

4. (Currently Amended) The method of claim 2, wherein the DRAM component [[is]] comprises a DDR DRAM component.

5. (Currently Amended) The method of claim 4, wherein the data signals comprise a plurality of data bus (DQ) signals for the DDR DRAM component.

6. (Currently Amended) The method of claim 5, wherein the sampling signals comprise a plurality of sampling bus (DQS) signals for the DDR DRAM component.

7. (Currently Amended) A system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the system comprising:

a controller configured to [[for]] generate[[ing]] command signals for accessing an integrated circuit component;

a delay calibrator integrated within the controller and configured to access data signals conveying data for the integrated circuit device and to access sampling signals for controlling [[the]] sampling of the data signals, ~~and for both data write transactions and data read transactions,~~ wherein the delay calibrator is further configured to ~~automatically adjust a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, without requiring a valid initial operating point to exist within the specified operating parameters for the integrated circuit device, and wherein the automatic adjusting is free of user input~~ systematically alter a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device; and wherein the valid operation range includes an optimal operation point for the integrated circuit device.

8. (Currently Amended) The ~~method~~ system of claim 7, wherein the integrated circuit device [[is]] comprises a DRAM component.

9. (Currently Amended) The ~~method~~ system of claim 8, wherein the DRAM component [[is]] comprises a DDR DRAM component.

10. (Currently Amended) The ~~method~~ system of claim 9, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

11. (Currently Amended) The ~~method~~ system of claim 10, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

12. (Currently Amended) In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, the method comprising:

generating command signals [[for]] to access[[ing]] a DRAM component;

accessing data signals [[for]] to convey[[ing]] data for the DRAM component;

accessing sampling signals [[for]] to control[[ling]] [[the]] sampling of the data signals; and

~~for both data write transactions and data read transactions, automatically~~ systematically altering ~~a phase relationship between~~ a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a[[n]] valid operating ~~mode~~ range of the DRAM component~~, without requiring a valid initial operating point to exist within the specified operating parameters for the DRAM component, and wherein the automatic altering is free of user input~~.

13. (Currently Amended) The method of claim 12, further comprising:

performing a coarse calibration by altering ~~the phase relationship~~ the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the

sampling signals in accordance with a large step interval to [[find]] determine if the valid operating [[mode]] range of the DRAM component exists; and

if the valid operating range exists, then performing a fine calibration by altering ~~the phase relationship~~ the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a small step interval to identify an optimal ~~optimize the~~ operating mode of the DRAM component.

14. (Currently Amended) The method of claim 13, further comprising[[:]] configuring the memory controller to operate [[with]] the DRAM component in ~~accordance with an~~ the optimal operating mode~~, wherein the optimal operating mode is determined via the fine calibration~~.

15. (Currently Amended) The method of claim 12, wherein the DRAM component [[is]] comprises a DDR DRAM component.

16. (Original) The method of claim 15, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

17. (Original) The method of claim 16, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

18. (Currently Amended) A computer-readable media having stored thereon, computer-executable instructions that, if executed by a processor, cause the processor to perform a method for finding an operating mode for a DDR DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, ~~the media storing computer readable code which when executed by a memory controller causes the memory controller to implement a~~ the method comprising:

generating command signals [[for]] to access[[ing]] a DDR DRAM component;

accessing DQ signals [[for]] to convey[[ing]] DQ signals for the DDR DRAM component;

accessing DQS signals [[for]] to control[[ling]] [[the]] sampling of the DQ signals; and

~~for both data write transactions and data read transactions, automatically~~ systematically altering ~~a phase relationship between~~ a phase shift of the command signals, a phase shift of the DQ signals, and a phase shift of the DQS signals to determine a[[n]] valid operating ~~mode~~ range of the DDR DRAM component~~, without requiring a valid initial operating point within the specified operating parameters for the DRAM component~~.

19. (Currently Amended) The computer-readable media of claim 18, wherein the method further ~~comprising~~ comprises:

performing a coarse calibration by altering ~~the phase relationship~~ the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a large step interval ~~to find~~ if the valid operating [[mode]] range of the DDR DRAM component exists; and

if the valid operating range exists, then performing a fine calibration by altering ~~the phase relationship~~ the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a small step interval to identify an optimal ~~optimize the~~ operating mode of the DDR DRAM component.

20. (Currently Amended) The computer-readable media of claim 19, wherein the method further ~~comprising:~~ comprises configuring the memory controller to operate [[with]] the DRAM component in ~~accordance with an~~ the optimal operating mode~~,~~ ~~wherein the optimal operating mode is determined via the fine calibration~~.

21. (Cancelled)

22. (Currently Amended) In a memory controller, a method for finding an operating mode for a DDR DRAM component coupled to a PCB (printed circuit board) by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the method comprising:

generating command signals [[for]] to access[[ing]] a DDR DRAM component;

accessing data signals [[for]] to convey[[ing]] data for the DDR DRAM component;

accessing sampling signals [[for]] to control[[ling]] [[the]] sampling of the data signals; and

~~for both data write transactions and data read transactions, automatically~~ systematically altering ~~a phase relationship between~~ a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals transmitted via a PCB to determine a[[n]] valid operating ~~mode~~ range of the DDR DRAM component~~, wherein the DDR DRAM component is inoperable at specified operating parameters, and wherein said automatic altering is performed free of user input~~.

23. (Canceled)

24. (Canceled))

25. (New) The method of claim 13, wherein said performing a coarse calibration comprises simultaneously varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal by a five percent step increase.

26. (New) The method of claim 13, wherein said performing a fine calibration

comprises varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal one at a time by a two percent step increase.

REMARKS/ARGUMENTS

Applicant acknowledges the rejection of Claims 1-20 and 22-24 with a right to traverse. Claims 1-6, 7-15, 18-20, and 22 are currently amended; Claims 23 and 24 are canceled; and Claims 25 and 26 are newly added. As a result, Claims 1-20, 22, 25, and 26 are pending in this application. No new matter has been introduced.

Applicant respectfully requests further examination and reconsideration of the rejections for the reasons stated below.

Claim Objections

Claims 23 and 24 are objected because of informalities. Claims 23 and 24 are canceled herein therefore, the objections are moot.

§103 Rejection of the Claims

Claims 1-3 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over U.S. Patent No. 6,553,472 (hereinafter "Yang") in view of U.S. Patent No. 6,606,041 (hereinafter "Johnson").

Applicant respectfully submits that the rejection fails to establish a prima facie case of obviousness since the combined references of Yang and Johnson fail to teach each and every element of the Claims.

Currently amended independent Claim 1 is recited below:

> 1. A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the method comprising:
> generating command signals to access an integrated circuit component;
> accessing data signals to convey data for the integrated circuit component;
> accessing sampling signals to control sampling of the data signals; and
> systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device, wherein the valid operation range includes an optimal operation point for the integrated circuit device.

The rejection states that Yang does not disclose "automatically adjusting a phase (timing) between the command signals, the data signals, and the clock (sampling) signals to calibrate (optimize) operation of the integrated circuit device," but alleges that Johnson "discloses calibrating timing (phase) relationship between control (command) and data signals (see section 0001), wherein calibrating the timing relationship between the data and command blocks also correctly calibrates the sampling (signals) of the data (see section 0006)" as recited in previously presented Claim 1.

However, regarding amended Claim 1, Applicant respectfully submits that the combined references fail to teach or suggest the claimed limitations of "systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device, wherein the valid operation range includes an optimal operation point for the integrated circuit device." Although section 0001 of Johnson teaches calibrating the timing of control and data signals in DRAM memory devices, Johnson fails to teach or suggest calibrating timing of sampling of the data signals. In addition, even though section 0006 of Johnson recites sampling of data by synchronously timing command clock signals and data clock signals, Johnson fails to teach or suggest the claimed limitations of systematically altering respective phase shifts of the command, data, and sampling signals to determine a valid operation range of the integrated device. That is, Johnson discloses achieving sampling or timing calibration by determining an optimal delay for the command signals and the data signals, whereas Claim 1 recites the determination of the valid range of the integrated circuit device by systemically altering the phase shift of the sampling signals as well as the phase shift of the command signal and the phase shift of the data signal, as claimed. Since the combined references fail to teach each and every element of Claim 1, Applicant respectfully requests the withdrawal of the rejection, and solicits allowance of Claim 1. Since Claims 2 and 3 are dependent on allowable Claim 1, the Claims overcome the rejections of record by virtue of their dependency to Claim 1 and for the additional features they recite, and respectfully solicit allowance of these Claims.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Yang in view of Johnson, and further in view of U.S. Patent No. 6,850,459 (hereinafter "Suzuki"). Since Claims 4-6 are dependent on allowable Claim 1, the Claims overcome the rejections of record by virtue of their dependency to Claim 1 and for the additional features they recite. Accordingly, Applicant respectfully solicits allowance of these Claims.

Claims 7, 8, 12, and 22 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Yang in view of Johnson, and further in view of U.S. Patent No. 6,898,683 (hereinafter "Nakamura"). Since independent Claims 7, 12, and 22 recite at least those features similar to that of Claim 1, and they are therefore patentable over the cited references for the same reasons. As such, allowance of the Claims is earnestly solicited. Since Claim 8 is dependent on allowable Claim 7, the Claim overcomes the rejection of record by virtue of its dependency to Claim 7 and for the additional features it recites. Accordingly, Applicant respectfully solicits allowance of the Claim.

Claims 9-11 and 15-18 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Yang in view of Johnson, further in view of Nakamura, and yet further in view of Suzuki. Since Claims 9-11 are dependent on allowable Claim 7, the Claims overcome the rejection of record by virtue of their dependency to Claim 7 and for the additional features they recite. Accordingly, Applicant respectfully solicits allowance of

the Claims. Likewise, since Claims 15-17 overcome the rejection of record by virtue of their dependency to Claim 12 and for the additional features they recite, they should be allowed accordingly. Independent Claim 18 recites at least those features similar to that of Claim 1 and is therefore patentable over the cited references for the same reasons.

Claims 13, 14, 23, and 24 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Yang in view of Johnson, further in view of Nakamura, and yet further in view of U.S. Patent Application 6,016,282 (hereinafter "Keeth"). Since Claims 13 and 14 are dependent on Claim 12, the Claims overcome the rejection of record by virtue of their dependency to Claim 12 and for the additional features they recite, and respectfully solicit allowance of the Claims. Likewise, Claims 23 and 24 should be allowed for their dependency to Claim 22 and for the additional features they recite, and the Applicant respectfully solicits allowance of the Claims.

Particularly, regarding previously presented Claim 13, the rejection states that the combined references of Yang, Johnson, Nakamura, and Keeth teach the claimed limitations as Keeth "states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, lines 46-55)." However, Applicant respectfully asserts that the combined references fail to teach or suggest the claimed limitations of "performing a coarse calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a large step

interval to determine if the valid operating range of the DRAM component exists, and if the valid operating range exists, then performing a fine calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a small step interval to identify an optimal operating mode of the DRAM component."

Applicant respectfully submits that Keeth fails to disclose that the coarse calibration performed by the vernier clock adjustment circuit determines "if the valid operating range of the DRAM component exists," as claimed. Unlike Claim 13, Keeth discloses that the coarse calibration performed by the vernier clock adjustment circuit provides coarse steps defined in bit periods (see column 4, lines 15-18). Furthermore, Applicant respectfully asserts that Keeth fails to teach or suggest that the fine calibration performed by the vernier clock adjustment circuit is used to "identify an optimal operating mode of the DRAM component," as claimed. Instead, unlike Claim 13, Keeth discloses that the fine calibration performed by the vernier clock adjustment circuit provides fine steps to cover adjustments within a single bit period (see column 4, lines 15-18). Since the combined references fail to teach each and every element of Claim 13, Applicant respectfully requests the withdrawal of the rejection and solicits allowance of Claim 13.

Accordingly, allowance of the pending Claims 1-20, 22, 25, and 26 is earnestly solicited.

Conclusion

Applicant respectfully submits that the Claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

Murabito, Hao & Barnes LLP

Date 03-12-2009

By /Steve S. Ko/
Steve S. Ko
Reg. No. 58,757

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060

Electronic Acknowledgement Receipt

EFS ID:	4959125
Application Number:	10716320
International Application Number:	
Confirmation Number:	5239
Title of Invention:	Method and system for automatically calibrating intra-cycle timing relationships for sampling signals for an integrated circuit device
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	Steve S. Ko/Mina Oliveri
Filer Authorized By:	Steve S. Ko
Attorney Docket Number:	TRAN-P156
Receipt Date:	12-MAR-2009
Filing Date:	17-NOV-2003
Time Stamp:	18:50:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		TRAN-P156_2279USAP160016_AMDT_03-11-09.pdf	169522 af495932e3fe645b5a94f4605d2cc7623a428b35	yes	17

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	10
	Applicant Arguments/Remarks Made in an Amendment	11	17
Warnings:			
Information:			
	Total Files Size (in bytes):	169522	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/716,320	11/17/2003	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT	03/12/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 23	Minus	** 23	= 0	X $ =		OR	X $52 =	0
	Independent (37 CFR 1.16(h))	* 5	Minus	*** 5	= 0	X $ =		OR	X $220 =	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	**0**

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/THERESA LINDSAY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

45590 7590 12/12/2008

TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
ODOM, CURTIS B	
ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
12/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	CURTIS B. ODOM	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10/23/2008 have been fully considered but they are not persuasive. On page 12 of the Remarks, the Applicant states Johnson (US 20030122696) does not disclose calibrating for both data write transactions and data read transactions. However, Johnson discloses discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). Johnson further discloses the calibration is performed for both read and write data transactions (see section 0046) so that read and write data and synchronized to the clock signals. With regards to the remainder of the arguments presented in the Remarks, the arguments are moot in view of the new grounds of rejection below.

Claim Objections

2. Claims 23 and 24 are objected to because of the following informalities: In claims 23 and 24, "computer readable media" is suggested to be changed to "memory controller". Appropriate correction is required.

Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in Office Action 1/25/2008).

Regarding claim 1, Yang et al. discloses a method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals by implementing programmable time delays (see column 3, lines 10-23) for an integrated circuit device SDRAM), comprising:

generating command signals (see column 3, lines 36-43) for accessing an integrated circuit component;

accessing data signals (see column 3, lines 36-43) for conveying data for the integrated circuit component;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67).

Yang et al. does not disclose for both read and write transactions, automatically adjusting a phase (timing) between the command signals, the data signals, and the clock (sampling) signals

to calibrate (optimize) operation of the integrated circuit device, wherein the automatic adjusting is free of user input.

However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place on the edge of a clock signal (see section 0036) and is free from a user input. Johnson further discloses the calibration is performed for both read and write data transactions (see section 0046) so that read and write data and synchronized to the clock signals. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Regarding claim 2, Yang et al. further discloses the circuit device is an SDRAM (see column 3, lines 10-23).

Regarding claim 3, Johnson et al. further discloses adjusting a timing (phase) relationship is performed by a memory controller (Fig. 1, block 13, section 0006)) coupled to an SDRAM component. It would have been obvious to include this feature since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

5. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in Office Action 1/25/2008), and in further view of Suzuki (previously cited in Office Action 1/8/2007).

Regarding claims 4-6, Yang et al. and Johnson et al. do not specifically disclose the calibrated SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to enable both reading and writing for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al. and Johnson et al. with the DDR SDRAM of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

6. Claims 7, 8, 12, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in Office Action 1/25/2008), and in further view of Nakamura (US 2002/0078316).

Regarding claim 7, Yang et al. discloses a system (see Fig. 2) for calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals by implementing programmable time delays (see column 3, lines 10-23) for an integrated circuit device SDRAM), comprising:

a controller (Fig. 2, block 31) for generating command signals (see column 3, lines 36-43) for accessing an integrated circuit component;

a delay calibrator of programmable delays (see column 5, line 31-column 6, line 25 and column 8, lines 41-67) integrated within the controller (see column 6, lines 20-25) for accessing data signals (see column 3, lines 36-43) for conveying data for the integrated circuit device and

for accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67), for both read and write transactions, the delay calibrator configured to adjust a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19 and column 8, lines 41-67) to calibrate (optimize) operation of the integrated circuit device.

Yang et al. does not disclose the phase relationship is automatically adjusted free of user input wherein the calibration takes place without a valid initial operation point that exists within specified operating parameters.

However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place on the edge of a clock signal (see section 0036) and is free from a user input. Johnson further discloses the calibration is performed for both read and write data transactions (see section 0046) so that read and write data and synchronized to the clock signals. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Nakamura further discloses during a normal mode of operation a clock synchronization (calibration) in an SDRAM component and during a power down mode the SDRAM component

is not accessed (inoperable) for read/write operations (see section 0059). Furthermore, during the power down mode, command signals are still synchronized to the clock signals even though the SDRAM is inoperable (see sections 0075-0076). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the device/method of Yang et al. and Johnson et al. with the power down mode of Nakamura to maintain synchronization while the SDRAM is inoperable since Nakamura states the power down mode (data hold mode) reduces power consumption (see sections 0059 and 0062).

Regarding claim 8, Yang et al. further discloses the circuit device is an SDRAM (see column 3, lines 10-23).

Regarding claim 12, Yang et al. discloses a method for finding an initialization point in a SDRAM (see column 2, lines 30-39) by altering intra-cycle timing relationships between command signals, data signals, and sampling (clock) signals by implementing programmable time delays (see column 3, lines 10-23) for the SDRAM, comprising:

generating command signals (see column 3, lines 36-43) for accessing the SDRAM;

accessing data signals (see column 3, lines 36-43) for conveying data for the SDRAM;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

for both read and write transactions, adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column

5, line 32-column 6, line 19) to calibrate (optimize) operation of the DRAM and find an optimal initialization point (see column 2, lines 30-39).

Yang et al. does not disclose the phase relationship is automatically adjusted free of user input wherein the calibration takes place without a valid initial operation point that exists within specified operating parameters.

However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place on the edge of a clock signal (see section 0036) and is free from a user input. Johnson further discloses the calibration is performed for both read and write data transactions (see section 0046) so that read and write data and synchronized to the clock signals. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Nakamura further discloses during a normal mode of operation a clock synchronization (calibration) in an SDRAM component and during a power down mode the SDRAM component is not accessed (inoperable) for read/write operations (see section 0059). Furthermore, during the power down mode, command signals are still synchronized to the clock signals even though the SDRAM is inoperable (see sections 0075-0076). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the device/method of Yang et al. and Johnson et al. with the power down mode of Nakamura to maintain synchronization while

the SDRAM is inoperable since Nakamura states the power down mode (data hold mode) reduces power consumption (see sections 0059 and 0062).

Regarding claim 22, Yang et al. discloses in a memory controller, a method for finding an initialization (operating) point in a SDRAM (see column 2, lines 30-39) coupled to a memory controller of a microprocessor chip which represents a printed circuit board (see column 1, lines 19-25) by altering intra-cycle timing relationships between command signals, data signals, and sampling (clock) signals by implementing programmable time delays (see column 3, lines 10-23) for the SDRAM, comprising:

generating command signals (see column 3, lines 36-43) for accessing the SDRAM;

accessing data signals (see column 3, lines 36-43) for conveying data for the SDRAM;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

for both read and write transactions, adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the DRAM and find an optimal initialization point (see column 2, lines 30-39).

Yang et al. does not disclose the SDRAM is a DDR DRAM, the phase relationship is automatically adjusted free of user input wherein the DDR DRAM is inoperable at specified operating parameters.

However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001) in a DDR SLDRAM (see section 0010), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place on the edge of a clock signal (see section 0036) and is free from a user input. Johnson further discloses the calibration is performed for both read and write data transactions (see section 0046) so that read and write data and synchronized to the clock signals. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Nakamura further discloses during a normal mode of operation a clock synchronization (calibration) in an SDRAM component and during a power down mode the SDRAM component is not accessed (inoperable) for read/write operations (see section 0059). Furthermore, during the power down mode, command signals are still synchronized to the clock signals even though the SDRAM is inoperable (see sections 0075-0076). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the device/method of Yang et al. and Johnson et al. with the power down mode of Nakamura to maintain synchronization while the SDRAM is inoperable since Nakamura states the power down mode (data hold mode) reduces power consumption (see sections 0059 and 0062).

7. Claims 9-11 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously

cited in Office Action 1/25/2008), and in view of Nakamura (US 2002/0078316), and in further view of Suzuki (previously cited in Office Action 1/8/2007).

Regarding claims 9-11 and 15-17, Yang et al., Johnson et al., and Nakamura do not specifically disclose the calibrated SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to enable both reading and writing for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al., Johnson et al., and Nakamura with the DDR SDRAM of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

Regarding claim 18, Yang et al., Johnson et al., and Nakamura disclose all the limitations of claim 18 (see rejection of claim 12), including the operations of the SDRAM written as software (see Yang et al., column 2, lines 11-16). Yang et al., Johnson et al., and Nakamura do not specifically disclose the calibrated SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to determine both reading and writing operations for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have

been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al., Johnson et al., and Nakamura with the DDR SDRAM (and DQ and DQS signals for control of the DDR SDRAM) of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

8. Claims 13, 14, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in Office Action 1/25/2008), and in view of Nakamura (US 2002/0078316) as applied to claim 12, and in further in view of Keeth (previously cited in Office Action 1/8/2007).

Regarding claims 13, 14, 23, and 24, Yang et al. discloses configuring the memory controller to operate with the DRAM in accordance with an optimal operating mode (see column 6, lines 20-25). Yang et al, Johnson et al., and Nakamura do not disclose the time delay operation involves performing a coarse time delay calibration by altering the timing relationship in accordance with a large step interval to find the operating mode of the (DDR) DRAM component; and performing a fine time delay calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the (DDR) DRAM component, wherein the optimal operating mode is determined by the fine calibration.

However, Keeth discloses a memory device (see Fig. 1) including a memory controller (see Fig. 1, block 22) coupled to a DRAM (Fig. 1, block 26), wherein minimum and maximum delays from command at the memory controller to read data an the memory controller are accommodated by performing vernier clock adjustments, wherein there is a coarse delay adjustment with a large bit interval and a fine delay adjustment with a smaller interval (within a bit period (see column 4, lines 11-18 and column 7, lines 44-51). Therefore, it would have been

obvious to one skilled in the art at the time the invention was made to modify the timing delays of Yang et al., Johnson et al., and Nakamura with the coarse and fine delay as disclosed by Keeth since Keeth states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, liens 46-55).

9. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in Office Action 1/25/2008), in view of Nakamura (2002/0078316) in view of Suzuki (previously cited in Office Action 1/8/2007) as applied to claim 18, and in further view of Keeth (previously cited in Office Action 1/8/2007).

Regarding claims 19 and 20 (see above rejection of claim 18), Yang et al. discloses configuring the memory controller to operate with the DRAM in accordance with an optimal operating mode (see column 6, lines 20-25). Yang et al., Johnson et al., Nakamura, and Suzuki do not disclose the time delay operation involves performing a coarse time delay calibration by altering the timing relationship in accordance with a large step interval to find the operating mode of the DRAM component; and performing a fine time delay calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component, wherein the optimal operating mode is determined by the fine calibration.

However, Keeth discloses a memory device (see Fig. 1) including a memory controller (see Fig. 1, block 22) coupled to a DRAM (Fig. 1, block 26), wherein minimum and maximum delays from command at the memory controller to read data an the memory controller are accommodated by performing vernier clock adjustments, wherein there is a coarse delay adjustment with a large bit interval and a fine delay adjustment with a smaller interval (within a

bit period (see column 4, lines 11-18 and column 7, lines 44-51). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the timing delays of Yang et al., Johnson et al., Nakamura, and Suzuki with the coarse and fine delay as disclosed by Keeth since Keeth states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, liens 46-55).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CURTIS B. ODOM whose telephone number is (571)272-3046. The examiner can normally be reached on Monday- Friday, 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Curtis B. Odom/
Examiner, Art Unit 2611
December 7, 2008

Notice of References Cited	Application/Control No. 10/716,320	Applicant(s)/Patent Under Reexamination ROZAS, GUILLERMO J.	
	Examiner CURTIS B. ODOM	Art Unit 2611	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2002/0078316	06-2002	Nakamura, Toshikazu	711/167
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10716320	ROZAS, GUILLERMO J.
	Examiner	Art Unit
	CURTIS B ODOM	2611

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/20/2008	12/07/2008							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	✓	✓							
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	13	✓	✓							
	14	✓	✓							
	15	✓	✓							
	16	✓	✓							
	17	✓	✓							
	18	✓	✓							
	19	✓	✓							
	20	✓	✓							
	21	-	-							
	22	✓	✓							
	23		✓							
	24		✓							

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	CURTIS B. ODOM	2611	

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	CURTIS B. ODOM	2611	

SEARCHED			
Class	Subclass	Date	Examiner
UPDATED		12/6/2008	CBO

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
UPDATED	12/6/2008	CBO

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CONFIRMATION NO. 5239

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/716,320	11/17/2003	398	2611	TRAN-P156

APPLICANTS
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**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
02/17/2004

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/CURTIS B ODOM/ Examiner's Signature	☐ Initials	CA	5	22	6

ADDRESS

TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113
UNITED STATES

TITLE

Method and system for automatically calibrating intra-cycle timing relationships for sampling signals for an integrated circuit device

FILING FEE RECEIVED		
1666	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	7	(714/767-773.ccls. or 375/354.ccls. or 371-376.ccls.) and (phase with (sampl$4 with (command or instruct $4) with (data or information)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:11
S2	13	((synchroniz$4 or align $4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40
S3	7	((adjust$4) near3 phase) same (sampl$4 adj2 signals) same ((command or instruct $4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:19
S4	1	((calibrat$4) near3 (phase or timing)) same (sampl$4 adj2 signals) same ((command or instruct $4 or address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S5	0	((synchroniz$4 or align $4) near3 phase) with (sampl$4 adj2 signals) with ((address) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S6	1	((synchroniz$4 or align $4) near3 phase) same (sampl$4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21

S7	3	"DRAM" same (sampl $4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21
S8	3	"DRAM" same (sampl $4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:23
S9	3	"DRAM" same (sampl $4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S10	325	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S11	66	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) same (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S12	2749	365/194.ccls. or 365/233.ccls. and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 10:47

S13	1453	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S14	318	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05
S15	13	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:13
S16	2	S15 and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:54
S17	1267	("DQ" and "DQS") same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:55
S18	13	S17 and ((phase or timing) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S19	10	S17 and ((delay$4) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:10

S20	47	S17 and ((phase or timing) same ((command or address) adj1 signals) same ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S21	11	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:18
S22	14	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S23	70	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S24	70	((phase or timing or synchroniz44) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22

S25	77	((phase or timing or synchroniz$4) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22
S26	965	S13 and "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S27	20	S26 and fine and coarse	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S28	1612	((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:08
S29	35	S28 and (fine same coarse)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:09
S30	0	Rozas.in. and ((synchroniz$4 or align $4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40
S31	0	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" near3 inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05

S32	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
S33	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
S34	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing or synchroniz44) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S35	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with (inoperable or inoperative))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:26
S36	3	(memory adj1 controller) same "DRAM" same coarse same fine	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:28
S37	10	((memory adj1 controller) same "DRAM") and ((memory adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:29

S38	11	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:45
S39	126	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) and (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:38
S40	87	(((memory or DRAM) adj1 controller) same "DRAM") and ((memory or DRAM) adj1 controller) and (coarse same fine same (address or command or data or clock))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:49
S41	1	"6016282".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S42	1	"6115318".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:44
S43	1	"6115318".pn. and (coarse same fine) and (coarse and fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S44	1	"6016282".pn. and (coarse same fine) and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S45	2	"6553472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/09/04 03:37
S46	2	"6553472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:50
S47	274	phase same (command same sampl $4 same data) same (adjust$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:52
S48	432	((adjust$4 or chang $4) with (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:53

S49	302	((adjust$4 or chang$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:54
S50	245	((adjust$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:54
S51	47	((calibrat$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:09
S52	1	((calibrat$4) near4 (phase or timing)) same (command adj1 signals) same (data adj1 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:10
S53	3	"20030131160".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:11
S54	3	"20030131160".pn. and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:12
S55	2	"20030131160".pn. and (sampl$4 same calibrat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:12
S56	1	"20030131160".pn. and (sampl$4 same calibrat$4) and (calibrat$4 same data same command)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:13
S57	2	"20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:35
S58	2	"20030122696".pn. and calibrat$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:36
S59	1	"20030122696".pn. and calibrat$4 and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:36

S60	2	"6553473".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/07/20 13:40
S61	4	"6553473".pn. or "20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/07/20 13:41
S62	4	"6553472".pn. or "20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/07/20 13:41
S63	1	"20030122696".pn. and (read$4 and writ $4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/12/05 10:56
S64	276	((calibrat$4 or synchroniz$4) near4 (phase or timing)) same (command same (sampl$4 or clock$4) same data) same (memory or RAM or DRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/05 11:11
S65	230	S64 and (read$4 and writ$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/05 11:12
S66	228	S64 and (read$4 and writ$5) and (operat$5 or inoperativ$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/05 11:26
S67	6	"6324171"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:08
S68	276	((calibrat$4 or synchroniz$4) near4 (phase or timing)) same (command same (sampl$4 or clock$4) same data) same (memory or RAM or DRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:37
S69	4	S68 and (inoperativ$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:37
S70	6	S68 and (operating adj2 point)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:39

S71	0	((DRAM or RAM or SDRAM) adj5 (inoperable or inoperative)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align) near4 (phase or timing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:52
S72	1	((DRAM or RAM or SDRAM) with (inoperable or inoperative)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align) near4 (phase or timing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:52
S73	32	((DRAM or RAM or SDRAM or memory) with (inoperable or inoperative)) and ((DRAM or RAM or SDRAM or memory) same ((calibrat$4 or synchroniz$4 or align) near4 (phase or timing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:53
S74	222	((DRAM or RAM or SDRAM or memory) with (inoperable or inoperative)) and ((DRAM or RAM or SDRAM or memory) same ((calibrat$4 or synchroniz$4 or align) same (read$4 or writ $4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:54
S75	199	S74 not S73	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:54

S76	38	((DRAM or RAM or SDRAM or memory) adj5 (inoperable or inoperative)) and ((DRAM or RAM or SDRAM or memory) same ((calibrat$4 or synchroniz$4 or align) same (read$4 or writ $4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:55
S77	30	S76 not S73	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:55
S78	1035	((DRAM or RAM or SDRAM or memory) adj5 (disabl$5)) and ((DRAM or RAM or SDRAM or memory) same ((calibrat$4 or synchroniz$4 or align) same (read$4 or writ $4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:58
S79	305	((DRAM or RAM or SDRAM) adj5 (disabl $5)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align $4) same (read$4 or writ$4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:58
S80	177	((DRAM or RAM or SDRAM) adj5 (disabl $5)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align $4) with (read$4 or writ$4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 15:59
S81	206	((DRAM or RAM or SDRAM) adj5 (disabl $5)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align $4) same (phase or timing))) and (command same (sampl$4 or clock$4) same data)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 16:03

S82	175	((DRAM or RAM or SDRAM) adj3 (disabl $5)) and ((DRAM or RAM or SDRAM) same ((calibrat$4 or synchroniz$4 or align $4) same (phase or timing))) and (command same (sampl$4 or clock$4) same data)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 16:04
S83	2	"20020078316".pn. and (disabl$4 or operat $4 or inoperative or inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 16:11
S84	1	"20020078316".pn. and (disabl$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/12/06 16:13
S85	1	"20030122696".pn. and (memory adj2 controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/12/06 17:41

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PTO/SB/30EFS (09-08)
Approved for use through 10/31/2008. OMB 0651-0031
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	10716320	Filing Date	2003-11-17	Docket Number (if applicable)	TRAN-P156	Art Unit	2611
First Named Inventor	Guillermo J. Rozas			Examiner Name	Odom, Curtis B.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 504160

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (09-08)
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Signature of Registered U.S. Patent Practitioner			
Signature	/Glenn D. Barnes/	Date (YYYY-MM-DD)	2008-10-23
Name	Glenn D. Barnes	Registration Number	42293

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Rozas, G.	Confirmation: 5239
Serial No.	: 10/716,320	Examiner: Odom, C
Filed:	: 11/17/2003	Group Art Unit: 2611

For : A METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

R.C.E. AND RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the Office Action mailed 07/23/2008, please consider the following amendments and remarks:

IN THE CLAIMS

Please amend the claims as follows:

1. (Previously presented) A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

generating command signals for accessing an integrated circuit component;

accessing data signals for conveying data for the integrated circuit component;

accessing sampling signals for controlling the sampling of the data signals; and

for both data write transactions and data read transactions, automatically adjusting a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, wherein the automatic adjusting is free of user input.

2. (Original) The method of claim 1, wherein the integrated circuit device is a DRAM component.

3. (Original) The method of claim 2, wherein the adjusting of the phase relationship is performed by a memory controller coupled to the DRAM component.

4. (Original) The method of claim 2, wherein the DRAM component is a DDR DRAM component.

5. (Original) The method of claim 4, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

6. (Original) The method of claim 5, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

7. (Previously presented) A system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

a controller for generating command signals for accessing an integrated circuit component;

a delay calibrator integrated within the controller and configured to access data signals conveying data for the integrated circuit device and to access sampling signals for controlling the sampling of the data signals, and for both data write transactions and data read transactions, the delay

calibrator further configured to automatically adjust a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, without requiring a valid initial operating point to exist within the specified operating parameters for the integrated circuit device, and wherein the automatic adjusting is free of user input.

8. (Original) The method of claim 7, wherein the integrated circuit device is a DRAM component.

9. (Original) The method of claim 8, wherein the DRAM component is a DDR DRAM component.

10. (Original) The method of claim 9, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

11. (Original) The method of claim 10, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

12. (Previously presented) In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle

timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

for both data write transactions and data read transactions, automatically altering a phase relationship between the command signals, the data signals, and the sampling signals to determine an operating mode of the DRAM component, without requiring a valid initial operating point to exist within the specified operating parameters for the DRAM component, and wherein the automatic altering is free of user input.

13. (Original) The method of claim 12, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component.

14. (Original) The method of claim 13, further comprising:

configuring the memory controller to operate with the DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

15. (Original) The method of claim 12, wherein the DRAM component is a DDR DRAM component.

16. (Original) The method of claim 15, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

17. (Original) The method of claim 16, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

18. (Previously presented) A computer readable media for finding an operating mode for a DDR DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the media storing computer readable code which when executed by a memory controller causes the memory controller to implement a method comprising:

generating command signals for accessing a DDR DRAM component;

accessing DQ signals for conveying DQ for the DDR DRAM component;

accessing DQS signals for controlling the sampling of the DQ signals; and

for both data write transactions and data read transactions, automatically altering a phase relationship between the command signals, the DQ signals, and the DQS signals to determine an operating mode of the DDR DRAM component, without requiring a valid initial operating point within the specified operating parameters for the DRAM component.

19. (Original) The computer readable media of claim 18, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DDR DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DDR DRAM component.

20. (Original) The computer readable media of claim 19, further comprising:

configuring the memory controller to operate with the DDR DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

21. (Cancelled)

22. (Previously presented) In a memory controller, a method for finding an operating mode for a DDR DRAM component coupled to a PCB (printed circuit board) by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, comprising:

generating command signals for accessing a DDR DRAM component;

accessing data signals for conveying data for the DDR DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

for both data write transactions and data read transactions, automatically altering a phase relationship between the command signals, the data signals, and the sampling signals transmitted via a PCB to determine an operating mode of the DDR DRAM component, wherein the DDR DRAM component is inoperable at specified operating parameters, and wherein said automatic altering is performed free of user input.

23. (New) The computer readable media of claim 22, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find an operating mode of the DDR DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DDR DRAM component.

24. (New) The computer readable media of claim 23, further comprising:

configuring the memory controller to operate with the DDR DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

REMARKS

Claims 1-20 and Claim 22 remain pending. New claims 23 and 24 have been added. Claim 22 is amended. Claims 1-20 and Claim 22 stand rejected under 35 USC Section 103 by the Yang reference in combination with Johnson (US 2003 0122696). Applicant requests reconsideration of the rejections in view of the above claim amendments and the arguments presented below.

35 USC Section 103 Rejections

The above referenced Office Action rejects independent Claims 1, 7, and 12 as being rendered obvious by Yang (US 6,553,472) in view of Johnson (US 2003 0122696). Applicant respectfully traverse.

Applicants respectfully point out that the Examiner has the burden of establishing a prima facie case of obviousness. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the

reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2100-126.

With respect to Claim 1, Claim 1 recites:

> ***
>
> A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:
>
> generating command signals for accessing an integrated circuit component;
>
> accessing data signals for conveying data for the integrated circuit component;
>
> accessing sampling signals for controlling the sampling of the data signals; and
>
> for both data write transactions and data read transactions, automatically adjusting a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, wherein the automatic adjusting is free of user input.
>
> ***

Claim 1 recites the limitation that for both data write transactions and data read transactions, the phase relationship adjusting process is accomplished for the command signals, the data signals, and the sampling signals. The calibration of the intra-cycle timing relationships is executed for both data write transactions and data read transactions. Additionally, the adjusting of the phase relationships between the command signals in the data signals and the sampling signals is executed automatically. The phase relationships are automatically adjusted, and this automatic adjusting is free of user input.

Applicant asserts that these limitations are not shown by the Yang reference. Specifically, the Yang reference requires the initial programming input and based upon that input, calibrates and adjust timing of the device. Applicant reiterates that a process requiring user input, or a process requiring a programmer to set initial parameters of multiple signals for the device is not automatically calibrating as in the claimed invention. Furthermore, independent Claims 1, 7, and 12 specifically recite the automatic adjusting of the claimed invention is free of user input.

Johnson has been added to show automatic adjusting free of user input as in the claimed invention. Applicant traverses by pointing out that Johnson does not disclose the calibration as in the claimed invention. Johnson does not disclose calibrating for both data write transactions and data read transactions. For example, in the cited paragraph 006 of Johnson, the memory controller is explicitly recited as "achieving this time in calibration at system initialization by sending continuous CCLK and DCLK transitions on the clock paths." Paragraph 006 further states "once a synchronization has been achieved, that is, the proper delays on the data receiving paths have been set, the memory controller stop sending the SYNCH pattern and the SLDRAM, after all calibrations are completed, can be used for normal memory READ and WRITE access." Accordingly, Applicant asserts that Yang does not show the calibration for both data write

transactions and data read transactions as in the claimed invention. Similar limitations are included in each of the independent Claims 7, 12, 18, and 22. Additionally, automatic calibrating and automatic adjusting limitations are included in each of the independent Claims 1, 7, 12, 18, and 22.

Accordingly, Yang in combination with Johnson does not show or suggest the claimed invention as recited in independent Claims 1, 7, 12, 18, and 22 and therefore Claims 1-20 and Claim 22 are not rendered obvious by Yang in combination with Johnson within the meaning of 35 USC Section 103.

With respect to independent Claims 12 and 18, the above referenced Office Action rejects independent Claim 18 as being rendered obvious by Yang in view of Johnson and in view of Suzuki (US 2004/0160833). Applicant respectfully traverses.

As described above, Applicant asserts that Yang does not disclose the automatic calibration and the automatic adjusting as in the claimed embodiments of the present invention. The addition of Suzuki does not cure this defect. Suzuki is relied upon for showing a memory controller that controls DDR SDRAM. As with Yang, Suzuki does not show or suggest the automatic calibration and automatic adjusting for both data write

transactions and data read transactions as in the claimed embodiments of the present invention.

Furthermore, applicant points out that Claims 12 and 18 explicitly recites the calibration as taking place without requiring a valid initial operating point within the specified operating parameters for the DRAM component. Applicant points out that the cited section of Yang (e.g., Yang column 2 lines 30-39) does not say anything about inoperative DRAM components. Applicant further point out that the DRAM component as envisioned by Yang must at least be operative to some extent in order to accept and receive the "initialization parameters". There is no disclosure or teaching within Yang of the finding of some parameters within an envelope that can support some functional capability of an otherwise nominally inoperative DRAM component. In contrast, such conditions are explicitly recited as within the capabilities of the present invention.

With respect to independent Claim 22, independent Claim 22 has limitations reciting that for both data write transactions and data read transactions, automatically altering a phase relationship between the command signals, the data signals, and the sampling signals transmitted via a PCB to determine an operating mode of the DRAM component, wherein the

DRAM component is inoperable at specified operating parameters, and wherein said automatic altering is performed free of user input.

Independent Claim 22 explicitly adds the limitation stating that the DRAM component that is being calibrated is inoperable at its specified operating parameters. In other words, even though the DRAM device specified as supposedly being operable within a nominal parameter range, within that range it is in fact inoperable. For both data write transactions and data read transactions, the present invention as in Claim 22 can automatically alter the phase relationships to determine some set of parameters that support an operating mode.

Applicant points out that these limitations are not shown or suggested by the Yang reference. As stated above, applicant points out that the DRAM component as envisioned by Yang must at least be operative to some extent in order to accept and receive the "initialization parameters". There is no disclosure or teaching within Yang of the finding of some parameters within an envelope double offers some functional capability of an otherwise nominally inoperative DRAM component.

CONCLUSION

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
MURABITO, HAO & BARNES

Dated: October 23, 2008

/Glenn Barnes/
Glenn Barnes
Registration No. 42,293

Two North Market Street
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San Jose, CA 95113
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Electronic Patent Application Fee Transmittal

Application Number:	10716320
Filing Date:	17-Nov-2003
Title of Invention:	Method and system for automatically calibrating intra-cycle timing relationships for sampling signals for an integrated circuit device
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Filer:	Glenn D. Barnes/Maronita Isaac
Attorney Docket Number:	TRAN-P156

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	1	52	52
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**862**

Electronic Acknowledgement Receipt

EFS ID:	4168812
Application Number:	10716320
International Application Number:	
Confirmation Number:	5239
Title of Invention:	Method and system for automatically calibrating intra-cycle timing relationships for sampling signals for an integrated circuit device
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	Glenn D. Barnes/Maronita Isaac
Filer Authorized By:	Glenn D. Barnes
Attorney Docket Number:	TRAN-P156
Receipt Date:	23-OCT-2008
Filing Date:	17-NOV-2003
Time Stamp:	20:50:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$862
RAM confirmation Number	6072
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Request for Continued Examination (RCE)	TRAN-P156_RCE_10-23-08.pdf	767975 397f41237cc11465978830820ecf79e4c254c8ce	no	3
Warnings:					
Information:					
2		TRAN-P156_AMDT_10-23-08.pdf	95732 4bf9761f3a089590d66570e363d41b50a1f0cfc0	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment Submitted/Entered with Filing of CPA/RCE	1	1
	Claims	2	9
	Applicant Arguments/Remarks Made in an Amendment	10	16

Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	32138 75ce8e814b71f3a151a62c38109f80a5cf89cb7c	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	895845	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 10/716,320	Filing Date 11/17/2003	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	10/23/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 23	Minus	** 22	= 1	X $ =		OR	X $52=	52
	Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	52

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DEBRA a. SAVOY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/716,320		2611	28M1

OC000000031805037

Correspondence Address/Fee Address Change

The following fields have been set to Customer Number 45590 on 08/27/2008

- **Correspondence Address**
- **Maintenance Fee Address**
- **Power of Attorney Address**

The address of record for Customer Number 45590 is:

45590
TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

7590 07/23/2008

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
ODOM, CURTIS B	
ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
07/23/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	CURTIS B. ODOM	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 4/25/08 have been fully considered but they are not persuasive. Applicant states (see page 10 of the Remarks) **"In contrast, the Yang (U. S. Patent No. 6, 553, 472) reference requires the initial programming input and based upon that input, calibrates and adjust timing of the device. Applicant reiterates that a process requiring user input, or a process requiring a programmer to set initial parameters of multiple signals for the device is not automatically calibrating as in the claimed invention. Furthermore, independent Claims 1, 7, and 12 specifically recite the automatic adjusting of the claimed invention is free of user input."**

However, it is the understanding of the Examiner that even though the initial parameters are set by a user input, the timing (delay) parameters "automatically" adjust based on the initial parameters using the functions/equations as described in Yang, column 5, line 32-column 6, line 19.

The Applicant further states (see page 11 of Remarks) **"Accordingly, Applicant asserts that Yang (or Johnson, US 20030122696) does not show the calibration for both data write transactions and data read transactions as in the claimed invention. Similar limitations are included in each of the independent Claims 7, 12, 18, and 22. Additionally, automatic calibrating and automatic adjusting limitations are included in each of the independent Claims 1, 7, 12, 18, and 22."**

However, Yang et al. discloses calibration (adjustment) of timing relationships (using delays) between signals from the MC to the SDRAM for both read and write operations (see column 5, line 32-column 6, line 19).

The Applicant also states (see page 12 of the Remarks) "**Furthermore, applicant points out that Claims 12 and 18 explicitly recites the calibration as taking place without requiring a valid initial operating point within the specified operating parameters for the DRAM component. Applicant points out that the cited section of Yang (e.g., Yang column 2 lines 30-39) does not say anything about inoperative DRAM components. Applicant further point out that the DRAM component as envisioned by Yang must at least be operative to some extent in order to accept and receive the "initialization parameters". There is no disclosure or teaching within Yang of the finding of some parameters within an envelope that can support some functional capability of an otherwise nominally inoperative DRAM component. In contrast, such conditions are explicitly recited as within the capabilities of the present invention.**"

It is the understanding of the Examiner that claims 12 and 18 recite adjustment (calibration) taking place without requiring a valid initial operating point within a the specified operating parameters. Thus, to the understanding of the Examiner, claims 12 and 18 recite the calibration does not need a specific operating point to begin calibration; the calibration can begin at any operating point within specified parameters. The Examiner would like to point out that these claims do not recite anything about inoperative DRAM components (wherein inoperative DRAM components are recited in claim 22 and properly rejected), rather the claims simply describes an initial operating point for the DRAM is not required. Furthermore, Yang discloses a

valid initial operation point is not required since the controller has the ability to calculate delays and set its own variable initialization point that offers the optimum system performance (see column 2, lines 30-39).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 7, 8, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in Office Action 1/25/2008).

Regarding claim 1, Yang et al. discloses a method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals by implementing programmable time delays (see column 3, lines 10-23) for an integrated circuit device SDRAM), comprising:

generating command signals (see column 3, lines 36-43) for accessing an integrated circuit component;

accessing data signals (see column 3, lines 36-43) for conveying data for the integrated circuit component;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

for both read and write transactions, automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the integrated circuit device.

Yang et al. does not disclose the automatic adjusting is free of user input. However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place at initialization and does not require a user input as described in section 0006. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Regarding claim 2, Yang et al. further discloses the circuit device is an SDRAM (see column 3, lines 10-23).

Regarding claim 3, Yang et al. further discloses adjusting a timing (phase) relationship is performed by a memory controller (Fig. 2, block 31, see column 6, lines 20-25) coupled to the SDRAM.

Regarding claim 7, Yang et al. discloses a system (see Fig. 2) for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals by implementing programmable time delays (see column 3, lines 10-23) for an integrated circuit device SDRAM), comprising:

a controller (Fig. 2, block 31) for generating command signals (see column 3, lines 36-43) for accessing an integrated circuit component;

a delay calibrator of programmable delays (see column 5, line 31-column 6, line 25 and column 8, lines 41-67) integrated within the controller (see column 6, lines 20-25) for accessing data signals (see column 3, lines 36-43) for conveying data for the integrated circuit device and for accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67), for both read and write transactions, the delay calibrator configured to automatically adjust a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19 and column 8, lines 41-67) to calibrate (optimize) operation of the integrated circuit device, wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Yang et al. does not disclose a valid initial operation point that exists within specified operating parameters is not required and wherein the automatic adjusting is free of user input. However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships

between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place at initialization and does not require a valid initial operation point that exists within specified operating parameters or a user input as described in section 0006. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Regarding claim 8, Yang et al. further discloses the circuit device is an SDRAM (see column 3, lines 10-23).

Regarding claim 12, Yang et al. discloses a method for finding an initialization point in a SDRAM (see column 2, lines 30-39) by altering intra-cycle timing relationships between command signals, data signals, and sampling (clock) signals by implementing programmable time delays (see column 3, lines 10-23) for the SDRAM, comprising:

generating command signals (see column 3, lines 36-43) for accessing the SDRAM;

accessing data signals (see column 3, lines 36-43) for conveying data for the SDRAM;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

for both read and write transactions, automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the DRAM

and find an optimal initialization point (see column 2, lines 30-39), wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Yang et al. does not disclose a valid initial operation point that exists within specified operating parameters is not required and wherein the automatic adjusting is free of user input. However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place at initialization and does not require a valid initial operation point that exists within specified operating parameters or a user input as described in section 0006. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

4. Claims 4-6, 9-11, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in Office Action 1/25/2008) as applied to claims 2, 8, and 12, and in further view of Suzuki (previously cited in Office Action 1/8/2007).

Regarding claims 4-6, 9-11, and 15-17, Yang et al. and Johnson et al. do not specifically disclose the calibrated SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to enable both reading and writing for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al. and Johnson et al. with the DDR SDRAM of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

Regarding claim 18, Yang et al. and Johnson et al. disclose all the limitations of claim 18 (see rejection of claim 12), including the operations of the SDRAM written as software (see Yang et al., column 2, lines 11-16). Yang et al. and Johnson et al. do not specifically disclose the calibrated SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to determine both reading and writing operations for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al. and Johnson et al. with the DDR SDRAM (and DQ and DQS signals for control of the DDR SDRAM) of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

5. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in

Office Action 1/25/2008) as applied to claim 12, and in further in view of Keeth (previously cited in Office Action 1/8/2007).

Regarding claims 13 and 14, Yang et al. discloses configuring the memory controller to operate with the DRAM in accordance with an optimal operating mode (see column 6, lines 20-25). Yang et al and Johnson et al. do not disclose the time delay operation involves performing a coarse time delay calibration by altering the timing relationship in accordance with a large step interval to find the operating mode of the DRAM component; and performing a fine time delay calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component, wherein the optimal operating mode is determined by the fine calibration.

However, Keeth discloses a memory device (see Fig. 1) including a memory controller (see Fig. 1, block 22) coupled to a DRAM (Fig. 1, block 26), wherein minimum and maximum delays from command at the memory controller to read data an the memory controller are accommodated by performing vernier clock adjustments, wherein there is a coarse delay adjustment with a large bit interval and a fine delay adjustment with a smaller interval (within a bit period (see column 4, lines 11-18 and column 7, lines 44-51). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the timing delays of Yang et al. and Johnson et al. with the coarse and fine delay as disclosed by Keeth since Keeth states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, liens 46-55).

6. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in

Office Action 1/25/2008) in view of Suzuki (previously cited in Office Action 1/8/2007) as applied to claim 18, and in further view of Keeth (previously cited in Office Action 1/8/2007).

Regarding claims 19 and 20 (see above rejection of claim 18), Yang et al. discloses configuring the memory controller to operate with the DRAM in accordance with an optimal operating mode (see column 6, lines 20-25). Yang et al., Johnson et al., and Suzuki do not disclose the time delay operation involves performing a coarse time delay calibration by altering the timing relationship in accordance with a large step interval to find the operating mode of the DRAM component; and performing a fine time delay calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component, wherein the optimal operating mode is determined by the fine calibration.

However, Keeth discloses a memory device (see Fig. 1) including a memory controller (see Fig. 1, block 22) coupled to a DRAM (Fig. 1, block 26), wherein minimum and maximum delays from command at the memory controller to read data an the memory controller are accommodated by performing vernier clock adjustments, wherein there is a coarse delay adjustment with a large bit interval and a fine delay adjustment with a smaller interval (within a bit period (see column 4, lines 11-18 and column 7, lines 44-51). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the timing delays of Yang et al., Johnson et al., and Suzuki with the coarse and fine delay as disclosed by Keeth since Keeth states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, liens 46-55).

7. Claims 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Davis (previously cited in Office Action 1/8/2007), and in further view of Johnson et al. (previously cited in Office Action 1/25/2008).

Regarding claim 12, Yang et al. discloses in a memory controller, a method for finding an initialization (operating) point in a SDRAM (see column 2, lines 30-39) coupled to a memory controller of a microprocessor chip which represents a printed circuit board (see column 1, lines 19-25) by altering intra-cycle timing relationships between command signals, data signals, and sampling (clock) signals by implementing programmable time delays (see column 3, lines 10-23) for the SDRAM, comprising:

generating command signals (see column 3, lines 36-43) for accessing the SDRAM;

accessing data signals (see column 3, lines 36-43) for conveying data for the SDRAM;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

for both read and write transactions, automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the DRAM and find an optimal initialization point (see column 2, lines 30-39), wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Yang et al. does not specifically disclose the DRAM component is inoperable at specified initial operating parameters, wherein the automatic altering is performed free of user input.

However, as described above, Yang et al. discloses the memory controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39). Davis further discloses operating points for the DRAM control and data signals wherein the DRAM produces invalid data (or is inoperable), see column 2, lines 30-49). Therefore, it would have been obvious to set an initialization point in Yang et al. when the DRAM produces invalid data as described by Davis since Yang et al. states calculating delays and setting an initialization point offers the optimum system performance (see column 2, lines 30-39).

Johnson et al. further discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place at initialization and does not require a user input as described in section 0006. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. and Davis with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CURTIS B. ODOM whose telephone number is (571)272-3046. The examiner can normally be reached on Monday- Friday, 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Curtis B. Odom/
Primary Examiner, Art Unit 2611
July 20, 2008

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	CURTIS B. ODOM	2611	

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	CURTIS B. ODOM	2611	

SEARCHED			
Class	Subclass	Date	Examiner
UPDATED		7/20/2008	CBO

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
UPDATED	7/20/2008	CBO

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10716320	ROZAS, GUILLERMO J.
	Examiner	Art Unit
	CURTIS B ODOM	2611

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/20/2008								
	1	=								
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BIB DATA SHEET

CONFIRMATION NO. 5239

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/716,320	11/17/2003	398	2611	TRAN-P156

APPLICANTS

Guillermo J. Rozas, Los Gatos, CA;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

02/17/2004

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /CURTIS B ODOM/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	5	22	6

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TITLE

Method and system for automatically calibrating intra-cycle timing relationships for sampling signals for an integrated circuit device

FILING FEE RECEIVED		
1614	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	7	(714/767-773.ccls. or 375/354.ccls. or 371-376.ccls.) and (phase with (sampl$4 with (command or instruct $4) with (data or information)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:11
S2	13	((synchroniz$4 or align $4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40
S3	7	((adjust$4) near3 phase) same (sampl$4 adj2 signals) same ((command or instruct $4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:19
S4	1	((calibrat$4) near3 (phase or timing)) same (sampl$4 adj2 signals) same ((command or instruct $4 or address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S5	0	((synchroniz$4 or align $4) near3 phase) with (sampl$4 adj2 signals) with ((address) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S6	1	((synchroniz$4 or align $4) near3 phase) same (sampl$4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21

S7	3	"DRAM" same (sampl $4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21
S8	3	"DRAM" same (sampl $4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:23
S9	3	"DRAM" same (sampl $4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S10	325	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S11	66	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) same (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S12	2749	365/194.ccls. or 365/233.ccls. and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 10:47

S13	1453	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S14	318	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05
S15	13	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:13
S16	2	S15 and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:54
S17	1267	("DQ" and "DQS") same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:55
S18	13	S17 and ((phase or timing) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S19	10	S17 and ((delay$4) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:10

S20	47	S17 and ((phase or timing) same ((command or address) adj1 signals) same ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S21	11	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:18
S22	14	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S23	70	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S24	70	((phase or timing or synchroniz44) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22

S25	77	((phase or timing or synchroniz$4) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22
S26	965	S13 and "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S27	20	S26 and fine and coarse	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S28	1612	((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:08
S29	35	S28 and (fine same coarse)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:09
S30	0	Rozas.in. and ((synchroniz$4 or align $4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40
S31	0	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" near3 inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05

S32	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
S33	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
S34	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing or synchroniz44) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S35	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with (inoperable or inoperative))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:26
S36	3	(memory adj1 controller) same "DRAM" same coarse same fine	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:28
S37	10	((memory adj1 controller) same "DRAM") and ((memory adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:29

S38	11	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:45
S39	126	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) and (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:38
S40	87	(((memory or DRAM) adj1 controller) same "DRAM") and ((memory or DRAM) adj1 controller) and (coarse same fine same (address or command or data or clock))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:49
S41	1	"6016282".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S42	1	"6115318".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:44
S43	1	"6115318".pn. and (coarse same fine) and (coarse and fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S44	1	"6016282".pn. and (coarse same fine) and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S45	2	"6553472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/09/04 03:37
S46	2	"6553472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:50
S47	274	phase same (command same sampl $4 same data) same (adjust$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:52
S48	432	((adjust$4 or chang $4) with (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:53

S49	302	((adjust$4 or chang$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:54
S50	245	((adjust$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:54
S51	47	((calibrat$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:09
S52	1	((calibrat$4) near4 (phase or timing)) same (command adj1 signals) same (data adj1 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:10
S53	3	"20030131160".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:11
S54	3	"20030131160".pn. and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:12
S55	2	"20030131160".pn. and (sampl$4 same calibrat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:12
S56	1	"20030131160".pn. and (sampl$4 same calibrat$4) and (calibrat$4 same data same command)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:13
S57	2	"20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:35
S58	2	"20030122696".pn. and calibrat$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:36
S59	1	"20030122696".pn. and calibrat$4 and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:36

S60	2	"6553473".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/07/20 13:40
S61	4	"6553473".pn. or "20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/07/20 13:41
S62	4	"6553472".pn. or "20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/07/20 13:41

7/20/08 2:52:05 PM
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Rozas, G.	Confirmation: 5239
Serial No.	: 10/716,320	Examiner: Odom, C
Filed:	: 11/17/2003	Group Art Unit: 2611

For : A METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the Office Action mailed 01/25/2008, please consider the following amendments and remarks:

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

generating command signals for accessing an integrated circuit component;

accessing data signals for conveying data for the integrated circuit component;

accessing sampling signals for controlling the sampling of the data signals; and

for both data write transactions and data read transactions, automatically adjusting a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, wherein the automatic adjusting is free of user input.

2. (Original) The method of claim 1, wherein the integrated circuit device is a DRAM component.

3. (Original) The method of claim 2, wherein the adjusting of the phase relationship is performed by a memory controller coupled to the DRAM component.

4. (Original) The method of claim 2, wherein the DRAM component is a DDR DRAM component.

5. (Original) The method of claim 4, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

6. (Original) The method of claim 5, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

7. (Currently amended) A system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

a controller for generating command signals for accessing an integrated circuit component;

a delay calibrator integrated within the controller and configured to access data signals conveying data for the integrated circuit device and to access sampling signals for controlling the sampling of the data signals~~,~~, and for both data write transactions and data read transactions, the delay

calibrator further configured to automatically adjust a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, without requiring a valid initial operating point to exist within the specified operating parameters for the integrated circuit device, and wherein the automatic adjusting is free of user input.

8. (Original) The method of claim 7, wherein the integrated circuit device is a DRAM component.

9. (Original) The method of claim 8, wherein the DRAM component is a DDR DRAM component.

10. (Original) The method of claim 9, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

11. (Original) The method of claim 10, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

12. (Currently amended) In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing

relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

for both data write transactions and data read transactions, automatically altering a phase relationship between the command signals, the data signals, and the sampling signals to determine an operating mode of the DRAM component, without requiring a valid initial operating point to exist within the specified operating parameters for the DRAM component, and wherein the automatic altering is free of user input.

13. (Original) The method of claim 12, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component.

14. (Original) The method of claim 13, further comprising:

configuring the memory controller to operate with the DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

15. (Original) The method of claim 12, wherein the DRAM component is a DDR DRAM component.

16. (Original) The method of claim 15, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

17. (Original) The method of claim 16, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

18. (Currently amended) A computer readable media for finding an operating mode for a DDR DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the media storing computer readable code which when executed by a memory controller causes the memory controller to implement a method comprising:

generating command signals for accessing a DDR DRAM component;

accessing DQ signals for conveying DQ for the DDR DRAM component;

accessing DQS signals for controlling the sampling of the DQ signals; and

for both data write transactions and data read transactions,

automatically altering a phase relationship between the command signals, the DQ signals, and the DQS signals to determine an operating mode of the DDR DRAM component, without requiring a valid initial operating point within the specified operating parameters for the DRAM component.

19. (Original) The computer readable media of claim 18, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DDR DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DDR DRAM component.

20. (Original) The computer readable media of claim 19, further comprising:

configuring the memory controller to operate with the DDR DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

21. (Cancelled)

22. (Currently amended) In a memory controller, a method for finding an operating mode for a DRAM component coupled to a PCB (printed circuit board) by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

<u>for both data write transactions and data read transactions,</u> automatically altering a phase relationship between the command signals, the data signals, and the sampling signals transmitted via a PCB to determine an operating mode of the DRAM component, wherein the DRAM component is inoperable at specified operating parameters, and wherein said automatic altering is performed free of user input.

REMARKS

Claims 1-20 and Claim 22 stand newly rejected under 35 USC Section 103 by the previously cited Yang reference in combination with the new reference Johnson (US 2003 0122696). Applicant requests reconsideration of the rejections in view of the above claim amendments and the arguments presented below.

35 USC Section 103 Rejections

The above referenced Office Action rejects independent Claims 1, 7, and 12 as being rendered obvious by Yang (US 6,553,472) in view of Johnson (US 2003 0122696). Applicant respectfully traverse.

With respect to Claim 1, Claim 1 has been amended to recite:

***

A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

generating command signals for accessing an integrated circuit component;

accessing data signals for conveying data for the integrated circuit component;

accessing sampling signals for controlling the sampling of the data signals; and

for both data write transactions and data read transactions, automatically adjusting a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, wherein the automatic adjusting is free of user input.

***

As recited in Claim 1, for both data write transactions and data read transactions, the phase relationship adjusting process is accomplished for both data write transactions and data read transactions. The calibration of the intra-cycle timing relationships is executed for both data write transactions and data read transactions. Additionally, the adjusting of the phase relationships between the command signals in the data signals and the sampling signals is executed automatically. The phase relationships are automatically adjusted.

In contrast, the Yang reference requires the initial programming input and based upon that input, calibrates and adjust timing of the device. Applicant reiterates that a process requiring user input, or a process requiring a programmer to set initial parameters of multiple signals for the device is not automatically calibrating as in the claimed invention. Furthermore, independent Claims 1, 7, and 12 specifically recite the automatic adjusting of the claimed invention is free of user input.

The above referenced Office Action adds Johnson to show automatic adjusting free of user input as in the claimed invention. Applicant traverses by pointing out that Johnson does not disclose the calibration as in the claimed invention. Johnson does not disclose calibrating for both data write transactions and data read transactions. For example, in the cited paragraph

006 of Johnson, the memory controller is explicitly recited as "achieving this time in calibration at system initialization by sending continuous CCLK and DCLK transitions on the clock paths." Paragraph 006 further states "once a synchronization has been achieved, that is, the proper delays on the data receiving paths have been set, the memory controller stop sending the SYNCH pattern and the SLDRAM, after all calibrations are completed, can be used for normal memory READ and WRITE access." Accordingly, Applicant asserts that Yang does not show the calibration for both data write transactions and data read transactions as in the claimed invention. Similar limitations are included in each of the independent Claims 7, 12, 18, and 22. Additionally, automatic calibrating and automatic adjusting limitations are included in each of the independent Claims 1, 7, 12, 18, and 22.

Accordingly, Yang in combination with Johnson does not show or suggest the claimed invention as recited in independent Claims 1, 7, 12, 18, and 22 and therefore Claims 1-20 and Claim 22 are not rendered obvious by Yang in combination with Johnson within the meaning of 35 USC Section 103.

With respect to independent Claims 12 and 18, the above referenced Office Action rejects independent Claim 18 as being rendered obvious by

Yang in view of Johnson and in view of Suzuki (US 2004/0160833). Applicant respectfully traverses.

As described above, Applicant asserts that Yang does not disclose the automatic calibration and the automatic adjusting as in the claimed embodiments of the present invention. The addition of Suzuki does not cure this defect. Suzuki is relied upon for showing a memory controller that controls DDR SDRAM. As with Yang, Suzuki does not show or suggest the automatic calibration and automatic adjusting for both data write transactions and data read transactions as in the claimed embodiments of the present invention.

Furthermore, applicant points out that Claims 12 and 18 explicitly recites the calibration as taking place without requiring a valid initial operating point within the specified operating parameters for the DRAM component. Applicant points out that the cited section of Yang (e.g., Yang column 2 lines 30-39) does not say anything about inoperative DRAM components. Applicant further point out that the DRAM component as envisioned by Yang must at least be operative to some extent in order to accept and receive the "initialization parameters". There is no disclosure or teaching within Yang of the finding of some parameters within an envelope that can support some functional capability of an otherwise nominally

inoperative DRAM component. In contrast, such conditions are explicitly recited as within the capabilities of the present invention.

With respect to independent Claim 22, independent Claim 22 has limitations reciting that for both data write transactions and data read transactions, automatically altering a phase relationship between the command signals, the data signals, and the sampling signals transmitted via a PCB to determine an operating mode of the DRAM component, wherein the DRAM component is inoperable at specified operating parameters, and wherein said automatic altering is performed free of user input.

Independent Claim 22 explicitly adds the limitation stating that the DRAM component that is being calibrated is inoperable at its specified operating parameters. In other words, even though the DRAM device specified as supposedly being operable within a nominal parameter range, within that range it is in fact inoperable. For both data write transactions and data read transactions, the present invention as in Claim 22 can automatically alter the phase relationships to determine some set of parameters that support an operating mode.

Applicant points out that these limitations are not shown or suggested by the Yang reference. As stated above, applicant points out that the DRAM

component as envisioned by Yang must at least be operative to some extent in order to accept and receive the "initialization parameters". There is no disclosure or teaching within Yang of the finding of some parameters within an envelope double offers some functional capability of an otherwise nominally inoperative DRAM component.

CONCLUSION

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
WAGNER, MURABITO & HAO

Dated: April 25, 2008

/Glenn Barnes/
Glenn Barnes
Registration No. 42,293

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060

Electronic Acknowledgement Receipt

EFS ID:	3213863
Application Number:	10716320
International Application Number:	
Confirmation Number:	5239
Title of Invention:	Method and system for automatically calibrating intra-cycle timing relationships for sampling signals for an integrated circuit device
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Correspondence Address:	WAGNER, MURABITO & HAO LLP - Third Floor Two North Market Street San Jose CA 95113 US 4089389060 -
Filer:	Glenn D. Barnes
Filer Authorized By:	
Attorney Docket Number:	TRAN-P156
Receipt Date:	25-APR-2008
Filing Date:	17-NOV-2003
Time Stamp:	19:54:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		TRAN-P0156_NonFinalOA_4-25-08.pdf	90122 1ade3fce245118f1ea9d98fb0169a5e55e12c13a	yes	15

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Amendment - After Non-Final Rejection	1	1
Claims	2	8
Applicant Arguments/Remarks Made in an Amendment	9	15

Warnings:	
Information:	
Total Files Size (in bytes):	90122

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/716,320	11/17/2003	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
FOR	NUMBER FILED	NUMBER EXTRA					
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	04/25/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 21	Minus	** 22	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $ =		OR	X $210=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/STELLA LITTLE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

7590 01/25/2008

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
ODOM, CURTIS B	
ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
01/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	Curtis B. Odom	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments regarding claims 13 and 19 have been fully considered but they are not persuasive. Applicant states (see page 13 of the Remarks) **"The cited section of the Keeth reference (e.g., Keeth col. 4 lines 11-18 and col. 7 lines 44-51) describes the adjustment of a variety of vernier circuits within each DRAM to implement the timing adjustment. There is no description of any coarse versus fine calibration. Additionally, the vernier circuits are adjusted within the DRAMs, not the memory controller as in the claimed invention."** First, claims 13 and 19 do not recite the coarse and fine calibration takes place within the memory controller. Furthermore, Keeth (U. S. Patent No. 6, 115, 318) discloses coarse and fine clock calibration for the operation of the clock of the DRAM in column 4, lines 11-18.

2. Applicant's arguments with respect to claims 1-12, 14-18, 20, and 22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 7, 8, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (US 20030122696).

Regarding claim 1, Yang et al. discloses a method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals by implementing programmable time delays (see column 3, lines 10-23) for an integrated circuit device SDRAM), comprising:

generating command signals (see column 3, lines 36-43) for accessing an integrated circuit component;

accessing data signals (see column 3, lines 36-43) for conveying data for the integrated circuit component;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the integrated circuit device.

Yang et al. does not disclose the automatic adjusting is free of user input. However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and

data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place at initialization and does not require a user input as described in section 0006. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Regarding claim 2, Yang et al. further discloses the circuit device is an SDRAM (see column 3, lines 10-23).

Regarding claim 3, Yang et al. further discloses adjusting a timing (phase) relationship is performed by a memory controller (Fig. 2, block 31, see column 6, lines 20-25) coupled to the SDRAM.

Regarding claim 7, Yang et al. discloses a system (see Fig. 2) for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals by implementing programmable time delays (see column 3, lines 10-23) for an integrated circuit device SDRAM), comprising:

a controller (Fig. 2, block 31) for generating command signals (see column 3, lines 36-43) for accessing an integrated circuit component;

a delay calibrator of programmable delays (see column 5, line 31-column 6, line 25 and column 8, lines 41-67) integrated within the controller (see column 6, lines 20-25) for accessing data signals (see column 3, lines 36-43) for conveying data for the integrated circuit device and for accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of

the data signals based on the rising edge of the clock signal (see column 3, lines 48-67), the delay calibrator configured to automatically adjust a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19 and column 8, lines 41-67) to calibrate (optimize) operation of the integrated circuit device, wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Yang et al. does not disclose a valid initial operation point that exists within specified operating parameters is not required and wherein the automatic adjusting is free of user input. However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place at initialization and does not require a valid initial operation point that exists within specified operating parameters or a user input as described in section 0006. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Regarding claim 8, Yang et al. further discloses the circuit device is an SDRAM (see column 3, lines 10-23).

Regarding claim 12, Yang et al. discloses a method for finding an initialization point in a SDRAM (see column 2, lines 30-39) by altering intra-cycle timing relationships between command signals, data signals, and sampling (clock) signals by implementing programmable time delays (see column 3, lines 10-23) for the SDRAM, comprising:

generating command signals (see column 3, lines 36-43) for accessing the SDRAM;

accessing data signals (see column 3, lines 36-43) for conveying data for the SDRAM;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the DRAM and find an optimal initialization point (see column 2, lines 30-39), wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Yang et al. does not disclose a valid initial operation point that exists within specified operating parameters is not required and wherein the automatic adjusting is free of user input. However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place at initialization and does not require a valid initial

operation point that exists within specified operating parameters or a user input as described in section 0006. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

5. Claims 4-6, 9-11, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (US 20030122696) as applied to claims 2, 8, and 12, and in further view of Suzuki (previously cited in Office Action 1/8/2007).

Regarding claims 4-6, 9-11, and 15-17, Yang et al. and Johnson et al. do not specifically disclose the calibrated SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to enable both reading and writing for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al. and Johnson et al. with the DDR SDRAM of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

Regarding claim 18, Yang et al. and Johnson et al. disclose all the limitations of claim 18 (see rejection of claim 12), including the operations of the SDRAM written as software (see Yang et al., column 2, lines 11-16). Yang et al. and Johnson et al. do not specifically disclose

the calibrated SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to determine both reading and writing operations for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al. and Johnson et al. with the DDR SDRAM (and DQ and DQS signals for control of the DDR SDRAM) of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

6. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (US 20030122696) as applied to claim 12, and in further in view of Keeth (previously cited in Office Action 1/8/2007).

Regarding claims 13 and 14, Yang et al. discloses configuring the memory controller to operate with the DRAM in accordance with an optimal operating mode (see column 6, lines 20-25). Yang et al and Johnson et al. do not disclose the time delay operation involves performing a coarse time delay calibration by altering the timing relationship in accordance with a large step interval to find the operating mode of the DRAM component; and performing a fine time delay calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component, wherein the optimal operating mode is determined by the fine calibration.

However, Keeth discloses a memory device (see Fig. 1) including a memory controller (see Fig. 1, block 22) coupled to a DRAM (Fig. 1, block 26), wherein minimum and maximum delays from command at the memory controller to read data an the memory controller are accommodated by performing vernier clock adjustments, wherein there is a coarse delay adjustment with a large bit interval and a fine delay adjustment with a smaller interval (within a bit period (see column 4, lines 11-18 and column 7, lines 44-51). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the timing delays of Yang et al. and Johnson et al. with the coarse and fine delay as disclosed by Keeth since Keeth states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, liens 46-55).

7. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (US 200301222696) in view of Suzuki (previously cited in Office Action 1/8/2007) as applied to claim 18, and in further view of Keeth (previously cited in Office Action 1/8/2007).

Regarding claims 19 and 20 (see above rejection of claim 18), Yang et al. discloses configuring the memory controller to operate with the DRAM in accordance with an optimal operating mode (see column 6, lines 20-25). Yang et al., Johnson et al., and Suzuki do not disclose the time delay operation involves performing a coarse time delay calibration by altering the timing relationship in accordance with a large step interval to find the operating mode of the DRAM component; and performing a fine time delay calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component, wherein the optimal operating mode is determined by the fine calibration.

However, Keeth discloses a memory device (see Fig. 1) including a memory controller (see Fig. 1, block 22) coupled to a DRAM (Fig. 1, block 26), wherein minimum and maximum delays from command at the memory controller to read data an the memory controller are accommodated by performing vernier clock adjustments, wherein there is a coarse delay adjustment with a large bit interval and a fine delay adjustment with a smaller interval (within a bit period (see column 4, lines 11-18 and column 7, lines 44-51). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the timing delays of Yang et al., Johnson et al., and Suzuki with the coarse and fine delay as disclosed by Keeth since Keeth states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, liens 46-55).

8. Claims 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Davis (previously cited in Office Action 1/8/2007), and in further view of Johnson et al. (US 200301222696).

Regarding claim 12, Yang et al. discloses in a memory controller, a method for finding an initialization (operating) point in a SDRAM (see column 2, lines 30-39) coupled to a memory controller of a microprocessor chip which represents a printed circuit board (see column 1, lines 19-25) by altering intra-cycle timing relationships between command signals, data signals, and sampling (clock) signals by implementing programmable time delays (see column 3, lines 10-23) for the SDRAM, comprising:

generating command signals (see column 3, lines 36-43) for accessing the SDRAM;

accessing data signals (see column 3, lines 36-43) for conveying data for the SDRAM;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the DRAM and find an optimal initialization point (see column 2, lines 30-39), wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Yang et al. does not specifically disclose the DRAM component is inoperable at specified initial operating parameters, wherein the automatic altering is performed free of user input.

However, as described above, Yang et al. discloses the memory controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39). Davis further discloses operating points for the DRAM control and data signals wherein the DRAM produces invalid data (or is inoperable), see column 2, lines 30-49). Therefore, it would have been obvious to set an initialization point in Yang et al. when the DRAM produces invalid data as described by Davis since Yang et al. states calculating delays and setting an initialization point offers the optimum system performance (see column 2, lines 30-39).

Johnson et al. further discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships

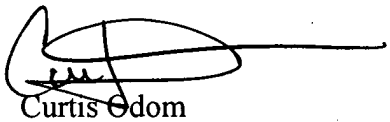
between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place at initialization and does not require a user input as described in section 0006. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. and Davis with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Curtis Odom
January 21, 2008

Notice of References Cited	Application/Control No. 10/716,320	Applicant(s)/Patent Under Reexamination ROZAS, GUILLERMO J.	
	Examiner Curtis B. Odom	Art Unit 2611	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0122696	07-2003	Johnson et al.	341/120
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Bib Data Sheet

CONFIRMATION NO. 5239

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/716,320	11/17/2003 RULE	375	2611	TRAN-P156

APPLICANTS
Guillermo J. Rozas, Los Gatos, CA;

** CONTINUING DATA **********
N/A CO

** FOREIGN APPLICATIONS **********
N/A CO

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 02/17/2004

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☐ no 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance Verified and Acknowledged _____ Examiner's Signature Initials	CA	5	22	6

ADDRESS
WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA95113

TITLE
Method and system for automatically calibrating intra-cycle timing relationships for sampling signals for an integrated circuit device

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1194	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/716,320	ROZAS, GUILLERMO J.
Examiner	**Art Unit**
Curtis B. Odom	2611

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Claim		Date								
Final	Original	1/21/08								
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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	Curtis B. Odom	2611	

SEARCHED			
Class	Subclass	Date	Examiner
UPDATED		1/21/2008	CBO

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
UPDATED	1/21/2008	CBO

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	7	(714/767-773.ccls. or 375/354.ccls. or 371-376.ccls.) and (phase with (sampl$4 with (command or instruct$4) with (data or information)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:11
S2	13	((synchroniz$4 or align$4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40
S3	7	((adjust$4) near3 phase) same (sampl$4 adj2 signals) same ((command or instruct$4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:19
S4	1	((calibrat$4) near3 (phase or timing)) same (sampl$4 adj2 signals) same ((command or instruct$4 or address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S5	0	((synchroniz$4 or align$4) near3 phase) with (sampl$4 adj2 signals) with ((address) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S6	1	((synchroniz$4 or align$4) near3 phase) same (sampl$4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21
S7	3	"DRAM" same (sampl$4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21
S8	3	"DRAM" same (sampl$4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:23
S9	3	"DRAM" same (sampl$4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25

EAST Search History

S10	325	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S11	66	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) same (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S12	2749	365/194.ccls. or 365/233.ccls. and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 10:47
S13	1453	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S14	318	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05
S15	13	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:13
S16	2	S15 and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:54
S17	1267	("DQ" and "DQS") same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:55
S18	13	S17 and ((phase or timing) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S19	10	S17 and ((delay$4) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:10

EAST Search History

S20	47	S17 and ((phase or timing) same ((command or address) adj1 signals) same ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S21	11	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:18
S22	14	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S23	70	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S24	70	((phase or timing or synchroniz44) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22
S25	77	((phase or timing or synchroniz$4) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22
S26	965	S13 and "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S27	20	S26 and fine and coarse	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S28	1612	((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:08

EAST Search History

S29	35	S28 and (fine same coarse)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:09
S30	0	Rozas.in. and ((synchroniz$4 or align$4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40
S31	0	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" near3 inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05
S32	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
S33	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
S34	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing or synchroniz44) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S35	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with (inoperable or inoperative))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:26
S36	3	(memory adj1 controller) same "DRAM" same coarse same fine	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:28
S37	10	((memory adj1 controller) same "DRAM") and ((memory adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:29

EAST Search History

S38	11	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:45
S39	126	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) and (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:38
S40	87	(((memory or DRAM) adj1 controller) same "DRAM") and ((memory or DRAM) adj1 controller) and (coarse same fine same (address or command or data or clock))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:49
S41	1	"6016282".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S42	1	"6115318".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:44
S43	1	"6115318".pn. and (coarse same fine) and (coarse and fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S44	1	"6016282".pn. and (coarse same fine) and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S45	2	"6553472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/09/04 03:37
S46	2	"6553472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:50
S47	274	phase same (command same sampl$4 same data) same (adjust$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:52
S48	432	((adjust$4 or chang$4) with (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:53

EAST Search History

S49	302	((adjust$4 or chang$4)near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:54
S50	245	((adjust$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 16:54
S51	47	((calibrat$4) near4 (phase or timing)) same (command same (sampl$4 or clock) same data) same memory	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:09
S52	1	((calibrat$4) near4 (phase or timing)) same (command adj1 signals) same (data adj1 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:10
S53	3	"20030131160".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:11
S54	3	"20030131160".pn. and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:12
S55	2	"20030131160".pn. and (sampl$4 same calibrat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:12
S56	1	"20030131160".pn. and (sampl$4 same calibrat$4) and (calibrat$4 same data same command)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2008/01/21 17:13
S57	2	"20030122696".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:35
S58	2	"20030122696".pn. and calibrat$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:36
S59	1	"20030122696".pn. and calibrat$4 and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2008/01/21 17:36

10-31-07

RCE



Docket Number: TRAN-P156

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

I hereby certify that this transmittal of the below described documents is being deposited with the United States Postal Service in an envelope bearing Express Mail Postage and an Express Mail label, with the below serial number, addressed to the Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450, on the below date of deposit.			
Express Mail Label No.:	EM118684918US	Name of Person Making the Deposit:	Anthony Chou
Date of Deposit:	10/29/07	Signature of the Person Making the Deposit:	Anthony Chou

In re Application of: Guillermo J. Rozas

Application No.: 10/716,320 Examiner: Odom, C.

Filed: 11/17/03 Art Unit: 2611

Confirmation No.: 5239

For: A METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL (SUBSECTION(B) OF 35 U.S.C. § 132)

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 for the above-identified application.

1. Submission required under a filing under 37 C.F.R. § 1.114

   a. [ ] Previously submitted

   i. [ ] Consider the amendment(s)/ reply under 37 C.F.R. § 1.116 previously filed on _____
   (Any unentered amendment(s) referred to above will be entered)

   ii. [ ] Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

   iii. [ ] Other _____

   b. [**X**] Enclosed

   i. [**X**] Amendment/Reply

   ii. [ ] Affidavit(s)/Declaration(s)

   iii. [ ] Information Disclosure Statement (IDS)

   iv. [ ] Other _____

2. Miscellaneous

11/01/2007 ATRINH 00000037 10716320
01 FC:1801 810.00 OP
02 FC:1201 420.00 OP

a. [ ] Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months.
(period of suspension shall not exceed 3 months: Fee under 37 C.F.R. § 1.17(l) required)

b. Other _____

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [ ] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
[ ] one month	$120.00
[ ] two months	$460.00
[ ] three months	$1,050.00
[ ] four months	$1,640.00

Fee $ _____

If an additional extension of time is required, please consider this a petition therefor.

(b) [X] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

FEES DUE

The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

CLAIMS					
	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEES
Basic Application Fee					$810.00
Total Claims	21	Minus 22=	0	X $50 =	$0.00
Independent Claims	5	Minus 3=	2	X $210 =	$420.00
If multiple dependent claims are presented, add $360.00					$0.00
TOTAL APPLICATION FEE DUE					$1,230.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[**X**] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 50-4160 .

A duplicate copy of this authorization is enclosed.

[**X**] A check in the amount of $1,230.00

[ ] A check in the amount of $_____

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 50-4160.

Please direct all correspondence concerning the above-identified application to the following address:

MURABITO HAO & BARNES LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 45590

Respectfully submitted,

Date: 10/29/07

By: _____
Glenn D. Barnes
Reg. No. 42,293

OIPE
OCT 3 0 2007
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Rozas, G.	Confirmation: 5239
Serial No.	: 10/716,320	Examiner: Odom, C
Filed:	: 11/17/2003	Group Art Unit: 2611

For : A METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

R.C.E. AND RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the Office Action mailed 09/06/2007, please consider the following amendments and remarks:

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

generating command signals for accessing an integrated circuit component;

accessing data signals for conveying data for the integrated circuit component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically adjusting a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, wherein the automatic adjusting is free of user input.

2. (Original) The method of claim 1, wherein the integrated circuit device is a DRAM component.

3. (Original) The method of claim 2, wherein the adjusting of the phase relationship is performed by a memory controller coupled to the DRAM component.

4. (Original) The method of claim 2, wherein the DRAM component is a DDR DRAM component.

5. (Original) The method of claim 4, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

6. (Original) The method of claim 5, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

7. (Currently amended) A system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

a controller for generating command signals for accessing an integrated circuit component;

a delay calibrator integrated within the controller and configured to access data signals conveying data for the integrated circuit device and to access sampling signals for controlling the sampling of the data signals, the delay calibrator further configured to automatically adjust a phase

relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, without requiring a valid initial operating point to exist within the specified operating parameters for the integrated circuit device, and wherein the automatic adjusting is free of user input.

8. (Original) The method of claim 7, wherein the integrated circuit device is a DRAM component.

9. (Original) The method of claim 8, wherein the DRAM component is a DDR DRAM component.

10. (Original) The method of claim 9, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

11. (Original) The method of claim 10, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

12. (Currently amended) In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically altering a phase relationship between the command signals, the data signals, and the sampling signals to determine an operating mode of the DRAM component, without requiring a valid initial operating point to exist within the specified operating parameters for the DRAM component, and wherein the automatic altering is free of user input. .

13. (Original) The method of claim 12, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a lar who ge step interval to find the operating mode of the DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component.

14. (Original) The method of claim 13, further comprising:

configuring the memory controller to operate with the DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

15. (Original) The method of claim 12, wherein the DRAM component is a DDR DRAM component.

16. (Original) The method of claim 15, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

17. (Original) The method of claim 16, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

18. (Currently amended) A computer readable media for finding an operating mode for a DDR DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the media storing computer readable code which when executed by a memory controller causes the memory controller to implement a method comprising:

generating command signals for accessing a DDR DRAM component;

accessing DQ signals for conveying DQ for the DDR DRAM component;

accessing DQS signals for controlling the sampling of the DQ signals; and

automatically altering a phase relationship between the command signals, the DQ signals, and the DQS signals to determine an operating mode

of the DDR DRAM component, without requiring a valid initial operating point within the specified operating parameters for the DRAM component.

19. (Original) The computer readable media of claim 18, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DDR DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DDR DRAM component.

20. (Original) The computer readable media of claim 19, further comprising:

configuring the memory controller to operate with the DDR DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

21. (Cancelled)

22. (Currently amended) In a memory controller, a method for finding an operating mode for a DRAM component coupled to a PCB (printed circuit

board) by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically altering a phase relationship between the command signals, the data signals, and the sampling signals transmitted via a PCB to determine an operating mode of the DRAM component, wherein the DRAM component is inoperable at ~~a specified initial operating point~~ specified operating parameters, and wherein said automatic altering is performed free of user input.

REMARKS

35 USC Section 102 Rejections

The above referenced Office Action rejects independent Claims 1-3, and 7-23 as being anticipated by Yang (US 6,553,472). Applicants respectfully traverse.

In the "response to argument" section of the above referenced Office Action, it is stated that the cited Yang reference discloses programmer input and that the memory controller of Yang calibrates and adjusts intra-cycle timing relationships based upon the programmer input. It is further stated that the device of the Yang reference requires the initial programming input and based upon that input, calibrates and adjust timing of the device. Applicants respond by reiterating that a process requiring user input, or a process requiring a programmer to set initial parameters of multiple signals for the device is not automatically calibrating as in the claimed invention. Accordingly, to further distinguish over the teaching of the Yang reference, Applicant have amended independent Claims 1, 7, and 12 to specifically recite the automatic adjusting of the claimed invention is free of user input.

Accordingly, Claim 1 has been amended to recite a method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device.

The method includes generating command signals for accessing an integrated circuit component, accessing data signals for conveying data for the integrated circuit component, accessing sampling signals for controlling the sampling of the data signals, and automatically adjusting a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device. Applicant points out that the claimed embodiments recite automatic calibration of the cycle timing relationships. Applicants further point out that the automatic adjusting is free of user input. The automatic calibration can be performed by, for example, the memory controller.

In contrast, the Yang reference would not be operable without the programming of its inputs. Yang discloses a method for programming clock delays, command delays, read command parameter delays, and write command parameter delays of a memory controller. Yang does not disclose the automatic calibration and the automatic adjusting as in the claimed embodiments of the present invention. For example, at col. 4 at line 25-34, Yang states that the "...programmable parameters for the MC required for correct and optimum I/O operation with the MC and SDRAM need to be specified. Table 2 lists and describes seventeen related programmable parameters in the MC. Other programmable parameters, such as refresh control and SDRAM initialization parameters are not listed. These timing

parameters are necessary for I/O operations such as memory read, memory write, same bank access, different bank access, etc."

Automatic calibrating and automatic adjusting limitations are included in each of the independent claims of the present application. Applicant asserts that Yang describes programming memory controller to operate at the desired point. This is different from automatically calibrating and automatically adjusting, which does not require any programmer input. Furthermore, independent Claims 1, 7 and 12 have also been amended to especially recite that the automatic adjusting is free of user input.

With respect to Claim 12, independent Claim 12 recites a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, by automatically altering a phase relationship between the command signals, the data signals, and the sampling signals to determine an operating mode of the DRAM component, without requiring a valid initial operating point to exist within the specified operating parameters for the DRAM component. There is no teaching or suggestion of any situation within Yang for dealing with a case where the DRAM component is not operable within the specified parameters. As pointed out in the response to argument of the above referenced Office Action,

the Yang reference requires operation within the specified parameters that are input by the user/programmer. Yang would not know how to operate with and "out of spec" DRAM component.

Accordingly, Yang does not show or suggest the claimed invention as recited in independent Claims 1-22 and therefore Claims 1-22 are not anticipated by Yang within the meaning of 35 USC Section 102.

35 USC Section 103 Rejections

The above referenced Office Action rejects Claims 4-6, 9-11, 13-22, and as being rendered obvious by Yang in view of Suzuki (US 2004/0160833), Keeth (US 6016282) and Davis (US 5781766). Applicants respectfully traverse.

As described above, Applicant asserts that Yang does not disclose the automatic calibration and the automatic adjusting as in the claimed embodiments of the present invention. The addition of Suzuki does not cure this defect. Suzuki is relied upon for showing a memory controller that controls DDR SDRAM. As with Yang, Suzuki does not show or suggest the automatic calibration and automatic adjusting as in the claimed embodiments of the present invention.

Accordingly, Applicants assert that the claimed invention as recited in Claims 1-22 is not shown or suggested by the combination of Yang and Suzuki, and therefore, Claims 1-22 are not rendered obvious by the Yang and Suzuki combination within the meaning of 35 USC Section 103.

With respect to dependent Claims 13 and 19, additional limitations are added that recite performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DRAM component, and performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component. The cited section of the Keeth reference (e.g., Keeth col. 4 lines 11-18 and col. 7 lines 44-51) describes the adjustment of a variety of vernier circuits within each DRAM to implement the timing adjustment. There is no description of any coarse versus fine calibration. Additionally, the vernier circuits are adjusted within the DRAMs, not the memory controller as in the claimed invention. Applicant point out that this is in addition to the fact that the DRAM component may not have a valid initial operating point within the specified operating parameters. The cited references do not mention scenarios for handling functionally dead or "out of spec" DRAM components.

With respect to dependent Claims 14 and 20, further limitations are added describing the configuring of the memory controller to operate with the DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration. As described above, there is no description of any coarse versus fine calibration in the cited references. The added limitations further describing the fine calibration further distinguish over the cited references.

With respect to Claim 18, Claim 18 recites a computer readable media for finding an operating mode for a DDR DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, and automatically altering a phase relationship between the command signals, the DQ signals, and the DQS signals to determine an operating mode of the DDR DRAM component, without requiring a valid initial operating point within the specified operating parameters for the DRAM component. There is no teaching or suggestion of any situation within Yang or Suzuki for dealing with a case where the DRAM component is not operable within the specified parameters. As pointed out in the response to argument of the above referenced Office Action, the Yang reference requires operation within the specified parameters that are input by the user/programmer. Yang would not know how to operate with and "out of spec" DRAM component.

Respect to independent Claim 22, Claim 22 recites a method performed by a memory controller comprising automatically altering a phase relationship between the command signals, the data signals, and the sampling signals transmitted via a PCB to determine an operating mode of the DRAM component, wherein the DRAM component is inoperable at specified operating parameters, and wherein said automatic altering is performed free of user input. For the rationale described above, Yang and Davis do not show automatic calibration free of user input. Additionally, with respect to the Davis reference, the cited section of Davis (e.g., col. 2 lines 30-40) does not show any automatic establishment of an operating mode when the DRAM component is inoperable within its operating parameters.

CONCLUSION

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
WAGNER, MURABITO & HAO

Dated: 10/29, 2007

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PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 10/716,320	Filing Date 11/17/2003	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	10/30/2007	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 21	Minus	** 22	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 5	Minus	***6	= 0	X $ =		OR	X $210=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
LaShawn Marks

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

7590 09/06/2007

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
ODOM, CURTIS B	
ART UNIT	**PAPER NUMBER**
2611	
MAIL DATE	**DELIVERY MODE**
09/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	Curtis B. Odom	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 6/11/2007 have been fully considered but they are not persuasive. Applicant states (see page 10 of the Remarks) **"Automatic calibrating and automatic adjusting limitations are included in each of the independent claims of the present application. Applicant asserts that Yang (U. S. Patent No. 6, 553, 472) describes programming memory controller to operate at the desired point. This is different from automatically calibrating and automatically adjusting, which does not require any programmer input. Accordingly, Yang does not show or suggest the claimed invention as recited in independent Claims 1-22 and therefore Claims 1-22 are not anticipated by Yang within the meaning of 35 USC Section 102.**

While Yang may disclose a programmer input, it is the understanding of the Examiner that the memory controller (see Fig. 2, block 31) in fact does automatically calibrate and automatically adjust intra-cycle timing relationships based on the user input. It is the memory controller which "automatically" generates commands to control timing in the device (see column 6, lines 39-51). Yang further discloses calculating timing parameters for the device (see column 11, lines 38-58), wherein the calculated parameters are stored, and based on the memory bandwidth and margins, the set of parameters is chosen from memory which give the best performance based on the memory and the margins. Therefore, it is the understanding of the Examiner that the device requires an initial user input, however, it is the memory controller

which automatically calibrates and adjusts the timing of the device using commands based on the user input. Therefore, despite the programmer input, it is the understanding of the Examiner that Yang does in fact disclose automatic adjusting and calibration.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 7, 8, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Yang et al. (previously cited in Office Action 1/8/2007).

Regarding claim 1, Yang et al. discloses a method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals by implementing programmable time delays (see column 3, lines 10-23) for an integrated circuit device SDRAM), comprising:

generating command signals (see column 3, lines 36-43) for accessing an integrated circuit component;

accessing data signals (see column 3, lines 36-43) for conveying data for the integrated circuit component;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the integrated circuit device.

Regarding claim 2, Yang et al. further discloses the circuit device is an SDRAM (see column 3, lines 10-23).

Regarding claim 3, Yang et al. further discloses adjusting a timing (phase) relationship is performed by a memory controller (Fig. 2, block 31, see column 6, liens 20-25) coupled to the SDRAM.

Regarding claim 7, Yang et al. discloses a system (see Fig. 2) for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals by implementing programmable time delays (see column 3, lines 10-23) for an integrated circuit device SDRAM), comprising:

a controller (Fig. 2, block 31) for generating command signals (see column 3, lines 36-43) for accessing an integrated circuit component;

a delay calibrator of programmable delays (see column 5, line 31-column 6, line 25 and column 8, lines 41-67) integrated within the controller (see column 6, lines 20-25) for accessing data signals (see column 3, lines 36-43) for conveying data for the integrated circuit device and for accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of

the data signals based on the rising edge of the clock signal (see column 3, lines 48-67), the delay calibrator configured to automatically adjust a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19 and column 8, lines 41-67) to calibrate (optimize) operation of the integrated circuit device, wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Regarding claim 8, Yang et al. further discloses the circuit device is an SDRAM (see column 3, lines 10-23).

Regarding claim 12, Yang et al. discloses a method for finding an initialization point in a SDRAM (see column 2, lines 30-39) by altering intra-cycle timing relationships between command signals, data signals, and sampling (clock) signals by implementing programmable time delays (see column 3, lines 10-23) for the SDRAM, comprising:

generating command signals (see column 3, lines 36-43) for accessing the SDRAM;

accessing data signals (see column 3, lines 36-43) for conveying data for the SDRAM;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-

column 6, line 19) to calibrate (optimize) operation of the DRAM and find an optimal initialization point (see column 2, lines 30-39), wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-6, 9-11, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) as applied to claims 2, 8, and 12, in view of Suzuki (previously cited in Office Action 1/8/2007).

Regarding claims 4-6, 9-11, and 15-17, Yang et al. does not disclose the SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to enable both reading and writing for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al. with

the DDR SDRAM of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

Regarding claim 18, Yang et al. discloses all the limitations of claim 18 (see rejection of claim 12), including the operations of the SDRAM written as software (see column 2, lines 11-16). Yang et al. does not disclose the SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to determine both reading and writing operations for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al. with the DDR SDRAM (and DQ and DQS signals for control of the DDR SDRAM) of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

6. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) as applied to claim 12, in view of Keeth (previously cited in Office Action 1/8/2007).

Regarding claims 13 and 14, Yang et al. discloses configuring the memory controller to operate with the DRAM in accordance with an optimal operating mode (see column 6, lines 20-25). Yang et al. does not disclose the time delay operation involves performing a coarse time delay calibration by altering the timing relationship in accordance with a large step interval to find the operating mode of the DRAM component; and performing a fine time delay calibration

by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component, wherein the optimal operating mode is determined by the fine calibration.

However, Keeth discloses a memory device (see Fig. 1) including a memory controller (see Fig. 1, block 22) coupled to a DRAM (Fig. 1, block 26), wherein minimum and maximum delays from command at the memory controller to read data an the memory controller are accommodated by performing vernier clock adjustments, wherein there is a coarse delay adjustment with a large bit interval and a fine delay adjustment with a smaller interval (within a bit period (see column 4, lines 11-18 and column 7, lines 44-51). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the timing delays of Yang et al. with the coarse and fine delay as disclosed by Keeth since Keeth states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, liens 46-55).

7. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Suzuki (previously cited in Office Action 1/8/2007) as applied to claim 18, and in further view of Keeth (previously cited in Office Action 1/8/2007).

Regarding claims 19 and 20 (see above rejection of claim 18), Yang et al. discloses configuring the memory controller to operate with the DRAM in accordance with an optimal operating mode (see column 6, lines 20-25). Yang et al. and Suzuki do not disclose the time delay operation involves performing a coarse time delay calibration by altering the timing relationship in accordance with a large step interval to find the operating mode of the DRAM

component; and performing a fine time delay calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component, wherein the optimal operating mode is determined by the fine calibration.

However, Keeth discloses a memory device (see Fig. 1) including a memory controller (see Fig. 1, block 22) coupled to a DRAM (Fig. 1, block 26), wherein minimum and maximum delays from command at the memory controller to read data an the memory controller are accommodated by performing vernier clock adjustments, wherein there is a coarse delay adjustment with a large bit interval and a fine delay adjustment with a smaller interval (within a bit period (see column 4, lines 11-18 and column 7, lines 44-51). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the timing delays of Yang et al. and Suzuki with the coarse and fine delay as disclosed by Keeth since Keeth states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, liens 46-55).

8. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Davis (previously cited in Office Action 1/8/2007).

Regarding claim 21, Yang et al. discloses a method for finding an initialization (operating) point in a SDRAM (see column 2, lines 30-39) by altering intra-cycle timing relationships between command signals, data signals, and sampling (clock) signals by implementing programmable time delays (see column 3, lines 10-23) for the SDRAM, comprising:

generating command signals (see column 3, lines 36-43) for accessing the SDRAM;

accessing data signals (see column 3, lines 36-43) for conveying data for the SDRAM;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the DRAM and find an optimal initialization (operating) point (see column 2, lines 30-39), wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Yang et al. does not specifically disclose the DRAM component is inoperable at specified initial operating points.

However, as described above, Yang et al. discloses the memory controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39). Davis further discloses operating points for the DRAM control and data signals wherein the DRAM produces invalid data (or is inoperable), see column 2, lines 30-49). Therefore, it would have been obvious to set an initialization point in Yang et al. when the DRAM produces invalid data as described by Davis since Yang et al. states calculating delays and setting an initialization point offers the optimum system performance (see column 2, lines 30-39).

Regarding claim 22, the claim method includes features corresponding the above rejection of claim 21, wherein Yang et al. also discloses the SDRAM coupled to a memory controller of a microprocessor chip which represents a printed circuit board (see column 1, lines 19-25).

Conclusion

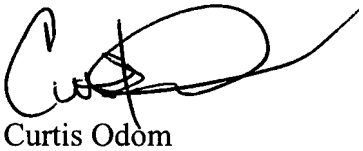
9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Curtis Odom
September 4, 2007

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Bib Data Sheet

CONFIRMATION NO. 5239

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/716,320	11/17/2003 RULE	375	2611	TRAN-P156

APPLICANTS

Guillermo J. Rozas, Los Gatos, CA;

** CONTINUING DATA **********

N/A CO

** FOREIGN APPLICATIONS **********

N/A CO

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 02/17/2004

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☐ no	CA	5	22	6

35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance

Verified and Acknowledged _____ Examiner's Signature Initials

ADDRESS

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA95113

TITLE

Method and system for automatically calibrating intra-cycle timing relationships for sampling signals for an integrated circuit device

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1194	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/716,320	ROZAS, GUILLERMO J.
Examiner	**Art Unit**
Curtis B. Odom	2611

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	9/4/07
	1	√
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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination
10/716,320	ROZAS, GUILLERMO J.
Examiner	**Art Unit**
Curtis B. Odom	2611

SEARCHED			
Class	Subclass	Date	Examiner
UPDATED		9/4/2007	CBO

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
UPDATED	9/4/2007	CBO

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"6553472".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/09/04 03:37
S1	7	(714/767-773.ccls. or 375/354.ccls. or 371-376.ccls.) and (phase with (sampl$4 with (command or instruct$4) with (data or information)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:11
S2	13	((synchroniz$4 or align$4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40
S3	7	((adjust$4) near3 phase) same (sampl$4 adj2 signals) same ((command or instruct$4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:19
S4	1	((calibrat$4) near3 (phase or timing)) same (sampl$4 adj2 signals) same ((command or instruct$4 or address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S5	0	((synchroniz$4 or align$4) near3 phase) with (sampl$4 adj2 signals) with ((address) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S6	1	((synchroniz$4 or align$4) near3 phase) same (sampl$4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21
S7	3	"DRAM" same (sampl$4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21
S8	3	"DRAM" same (sampl$4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:23
S9	3	"DRAM" same (sampl$4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25

EAST Search History

S10	325	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S11	66	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) same (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S12	2749	365/194.ccls. or 365/233.ccls. and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 10:47
S13	1453	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S14	318	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05
S15	13	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:13
S16	2	S15 and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:54
S17	1267	("DQ" and "DQS") same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:55
S18	13	S17 and ((phase or timing) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S19	10	S17 and ((delay$4) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:10
S20	47	S17 and ((phase or timing) same ((command or address) adj1 signals) same ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11

EAST Search History

S21	11	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:18
S22	14	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S23	70	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S24	70	((phase or timing or synchroniz44) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22
S25	77	((phase or timing or synchroniz$4) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22
S26	965	S13 and "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S27	20	S26 and fine and coarse	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S28	1612	((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:08
S29	35	S28 and (fine same coarse)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:09
S30	0	Rozas.in. and ((synchroniz$4 or align$4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40

EAST Search History

S31	0	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" near3 inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05
S32	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
S33	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
S34	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing or synchroniz44) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S35	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with (inoperable or inoperative))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:26
S36	3	(memory adj1 controller) same "DRAM" same coarse same fine	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:28
S37	10	((memory adj1 controller) same "DRAM") and ((memory adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:29
S38	11	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:45
S39	126	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) and (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:38
S40	87	(((memory or DRAM) adj1 controller) same "DRAM") and ((memory or DRAM) adj1 controller) and (coarse same fine same (address or command or data or clock))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:49

EAST Search History

S41	1	"6016282".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S42	1	"6115318".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:47
S43	1	"6115318".pn. and (coarse same fine) and (coarse and fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S44	1	"6016282".pn. and (coarse same fine) and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50

OIPE IAP76
JUN 11 2007
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Rozas, G.	Confirmation: 5239
Serial No.	: 10/716,320	Examiner: Odom, C
Filed:	: 11/17/2003	Group Art Unit: 2611

For : A METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the Office Action mailed 01/08/2007, please consider the following amendments and remarks:

IN THE CLAIMS

Please amend the claims as follows:

1. (Original) A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

generating command signals for accessing an integrated circuit component;

accessing data signals for conveying data for the integrated circuit component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically adjusting a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device.

2. (Original) The method of claim 1, wherein the integrated circuit device is a DRAM component.

3. (Original) The method of claim 2, wherein the adjusting of the phase relationship is performed by a memory controller coupled to the DRAM component.

4. (Original) The method of claim 2, wherein the DRAM component is a DDR DRAM component.

5. (Original) The method of claim 4, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

6. (Original) The method of claim 5, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

7. (Original) A system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

a controller for generating command signals for accessing an integrated circuit component;

a delay calibrator integrated within the controller and configured to access data signals conveying data for the integrated circuit device and to access sampling signals for controlling the sampling of the data signals, the delay calibrator further configured to automatically adjust a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device,

without requiring a valid initial operating point for the integrated circuit device.

8. (Original) The method of claim 7, wherein the integrated circuit device is a DRAM component.

9. (Original) The method of claim 8, wherein the DRAM component is a DDR DRAM component.

10. (Original) The method of claim 9, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

11. (Original) The method of claim 10, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

12. (Original) In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically altering a phase relationship between the command signals, the data signals, and the sampling signals to determine an operating mode of the DRAM component, without requiring a valid initial operating point for the DRAM component.

13. (Original) The method of claim 12, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component.

14. (Original) The method of claim 13, further comprising:

configuring the memory controller to operate with the DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

15. (Original) The method of claim 12, wherein the DRAM component is a DDR DRAM component.

16. (Original) The method of claim 15, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

17. (Original) The method of claim 16, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

18. (Original) A computer readable media for finding an operating mode for a DDR DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the media storing computer readable code which when executed by a memory controller causes the memory controller to implement a method comprising:

generating command signals for accessing a DDR DRAM component;

accessing DQ signals for conveying DQ for the DDR DRAM component;

accessing DQS signals for controlling the sampling of the DQ signals; and

automatically altering a phase relationship between the command signals, the DQ signals, and the DQS signals to determine an operating mode of the DDR DRAM component, without requiring a valid initial operating point for the DRAM component.

19. (Original) The computer readable media of claim 18, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DDR DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DDR DRAM component.

20. (Original) The computer readable media of claim 19, further comprising:

configuring the memory controller to operate with the DDR DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

21. (Currently Amended) In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically altering a phase relationship between the command signals, the data signals, and the sampling signals to determine an operating mode of the DRAM component, wherein the DRAM component is inoperable at a specified initial operating point.

22. (Original) In a memory controller, a method for finding an operating mode for a DRAM component coupled to a PCB (printed circuit board) by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically altering a phase relationship between the command signals, the data signals, and the sampling signals transmitted via a PCB to determine an operating mode of the DRAM component, wherein the DRAM component is inoperable at a specified initial operating point.

REMARKS

35 USC Section 102 Rejections

The above referenced Office Action rejects independent Claims 1-3, and 7-23 as being anticipated by Yang (US 6,553,472). Applicants respectfully traverse.

With respect to independent Claim1, Claim 1 recites a method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device. The method includes generating command signals for accessing an integrated circuit component, accessing data signals for conveying data for the integrated circuit component, accessing sampling signals for controlling the sampling of the data signals, and automatically adjusting a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device. Applicant points out that the claimed embodiments recite automatic calibration of the cycle timing relationships. The automatic calibration can be performed by, for example, a memory controller.

In contrast, Yang discloses a method for programming clock delays, command delays, read command parameter delays, and write command parameter delays of a memory controller. Yang does not disclose the

automatic calibration and the automatic adjusting as in the claimed embodiments of the present invention. For example, at col. 4 at line 25-34, Yang states that the "...programmable parameters for the MC required for correct and optimum I/O operation with the MC and SDRAM need to be specified. Table 2 lists and describes seventeen related programmable parameters in the MC. Other programmable parameters, such as refresh control and SDRAM initialization parameters are not listed. These timing parameters are necessary for I/O operations such as memory read, memory write, same bank access, different bank access, etc." Applicant points out that this is not automatic calibration and automatic adjustment as in the claimed invention.

Automatic calibrating and automatic adjusting limitations are included in each of the independent claims of the present application. Applicant asserts that Yang describes programming memory controller to operate at the desired point. This is different from automatically calibrating and automatically adjusting, which does not require any programmer input. Accordingly, Yang does not show or suggest the claimed invention as recited in independent Claims 1-22 and therefore Claims 1-22 are not anticipated by Yang within the meaning of 35 USC Section 102.

35 USC Section 103 Rejections

The above referenced Office Action rejects Claims 4-6, 9-11, and 15-18 as being rendered obvious by Yang in view of Suzuki (US 2004/0160833). Applicants respectfully traverse.

As above, Applicant asserts that Yang does not disclose the automatic calibration and the automatic adjusting as in the claimed embodiments of the present invention. The addition of Suzuki does not cure this defect. Suzuki is relied upon for showing a memory controller that controls DDR SDRAM. As with Yang, Suzuki does not show or suggest the automatic calibration and automatic adjusting as in the claimed embodiments of the present invention.

Accordingly, Applicants assert that the claimed invention as recited in Claims 1-22 is not shown or suggested by the combination of Yang and Suzuki, and therefore, Claims 1-22 are not rendered obvious by the Yang and Suzuki combination within the meaning of 35 USC Section 103.

CONCLUSION

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
WAGNER, MURABITO & HAO

Dated: 6/8, 2007

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OIPE IAP76
JUN 11 2007
PATENT & TRADEMARK OFFICE

Attorney Docket No.: TRAN-P156

DTW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.

Date of Deposit:	06/08/07	Name of Person Making the Deposit:	Julie Giaramita	Signature of the Person Making the Deposit:	Julie Giaramita

In re Application of: Guillermo J. Rozas

Application No.: 10/716,320 Examiner: Odom, C.

Filed: 11/17/03 Art Unit: 2611

Confirmation No.: 5239

For: A METHOD AND SYSTEM FOR AUTOMATIC CALIBRATING INTRA-CYCLE TIMING RELATIONSHIP FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application

X Transmitted herewith is a response to an office action for the above identified patent application. (12 sheets)
____ Transmitted herewith are ____ sheets of substitute formal drawings.
____ Other:

2. Applicant is other than a small entity

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [X] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
[ ] one month	$120.00
[X] two months	$450.00
[ ] three months	$1,020.00
[ ] four months	$1,590.00
[ ] five months	$2,160.00
	Fee $450.00

If an additional extension of time is required, please consider this a petition therefor.

(b) [ ] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

06/12/2007 CCHAU1 00000016 504160 10716320

01 FC:1252 450.00 DA

rev. 10/04 kgr

Fee Calculation

4. The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

(for other than a small entity)					
Fee Items	Claims Remaining After Amendment	Highest Number of Claims Previously Paid For	Present Extra Claims	Fee Rate	Total
Total Claims	22	- 22 =	0	x $50.00	$0.00
Independent Claims	3	- 3 =	0	x $200.00	$0.00
Multiple Dependent Claim Fee (one or more, first added by this amendment)				$360.00	$0.00
Total Fees					$0.00

PAYMENT OF FEES

5. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 50-4160 . A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $

[X] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 50-4160.

Please direct all correspondence concerning the above-identified application to the following address:

MURABITO HAO & BARNES LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 45594

Respectfully submitted,

Date: 6/8/07

By: _____
Glenn D. Barnes
Reg. No. 42,293

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/716,320	11/17/2003	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	06/11/2007	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 6	Minus	***6	= 0	X $ =		OR	X $200=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
CORALIA -. BETANCOURT

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

7590 01/08/2007

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
ODOM, CURTIS B	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	Curtis B. Odom	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2-6 and 7-23 are objected to because of the following informalities:

a. In claims 2-6 and 7-23, the acronyms (DRAM, DDR, DQ, and DQS) are suggested to be defined.

b. In claim 21, the phrase "DRAM component inoperable" is suggested to be changed to "DRAM component is inoperable".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 7, 8, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Yang et al. (U. S. Patent No. 6, 553, 472).

Regarding claim 1, Yang et al. discloses a method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals by

implementing programmable time delays (see column 3, lines 10-23) for an integrated circuit device SDRAM), comprising:

generating command signals (see column 3, lines 36-43) for accessing an integrated circuit component;

accessing data signals (see column 3, lines 36-43) for conveying data for the integrated circuit component;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the integrated circuit device.

Regarding claim 2, Yang et al. further discloses the circuit device is an SDRAM (see column 3, lines 10-23).

Regarding claim 3, Yang et al. further discloses adjusting a timing (phase) relationship is performed by a memory controller (Fig. 2, block 31, see column 6, liens 20-25) coupled to the SDRAM.

Regarding claim 7, Yang et al. discloses a system (see Fig. 2) for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals by implementing programmable time delays (see column 3, lines 10-23) for an integrated circuit device SDRAM), comprising:

a controller (Fig. 2, block 31) for generating command signals (see column 3, lines 36-43) for accessing an integrated circuit component;

a delay calibrator of programmable delays (see column 5, line 31-column 6, line 25 and column 8, lines 41-67) integrated within the controller (see column 6, lines 20-25) for accessing data signals (see column 3, lines 36-43) for conveying data for the integrated circuit device and for accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67), the delay calibrator configured to automatically adjust a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19 and column 8, lines 41-67) to calibrate (optimize) operation of the integrated circuit device, wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Regarding claim 8, Yang et al. further discloses the circuit device is an SDRAM (see column 3, lines 10-23).

Regarding claim 12, Yang et al. discloses a method for finding an initialization point in a SDRAM (see column 2, lines 30-39) by altering intra-cycle timing relationships between command signals, data signals, and sampling (clock) signals by implementing programmable time delays (see column 3, lines 10-23) for the SDRAM, comprising:

generating command signals (see column 3, lines 36-43) for accessing the SDRAM;

accessing data signals (see column 3, lines 36-43) for conveying data for the SDRAM;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the DRAM and find an optimal initialization point (see column 2, lines 30-39), wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-6, 9-11, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (U.S. Patent No. 6, 553, 472) as applied to claims 2, 8, and 12, in view of Suzuki (US 2004/0160833).

Regarding claims 4-6, 9-11, and 15-17, Yang et al. does not disclose the SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to enable both reading and writing for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al. with the DDR SDRAM of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

Regarding claim 18, Yang et al. discloses all the limitations of claim 18 (see rejection of claim 12), including the operations of the SDRAM written as software (see column 2, lines 11-16). Yang et al. does not disclose the SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to determine both reading and writing operations for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al. with the DDR SDRAM (and DQ and DQS signals for control of the DDR SDRAM) of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

6. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (U.S. Patent No. 6, 553, 472) as applied to claim 12, in view of Keeth (U. S. Patent No. 6, 016, 282).

Regarding claims 13 and 14, Yang et al. discloses configuring the memory controller to operate with the DRAM in accordance with an optimal operating mode (see column 6, lines 20-25). Yang et al. does not disclose the time delay operation involves performing a coarse time delay calibration by altering the timing relationship in accordance with a large step interval to find the operating mode of the DRAM component; and performing a fine time delay calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component, wherein the optimal operating mode is determined by the fine calibration.

However, Keeth discloses a memory device (see Fig. 1) including a memory controller (see Fig. 1, block 22) coupled to a DRAM (Fig. 1, block 26), wherein minimum and maximum delays from command at the memory controller to read data an the memory controller are accommodated by performing vernier clock adjustments, wherein there is a coarse delay adjustment with a large bit interval and a fine delay adjustment with a smaller interval (within a bit period (see column 4, lines 11-18 and column 7, lines 44-51). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the timing delays of Yang et al. with the coarse and fine delay as disclosed by Keeth since Keeth states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, liens 46-55).

7. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (U.S. Patent No. 6, 553, 472) in view of Suzuki (US 2004/0160833) as applied to claim 18, and in further view of Keeth (U. S. Patent No. 6, 016, 282).

Regarding claims 19 and 20 (see above rejection of claim 18), Yang et al. discloses configuring the memory controller to operate with the DRAM in accordance with an optimal operating mode (see column 6, lines 20-25). Yang et al. and Suzuki do not disclose the time delay operation involves performing a coarse time delay calibration by altering the timing relationship in accordance with a large step interval to find the operating mode of the DRAM component; and performing a fine time delay calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component, wherein the optimal operating mode is determined by the fine calibration.

However, Keeth discloses a memory device (see Fig. 1) including a memory controller (see Fig. 1, block 22) coupled to a DRAM (Fig. 1, block 26), wherein minimum and maximum delays from command at the memory controller to read data an the memory controller are accommodated by performing vernier clock adjustments, wherein there is a coarse delay adjustment with a large bit interval and a fine delay adjustment with a smaller interval (within a bit period (see column 4, lines 11-18 and column 7, lines 44-51). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the timing delays of Yang et al. and Suzuki with the coarse and fine delay as disclosed by Keeth since Keeth states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, liens 46-55).

8. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (U.S. Patent No. 6, 553, 472) in view of Davis (U. S. Patent No. 5, 781, 766).

Regarding claim 21, Yang et al. discloses a method for finding an initialization (operating) point in a SDRAM (see column 2, lines 30-39) by altering intra-cycle timing relationships between command signals, data signals, and sampling (clock) signals by implementing programmable time delays (see column 3, lines 10-23) for the SDRAM, comprising:

generating command signals (see column 3, lines 36-43) for accessing the SDRAM;

accessing data signals (see column 3, lines 36-43) for conveying data for the SDRAM;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the DRAM and find an optimal initialization (operating) point (see column 2, lines 30-39), wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Yang et al. does not specifically disclose the DRAM component is inoperable at specified initial operating points.

However, as described above, Yang et al. discloses the memory controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39). Davis further discloses operating points for the DRAM control and data signals wherein the DRAM produces invalid data (or is inoperable), see column 2, lines 30-49). Therefore, it would have been obvious to set an initialization point in Yang et al. when the DRAM produces invalid data as described by Davis since Yang et al. states calculating delays and setting an initialization point offers the optimum system performance (see column 2, lines 30-39).

Regarding claim 22, the claim method includes features corresponding the above rejection of claim 21, wherein Yang et al. also discloses the SDRAM coupled to a memory controller of a microprocessor chip which represents a printed circuit board (see column 1, lines 19-25).

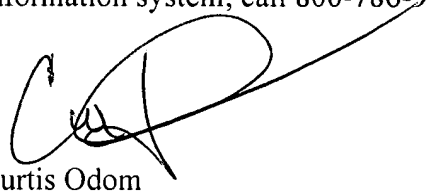
Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Matsui (U. S. Patent No. 2003/0231543) discloses a memory controller for controlling a DRAM. Keeth et al. (U. S. 6, 101, 197) discloses coarse and fine delay tuning for signals in an integrated circuit including a memory controller and DRAMs.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Curtis Odom
January 3, 2007

Notice of References Cited	Application/Control No. 10/716,320	Applicant(s)/Patent Under Reexamination ROZAS, GUILLERMO J.	
	Examiner Curtis B. Odom	Art Unit 2611	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,553,472	04-2003	Yang et al.	711/167
*	B	US-6,016,282	01-2000	Keeth, Brent	365/233
*	C	US-5,781,766	07-1998	Davis, Ian E.	713/401
*	D	US-2004/0160833	08-2004	Suzuki, Takanobu	365/194
*	E	US-6,101,197	08-2000	Keeth et al.	370/517
*	F	US-2003/0231543	12-2003	Matsui, Yoshinori	365/233
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Bib Data Sheet

CONFIRMATION NO. 5239

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/716,320	11/17/2003 RULE	375	2611	TRAN-P156

APPLICANTS

Guillermo J. Rozas, Los Gatos, CA;

** CONTINUING DATA **********

N/A CO

** FOREIGN APPLICATIONS **********

N/A CO

IF REQUIRED, FOREIGN FILING LICENSE GRANTED

** 02/17/2004

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☐ no 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance Verified and Acknowledged _____ Examiner's Signature Initials	CA	5	22	6

ADDRESS

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA95113

TITLE

Method and system for automatically calibrating intra-cycle timing relationships for sampling signals for an integrated circuit device

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1194	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/716,320	ROZAS, GUILLERMO J.
Examiner	**Art Unit**
Curtis B. Odom	2611

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	1/3/07
	1	√
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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination
10/716,320	ROZAS, GUILLERMO J.
Examiner	**Art Unit**
Curtis B. Odom	2611

SEARCHED			
Class	Subclass	Date	Examiner
375	371-376 354	1/2/2007	CBO
714	767-773	1/2/2007	CBO
365	194,233	1/3/2007	CBO

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST: USPAT; USPGPUB; EPO; JPO; DERWENT	1/2/2007	CBO
INVENTOR SEARCH	1/3/2007	CBO

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" near3 inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05
L2	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM") and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
L3	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:06
L4	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing or synchroniz44) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with inoperable)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
L5	2	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) and ("DRAM" with (inoperable or inoperative))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:26
L6	3	(memory adj1 controller) same "DRAM" same coarse same fine	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:28
L7	10	((memory adj1 controller) same "DRAM") and ((memory adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:29
L8	11	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) same (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:45
L9	126	(((memory or DRAM) adj1 controller) same "DRAM") and (((memory or DRAM) adj1 controller) and (coarse same fine))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:38

L10	87	(((memory or DRAM) adj1 controller) same "DRAM") and ((memory or DRAM) adj1 controller) and (coarse same fine same (address or command or data or clock))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:49
L11	1	"6016282".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
L12	1	"6115318".pn. and (coarse same fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:47
L13	1	"6115318".pn. and (coarse same fine) and (coarse and fine)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
L14	1	"6016282".pn. and (coarse same fine) and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:50
S1	7	(714/767-773.ccls. or 375/354.ccls. or 371-376.ccls.) and (phase with (sampl$4 with (command or instruct$4) with (data or information)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:11
S2	13	((synchroniz$4 or align$4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40
S3	7	((adjust$4) near3 phase) same (sampl$4 adj2 signals) same ((command or instruct$4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:19
S4	1	((calibrat$4) near3 (phase or timing)) same (sampl$4 adj2 signals) same ((command or instruct$4 or address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20
S5	0	((synchroniz$4 or align$4) near3 phase) with (sampl$4 adj2 signals) with ((address) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:20

EAST Search History

S6	1	((synchroniz$4 or align$4) near3 phase) same (sampl$4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21
S7	3	"DRAM" same (sampl$4 adj2 signals) same ((address) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:21
S8	3	"DRAM" same (sampl$4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:23
S9	3	"DRAM" same (sampl$4 adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S10	325	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) and (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S11	66	"DRAM" same (clock adj2 signals) same ((address or command or instruct$4) adj2 signals) same ((data or information) adj2 signals) same (phase or timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/02 19:25
S12	2749	365/194.ccls. or 365/233.ccls. and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 10:47
S13	1453	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:07
S14	318	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 15:05
S15	13	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:13

S16	2	S15 and sampl$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:54
S17	1267	("DQ" and "DQS") same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 11:55
S18	13	S17 and ((phase or timing) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S19	10	S17 and ((delay$4) with ((command or address) adj1 signals) with ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:10
S20	47	S17 and ((phase or timing) same ((command or address) adj1 signals) same ((data or information) adj1 signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:11
S21	11	(365/194.ccls. or 365/233.ccls.) and ((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or clock$4) adj1 signals) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:18
S22	14	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals) same "DRAM") and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S23	70	((phase or timing) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:21
S24	70	((phase or timing or synchroniz44) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22
S25	77	((phase or timing or synchroniz$4) same ((command$4 or address$4) adj1 signals) same ((sampling or "DQS")) same ((data or information) adj1 signals)) and "DRAM" and delay$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:22

EAST Search History

S26	965	S13 and "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S27	20	S26 and fine and coarse	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 12:56
S28	1612	((phase or timing) same (command$4 or address$4) same (sampling or clock$4) same (data or information)) same "DRAM"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:08
S29	35	S28 and (fine same coarse)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:09
S30	0	Rozas.in. and ((synchroniz$4 or align$4) near3 phase) with (sampl$4 adj2 signals) with ((command or instruct$4) adj2 signals) with ((data or information) adj2 signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2007/01/03 13:40

OIPE JC58
JUN 01 2004
PATENT & TRADEMARK OFFICE

Declaration and Power of Attorney for a Patent Application

Declaration

As below named inventor, I hereby declare that my residence post office address, and citizenship are as stated below my name. Further, I hereby declare that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

A METHOD AND SYSTEM FOR AUTOMATIC CALIBRATING INTRA-CYCLE TIMING RELATIONSHIP FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

the specification of which:

_____ is attached hereto, or
X was filed on 11/17/03 as application serial no. 10/716,320 : and
_____ was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; and

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

Foreign Priority Claim

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Number	Country	Date Filed	Priority Claimed	
			yes	no
			yes	no

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 and 119(e) of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Filing Date	Status (patented/pending/abandoned)

Power of Attorney

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent Trademark Office connected therewith.

James P. Hao	Registration No.: 36,398
Anthony C. Murabito	Registration No.: 35,295
John P. Wagner	Registration No.: 35,398
Glenn D. Barnes	Registration No.: 42,293
Thomas M. Catale	Registration No.: 46,434
Jose S. Garcia	Registration No.: 43,628
Eric J. Gash	Registration No.: 46,274
Lin C. Hsu	Registration No.: 46,315
Ronald M. Pomerenke	Registration No.: 43,009
John F. Ryan	Registration No.: 47,050
Matthew J. Blecher	Registration No.: 46,558
Lawrence R. Goerke	Registration No.: 45,927
Reginald A. Ratliff	Registration No.: 48,098
William A. Zarbis	Registration No.: 46,120
Mehlin Dean Matthews	Registration No.: 46,127
Joel D. Youngs	Registration No.: 52,389
Michael R. Hardaway	Registration No.: 52,992
Cheryl A. Eichstaedt	Registration No.: 50,761
Bryn C. Ekroot	Registration No.: 38,129

Send Correspondence to:

WAGNER, MURABITO & HAO LLP
Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060

Signatures

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: Guillermo J. Rozas

Inventor's Signature _____ Date May 19, 2004

Residence Los Gatos, CA (City State) Citizenship USA

P.O. Address 104 Magneson Terrace, Los Gatos, CA 95032

OIPE JUN 01 2004 PATENT & TRADEMARK OFFICE

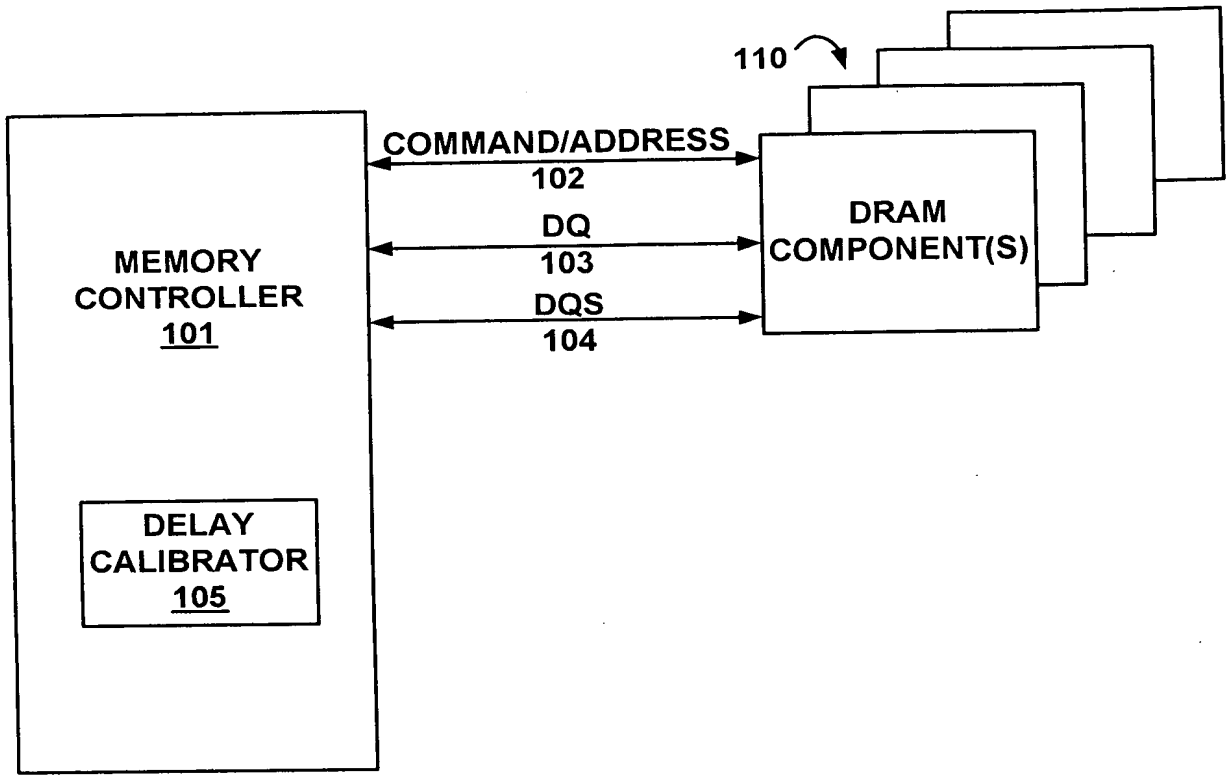


FIGURE 1

200

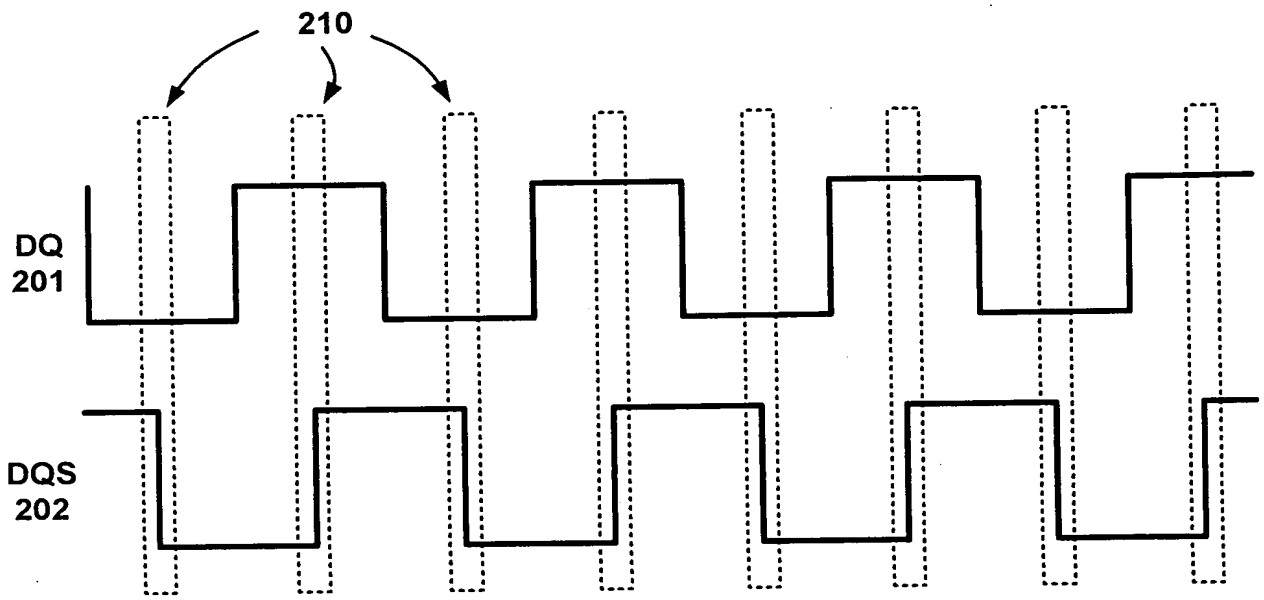


FIGURE 2

300

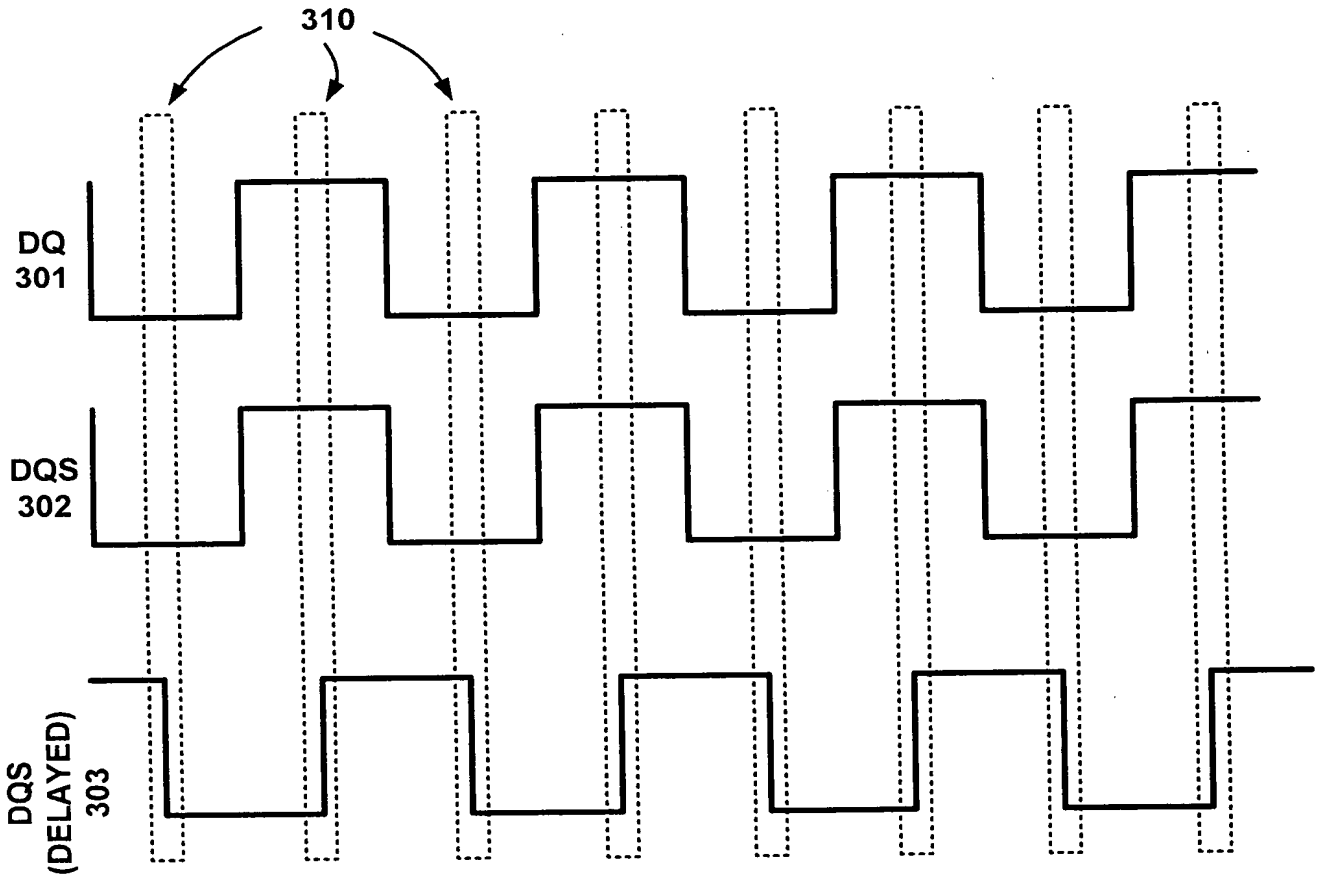


FIGURE 3

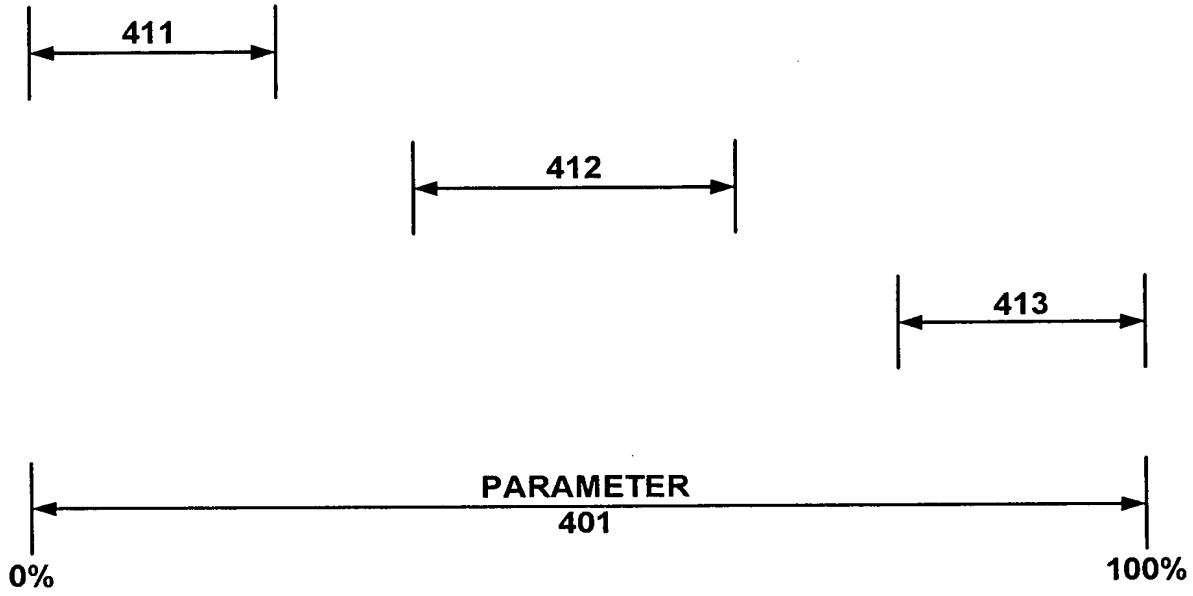


FIGURE 4

500

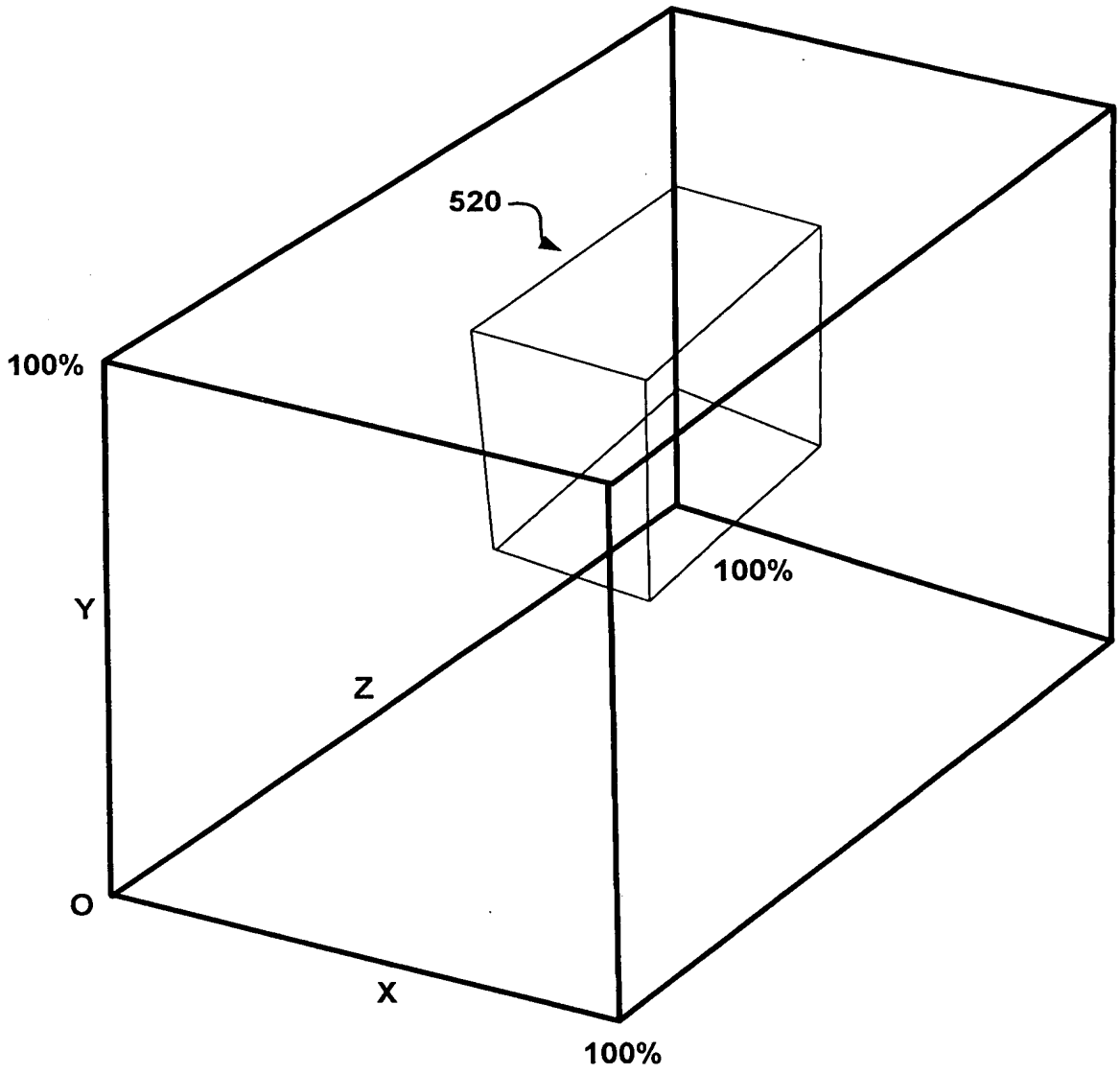


FIGURE 5

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156

CONFIRMATION NO. 5239

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

FORMALITIES LETTER

OC000000011924342

Date Mailed: 02/19/2004

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121 are required. The drawings submitted are not acceptable because:
    - The drawings must be reasonably free from erasures and must be free from alterations, overwriting, interlineations, folds, and copy marks. See Figure(s) 1, 2, 4 & 5.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$130** for a Large Entity

- **$130** Late oath or declaration Surcharge.

Replies should be mailed to: Mail Stop Missing Parts

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY

Attorney Docket No.: TRAN-P156

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

I hereby certify that this transmittal of the below described documents is being deposited with the United States Postal Service in an envelope bearing Express Mail Postage and an Express Mail label, with the below serial number, addressed to the Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450, on the below date of deposit.			
Express Mail Label No.:	EL965667570US	Name of Person Making the Deposit:	ANTHONY CHOU
Date of Deposit:	11/17/03	Signature of the Person Making the Deposit:	Anthony Chou

2389 U.S. PTO 10/716320 111703

Inventor(s): Guillermo J. Rozas

Title: A METHOD AND SYSTEM FOR AUTOMATIC CALIBRATING INTRA-CYCLE TIMING RELATIONSHIP FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

Transmittal of a Patent Application
(Under 37 CFR §1.53)

Transmitted herewith is the above identified patent application, including:

- X Specification, claims and abstract, totaling 21 pages.
- ____ Formal drawings, totaling ____ pages.
- X Informal drawings, totaling 5 pages.
- X Declaration and Power of Attorney.
- ____ Information Disclosure statement.
- ____ Form 1449
- ____ Assignment(s)
- ____ Assignment Recordation Form (duplicate)
- X Request and Certification under 35 U.S.C. 122(b)(2)(B)(i)

Amendments, Priority Claim

35 U.S.C. 119

☐ Priority of application Serial Number ____ filed on ____ in ____ is claimed under 35 U.S.C. 119.

☐ The certified copy has been filed in prior U.S. application Serial No. ____ in ____

☐ The certified copy will follow.

35 U.S.C. 120, 121 and 365(c)

"This application is a continuation of and claims the benefit of copending application(s)

☐ application number ____ filed on ____

☐ International Application ____ filed on ____

and which designated in the U.S."

☐ Amend this specification by inserting, before the first line, the following sentence:

"This application claims priority to the copending application(s)

☐ Serial Number filed on .....

which is hereby incorporated by reference to this specification

☐ International Application ..... filed on .....

which designated the U.S."

FEES DUE

The fees due for filing the specification pursuant to 37 C.F.R. § 1.16 and for recording of the Assignment, if any, are determined as follows:

CLAIMS					
	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEES
Basic Application Fee					$770.00
Total Claims	22	Minus 20=	2	X $18 =	$36.00
Independent Claims	6	Minus 3=	3	X $86=	$258.00
If multiple dependent claims are presented, add $290.00					$0.00
Add Assignment Recording Fee of $40.00 If Assignment document is enclosed					$0.00
TOTAL APPLICATION FEE DUE					$1,064.00

PAYMENT OF FEES

The full fee due in connection with this communication is provided as follows:

1. Not enclosed

   [ ] No filing fee is to be paid at this time.

2. Enclosed

   [X] Filing fee

   [ ] Recording assignment

   [X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

[X] A check in the amount of $1,064.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

This application is filed pursuant to 37 C.F.R. § 1.53 in the name of the above-identified Inventor(s).

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

[X] This transmittal ends with this page.

Respectfully submitted,

Date: 17 Nov 03

By: _____
Glenn D. Barnes
Reg. No. 42,293

Attorney Docket No.: **TRAN-P156**

Inventor(s): Guillermo J. Rozas

Title: A METHOD AND SYSTEM FOR AUTOMATIC CALIBRATING INTRA-CYCLE TIMING RELATIONSHIP FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

REQUEST AND CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

Date: 12 Nov 03

By: _____
Glenn D. Barnes
Reg. No. 42,293

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing**.

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant must notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

UNITED STATES PATENT APPLICATION

FOR

A METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

Inventor:

Guillermo J. Rozas

Prepared by:
WAGNER, MURABITO & HAO, LLP
Two North Market Street
Third Floor
San Jose, California 95113

A METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

TECHNICAL FIELD

The present invention relates to input and output signaling for digital integrated circuit devices.

BACKGROUND ART

The design and fabrication of high-performance signaling mechanisms for digital integrated circuit devices has become a significant challenge. For example, with respect to high-performance memory integrated circuit devices (e.g., DDR memory), ensuring the reliability in the design and fabrication of high performance memory modules has become problematic for many OEMs. In the past, slower memory bus speeds allowed significant specification margins in the design and fabrication of a given memory module. However, modern memory integrated circuit designs require exacting control of critical timing specifications, and design parameters must be strictly maintained to keep the entire system in balance. A stable DDR memory module must provide reliability, speed, and proper timing to insure the overall system (e.g., CPU, bridge components, peripheral busses, etc.) operates at peak performance. Thus what is required is a solution that can ensure critical timing specifications remain within certain specified parameters.

DISCLOSURE OF THE INVENTION

Embodiments of the present invention provide a method and system for automatically calibrating intra-cycle timing relationships for sampling signals for integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

Figure 1 shows a diagram of a memory system in accordance with one embodiment of the present invention.

Figure 2 shows a timing diagram depicting a typical DQ signal and a typical DQS signal during a write transaction in accordance with one embodiment of the present invention.

Figure 3 shows a timing diagram depicting a DQ signal and a DQS signal during a read transaction in accordance with one embodiment of the present invention.

Figure 4 shows a parameter range in accordance with one embodiment of the present invention.

Figure 5 shows a diagram of typical case where three parameters x, y, and z are varied across a range of adjustment to obtain valid windows for a DDR memory.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of embodiments of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the embodiments of the present invention.

Embodiments of the present invention implement a method and system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device. The method includes generating command signals for accessing an integrated circuit component, accessing data signals for conveying data for the integrated circuit component, and accessing sampling signals for controlling the sampling of the data signals. A phase relationship between the command signals, the data signals, and the sampling signals is automatically adjusted to calibrate the operation of the integrated circuit device. Embodiments of the present invention and their benefits are further described below.

Notation and Nomenclature

Some portions of the detailed descriptions which follow are presented in terms of procedures, steps, logic blocks, processing, and other symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. A procedure, computer executed step, logic block, process, etc., is here, and generally, conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present invention, discussions utilizing terms such as "storing" or "accessing" or "recognizing" or "retrieving" or "translating" or the like, refer to the action and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data

similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

Figure 1 shows a diagram of a memory system 100 in accordance with one embodiment of the present invention. As depicted in figure 1, the memory system 100 shows a memory controller 101 coupled to a plurality of DRAM components 110 via a command/address bus 102, a data bus (e.g., DQ) 103,and a sampling signal bus (e.g., DQS) 104. The memory controller 101 includes a delay calibrator 105.

The system 100 embodiment implements a method for automatically calibrating intra-cycle timing relationships between command signals of the command/address bus 102, data signals of the DQ bus 103, and sampling signals of the DQS bus 104. In the present embodiment, each of the DRAM components 110 comprise the integrated circuit device for which the calibration adjustments are performed. The actual adjustments are performed by the memory controller 101. The particular amounts of phase delay, or phase calibration, is determined by the delay calibrator 105.

The intra-cycle timing relationships between the command/address signals, the DQ signals, and the DQS signals are calibrated to ensure the optimal operation of the DRAM components 110. Generally, the calibration process includes generating command signals and address signals for accessing the DRAM components (e.g., DRAM chips of a memory module). The calibration process also includes accessing data signals (e.g., DQ signals) that convey data for the DRAM components, in both a data read transaction (e.g., data driven from the DRAM components 110 to the memory controller 101) and a data write

transaction (e.g., data driven from the memory controller 101 to the DRAM components 110). The calibration process also includes accessing sampling signals (e.g., DQS signals) for controlling the sampling of the data signals. A phase relationship between the command signals, the data signals, and the sampling signals is automatically adjusted to calibrate the operation of the DRAM components 110. In one embodiment, the adjusting is performed by the delay calibrator 105.

In this manner, the automatic calibration process of embodiments of the present invention enhances the design and qualification process required in certifying the proper operation of high-speed integrated circuit devices, such as DDR DRAMs (e.g., DRAM components 110). As is well-known, the designing and certification of high-speed DDR (Double Data Rate) memory modules has become a significant challenge for many system manufacturers. Practically all of the integral features of a given DDR DIMM (Dual In-Line Memory Module), such as the particular type of silicon used, the routing and thickness of the PCB (printed circuit board), and the signal integrity performance under stressed conditions (e.g., temperature, voltage, etc.), have an impact on the overall system performance and reliability. Failure to properly account for these variables can result in single or mutli-bit errors, read/write command sequencing failures, failure of the system to attain rated performance, and the like.

The automatic calibration process as provided by embodiments of the present invention adds a significant amount of "extra margin" to the specifications of a memory system. For example, for integrated circuit devices such as DDR DRAMs (e.g., DRAM components 110), the DDR timing specifications are so stringent that even slight variations

(e.g., between motherboards, devices from different lots, etc.) can have an impact on overall system performance and cause intermittent timing-related DIMM failures. These failures can be the most difficult types of failures to detect and correct. The extra margin provided by the embodiments of the present invention increase the reliability rate of computer systems incorporating such high performance integrated circuit devices. Alternatively, the extra margin provided by embodiments of the present invention can be used to increase the maximum obtainable performance of such computer systems.

An additional benefit provided by the automatic calibration embodiments of the present invention is fact that the variable operating parameters of an integrated circuit device can be efficiently explored (e.g., varied about a specified point of operation) even in those cases where no stable initial condition is known. Thus, for example, the even though a given PCB (printed circuit board) may not be properly manufactured within specified tolerances, the PCB may still be used because, unlike the prior art, no particular point of initial stable operation in the configuration space is required. What is needed is merely that some region of the configuration space (not known a-priori) be operable.

Embodiments of the present invention search for and find the valid region of operation within the configuration space without requiring knowledge , a-priori, where the valid region is. Thus, for example, embodiments of the present invention can automatically search the configuration space for a device (e.g., DRAM, PCB, etc.) by altering device parameters (e.g., the phase relationship between command signals, data signals, sampling signals, etc.) to find an optimal operating point even when the device is inoperable at its

supposed specified initial operating point (e.g., at the specified values for the parameters), thereby relaxing the specification tolerances required for successful operation of the device.

Although embodiments of the present invention are discussed in the context of DDR DRAM components, it should be appreciated that the automatic calibration aspects of the present invention can be used to enhance the performance of a number of different types of high-performance integrated circuit devices that require precisely aligned signals for their input and output.

Figure 2 shows a timing diagram 200 depicting a typical DQ signal 201 and a typical DQS signal 202 during a write transaction in accordance with one embodiment of the present invention. As shown in figure 2, a plurality of sampling windows 210 are also shown.

Timing diagram 200 illustrates the sampling windows 210 over which valid data can be read from a DDR memory component. This parameter is often referred to as "tDV". As described above, factors such as signal noise, crosstalk, skew, jitter, and drift effects brought on by voltage and thermal variations contribute to the available margin for tDV.

Timing diagram 200 shows the DQ signal 201 and the DQS signal 202 during write transaction, as in a case where data is written from a memory controller to a DRAM array. Generally, with DDR DRAMs, the sampling windows 210 correspond to the rising and falling edges of the DQS signal 202. The rising and falling edges of DQS 202 need to be accurately placed at the center of the rise-and-hold times of DQ 201 as shown (e.g., phase

shifted 90°). During the sampling windows 210, the logical value of the DQ signal is sampled and latched. As memory performance increases, the width of the sampling windows 210 correspondingly decreases (e.g., 2.5 nanoseconds for DDR 400 DRAM and 1.875 nanoseconds for DDR II 533 DRAM).

Figure 3 shows a timing diagram 300 depicting a DQ signal 301 and a DQS signal 302 during a read transaction in accordance with one embodiment of the present invention. During a read transaction, the rising and falling edges of DQS 302 needs to be accurately aligned with the rising and falling edges of the DQ signal 301 as shown. The memory controller then performs a 90° phase shift to place the sampling windows 310 at the center of the rise-and-hold times of DQ 301 (e.g., shown as DQS delayed 303). During read transactions, the memory controller is responsible for placing the sampling windows 310 at the correct locations.

Figure 4 shows a parameter range 401 in accordance with one embodiment of the present invention. As described above, a number of factors such as signal noise, crosstalk, skew, jitter, and drift effects brought on by voltage and thermal variations contribute to the available margin for tDV. These factors are in addition to the normal process variation inherent in any motherboard or device fabrication process. The parameter range 401 visually depicts a range of adjustment of a given parameter for an integrated circuit component (e.g., DRAM component 110).

For example, the phase shift of a DQS signal (e.g., DQS signal 202) can be adjusted over a certain range. This range extends from a minimum to a maximum and is typically

demarcated standard units (e.g., percent, etc.). Thus in a case where the parameter 401 is DQS phase shift or DQS delay, the range extends from an earliest phase shift (e.g., 0%) to a latest phase shift (e.g., 100%).

Three valid ranges 411-413 are shown. Over the range 401, there will exist a window at which the given parameter is "correct" for a given device. This is usually a limited range across which the parameter provides for correct device operation. Three such valid ranges 411-413 are shown. Embodiments of the present invention take advantage of the fact that such valid windows typically occur at a lower end of the range (e.g., range 411), near the center of the range (e.g., range 412), or near the upper end of the range (e.g., range 413), and that there is only one such valid window across a parameter range of adjustment 401.

Figure 5 shows a diagram 500 of typical case where three parameters x, y, and z are varied across a range of adjustment to obtain valid windows for a DDR memory. As depicted in figure 5, the three axes of the parameters are plotted orthogonal to one another. In the case of a DDR DRAM component, for example, the x parameter can correspond to a phase range of command/address signals, the y parameter can correspond to a phase range of DQ signals, and the z parameter can correspond to a phase range of DQS signals.

For a given device, there will be a valid region within which the values of the x, y, and z parameters result in the correct operation of the device. This is shown in figure 5 as the valid region 520. Ideally, the valid region 520 will correspond to the specified region of operation as determined by the system builder. However, as described above, a number of

factors affect the location and size of the valid region 520, or whether even such a valid region 520 exists for a given device. For example, a faulty DRAM component may not have a valid region 520.

Embodiments of the present invention automatically alter the x, y, and z parameters (e.g., the intra-cycle command/address phase, DQ phase, and DQS phase) in order to determine the boundaries of the valid region 520. Once such boundaries are discovered, configuration choices can be intelligently made as to the optimal operating point for a given device.

Embodiments of the present invention determine the boundaries of the valid region 520 by systematically altering the variable parameters. In one embodiment, a coarse calibration method is first used in order to determine whether or not a valid region 520 exists, and a fine calibration method is subsequently used in order to determined the precise boundaries of the valid region 520.

In a coarse calibration method, parameters can be varied across the range using a relatively large step increment (e.g., ranging from 0% to 100% in 5% step increments). In one embodiment, the coarse calibration method is configured to vary each of the parameters (e.g., x, y, and z) simultaneously (e.g., it is multi-variate), as it tries to find an approximation to the corner of the valid region 520 nearest point at [0%,0%,0%], and an approximation to the corner of the valid region 520 nearest the point at [100%,100%,100%].

In a fine calibration method, parameters can be varied across the range using a relatively small step increment (e.g., a 2% step increment). In one embodiment, the fine calibration method explores single parameters at a time (e.g., it is uni-variate), given that stable points for the aggregate are known and hence the other parameters can be left unmodified. Thus, a coarse calibration can be performed relatively quickly determine whether any valid region of operation exists for given device. If such a region does exist, the fine calibration can be performed to determine a best operating point within such region for the device.

In one embodiment, the device (e.g., a DDR DRAM) is stimulated by writing test data to the DRAM and then reading the test data. The presence of errors in the read test data indicates one or more of the parameters is out of alignment.

A pseudo code example representation of the calibration process is now described. In the following pseudo code example, the terms x_limit, y_limit, and z_limit correspond to the maximum value of the parameter's range, and the terms x_step, y_step, and z_step correspond to the step increment used (e.g., coarse vs. fine). In one embodiment, the calibration process is implemented by a delay calibrator (e.g., delay calibrator 105) integrated within a memory controller (e.g., memory controller 101).

```
For (x=0, x<= x_limit, x+=x_step)
    For (y=0, y<=y_limit, y+=y_step)
        For (z=0, z<=z_limit, z+=z_step)
            If test(x,y,z) passes, then abort loop and remember x,y,z.
```

The above process searches for the point nearest [0%,0%,0%] of the valid region 520. Then, in the process below, the range is searched for the point nearest [100%,100%,100%] of the valid region 520.

```
For (x=x_limit, x>= 0, x-=x_step)
    For (y=0, y<=y_limit, y+=y_step)
        For (z=0, z<=z_limit, z+=z_step)
            If test(x,y,z) passes, then abort loop and remember x,y,z.
```

Once the location of the valid region 520 is approximated, a fine calibration method can be performed (e.g., uni-variate) to precisely identify the boundaries of the valid region 520.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

CLAIMS

What is claimed is:

1. A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

generating command signals for accessing an integrated circuit component;

accessing data signals for conveying data for the integrated circuit component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically adjusting a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device.

2. The method of claim 1, wherein the integrated circuit device is a DRAM component.

3. The method of claim 2, wherein the adjusting of the phase relationship is performed by a memory controller coupled to the DRAM component.

4. The method of claim 2, wherein the DRAM component is a DDR DRAM component.

5. The method of claim 4, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

6. The method of claim 5, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

7. A system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

a controller for generating command signals for accessing an integrated circuit component;

a delay calibrator integrated within the controller and configured to access data signals conveying data for the integrated circuit device and to access sampling signals for controlling the sampling of the data signals, the delay calibrator further configured to automatically adjust a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, without requiring a valid initial operating point for the integrated circuit device.

8. The method of claim 7, wherein the integrated circuit device is a DRAM component.

9. The method of claim 8, wherein the DRAM component is a DDR DRAM component.

10. The method of claim 9, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

11. The method of claim 10, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

12. In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically altering a phase relationship between the command signals, the data signals, and the sampling signals to determine an operating mode of the DRAM component, without requiring a valid initial operating point for the DRAM component.

13. The method of claim 12, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component.

14. The method of claim 13, further comprising:

configuring the memory controller to operate with the DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

15. The method of claim 12, wherein the DRAM component is a DDR DRAM component.

16. The method of claim 15, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

17. The method of claim 16, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

18. A computer readable media for finding an operating mode for a DDR DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the media storing computer readable code which when executed by a memory controller causes the memory controller to implement a method comprising:

generating command signals for accessing a DDR DRAM component;

accessing DQ signals for conveying DQ for the DDR DRAM component;

accessing DQS signals for controlling the sampling of the DQ signals; and

automatically altering a phase relationship between the command signals, the DQ signals, and the DQS signals to determine an operating mode of the DDR DRAM component, without requiring a valid initial operating point for the DRAM component.

19. The computer readable media of claim 18, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DDR DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DDR DRAM component.

20. The computer readable media of claim 19, further comprising:

configuring the memory controller to operate with the DDR DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

21. In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically altering a phase relationship between the command signals, the data signals, and the sampling signals to determine an operating mode of the DRAM component, wherein the DRAM component inoperable at a specified initial operating point.

22. In a memory controller, a method for finding an operating mode for a DRAM component coupled to a PCB (printed circuit board) by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically altering a phase relationship between the command signals, the data signals, and the sampling signals transmitted via a PCB to determine an operating mode of the DRAM component, wherein the DRAM component is inoperable at a specified initial operating point.

A METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

ABSTRACT OF THE DISCLOSURE

A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device. The method includes generating command signals for accessing an integrated circuit component, accessing data signals for conveying data for the integrated circuit component, and accessing sampling signals for controlling the sampling of the data signals. A phase relationship between the command signals, the data signals, and the sampling signals is automatically adjusted to calibrate operation of the integrated circuit device.

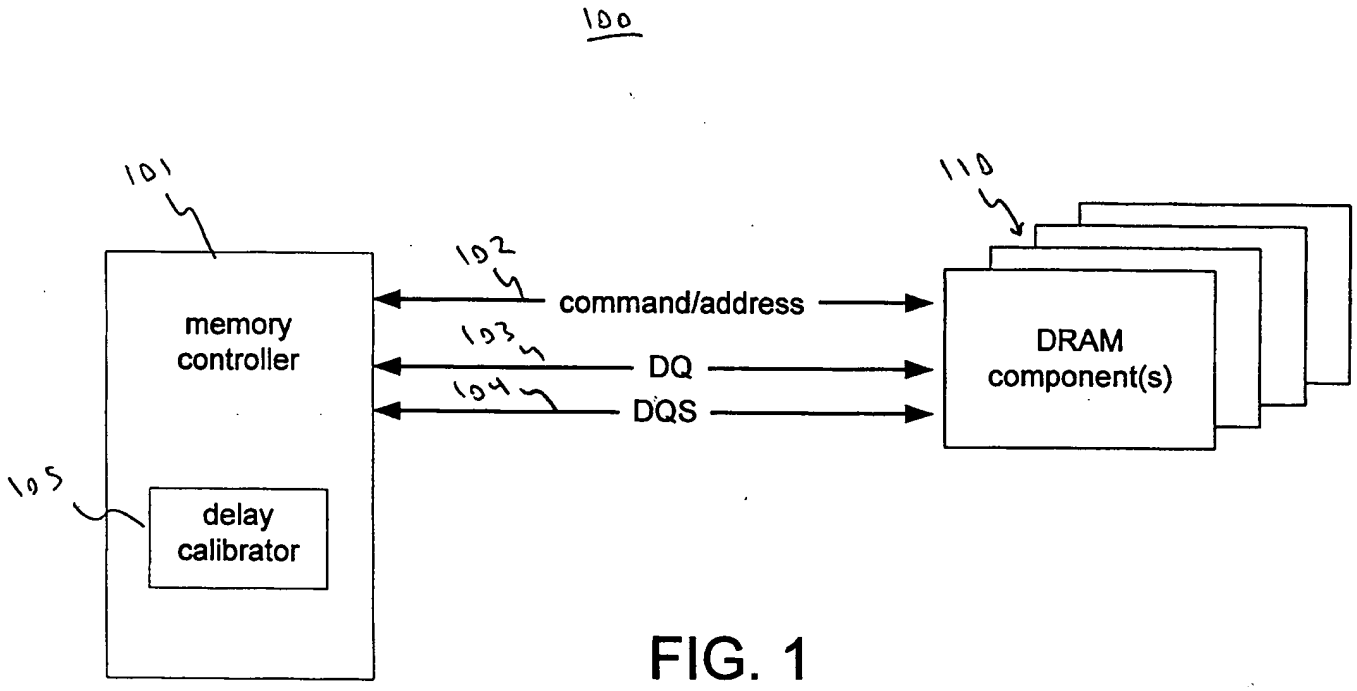

100
101
memory controller
105
delay calibrator
102
command/address
103
DQ
104
DQS
110
DRAM component(s)

FIG. 1

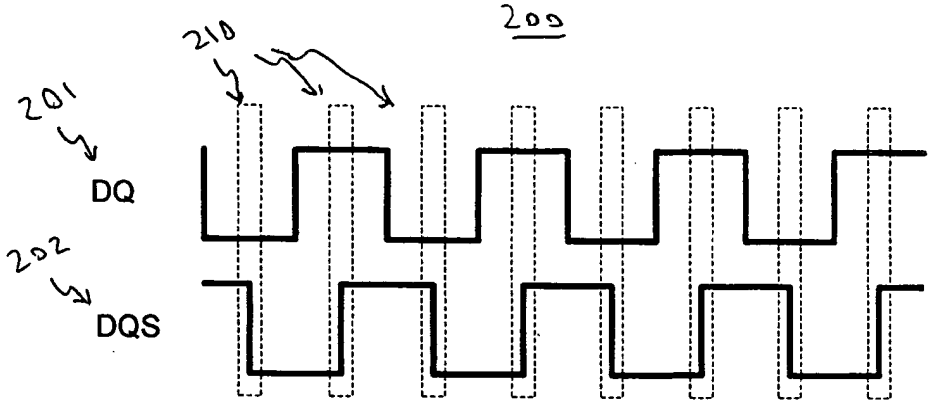


FIG. 2

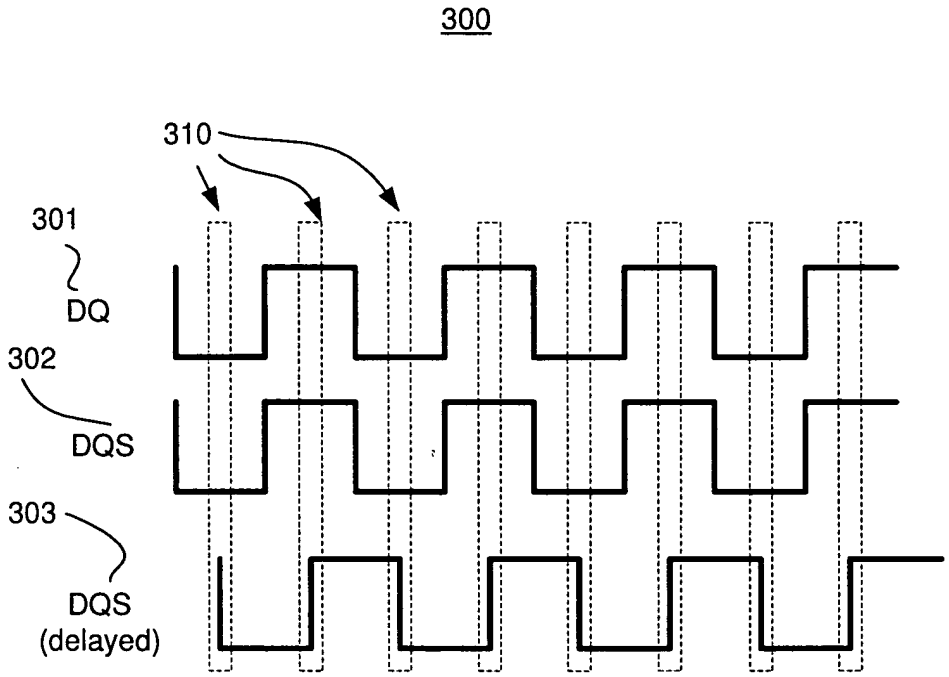


FIG. 3

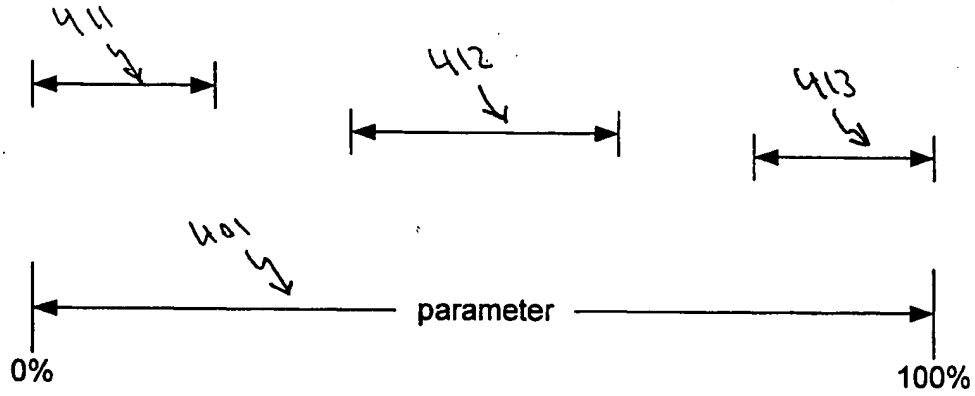


FIG. 4

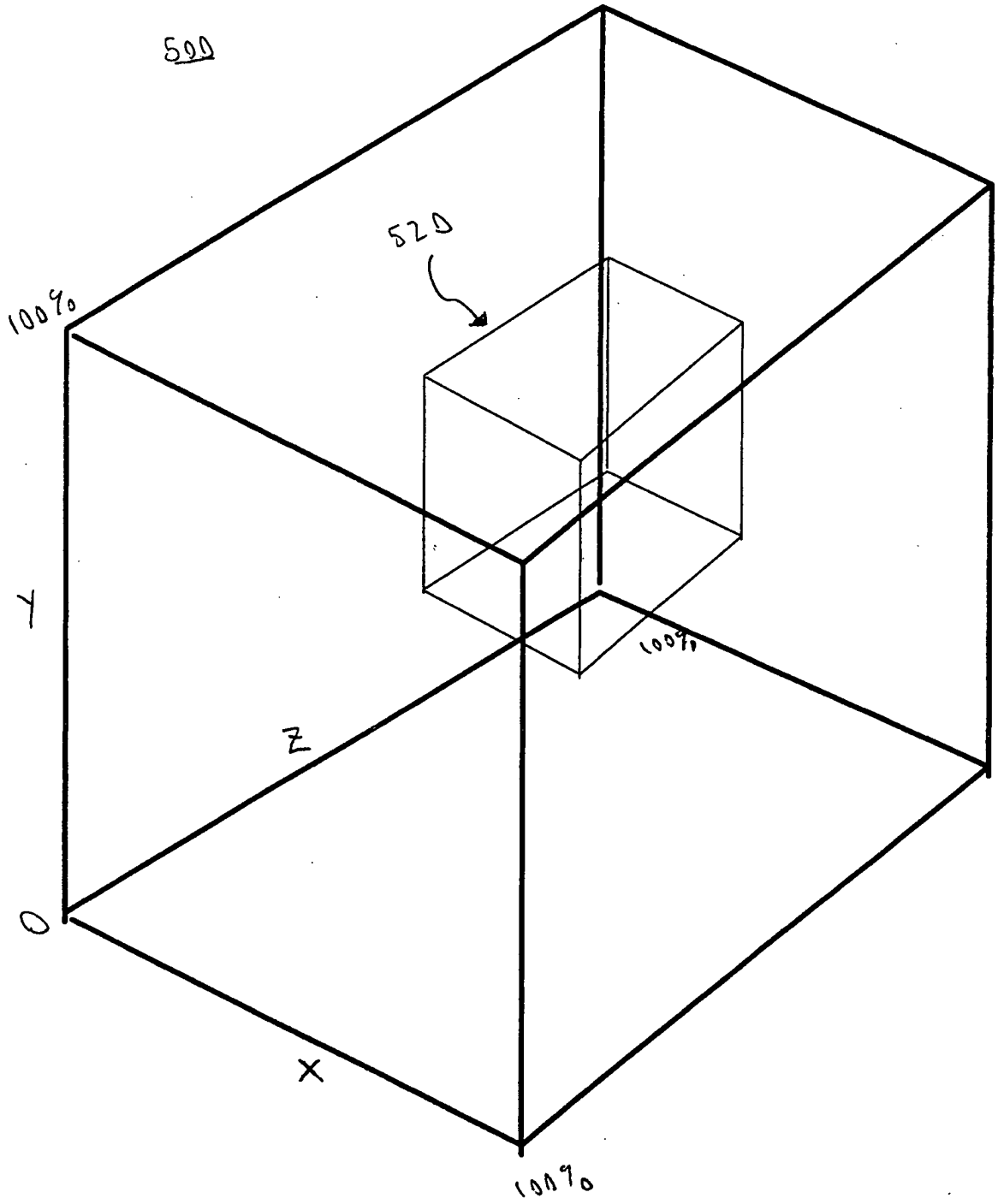


FIG. 5

Declaration and Power of Attorney for a Patent Application

D claration

As below named inventor, I hereby declare that my residence post office address, and citizenship are as stated below my name. Further, I hereby declare that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

A METHOD AND SYSTEM FOR AUTOMATIC CALIBRATING INTRA-CYCLE TIMING RELATIONSHIP FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE

the specification of which:

.X. is attached hereto, or
..... was filed on ..... as application serial no. ..... : and
..... was amended on .....

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; and

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

Foreign Priority Claim

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Number	Country	Date Filed	Priority Claimed	
.....	.....	.....	..... yes	..... no
.....	.....	.....	..... yes	..... no

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 and 119(e) of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Filing Date	Status (patented/pending/abandoned)
.....	.....	.....
.....	.....	.....

Pow r of Attorn y

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent Trademark Office connected therewith.

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Signatures

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: **Guillermo J. Rozas**

Inventor's Signature _____ Date _____

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PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

11/21/2003 HLE333 00000071 10716320

01 FC:1001	770.00 OP
02 FC:1201	258.00 OP
03 FC:1202	36.00 OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10/716,320

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	22	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	22 minus 20=	* 2
INDEPENDENT CLAIMS	6 minus 3 =	* 3
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
X$ 9=		OR	X$18=	216
X43=		OR	X86=	258
+145=		OR	+290=	
TOTAL		OR	TOTAL	1064

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.