UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.
Petitioner

v.

INTELLECTUAL VENTURES II LLC
Patent Owner

Case No. IPR2024-01226
Patent No. 7,646,835 B1

**DECLARATION OF R. JACOB BAKER, P.E., PH.D.
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,646,835 B1**

Petitioner Lenovo (United States) Inc. - Ex. 1002

TABLE OF CONTENTS

I. INTRODUCTION 1

A. Background and Qualifications 2

1. Industry Experience 3

2. Academic Experience 7

3. Other Relevant Experience 9

B. Summary of Opinions and Materials Reviewed 10

II. LEGAL STANDARDS FOR PATENTABILITY 13

A. Anticipation 13

B. Obviousness 13

C. Level of Ordinary Skill in the Art 17

D. Claim Construction 19

1. Preambles (Claims 1, 7, 12, 20, and 23) 20

2. "the valid operating range includes an optimal operation point for the integrated circuit device" (Claims 1 and 7) 20

III. OPINION 21

A. Background of the Technology 21

1. Dynamic Random-Access Memory (DRAM) 21

2. DDR DRAM and SLDRAM 24

3. Memory Controllers 27

B. Overview of the '835 Patent 31

C. Overview of the '835 Patent's File History 39

D. Summary of the Prior Art References 43

1. Johnson (Ex. 1004).....43

2. Jeddeloh (Ex. 1005).....49

3. Keeth (Ex. 1006).....56

E. Summary of the Grounds.....64

F. Ground 1: Claims 1-23 are Obvious Over *Johnson* in View of *Jeddeloh*.....66

1. Claim 1.....66

2. Claim 2 – The method of claim 1, wherein the integrated circuit device comprises a DRAM component.....97

3. Claim 3 – The method of claim 2, wherein said altering is performed by a memory controller coupled to the DRAM component. 97

4. Claim 4 – The method of claim 2, wherein the DRAM component comprises a DDR DRAM component.....103

5. Claim 5 – The method of claim 4, wherein the data signals comprise a plurality of data bus (DQ) signals for the DDR DRAM component.....106

6. Claim 6 – The method of claim 5, wherein the sampling signals comprise a plurality of sampling bus (DQS) signals for the DDR DRAM component.....108

7. Claim 7.....112

8. Claim 8 – The system of claim 7, wherein the integrated circuit device comprises a DRAM component.....123

9. Claim 9 – The system of claim 8, wherein the DRAM component comprises a DDR DRAM component.....124

10. Claim 10 – The system of claim 9, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component. 124

11. Claim 11 – The system of claim 10, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component. 125

12. Claim 12 125

13. Claim 13 127

14. Claim 14 – The method of claim 13, wherein said performing a coarse calibration comprises simultaneously varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal by a five percent step increase... 134

15. Claim 15 – The method of claim 13, wherein said performing a fine calibration comprises varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal one at a time by a two percent step increase.136

16. Claim 16 – The method of claim 13, further comprising configuring the memory controller to operate the DRAM component in the optimal operating mode..... 139

17. Claim 17 – The method of claim 12, wherein the DRAM component comprises a DDR DRAM component..... 140

18. Claim 18 – The method of claim 17, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component. 140

19. Claim 19 – The method of claim 18, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component. 140

20. Claim 20 141

21. Claim 21 144

22. Claim 22 – The computer readable media of claim 21, wherein the method further comprises configuring the memory controller to operate the DRAM component in the optimal operating mode. 146

23. Claim 23 147

G. Ground 2: Claims 1-3, 7-8, and 12 are Obvious Over *Johnson* in View of *Keeth*. 149

1. Claim 1 150

2. Claim 2 – The method of claim 1, wherein the integrated circuit device comprises a DRAM component. 166

3. Claim 3 – The method of claim 2, wherein said altering is performed by a memory controller coupled to the DRAM component. 166

7. *Claim 7* 169

8. *Claim 8 – The system of claim 7, wherein the integrated circuit device comprises a DRAM component.* 174

12. *Claim 12* 174

H. Ground 3: Claims 4-6, 9-11, 13-19 are Obvious Over *Johnson* in View of *Keeth* and *Jeddeloh* 176

IV. CONCLUSION 178

I, R. Jacob Baker, declare as follows:

I. INTRODUCTION

1. I have been retained by Lenovo (United States) Inc. ("Lenovo" or "Petitioner") as an independent technical expert consultant in connection with the above-captioned *Inter Partes* Review of U.S. Patent No. 7,646,835 B1 ("the '835 Patent") (Ex. 1001). Although I am being compensated at my normal consulting rate of $765 per hour for the time I spend on this matter, no part of my compensation is dependent on the outcome of this proceeding or any other related proceeding. I have no other interest in this proceeding.

2. I understand that the '835 Patent is assigned to Intellectual Ventures II LLC ("Intellectual Ventures" or "Patent Owner"). In addition, I understand that the '835 Patent issued from U.S. Application No. 10/716,320 (the "'320 application"), which was filed on November 17, 2003. (Ex. 1001.)

3. I am familiar with the technology at issue as of November 17, 2003, i.e., the filing date of the '320 application.

4. I have been asked to consider how a person having ordinary skill in the art (POSITA) would have understood the claims of the '835 Patent and the applied references. More specifically, I have been asked to provide my technical opinion on concepts discussed in the '835 Patent and the reference documents, as

well as my technical opinion on how these concepts relate to the '835 Patent's claim limitations in the context of the written description.

5. In reaching the opinions stated herein, I have considered the '835 Patent and the various other documents listed in Section III below in the context of my own education, training, research, knowledge, and personal and professional experiences. My opinions are provided below.

A. Background and Qualifications

6. My qualifications generally are set forth in my Curriculum Vitae, which is attached as Appendix A. Appendix A also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

7. I have been working as an Engineer since 1985 and I have been teaching Electrical and Computer Engineering courses since 1991. I am currently a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas ("UNLV").

8. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

9. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power,

and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 V and 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices," published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

1. *Industry Experience*

10. I have done technical and expert witness consulting for over 200 companies and their subsidiaries since I started working as an engineer in 1985. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada Test Site. During this time, I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments, including high-speed cable and fiber-optic receiver/transmitters, phase locked loops (PLLs), frame and bit-syncs, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

11. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and

industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working in industry. I hold a patent, Patent No. 5,874,830, in the area of power supply design, titled, "Adaptively biased voltage regulator and operating method," which was issued on February 23, 1999. I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

12. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. ("MTI") in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that

can improve a computing system's performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via inter-process communications (IPC) with the memory controller (MC). This included interfacing with processors having multiple cores that operate at various independent clock frequencies using, for example, DDR protocols. I also developed delay locked loops in DDR memory. I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and 2010. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

13. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays)

circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB, firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics. For example, a part of my research at Boise State, for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density 3D packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while I did consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc. in the late 1990s. The main processor and GPU ran at independent clock frequencies which required the design of a phase-locked loop on the GPU. I did similar work for Amkor also in the late 1990s. From 1994 to 1996, I worked on the design of displays at Micron Display and MTI in Boise, Idaho. This work was at a time when cathode ray tubes (CRTs) were still the dominant type of display. Flat panel displays were being developed with the hope of replacing CRTs in the consumer market. I worked on flat panel displays which resulted in 5 patents: U.S.

Patent Nos. 5,598,156, 5,638,085, 5,818,365, 5,894,293, and 5,909,201. I worked on the design of the pixels, both active and passive, as well as the supporting electronics for processing video signals. I was involved with the evaluation of display technologies including liquid crystal displays (LCDs), light-emitting diodes, plasma displays, and organic light emitting diode (OLED) displays; the display technologies that were looking to displace CRTs in the consumer market. I was also involved with the packaging of the displays including the vacuum sealing and deposition of the phosphors for light wavelength conversion. I also taught display design as a topic in my courses and did display design consulting again in industry for Cirque in 2013.

14. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (LIght Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years focused on the digitization of IQ channels using delta-sigma modulation. The knowledge and experience gained from this effort are reflected in my textbook *CMOS Mixed-Signal Circuit Design*.

2. *Academic Experience*

15. I was an adjunct faculty member in the Electrical Engineering departments of UNLV and University of Nevada, Reno (UNR) from 1991-1993. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University ("BSU"), where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate programs in Electrical and Computer Engineering including, in 2006, the university's second Ph.D. degree. In 2012, I rejoined the faculty at UNLV. Over the course of my career as a professor, I have advised more than 100 masters and doctoral students.

16. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the "Father of Silicon Valley"). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the Tau Beta Pi Outstanding Electrical and Computer

Engineering Professor Award every year it was awarded while I have been back at UNLV.

17. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and Simulation (Baker, R.J., Wiley-IEEE, ISBN: 9781119481515 (4th ed., 2019)) and CMOS Mixed-Signal Circuit Design (Baker, R.J., Wiley-IEEE, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I co-authored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 9780470184752 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley - IEEE, ISBN: 9780780334168 (1998)). I contributed as an editor and co-author on several other electrical and computer engineering books.

3. *Other Relevant Experience*

18. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries, and given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication, and packaging.

19. I currently serve, or have served, as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-present). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

20. In addition to the above, I am an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

B. Summary of Opinions and Materials Reviewed

21. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my knowledge and

experience in designing, developing, and researching high-speed computer memory devices, I reviewed the following documents:

- '835 Patent (Ex. 1001)
- Prosecution History of '835 Patent (Ex. 1003)
- U.S. Patent No. 6,434,081 B1 to Johnson *et al.* ("*Johnson*") (Ex. 1004)
- U.S. Patent No. 6,629,222 B1 to Jeddeloh ("*Jeddeloh*") (Ex. 1005)
- U.S. Patent No. 6,115,318 A to Keeth ("*Keeth*") (Ex. 1006)
- Claim Construction Order, *Intellectual Ventures I LLC et al. v. Lenovo Group Limited*, 6:23-cv-307 (WDTX) (Ex. 1007)
- *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* by Bruce L. Jacob, published in December of 2002 ("*Jacob*") (Ex. 1008)
- *RAM Guide Part I: DRAM and SDRAM Basics* by Jon Stokes, published in July of 2000 ("*Stokes*") (Ex. 1009)
- *Design and PCB Layout Considerations for Dynamic Memories Interfaced to the Z80 CPU* by Tim Olmstead, published in October of 1996 ("*Olmstead*") (Ex. 1010)
- *A Performance Comparison of Contemporary DRAM Architectures* by Vinodh Cuppu *et al.*, published in May of 1999 ("*Cuppu*") (Ex. 1011)
- *How to Use DDR SDRAM* by Elpida Memory, published in April of 2002 ("*Elpida*") (Ex. 1012)
- *Hyundai Electronics Actively Supplying DDR SDRAM Modules to Major PC Makers* by SK hynix, published in March of 2001 (Ex. 1013)
- *SLDRAM: High Performance, Open-Standard Memory* by Peter Gillingham *et al.*, published in December of 1997 ("*SLDRAM*") (Ex. 1014)

- *3.1. How Memory Works with the Processor* by Technick, published in March of 1998 (Ex. 1015)
- *Memory Access Scheduling* by Scott Rixner *et al.*, published in March of 2000 (Ex. 1016)
- *Computer-System Operation,* published in July of 1999 ("*Computer-System*") (Ex. 1017)
- *Course-to-fine Estimation of Visual Motion* by Eero P. Simoncelli, published in September of 1993 (Ex. 1018)
- *Modern Dictionary of Electronics Seventh Edition* by Rudolf F. Graf, published in February of 1999 ("*Dictionary of Electronics*") (Ex. 1019)
- *Merriam-Webster's Collegiate Dictionary Tenth Edition*, published in 2000 ("*Merriam-Webster's Dictionary*") (Ex. 1020)
- *Double Data Rate (DDR) SDRAM Specification* by JEDEC Solid State Technology Association, published in June of 2000 (Ex. 1021)

22. The opinions in this Declaration additionally are guided by my appreciation of how a POSITA (defined below in Section II(C)) would have understood the claims and specification of the '835 Patent at the time of alleged invention of the '835 Patent. I have been asked to assume that the time of alleged invention of the '835 Patent is November 17, 2003, which is the filing date of the '320 application. The opinions below reflect how a POSITA would have understood the '835 Patent, the prior art to the patent, and the state of the art at the time of alleged invention of the '835 Patent.

23. Based on my experience and expertise, it is my opinion that certain references disclosed all of the features recited in Claims 1-23 ("Challenged Claims") of the '835 patent, as I discuss in detail below.

II. LEGAL STANDARDS FOR PATENTABILITY

24. I am not an attorney and I offer no opinions on the law itself. My understanding of the relevant legal principles in this section is based on information provided to me by counsel.

A. Anticipation

25. I have been informed by counsel that under 35 U.S.C. § 102, for a claim to be invalid as "anticipated," every limitation of the claim must be found in a single prior art reference, either expressly or inherently.

B. Obviousness

26. I have been informed by counsel that a patent claim may be found invalid under 35 U.S.C. § 103(a) if the subject matter of the claim as a whole would have been obvious to a hypothetical POSITA in view of a prior art reference or in view of a combination of references at the time of the alleged invention. I have been informed that obviousness is determined from the perspective of a POSITA and that the Challenged Claims should be read from the point of view of such a person at the time the alleged invention was made. I have also been informed that a POSITA is assumed to know and to have all relevant prior art in

the field of endeavor covered by the patent in suit, and would thus have been familiar with each of the references cited herein, as well as the background knowledge in the art discussed in Section III(A), and the full range of teachings they contain.

27. I have been informed of two criteria for determining whether a prior art reference is analogous and therefore qualifies as prior art: (1) whether the reference is from the same field of endeavor as the Challenged Claims, regardless of the problem addressed, and (2) if the reference is not within the field of endeavor of the Challenged Claims, whether the reference still is reasonably pertinent to the particular problem which the Challenged Claims purport to address. I have additionally been informed that the field of endeavor of a patent is not limited to a specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference may be reasonably pertinent to the Challenged Claims if, even though the reference may be in a different field than the Challenged Claims, the reference is one which logically would have commended itself to a patentee's attention in considering his problem because of the subject matter with which the reference deals.

28. I further have been informed that whether an alleged invention would have been obvious should be analyzed in view of the scope and content of the prior

art, the differences (if any exist) between the prior art references and the alleged invention, and the level of ordinary skill in the pertinent art involved. I have been additionally informed that a prior art reference should be viewed as a whole when performing the above analysis.

29. I have been informed that in considering whether a claimed combination would have been obvious, I may assess whether there were apparent reasons to combine elements in the prior art in the manner claimed in view of interrelated teachings of one or more prior art references, the impact of demands known to the community or present in the market place, and/or the general knowledge possessed by a POSITA at the time of alleged invention. I have been informed that other principles may be relevant in evaluating whether an alleged invention would have been obvious, and that these principles may include the following:

- A combination of prior art elements according to known methods is likely to be obvious when it does nothing more than yield predictable results;
- When a known device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or in a different one, so that if a POSITA is able to implement a predictable variation, then that variation is likely obvious;
- If a known technique has been used to improve a device, method, or product, and a POSITA would recognize that it would improve similar devices in the same predictable way, using the technique is obvious

unless the actual implementation of the technique is beyond his or her skill;

- An explicit or implicit teaching, suggestion, or motivation in the prior art to combine the prior art references to form the claimed combination may demonstrate obviousness (but a teaching, suggestion, or motivation to combine is not a requirement for proving obviousness);

- Market demand, rather than scientific literature, can drive design trends and may show obviousness;

- In determining whether the subject matter of a patent claim would have been obvious, neither the motivation nor the purpose of the named inventor controls;

- The subject matter of a patent may be proved obvious by demonstrating that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;

- Any need or problem known in the field and addressed by the prior art can provide a reason for a POSITA at the time of the invention to combine the elements in the manner claimed;

- "Common sense" indicates that known items and methods may have obvious uses beyond their primary purposes, and in many cases, a POSITA would be able to fit the teachings of multiple prior art references together similar to the pieces of a puzzle;

- A POSITA is also a person having ordinary creativity, and is not an automaton;

- A patent claim may be proved obvious by demonstrating that the claimed combination of elements was "obvious to try," especially when there exists a design need or market pressure to solve the problem and there are a limited number of identified, predictable solutions such that a POSITA would have had good reason to pursue the known options within his or her technical grasp; and

- One should be careful of relying on hindsight in evaluating whether an alleged invention would have been obvious.

30. I have further been informed that, in making a determination as to whether or not the alleged invention would have been obvious to a POSITA, the Board might consider the presence of additional objective or secondary factors, such as: commercial success of products which practice the purported invention; a long-felt but unsolved need; teaching away; unexpected results; copying; and industry praise. These factors are typically referred to as "secondary considerations" or "objective indicia" of nonobviousness. I have been informed, however, that for such objective indicia or secondary evidence to be relevant to the obviousness analysis, there must be a causal relationship (known as a "nexus") between the challenged claim and the objective indicia evidence, and that this nexus must be based on what is claimed and novel in the claim, and not something in the prior art. I have also been informed by counsel that even when objective indicia evidence is present, these secondary considerations may be unable to overcome sufficiently strong primary evidence showing obviousness (e.g., motivation to combine with predictable results).

C. Level of Ordinary Skill in the Art

31. I understand that certain issues relating to patent validity must be judged from the perspective of a POSITA, as discussed below.

32. The ’835 Patent relates to input and output signaling for digital memory devices, and, in particular, to calibration of intra-cycle timing relationships between signals in high-speed computer memory devices.

33. Based on my knowledge and experience, I understand what a POSITA would have known at the time of the alleged invention (as I mentioned above). The opinions herein are, where appropriate, based on my understanding of the perspective of a POSITA at that time. In determining the level of ordinary skill, I have been asked to consider, for example, the types of problems encountered in the field, prior solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the education level of active workers in the field.

34. In my opinion, based on the materials and information I have reviewed, and based on my experience in the technical areas relevant to the ’835 Patent, a POSITA at the time of the alleged invention of the ’835 Patent would have had a bachelor’s degree in electrical engineering, computer engineering, or the equivalent, and two to three years of experience designing high-speed computer memory devices. More practical experience could qualify one not having the aforementioned education as a POSITA, while a higher level of education could offset lesser experience.

35. Under these definitions, I am qualified as a person of ordinary skill in the art during the relevant time frame stated above (i.e., November 2003). I provide my analysis of the '835 Patent, the prior art, and my opinions in this Declaration from the perspective of a POSITA, as I have defined it above, during the relevant time frame stated above, where appropriate.

D. Claim Construction

36. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a POSITA, during the relevant time frame, which I was asked to assume was in November of 2003. In considering the meaning of the claims, I also understand that one must consider the claim language, specification, prosecution history, and the knowledge of a POSITA at the relevant time. I have followed these principles in my analysis.

37. I also understand that certain terms of the claims of the '835 Patent were previously construed by the United States District Court for the Western District of Texas in *Intellectual Ventures I LLC et al. v. Lenovo Group Ltd.*, No.

6:23-cv-00307 (WDTX May 28, 2024). Ex. 1007 at 8[1]. I have reviewed the following prior constructions and have applied them in my analysis as discussed below.

1. *Preambles (Claims 1, 7, 12, 20, and 23)*

38. I understand that the preambles of Claims 1, 7, 12, 20, and 23 have been construed so as not to be not limiting. *Id.* at 8. My analysis below is consistent with this construction. Additionally, I have explained in my analysis how the prior art nonetheless teaches the preambles of each of Claims 1, 7, 12, 20, and 23. Therefore, even if the preambles were limiting, the opinions in this Declaration would not change.

2. *"the valid operating range includes an optimal operation point for the integrated circuit device" (Claims 1 and 7)*

39. I understand that this term has been afforded its plain and ordinary meaning. *Id.* at 8. I also understand that this term has been construed such that it "does not require determining the optimal operation point." My analysis below is consistent with this construction. Additionally, I have explained in my analysis

[1] In this Declaration, I refer to the written portions of a patent document by making reference to the column:line number or paragraph number of the exhibit. For all other documents or portions of patent documents, I refer to the page number of the exhibit.

how the prior art teaches "determining the optimal operation point." Therefore, even if this term required "determining the optimal operation point," my opinions would not change.

III. OPINION

A. Background of the Technology

40. In this section, I discuss the state of the art relevant to the subject matter of the '835 Patent, as would have been known, understood, and appreciated by a POSITA at the time of the alleged invention of the '835 Patent.

1. *Dynamic Random-Access Memory (DRAM)*

41. Dynamic random-access memory (DRAM) has been used for computer systems since the 1980s. Ex. 1008 at 2. By the 1990's, "the conventional DRAM interface started to become a performance bottleneck in high-performance as well as desktop systems" because the improvements of CPUs was outpacing the improvement of DRAM chips. *Id.* It was generally known that DRAM allows a computer system to perform processes by receiving and sending data. *Id.* at 1-2. It was also known that several DRAM chips could be attached to a printed circuit board (PCB) with associated circuitry to connect to the overall system. *Id.* at 1. *Stokes* explains that placing eight DRAM chips on a PCB "with a common address and data bus would make an 8-bit RAM module." Ex. 1009 at 2. Moreover, "design considerations for laying out a PCB" with DRAMs and other components

was discussed in the 1990s. Ex. 1010 at 50. An example of the architecture of a computer system, including a memory controller and DRAM chips, is shown in Figure 3 of *Jacob* replicated below.

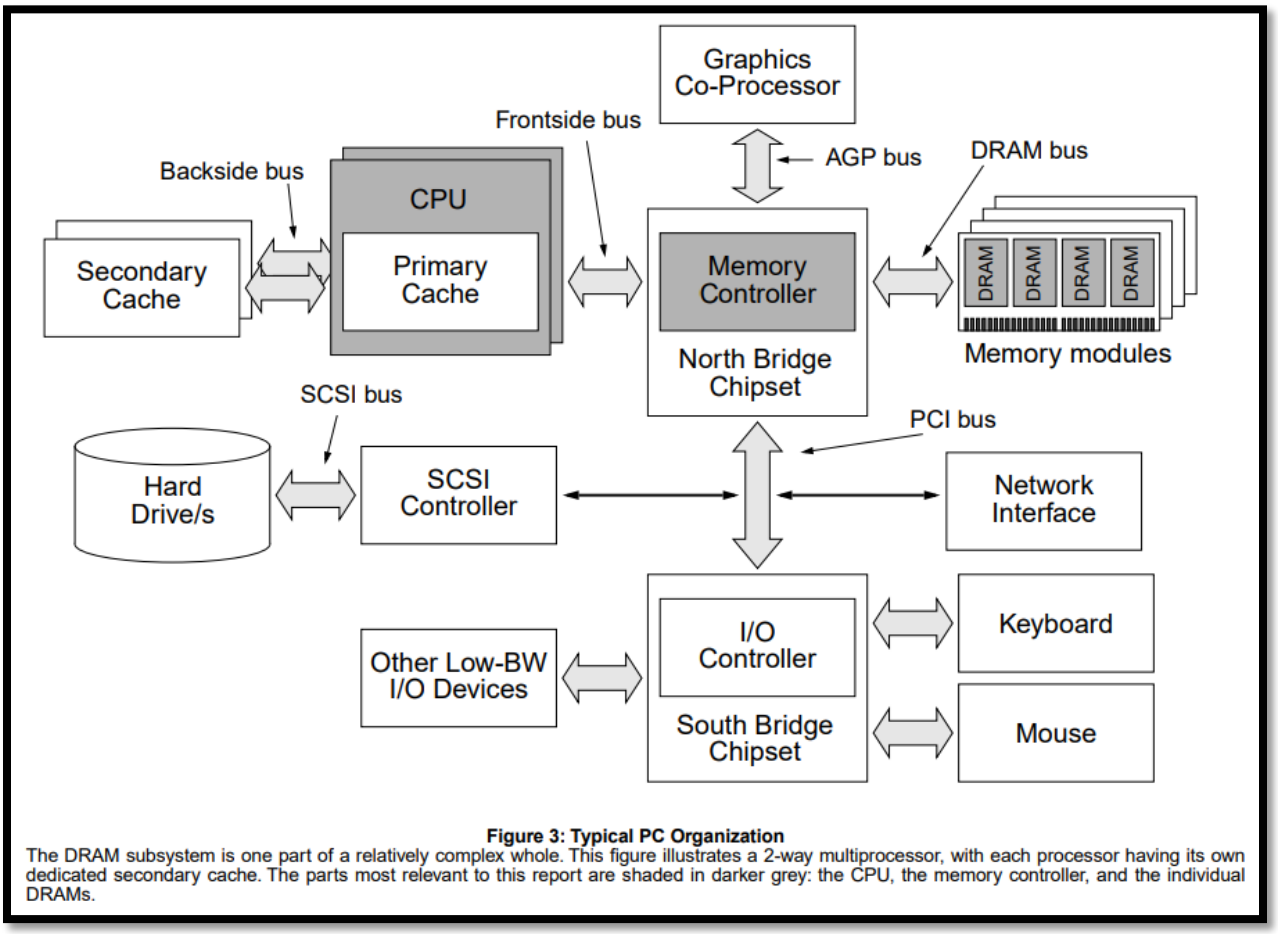


Figure 3: Typical PC Organization
The DRAM subsystem is one part of a relatively complex whole. This figure illustrates a 2-way multiprocessor, with each processor having its own dedicated secondary cache. The parts most relevant to this report are shaded in darker grey: the CPU, the memory controller, and the individual DRAMs.

Reproduced from *Jacob*

Ex. 1008 at 3.

42. The CPU of the system sends a transaction request to the memory controller, which then converts the transaction into command signals. *Id.* at 3-4. The command signals are sent to the DRAM chips, which first activate the

necessary data in the DRAM for the DRAM to then send the data to the memory controller. *Id.* The memory controller finally returns the data back to the CPU. *Id.* This process is shown in Figure 4 of *Jacob*, which I have provided below.

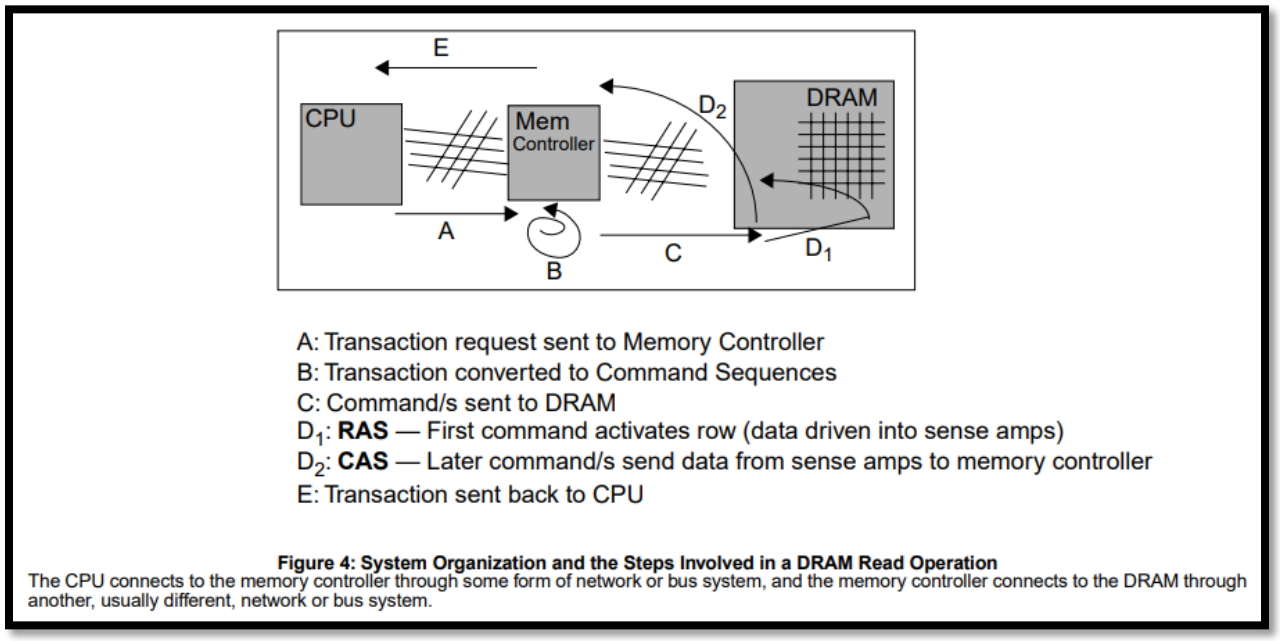


Figure 4: System Organization and the Steps Involved in a DRAM Read Operation
The CPU connects to the memory controller through some form of network or bus system, and the memory controller connects to the DRAM through another, usually different, network or bus system.

Reproduced from *Jacob*

Id. at 3.

43. DRAM chips were constantly evolving as the technology continued to improve. The gap between memory access time and processor speed was still growing early on. Ex. 1011 at 1. DRAM manufacturers, in response, created several DRAM architectures as an attempt to close that gap. *Id.* Some examples of DRAM architectures included Fast Page Mode, Extended Data Out, Synchronous, Enhanced Synchronous, Synchronous Link, Rambus, and Direct Rambus. *Id.* In general, the evolution of DRAM architecture went from "clocked to asynchronous

to fast page mode (FPM) to extended data-out (EDO) to burst-mode EDO (BEDO) to synchronous (SDRAM)" with the changes being largely structural in nature. Ex. 1008 at 5. SDRAM eventually transformed into double data rate (DDR) SDRAM, which provided a much higher (e.g., double) data rate. *Id.* at 7.

2. *DDR DRAM and SLDRAM*

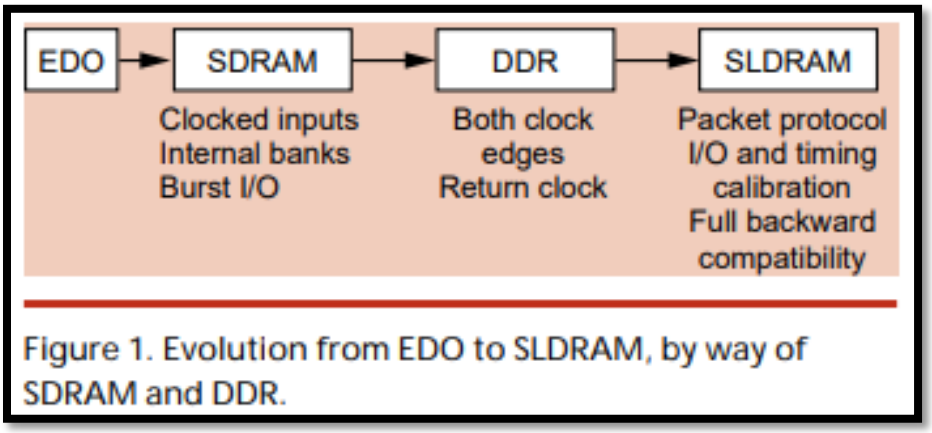
44. One architecture type that became widely adopted was DDR DRAM. DDR DRAM transfers data at both the rising edge and the falling edge of the clock unlike the previous single data rate SDRAM. Ex. 1008 at 7. Besides the double data rate aspect, "DDR DRAM are very similar to single data rate SDRAM in all other characteristics." *Id.* "They use the same signaling technology, the same interface specification, and the same pinouts on the DIMM carriers." *Id.* DDR SDRAM is a "type of DRAM that realizes twice the data transfer rate of conventional SDRAM[.]" Ex. 1012 at 10.

45. Additionally, DDR SDRAM includes an on-chip delay-locked loop (DLL), which "synchronizes the DRAM's outgoing data and DQS (data strobe) signals with the memory controller's global clock [JEDEC Standard 21-C, Section 3.11.6.6]." *Id.* at 11. "JEDEC uses an on-chip DLL in their DDR SDRAMs to ensure that data being driven onto the data bus is aligned with the global clock signal. The DLL does this by delaying the DRAM's response to a read request just long enough that the data is driven at the same time the DRAM sees the next clock

edge." *Id.* at 16. *Jacob* also explains that an alternative that "would have been available to the JEDEC community in the early to mid 1990's and would have been considered technically sound" included putting the DLL in the memory controller, or even using a Vernier method to measure and account for dynamic changes in skew. *Id.* at 20.

46. DDR SDRAM, because of its high data rate and easy operability, became successful quickly. For example, Hyundai, in March of 2001, estimated "the sales of DDR SDRAM could total US $380 million for [2001], equaling nearly 21% of the rapidly growing DDR market." Ex. 1013 at 2. Further, Hyundai expected "the adoption of DDR SDRAM begun by Compaq and Hewlett Packard will rapidly extend to other PC makers such [as] IBM, Gateway and Dell as well as major Taiwanese motherboard makers, boosting the need for the cutting-edge chip." *Id.*

47. Synchronous-link DRAM, or SLDRAM, was also a new memory interface specification. Ex. 1014 at 1. "SLDRAM meets the high data bandwidth requirements of emerging processor architectures and retains the low cost of earlier DRAM interface standards." *Id.* Because of this, it was thought that "SLDRAM will become the mainstream commodity memory of the early 21st century." *Id.* An example of the evolution from EDO to SLDRAM is shown in Figure 1 of *SLDRAM* below.



Reproduced from *SLDRAM*

Id. at 2.

48. SLDRAM builds on the features of SDRAM and DDR by "adding an address/control packet protocol, in-system timing and signaling optimization, and full compatibility from generation to generation." *Id.* at 1. Moreover, SDRAM, DDR, and SLDRAM "all use a DRAM core that has a page-mode cycle time of roughly 10 ns." *Id.* at 2. SLDRAM is able to keep system costs low by using conventional packaging and PCB technology, as many DRAM chips were used on PCBs. *Id.* at 3.

49. As *Cuppu* explains, SLDRAM was an adaption of RamLink and had its own IEEE standard. Ex. 1011 at 3. SLDRAM uses a "packet-based split request/response protocol." *Id.* However, SLDRAM designs have higher end-to-end transaction latencies when compared to SDRAM because they require "multiple narrow-bus cycles to complete a 128-bit transaction." *Id.* at 8. Even so,

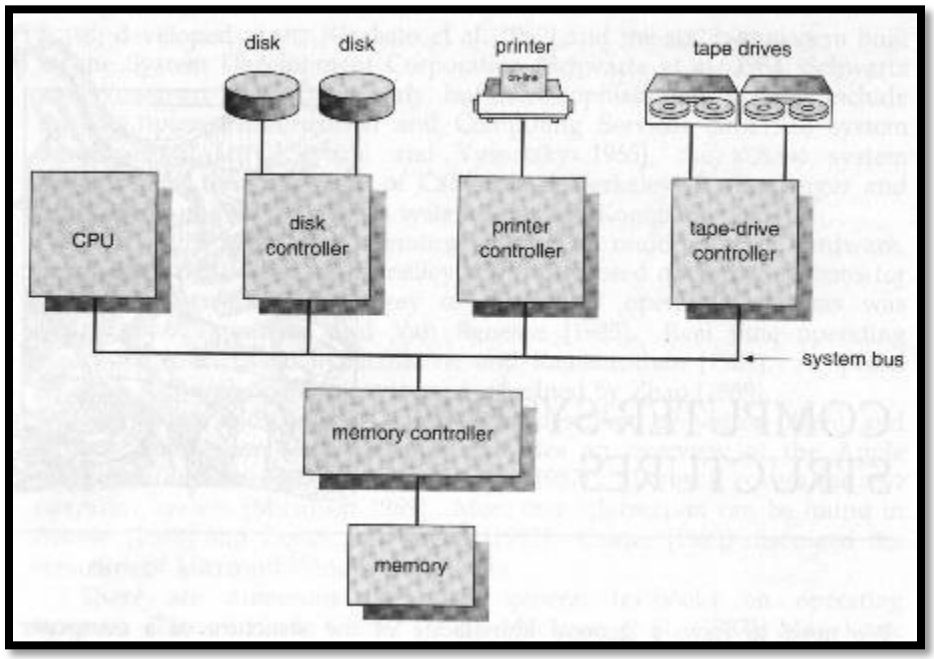
SLDRAM performs well and still has twice the number of data transfers as other DRAM architectures, similar to DDR DRAM. *Id.*

3. *Memory Controllers*

50. A memory controller is an important component for many memory systems. For example, a chipset that supports a CPU "usually contains several 'controllers' which govern how information travels between the processor and other components in the system." Ex. 1015 at 2. The memory controller is part of the chipset and "establishes the information flow between memory and CPU." *Id.* As I stated previously, a CPU, when data is needed from memory, will send out a request that is managed by the memory controller. *Id.* In turn, the memory controller "sends the request to memory and reports to the CPU when the information will be available for it to read." *Id.*

51. A memory controller leverages characteristics of DRAM to improve maximize memory performance. Ex. 1016 at 2. To do so, a memory controller can issue a command to the DRAM for a specific row activation or column access depending on the data requested by the CPU. *Id.* at 4. A computer system typically consists of "a CPU and a number of device controllers that are connected through a common bus that provides access to shared memory[.]" Ex. 1017 at 1. As the CPU and device controllers access the same memory, they can execute programs (e.g., a series of commands understood by the CPU) concurrently and compete for the

same memory. *Id.* A memory controller ensures orderly access to the RAM by "synchroniz[ing] access to the memory." *Id.* A figure from *Computer-System* illustrating a computer system is replicated below.



Reproduced from *Computer-System*

Id. at 1.

52. In SLDRAM systems, "[c]ommand, address, and control information from the memory controller flows to the SLDRAMs on the unidirectional CommandLink [and read] and write data flow between [the memory] controller and SLDRAM on the bidirectional DataLink." Ex. 1014 at 3. Write data is transmitted from the memory controller to the SLDRAMs while read data is transmitted form the SLDRAMs back to the memory controller. For example, an

SLDRAM "drives the read data on the data bus along with DCLK0 to provide the memory controller the necessary edges to strobe in read data." *Id.* at 4. Conversely, a write command causes the memory controller to drive "DCLK0 to strobe write data into [an] SLDRAM[.]" *Id.* Exemplary architecture of the SLDRAM bus topology is shown in Figure 3 of *SLDRAM*, which I have reproduced below.

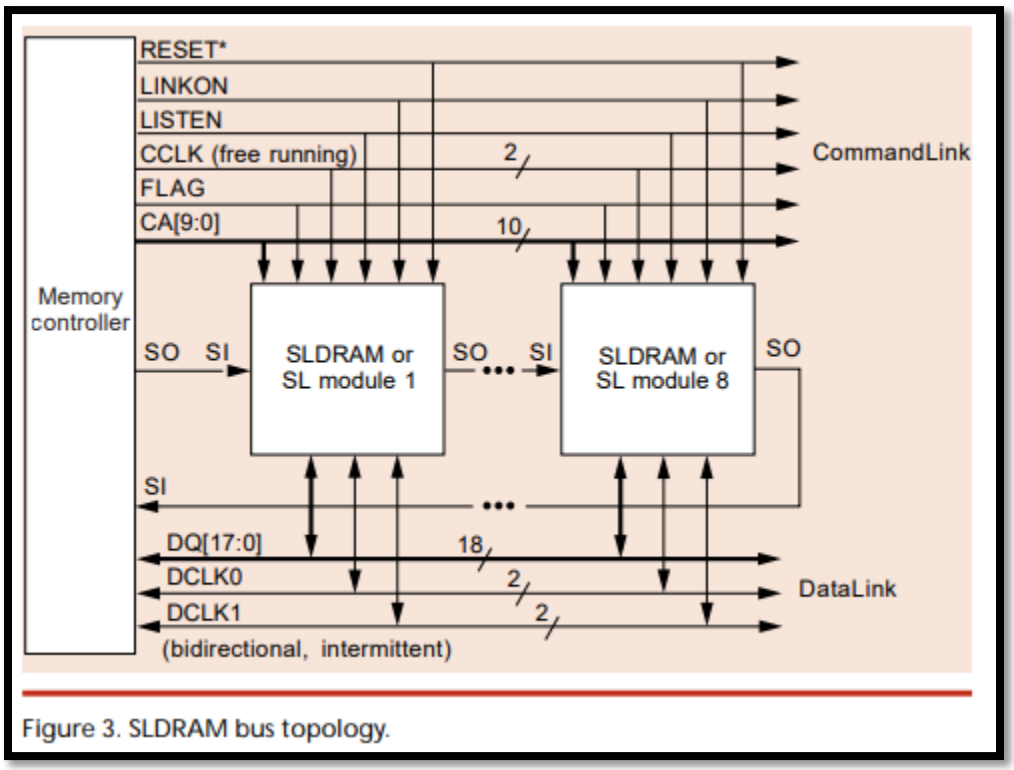
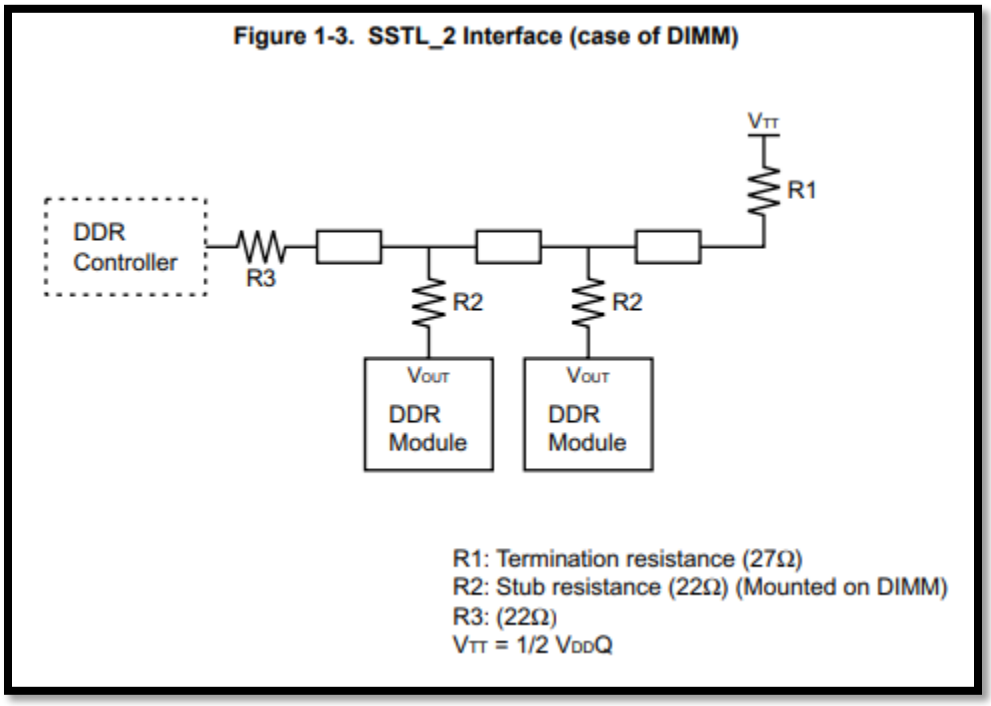


Figure 3. SLDRAM bus topology.

Reproduced from *SLDRAM*

Id. at 3.

53. A memory controller is similarly used in DDR DRAM systems, as shown in Figure 1-3 of *Elpida* below.



Reproduced from *Elpida*

Ex. 1012 at 14.

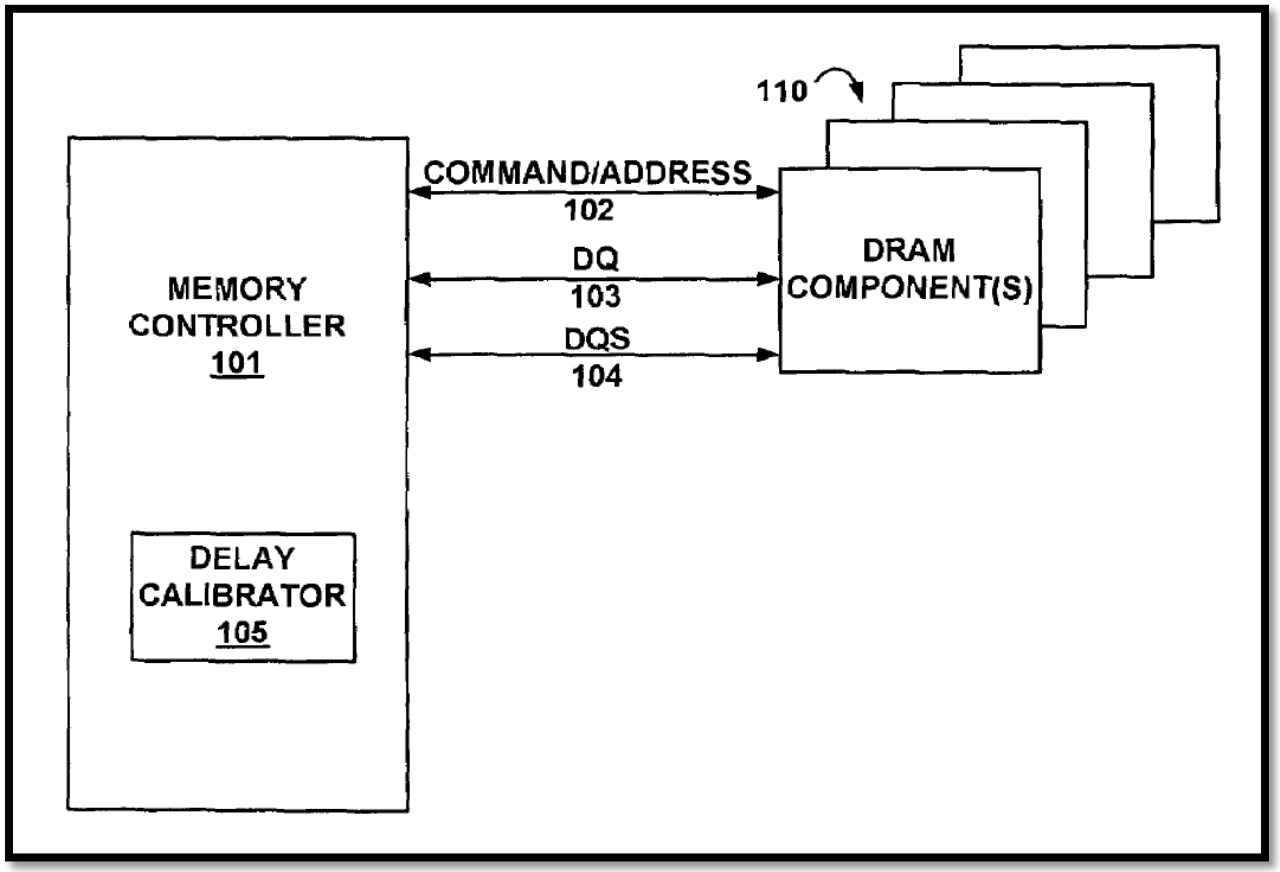
54. In DDR DRAM, data "is edge-aligned to DQS for read data and center-aligned for write data" which means "when [the memory] controller receives read data from DDR SDRAM, it will internally delay the received strobe to the center of the received data window." *Id.* at 65. "In the write cycle, the controller drives the data strobe signal (DQS), which is in synchronization with the clock (CK). DDR SDRAM captures the data (DQ) using DQS as a timing reference." *Id.* at 67. In some cases, a memory system would include a delay circuit to properly synchronize signals, such as data signals with clock signals,

which would use a coarse-to-fine estimation process for finding proper delay values. Ex. 1018 at 1; *see also infra* Section (III)(E)(13).

B. Overview of the '835 Patent

55. The '835 Patent describes methods and systems relating to input and output signaling for digital integrated circuit devices. Ex. 1001 at 1:9-10. The '835 Patent states that high performance memory devices require precise control of timing specifications for peak performance. *Id.* at 1:16-28. The '835 Patent purports to describe automatic calibration of intra-cycle timing relationships for sampling signals of an integrated circuit device. *Id.* at 1:34-37.

56. Figure 1 of the '835 Patent, reproduced below, shows a functional block diagram of a memory system according to an embodiment. *Id.* at 2:63-64.



Reproduced from the '835 Patent

Id. at 2.

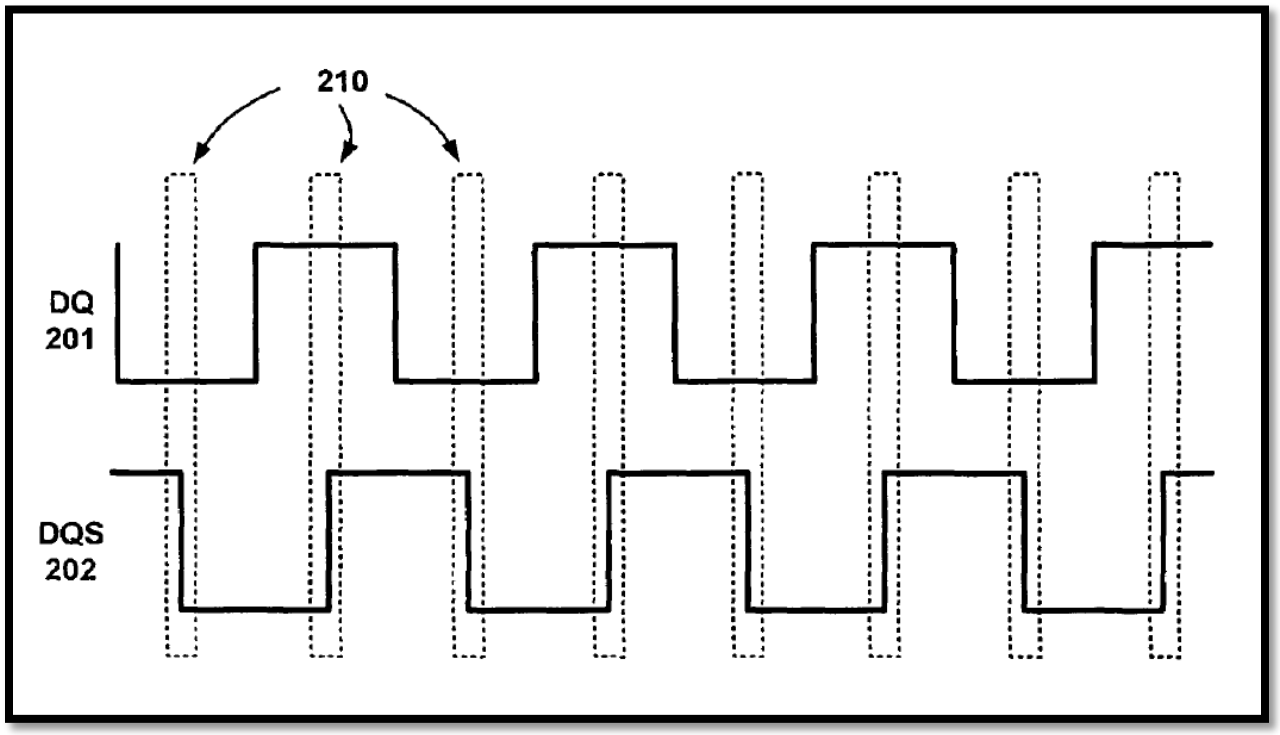
57. The memory system shown in Figure 1 includes a memory controller 101 having a delay calibrator 105. *Id.* at 3:1-2. The memory controller 101 is coupled to DRAM component(s) 110 via a command/address bus 102, a data bus ("DQ") 103, and a sampling signal bus ("DQS") 104. *Id.* at 1:65-2:2. The '835 Patent states that the memory system of Figure 1 "implements a method for automatically calibrating intra-cycle timing relationships between command signals of the command/address bus 102, data signals of the DQ bus 103, and

sampling signals of the DQS bus 104." *Id.* at 3:3-6. The '835 Patent further states that "each of the DRAM components 110 comprise the integrated circuit device for which the calibration adjustments are performed," and that the memory controller 101 performs the adjusting. *Id.* at 3:6-9.

58. The '835 Patent explains that intra-cycle relationships between command/address signals, DQ signals, and DQS signals are calibrated to optimize operation of the system. *Id.* at 3:13-16. In particular, the '835 Patent states that the DQ signals targeted by the calibration include signals that convey data in both the read direction (from DRAM components 110 to memory controller 101) and write direction (from memory controller 101 to DRAM components 110). *Id.* at 3:19-24.

59. The '835 Patent describes the relative timing of signals in the system with reference to Figures 2 and 3. Timing diagram 200 of Figure 2 illustrates a DQ signal 201 and a DQS signal 202 during a write transaction while timing diagram 300 of Figure 3 illustrates a DQ signal 301 and a DQS signal 302 during a read transaction. *Id.* at 4:40-41; 4:53-54. In both cases, the signals must adhere to specific timing requirements. For example, the rising and falling edges of DQS signal 202 must be "accurately placed at the center of the rise-and-hold times of DQ 201 as shown (e.g., phase shifted 90°)" as the sampling windows 210 correspond to the rising and falling edges of DQS signal 202. *Id.* at 4:42-47. Figure

2 of the '835 Patent shows the rising and falling edges of DQS signal 202 centered to rise-and-hold times of DQ signal 201:

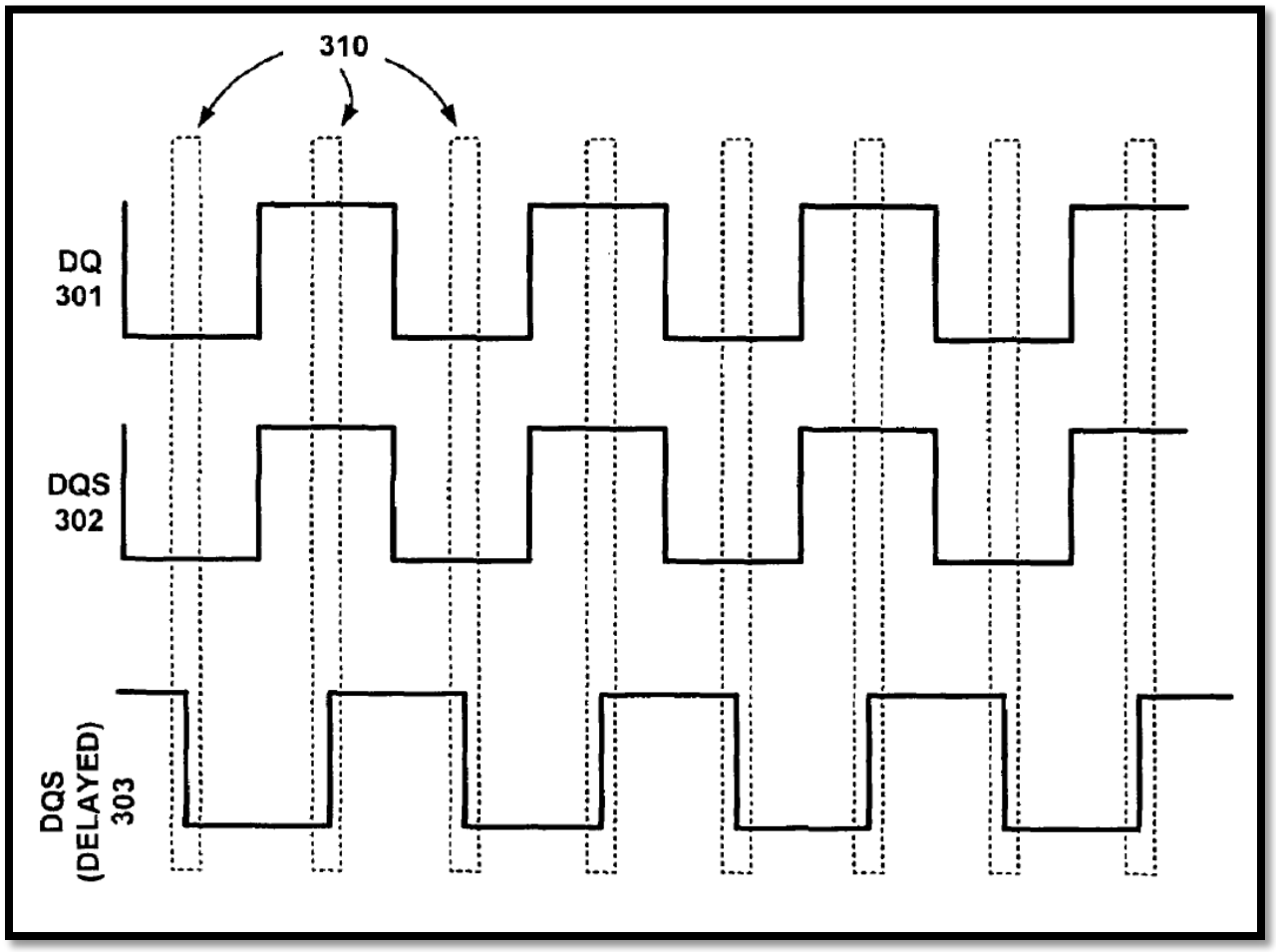


Reproduced from the '835 Patent

Id. at 3.

60. Figure 3 depicts an example in which the DQS signal is adjusted during a read transaction. The "rising and falling edges of DQS 302 need[] to be accurately aligned with the rising and falling edges of the DQ signal 301." *Id.* at 4:56-58. To align DQS signal 302, a 90° phase shift is performed by the memory controller to "place the sampling windows 310 at the center of the rise-and-hold times of DQ 301 (e.g., shown as DQS delayed 303)." *Id.* at 4:59-61. Figure 3 of the

'835 Patent shows the rising and falling edges of DQS signal 303, with the 90° phase shift, centered to rise-and-hold times of DQ signal 301:



Reproduced from the '835 Patent

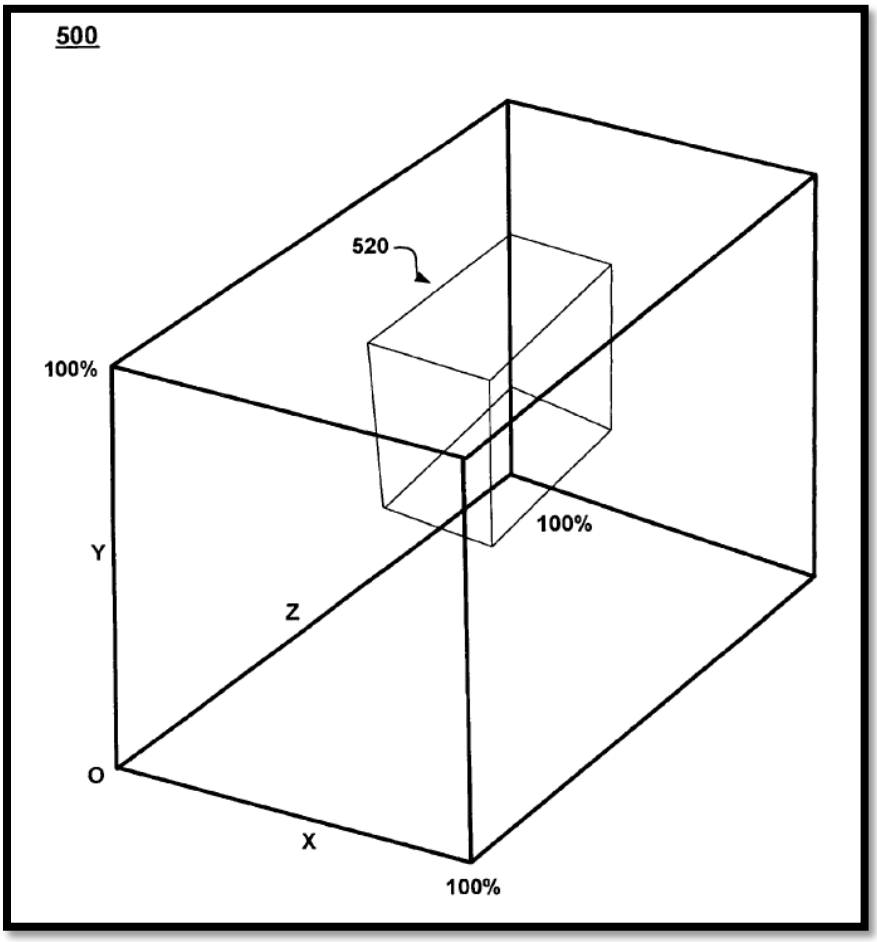
Id. at 4.

61. The '835 Patent states that the "available margin" of the sampling window is impacted by multiple factors, including "signal noise, crosstalk, skew, jitter, and drift effects brought on by voltage and thermal variations." *Id.* at 4:66-5:1. Certain timing specifications, like those for DDR, can be so stringent that

slight variations of system parts which can cause a degradation of overall performance. *Id.* at 3:53-55. The '835 Patent purports to add margin to sampling windows, allowing for more variability in the system while continuing to perform optimally. *Id.* at 3:49-51. "The extra margin provided by the embodiments of the present invention increase the reliability rate of computer systems incorporating such high performance integrated circuit devices … [and] can be used to increase the maximum obtainable performance of such computer systems." *Id.* at 3:58-64.

62. The '835 Patent asserts that optimal operation of DRAM components is achieved by calibrating intra-cycle timing relationships between command/address signals, DQ, signals, and DQS signals. *Id.* at 3:13-16. The calibration includes "generating command signals and address signals for accessing the DRAM components (e.g., DRAM chips of a memory module)[,] … accessing data signals (e.g., DQ signals) that convey data for the DRAM components, in both a data read transaction (e.g., data driven from the DRAM components 110 to the memory controller 101) and a data write transaction (e.g., data driven from the memory controller 101 to the DRAM components 110)[, and] … accessing sampling signals (e.g., DQS signals) for controlling the sampling of the data signals." *Id.* at 3:16-27. A phase relationship between the command, data, and sampling signals is then automatically adjusted for calibration. *Id.* at 3:27-29.

63. The '835 Patent states that embodiments of the alleged invention "search for and find the valid region of operation within the configuration space without requiring knowledge, a-priori, where the valid region is." *Id.* at 4:10-13. The '835 Patent characterizes the "valid region" as a three-dimensional space defined by "x, y, and z parameters (e.g., the intra-cycle command/address phase, DQ phase, and DQS phase)." *Id.* at 5:34-48. The '835 Patent states that the intra-cycle parameters are automatically altered to find the boundaries of a valid region of operation. *Id.* at 5:45-48. Once the boundaries are found, configuration choices are made to find the optimal operating point. *Id.* at 5:48-51. Figure 5 depicts a "valid region" 520 within a three-dimensional space defined by x, y, and z parameters, which I have reproduced below.



Reproduced from the '835 Patent

Id. at 6.

64. The '835 Patent states that coarse calibration and fine calibration can be used to find a "valid region." *Id.* at 5:54-58. Large step increments are used in the coarse calibration method to vary the parameters. *Id.* at 5:59-61. The coarse calibration method can be configured to simultaneously vary the parameters. *Id.* at 5:61-64. The coarse calibration can be performed quickly to determine the general region of valid operation, if any exists, for a given device. *Id.* at 6:8-9.

65. Small step increments, on the other hand, are used in the fine calibration method. *Id.* at 6:1-3. The fine calibration method varies parameters individually, instead of simultaneously. *Id.* at 6:3-5. The '835 Patent states that parameters are varied individually because "stable points for the aggregate are known," and the other variables can be left unvaried. *Id.* at 6:5-6. The fine calibration method can be used to determine a specific "best operating point" within the valid region of a device. *Id.* at 6:10-11. To find the valid region and the parameter values for optimization, "the device (e.g., a DDR DRAM) is stimulated by writing test data to the DRAM and then reading the test data" as the "presence of errors in the read test data indicates one or more of the parameters is out of alignment." *Id.* at 6:12-15.

C. Overview of the '835 Patent's File History

66. I have reviewed the file history of the application that issued as the '835 Patent. The '835 Patent was filed as Application No. 10/716,320 ("'320 application") on November 17, 2003. While the claims originally-filed in the '320 application and the Challenged Claims of the '835 Patent have some overlap in scope, there are significant differences between them. Compare Ex. 1003 at 342-347, with Ex. 1001 at 6:56-10:4.

67. In a first Office Action dated January 8, 2007, all pending claims were rejected over prior art. Ex. 1003 at 293-303. The claims were rejected over U.S.

Patent No. 6,553,472 ("Yang") or rejected over Yang in view of U.S. Patent Publication No. 2004/0160833 ("Suzuki"), U.S. Patent No. 6,016,282 ("Keeth"), and/or U.S. Patent No. 5,781,766 ("Davis"). *Id.*

68. In a response dated June 11, 2007, Patent Owner did not amend any of the claims. *Id.* at 279-285. In the remarks, Patent Owner argued that Yang does not disclose "automatic calibration" of cycle timing relationships, but instead discloses "programming clock delays, command delays, read command parameter delays, and write command parameter delays of a memory controller." *Id.* at 286-287 (emphasis in original).

69. In a Final Office Action dated September 6, 2007, all pending claims were again rejected over the same prior art. *Id.* at 257-269.

70. In a response dated October 30, 2007, Patent Owner canceled claim 21 and amended all independent claims 1, 7, 12, 18, and 22. *Id.* at 241-247. Patent Owner also filed a Request for Continued Examination ("RCE"). *Id.* at 237-239. In the remarks, Patent Owner again argued that "a process requiring user input, or a process requiring a programmer to set initial parameters of multiple signals for the device is not automatically calibrating[.]" *Id.* at 248 (emphasis in original). Patent Owner further explained that the amended claims "specifically recite the automatic adjusting of the claimed invention is free of user input." *Id.*

71. The next Office Action received on January 25, 2008, again rejected all pending claims over the same prior art combined with newly cited U.S. Patent Publication No. 2003/0122696 ("Johnson"). *Id.* at 216.

72. In a response dated April 25, 2008, Patent Owner amended all of the independent claims. *Id.* at 196-202. In remarks, Patent Owner argued that the cited prior art reference does not disclose both "the phase relationship adjusting process is accomplished" and "[t]he calibration of the intra-cycle timing relationships is executed" for "both data write transactions and data read transactions." *Id.* at 204. The Patent Owner further reiterated "a process requiring user input, or a process requiring a programmer to set initial parameters of multiple signals for the device is not automatically calibrating[.]" *Id.* (emphasis in original).

73. In a Final Office Action dated July 23, 2008, all pending claims were again rejected over the same prior art as cited in the previous Office Action. *Id.* at 167-180.

74. In a response dated October 23, 2008, Patent Owner added claims 23 and 24. *Id.* at 151-152. Patent Owner also filed an RCE. *Id.* at 141-142. In the remarks, Patent Owner reiterated, once again, that the prior art does not teach automatically calibrating/adjusting. *Id.* at 154-158.

75. In a non-final Office Action dated December 12, 2008, all pending claims were again rejected over the same prior art in view of U.S. Patent Publication No. 2002/0078316 ("Nakamura"). *Id.* at 108-122.

76. In a response dated March 12, 2009, claims 23 and 24 were cancelled, claims 25 and 26 were added, and all independent claims were amended. *Id.* at 89-97. In the remarks, Patent Owner argued the prior art fails to teach "systematically altering respective phase shifts of the command, data, and sampling signals to determine a valid operation range of the integrated device." *Id.* at 100 (emphasis in original). Patent Owner further explained that the prior art "discloses achieving sampling or timing calibration by determining an optimal delay for the command signals and the data signals, whereas claim 1 recites the determination of the valid range of the integrated circuit device by systemically altering the phase shift of the sampling signals as well as the phase shift of the command signal an the phase shift of the data signal, as claimed." *Id.*

77. A Notice of Allowance was subsequently issued on May 14, 2009. *Id.* at 65. The Notice of Allowance stated that the pending claims were allowable because "related references do not disclose altering inter-cycle timing relationships between signals by altering a phase shift of command signals, a phase shift of data signals, and a phase shift of sampling to determine a valid operation range of an integrated circuit device[.]" *Id.* at 69.

D. Summary of the Prior Art References

1. *Johnson (Ex. 1004)*

78. U.S. Patent No. 6,434,081 ("*Johnson*") was filed on May 12, 2000 and issued on August 13, 2002. Ex. 1004 at 1. *Johnson* lists Brian Johnson and Brent Keeth as the inventors and lists Micron Technology, Inc. as Assignee. *Id.* at 1. *Johnson* is titled "Calibration Technique for Memory Devices." *Id.* at 1.

79. *Johnson* discloses a calibration technique that "provides correct alignment of data entering a memory module, e.g., an SLDRAM module, on a plurality of incoming data paths in both a serial and parallel direction." *Id.* at 2:45-48. Data paths are calibrated relative to a clock signal to produce properly aligned bits. *Id.* at Abstract. *Johnson* explains that memory devices are constantly improved including memory devices such as dynamic random access memory (DRAM), synchronous DRAM (SDRAM), double data rate SDRAM (DDR SDRAM), and SyncLink dynamic random access memory (SLDRAM). *Id.* at 1:11-20. *Johnson* focuses on SLDRAM, which is "a double data rate device which uses both the positive- and negative-going edges of a clock cycle to READ and WRITE data to the memory cells and to receive command and FLAG data from a memory controller." *Id.* at 1:26-30. An SLDRAM is shown in FIG. 3, which I have replicated below.

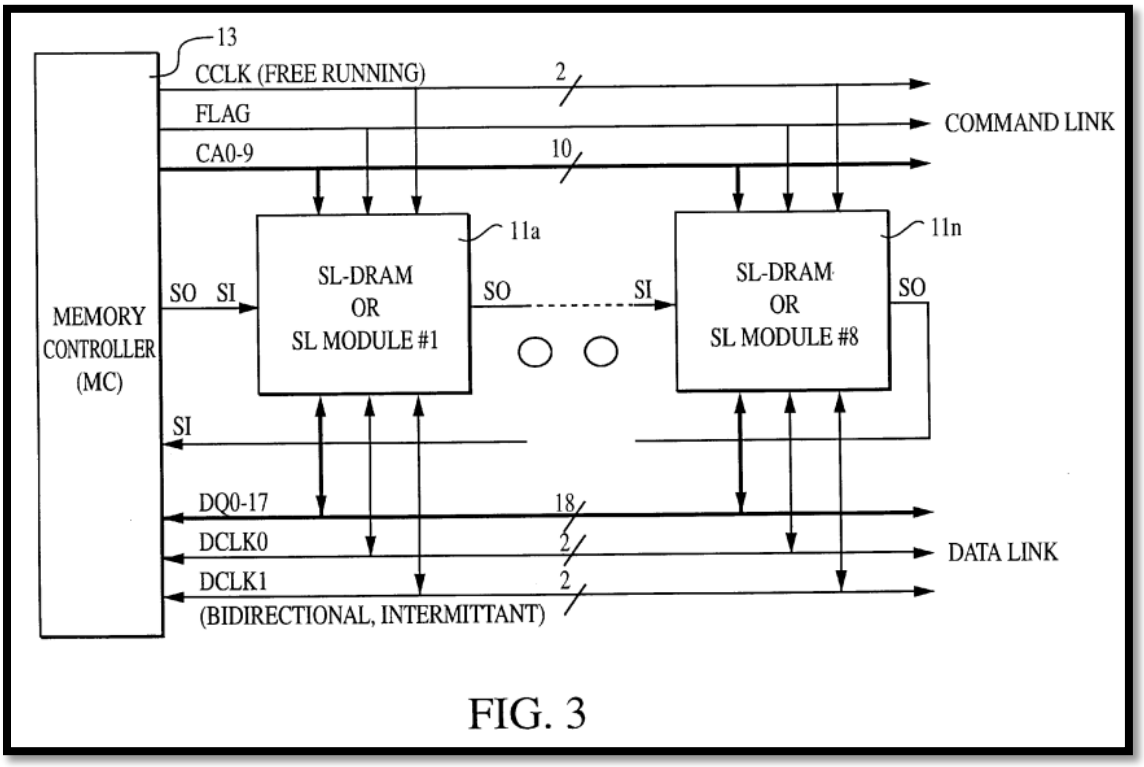


FIG. 3

Reproduced from *Johnson*

Id. at 3.

80. SLDRAM modules 11a-11n are "accessed and controlled" by the memory controller 13. *Id.* at 3:31-33. A command link that includes a clock signal CCLK, a FLAG data path, and a 10 bit command bus path CA0-9 is provided by the memory controller 13 to each of the SLDRAM modules 11a-11n. *Id.* at 3:33-38. Additionally, "a bi-directional data bus DQO-17 is provided between memory controller 13 and each of the SLDRAM modules 11a … 11n, as are bi-directional data clocks DCLK0 and DCLK1." *Id.* at 3:41-44. DCLK0 strobes input and output

data into and out of the SLDRAM modules 11a-11n. *Id.* at 3:44-45. FIG. 4, reproduced below, shows the circuitry of the SLDRAM modules 11a-11n.

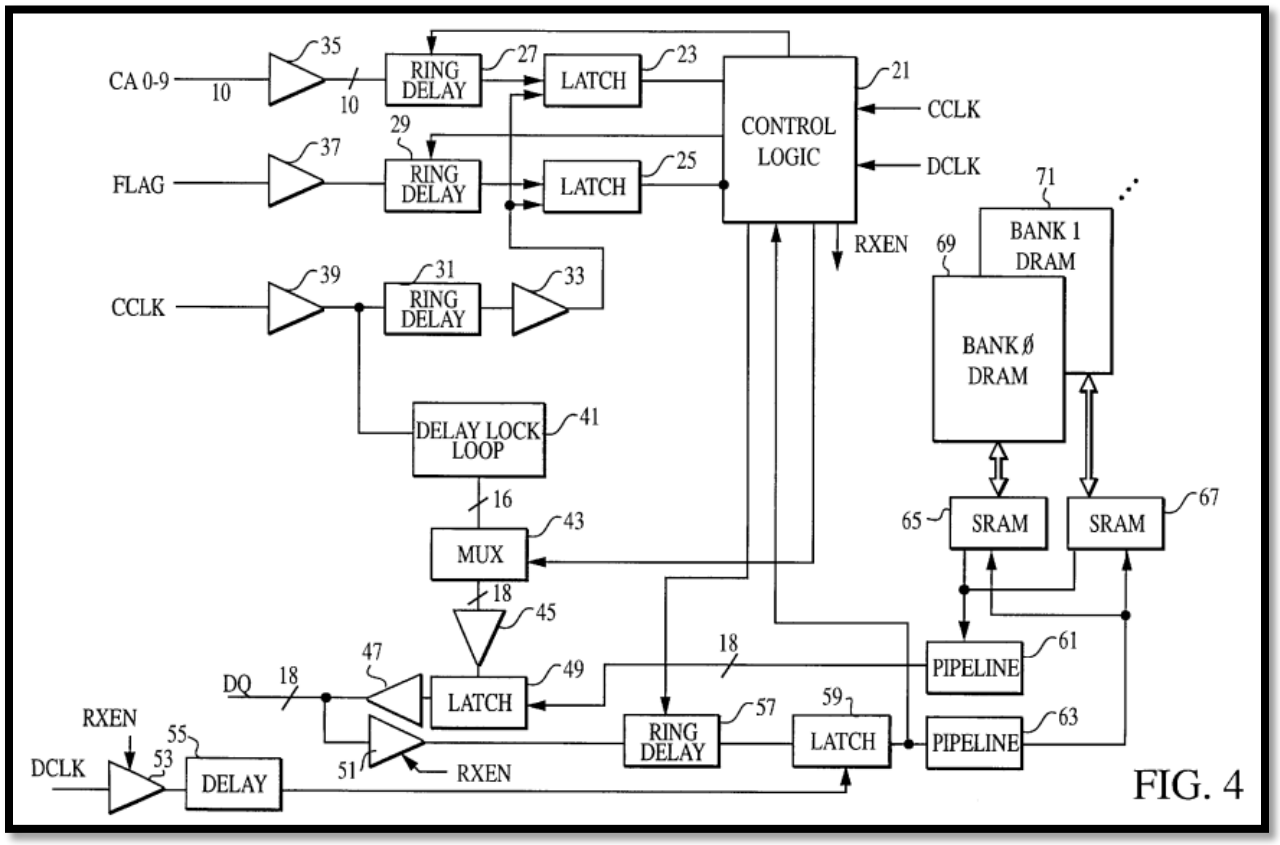


FIG. 4

Reproduced from *Johnson*

Id. at 4.

81. The control logic circuit 21 "receives and analyzes commands on the CA0-9 bus" and also receives the clock signals CCLK and DCLK. *Id.* at 3:57-62. As part of the alignment process, *Johnson* explains that signals "on each of the command bus paths CA0-9 are passed through respective adjustable ring delay circuits 27 and into respective latches 23 where the signals are latched by a CCLK

signal, as buffered by buffer 39, delayed by delay 31 and buffered by buffer 33." *Id.* at 3:63-67.

82. CCLK passes from buffer 39 into delay lock loop 41 and "provides 16 clock signals into a multiplexer 43" which subsequently provides "18 clock output signals through respective buffers 45 to 18 latches 49 which latch data output from the memory banks 69, 71." *Id.* at 4:2-5. Memory controller 13 supplies the data on DQ data bus to the memory banks 69 and 71 and is "passed through gated buffers 51 through ring delays 57 on each path of the data bus, into latches 59, through pipeline circuit 63." *Id.* at 4:14-16. DCLK passes through gated buffer 53 and delay circuit 55 and is used to control latch 59 to latch in incoming data on the data bus DQ. *Id.* at 4:24-26.

83. To "ensure proper timing of the various memory operations performed by the SLDRAM modules 11a … 11n, the FIG. 4 circuit must be synchronized to ensure that the incoming data is properly clocked in by the clock signals CCLK and DCLK." *Id.* at 4:27-31. *Johnson* describes a 2^N bit synchronizing pattern is applied to each of the data input paths CA0-9. *Id.* at 4:33-34. FIG. 5 shows a timing diagram between CLCK, FLAG, CA0-9, DQ, and DCLK, which I have provided below.

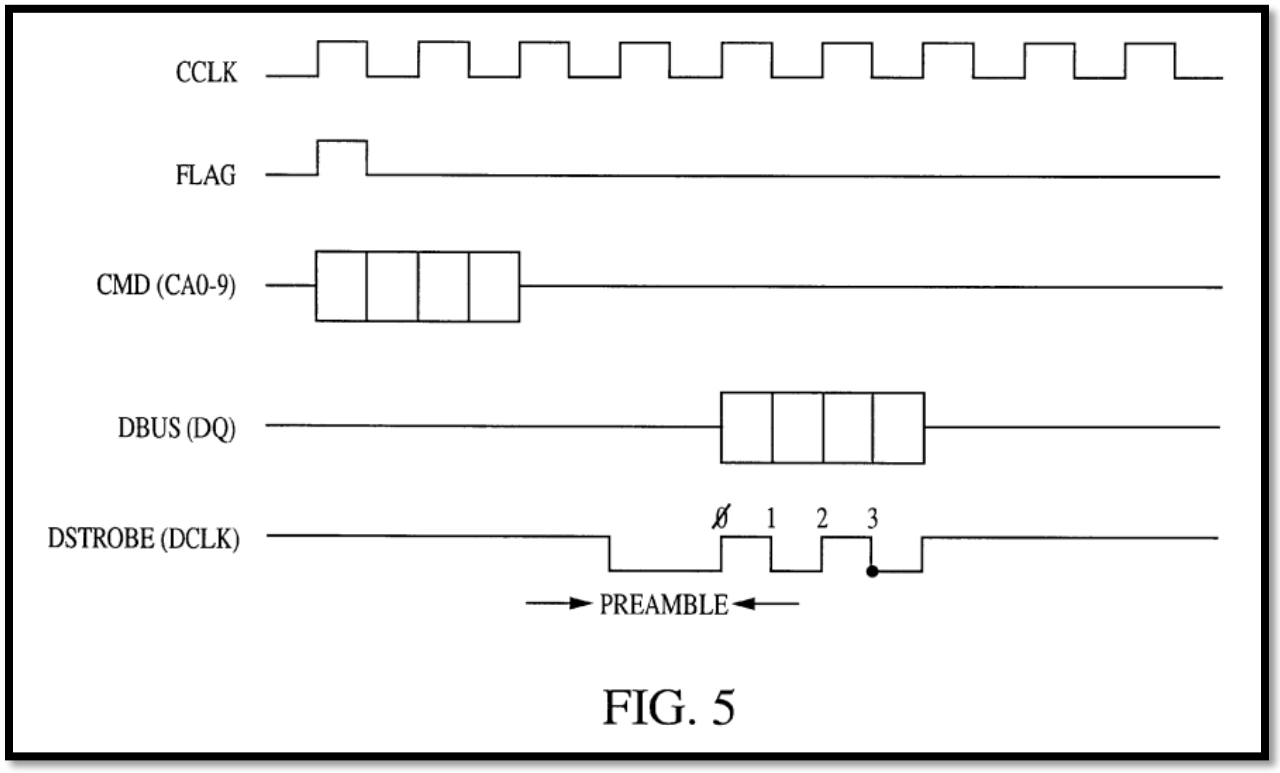


FIG. 5

Reproduced from *Johnson*

Id. at 5.

84. Bits of data on the DQ path of the data bus are clocked in sequential transitions of the data clock signal DCLK while the data on each of the command signal paths CA0-9 is clocked in sequential transitions of the command clock signal CCLK. *Id.* at 4:63-5:3. *Johnson* shows a part of the alignment process for the command signal paths in FIG. 9 replicated below.

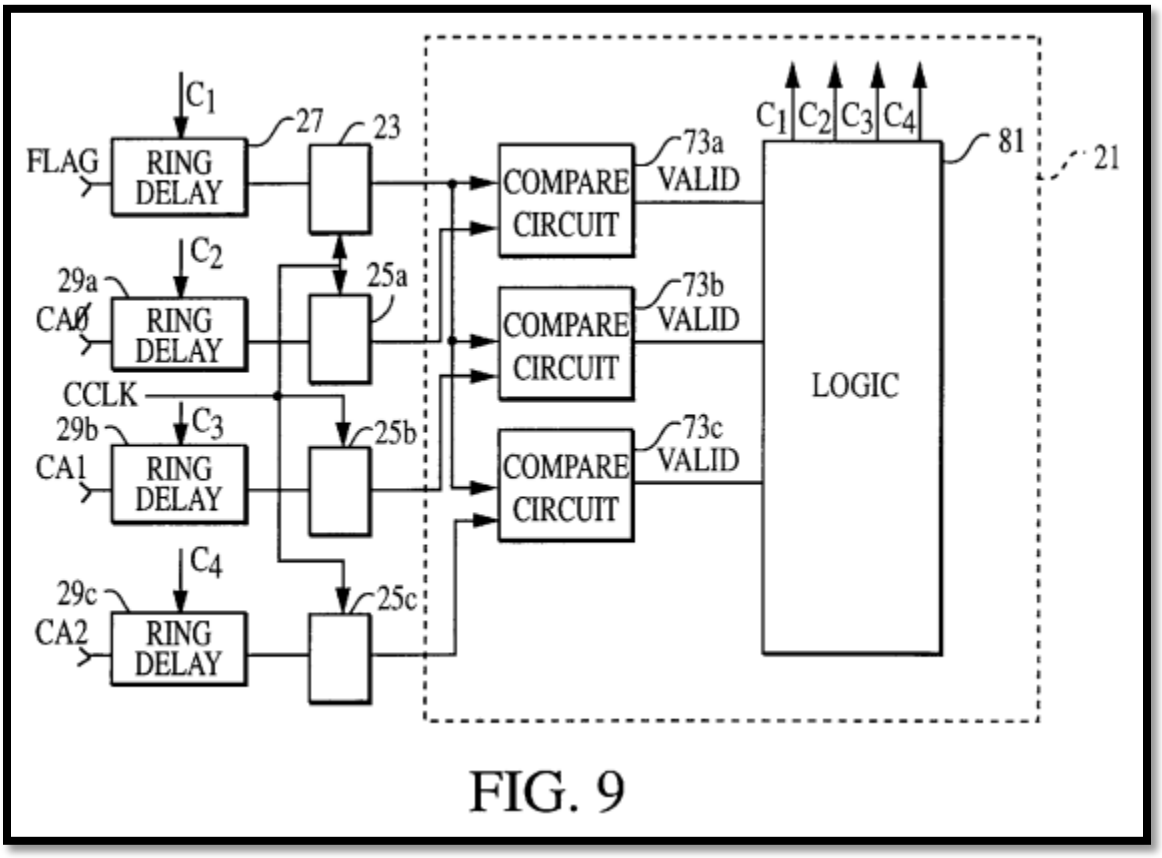


FIG. 9

Reproduced from *Johnson*

Id. at 7.

85. Via ring delays and compare circuits, the control logic circuit aligns the CA0-9 data paths to the CCLK signal while the DQ0-17 data paths are aligned to the DCLK signal. *Id.* at 6:42-54. "VALID signals are generated by the compare circuits 73a, 73b, 73c to signal whether the synchronization pattern is properly recognized to the logic 81." *Id.* A part of the alignment process for the data signal paths is shown in FIG. 10 below.

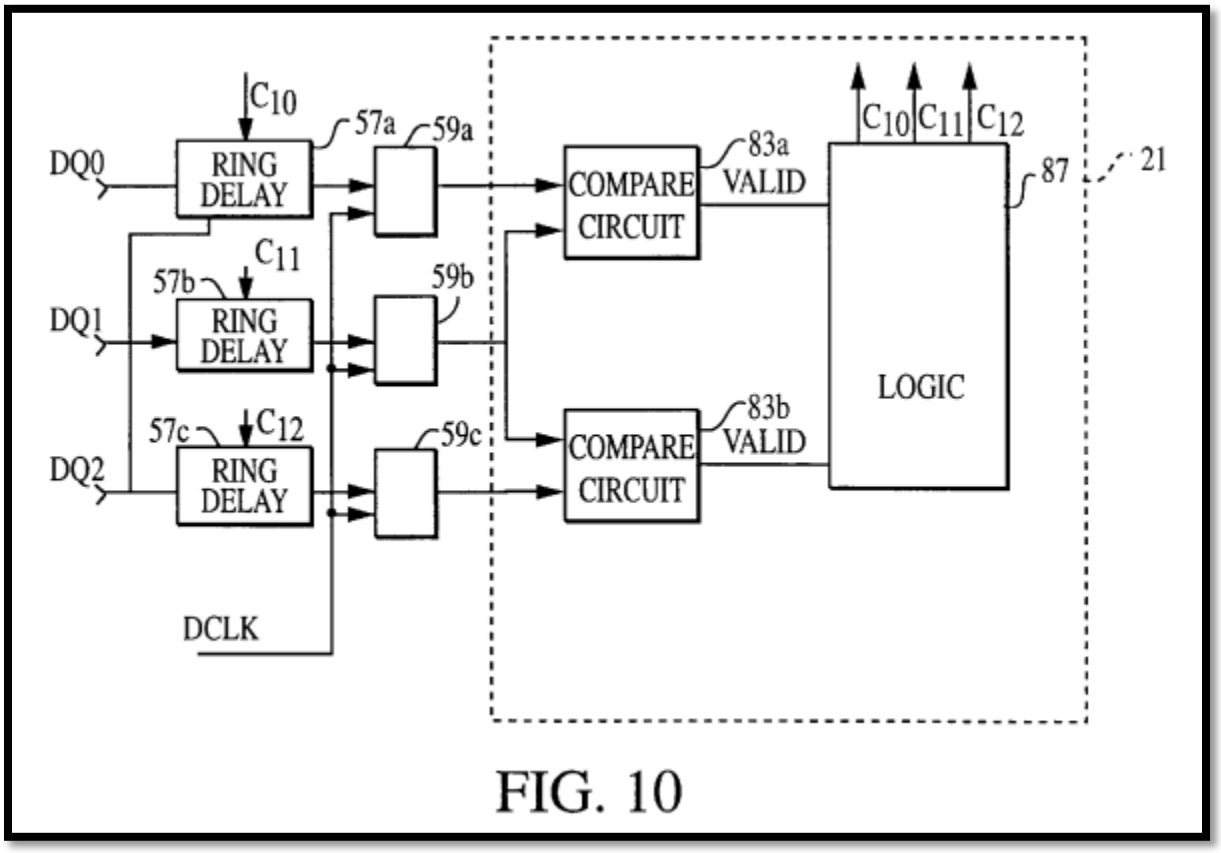


FIG. 10

Reproduced from *Johnson*

Id. at 7.

2. *Jeddeloh (Ex. 1005)*

86. U.S. Patent No. 6,629,222 ("*Jeddeloh*") was filed on July 13, 1999 and issued on September 30, 2003. Ex. 1005 at 1. *Jeddeloh* lists Joseph Jeddeloh as the sole inventor and lists Micron Technology, Inc. as Assignee. *Id.* at 1. *Jeddeloh* is titled "Apparatus for Synchronizing Strobe and Data Signals Received from a RAM." *Id.* at 1.

87. *Jeddeloh* is directed to "an apparatus that synchronizes a data signal and a data strobe signal received from a random access memory." *Id.* at Abstract. Specifically, a first programmable delay circuit is coupled "to an enable input of the input driver in order to synchronize the driving of the input driver with the data signal received from the random access memory" and a second programmable delay circuit is coupled "between the data strobe signal and a clock input of the register" to delay the data strobe signal to synchronize with the data signal. *Id.* *Jeddeloh* focuses on DDR memory devices that can be implemented in a computer system as seen in FIG. 1 replicated below.

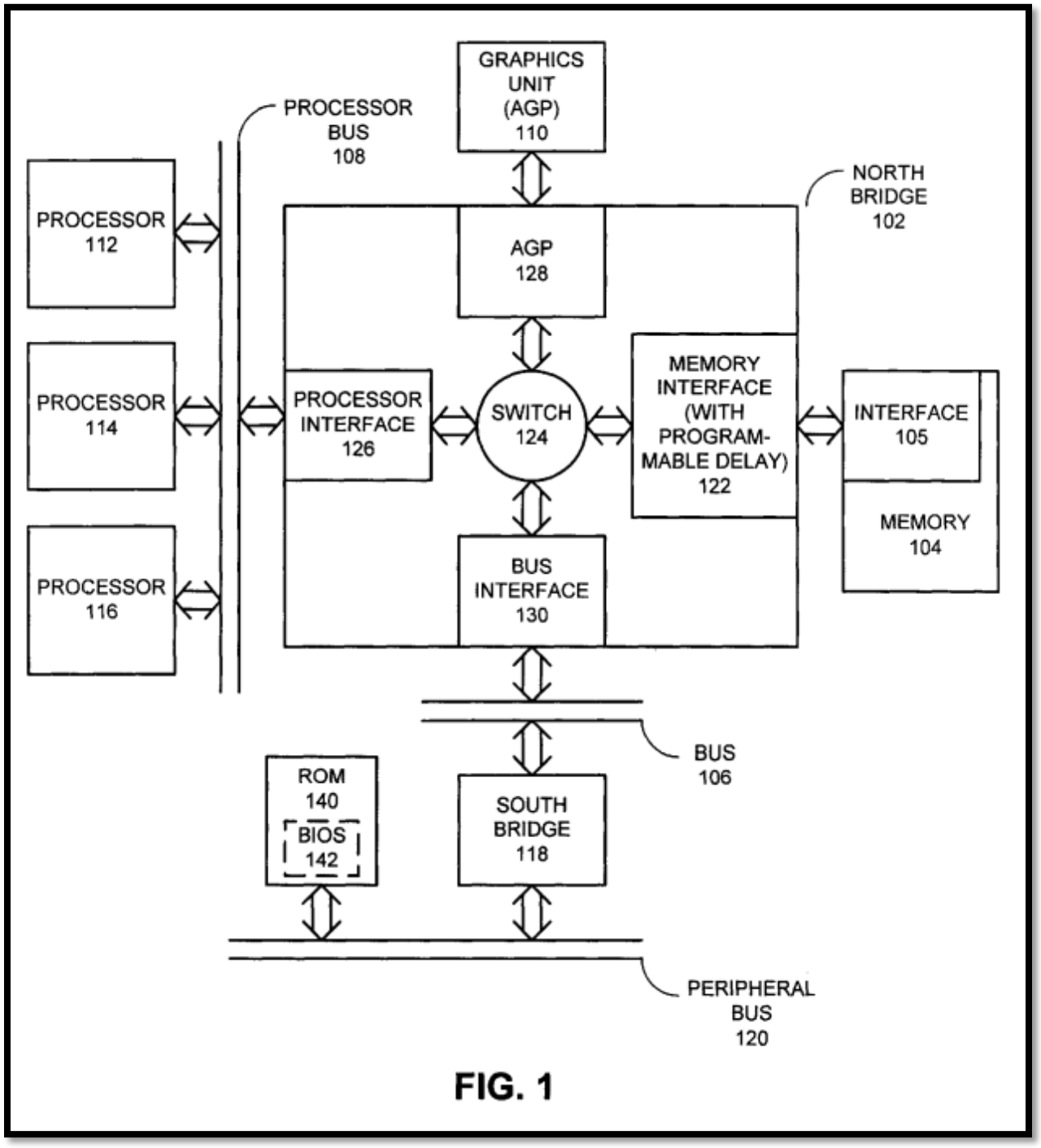


FIG. 1

Reproduced from *Jeddeloh*

Id. at 2.

88. The memory 104 is a type of memory with a clocked interface that "returns data along with a strobe signal for latching the data during read operations" such as "memory implementing the DDR interface standard." *Id.* at 3:52-55. Memory 104 interacts with memory interface 122 that includes the programmable delay circuitry for aligning memory reference signals. *Id.* at 3:58-63. The internal structure of memory interface 122, e.g., the memory controller, is shown in replicated FIG. 2 below.

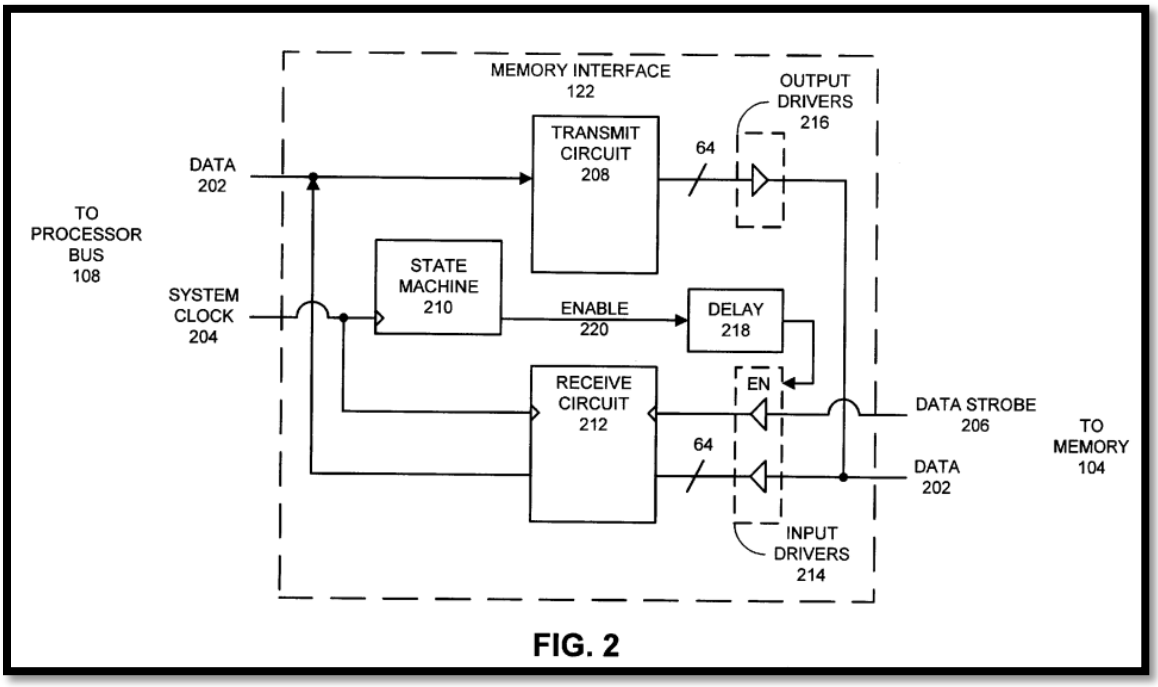


FIG. 2

Reproduced from *Jeddeloh*

Id. at 3.

89. Memory interface 122 includes, among other circuitry, receive circuit 212 and delay 218 and receives data signal 202 and data strobe signal 206 from the

memory 104 while being coupled to data signal 202 and the system clock 204. *Id.* at 4:38-42. Data is transmitted to memory 104 during a write operation and receive data from memory 104 during a read operation. *Id.* at 4:43-46. During a read operation, "data signal 202 and data strobe signal 206 from memory 104 passes through input drivers 214 into receive circuit 212" that includes "circuitry to transfer data signal 202 from the clock domain of data strobe signal 206 into the clock domain of system clock 204." *Id.* at 4:54-59. Data signal 202 is clocked by data strobe signal 206 and enable signal 220 passes through delay circuit 218 to assist with the alignment process. *Id.* at 5:1-3. The circuitry of receive circuit 212 is shown in FIG. 3, which I have reproduced below.

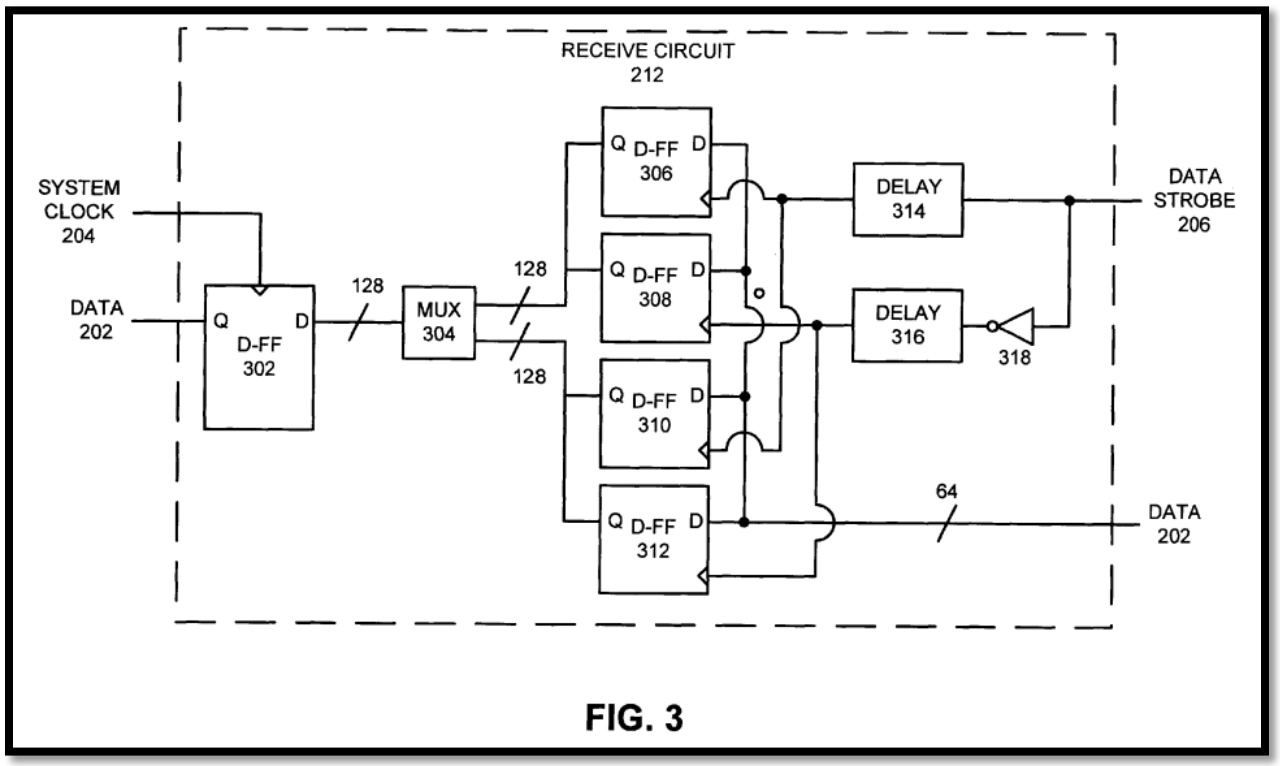


FIG. 3

Reproduced from *Jeddeloh*

Id. at 4.

90. The receive circuit 212 receives data signal 202, which feeds into D-flip-flops (D-FFs), and data strobe signal 206, which feeds into clock inputs of the D-flip-flops. *Id.* at 5:16-23. The data strobe signal 206 is used to latch data signal 202 each of the D-flip-flops. *Id.* at 5:23-25. Data strobe signal 206 also passes through delay circuits 314 and 316 where "D-FFs 306 and 310 are clocked on the rising edge of data strobe signal 206, while D-FFs 308 and 312 are clocked on the falling edge of data strobe signal 206." *Id.* at 5:28-31. A general programmable delay circuit, such as delay circuit 218, delay circuit 314, or delay circuit 316, is shown in FIG. 4 below.

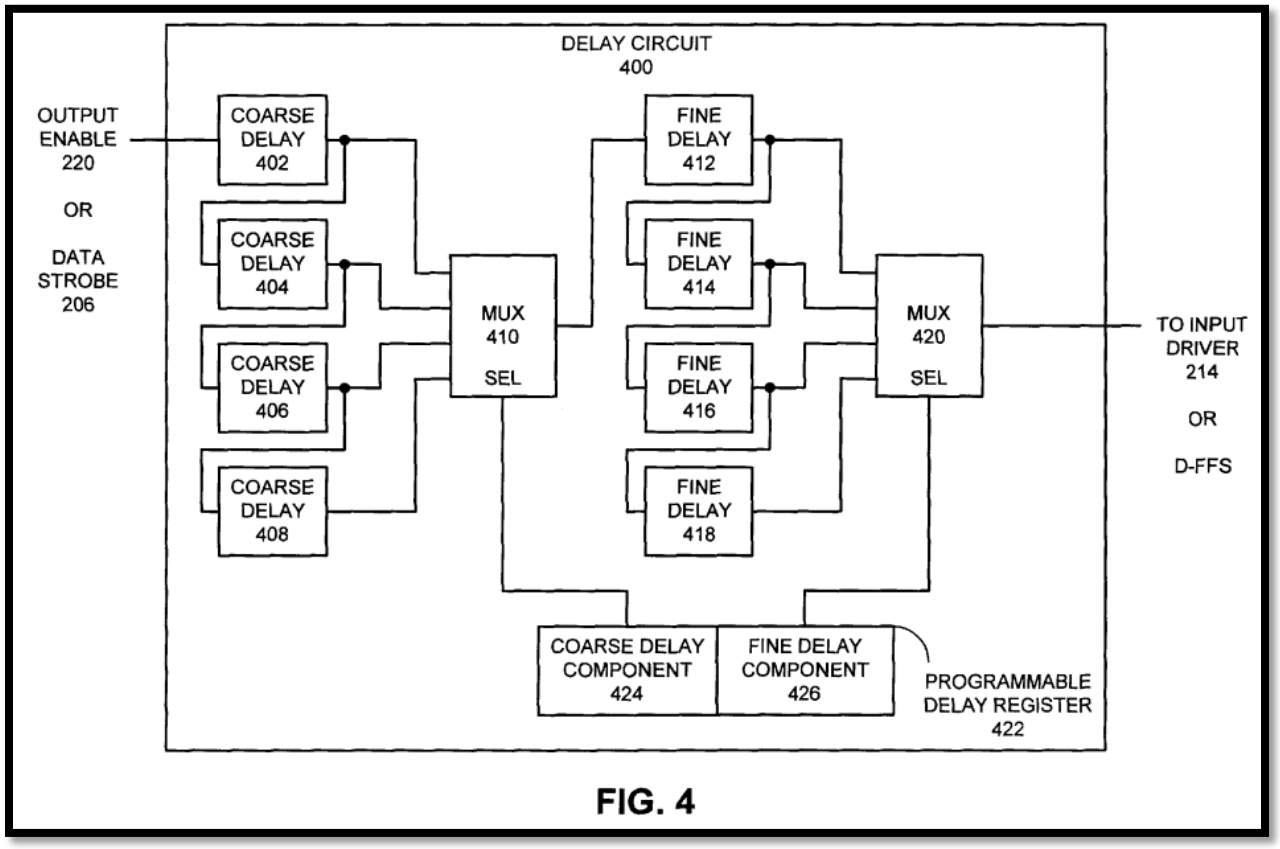


FIG. 4

Reproduced from *Jeddeloh*

Id. at 5.

91. Programmable delay circuit 400 "receives an enable signal 220 and produces a delayed output that feeds into an enable input of input drivers 214 to enable driving of input drivers 214" and/or "receives data strobe signal 206 and produces a delayed output that feeds into a clock input of a D-flip-flop in order to latch a data Signal into the D-flip-flop." *Id.* at 5:54-65. The input passes through a chain of coarse delay elements 402, 404, 406, and 408 which is then fed into MUX 410. *Id.* at 5:66-6:2. MUX 410 selects an output which then feeds into a chain of

fine delay elements 412, 414, 416, and 418. *Id.* at 6:2-5. The output of the fine delay elements is provided to MUX 420 which selects a final output for the delay circuit 400. *Id.* at 6:5-8.

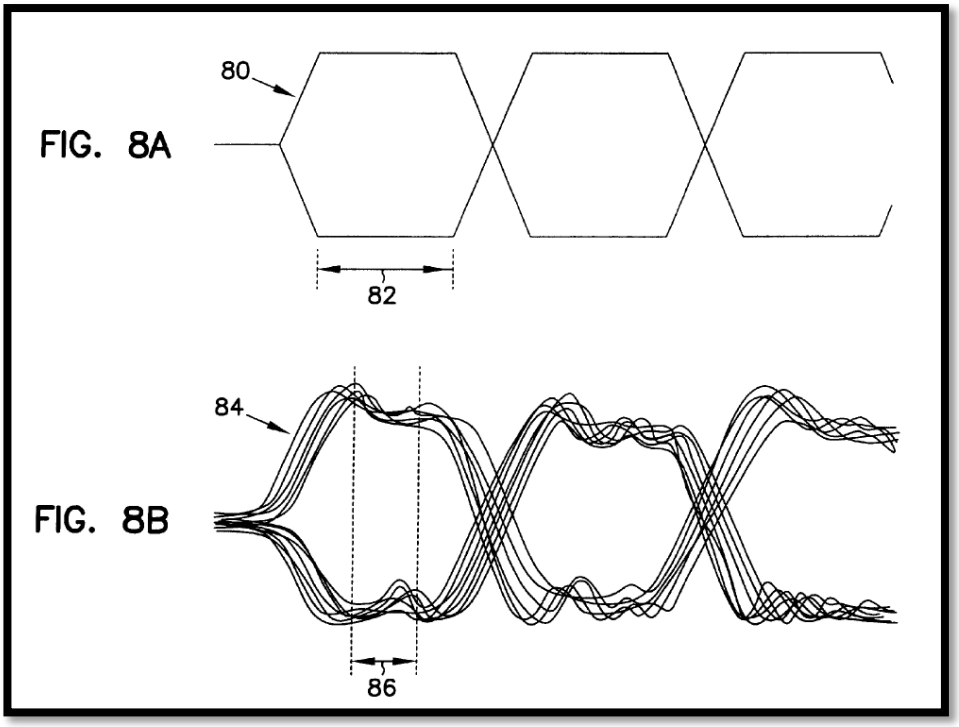
92. Specifically, the coarse delay component 424 of programmable delay register 422 controls MUX 410 and the fine delay component 426 of programmable delay register 422 controls MUX 420. In this way, *Jeddeloh* describes a delay circuit that has both a coarse adjustment and a fine adjustment.

3. *Keeth (Ex. 1006)*

93. U.S. Patent No. 6,115,318 ("*Keeth*") was filed on December 3, 1996 and issued on September 5, 2000. Ex. 1006 at 1. *Keeth* lists Brent Keeth as the sole inventor and lists Micron Technology, Inc. as Assignee. *Id.* at 1. *Keeth* is titled "Clock Vernier Adjustment." *Id.* at 1.

94. *Keeth* describes a dynamic random access memory (DRAM) system in which clock adjustments are used to accurately "clock" command data, write data, and read data. *Id.* at 1:4-7; 1:39-43. *Keeth* recognizes that the increasing speed of computer memory systems amplified the effects of system variables such as "duty cycle variation, bus position of a given memory device, timing drift, loading variations, clock jitter, clock skew, noise, overshoot, and ringing." *Id.* at 1:43-50. One such effect that *Keeth* identifies is a shrinking of the time period during which valid data can be sampled. *Id.* at 9:51-60. *Keeth* illustrates this effect

in Figures 8A and 8B, which show an "ideal" signal waveform and a "non-ideal" signal waveform, respectively. *Id.* I have reproduced Figures 8A and 8B below.



Reproduced from *Keeth*

Id. at 11.

95. *Keeth* explains that the ideal waveform in Figure 8A forms a "big eye" 82 in which data is valid and can be accurately sampled. *Id.* at 9:52-55. Figure 8B, by contrast, shows a signal waveform in which the data eye 86 is significantly reduced, relative to eye 82, by "jitter, skew, noise, overshoot, ringing and other such known problems." *Id.* at 9:55-60.

96. To address these issues, *Keeth* describes a memory system incorporating vernier clock adjustment circuits to control the timing of clock

signals, or sampling signals, transmitted between a memory controller and memory devices. *Id.* at 1:51-2:4. Figure 1 of *Keeth* shows a DRAM memory system in simplified block diagram form. *Keeth* explains that memory system 20 in Figure 1 includes a memory controller 22 and DRAM modules 24 and 26. *Id.* at 3:39-41. Memory system 22 includes command bus 28, data bus 32, and clock lines 30, 34, and 36 running between memory controller 22 and DRAM modules 24 and 26. Command bus 28 carries address and control information from memory controller 22 to the DRAM module in packets. *Id.* at 3:43-47. Data bus 32 carries read data from the DRAM modules to the memory controller and write data from the memory controller to the DRAM modules. *Id.* at 3:51-54. Clocks CCLK, DCLK0, and DCLK1 are transmitted on clock lines 30, 34, and 36, respectively. *Id.* at 47-56. I have reproduced Figure 1 of *Keeth* immediately below.

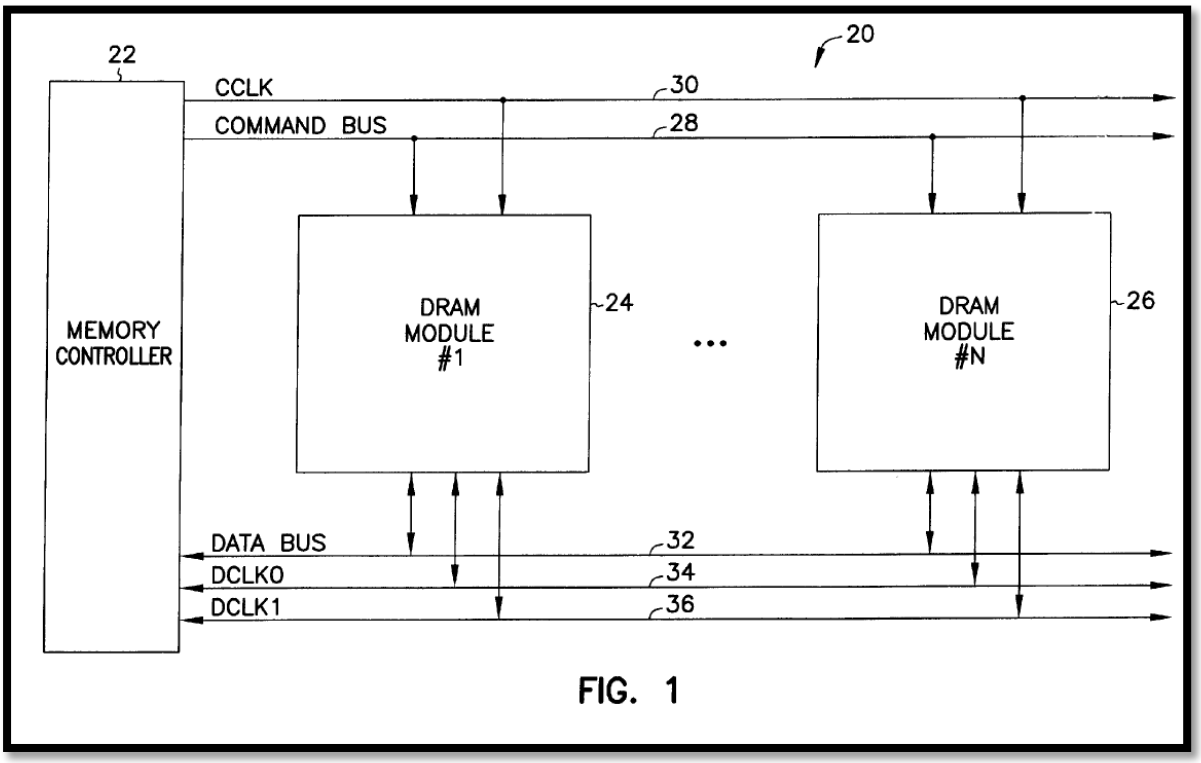


FIG. 1

Reproduced from *Keeth*

Id. at 4.

97. CCLK is generally used to clock command packets sent on command bus 28 from the memory controller 22, whereas DCLK0 and DCLK1 are generally used to latch data transmitted between the DRAM modules and memory controller 22 along the data bus 32. *Id*.

98. Figure 2 of *Keeth* illustrates a timing diagram for the memory system shown in Figure 1. Free-running CCLK is illustrated at the top of Figure 2 and has a rising edge or falling edge transition at intervals of time T. *Id.* at 4:19-21. T may be 2.5 nanoseconds, for example. *Id.* at 4:22-23. I have reproduced Figure 2 below:

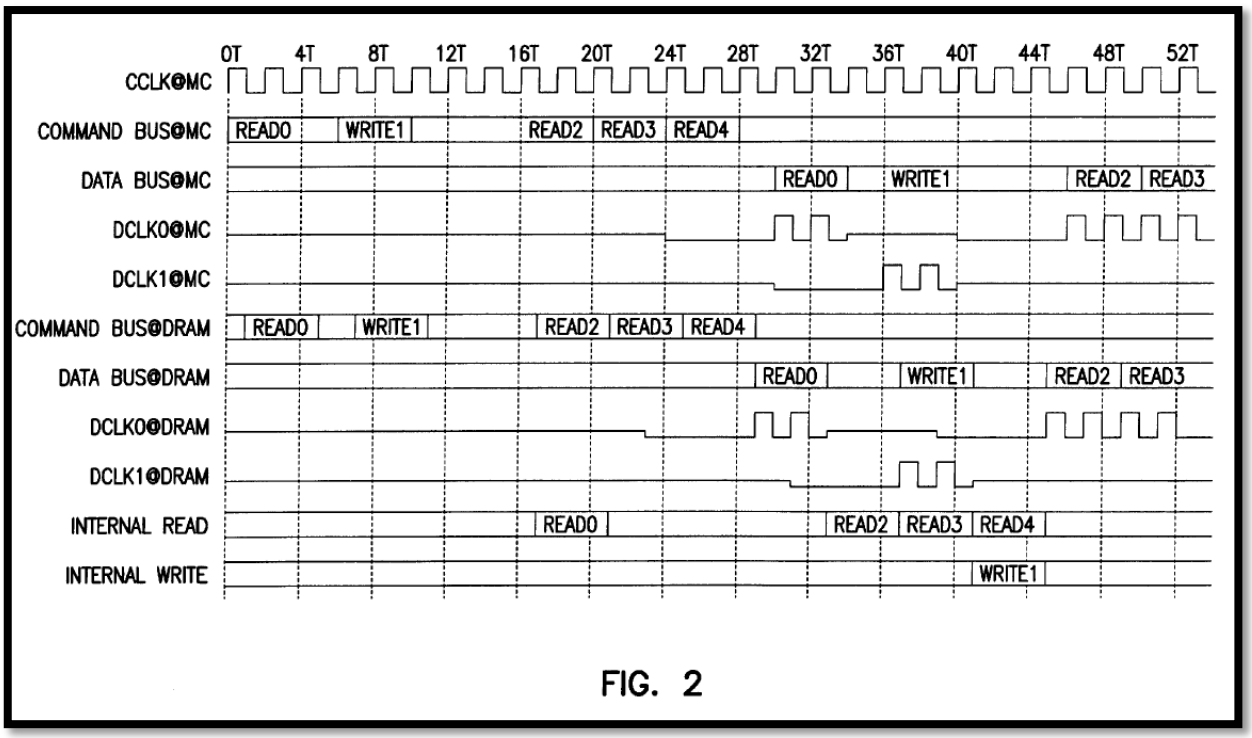


FIG. 2

Reproduced from *Keeth*

Id. at 5.

99. CCLK generally sets the timing of the overall system. *Id.* at 4:19-27. For example, commands READ0 and WRITE1 issued by the memory controller are aligned with rising and falling edges of CCLK. *Id.* at 5. The READ0 command is issued at 0T and the WRITE1 command is issued at 6T. *Id.* Read data corresponding to the READ0 command is transmitted from a DRAM module at 29T on the data bus. *Id.* at 4:30-32. Rising and falling edges of DCLK0 corresponding to the read data are also transmitted at 29T. *Id.* The read data and corresponding DCLK0 for the READ0 command arrive at the memory controller at 30T. *Id.* at 4:32-35. Similarly, write data corresponding to the WRITE1

command is transmitted from the memory controller at 36T on the data bus. *Id.* at 4:40-47. Rising and falling edges of DCLK1 corresponding to the write data are also transmitted at 36T. *Id.* The write data and corresponding DCLK1 for the WRITE1 command arrive at the target DRAM module at 37T. *Id.* at 4:41-43. These timings of command, data, and sampling signals are controlled by vernier delay adjustment circuitry within the memory system. *Id.* at 6:10-16.

100. Figure 7 of *Keeth* illustrates the memory system in further detail, showing several vernier delay adjustment circuits (including vernier clock adjustment circuits 60, 70, and 74) used to control timing of signals within the system. *Id.* at 7:41-46. In *Keeth*, the vernier delay adjustment circuits are used to control the timing of clock signals CCLK, DCLK0, and DCLK1 relative to other signals to ensure that commands, read data, and write data are clocked and/or latched accurately. *Id.* I have reproduced Figure 7 below.

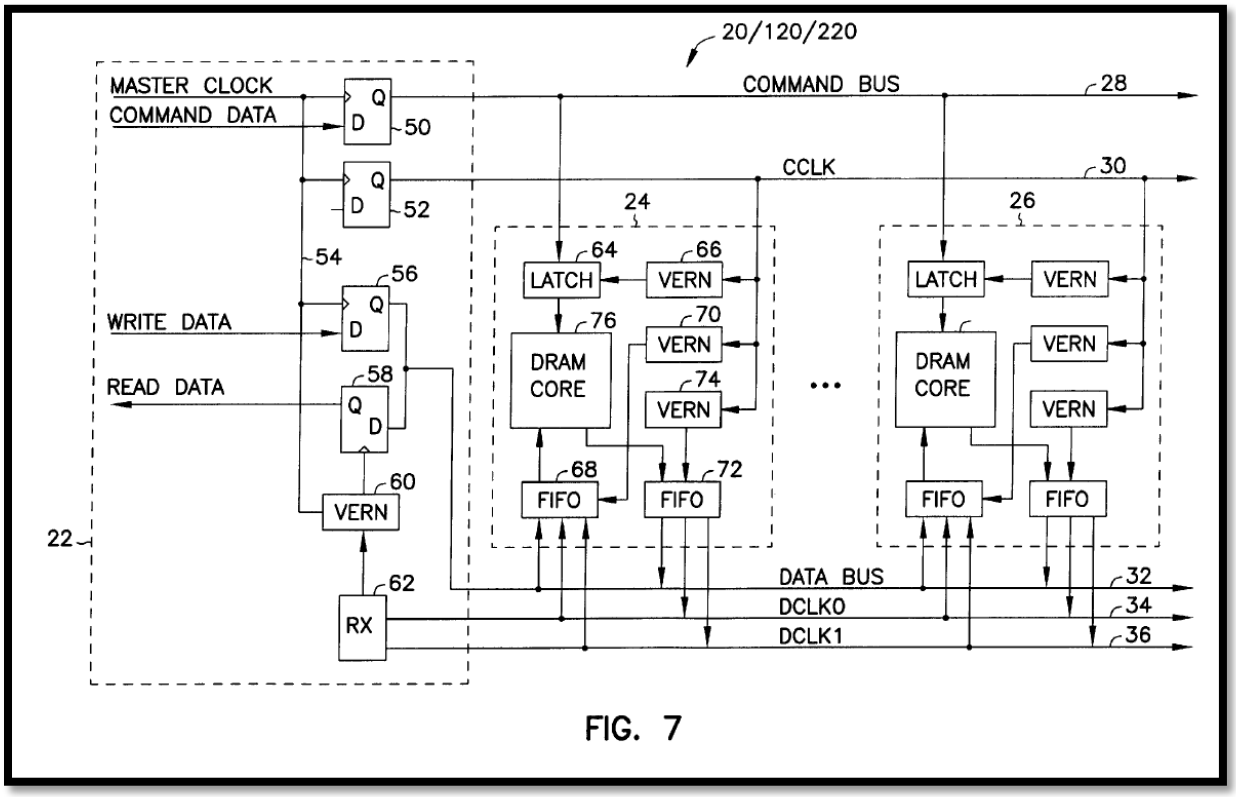


FIG. 7

Reproduced from *Keeth*

Id. at 10.

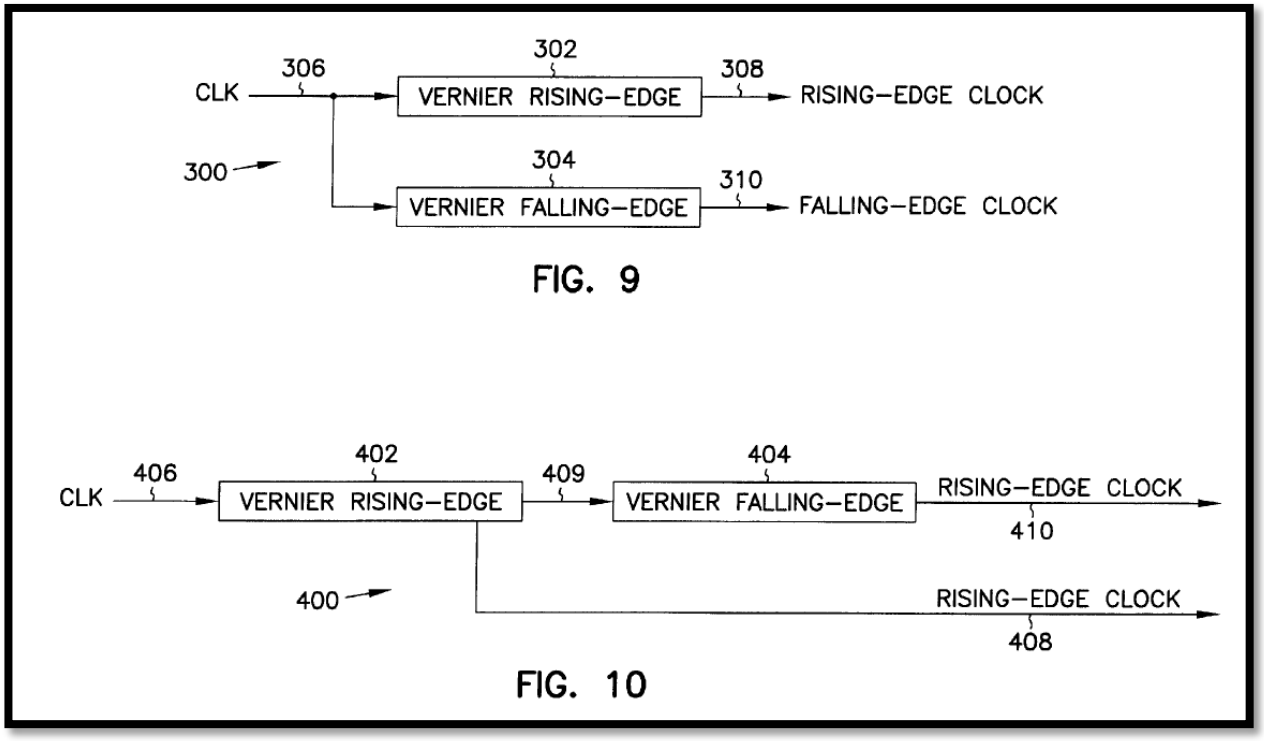
101. In the memory controller, vernier clock adjustment circuit 60 is used to control the timing of an active one of DCLK0 and DCLK1. *Id.* at 6:66-7:3. Vernier clock adjustment circuit 60 is used to adjust the timing of DCLK0 or DCLK1, whichever is active, for optimal sampling of read data at read data register 58. *Id.* at 8:38-42.

102. DRAM modules 24 and 26 also include vernier clock adjustment circuits 66, 70, and 74, each of which are used to control the timing of CCLK for operations occurring within the DRAM modules. *Id.* at 7:4-22. Vernier clock

adjustment circuit 66 provides a delayed CCLK to latch 64 to ensure appropriate timing between commands issued by the memory controller and CCLK. *Id.* at 7:4-9. Write vernier clock adjustment 70 provides a delayed CCLK to write first-in, first-out (FIFO) buffer 68 to ensure appropriate timing between write data signals and CCLK at the FIFO buffer 68 when data is written to DRAM core 76. *Id.* at 7:9-15. Read vernier clock adjustment 74 provides a delayed CCLK to read FIFO buffer 72 to ensure appropriate timing between read data signals and CCLK at the FIFO buffer 72 when data is read from DRAM core 76. *Id.* at 7:15-22.

103. *Keeth* explains that the foregoing vernier clock adjustment circuits are configured to adjust the rising edges and falling edges of clock signals to properly align with valid data signals. *Id.* at 10:1-5. Figure 9 of *Keeth* shows a first configuration in which a clock signal CLK is input to a vernier clock adjustment circuit 300 on line 306. *Id.* at 10:5-8. The clock signal CLK proceeds to adjustment circuit 302, which is used to adjust a timing of a rising edge of the CLK. *Id.* The clock signal CLK also proceeds to adjustment circuit 304, which is used to adjust a timing of a falling edge of the CLK. *Id.* at 10:10-13. The adjusted rising-edge clock and falling-edge clock are output on lines 308 and 310, respectively. *Id.* at 9-15. In another configuration shown in Figure 10, CLK 406 is first input to adjustment circuit 402 for adjustment of rising edge timing. *Id.* at 12. A delayed version of

CLK then proceeds to adjustment circuit 404, which adjusts falling edge timing. I have reproduced Figures 9 and 10 below.



Reproduced from *Keeth*

Id. at 12.

E. Summary of the Grounds

104. Below, I discuss the grounds for why the challenged claims 1 and 3-12 of the '443 Patent would have been obvious to a POSITA.

105. Ground 1: Claims 1-23 are obvious over *Johnson* in view of *Jeddeloh.*

106. Ground 2: Claims 1-3, 7-8, and 12 are obvious over *Johnson* in view of *Keeth*.

107. Ground 3: Claims 4-6, 9-11, 13-19 are obvious over *Johnson* in view of *Keeth* and *Jeddeloh*.

108. Below, I address each claim limitation on a limitation-by-limitation basis for each reference and/or combination of references. When a single reference is used to address a claim limitation, I provide the reason why the claim limitation either would have been recognized by a POSITA as being disclosed by the reference at the time of the purported invention, or would have been obvious to a POSITA in view of the reference at the time of the purported invention. When a combination of references are used to address a claim limitation, I also provide the motivation to combine references and reasons that there would have been a reasonable expectation of success in doing so. Given certain similar claim limitations and the use of the same references in multiple combinations, many of the explanations herein would apply to multiple claim limitations and reasons that a POSITA would have been motivated to combine these references and have a reasonable expectation of success in doing so. Therefore, my explanation regarding a certain claim limitation and certain reference or combination may also apply to other claim limitations, or the use of that same reference in another combination for the same or a similar claim limitation. This applies even if there is no explicit incorporation by reference. Furthermore, while I have cited portions of each reference to support my opinions below, I may rely on additional portions of the

references to further support those opinions, or portions of other references, including portions identified above where I discussed the prior art and technology background.

F. Ground 1: Claims 1-23 are Obvious Over *Johnson* in View of *Jeddeloh*

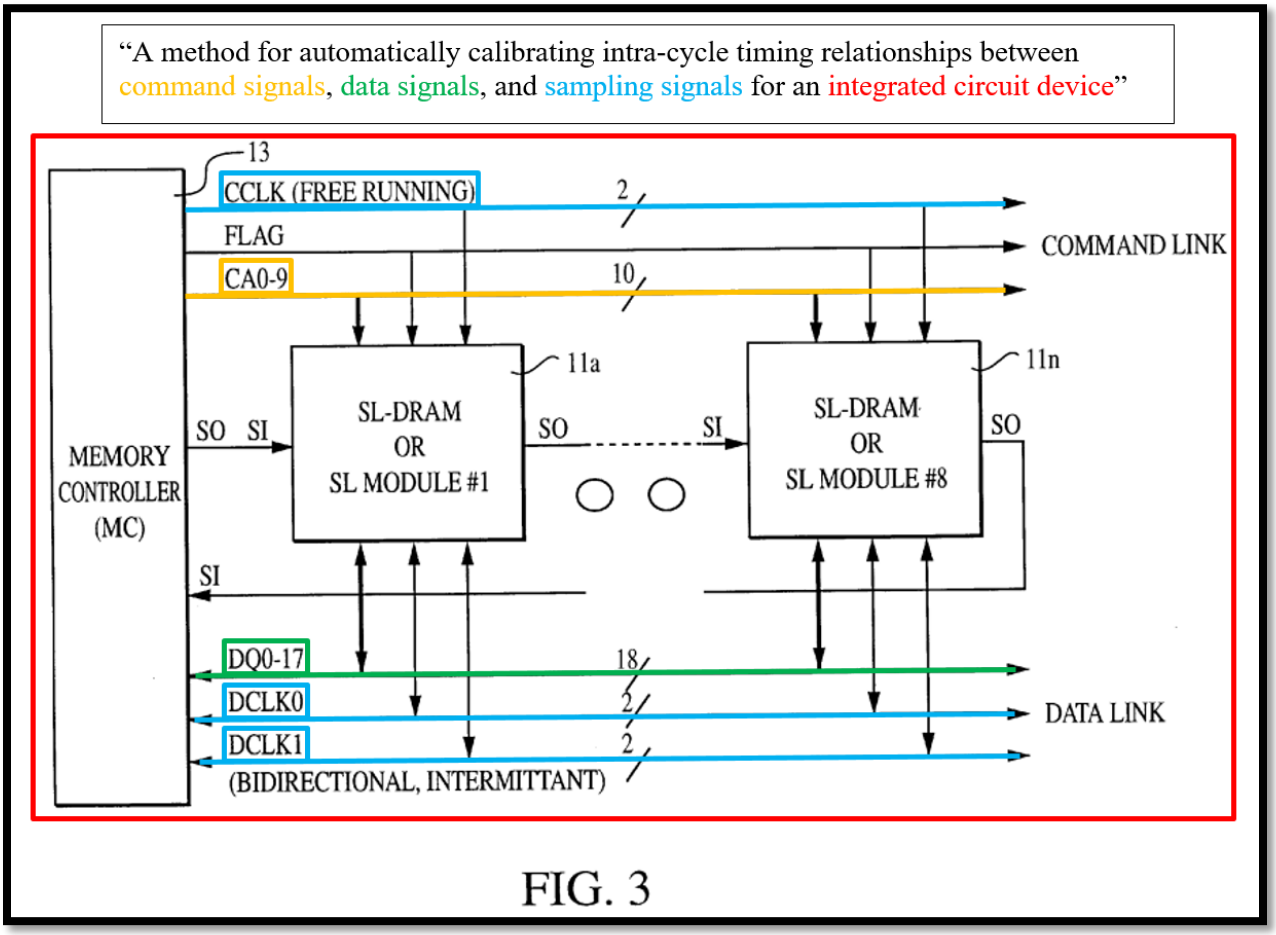
1. *Claim 1*

(a) *1[P]. A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the method comprising:*

109. *Johnson* discloses a method for automatically calibrating intra-cycle timing relationships between commands on the CA0-9 bus (e.g., the claimed *command signals*[2]), data on data paths DQ (e.g., the claimed *data signals*), and command clock signal (CCLK) and data clock signal (DCLK) (e.g., the claimed *sampling signals*) for a memory system (e.g., the claimed *integrated circuit device*) including a memory controller and SLDRAM modules. Ex. 1004 at 3. In general, *Johnson* is directed to a "calibration apparatus and method for use in a memory device[.]" *Id.* at Abstract. *Johnson* explicitly states embodiments of the memory device are incorporated in a processor-based system (e.g., an integrated circuit device) that contains a processor, a memory device, and an I/O (input/output)

[2] I have formatted exact claim language with underlining and italicizing throughout this declaration for emphasis.

device. *Id.* at 8:31-34. The calibration technique is useful for "calibrating the timing of control and data signals in memory devices, for example, SLDRAM memory devices." *Id.* at 1:5-8. I have reproduced an annotated version of FIG. 3 of *Johnson* below to help illustrate this claim limitation.



Reproduced from *Johnson* (Annotated)[3]

Id. at 3, annotated.

[3] Quoted claim elements in text boxes in annotated are added by me unless otherwise indicated.

110. *Johnson* shows an SLDRAM system topography incorporating the calibration system in FIG. 3. *Id*. at 3:30-31. The SLDRAM system includes a plurality of SLDRAM modules 11a-11n, accessed by memory controller 13. *Johnson* explains that the SLDRAM system generally works as follows:

> Memory controller 13 provides **a command link** to each of the SLDRAM modules 11a ...11n which includes **a clock signal CCLK** on inverted and non-inverted clock signal paths, a 1 bit FLAG signal on a FLAG data path, and **a 10 bit command bus data path CA0-9**. In addition, SLDRAM input/output enabling signals SO, SI are provided from memory controller 13 in daisy chain fashion to the SLDRAM modules 11a . . . 11n. In addition, **a bi-directional data bus DQ0-17** is provided between memory controller 13 and each of the SLDRAM modules 11a . . . 11n, as are **bi-directional data clocks DCLK0 and DCLK1**. The clock DCLK0 is used to Strobe input/output data into and out of the SLDRAM modules, a process for which the DCLK1 signal path is also intermittently used.

Id. at 3:33-47 (emphases added).

111. The calibration technique of *Johnson* provides "correct alignment of data entering a memory module, e.g., an SLDRAM module, on a plurality of incoming data paths in both a serial and parallel direction." *Id.* at 2:45-48. Thus, "serial and parallel calibration of all data paths is achieved." *Id.* at 2:51-52. *Johnson* also describes a processor-based system that utilizes the "memory device

containing the calibration structure[.]" *Id.* at 8:30-33. The calibration process is performed on "any one of the data paths of the command bus CA0-9 and any one of the receive data paths of the data bus DQ." *Id.* at 4:56-58. Therefore, timing relationships between the command signals and both of the data signals and sampling signals are changed. Timing relationships between the data signals and both of the command and sampling signals are also changed. *Id.* For example, *Johnson* explains one of the data paths is "**calibrated relative to a clock signal**[.]" *Id.* at Abstract (emphasis added). *Johnson* further explains that the "optimal delay is achieved by **adjusting the temporal position of the received data bits** to achieve a desired bit alignment **relative to the clock**." *Id.* at 1:59-61 (emphasis added). Put another way, each "data path has its data eye correctly centered on a rising or falling clock edge." *Id.*, 6:30-33. *Johnson* states that its "memory device [] clocks data (i.e., reads or writes data) twice per clock **cycle**: on both the rising and falling edges of the clock." *Id.* at 8:41-44 (emphasis added). A POSITA would have recognized that to be centered on a clock edge, a data eye and its corresponding data signal would have a timing relationship with the cycling clock. Because the clock edges are cycled, a POSITA would have understood that the relationship governing alignment of data to a clock edge of a cycle to be an "intra-cycle timing relationship."

112. Due to the high speed of operation of memory devices, *Johnson's* calibration technique is performed at initialization (e.g., start-up or reset). *Id.* at 1:36-40. In other words, as would have been understood by a POSITA, *Johnson's* calibration technique is automatic because it is performed without human intervention. Ex. 1019 at 53 (*Dictionary of Electronics*, defining "automatic" as "capable of producing a desired response to certain predetermined conditions[,] …operating without human intervention[,] …without intervention by a human operator"). A POSITA would have understood that the calibration technique of *Johnson* produced a desired response (e.g., a calibration of timing relationships between signals) to certain predetermined conditions (e.g., the memory device starting up or resetting). Thus, *Johnson* teaches *a method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device*.

(b) *[1(a)] generating command signals to access an integrated circuit component;*

113. *Johnson* discloses a memory controller generating data on command signal paths CA0-9 (e.g., the claimed *generating command signals*) to access the SLDRAM modules (e.g., the claimed *access an integrated circuit component*). Ex. 1004 at 3. *Johnson* describes a memory system with a memory controller component and one or more SLDRAM module components. *Id.* at 3:30-46. In this

way, the SLDRAM module of *Johnson* is an integrated circuit component. Command signals, such as the data on paths CA0-9, are used to dictate read and write functions of a memory device, such as the SLDRAM module, to facilitate memory access. *Id.* at 4:19-22 ("The control logic circuit 21 also issues an enable command RXEN whenever **the memory controller indicates a memory access WRITE operation by way of a WRITE command in the data on the command bus CA0-9**." (emphasis added)). *Johnson* explicitly discloses that the SLDRAM modules are accessed by the memory controller 13. *Id.* at 3:32-33.

114. For example, in *Johnson*, memory controller 13 "provides a command link to each of the SLDRAM modules 11 a … 11 n," which includes "a 10 bit command bus data path CA0-9." *Id.* at 3:30-40. Moreover, the "plurality of SLDRAM modules 11 a … 11 n [] are **accessed** and controlled by [] memory controller 13." *Id.* (emphasis added). I have once again provided an annotated version of *Johnson's* FIG. 3 below to help illustrate this claim limitation.

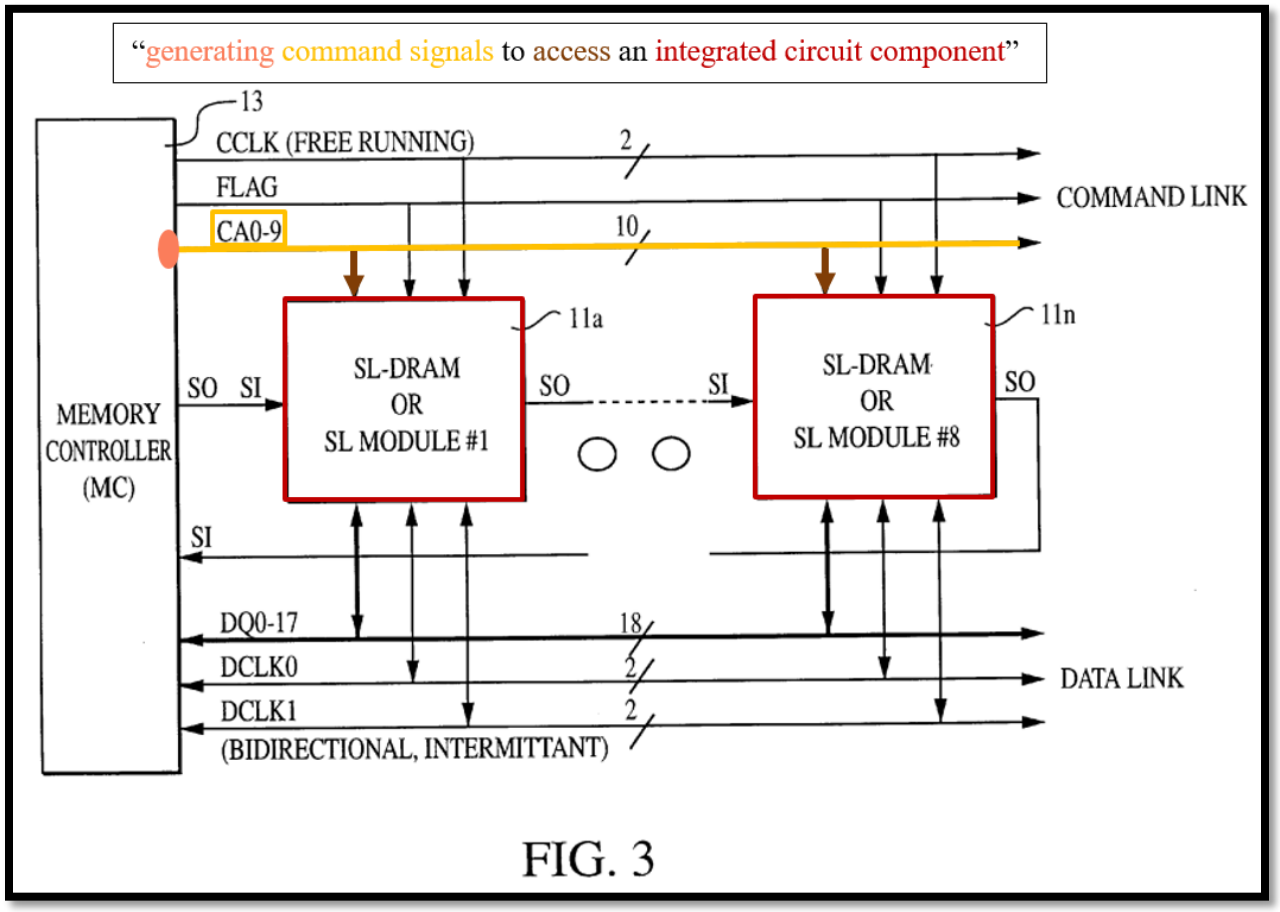


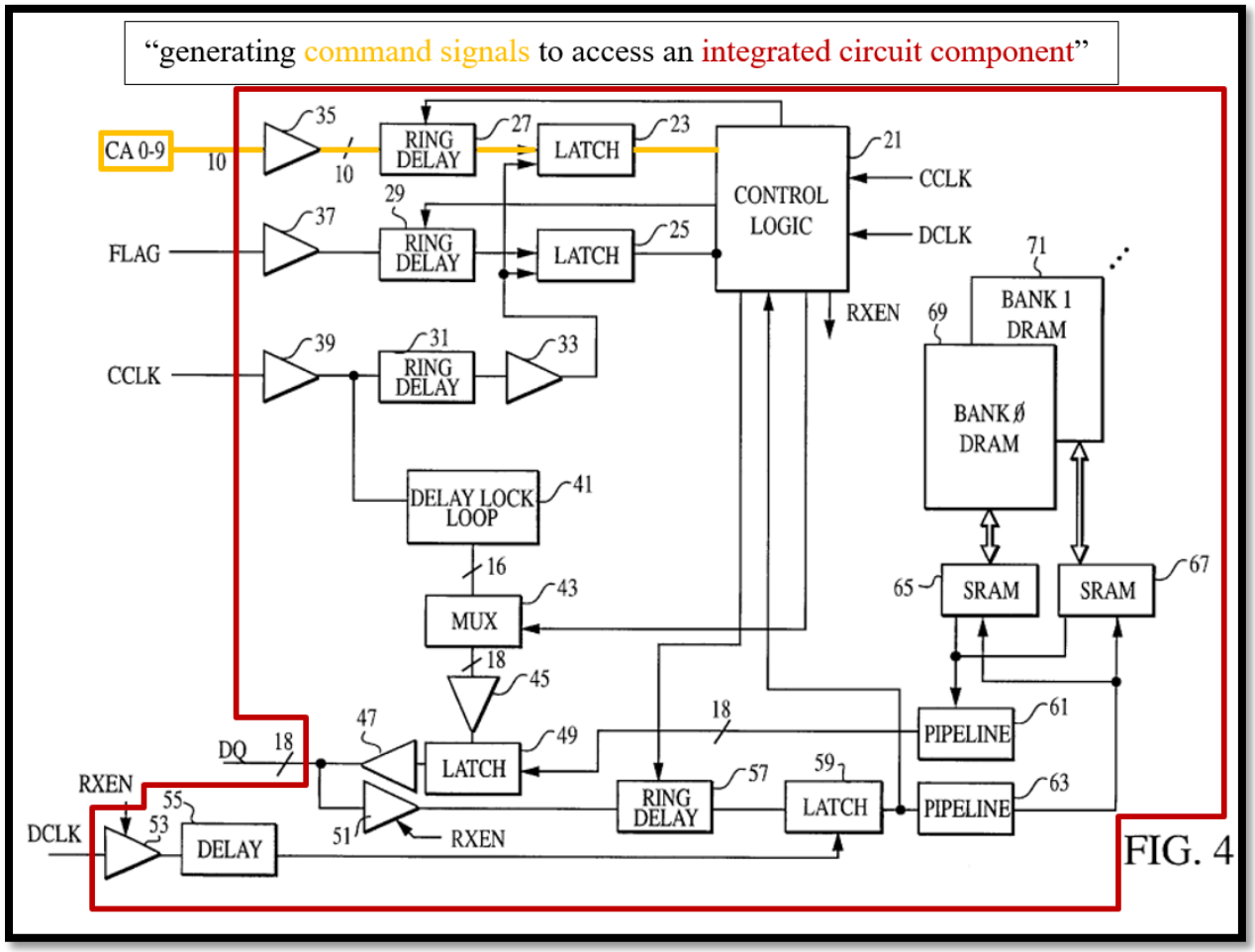
FIG. 3

Reproduced from *Johnson* (Annotated)

Id. at 3, annotated.

115. The memory controller 13 is responsible for managing the flow of data and signals to ensure proper memory operations and does so at least in part by generating command signals to indicate a write or read operation to the memory device. *Id.* at 4:19-26 ("the memory controller **indicates** a memory access WRITE operation by way of a **WRITE command in the data on the command bus CA0-9**." (emphasis added)); *see also supra* Section III(A); Ex. 1015 at 2 ("[the memory]

controller establishes the information flow between memory and the CPU."). As I previously explained, the memory controller 13 of *Johnson* provides a command link to the SLDRAM modules that includes command bus data path CA0-9. *Id.* at 3:30-40. Data comes into an SLDRAM module "from a memory controller for… [all of] the command bus data paths." *Id.* at 2:15-16. *Johnson* also shows the command signals in a functional block diagram of a portion of one of the SLDRAM modules in FIG. 4, which I have annotated and reproduced below.



Reproduced from *Johnson* (Annotated)

Id. at 4, annotated.

116. As shown, control logic 21, among other things, "receives and analyzes commands on the CA0-9 bus and controls the input/output (I/O) **access operations** of the memory banks 69, 71." *Id.* at 3:57-59 (emphasis added). "The signals on each of the command bus paths CA0-9 are passed through respective adjustable ring delay circuits 27 and into respective latches 23 where the signals are latched by a CCLK signal, as buffered by buffer 39, delayed by delay 31 and buffered by buffer 33." *Id.* at 3:63-67.

117. The memory controller 13 generates the data for the command signals found on command bus paths CA0-9 to then access SLDRAM modules 11a-11n. "The data present on the command signal paths CA0-9 and on the FLAG path is clocked in by sequential positive and negative going transitions of the command clock signal CCLK." *Id.* at 4:67-5:3. A POSITA would have known that memory controllers in memory systems generate command signals in order to issue commands to the memory component to perform the read or write operations requested by system. *See supra* Section III(A); Ex. 1016 at 4 ("Throughout the paper, the term *operation* denotes a **command**, such as a row activation or a column access, **issued by the memory controller to the DRAM**." (emphasis added)). For these reasons, *Johnson* teaches *generating command signals to access an integrated circuit component*.

(c) *[1(b)] accessing data signals to convey data for the integrated circuit component;*

118. *Johnson* discloses data provided on data paths DQ (e.g., the claimed *accessing data signals*) that is transmitted between the memory controller 13 and the SLDRAM modules 11a-11n (e.g., the claimed *convey data for the integrated circuit component*). Ex. 1004 at 3. Specifically, as I have described below, the memory controller of *Johnson* accesses data signals when transmitting data for write operations and when receiving data for read operations. The SLDRAM module accesses data signals when receiving data for write operations and when transmitting data for read operations.

119. For example, *Johnson* explains that the calibration procedure includes timing synchronization of clock signals "with data provided on an incoming command path CA and FLAG path (for the CCLK signal) and on the **data paths DQ (for the DCLK signal)** so that **incoming data is correctly sampled**." *Id.* at 1:42-48 (emphasis added). I have annotated FIG. 3 for this claim limitation and provided it below.

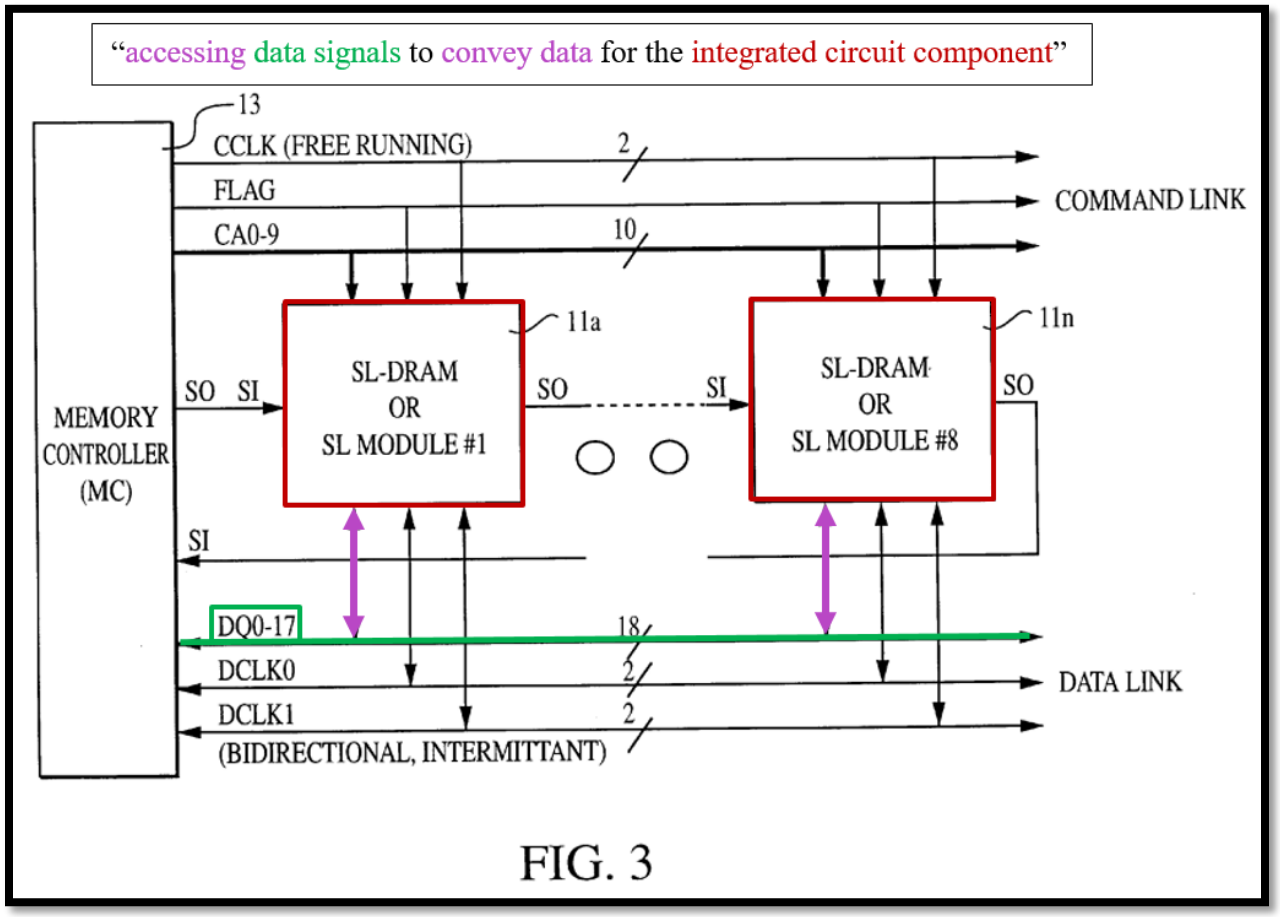


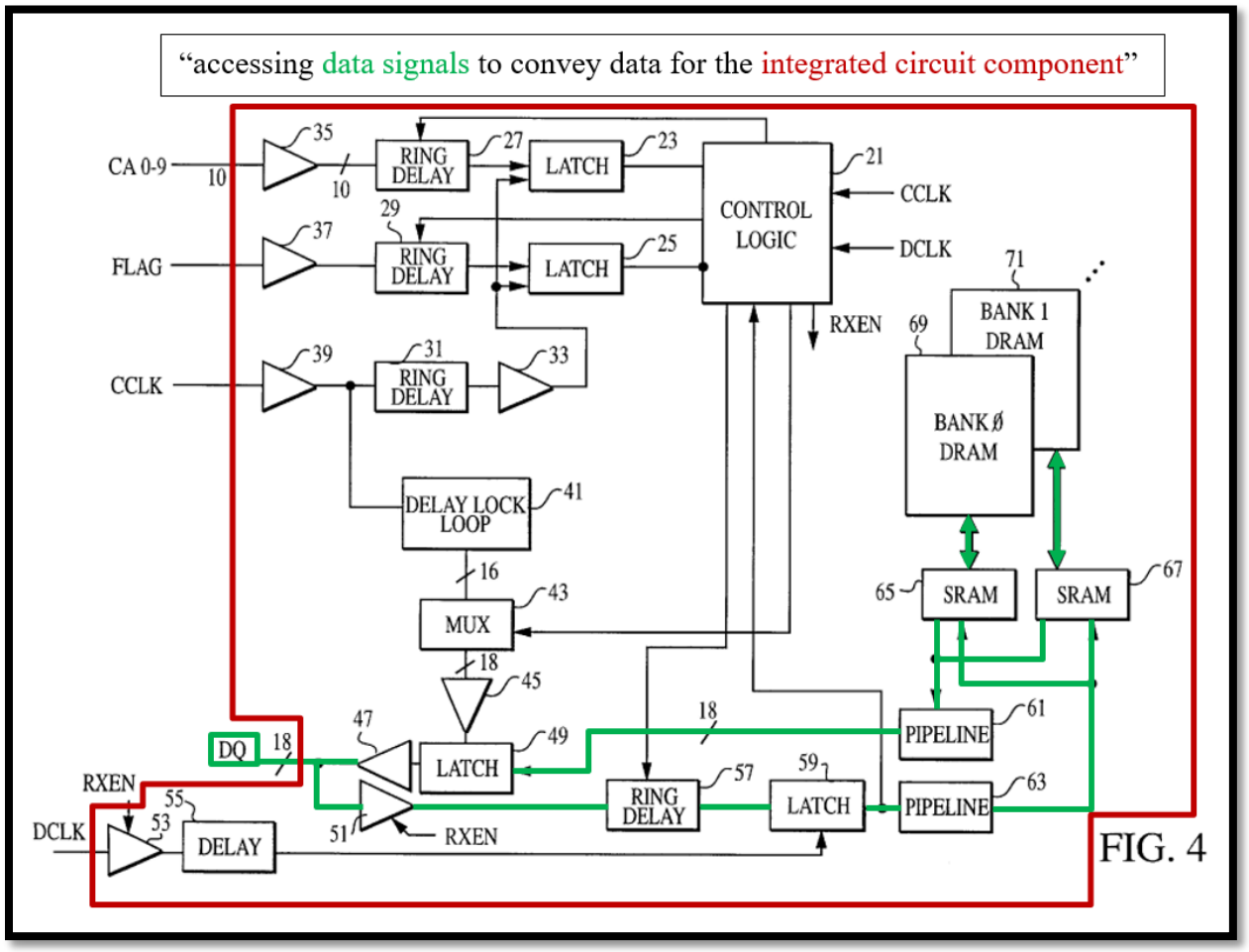
FIG. 3

Reproduced from *Johnson* (Annotated)

Id. at 3, annotated.

120. As previously discussed, the SLDRAM system shown in FIG. 3 includes "a plurality of SLDRAM modules 11 a … 11 n which are accessed and controlled by a memory controller 13." *Id.* at 3:30-33. More specifically, the SLDRAM system includes "a bi-directional data bus DQ0-17 is provided between memory controller 13 and each of the SLDRAM modules 11 a … 11 n[.]" *Id.* at 3:41-43. The SLDRAM modules include a latch to "latch in incoming **data on the**

data bus DQ." *Id.* at 4:24-26 (emphasis added). This is shown in more detail in annotated FIG. 4 below:



Reproduced from *Johnson* (Annotated)

Id. at 4, annotated.

121. *Johnson* thus discloses a calibration system that accesses data signals from data bus DQ to convey the data for an integrated circuit component, such as an SLDRAM module. The system uses a bi-directional data bus such that data can be read from and written to the SLDRAM module. For example, output data from

memory banks 69 and 71 pass through the circuitry until it is "passed back to memory controller 13 (FIG. 3) via data bus DQ." *Id.* at 4:5-11. The memory controller 13, therefore, accesses data signals via data bus DQ that convey data outputted from the memory banks of the SLDRAM module (e.g., the *integrated circuit component*). Conversely, "[d]ata which is to be **input[ted] to memory banks 69, 71 is supplied by memory controller 13** (FIG. 3) on the DQ data bus, is passed through gated buffer 51 … [and eventually into] a memory bank 69, 71." *Id.* at 4:12-18 (emphasis added). Thus, the SLDRAM module accesses data signals transmitted via data bus DQ from the memory controller 13.

122. The control logic circuit issues an enable command (RXEN) for write operations that "enables the data input buffers 51 and a data clock input buffer 53" such that DCLK passes through gated buffer 53 and delay circuit 55 to "latch in **incoming data** on the data bus DQ." *Id.* at 4:20-26 (emphasis added). In light of the fact *Johnson* is directed to a "calibration technique which is useful for calibrating the timing of control and **data signals in memory devices**," it was well understood that the data signals provided on DQ would be accessed to convey data for the SLDRAM module. *Id.* at 1:6-7. Therefore, *Johnson* teaches *accessing data signals to convey data for the integrated circuit component*.

(d) *[1(c)] accessing sampling signals to control sampling of the data signals; and*

123. *Johnson* discloses transmitting clock signals (e.g., the claimed *accessing sampling signals*) to adjust data signals that are both output by and input to the SLDRAM module (e.g., the claimed *control sampling of the data signals*). Ex. 1004 at 3. Specifically, as I have described below, the memory controller of *Johnson* accesses data sampling signals when data is read from or written to the SLDRAM module. The SLDRAM module also accesses data sampling signals when data is read from or written to the SLDRAM module.

124. *Johnson* explains that, in some prior art synchronizing schemes, "**all incoming data can properly be aligned with respect to the clock** used to latch in the data **by adjusting the data delays relative to the clock** (CCLK or DCLK) to position a sampling clock edge at or near the center of the data 'eye' or 'window' where the data is valid on an incoming data path." *Id.* at 2:3-9 (emphasis added). "When the conventional calibration procedure is performed … each of the data bits on each of the incoming data paths is properly serially aligned with an edge of clock signal CCLK[.]" *Id.* at 2:23-27. I have annotated and reproduced FIG. 3 to show the clock signals below.

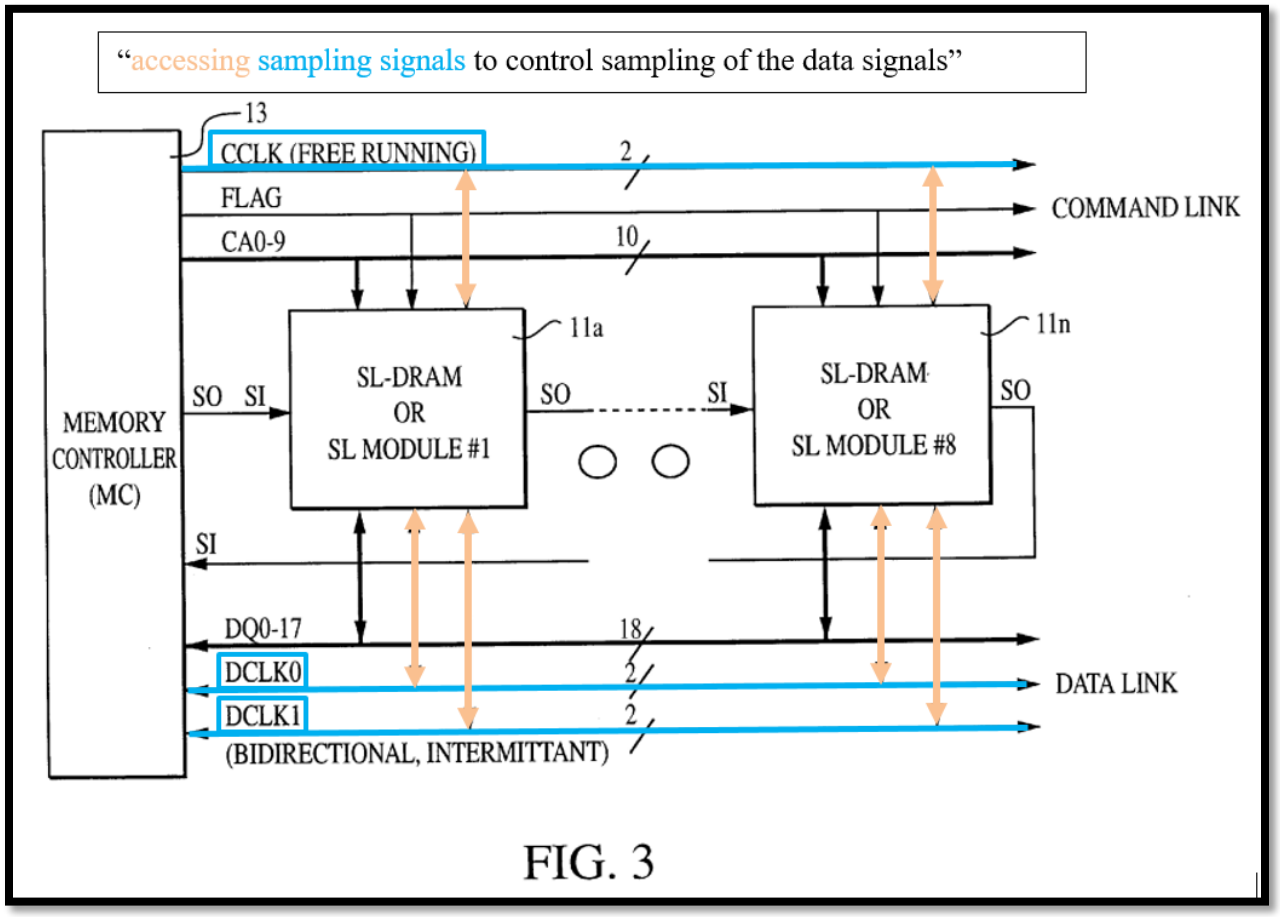


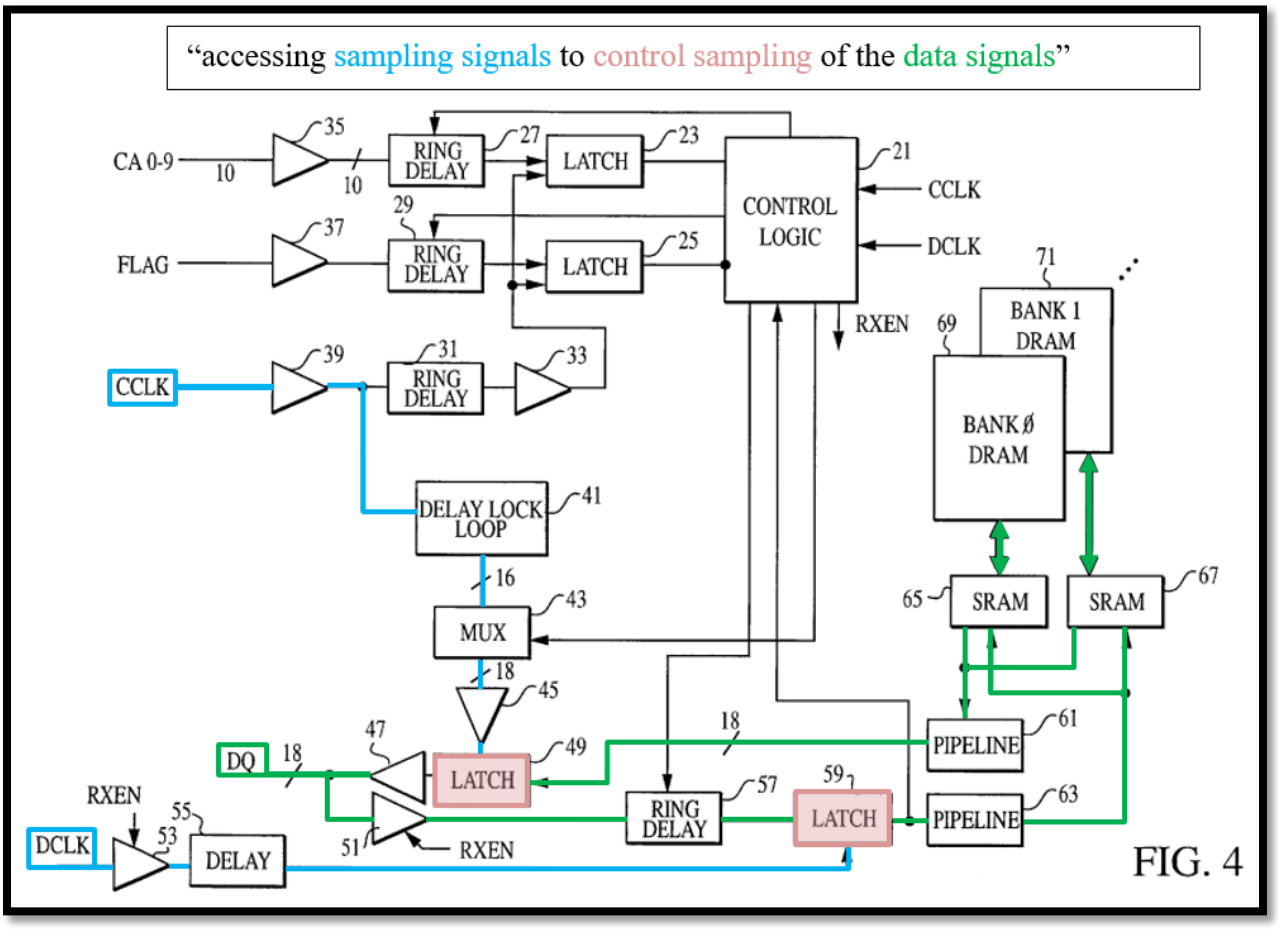
FIG. 3

Reproduced from *Johnson* (Annotated)

Id. at 3, annotated.

125. In *Johnson*, "[m]emory controller 13 provides a command link to each of the SLDRAM modules 11 a … 11 n which **includes a clock signal CCLK** on inverted and non-inverted clock signal paths[.]" *Id.* at 3:33-36 (emphasis added). Additionally, "bi-directional data clocks DCLK0 and DCLK1" are provided between the memory controller 13 and the SLDRAM modules 11a-11n; the clock DCLK0 (and the clock DCLK1 intermittently) is used "to strobe input/output data

into and out of the SLDRAM modules." *Id.* at 3:44-47. This is shown in more detail in annotated FIG. 4 below:



Reproduced from *Johnson* (Annotated)

Id. at 4, annotated.

126. The control logic 21 of the SLDRAM module receives (i.e., accesses) both CCLK and DCLK. *Id.* at 3:60-62. CCLK passes through buffer 39 and delay lock loop circuit 41 *Id.* at 4:1-3. From there, the clock signals are provided to a multiplexer and passed through buffer 45, eventually latching to data signals at latch 49. *Id.* at 4:3-5 ("The multiplexer provides 18 clock output signals through

respective buffers 45 to 18 latches 49 which latch data output from the memory banks 69, 71."). *Johnson* explains that "the output data latched in latches 49" is then passed "to memory controller 13 [] via data bus DQ." *Id.* at 4:5-11. By latching to the clock data signals, the sampling signals effectively control the sampling of the data signals latched. CCLK controls sampling of data signals, via latches 49, at least when the data signals are output from the memory banks onto the data bus DQ.

127. Additionally, the data clock DCLK "passes through gated buffer 53, delay circuit 55 and is used to **control latch 59 to latch in incoming data on the data bus DQ**." *Id.* at 4:23-26 (emphasis added). The circuit shown in FIG. 4 must be "synchronized to ensure that the incoming data is properly clocked in by the clock signals CCLK and DCLK." *Id.* at 4:29-31. The data from CA0-9 is "sampled in latches 23 and 25 by the delayed clock signal CCLK." *Id.* at 4:34-36. Thus, the sampling of data from the DQ data bus and the sampling of data from the CA bus are controlled by DCLK and CCLK respectively as they are used to latch the data. CCLK is used for the clocking of the data paths of the command bus CA0-9 and DCLK is used for the clocking of the data paths of the data bus DQ. *Id.* at 4:56-59.

128. An excerpt of *Johnson's* FIG. 5 is shown below to illustrate DCLK controlling the sampling of the data signals from DQ.

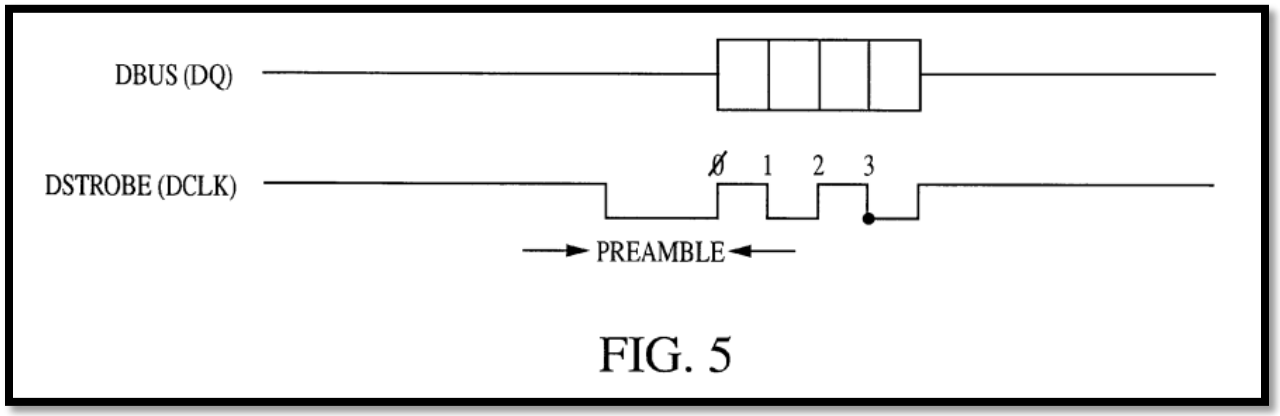


FIG. 5

Reproduced from *Johnson* (Excerpted and Annotated)

Id. at 5 (excerpt), annotated.

129. "FIG. 5 illustrates a simplified timing diagram showing the timing relationship of … a data bus signal DQ/DBUS and a data strobe signal DCLK. As shown, four bits of **data on a DQ path of the data bus (DBUS) are clocked in** on four sequential positive and negative going transitions of **the data clock signal DCLK** after an initial PREAMBLE portion of DCLK appears." *Id.* at 4:59-67 (emphasis added). For at least these reasons, a POSITA would have understood that *Johnson* teaches *accessing sampling signals to control sampling of the data signals*.

(e) *[1(d)(i)] systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device,*

130. *Johnson* discloses testing delay values of the command signals transmitted via data bus CA0-9 (e.g., the claimed *systematically altering a phase*

shift of the command signals) to determine values that result in alignment with CCLK and testing delay values of the data signals transmitted by data bus DQ0-17 (e.g., the claimed *a phase shift of the data signals*) to determine values that result in alignment with DCLK. Ex. 1004 at 1:42-48. In doing so, *Johnson* identifies a range of delay values that result in valid sampling for the memory device (e.g., the claimed *determine a valid operation range of the integrated circuit device*). *Id.* at 4:41-43. Moreover, the prior art, as explained by *Johnson*, included a calibration procedure that "**is a timing synchronization of clock signals CCLK (command clock signal) and DCLK (data clock signal)** with data provided on an incoming command path CA and FLAG path (for the CCLK signal) and on the data paths DQ (for the DCLK signal) **so that incoming data is correctly sampled**." *Id.* at 1:42-48 (emphases added).

131. *Johnson* explains that the calibration process, as described for the CCLK clock signal and data from CA0-9, is also used for the DCLK data clock signal and data from DQ. *Id.* at 4:53-59 ("[T]he same calibration process may be carried out on any one of the data paths of the command bus CA0-9 and **any one of the receive data paths of the data bus DQ (although for the latter the DCLK signal is used for clocking)**.") (emphasis added). While CA0-9 data paths are aligned to CCLK, "the data paths DQ0-17 are aligned to [DCLK]." *Id.* at 6:46-48. Thus, the same calibration procedure is applied to the CMD data paths CA0-9

as the data paths of the DQ bus, except that the data clock DCLK is used to latch the data present in each of the data paths of the DQ data bus. *Id.* at 6:7-11. An annotated version of FIG. 4 is provided below to illustrate this claim limitation.

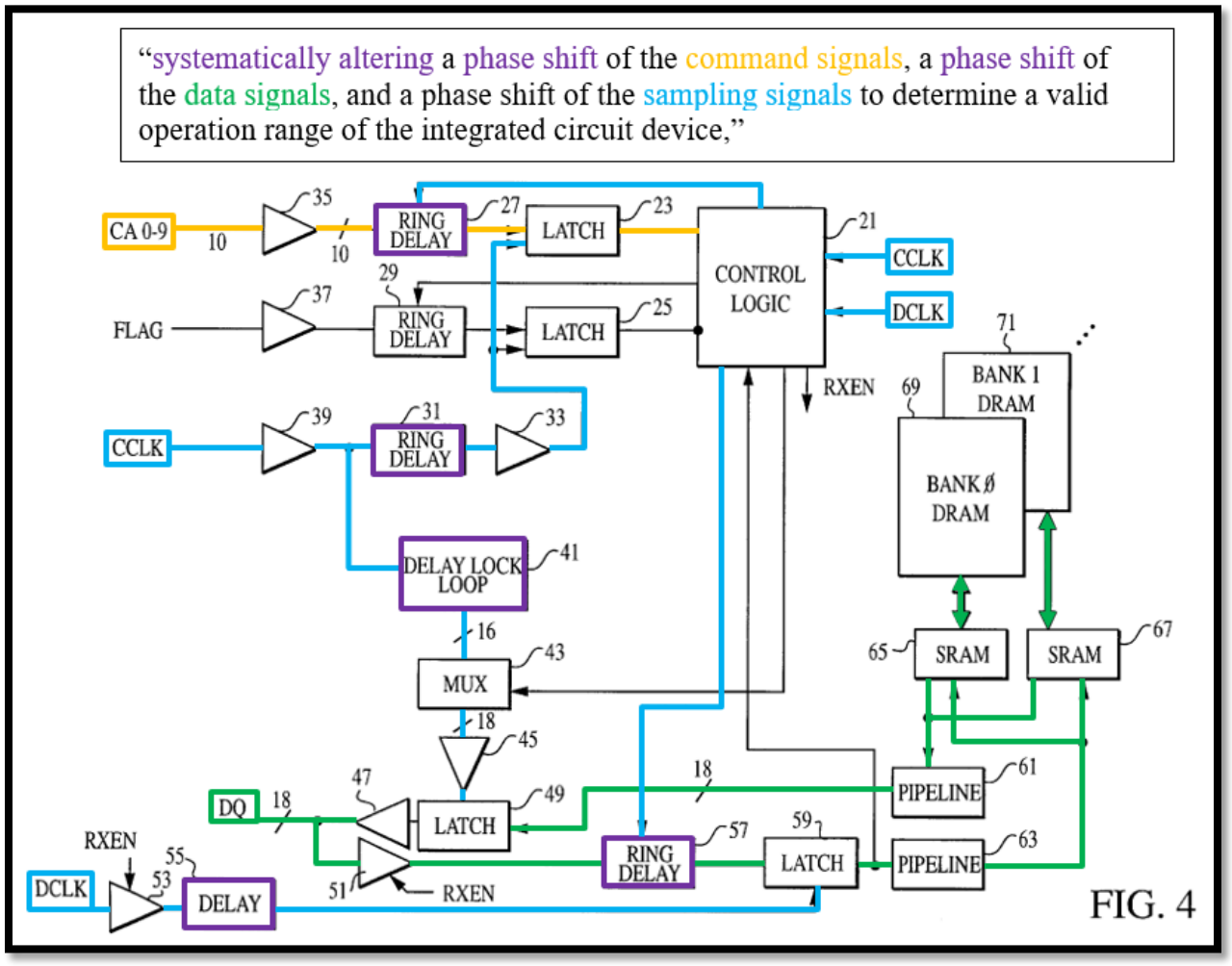


FIG. 4

Reproduced from *Johnson* (Annotated)

Id. at 4, annotated.

132. The command signals of the command bus paths CA0-9 pass through the ring delay 27, altering a phase shift as further described below. *Id.* at 3:63-67.

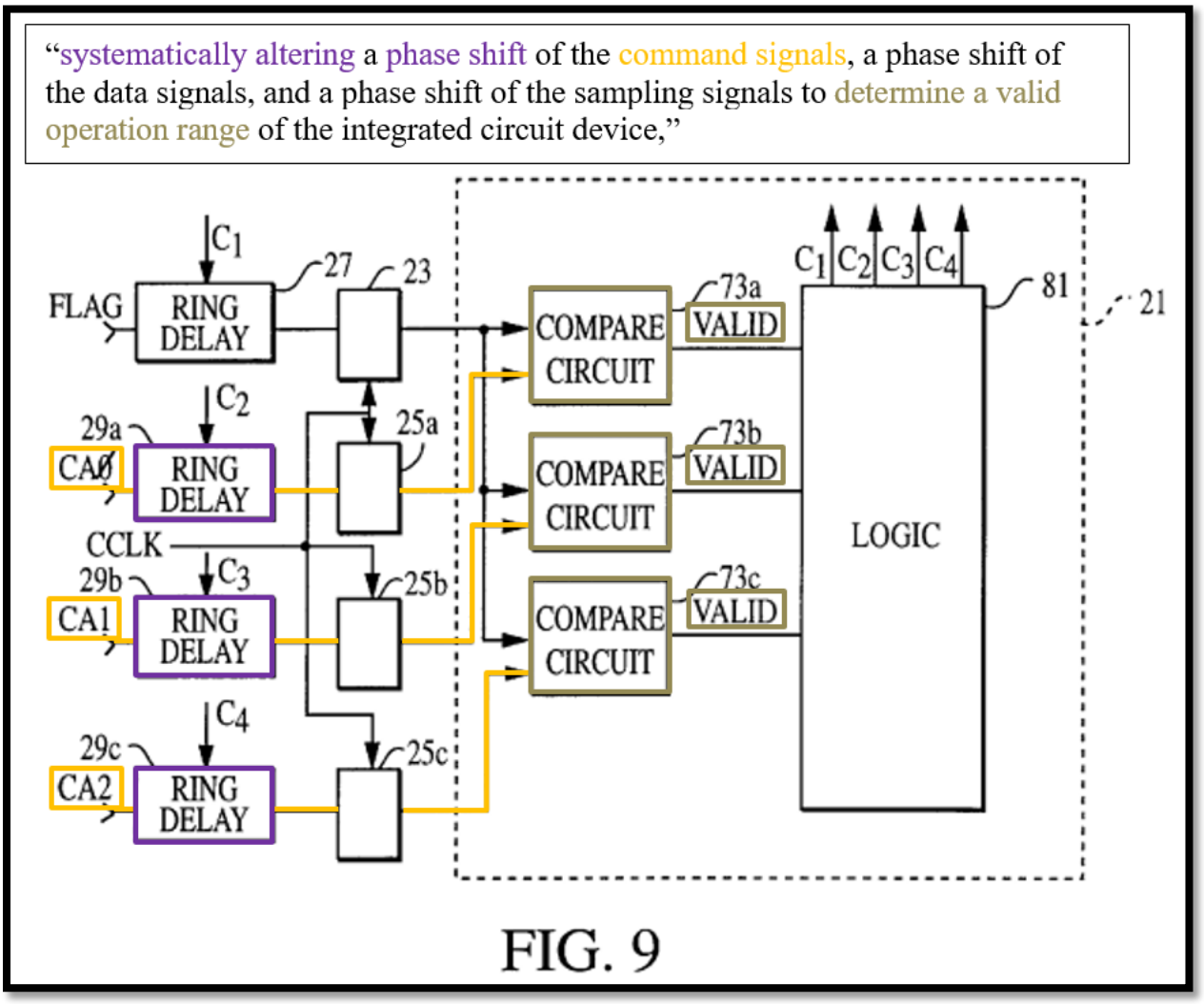
Similarly, the data signals of the data bus DQ pass through the ring delay 57. *Id.* at 4:12-16 ("Data which is to be input to memory banks 69, 71 is supplied by memory controller 13 (FIG. 3) on the DQ data bus, is passed through gated buffers 51 through ring delays 57 on each path of the data bus, into latches 59, through pipeline circuit 63."). CCLK is used to latch the command signals and DCLK is used to latch the data signals, as highlighted above with my annotations, to alter the phase shift of the signals such that the signals are valid for sampling.

133. *Johnson* also explains that the "signal CCLK also passes from buffer 39 into a **delay lock loop circuit 41** which provides 16 clock signals into a multiplexer 43. The **multiplexer provides 18 clock output signals** through respective buffers 45 to 18 latches 49 which latch data output from the memory banks 69, 71." *Id.* at 2:1-8. A POSITA would have understood that CCLK and the data output from the memory banks would be aligned at latches 49. Figure 4 of *Johnson*, however, shows that the data output from the memory banks 69, 71 does not pass through a delay before it reaches latches 49 where it is latched by CCLK. A POSITA would have therefore recognized that CCLK is aligned to the data signals by delay lock loop circuit 41 and would have understood that such alignment would be achieved by "step[ping[through all possible delay values," as *Johnson* teaches. *E.g.*, Ex-1004, 4:36-41. Similarly, DCLK is also delayed as it passes through "delay circuit 55" before arriving at latch 59 to latch a data signal

transmitted to the memory banks. *Id.* at 4:24-26. A POSITA would have recognized that the sampling signals of *Johnson* are delayed for latching with data signals from the DQ data bus or CA bus. *Johnson* explicitly shows and describes the sampling signals passing through delays and further describes a calibration technique that steps through valid delay values as I have described below. Thus, a POSITA would have understood a phase shift of the sampling signals of *Johnson*, along with the data signals and command signals, is systematically altered to properly synchronize with the other signals as doing so would provide additional alignment.

134. The circuit "must be synchronized to ensure that the incoming data is properly clocked in by the clock signals CCLK and DCLK" to ensure proper timing "of the various memory operations performed by the SLDRAM modules[.]" *Id.* at 4:27-31. A "2^N bit synchronizing pattern is applied to each of the data input paths CA0-9 and FLAG while the data pattern is sampled in latches 23 and 25 by the delayed clock signal CCLK." *Id.* at 4:33-36. The control logic circuit 21 then "steps through all possible delay positions of ring delays 27 and 29 as the data sampling is performed and stores patterns representing which delay values for the ring delays 27 and 29 provide for a correct sampling and recognition of the 2^N bit pattern." *Id.* at 4:36-41. Thus, control logic circuit 21 establishes an "eye" or "window" of acceptable delays for "ring delays 27 for the command data paths

CA0-9[.]" *Id.* at 4:41-43. FIG. 9 shows a portion of the control logic circuit 21, which is reproduced and annotated below.

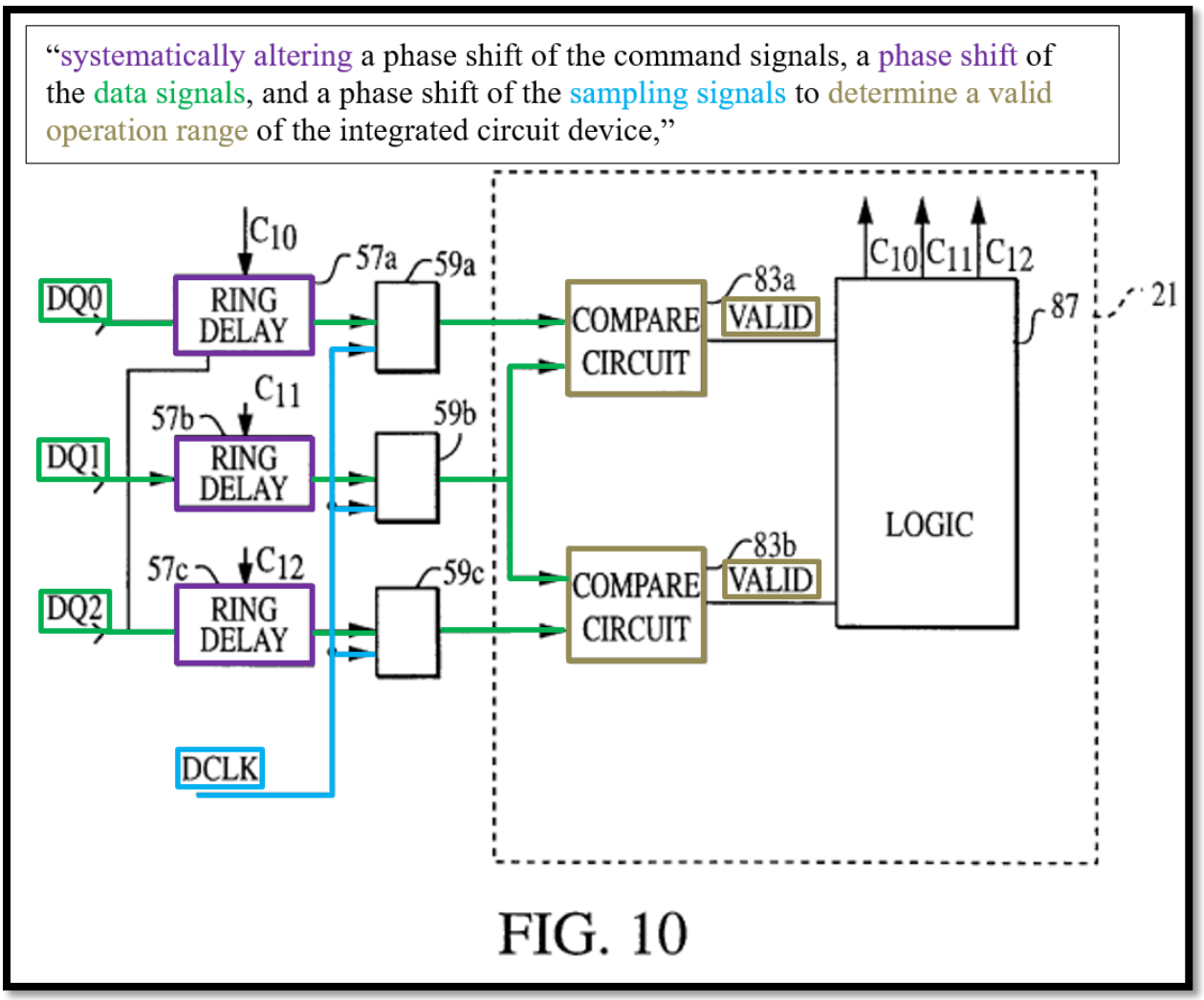


Reproduced from *Johnson* (Annotated)

Id. at 7, annotated.

135. The CA0-9 data paths are aligned to CCLK and are fed into ring delays, each ring delay being provided a C1-4 signal "used by the logic 81 to control the delay settings of the ring delays 27, 29a, 29b, 29c, respectively" *Id.* at

6:46-51. Moreover, *Johnson* discloses determining a valid operation range as the compare circuits 73a-c generate "VALID signals" to "signal whether the **synchronization pattern is properly recognized** to the logic 81." *Id.* at 6:51-54 (emphasis added). This is similarly shown in FIG. 10 with respect to the data signals, as I have annotated below:



Reproduced from *Johnson* (Annotated)

Id. at 7, annotated.

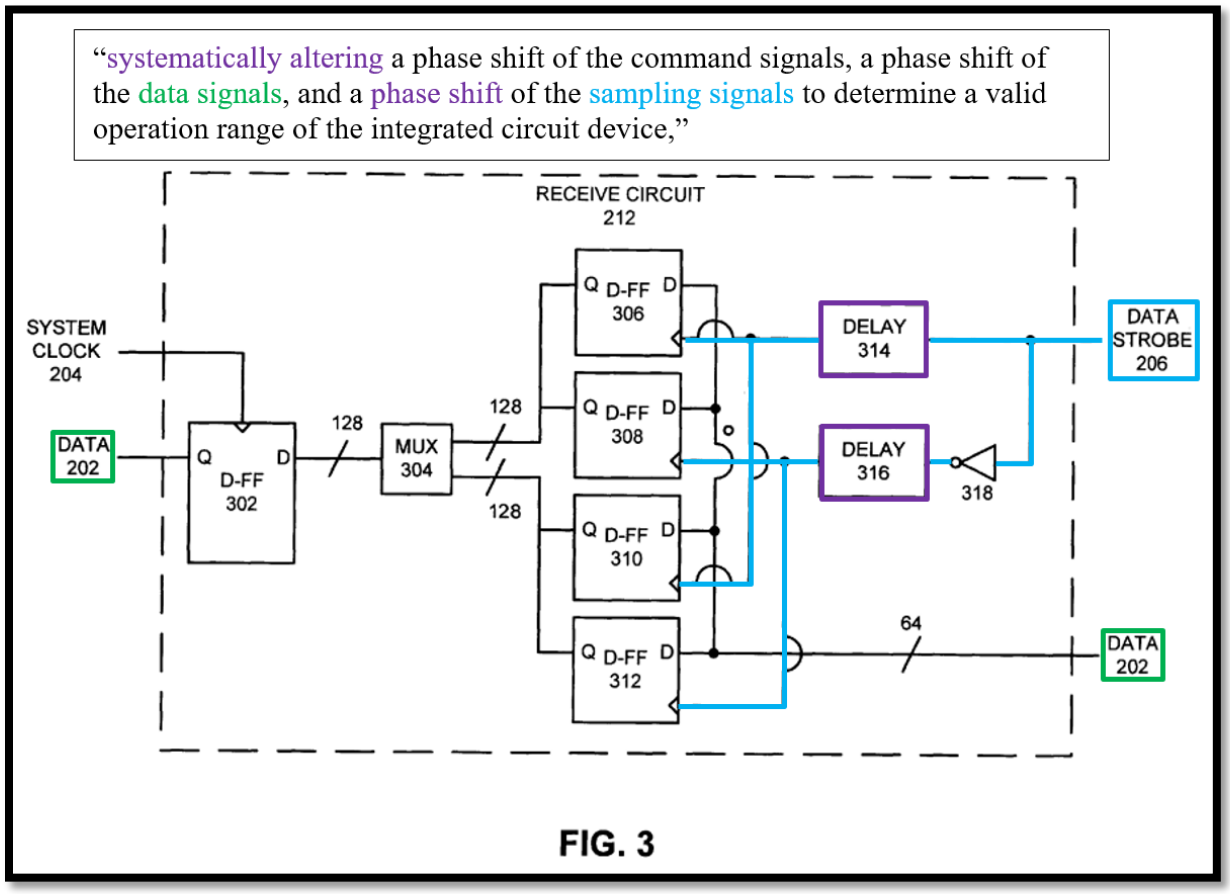
136. The DQ0-2 data paths are fed into ring delays that have settings set by the logic 87 using signals C10-C12. *Id.* at 7:30-35. *Johnson* illustrates this with data paths for the DQ0-17 data bus. *Id.* at 7:35-36. "**Once a first data path**, e.g., DQ0, **is serially aligned to DCLK** using the technique described with reference to FIGS. 1-7, the remaining DQ1-17 data paths can then be aligned by comparing the calibration pattern of a subsequent non-aligned data path to the calibration pattern which exists on a previously aligned data path." *Id.* at 7:36-42 (emphasis added). Further, "control logic circuit 21 includes compare circuit 83 a, which aligns the DQ1 data path including ring delay 57 b to the previously aligned DQ0 data path which includes ring delay 57 a **by comparing the calibration pattern on aligned data path DQ0 with the calibration pattern on the DQ1 data path to generate an appropriate validity signal on signal lines VALID**." *Id.* at 7:46-52 (emphasis added). The control logic 21 "steps through all possible delay values of ring delay 57 b, and **notes those delays which produce a coincidence of the calibration pattern on data paths DQ<0> and DQ<1>, and selects a final delay value for delay 57 b which is at or near the center of acceptable delays**." *Id.* at 7:52-57 (emphasis added). Since the control logic performs the adjustment methodically according to a defined procedure or plan (e.g., stepping through possible delay values), a POSITA would have understood this to be *systematically altering* the delay values. Ex. 1020 at 1230 (*Merriam-Webster's Dictionary*, defining

"systematic" as "methodical in procedure or plan"). Additionally, a POSITA would have understood that the delayed signals in *Johnson* are cyclic in nature. *See* Ex. 1004, 8:41-44. *Johnson* shows in Figure 5, for example, that the signals of the memory system are each cyclic. *Id.* at Fig. 5. A POSITA would have therefore understood that each cycle of the signals have a phase and a POSITA would have recognized that delays of the cyclic signals are phase shifts.

137. To the extent it may be argued that *Johnson* does not explicitly disclose *systematically altering a phase shift of … the sampling signals*, *Jeddeloh* teaches this element and this claimed combination would have been obvious over *Johnson* in view of the teachings *Jeddeloh*, for at least the following reasons. For example, *Jeddeloh* discloses a system that "synchronizes a data signal and a data strobe signal [e.g., the claimed *sampling signals*] received from a random access memory." Ex. 1005 at Abstract. Specifically, a second programmable delay circuit "is coupled between the data strobe signal and a clock input of the register." *Id.* "This second programmable delay circuit is **configured to delay the data strobe signal so as to synchronize the data strobe signal** with the data signal received from the random access memory." *Id.* (emphasis added).

138. An initialization mechanism determines a valid delay value "by performing test read operations using a plurality of different combinations of different first delay values and different second delay values." *Id.* I have annotated

and reproduced FIG. 3 of *Jeddeloh* below, which illustrates the architecture of a receive circuit.



Reproduced from *Jeddeloh* (Annotated)

Id. at 4, annotated.

139. As shown, in *Jeddeloh* "data strobe signal 206 passes through delay circuit 314 into clock inputs of D-FFs 306 and 310. Data strobe signal 206 also passes through inverter 318 and delay circuit 316 into clock inputs of D-FFs 308 and 312." *Id.* at 5:25-28. The delay circuits 314 and 316 can be "programmed to

precisely synchronize data strobe signal 206 with data signal 202." *Id.* at 5:32-34 (emphasis added).

140. "The system first determines delay values to be loaded into delay circuits 218, 314 and 316[.]" *Id.* at 6:27-28. *Jeddeloh* explains that the BIOS code performs "test read operations using **different delay values**[.]" *Id.* at 6:30-31 (emphasis added). The "optical delay values" are then determined and programmed into the delay circuits. *Id.* at 6:32-35. Delay values from the middle of the valid range for the delay circuits are selected by the system. *Id.* at 7:19-24.

141. A POSITA would have appreciated the advantages of modifying the circuitry described in *Johnson* that describes altering a phase shift of command and data signals with the circuitry of *Jeddeloh* that describes altering a phase shift of the sampling signals. This is especially true given the fact *Johnson* already describes delaying the sampling signals CCLK and DCLK.

142. For example, the CCLK in *Johnson* passes into delay lock loop circuit 41. Ex. 1004 at 4:1-3. Additionally, the DCLK passes through delay circuit 55 and "is used to control latch 59 to latch in incoming data on the data bus DQ." *Id.* at 4:24-26. In general, the SLDRAM "**determines an optimal internal delay for CCLK and DCLK** relative to the data each clocks to optimally sample the known bit pattern." *Id.* at 1:57-59 (emphasis added). The sampling signal (data strobe signal) describes in *Jeddeloh* also latches data from a data signal to synchronize.

Similar to *Johnson*, since the SLDRAM determines the adjustment methodically according to a defined procedure or plan (e.g., determining an optimal delay relative to the data clocked), a POSITA would have understood this to be *systematically altering* the delay values. Ex. 1020 at 1230 (*Merriam-Webster's Dictionary*, defining "systematic" as "methodical in procedure or plan"). Thus, a POSITA would have understood to use the explicit teachings of *Jeddeloh* with respect to the data strobe signal and apply the teachings to the DCLK (and CCLK) teachings of *Johnson*.

143. A POSITA would have been motivated to modify the system of *Johnson* according to the teachings of *Jeddeloh* at least to ensure proper synchronization of data signals and sampling signals when both writing to and reading from DRAM banks. *Johnson*, on the one hand, teaches that data signals transmitted via data bus DQ0-17 are phase shifted for alignment with DCLK. *Johnson* shows in FIG. 4 that DCLK latches the data signals on DQ0-17 when writing to DRAM banks. For reading from the DRAM banks, *Johnson* shows in FIG. 4 that CCLK latches data signals on DQ0-17. *Johnson* shows that CCLK passes through a delay lock loop 41, but may not explicitly explain how CCLK is synchronized to the data signals received from the DRAM banks.

144. A POSITA therefore would have had reason to look to *Jeddeloh* for specificity as to how to synchronize data signals received from the DRAM banks

to the sampling signals used to latch them. Following the teachings of *Jeddeloh*, a person having of ordinary skill in the art would have been able to modify the system of *Johnson* to systematically alter the phase shift of the sampling signals to ensure alignment of the sampling signals and data signals during read operations as such a combination would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. This is especially true given the fact that *Johnson* and *Jeddeloh* were both apparently the product of high-speed computer memory development at Micron Technology, Inc. and were filed only about a year apart. *See* Ex. 1004, Ex. 1005. Thus, *Johnson* in view of *Jeddeloh* teaches *systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device*.

(f) *[1(d)(ii)] wherein the valid operation range includes an optimal operation point for the integrated circuit device.*

145. *Johnson* discloses selecting the best delay values in the middle of the data windows (e.g., the claimed *optimal operation point*). As I have previously discussed, "incoming data is properly clocked in by the clock signals CCLK and DCLK" and "the data pattern is sampled in latches 23 and 25 by the delayed clock signal CCLK." Ex. 1004 at 4:30-36. The control logic circuit 21 "steps through all

possible delay positions of ring delays 27 and 29 as the data sampling is performed and **stores patterns representing which delay values** for the ring delays 27 and 29 **provide for a correct sampling** and recognition of the 2^N bit pattern." *Id.* at 4:36-41 (emphasis added). "In this manner, control logic circuit 21 establishes an 'eye' or 'window' of acceptable delays for each of the ring delays 27 for the command data paths CA0-9[.]" *Id.* at 4:41-43.

146. *Johnson* further explains that, once a window of acceptable delays is established, "the control logic circuit 21 **determines the 'best' delay value** as that value which is approximately in the middle of the window." *Id.* at 4:46-48 (emphasis added). Based on the delay settings, VALID signals are generated by compare circuits to "signal whether the synchronization pattern is properly recognized to the logic 81." *Id.* at 6:48-54. With respect to the data signals, the calibration pattern on data path DQ0 is compared with the calibration pattern on data path DQ1 to "generate an appropriate validity signal on signal lines VALID." *Id.* at 7:46-52. The circuit "notes those delays which produce a coincidence of the calibration pattern on data paths DQ<0> and DQ<1>, and **selects a final delay value for delay 57 b** which is at or near the center of acceptable delays." *Id.* at 7:54-57 (emphasis added). For these reasons, *Johnson* teaches *wherein the valid operation range includes an optimal operation point for the integrated circuit device*.

2. *Claim 2 – The method of claim 1, wherein the integrated circuit device comprises a DRAM component.*

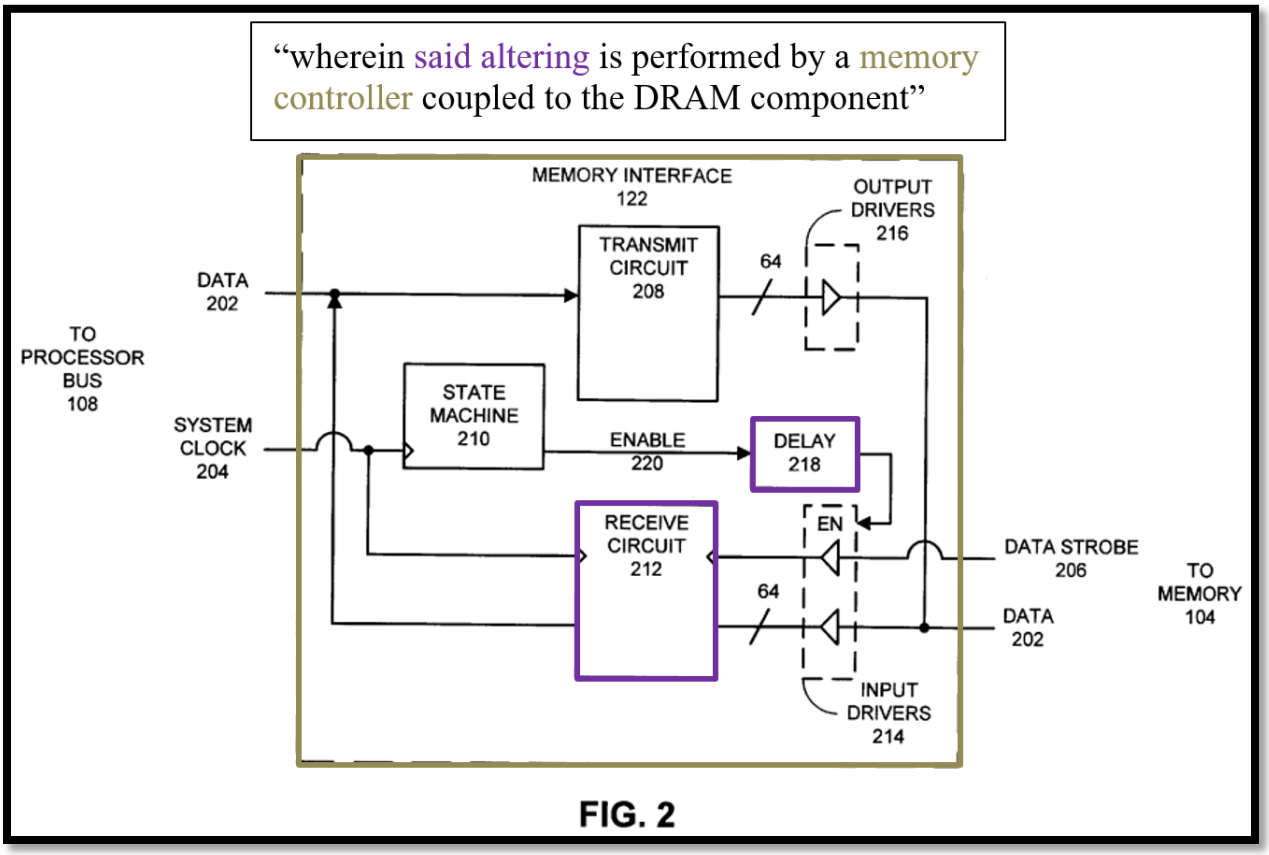
147. For the reasons I have discussed previously, *Johnson* in view of *Jeddeloh* discloses *the method of claim 1*. *See supra* Section III(F)(1). Additionally, *Johnson* explicitly discloses a memory device "may be any type of **DRAM device including an SLDRAM**." Ex. 1004 at 8:35-37 (emphasis added). The memory device contains the calibration structure as described in Claim 1 and is an "integrated memory circuit[.]" Ex. 1004 at 13:59-14:6, Claim 67; 15:30-45, Claim 86 ("a memory circuit formed on a same integrated circuit"). Thus, *Johnson* teaches *wherein the integrated circuit device comprises a DRAM component*.

3. *Claim 3 – The method of claim 2, wherein said altering is performed by a memory controller coupled to the DRAM component.*

148. For the reasons I have discussed previously, *Johnson* in view of *Jeddeloh* discloses *the method of claim 2*. *See supra* Section III(F)(2). *Johnson* also discloses a memory controller coupled to the SLDRAM modules that achieves a timing calibration for signals sent to the SLDRAM module. Ex. 1004 at 1:42-54. The SLDRAM receives "command and FLAG data from a memory controller." *Id.* at 1:27-30. "One of the several calibration procedures which is performed in current SLDRAM devices is a timing synchronization of clock signals CCLK (command clock signal) and DCLK (data clock signal) with data provided on an

incoming command path CA and FLAG path (for the CCLK signal) and on the data paths DQ (for the DCLK signal) so that incoming data is correctly sampled." *Id.* at 1:42-48. The memory controller "achieves this timing calibration at system initialization[.]" *Id.* at 1:48-50. A POSITA would have recognized that the memory controller in *Johnson* is capable of performing the said altering as is disclosed in *Jeddeloh*.

149. Additionally, *Jeddeloh* describes a memory controller (e.g., memory interface 122) that includes "state machine 210, transmit circuit 208, receive circuit 212, input drivers 214 and output drivers 216" Ex. 1005 at 4:35-38. The memory interface 122 receives "data signal 202 and data strobe signal 206 from memory 104" which can be seen on the right side of FIG. 2. *Id.* at 4:39-40. The memory interface 122 is coupled to data signal 202 and system clock 204 which can be seen on the left side. *Id.* at 4:41-42. I have replicated FIG. 2 of *Jeddeloh* below and have provided annotations to clearly show that *said altering is performed by a memory controller*.

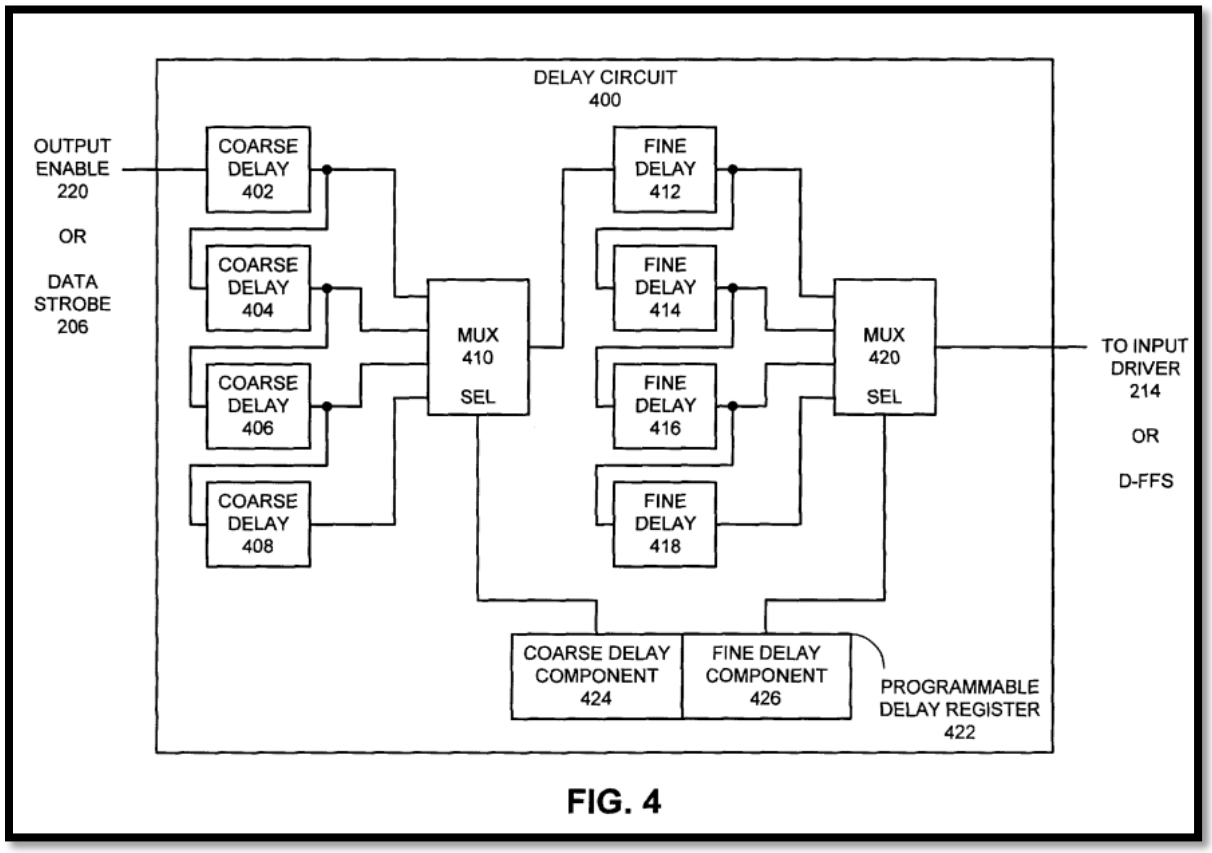


Reproduced from *Jeddeloh* (Annotated)

Id. at 3, annotated.

150. I have highlighted receive circuit 212 in FIG 2 as receive circuit 212 includes delay circuits 314 and 316 (shown in FIG. 3) which also perform the *said altering* as previously described in Claim 1(d)(i). With respect to delay circuit 218, *Jeddeloh* states: "For alignment purposes, enable signal [220] passes through delay circuit 218, which can be adjusted to compensate for skew between enable signal 220 and data signal 202. Delay circuit 218 is described in more detail below with

reference to FIG. 4." *Id.* at 5:2-6. *See supra* Section III(F)(1). FIG. 4 is shown below:



Reproduced from *Jeddeloh* (Annotated)

Id. at 5, annotated.

151. In *Jeddeloh*, the programmable delay circuit 400 shown represents "**the internal structure of delay circuit 218 from FIG. 2, or delay circuits 314 and 316 from FIG. 3**." *Id.* at 5:56-58 (emphasis added). An enable signal 220 is received by the programmable delay circuit 400 which "produces a delayed output that feeds into an enable input of input drivers 214 to enable driving of input

drivers 214." *Id.* at 5:58-61. Programmable delay circuit 400 also "**receives data strobe signal 206 and produces a delayed output** that feeds into a clock input of a D-flip-flop in order to latch a data signal into the D-flip-flop." *Id.* at 5:61-65. Delay elements, such as coarse delay 402 or fine delay 412, are included in delay circuit 400 to perform numerous delays by feeding different combinations of the delay elements into the multiplexers. *Id.* at 5:66-6:8.

152. A POSITA would have understood that the memory controller of *Johnson* would have been capable of performing the phase altering to delay the command, data, and sampling signals as described by *Jeddeloh*. As I have previously explained, a POSITA would have been able and motivated to apply the teachings of *Jeddeloh* to *Johnson*. *See supra* Section III(F)(1)(e). For example, both *Johnson* and *Jeddeloh* describe a calibration (e.g., synchronization) technique to manipulate (e.g., delay) command, data, and/or sampling signals in an integrated circuit device such as a memory device, a DRAM component, a memory controller, etc. Ex. 1004 at 2:44-53 and Ex. 1005 at Abstract. Moreover, both patents were filed by Micron Technology and only about a year apart from one another. Given that both *Johnson* and *Jeddeloh* concern similar issues in the same technical field (high-speed computer memory) and were developed within the same company, a POSITA would have been aware of the teachings found in *Johnson* or *Jeddeloh*.

153. A POSITA would have been motivated to incorporate *Jeddeloh's* explicit teachings of a memory controller delaying (e.g., phase altering) signals in the integrated circuit system described by *Johnson*. *Johnson* provides a substantially similar architecture, with an SLDRAM module coupled to a memory controller. The memory controller of *Johnson* achieves a "timing calibration at system initialization[.]" Ex. 1004 at 1:48-50. A POSITA would have understood that the memory controller of *Johnson* is capable of performing synchronizing functions, such as delays on signals as described in *Jeddeloh*. *See* Ex. 1005 at FIG. 2 (illustrating the delay circuit 218 and receive circuit 212 in the memory interface 122); *see also supra* Section III(A); Ex. 1017 at 1 ("To ensure orderly access to the shared memory (RAM), a memory controller is provided whose **function is to synchronize access to the memory**." (emphasis added)).

154. A POSITA would have been motivated to modify *Johnson* such that the memory controller, instead of the individual memory modules, includes the delay circuitry to realize several advantages recognized in the art, including system flexibility, reduced complexity and cost, power efficiency, and compatibility. *See supra* Section III(A). Indeed, such a combination would be nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. In light of these reasons, *Johnson*

in view of *Jeddeloh* discloses *wherein said altering is performed by a memory controller coupled to the DRAM component*.

4. *Claim 4 – The method of claim 2, wherein the DRAM component comprises a DDR DRAM component.*

155. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *the method of claim 2*. *See supra* Section III(F)2. *Johnson* also explicitly discloses an SLDRAM component that "is a **double data rate device**[.]" Ex. 1004 at 1:26-27; *see also id.* at 2:44-47 ("The present invention provides correct alignment of data entering a memory module, e.g., **an SLDRAM module**, on a plurality of incoming data paths in both a serial and parallel direction." (emphasis added)). *Johnson* also states that the "memory device may be any type of DRAM device including an SLDRAM." Ex. 1004, 8:36-38. A POSITA would have understood "any type of DRAM" to include DDR DRAM. *See supra* Section III(A)(2). *Johnson* explains that memory devices were, and are, constantly evolving for faster speed and higher memory density. *Id.* at 1:11-12. As was known by a POSITA and described in *Johnson*, SLDRAM was a type of innovative DRAM that was comparable to and backwards compatible with DDR DRAM. *See supra* Section III(A)(3); Ex. 1014 at 1 ("The emerging standard for DDR adds data clocking on botch clock edges and a return clock[.] … SLDRAM builds on the features of SDRAM and DDR … [with] full compatibility from

generation to generation."); Ex. 1014 at 2 ("SDRAM, DDR, and SLDRAM all use a DRAM core that has a page-mode cycle time of roughly 10 ns."). DRAM devices evolved into DDR SDRAM which evolved into SLDRAM, which "is the subject of much current industry interest." Ex. 1004 at 1:14-20. *Johnson* suggests that the memory device "may be **any type of DRAM device** including an SLDRAM." *Id.* at 8:35-37 (emphasis added).

156. To the extent *Johnson* may not explicitly teach *wherein the DRAM component comprises a DDR DRAM component*, a POSITA would have known to, and been motivated to, modify *Johnson* based on the explicit teachings of *Jeddeloh*. For example, *Jeddeloh* explains the memory can be any type of memory "with a clocked interface that returns data along with a strobe signal for latching the data during read operations" which includes "memory implementing the DDR interface standard." Ex. 1005 at 3:54-56.

157. Claim 1 of *Jeddeloh* also states "the random access memory is configured to adhere to the double data rate (DDR) memory interface standard" *Id.* at Claim 1. *Jeddeloh* suggests strobed memory modules, such as DDR DRAM in *Jeddeloh* and SLDRAM in *Johnson*, can utilize the circuitry of "delay circuits 314 and 316 [which] can be programmed to precisely synchronize data strobe signal 206 with data signal 202." *Id.* at 5:31-33.

158. *Johnson* clearly describes the SLDRAM module as having similar characteristics as DDR DRAM, such as "a double data rate[.]" Ex. 1004 at 1:26-27. Both *Johnson* and *Jeddeloh* describe a device "which uses both the positive- and negative-going edges of a clock cycle to READ and WRITE data to the memory cells[.]" *Id.* at 1:27-29. A POSITA would have recognized *Johnson* and *Jeddeloh* both mention DDR for their respective memory components. A POSITA would have appreciated incorporating DDR into the integrated circuit system of *Johnson* to realize numerous advantages.

159. For example, as would have been understood by a POSITA, the DDR standard was already widely adopted at the time of the '835 Patent, thus adhering to DDR would allow a memory system to have better compatibility, availability, support, and cost efficiency. *See supra* Section III(A); Ex. 1013 at 2 ("The company estimates the sales of DDR SDRAM could total US$ 380 million for [2001], equaling nearly 21% of the rapidly growing DDR market. Hyundai expects that the adoption of DDR SDRAM begun by Compaq and Hewlett Packard will rapidly extend to other PC makers such IBM, Gateway and Dell as well as major Taiwanese motherboard makers, boosting the need for the cutting-edge chip.").

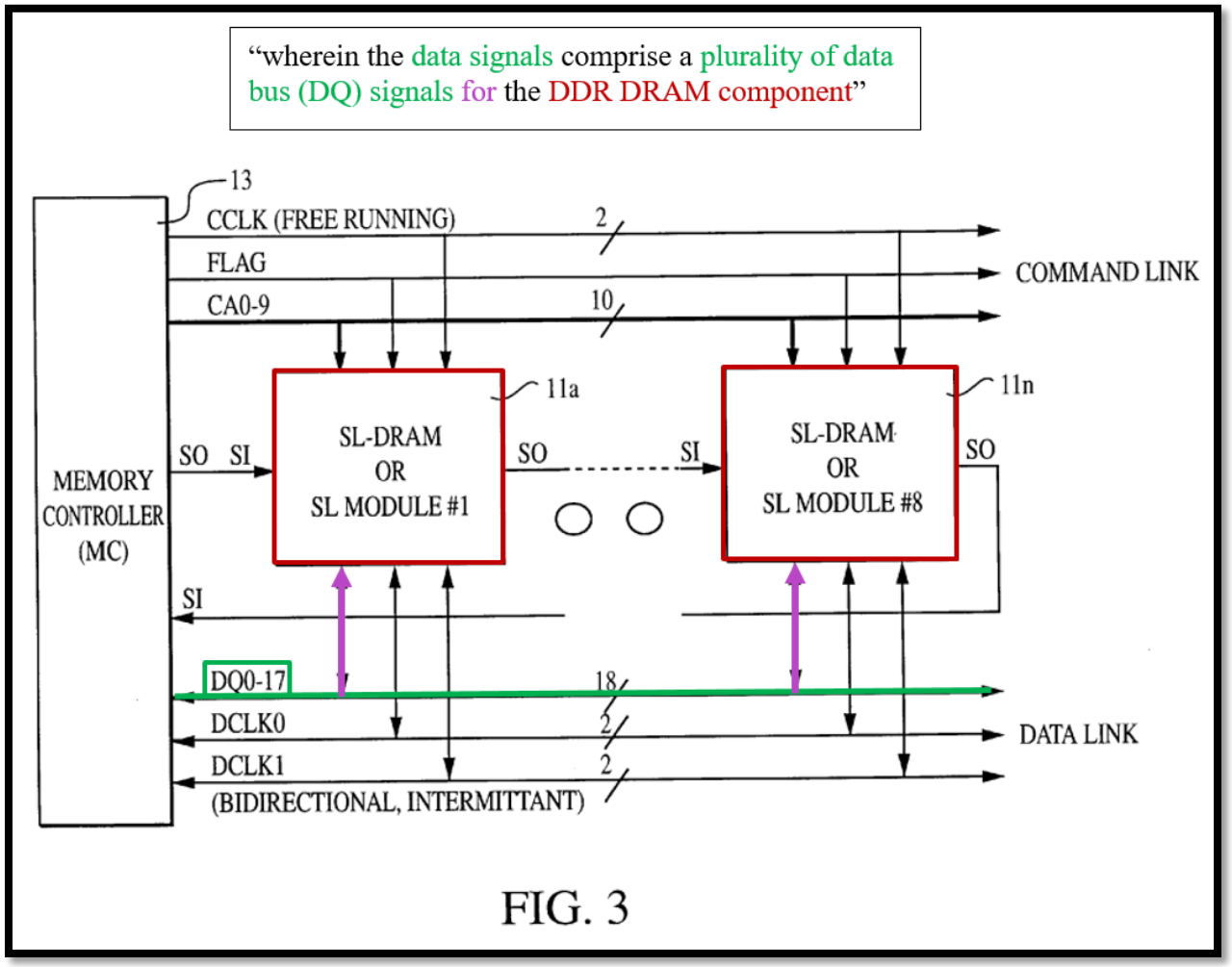
160. Moreover, DDR was implemented in systems to provide high data rates since, by definition, DDR provides a double data rate. *See supra* Section III(A); Ex. 1012 at 10 ("DDR SDRAM (double data rate synchronous DRAM) is a

type of DRAM that realizes twice the data transfer rate of conventional SDRAM[.]"). A POSITA would have been motivated to use a DDR DRAM module, as described in *Jeddeloh*, instead of the SLDRAM module of *Johnson* as this would have been nothing more than simple substitution of one known element for another to obtain predictable results with a reasonable expectation of success. For these reasons, *Johnson* in view of *Jeddeloh* discloses *wherein the DRAM component comprises a DDR DRAM component*.

5. *Claim 5 – The method of claim 4, wherein the data signals comprise a plurality of data bus (DQ) signals for the DDR DRAM component.*

161. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *the method of claim 4*. *See supra* Section III(F)(4). Additionally, as I have previously explained, *Johnson* discloses *data signals* which *comprise a plurality of data bus (DQ) signals*. These data signals are *for the DDR DRAM component* in the *Jeddeloh*-modified *Johnson* method.

162. For example, *Johnson* explains data is provided on "data paths DQ[.]" Ex. 1004 at 1:46-48. Further, the "bi-directional data bus DQ0-17 is provided between memory controller 13 and each of the SLDRAM modules 11 a…11 n[.]" *Id.* at 3:40-43. Annotated FIG. 3 of *Johnson* is provided below:



Reproduced from *Johnson* (Annotated)

Id. at 3, annotated.

163. A control latch is used to "latch in incoming data on the **data bus DQ**." *Id.* at 4:25-26 (emphasis added). A POSITA would have understood that data signals transmitted on data bus DQ would be considered DQ signals. Moreover, *Johnson* explicitly illustrates "the timing relationship of the clock signal CCLK,

the FLAG signal, the command bus signal CMD, **a data bus signal DQ**/DBUS and a data strobe signal DCLK" in FIG. 5. *Id.* at 4:59-65 (emphasis added).

164. Using the DDR teachings found in *Jeddeloh*, a POSITA would have been motivated to combine *Johnson* with *Jeddeloh* to substitute the SLDRAM module with a DDR DRAM module for the reasons I provided previously, as such a such a substitution would be nothing more than a simple substitution of one known element for another to obtain predictable results. *See supra* Section III(F)(4). Thus, the data bus signals DQ disclosed in *Johnson* would carry data from the memory controller for writing to the DDR DRAM component and carry data from the DDR DRAM component to the controller for reading instead of the SLDRAM component. Additionally, to conform to the DDR standards when using a DDR DRAM module, a POSITA would have understood to use DQ signals as the data signals for the DDR DRAM module as specified in the standard. *See* Ex. 1021 at 11 ("[DQ is the symbol for the] data bus[.] … LDQS corresponds to the data on DQ0–DQ7[.]"). In view of this, *Johnson* in view of *Jeddeloh* discloses *wherein the data signals comprise a plurality of data bus (DQ) signals for the DDR DRAM component*.

6. *Claim 6 – The method of claim 5, wherein the sampling signals comprise a plurality of sampling bus (DQS) signals for the DDR DRAM component.*

165. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *the method of claim 5*. *See supra* Section III(F)(5). Additionally, *Johnson* in view of *Jeddeloh* discloses *sampling signals* which *comprise a plurality of sampling bus (DQS) signals*. These data signals are *for the DDR DRAM component* in the *Jeddeloh*-modified *Johnson* method.

166. For example, *Johnson* describes sampling signals DCLK that are used specifically for strobing of data signals (e.g., DQ). Ex. 1004 at 3:40-47 ("In addition, a bi-directional data bus DQ0-17 is provided between memory controller 13 and each of the SLDRAM modules 11 a…11 n, as are bi-directional data clocks DCLK0 and DCLKI. **The clock DCLK0 is used to strobe input/output data into and out of the SLDRAM modules, a process for which the DCLK1 signal path is also intermittently used**." (emphasis added)). Both sampling signals DCLK0 and DLCK1 are shown in FIG. 3 replicated and annotated below:

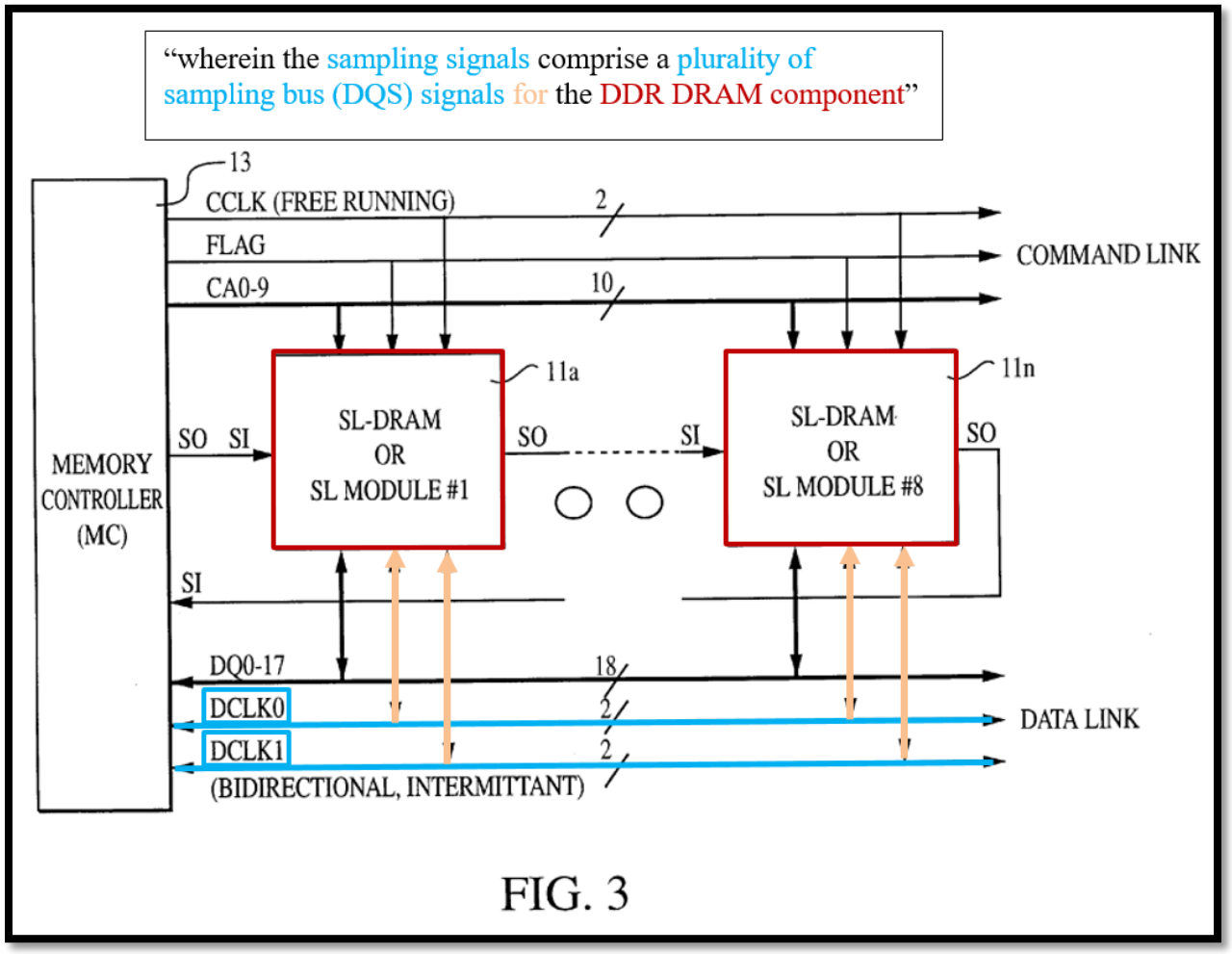


FIG. 3

Reproduced from *Johnson* (Annotated)

Id. at 3, annotated.

167. The clock signals DCLK are provided to the SLDRAM modules, specifically to the control logic circuit 21. *Id.* at 3:60-62. The clock signals DCLK0 and DCLK1 are bi-directional data clocks, which a POSITA would have recognized to be sampling bus signals. *Id.* at 3:43-46. The "data clock DCLK passes through gated buffer 53, delay circuit 55 and is used to control latch 59 to latch in incoming data on the data bus DQ." *Id.* at 4:24-26. Incoming data is

clocked in by DCLK. *Id.* at 4:30-31; *see also id.* at 6:46-48 ("**It should again be noted that** while the FLAG and CA0-9 data paths are aligned to CCLK, **the data paths DQ0-17 are aligned to DCLK**." (emphasis added)).

168. *Jeddeloh* also describes a "strobe signal for latching the data" for memory "implementing the DDR interface standard" similar to DCLK described in *Johnson*. Ex. 1005 at 3:53-56. Using the DDR teachings found in *Jeddeloh*, a POSITA would have been motivated to combine *Johnson* with *Jeddeloh* to substitute the SLDRAM module with a DDR DRAM module for the reasons I provided previously. *See supra* Section III(F)(4). Such a substitution, as described previously, would have been nothing more than simple substitution of one known element for another to obtain predictable results with a reasonable expectation of success. In this *Jeddeloh*-modified system, the sampling signals disclosed in *Johnson* would be used for the DDR DRAM component instead of the SLDRAM component. Additionally, to conform to the DDR standards when using a DDR DRAM module, a POSITA would have understood and would have been motivated to use DQS signals as the sampling signals for the DDR DRAM module as specified in the standard. *See* Ex. 1021 at 5 ("Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver[.]"). In view of this, *Johnson* in view of *Jeddeloh* discloses *wherein the sampling signals*

comprise a plurality of sampling bus (DQS) signals for the DDR DRAM component.

7. *Claim 7*

(a) *7[P]. A system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the system comprising:*

169. I have previously explained why *Johnson* discloses a method *for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device*. *See supra* Section III(F)(1)(a). For the same reasons, *Johnson* discloses *a system* for such. Specifically, *Johnson* discloses "**an improved start-up/reset calibration apparatus** and method for use in a memory device." Ex. 1004 at Abstract (emphasis added). Moreover, in FIG. 3, it would have been apparent to a POSITA that *Johnson* illustrates a memory system implementing the calibration method described.

(b) *[7(a)] a controller configured to generate command signals for accessing an integrated circuit component;*

170. I have previously explained why *Johnson* discloses *generating command signals* to *access an integrated circuit component*. *See supra* Section III(F)(1)(b). *Johnson* describes a memory controller that provides the command signals. Memory control 13 can be seen in FIG. 3 replicated and annotated below:

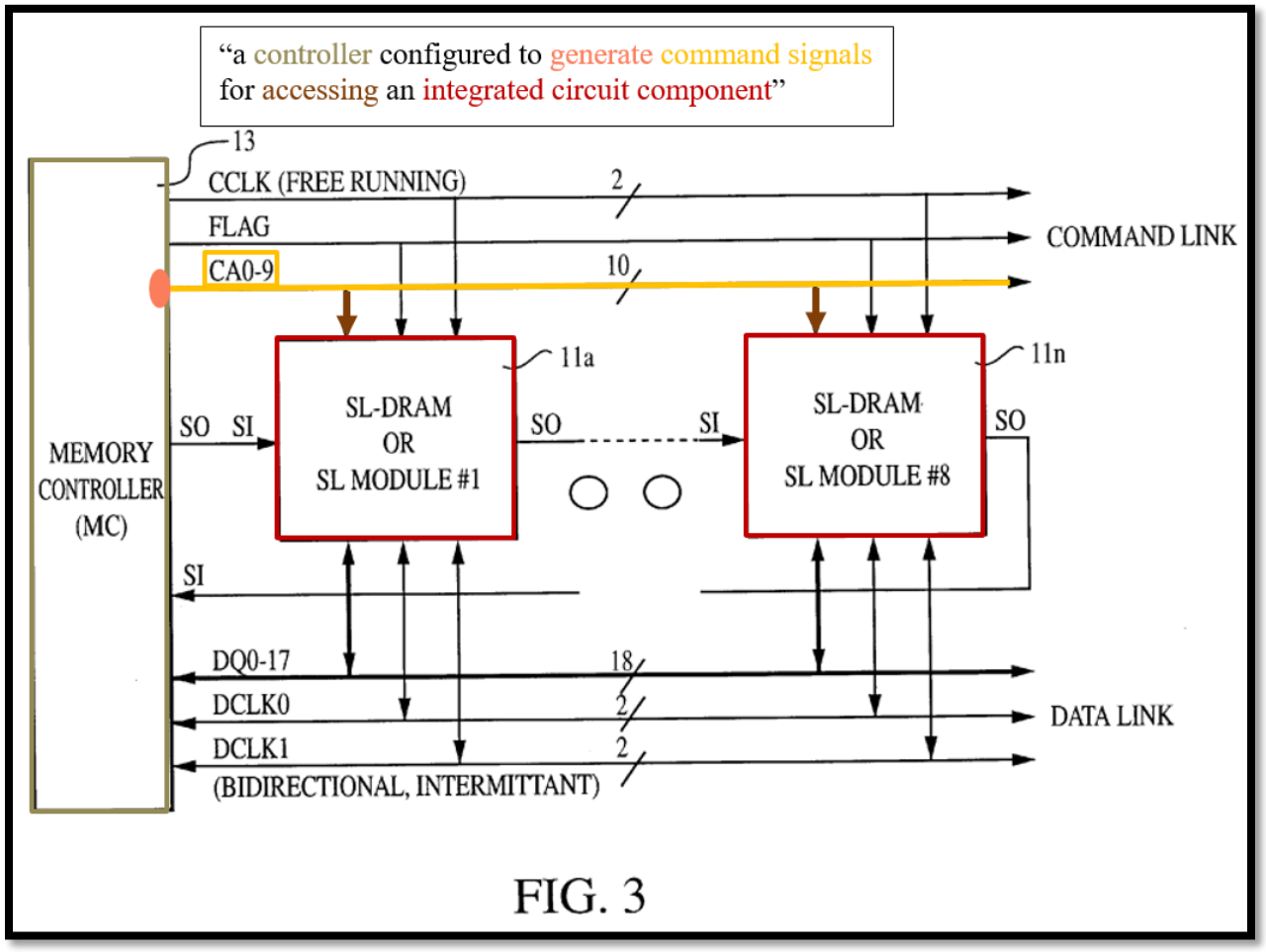


FIG. 3

Reproduced from *Johnson* (Annotated)

Id. at 4, annotated.

171. The SLDRAM "is a double data rate device which uses both the positive- and negative-going edges of a clock cycle to READ and WRITE data to the memory cells and **to receive command** and FLAG **data from a memory controller**." Ex. 1004 at 1:26-30 (emphasis added). In view of the additional disclosure I provided in Claim 1(a), *Johnson* discloses *a controller configured to*

generate command signals for accessing an integrated circuit component. *See supra* Section III(F)(1)(b).

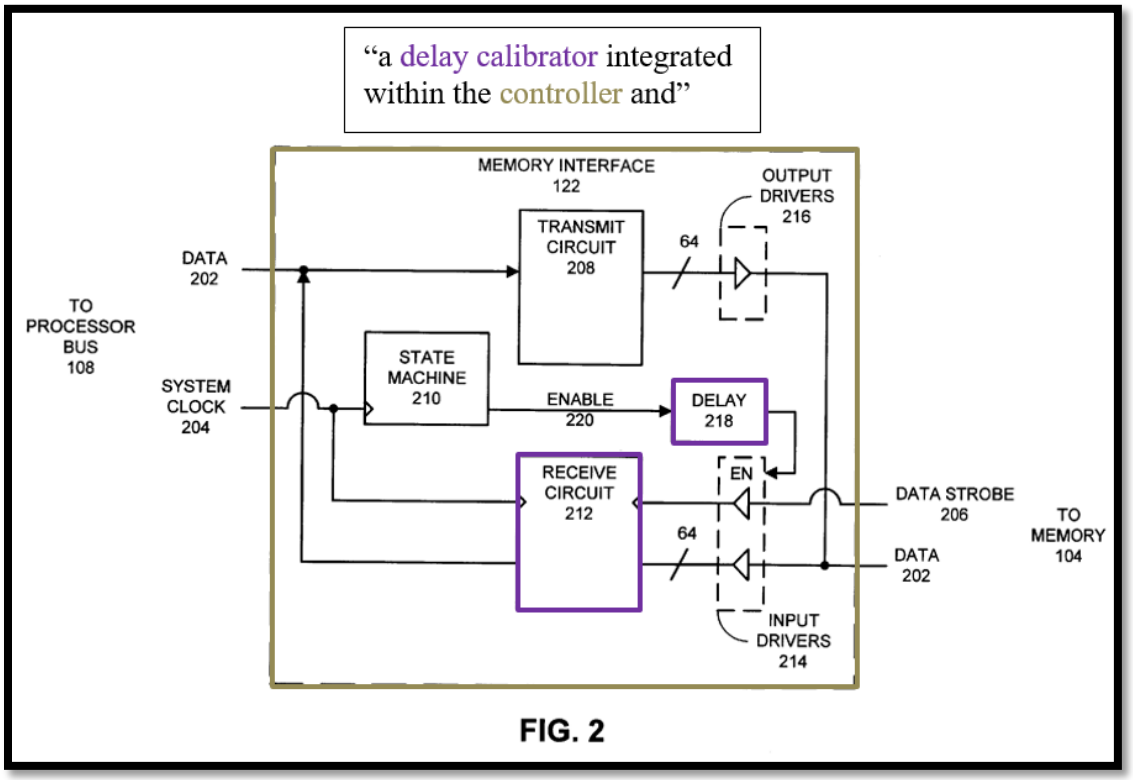
(c) *[7(b)(i)] a delay calibrator integrated within the controller and*

172. *Johnson* describes a memory controller that achieves "timing calibration at system initialization." Ex. 1004 at 1:48-50. While *Johnson* does not explicitly describe the components and/or circuitry of the memory controller, a POSITA would have known that the memory controller in *Johnson* includes a delay calibrator. For example, with respect to conventional calibration procedures, *Johnson* explains "the data bits on each of the incoming data paths [from the memory controller to the SLDRAM module] **is properly serially aligned** with an edge of clock signal CCLK[.]" Ex. 1004 at 2:26-28. To be properly aligned with the clock signal, the data must be phase altered (e.g., delayed) within the memory controller. *Id. Johnson* additionally states that, during the calibration period, the synchronization pattern is applied "by memory controller 13[.]" *Id.* at 5:8-10. Thus, a POSITA would have understood the memory controller of *Johnson* included a delay calibrator.

173. Moreover, a POSITA would have known to incorporate a delay calibrator within the memory controller to provide pre-aligned data as explicitly taught by *Jeddeloh*. The memory controller (e.g., memory interface 122) of

Jeddeloh explicitly includes *a delay calibrator* (e.g., delay circuit 218 and/or delay circuits 314 and 316 in receive circuit 212) *integrated within* it. Ex. 1020 at 197 (*Merriam-Webster's Dictionary*, defining "calibrate" as "to adjust precisely for a particular function"). "For alignment purposes, enable signal [220] passes through delay circuit 218, which can be adjusted to compensate for skew between enable signal 220 and data signal 202." Ex. 1005 at 5:2-5.

174. Receive circuit 212 of memory interface 122 also includes delay circuits 314 and 316. *Id.* at FIGs. 2 and 3. The system "determines delay values to be loaded into delay circuits 218, 314 and 316" and, "[o]nce the optimal delay values are determined, the delay values are programmed into first delay circuit 218 (step 504) and a second delay circuit 314 (step 506)." *Id.* at 6:27-35. I have annotated FIG. 2 which shows the memory interface 122 which I have replicated below.



Reproduced from *Jeddeloh* (Annotated)

Id. at 3, annotated.

175. I have also annotated FIG. 4 which shows a delay circuit, such as delay circuit 218, and reproduced it below.

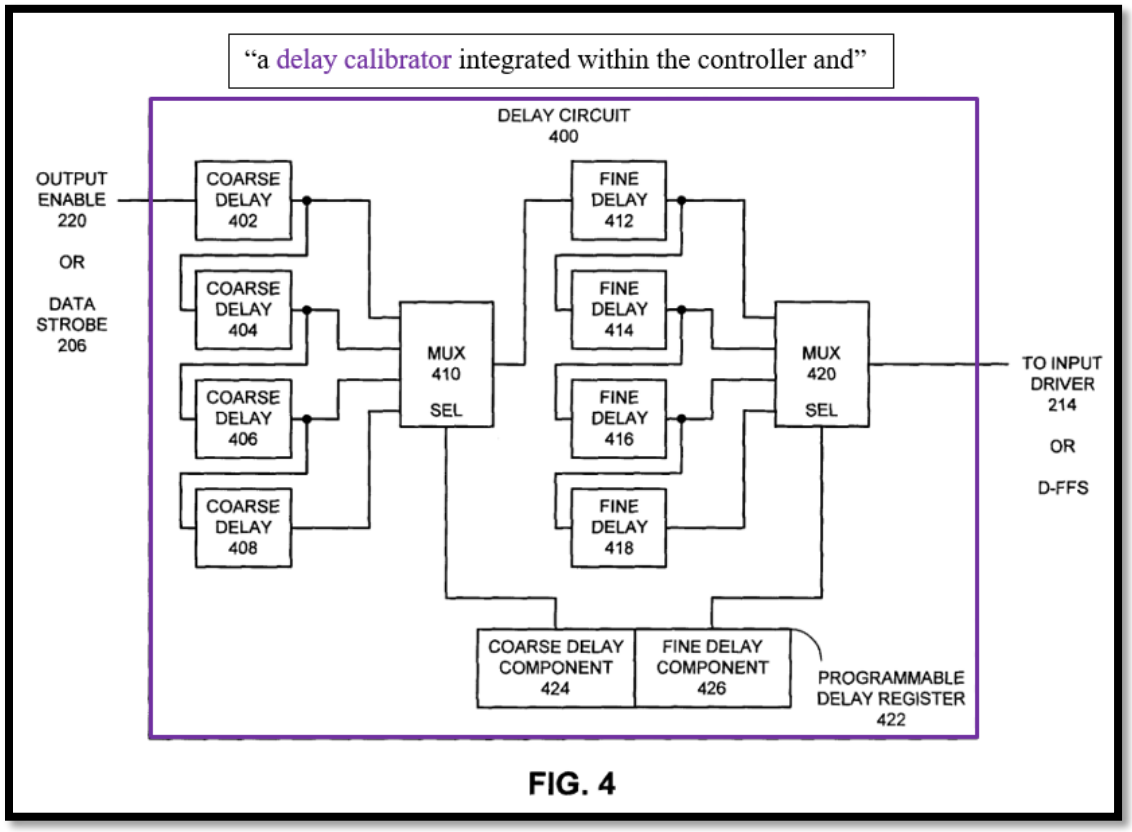


FIG. 4

Reproduced from *Jeddeloh* (Annotated)

Id. at 5, annotated.

176. As previously described, programmable delay circuit 400 "represents the internal structure of **delay circuit 218** from FIG. 2, or **delay circuits 314 and 316** from FIG. 3." *Id.* at 5:56-58. Further, the programmable delay circuit 400 "receives an enable signal 220 and produces a delayed output that feeds into an enable input of input drivers 214 to enable driving of input drivers 214." *Id.* at 5:59-61. Programmable delay circuit 400 alternatively "receives data strobe signal 206 and produces a delayed output that feeds into a clock input of a D-flip-flop in

order to latch a data signal into the D-flip-flop." *Id.* at 5:62-65 (emphasis added). The delay circuits include coarse delay elements 402-408 and fine delay elements 412-418 that are fed into multiplexers (e.g., MUX 410 or 420). *Id.* at 5:66-6:6. Thus, the delay circuits are capable of selecting a specific delay depending on the alignments needs of the system. In other words, the delay circuits act as delay calibrators since they calibrate the delay of signals fed to the DRAM module.

177. For example, the programmable delay register 422 controls MUX 410 and 420 by selecting the combination of delay elements needed to properly alter the signals fed through the delay circuit. *Id.* at 6:9-16. The "programmable delay register 422 is memory mapped so that it can be loaded by a processor." *Id.* at 6:15-16. To the extent not already present in *Johnson*, a POSITA would have known and would have been motivated to include a similar delay circuit within the memory controller of *Johnson* as both *Johnson* and *Jeddeloh* describe calibration techniques to better align data within an integrated circuit, and specifically between a memory controller and a DRAM module. *Johnson's* control logic circuit 21 is "arranged to compare a next data path **to be calibrated** to **a just calibrated** data path and **control the incremental adjustment of the ring delay for the new data path** in the manner described above until a final delay value is selected." Ex. 1004 at 7:25-29 (emphasis added).

178. For similar reasons as I have previously described, a POSITA would have been motivated to combine the teachings of *Jeddeloh* with *Johnson*. *See supra* Section III(F)(1)(e). Moreover, a POSITA would have recognized the benefits from integrating a delay calibrator, such as delay circuit 400 of *Jeddeloh*, into a memory controller, such as memory controller 13 of *Johnson*. By having a delay calibrator within the memory controller, data fed into the SLDRAM modules of *Johnson* could be pre-aligned to provide faster performance rates. For example, the additional alignment would allow for data transfer with smaller windows of valid data, thereby enabling increased data rates, which shrink the windows of valid data. *Johnson* already includes control logic circuit 21 within the SLDRAM modules which "receives and analyzes commands on the CA0-9 bus[, FLAG signal, and clock signals CCLK and DCLK,] and controls the input/output (I/O) access operations of the memory banks 69, 71." Ex. 1004 at 3:57-62. A POSITA would have recognized the benefits of including a delay circuit within memory controller 13 as well.

179. Incorporating a delay calibrator (e.g., delay circuit) integrated within a memory controller, as explicitly taught by *Jeddeloh*, with the memory controller and overall integrated circuit system taught by *Johnson* would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. A POSITA would

have recognized the delay circuit of *Jeddeloh* as a common component of a memory controller, and thus would have been motivated to include it within the memory controller of *Johnson*. By doing so, a POSITA would have realized the advantages described previously, such as faster data rates, better system optimization, and enhanced compatibility. In light of this, *Johnson* in view of *Jeddeloh* discloses *a delay calibrator integrated within the controller*.

(d) *[7(b)(ii)] configured to access data signals conveying data for the integrated circuit device and*

180. For the reasons I have described previously, *Johnson* discloses accessing *data signals* to *convey data for the integrated circuit device*. *See supra* Section III(F)(1)(c). I have also explained why a POSITA would have understood to and would have been motivated to include the delay calibrator of *Jeddeloh* in the memory controller of *Johnson* as it would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. *See supra* Section III(F)(7)(c). The delay calibrator of *Jeddeloh* is *configured to access data signals*.

181. For example, "memory interface 122 receives **data signal 202** and data strobe signal 206 from memory 104 (from FIG. 1)." Ex. 1005 at 4:39-40 (emphasis added). Specifically, "data signal 202 and data strobe signal 206 from memory 104 passes through input drivers 214 into **receive circuit 212**." *Id.* at

4:55-56 (emphasis added). *Johnson's* control logic circuit 21 also accesses data signals, as it is "arranged to compare a **next data path** to be calibrated to a just **calibrated data path** and control the incremental adjustment of the ring delay for the **new data path** in the manner described above until a final delay value is selected." Ex. 1004 at 7:25-29 (emphasis added). The memory controller, and the delay calibrator, of the *Jeddeloh*-modified system of *Johnson* accesses data signals. Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

(e) *[7(b)(iii)] to access sampling signals for controlling sampling of the data signals,*

182. For the reasons I have described previously, *Johnson* discloses accessing *sampling signals* to *control sampling of the data signals*. *See supra* Section III(F)(1)(d). I have also explained why a POSITA would have understood to and would have been motivated to include the delay calibrator of *Jeddeloh* in the memory controller of *Johnson* as it would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. *See supra* Section III(F)(7)(c). The delay calibrator of *Jeddeloh* is *configured to access sampling signals*.

183. For example, "memory interface 122 receives data signal 202 and **data strobe signal 206** from memory 104 (from FIG. 1)." Ex. 1005 at 4:39-40 (emphasis added). Specifically, "data signal 202 and data strobe signal 206 from

memory 104 passes through input drivers 214 into receive circuit 212." *Id.* at 4:55-56. *Johnson's* control logic circuit 21 also accesses sampling signals, as it "receives … the **clock signals CCLK, DCLK**." Ex. 1004 at 7:25-29 (emphasis added). The memory controller, and the delay calibrator, of the *Jeddeloh*-modified system of *Johnson* accesses sampling signals. Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

(f) *[7(c)(i)] wherein the delay calibrator is further configured to systematically alter a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device; and*

184. For the reasons I have described previously, *Johnson* in view of *Jeddeloh* discloses accessing *systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device*. *See supra* Section III(F)(1)(e). I have also explained why a POSITA would have been motivated to include the delay calibrator of *Jeddeloh* in the memory controller of *Johnson* as it would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. *See supra* Section III(F)(7)(c). The delay calibrator of *Jeddeloh* is *configured* to perform the systematic altering of the phase shifts as seen with coarse and fine delay elements. Ex. 1005 at FIG. 4.

185. A POSITA would have appreciated the similarities between *Jeddeloh's* delay calibrator that is configured to alter a phase shift of sampling (and data) signals, *Johnson's* ring delays that are configured to alter a phase shift of data and command signals, and *Johnson's* delay and delay lock loop that are configured to alter a phase shift of sampling signals. In this way, the *Jeddeloh*-modified system of *Johnson* would include a delay calibrator within the memory controller that is configured to calibrate delays depending on the alignment needed for command, data, and sampling signals. A POSITA would have been motivated to combine *Jeddeloh* with *Johnson* as described since it would have been nothing more than combining prior art elements according to known methods to yield predictable results. Indeed, based on the disclosure of *Johnson*, a POSITA would have had a reasonable expectation of success doing so. For these reasons, *Johnson* in view of *Jeddeloh* discloses this limitation.

(g) *[7(c)(ii)] wherein the valid operation range includes an optimal operation point for the integrated circuit device.*

186. For the reasons provided previously, *Johnson* discloses *wherein the valid operation range includes an optimal operation point for the integrated circuit device*. *See supra* Section III(F)(1)(f).

8. *Claim 8 – The system of claim 7, wherein the integrated circuit device comprises a DRAM component.*

187. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *the system of claim 7*. *See supra* Section III(F)(7). I have additionally explained why *Johnson* discloses *wherein the integrated circuit device comprises a DRAM component*. *See supra* Section III(F)(2). Thus, *Johnson* in view of *Jeddeloh* discloses Claim 8.

9. *Claim 9 – The system of claim 8, wherein the DRAM component comprises a DDR DRAM component.*

188. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *the system of claim 8*. *See supra* Section III(F)(8). I have additionally explained why *Johnson* in view of *Jeddeloh* discloses *wherein the DRAM component comprises a DDR DRAM component*. *See supra* Section III(F)(4). Thus, *Johnson* in view of *Jeddeloh* discloses Claim 9.

10. *Claim 10 – The system of claim 9, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.*

189. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *the system of claim 9*. *See supra* Section III(F)(9). I have additionally explained why *Johnson* in view of *Jeddeloh* discloses *wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component*. *See supra* Section III(F)(5). Thus, *Johnson* in view of *Jeddeloh* discloses Claim 10.

11. *Claim 11 – The system of claim 10, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.*

190. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *the system of claim 10*. *See supra* Section III(F)(10). I have additionally explained why *Johnson* in view of *Jeddeloh* discloses *wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component*. *See supra* Section III(F)(6). Thus, *Johnson* in view of *Jeddeloh* discloses Claim 11.

12. *Claim 12*

(a) *12[P]. In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, the method comprising:*

191. I have previously explained how *Johnson* discloses *a method for* automatically calibrating *intra-cycle timing relationships between command signals, data signals, and sampling signals for* an integrated circuit device to find a valid operation range (i.e., an *operating mode*). *See supra* Section III(F)(1)(a). I have also explained how *Johnson* discloses *a DRAM component*. *See supra* Section III(F)2. Specifically, *Johnson* discloses systematically altering timing relationships between the signals *for the DRAM component*. *Id.* Further, I have explained how *Johnson* in view of *Jeddeloh* discloses a delay calibrator integrated within *a*

memory controller that is configured to perform the altering. *See supra* Section III(F)(7)(f) Thus, *Johnson* in view of *Jeddeloh* discloses this limitation.

(b) *[12(a)] generating command signals to access a DRAM component;*

192. I have previously explained how *Johnson* discloses *generating command signals to access an integrated circuit component* such as an SLDRAM component. *See supra* Section III(F)(1)(b). I have also explained how the SLDRAM component is *a DRAM component*. *See supra* Section III(F)(2) Therefore, *Johnson* discloses this limitation.

(c) *[12(b)] accessing data signals to convey data for the DRAM component;*

193. I have previously explained how *Johnson* discloses *accessing data signals to convey data for the integrated circuit component* such as an SLDRAM component. *See supra* Section III(F)(1)((c). I have also explained how the SLDRAM component is *a DRAM component*. *See supra* Section III(F)(2). Therefore, *Johnson* discloses this limitation.

(d) *[12(c)] accessing sampling signals to control sampling of the data signals; and*

194. I have previously explained how *Johnson* discloses *accessing sampling signals to control sampling of the data signals*. *See supra* Section III(F)(1)(d). Therefore, *Johnson* discloses this limitation.

(e) *[12(d)] systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operating range of the DRAM component.*

195. I have previously explained how *Johnson* in view of *Jeddeloh* discloses *systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operating range of the integrated circuit device* such as an SLDRAM component. *See supra* Section III(F)(1)(e). I have also explained how the SLDRAM component is *a DRAM component*. *See supra* Section III(F)(2). Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

13. *Claim 13*

(a) *13[P]. The method of claim 12, further comprising:*

196. For the reasons I provided previously, *Johnson* in view of *Jeddeloh* discloses *the method of claim 12*. *See supra* Section III(F)(12).

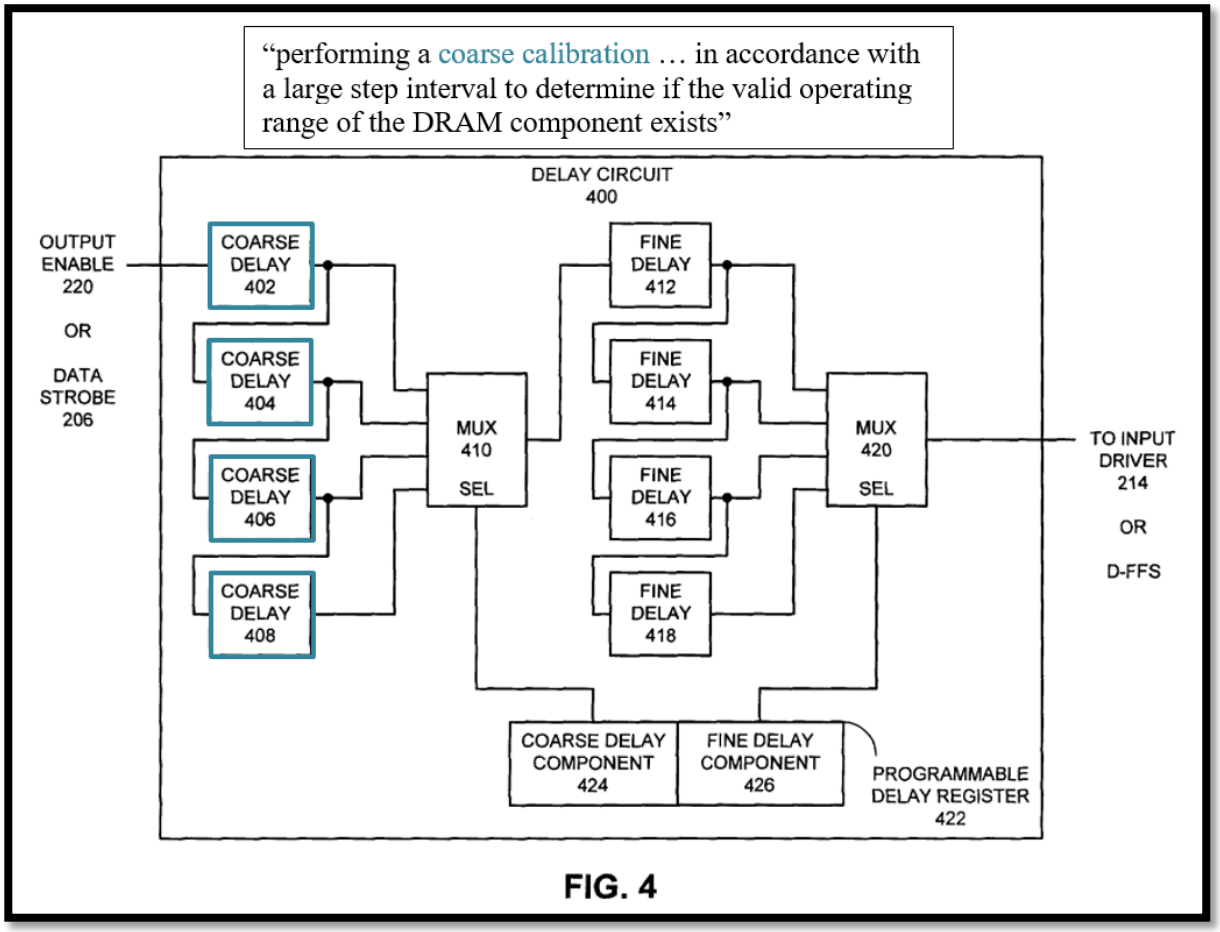
(b) *[13(a)] performing a coarse calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a large step interval to determine if the valid operating range of the DRAM component exists; and*

197. As previously explained, *Johnson* in view of *Jeddeloh* discloses *altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals to determine* a *valid operating range of*

the DRAM component. *See supra* Section III(F)(12)(e). Additionally, *Johnson* discloses a control logic circuit that "steps through all possible delay positions of ring delays 27 and 29 as the data sampling is performed and stores patterns representing which delay values for the ring delays 27 and 29 provide for a correct sampling and recognition of the 2^N bit pattern." Ex. 1004 at 4:37-41. The control logic circuit also "steps through all data paths, aligning the ring delays of a path under calibration to an immediate previously calibrated data path until all data paths have been calibrated." *Id.* at 7:64-67. By stepping through all possible delay positions and identifying those that yield correct sampling, *Johnson* determines *a valid operation range*.

198. *Jeddeloh* explicitly describes coarse delay elements and fine delay elements included in the circuitry of the programmable delay circuit. A "coarse" adjustment, especially when compared with a "fine" adjustment, uses a large interval (e.g., a coarse interval) to make an adjustment. *See supra* Section III(A). Often, coarse adjustments are made to find the general optimal value range while fine adjustments are subsequently made to find a more precise optimal value range. For example, the input "into programmable delay circuit 400 passes through a chain of coarse delay elements 402, 404, 406 and 408. The outputs of coarse delay elements 402, 404, 406 and 408 feed into MUX 410. MUX 410 selects between the outputs of coarse delay elements 402, 404, 406 and 408 to generate an output[.]"

Id. at 5:65-6:4. This multiplexer is controlled by coarse delay component 424, thus the delay circuit has a coarse adjustment through MUX 410. *Id.* at 6:10-14. I have provided an annotated version of FIG. 4 illustrating the programmable delay circuit 400 below.



Reproduced from *Jeddeloh* (Annotated)

Id. at 5, annotated.

199. As seen, the programmable delay circuit includes "a coarse delay adjustment mechanism and a fine delay adjustment mechanism." *Id.* at 2:40-41.

The "[p]rogrammable delay circuit 400 represents the internal structure of delay circuit 218 [] or delay circuits 314 and 316," all of which are in *Jeddeloh*'s memory interface 122. Ex-1005, 5:54-58; *see also id.*, 4:56-60, 5:2-7, 5:16-33. A POSITA would have understood a coarse delay element configured to perform coarse adjustments would do so with a large step interval. Thus, a POSITA would have appreciated the fact that the coarse delay elements described in *Jeddeloh* perform adjustments based on a large step interval.

200. A POSITA would have known to incorporate the circuitry of *Jeddeloh's* delay circuit that is configured to perform a coarse calibration by altering the phase shift of the sampling signals into the delay elements taught by *Johnson* that are configured to alter the phase shift of the command and data signals. Indeed, a POSITA would have recognized the common practice of first performing a coarse adjustment to find an acceptable range of values and then subsequently performing a fine adjustment to find a more precise range as this has been practiced in the field of programming, mathematics, and general approximation long before the filing of the '835 Patent. *See supra* Section III(A); Ex. 1018 at 1 ("A number of authors have developed 'coarse-to-fine' processing strategies[.]"). *Johnson's* delay elements are configured to delay both the command signals and the data signals. *See supra* Section III(F)(1)(e). Additionally, *Jeddeloh* describes initializing "the first delay value and the second delay value to

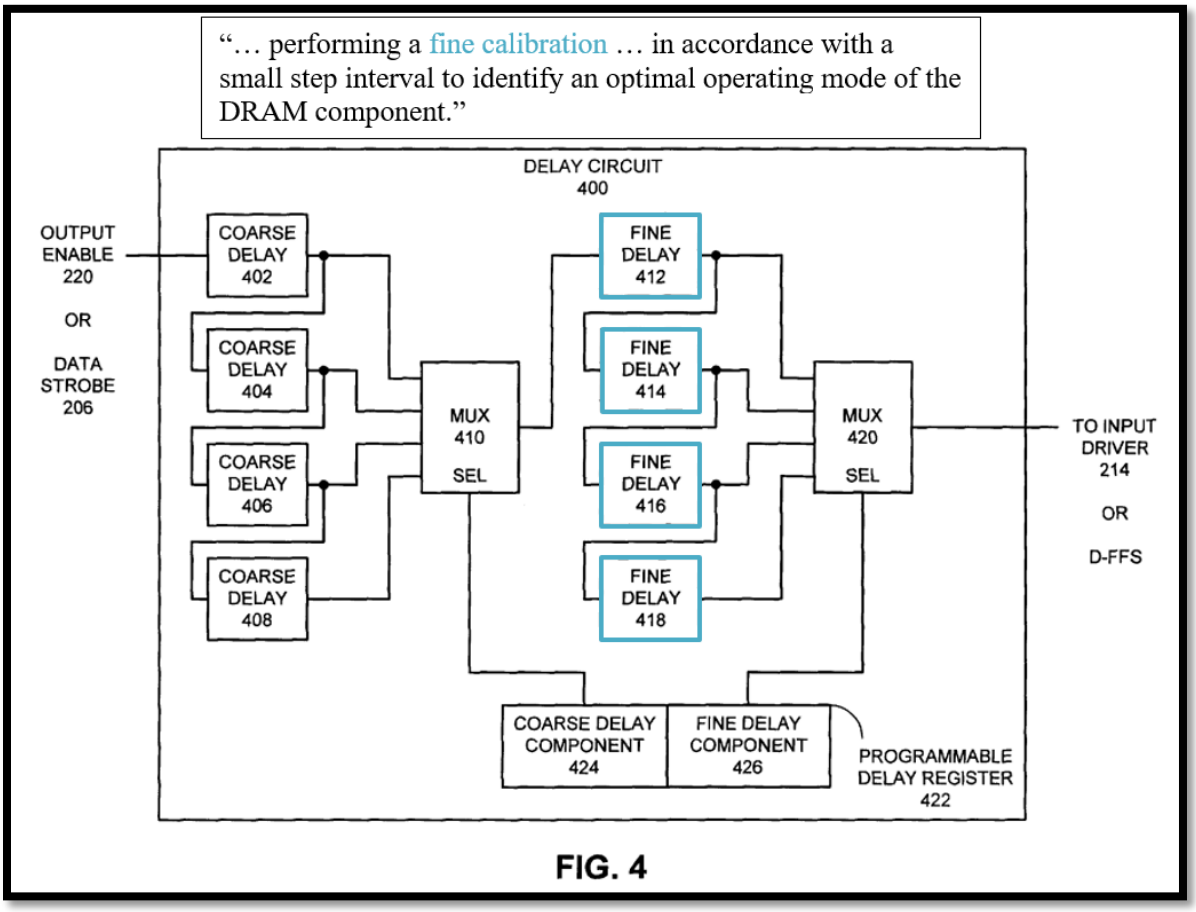
their lowest possible values[.] Ex-1005, 7:7-9. The system then attempts to read a written value to determine if "the read operation [is] successful." *Id.*, 7:12-14. The values are incremented and, once the system has attempted "all possible combinations of delay values," the system "selects a first [and a second] delay value in the middle of a **valid range of first [and second] delay values** [respectively.]" *Id.*, 7:14-24. A POSITA would have understood that selecting delay values in the "valid range" includes "determin[ing] if the valid operating range of the DRAM component exists," at least because determining that the "valid range" exists and identifying its boundaries are prerequisite to selecting values within that range.

201. A POSITA would have been motivated to incorporate the coarse delay elements of *Jeddeloh* within the delay elements of *Johnson* to correspondingly delay command, data, and sampling signals. *Johnson* already discloses finding an acceptable range of delay values and, therefore, would benefit from having an efficient adjustment technique as described by *Jeddeloh*. Ex. 1004 at 4:41-43 ("In this manner, control logic circuit 21 establishes an 'eye' or 'window' of acceptable delays for each of the ring delays 27 for the command data paths CA0-9[.]"). By first performing a coarse delay adjustment followed by a fine delay adjustment, the total number of incremental adjustments required is reduced, resulting in more efficient and faster adjustment.

202. Including the explicitly taught delay circuit with coarse delay elements of *Jeddeloh* within the memory controller of *Johnson* to not only alter a phase shift of the sampling signals (as taught by *Jeddeloh* and *Johnson*), but also alter a phase shift of the data and command signals (as taught by *Johnson*) would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. In this way, the memory controller of *Johnson* would include delay circuitry that can perform a coarse calibration with a large step interval. Thus, *Johnson* in view of *Jeddeloh* discloses this limitation.

> (c) *[13(b)] if the valid operating range exists, then performing a fine calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a small step interval to identify an optimal operating mode of the DRAM component.*

203. *Johnson* discloses control logic that establishes acceptable delays for the signals. *See supra* Section III(F)(13)(b) I have also explained how *Jeddeloh* teaches first performing a coarse delay calibration and then subsequently performing a fine delay calibration. *Id.* FIG. 4, which I have annotated below, shows multiple fine delay elements.



Reproduced from *Jeddeloh* (Annotated)

Id. at 5, annotated.

204. *Jeddeloh* explains that "MUX 410 selects between the outputs of coarse delay elements 402, 404, 406 and 408 to generate an output that feeds into a chain of fine delay elements 412, 414, 416 and 418." Ex. 1005 at 6:2-8. "The outputs of fine delay elements 412, 414, 416 and 418 feed into MUX 420." *Id.* "MUX 420 selects between the outputs of fine delay elements 412, 414, 416 and 418 to generate an output for delay circuit 400." *Id.* Fine delay component 426

controls MUX 420 such that delay circuit 400 has a fine adjustment through MUX 420. *Id.* at 6:10-14.

205. I have already explained why a POSITA would have understood to, and would have been motivated to, include the circuitry of the delay circuit within the memory controller of *Johnson*. *See supra* Section III(F)(13)(b) Specifically, I explained why a POSITA would have appreciated using a coarse calibration with a subsequent fine calibration to find optimal delays. Therefore, for the same reasons, a POSITA would have included the fine delay elements of *Jeddeloh* when incorporating the circuitry within the memory controller of *Johnson* as it would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. It is consequently my opinion that *Johnson* in view of *Jeddeloh* discloses this limitation.

14. *Claim 14 – The method of claim 13, wherein said performing a coarse calibration comprises simultaneously varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal by a five percent step increase.*

206. For the reasons I provided above, *Johnson* in view of *Jeddeloh* discloses the method of claim 13. *See supra* Section III(F)(13). *Johnson* in view of *Jeddeloh* additionally discloses *wherein said performing a coarse calibration comprises simultaneously varying each of the phase shift of the command signal,*

the phase shift of the data signal, and the phase shift of the sampling signal. For example, the optimal delay in Johnson is achieved by "adjusting the temporal position of the received data bits to achieve a desired bit alignment relative to the clock" which is "accomplished by adjusting a delay in the receiving path of the received data until the received data is properly sampled by the clock and recognized internally." Ex. 1004 at 1:59-64. "Once synchronization has been achieved, that is, the proper delays on the data receiving paths have been set, the memory controller stops sending the SYNC pattern[.]" *Id.* at 1:64-67.

207. The control logic 21 "establishes an 'eye' or 'window' of acceptable delays for each of the ring delays 27 for the command data paths CA0-9 and for ring delay 29 for the FLAG input path." *Id.* at 4:41-43. The window of acceptable delays in *Johnson* is equivalent to a coarse calibration as it is used to establish the general range of acceptable delay values, similar to a calibration with a large (e.g., coarse) step interval. Additionally, as described previously, *Jeddeloh* explicitly includes a plurality of coarse delay elements that feed into a MUX to provide varying delay values. *See supra* Section III(F)(13). While *Johnson* and *Jeddeloh* are silent on the exact percent for the step increase between delay values, a POSITA would have understood to choose a reasonably large percent step increase that allows for a quick calibration process while also finding an acceptable range of delay values as this would be an obvious design choice.

208. In other words, a POSITA would have recognized using *a five percent step increase* as a suitable value for the coarse, or initial, calibration process. With a step increase of five percent, the system would test at most 20 delay possibilities per signal period, allowing the system to quickly find the general area of acceptable delay values. A POSITA would have chosen from a finite number of identified, predictable solutions with a reasonable expectation of success. The range of predictable step increase values for the coarse calibration would include five percent, and, thus, it would be obvious to try for a POSITA.

209. A POSITA would also have understood that calibrating phase shifts of the respective signals would occur *simultaneously*. As explained previously, *Johnson's* calibration technique is performed at initialization (e.g., start-up or reset). *Id.* at 1:36-40. Logically, such calibration would occur all at once and before the memory system is utilized to ensure proper functionality of the memory system. A POSITA would thus have understood that *Johnson's* system performs calibration of the phase shifts all at initialization. Therefore, *Johnson* in view of *Jeddeloh* discloses this claim.

15. *Claim 15 – The method of claim 13, wherein said performing a fine calibration comprises varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal one at a time by a two percent step increase.*

210. For the reasons I provided above, *Johnson* in view of *Jeddeloh* discloses the method of claim 13. *See supra* Section III(F)(13). *Johnson* in view of *Jeddeloh* additionally discloses *wherein said performing a fine calibration comprises simultaneously varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal*. For example, the optimal delay in Johnson is achieved by "adjusting the temporal position of the received data bits to achieve a desired bit alignment relative to the clock" which is "accomplished by adjusting a delay in the receiving path of the received data until the received data is properly sampled by the clock and recognized internally." Ex. 1004 at 1:59-64. "Once synchronization has been achieved, that is, the proper delays on the data receiving paths have been set, the memory controller stops sending the SYNC pattern[.]" *Id.* at 1:64-67.

211. The control logic 21, after window of acceptable delays is established, "determines the 'best' delay value as that value which is approximately in the middle of the window." *Id.* at 4:46-48. Determining the best delay value within the window of acceptable delays in *Johnson* is equivalent to a fine calibration as it is used to find the specific optimal delay value once a range is established, similar to a calibration with a small (e.g., fine) step interval. Additionally, as described previously, *Jeddeloh* explicitly includes a plurality of fine delay elements that feed into a MUX to provide varying delay values. *See supra* Section III(F)(13). While

Johnson and *Jeddeloh* are silent on the exact percent for the step increase between delay values, a POSITA would have understood to choose a reasonably small percent step increase that allows for a precise calibration process after a range of acceptable values is determined as this would be an obvious design choice.

212. In other words, a POSITA would have recognized using *a two percent step increase* as a suitable value for the fine calibration process. A step increase of two percent would allow the system to accurately find an exact delay value that may be passed over during the coarse calibration. A POSITA would have chosen from a finite number of identified, predictable solutions with a reasonable expectation of success. The range of predictable step increase values for the fine calibration would include two percent, and, thus, it would be obvious to try for a POSITA. Moreover, a POSITA would have been motivated to perform the fine adjustments *one at a time*. Identifying the "best" delay values for each of the signals one at a time would conserve system resources by staggering the fine adjustments. Identifying the "best" delay values for each of the signals one at a time would also allow the system to test delays for each signal independently of other system changes. Varying the delay values one at a time, as opposed to simultaneously, would have amounted to nothing more than choosing from a finite number of identified, predictable solutions (simultaneously or one at a time), with

a reasonably expectation of success. Therefore, *Johnson* in view of *Jeddeloh* discloses this claim.

16. *Claim 16 – The method of claim 13, further comprising configuring the memory controller to operate the DRAM component in the optimal operating mode.*

213. For the reasons I provided above, *Johnson* in view of *Jeddeloh* discloses *the method of claim 13*. *See supra* Section III(F)(13). *Johnson* further explains that, once a window of acceptable delays is established, "the control logic circuit 21 **determines the 'best' delay value** as that value which is approximately in the middle of the window." Ex. 1004 at 4:46-48 (emphasis added); *see also supra* Section III(F)(1). Moreover, *Jeddeloh* explicitly states: "Once the **optimal delay values are determined, the delay values are programmed into first delay circuit 218** (step 504) and a second delay circuit 314 (step 506). Ex. 1005 at 6:32-35 (emphasis added). Thus, when applying the teachings of *Jeddeloh* to *Johnson*, the *Jeddeloh*-modified memory controller of *Johnson* is configured *to operate the DRAM component in the optimal operating mode*. A POSITA would have appreciated combining *Jeddeloh's* disclosure with *Johnson's* memory controller as I have extensively described previously since it would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. *See supra* Section III(F)(13). Therefore, *Johnson* in view of *Jeddeloh* discloses this claim.

17. *Claim 17 – The method of claim 12, wherein the DRAM component comprises a DDR DRAM component.*

214. For the reasons I provided previously, *Johnson* in view of *Jeddeloh* discloses *the method of claim 12*. *See supra* Section III(F)(12). Additionally, for the reasons I provided previously, *Johnson* in view of *Jeddeloh* discloses *wherein the DRAM component comprises a DDR DRAM component*. *See supra* Section III(F)(4). Therefore, *Johnson* in view of *Jeddeloh* discloses this claim.

18. *Claim 18 – The method of claim 17, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.*

215. For the reasons I provided previously, *Johnson* in view of *Jeddeloh* discloses *the method of claim 17*. *See supra* Section III(F)(17). Additionally, for the reasons I provided previously, *Johnson* in view of *Jeddeloh* discloses *wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component*. *See supra* Section III(F)(5). Therefore, *Johnson* in view of *Jeddeloh* discloses this claim.

19. *Claim 19 – The method of claim 18, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.*

216. For the reasons I provided previously, *Johnson* in view of *Jeddeloh* discloses *the method of claim 18*. *See supra* Section III(F)(18). Additionally, for the reasons I provided previously, *Johnson* in view of *Jeddeloh* discloses *wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM*

component. *See supra* Section III(F)(6). Therefore, *Johnson* in view of *Jeddeloh* discloses this claim.

20. *Claim 20*

(a) *20[P]. A computer readable media having stored thereon, computer-executable instructions that, if executed by a processor, cause the processor to perform a method for finding an operating mode for a DDR DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the method comprising:*

217. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component*. *See supra* Section III(F)(12). I have also explained why *Johnson* in view of *Jeddeloh* discloses the DRAM component comprises *a DDR DRAM component*. *See supra* Section III(F)(4). *Johnson* states that the memory device "containing the calibration structure and operating as described above may be **used in a processor-based system** of the type shown in FIG. 12. **The processor-based system 90 comprises a processor 94, a memory device 96, and an I/O (input/output) device 92**. The memory device 96 contains the calibration structure operating as described in accordance with the present invention." Ex. 1004 at 8:30-36 (emphasis added). A POSITA

would have understood that, to perform the calibration described in *Johnson* as modified by *Jeddeloh*, executable instructions would be stored on a readable media accessible by *Johnson's* processor. For example, a POSITA would have understood that the I/O device 92 is a thumb drive, hard drive, etc. A POSITA would have understood that the readable media could include any suitable type of memory, such as read-only memory, cache, SRAM, DRAM, or the like. A POSITA would have understood this as a combination of prior art elements according to known methods to yield predictable results with a reasonable expectation of success. Thus, *Johnson* in view of *Jeddeloh* discloses this limitation.

(b) *[20(a)] generating command signals to access a DDR DRAM component;*

218. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *generating command signals to access a DRAM component*. *See supra* Section III(F)(12)(b). I have also explained why *Johnson* in view of *Jeddeloh* discloses the DRAM component comprises *a DDR DRAM component*. *See supra* Section III(F)(4). Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

(c) *[20(b)] accessing DQ signals to convey DQ signals for the DDR DRAM component;*

219. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *accessing* data *signals to convey* data *for the DRAM component*. *See supra* Section III(F)(12)(c). I have also explained why *Johnson* in view of

Jeddeloh discloses the DRAM component comprises *a DDR DRAM component*. *See supra* Section III(F)(4). Additionally, for the reasons provided previously, *Johnson* in view of *Jeddeloh* discloses the data signals comprise a plurality of *DQ signals for the DDR DRAM component*. *See supra* Section III(F)(5). Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

(d) *[20(c)] accessing DQS signals to control sampling of the DQ signals; and*

220. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *accessing* sampling *signals to control sampling of the* data *signals*. *See supra* Section III(F)(12)(d). I have also explained why *Johnson* in view of *Jeddeloh* discloses the DRAM component comprises *a DDR DRAM component*. *See supra* Section III(F)(4). Additionally, for the reasons provided previously, *Johnson* in view of *Jeddeloh* discloses the sampling signals comprise a plurality of *DQS signals* for the DDR DRAM component. *See supra* Section III(F)(6). Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

(e) *[20(d)] systematically altering a phase shift of the command signals, a phase shift of the DQ signals, and a phase shift of the DQS signals to determine a valid operating range of the DDR DRAM component.*

221. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *systematically altering a phase shift of the command signals, a phase shift of the* data *signals, and a phase shift of the* sampling *signals to determine a*

valid operating range of the DRAM component. *See supra* Section III(F)(12)(e). I have also explained why *Johnson* in view of *Jeddeloh* discloses the DRAM component comprises *a DDR DRAM component*. *See supra* Section III(F)(4). Additionally, for the reasons provided previously, *Johnson* in view of *Jeddeloh* discloses the data signals comprise a plurality of *DQ signals* for the DDR DRAM component and discloses the sampling signals comprise a plurality of *DQS signals* for the DDR DRAM component. *See supra* Section III(F)(5) and *supra* Section III(F)(6). Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

21. *Claim 21*

(a) *21[P]. The computer readable media of claim 20, wherein the method further comprises:*

222. I have discussed above why *Johnson* in view of *Jeddeloh* discloses *the computer readable media of claim 20*. *See supra* Section III(F)(20). Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

(b) *[21(a)] performing a coarse calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a large step interval if the valid operating range of the DDR DRAM component exists; and*

223. For the reasons explained above, *Johnson* in view of *Jeddeloh* discloses *performing a coarse calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the*

sampling signals in accordance with a large step interval to determine if the valid operating range of the DRAM component exists. *See supra* Section III(F)(13)(b). I have also explained why *Johnson* in view of *Jeddeloh* discloses the DRAM component comprises *a DDR DRAM component*. *See supra* Section III(F)(4). Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

224. Counsel for Petitioner has asked me to assume that the term "phase shift of the data signals" in claim 21 corresponds to the term "phase shift of the DQ signals," as recited in independent claim 20. Counsel for Petitioner has also asked me to assume that the term "phase shift of the sampling signals" in claim 21 corresponds to the term "phase shift of the DQS signals," as recited in independent claim 20. *Johnson* explicitly describes DQ signals from data bus DQ. *See supra* Section III(E)(5). Additionally, a POSITA would have used DQS signals in a system with a DDR DRAM module as specified in the standard. *See supra* Section III(F)(6).

> (c) *[21(b)] if the valid operating range exists, then performing a fine calibration by altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a small step interval to identify an optimal operating mode of the DDR DRAM component.*

225. For the reasons explained above, *Johnson* in view of *Jeddeloh* discloses *if the valid operating range exists, then performing a fine calibration by*

altering the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a small step interval to identify an optimal operating mode of the DRAM component. *See supra* Section III(F)(13)(c). I have also explained why *Johnson* in view of *Jeddeloh* discloses the DRAM component comprises *a DDR DRAM component*. *See supra* Section III(F)(4). Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

226. Counsel for Petitioner has asked me to assume that the term "phase shift of the data signals" in claim 21 corresponds to the term "phase shift of the DQ signals," as recited in independent claim 20. Counsel for Petitioner has also asked me to assume that the term "phase shift of the sampling signals" in claim 21 corresponds to the term "phase shift of the DQS signals," as recited in independent claim 20. *Johnson* explicitly describes DQ signals from data bus DQ. *See supra* Section III(F)(5). Additionally, a POSITA would have used DQS signals in a system with a DDR DRAM module as specified in the standard. *See supra* Section III(F)(6).

22. *Claim 22 – The computer readable media of claim 21, wherein the method further comprises configuring the memory controller to operate the DRAM component in the optimal operating mode.*

227. I have discussed above why *Johnson* in view of *Jeddeloh* discloses *the computer readable media of claim 21*. *See supra* Section III(F)(21). Additionally, I

have explained why *Johnson* in view of *Jeddeloh* discloses *configuring the memory controller to operate the DRAM component in the optimal operating mode*. *See supra* Section III(F)(16). Thus, *Johnson* in view of *Jeddeloh* discloses this claim.

23. *Claim 23*

(a) *23[P]. In a memory controller, a method for finding an operating mode for a DDR DRAM component coupled to a PCB (printed circuit board) by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the method comprising:*

228. I have already explained how *Johnson* discloses in a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component. See *supra* Section III(F)(12)(a). Additionally, I have discussed how *Johnson* in view of *Jeddeloh* discloses wherein the DRAM component comprises a DDR DRAM component. See *supra* Section III(F)(4). By the filing of the '835 patent, arranging DRAM modules on a printed circuit board was well known in the art. For example, a "SIMM module already has a PCB with the DRAMs mounted on it." *See supra* Section III(A); Ex. 1010 at 15. Eight RAM chips are placed "on one printed circuit board (PCB) with a

common address and data bus [to] make an 8-bit RAM module." *See supra* Section III(A); Ex. 1009 at 1.

229. As I have described previously, the CPU will initiate data requests to access data from the memory modules which is facilitated by the PCB. *See supra* Section III(A). The DRAMs transmit signals via the PCB, while also receiving signals via the PCB. *Id.* A POSITA would have known that memory components, such as a DDR DRAM component, could be and frequently were implemented on a PCB. PCBs were often used for the interface of DRAM systems prior to the rise of integrated circuits. *See supra* Section III(A). In the early 2000s, during the time of the '835 Patent, a POSITA would have been aware of the practice of using PCBs for memory systems. Therefore, *Johnson* discloses this limitation.

(b) *[23(a)] generating command signals to access a DDR DRAM component;*

230. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *generating command signals to access a DDR DRAM component*. *See supra* Section III(F)(20)(b). Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

(c) *[23(b)] accessing data signals to convey data for the DDR DRAM component;*

231. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *accessing data signals to convey data for the DDR DRAM component*.

See supra Section III(F)(20)(c). Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

(d) *[23(c)] accessing sampling signals to control sampling of the data signals; and*

232. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *accessing sampling signals to control sampling of the data signals*. *See supra* Section III(F)(20)(d) Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

(e) *[23(d)] systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals transmitted via a PCB to determine a valid operating range of the DDR DRAM component.*

233. I have previously explained why *Johnson* in view of *Jeddeloh* discloses *systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operating range of the DDR DRAM component*. *See supra* Section III(F)(20)(e) I have also explained that the respective signals would be transmitted via a PCB. *See supra* Section III(F)(23)(a). Therefore, *Johnson* in view of *Jeddeloh* discloses this limitation.

G. Ground 2: Claims 1-3, 7-8, and 12 are Obvious Over *Johnson* in View of *Keeth.*

234. As discussed previously in Section III(F), *Johnson* (Ex. 1004) and *Jeddeloh* (Ex. 1005) together disclose or suggest each and every element of Claims 1-23. Additionally, *Johnson* and *Keeth* (Ex. 1006) disclose or suggest each and every element of Claims 1-3, 7-8, and 12.

1. *Claim 1*

(a) *1[P]. A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the method comprising:*

235. To the extent the preamble is considered limiting, I have previously explained how *Johnson* discloses the preamble. *See supra* Section III(F)(1)(a). Therefore, *Johnson* discloses this element.

(b) *[1(a)] generating command signals to access an integrated circuit component;*

236. I have previously explained how *Johnson* discloses *generating command signals to access an integrated circuit component*. *See supra* Section III(F)(1)(b). Therefore, *Johnson* discloses this element.

(c) *[1(b)] accessing data signals to convey data for the integrated circuit component;*

237. I have previously explained how *Johnson* discloses *accessing data signals to convey data for the integrated circuit component*. *See supra* Section III(F)(1)(c). Therefore, *Johnson* discloses this element.

(d) *[1(c)] accessing sampling signals to control sampling of the data signals; and*

238. I have previously explained how *Johnson* discloses *accessing sampling signals to control sampling of the data signals*. *See supra* Section III(F)(1)(d). Therefore, *Johnson* discloses this element.

(e) *[1(d)(i)] systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device,*

239. As explained previously for Claim 1(d)(i) in Section III(F)(1), *Johnson* teaches this element. To the extent *Johnson* does not explicitly disclose *systematically altering a phase shift of … the sampling signals*, *Keeth* teaches this element.

240. *Keeth* discloses memory systems including DRAM in which clock adjustments are employed for accurate clocking of command data, write data, and read data. Ex. 1006, 1:11-17; 1:39-45. *Keeth* states in particular that the clock adjustments "compensate[] for such effects as duty cycle variation, bus position of a given memory device, timing drift, loading variations, clock jitter, clock skew, noise, overshoot, and ringing so that data can be accurately clocked in the memory devices." *Id.* at 1:51-59.

241. *Keeth* describes a memory system similar to that of *Johnson*, having a memory controller 22 and DRAM modules. *Id.* at 3:39-41. The DRAM modules

are identified with reference numerals 24 and 26 in *Keeth's* Figure 1, which is a simplified representation of the memory system. The system of *Keeth* includes a command bus 28, which "is an unidirectional bus for carrying address and control information from memory controller 22 to the DRAM modules." *Id.* at 3:43-55. The system of *Keeth* further includes a data bus 32 for carrying *data signals* between DRAM modules. *Keeth* states in particular that data bus 32 is "a bidirectional bus carrying write data from memory controller 22 to the DRAM modules and further carrying read data from the DRAM modules to memory controller 22." *Id.* at 3:51-54. A "free-running clock (CCLK) [is] provided on a clock line 30 from memory controller 22" and "[t]wo bidirectional data clocks, DCLK0 and DCLK1, are respectively provided on clock line 34 and clock line 36." CCLK, DCLK0, and DCLK1 are all used to control sampling of *data signals* on data bus 32, as I will discuss in further detail hereinafter, and are therefore *sampling signals*. *Id.* at 3:50-56. I have reproduced Figure 1 of *Keeth* below, with annotations showing the path of the *data signals* green and the paths of the *sampling signals* in blue.

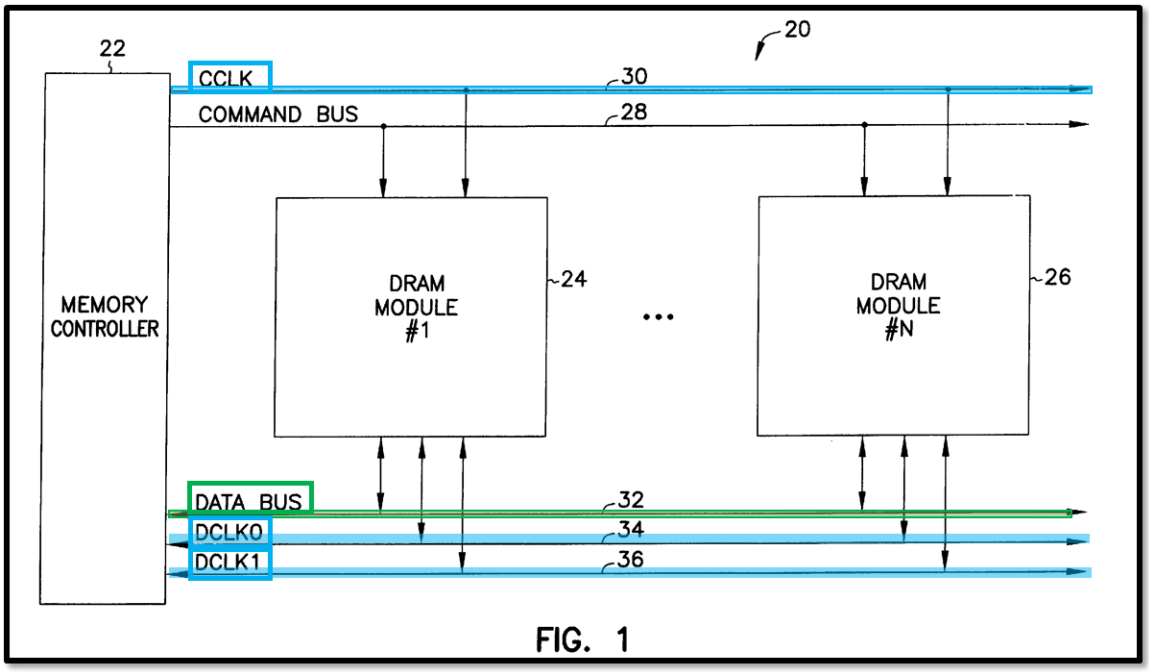


FIG. 1

Reproduced from *Keeth* (Annotated)

Id. at 4, annotated.

242. *Keeth* explains that vernier clock adjustment circuitry is used in the memory system to control timing of signals within the system and ensure that data is accurately clocked. *Id.* at 2:46-55; 4:11-18. *Keeth* states that when the memory system is "powered up, the command timing, read timing, and write timing of each individual DRAM is adjusted by the memory controller 22[] so that bursts of data on the data bus originating from different devices are properly spaced." *Id.* at 7:24-28. *Keeth* further states that "each DRAM includes a variety of vernier adjustment circuits which compensate" for variability in signal timing "to permit read data from all DRAMs to arrive at memory controller 22 within fixed, deterministic

timing, and similarly permit write data to arrive with fixed, deterministic timing to the selected DRAM devices." *Id.* at 7:41-46. *Keeth* shows vernier clock adjustment circuitry within the memory system in block diagram form in Figure 7. *Id.* at 6:55-58. I have reproduced Figure 7 of *Keeth* below, with annotations showing the relevant vernier delays of the memory system in purple.

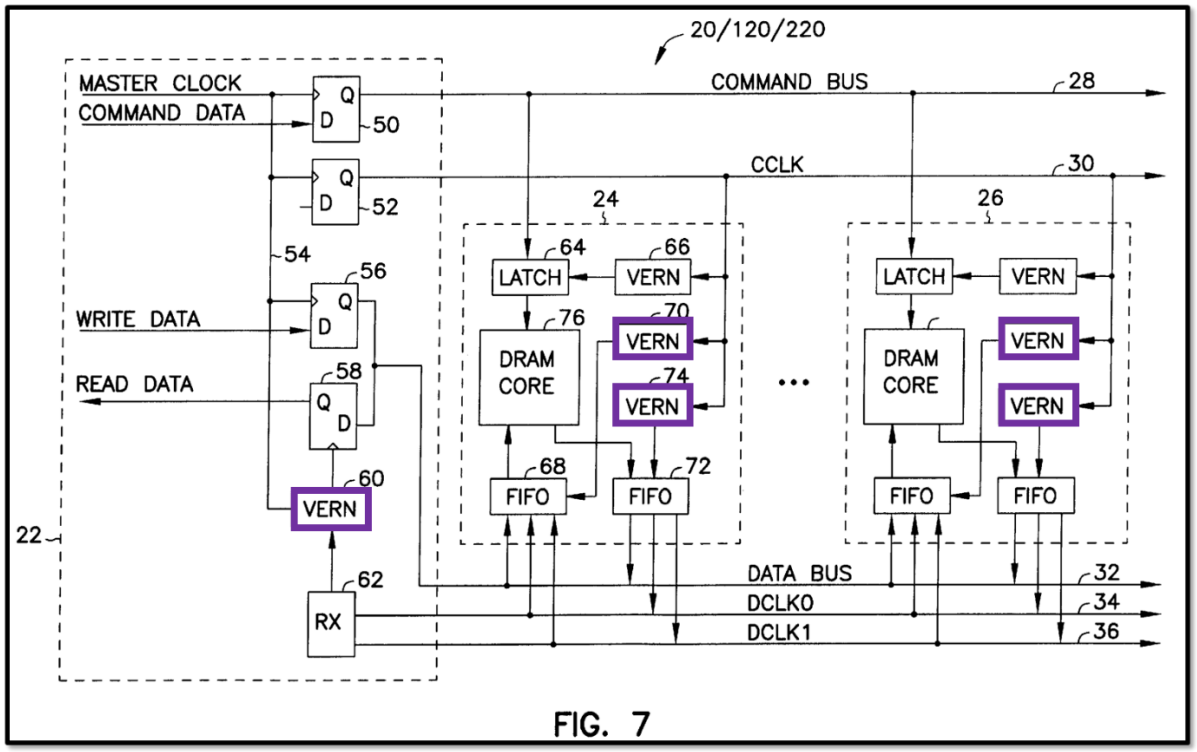


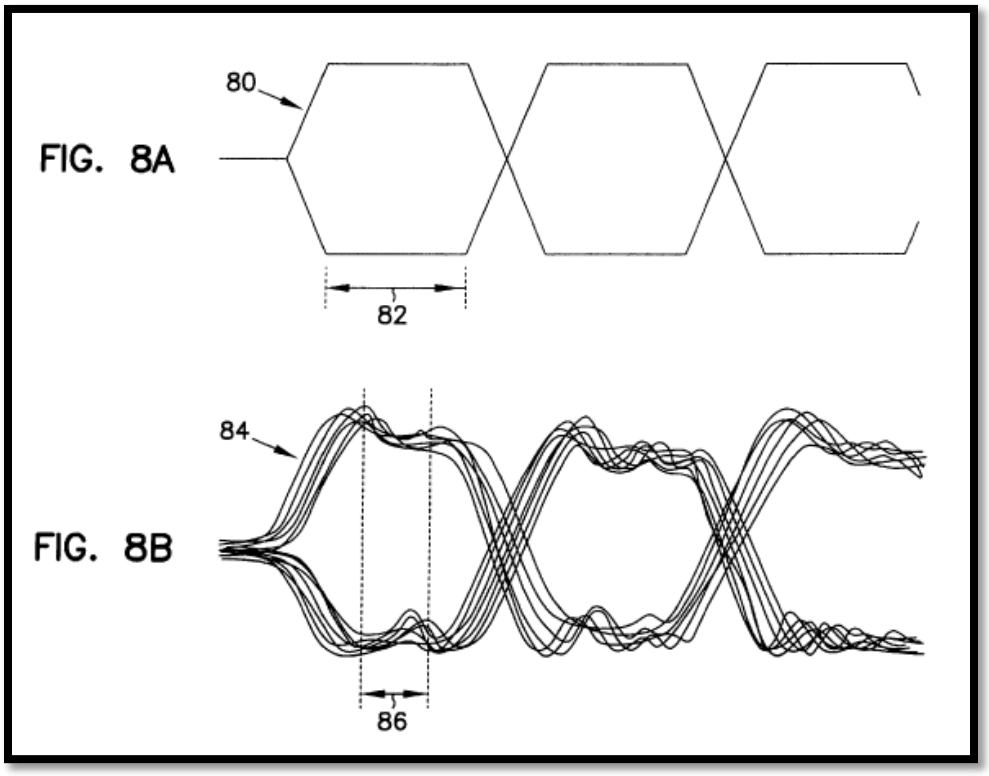
FIG. 7

Reproduced from *Keeth* (Annotated)

Id. at 10, annotated.

243. As shown in Figure 7, the memory system includes vernier clock adjustment circuit 60 within memory controller 22, vernier clock adjustment circuits 70 and 74 within DRAM module 24, and similar vernier clock adjustment

circuits within DRAM module 26. Each of the vernier clock adjustment circuits 60, 70, and 74 includes circuitry for adjusting the timing of rising edges and falling edges of corresponding clock signals. *Id.* at 9:61-67; 10:37-42. With reference to Figures 8A and 8B, *Keeth* explains that adjustments to the rising edges and falling edges of clocks are used to compensate for a reduction of a valid data window. *Id.* at 9:51-57. Figures 8A and 8B are reproduced below.



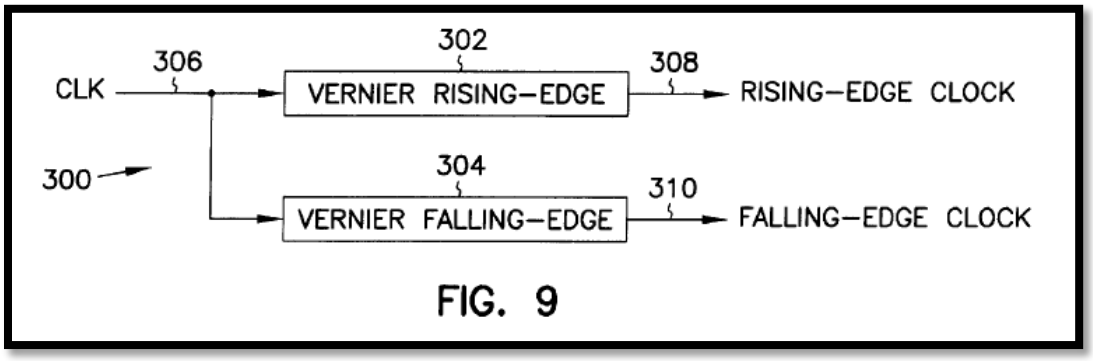
Reproduced from *Keeth* (Annotated)

Id. at 11, annotated.

244. *Keeth's* Figure 8A shows an "ideal" signal waveform 80 representing a data signal. *Id.* at 9:51-53. The ideal signal waveform in Figure 8A has a "big eye

pattern" with valid data within the period defined by arrows 82. *Id.* at 9:52-54. Figure 8B, on the other hand, shows a "non-ideal" waveform 84 representing a data signal "produced as a result of jitter, skew, noise, overshoot, ringing and other such known problems." *Id.* at 9:55-60. The non-ideal waveform has a "significantly reduced valid data period indicated by arrows 86. *Id.* at 9:55-58. *Keeth*'s vernier adjustment circuitry adjusts timings of clocks' rising edges and falling edges to ensure accurate sampling of data signals within valid data periods. *Id.* at 9:61-67. By adjusting the timing of rising and falling edges relative to data signals, *Keeth*'s system *alter[s] a phase shift of … the sampling signals*.

245. *Keeth* teaches that the vernier clock adjustment circuits 60, 70, and 74 are configured to implement the rising edge adjustments and falling edge adjustments. *Id.* at 10:37-45. Figure 9 depicts the circuitry used for such adjustments in block diagram form. *Id.* at 10:2-5. As shown in Figure 9, a clock signal is provided to parallel vernier adjustment circuits 302 and 304. Each of the circuits 302 and 304 independently delays the CLK signal such that each of circuit 302 and 304 produces a delayed version of the CLK signal. *Id.* at 10:1-17. The clock signal produced by circuit 302 is used for rising edge clockings, whereas the clock signal produced by circuit 304 is used for falling edge clockings. *Id.* at 10:6-17. Figure 9 is reproduced below.



Reproduced from *Keeth*

Id. at 12.

246. *Keeth* explains that the memory system adjusts the delays of the vernier clock adjustment circuits in either of two ways. One way the memory system performs the adjustments is by "run[ning] through all delay steps of the vernier circuit and determin[ing] when data misses on low adjustments and on high adjustments." *Id.* at 7:66-8:5. The system then "sets the vernier adjustment in an approximated optimal middle setting." *Id.* Alternatively, *Keeth* states that the memory system "includes a feedback controller used to set the vernier settings by first selecting an estimated optimal setting and allowing the controller and feedback circuitry to arrive at the optimal delay setting for the vernier clock adjustment circuit." *Id.* at 8:5-9. In either manner of adjusting delays for the vernier clock adjustment circuits, the memory system performs the adjustment methodically according to a defined procedure or plan. Adjustment of the delays in *Keeth*'s memory system therefore amounts to *systematically altering*. Ex. 1020 at

1230 (*Merriam-Webster's Dictionary*, defining "systematic" as "methodical in procedure or plan").

247. Turning back to the memory system shown in Figure 7, Vernier clock adjustment circuit 60 is used to adjust the timing of DCLK0 or DCLK1 for a read operation. *Keeth* explains that "clocks DCLK0 and DCLK1 are used to precisely transfer read data timing from the DRAM modules to the memory controller 22." Ex. 1006 at 3:57-61. Memory controller 22 selects one of DCLK0 or DCLK1 for a given read or write operation, and deactivates the other. *Id.* at 4:1-10. *Keeth* teaches that the "rising edge and falling edge transitions of the selected DCLK are employed to clock the input latches of the DRAM modules and memory controller receiving data." *Id.* at 3:61-63. During a read operation, *i.e.* when data is received from a DRAM module by memory controller 22, "one of DCLK0 or DCLK1 clocks is selected in vernier clock adjustment circuit 60 to latch the read data in read data register 58." *Id.* at 8:66-9:2. In other words, an active one of DCLK0 or DCLK1 controls sampling of data transmitted on data bus 32 to memory controller 22 during a read operation. DCLK0 or DCLK1 are therefore ***sampling signals***.

248. As explained previously, vernier clock adjustment circuit 60 is configured as shown in Figure 9 to produce a delayed version of the active DCLK used for rising edge clockings and a delayed version of the active DCLK used for falling edge clockings. *Id.* at 12. These delayed versions of the active DCLK are

used to ensure that read data transmitted on data bus 32 to memory controller 22 is latched during valid data periods. Delaying the active DCLK signals is *systematically altering a phase shift of … the sampling signals*. I have reproduced Figure 7 below again with annotations, in this instance to highlight in purple the vernier clock adjustment circuit 60, which is responsible for *systematically altering a phase shift of … the sampling signals* (DCLK signals), which are highlighted in blue.

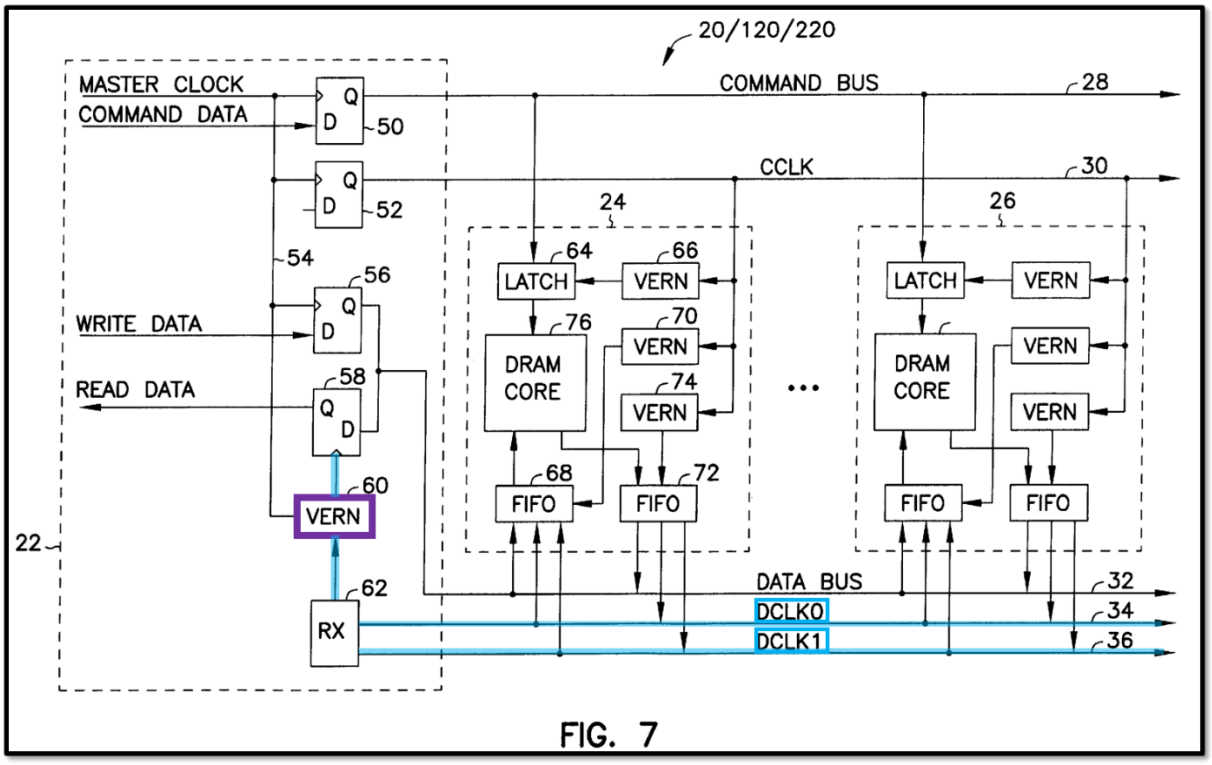


FIG. 7

Reproduced from *Keeth* (Annotated)

Id. at 10, annotated.

249. Additionally, vernier clock adjustment circuits 70 and 74 are used in write and read operations, respectively, to adjust the timing of CCLK, which controls sampling of data signals at DRAM module 24. *Keeth* states that a "write first-in, first-out (FIFO) buffer 68 receives the DCLK0 and DCLK1 clock signals from lines 34 and 36 and the write data from data bus 32 and provides write data to a DRAM core 76." *Id.* at 7:9-12. The write FIFO buffer 68 "receives a delayed CCLK clock from a write vernier clock adjustment circuit 70," which is used to clock write FIFO buffer 68. *Id.* at 7:12-14; 9:15-18. The write FIFO buffer 68 is used to compensate for differences between a speed data transmission on data bus 32 and speed of writing to DRAM core 76. Ex. 1019 at 95 (*Dictionary of Electronics*, defining "buffer" as "9. high-speed area of storage in a computer that is temporarily reserved for use in performing the input/output operation, into which data is read or from which data is written. 10. A storage area in a computer for data that is used to compensate for a speed difference when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written."). During write operations, write FIFO buffer 68 samples data signals from data bus 32 before the data is written to DRAM core 76. Ex. 1006 at 7:10-12. Because write FIFO buffer 68 is clocked by the delayed CCLK provided by write vernier clock adjustment circuit 70, CCLK

controls, at least in part, sampling of the data signals written to DRAM core 76. *Id*. at 7:12-14. CCLK is therefore a ***sampling signal***.

250. Similarly, a "read FIFO buffer 72 receives read data from DRAM core 76 and provides the read data to data bus 32 along with the DCLK0 and DCLK1 clock signals to clock lines 34 and 36." *Id.* at 7:15-18. The read FIFO buffer 72 "receives a delayed CCLK clock from a read vernier clock adjustment circuit 74," which is used to clock read FIFO buffer 72. *Id.* at 7:20-22; 9:15-18. The read FIFO buffer 72 is used to compensate for differences between a speed data transmission on data bus 32 and speed of reading from DRAM core 76. Ex. 1019 at 95 (*Dictionary of Electronics*, defining "buffer" as "9. high-speed area of storage in a computer that is temporarily reserved for use in performing the input/output operation, into which data is read or from which data is written. 10. A storage area in a computer for data that is used to compensate for a speed difference when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written."). During read operations, read FIFO buffer 72 samples data signals read from DRAM core 76 before transmitting the data on data bus 32. Ex. 1006 at 7:15-17. Because read FIFO buffer 72 is clocked by the delayed CCLK provided by read vernier clock adjustment circuit 74, CCLK controls, at least in part, sampling of the data signals

read from DRAM core 76. *Id.* at 7:17-20. The CCLK signals are therefore *sampling signals*.

251. As explained previously, vernier clock adjustment circuits 70 and 74 are configured as shown in Figure 9 to produce a delayed versions of CCLK used to clock write FIFO buffer 68 and read FIFO buffer 72. *Id.* at 12. The delayed versions of CCLK are used to ensure proper timing of write FIFO buffer 68 and read FIFO buffer 72. Delaying the CCLK signals is therefore *systematically altering a phase shift of … the sampling signals*. I have reproduced Figure 7 below again with annotations, in this instance to highlight in purple the vernier clock adjustment circuits 70 and 74, which are responsible for *systematically altering a phase shift of … the sampling signals* (CCLK signals), which are highlighted in blue.

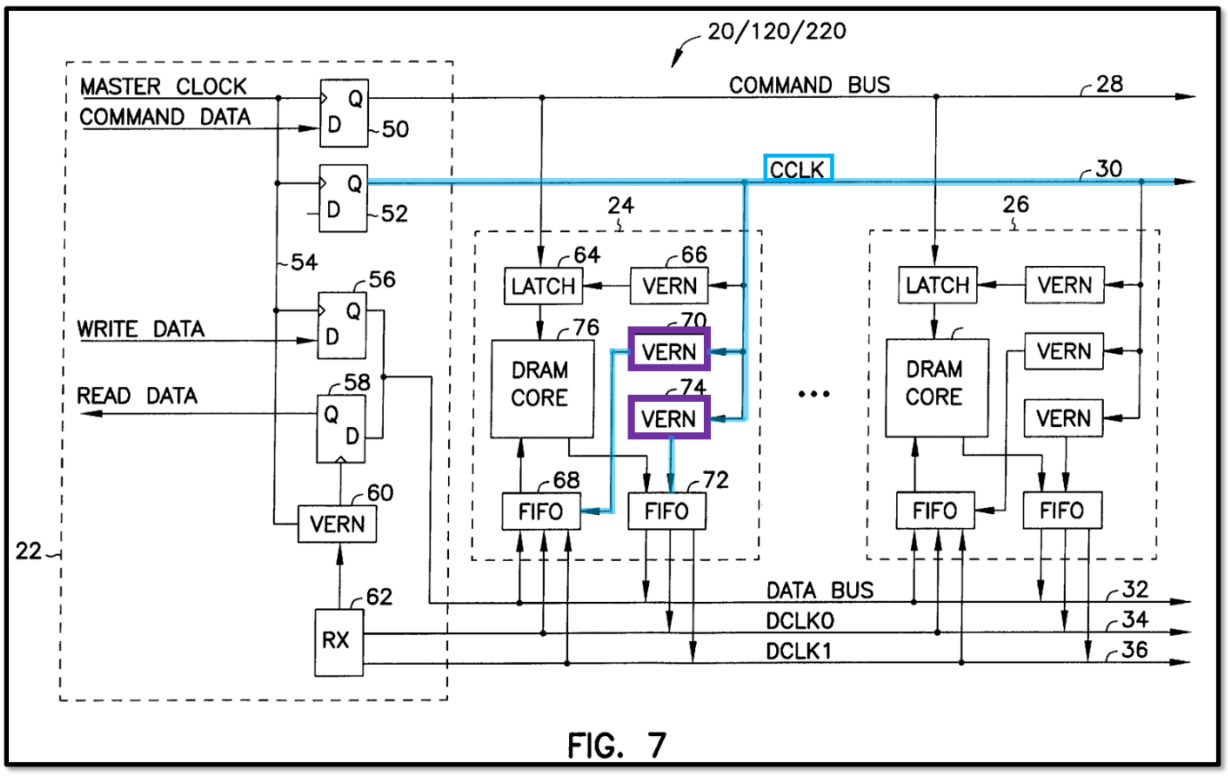


FIG. 7

Reproduced from *Keeth* (Annotated)

Id. at 10, annotated.

252. A POSITA would have been motivated to modify the system of *Johnson* according to the teachings of *Keeth* at least to ensure proper synchronization of data signals and sampling signals when received at the memory controller from the SLDRAM modules. As an initial matter, both *Johnson* and *Keeth* relate to high-speed computer memory devices. Ex. 1004 at 1:5-25, Ex. 1006 at 1:40-50. *Johnson* and *Keeth* are therefore in the same field of endeavor. Additionally, both references list Micron Technology, Inc. as assignee on their face, and both references name Brent Keeth as an inventor. Ex. 1004; Ex. 1006.

253. As explained previously, *Johnson* teaches that data signals transmitted via data bus DQ0-17 are phase shifted for alignment with DCLK. *See supra* Section III(F)(1). *Johnson* shows in FIG. 4 that the DCLK signals latch the data signals on DQ0-17 when writing to DRAM banks. *Id. Johnson*, however, is concerned primarily with synchronization of sampling signals and data signals within SLDRAM modules and is silent as to synchronization of such signals within the memory controller. *Id.* Upon transmission from memory modules to the memory controller, data signals and sampling signals may fall out of sync due to jitter, skew, noise, or the like. A POSITA would have had reason to look to the teachings of *Keeth* to address this issue and would have been motivated to incorporate at least vernier delay adjustment circuit 60 within the memory controller of *Johnson* to ensure that sampling signals and data signal received at the memory controller are appropriately synchronized. Moreover, incorporating vernier clock adjustment circuit 60 of *Keeth* within the memory controller of *Johnson* would allow greater flexibility for synchronizing sampling signals and data signals and allow for greater accuracy in the alignment.

254. Additionally, as explained previously, when reading from the DRAM banks, *Johnson* shows in FIG. 4 that CCLK latches data signals on DQ0-17. *Id. Johnson* shows that CCLK passes through a delay lock loop 41, but does not explicitly explain how CCLK is synchronized to the data signals received from the

DRAM banks. *Id.* A POSITA therefore would have had reason to look to *Keeth* for specificity as to how to synchronize data signals and sampling signals, at least as the data signals and samplings are being transmitted from the SLDRAM modules to the memory controller. Following the teachings of *Keeth*, a POSITA would have understood that incorporating one or more vernier clock adjustment circuits in the SLDRAM modules to systematically alter the phase shift of the sampling signals (CCLK) of *Johnson* would be beneficial. This would ensure alignment of the sampling signals with read data signals at the SLDRAM modules, thereby increasing a likelihood of alignment of the sampling signals and data signals when received for reading by the memory controller.

255. Further, a POSITA would have understood that incorporating *Keeth*'s vernier clock adjustment circuit 70 within *Johnson*'s SLDRAM modules to adjust timing of sampling signals during write operations would likewise be beneficial. While *Johnson* describes altering a phase shift of data signals DQ0-17, adding circuitry to further alter a phase shift of sampling signal DCLK when writing to the SLDRAM modules would introduce an additional degree of adjustment, thereby improving the alignment of data signals and sampling signals at the SLDRAM modules during write operations. Improving the alignment would in turn improve the reliability and proper functioning of the memory system.

256. The foregoing modifications of *Johnson* according to the teachings of *Keeth* would have been well within the skill of a POSITA, as evidenced at least by Brent Keeth being listed as a common inventor on both references. Combining *Johnson* with *Keeth* would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. The modified system would indeed result in a functional high-speed computer memory capable of reading and writing data to and from DRAM storage.

(f) *[1(d)(ii)] wherein the valid operation range includes an optimal operation point for the integrated circuit device.*

257. I have previously explained how *Johnson* discloses that *the valid operation range includes an optimal operation point for the integrated circuit device*. *See supra* Section III(F)(1)(f). Therefore, *Johnson* discloses this element.

2. *Claim 2 – The method of claim 1, wherein the integrated circuit device comprises a DRAM component.*

258. For the reasons I have discussed previously, *Johnson* in view of *Keeth* discloses *the method of claim 1*. Also, for the reasons discussed previously for Ground 1, *Johnson* teaches the additional element(s) of Claim 2. *See supra* Section III(F)(2). *Johnson* and *Keeth* therefore collectively teach all elements of Claim 2.

3. *Claim 3 – The method of claim 2, wherein said altering is performed by a memory controller coupled to the DRAM component.*

259. As discussed previously in Section III(F)(3), *Johnson*'s memory system includes a memory controller configured to access and control SLDRAM modules. Ex. 1004 at 3:31-33. *Johnson* teaches that conventional memory controllers would be configured to perform timing calibration for signals sent to SLDRAM modules. *Id.* at 1:42-54.

260. Each of the SLDRAM modules 11a . . . 11n of *Johnson*'s memory system includes a control logic 21. *Id.* at 3:48-50. *Johnson* explains that control logic 21 "steps through all possible delay positions of ring delays 27 and 29" and "establishes an 'eye' or 'window' of acceptable delays for each of the ring delays 27 for the command data paths CA0-9 and for ring delay 29 for the FLAG input path." *Id.* at 4:36-4:44. *Johnson* further teaches that control logic 21 of the SLDRAM modules calibrates ring delays for each of the data paths on the DQ0-17 bus. *Id.* at 7:25-7:61. *Johnson*'s memory system therefore includes as many control logics as SLDRAM modules to calibrate the various ring delays.

261. *Keeth* teaches that memory controller 22 performs altering of the vernier delay adjustment circuits in the memory controller and in the DRAM modules. In particular, *Keeth* states that "adjustments to vernier clock adjustment circuit 66, 70, 74 in each DRAM device is made by writing a delay value in a register located in each DRAM device." Ex. 1006 at 7:47-50. For example, *Keeth* explains that memory controller 22 "writes the vernier delay control register of

read vernier clock adjustment circuit 74 or otherwise sets the delay of the read vernier clock adjustment circuit to increase the delay until read delay data can be optimally sampled." *Id.* at 8:49-55. *Keeth* further states that "[m]emory controller 22 correspondingly adjusts the read vernier clock adjustment circuits of each of the DRAM modules through the Nth DRAM module 26." *Id.* at 8:56-58. *Keeth*'s memory controller also adjusts vernier clock adjustment circuit 60 within the memory controller. 8:40-42.

262. *Keeth* therefore discloses a memory system in which delay adjustments, *i.e.*, alterations of signal phases, are performed by memory controller 22. Memory controller 22 of *Keeth* is responsible for setting delays of vernier clock adjustment circuits both within the memory controller 22 itself and within DRAM modules.

263. As explained previously in Section III(G)(1), applying the teachings of *Keeth* to the memory system of *Johnson* would have been well within the ability and understanding of a POSITA since it would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. Moreover, a POSITA would have been motivated to modify the memory system of *Johnson* such that *Johnson*'s memory controller would set the ring delays in each of the SLDRAM modules just as *Keeth*'s memory controller sets the vernier clock adjustment circuits within

DRAM modules. Such a configuration would obviate a need to include control logic circuits within each of *Johnson*'s SLDRAM modules and would consolidate the functionality of the multiple control logic circuits within *Johnson*'s memory controller. A POSITA would have recognized that the cost and complexity of each of *Johnson*'s SLDRAM modules would therefore be reduced, in turn reducing the cost and complexity of *Johnson*'s overall memory system.

7. <u>*Claim 7*</u>

(a) *7[P]. A system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the system comprising:*

264. For the reasons that I have discussed previously, *Johnson* discloses this element. *See supra* Section III(F)(1)(a); Section III(F)(7)(a).

(b) *[7(a)] a controller configured to generate command signals for accessing an integrated circuit component;*

265. For the reasons that I have discussed previously, *Johnson* discloses this element. *See supra* Section III(F)(1)(b); Section III(F)(7)(b).

(c) *[7(b)(i)] a delay calibrator integrated within the controller and*

266. As discussed previously for Claim 3 in Section III(G)(3), *Keeth* discloses a memory system in which a memory controller 22 alters delays of vernier delay adjustment circuits within DRAM modules. *Keeth* explains that altering the delays is performed as part of an "initialization" procedure to identify

"optimal" delay settings. *See* Ex. 1006 at 7:66-8:60. *Keeth* adjusts the various vernier delay adjustment circuits to "optimal" delay settings to enable "alignments of clocks, commands, write data bursts, and read data bursts," for accurate sampling of command signals, read data signals, and write data signals." *Id.* at 8:10-32. *Keeth*'s memory controller 22 therefore calibrates the delays. Ex. 1020 at 197 (*Merriam-Webster's Dictionary*, defining "calibrate" as "to adjust precisely for a particular function"). As *Keeth*'s memory controller 22 calibrates delays of the vernier delay adjustment circuits in the memory system, the memory controller 22 thus includes a *delay calibrator integrated within the controller*.

267. As also explained previously for Claim 3 in Section III(G)(3), a POSITA would have been able and motivated to modify the memory system of *Johnson* such that *Johnson*'s memory controller would set the ring delays in each of the SLDRAM modules just as *Keeth*'s memory controller sets the vernier clock adjustment circuits within DRAM modules. In other words, a POSITA would have been able and motivated to modify the memory controller of *Johnson* according to the teachings of *Keeth* to include *a delay calibrator integrated within the controller* as it would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. For these reasons, *Johnson* in view of *Keeth* discloses this element.

(d) *[7(b)(ii)] configured to access data signals conveying data for the integrated circuit device and*

268. For the reasons that I have discussed previously, *Johnson*'s memory controller is *configured to access data signals conveying data for the integrated circuit device*. *See supra* Section III(F)(1)(c). For example, *Johnson* specifies that a "a bi-directional data bus DQO-17 is provided between memory controller 13 and each of the SLDRAM modules 11a . . . 11n." Ex. 1004 at 3:40-44. *Johnson* further explains that "[d]ata which is to be input to memory banks 69, 71 is supplied by memory controller 13 (FIG. 3) on the DQ data bus." *Id.* at 4:12-16. To receive and transmit data on the DQ data bus, *Johnson's* memory controller 13 is *configured to access data signals*. The *delay calibrator integrated within Johnson*'s memory controller according to the teachings of *Keeth*, is a functional element of the memory controller. Therefore, the *delay calibrator integrated within Johnson*'s memory controller is *configured to access data signals conveying data for the integrated circuit device* for the same reasons that *Johnson*'s memory controller as a whole is. A POSITA would have understood incorporating the teachings of *Keeth* with *Johnson* would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. For these reasons, *Johnson* in view of *Keeth* discloses this element.

(e) *[7(b)(iii)] to access sampling signals for controlling sampling of the data signals,*

269. For the reasons that I have discussed previously, *Johnson*'s memory controller is *configured . . . to access sampling signals for controlling sampling of the data signals*. *See supra* Section III(F)(1)(d). For example, *Johnson* specifies that "[m]emory controller 13 provides a command link to each of the SLDRAM modules 11a … 11n which includes a clock signal CCLK." *Id.* at 3:33-36. Also, "bi-directional data clocks DCLK0 and DCLK1" are provided between the memory controller 13 and the SLDRAM modules 11a-11n, which are used "to strobe input/output data into and out of the SLDRAM modules." *Id.* at 3:44-47. To receive and transmit CCLK, DCLK0, and DCLK1, *Johnson's* memory controller 13 is *configured to access sampling signals*. The *delay calibrator integrated within Johnson*'s memory controller according to the teachings of *Keeth*, is a functional element of the memory controller. Therefore, the *delay calibrator integrated within Johnson*'s memory controller is *configured to access sampling signals for controlling sampling of the data signals* for the same reasons that *Johnson*'s memory controller as a whole is. A POSITA would have understood incorporating the teachings of *Keeth* with *Johnson* would have been nothing more than combining prior art elements according to known methods to yield predictable

results with a reasonable expectation of success. For these reasons, *Johnson* in view of *Keeth* discloses this element.

> (f) *[7(c)(i)] wherein the delay calibrator is further configured to systematically alter a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device; and*

270. For the reasons I have described previously, *Johnson* in view of *Keeth* teaches *systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device*. *See supra* Section III(F)(1)(e); Section III(G)(1)(e).

271. As also explained previously, a POSITA would have been able and motivated to modify the memory system of *Johnson* such that *Johnson*'s memory controller would set the ring delays in each of the SLDRAM modules just as *Keeth*'s memory controller sets the vernier clock adjustment circuits within DRAM modules since such a combination would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. *See supra* Section III(G)(3). By modifying *Johnson*'s memory controller to set the ring delays in each of the SLDRAM modules, *Johnson*'s memory controller would *systemically alter* the recited phase shifts. It follows that *Johnson's* memory controller is *configured to systemically*

alter the recited phase shifts. As the *delay calibrator integrated within Johnson*'s memory controller according to the teachings of *Keeth*, is a functional element of the memory controller, the *delay calibrator* is *configured to systemically alter* the recited phase shifts for the same reasons that *Johnson*'s memory controller as a whole is. For these reasons, *Johnson* in view of *Keeth* discloses this element.

(g) *[7(c)(ii)] wherein the valid operation range includes an optimal operation point for the integrated circuit device.*

272. For the reasons provided previously, *Johnson* discloses *wherein the valid operation range includes an optimal operation point for the integrated circuit device*. *See supra* Section III(F)(1)(f).

8. *Claim 8 – The system of claim 7, wherein the integrated circuit device comprises a DRAM component.*

273. For the reasons that I have discussed previously, *Johnson* in view of *Keeth* discloses *the method of claim 7*. *See supra* Section III(G)(7). Also, for the reasons discussed previously for Ground 1, *Johnson* teaches the additional element(s) of Claim 2. *See supra* Section III(F)(2). *Johnson* and *Keeth* therefore collectively teach all elements of Claim 8.

12. *Claim 12*

(a) *12[P]. In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, the method comprising:*

274. I have previously explained how *Johnson* in view of *Keeth* discloses *a method for* automatically calibrating *intra-cycle timing relationships between command signals, data signals, and sampling signals for* an integrated circuit device. *See supra* Section III(G)(1)(a). I have also explained how *Johnson* discloses *a DRAM component*. *See supra* Section III(F)(2). Specifically, *Johnson* discloses systematically altering timing relationships between the signals *for the DRAM component*. *Id.* Further, I have explained how *Johnson* in view of *Keeth* discloses a delay calibrator integrated within *a memory controller* that is configured to perform the altering. *See supra* Section III(G)(7)(f). For these reasons, *Johnson* in view of *Keeth* discloses this element.

(b) *[12(a)] generating command signals to access a DRAM component;*

275. I have previously explained how *Johnson* discloses *generating command signals to access an integrated circuit component* such as an SLDRAM component. *See supra* Section III(F)(1)(b). I have also explained how the SLDRAM component is *a DRAM component*. *See supra* Section III(F)2. Therefore, *Johnson* discloses this element.

(c) *[12(b)] accessing data signals to convey data for the DRAM component;*

276. I have previously explained how *Johnson* discloses *accessing data signals to convey data for the integrated circuit component* such as an SLDRAM

component. *See supra* Section III(F)(1)(c). I have also explained how the SLDRAM component is *a DRAM component*. *See supra* Section III(F)2. Therefore, *Johnson* discloses this element.

(d) *[12(c)] accessing sampling signals to control sampling of the data signals; and*

277. I have previously explained how *Johnson* discloses *accessing sampling signals to control sampling of the data signals*. *See supra* Section III(F)(1)(d). Therefore, *Johnson* discloses this element.

(e) *[12(d)] systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operating range of the DRAM component.*

278. I have previously explained how *Johnson* in view of *Keeth* discloses *systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operating range of the integrated circuit device*, such as an SLDRAM component. *See supra* Section III(F)(1)(e); Section III(G)(1)(e). I have also explained how the SLDRAM component is *a DRAM component*. *See supra* Section III(F)(2). For these reasons, *Johnson* in view of *Keeth* discloses this element.

H. Ground 3: Claims 4-6, 9-11, 13-19 are Obvious Over *Johnson* in View of *Keeth* and *Jeddeloh*

279. I have previously explained that *Johnson* in view of *Keeth* teaches all elements of independent Claims 1, 7, and 12 and that a POSITA would have been

capable of and motivated to modify *Johnson* according to the teachings of *Keeth*. *See supra* Section III(G)(1); Section III(G)(7); Section III(G)(12). I have also previously explained that *Johnson* in view of *Jeddeloh* teaches all elements of dependent Claims 4-6, 9-11, and 13-19, and that a POSITA would have been capable of and motivated to modify *Johnson* according to the teachings of *Keeth*. *See supra* Section III(F)(4-6); Section III(F)(9-11); Section III(F)(13-19).

280. Claims 4-6 depend from Claim 1, Claims 9-11 depend from Claim 7, and Claims 13-19 depend from Claim 12. Ex. 1001 at 7:8-8:27. *Johnson* in view of *Keeth* and *Jeddeloh* teaches all elements of Claims 4-6, 9-11, and 13-19 for at least the reasons set for in Sections III(E) and III(F).

281. Modifying *Johnson* as I have explained according to the teachings of *Keeth* and *Jeddeloh* would result in a high-speed memory system that functions as a POSITA would have expected. A POSITA would have recognized the benefits of modifying *Johnson*'s memory system according to the teachings of both *Keeth and Jeddeloh*. A POSITA would have understood incorporating the teachings of *Keeth* and *Jeddeloh* with *Johnson* would have been nothing more than combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. For these reasons, *Johnson* in view of *Keeth* and *Jeddeloh* discloses all of the elements of Claims 4-6, 9-11, and 13-19.

IV. CONCLUSION

282. In summary, it is my opinion that the references discussed in this Declaration disclose or suggest all of the features recited in Claims 1-23 of the '835 Patent.

283. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: Aug. 2, 2024 By: R. Jacob Baker, P.E., Ph.D.

Appendix A

R. JACOB BAKER, PH.D., P.E.

professor emeritus of electrical and computer engineering

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PROFESSIONAL SUMMARY

Russel Jacob Baker (R. Jacob Baker), Ph.D., P.E. (IEEE Student Member 1983, Member 1988, Senior Member 1997, and Fellow 2013) was born in Ogden, Utah, on October 5, 1964. He received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas (UNLV) in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno (UNR) in 1993. His Google Scholar profile is here and his ResearchGate profile is here.

From 1981-1987 he served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division). From 1985-1993 he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada Test Site. During this time he designed, and oversaw the fabrication and the electrical/mechanical manufacture of, over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs for high-speed imaging, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1991-1993 he was an adjunct faculty member in the Departments of Electrical Engineering at UNLV and UNR. From 1993-2000 he served on the faculty in the Department of Electrical Engineering at the University of Idaho (UI), first as an untenured assistant professor and then from 1998 as a tenured associate professor. In 2000 he joined a new electrical and computer engineering (ECE) program at Boise State University (BSU) where he was promoted to professor in 2002. He then served as the ECE department chair from 2004-2007. At BSU he helped establish graduate programs in ECE including, in 2006, the university's second PhD degree. In 2012 he rejoined the faculty at UNLV as a tenured full professor of ECE. During his tenure at the UI, BSU, and UNLV he has been the major professor to more than 100 graduate students.

Dr. Baker has done consulting for over 200 companies. His research/development activities are in: photonics, circuit design for wireless and wired communications, analog-to-digital/digital-to-analog data conversion and transmission, optoelectronics (imagers, displays, LIDARs, APDs, SiPMs, and associated electronics), analog and digital integrated circuit design and fabrication, design of diagnostic electrical and electro-optic instrumentation for scientific research, integrated electrical/biological circuits and systems, array (memory, imagers, and displays) fabrication and design, design of digital processors for signal processing, CAD tool development and online tutorials, low-power interconnect and packaging (electrical and optical) techniques, design of wired/wireless communication and interface circuits, circuit design for the use and storage of renewable energy, power electronics and power supply design, and the delivery of online engineering education. As a result of this work, he is the named inventor on over 150 US patents and the author of over 100 publications.

He is a member of the honor societies Eta Kappa Nu and Tau Beta Pi, a licensed Professional Engineer, a popular lecturer that has delivered over 50 invited talks around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation, CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the 2000 Best Paper Award from the IEEE Power Electronics Society,

the 2007 Frederick Emmons Terman Award, the 2011 IEEE Circuits and Systems Education Award, and the 2021 Wiley-IEEE Press Textbook Award for the 4th Edition of his book CMOS Circuit Design, Layout, and Simulation.

His service activities include the IEEE Press Editorial Board (1999-2004), editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015), the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), Distinguished Lecturer for the SSCS (2012-2015), Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the IEEE Solid-State Circuits Magazine, IEEE Kirchhoff Award Committee (2020-2023), and advisor for the student branch of the IEEE at UNLV (2013-2024).

INDUSTRY EXPERIENCE

2008 - present: Expert witness in intellectual property disputes in electrical, electro-optic, and computer engineering matters for: 1) district court and ITC patent disputes, 2) inter partes reviews at the PTAB, and 3) arbitrations and mediations.

2013 - 2022: Worked with Freedom Photonics, Santa Barbara, CA, on the integration, fabrication and design, of optoelectronics with CMOS integrated circuits. Work includes the design of compact optical transceivers for range finding applications, high-efficiency integrated silicon avalanche photodetectors for quantum key receivers, Geiger mode SiGe receivers for long-range communications, cryptography, and the fabrication of near-infrared focal plane arrays. Packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies using LEDs, ILDs, PIN, APDs, and ROICs.

2017 - 2019: Worked with Vorpal Research Systems, Las Vegas, NV on the design of integrated circuit electronics and optoelectronics for optical transceivers used in LIDARs/LADARs.

2016 - 2019: Worked with Attollo Engineering on the design of transient digitizers for the capture of high-speed signals for range finders using LEDs and lasers in compact optical transceivers.

2013 - 2018: Working with Mission Support and Test Services, LLC (MSTS, formerly National Security Technologies, LLC, [NSTec]) on the Design and Fabrication of Integrated electrical/photonic application specific integrated circuit (ASIC) design for use in the implementation of diagnostic instrumentation.

2013 - 2015: Consultant for OmniVision. Working on integrating CMOS image sensors (CIS) with memory for very high-speed consumer imager products. Design specialty DRAM, high-speed interfaces between CIS and DRAM, packaging techniques to pair the CIS with DRAM.

2010 - 2013: Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2013: Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

2012: Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design and fabrication for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, high-speed interfaces between image processors and imaging systems, and infrared imaging systems.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

2009 - 2010: Sun Microsystems, Inc. (and then Oracle) VLSI research group. Provided consulting on memory circuit design/fabrication and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power, 3D packaging, for memory modules and controllers implemented with FPGAs and custom ASICs.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

1994 - 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs, PLLs for embedded processors, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), SRAMs, RFIDs, CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project

between Micron and HP labs in magnetic memory fabrication and design using the MTJ memory cell. Worked on numerous technologies ranging from LED lighting to medical imaging using CMOS image sensors (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line from fabrication to test. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing.

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1999: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips, interfaces, and serial buses including USB circuits, charging circuits based upon power up/down circuits using an MOS or bandgap reference, pre-amplifiers, comparators, etc.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and processors.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television. Worked on the fabrication and design of video peripheral circuits for these displays.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns rise-time and 8 ns fall-time for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant while finishing up my Ph.D.), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing and fabricating over 30 electronic and electro-optic instruments including: CCD camera design, communication networks, fiber optic transmitters employing high speed laser drive electronics, receivers employing envelop tracking for DC voltage restoration and regeneration of received information, receiver low noise amplifier design, frame synchronizers for re-assembling transmitted images, high-speed SRAM memory system design with battery back-up, calibration equipment design such as a tunnel diode pulse generator for testing compensation of oscilloscopes and DAC design for calibrating CCD readout electronics, power supply and battery charger designs, sweep circuits for streak cameras, Pockel's cell drive electronics, vertical amplifier design using HBTs for analog oscilloscopes used at the Nevada Test Site, and 10 kV ramp designs using a planar triode to name some of the designs.

This position provided considerable fundamental grounding in EE with a broad exposure ranging from the design of PC boards to, for example, the design of cable equalizers. Summarizing, gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuit fabrication and design, GaAs (high speed logic and HBTs), Mach-Zehnder interferometers, Pockels cells, krytrons, power MOSFETs, microwave techniques, power supplies, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble-shooting electric motors on mining equipment.

ACADEMIC EXPERIENCE

January 1991 – present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho**: Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998 - 2000). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit fabrication and design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, Army, DMEA, Navy, and the AFRL.
- Current and past research and development interests are:
  - Design and packaging of electrical/optical systems (e.g., LiDARs/LADARs) using LEDs, semiconductor lasers, lens for focusing and directing light, integrated circuits, and associated control and communication systems/circuits.
  - Capacitive sensing techniques using delta-sigma modulation and interfacing to sensors
  - Design of high-voltage and energy switching circuits
  - Circuit design and fabrication for the control, use, and storage of renewable energy using thermoelectric generators
  - Design of electrical/biological/optical circuits and systems using electrowetting on dielectric for automating and controlling biological experiments
  - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
  - Heterogeneous integration of III-V photonic devices (e.g., FPAs and VCSELs) with CMOS
  - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories, memory modules, and digital systems using custom and non-custom (e.g., FPGAs) implementations
  - Analog and mixed-signal circuit fabrication and design for communication systems, synchronization, energy storage, data conversion, and interfaces
  - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g., magnetic, chalcogenide)
  - Reconfigurable electronics design and fabrication using nascent memory technologies such as the memristor to implement FPGAs
  - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
  - Power electronics circuit design for consumers and consumer electronics including power management and adaptive control to reduce power consumption
  - Design of bandpass delta-sigma modulators for IQ demodulation in wireless communication systems in OFDM, WiFi, 802.11, Bluetooth, 3G, 4G, etc.
  - University prototyping, fabricating, and packaging of integrated circuits
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI design and fabrication, fiber optics, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

EDUCATION

- Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*
- M.S. and B.S. in Electrical Engineering: May 1986 and May 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge*.

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)
Member of the honor societies Eta Kappa Nu and Tau Beta Pi
Licensed Professional Engineer

HONORS AND AWARDS

- Consolidated Students of the University of Nevada, Las Vegas (CSUN) Faculty Award, 2017
- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013, 2014, 2015 and 2016
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2012 - 2015
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Master's graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as a Distinguished Lecturer for the SSCS (2012-2015), as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015, as advisor for the student branch of the IEEE at UNLV (2013-2023), and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the *IEEE Solid-State Circuits Magazine*, and IEEE Kirchhoff Award Committee (2020-2023).

ARMED FORCES

From 1981 to 1987 served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge. Military Occupational Specialty (MOS) was Machine Gunner (MOS 0331)

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Fourth Edition" *Wiley-IEEE Press*, 1234 pages. ISBN 9781119481515 (2019) **Over 50,000 copies of this book in print.** (Third Edition published in 2010, Revised Second Edition published in 2008, and Second Edition Published in 2005)

Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 9780471227540 (First Edition published in 2002)

Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, 201 pages. ISBN: 9780470184752

Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, 201 pages. ISBN 0780360141

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 9780780334168

BOOKS, OTHER (edited, chapters, etc.)

Saxena, V. and Baker, R. J., "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 2000. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 22 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

INVITED TALKS AND SEMINARS

Have given over 50 invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICSEng Keynote, ICySSS keynote, IEEE Computing and Communication Workshop (CCWC), IEEE Electron Devices Conference (NVMTS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Lockheed-Martin, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING

In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. J., (2023-2024) "Silicon Germanium (SiGe) Avalanche Photo Diode (APD) Chip," Department of Energy, Mission Support and Test Services (MSTS), LLC, $120,000
- Baker, R. Jacob, (2017-2023) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit," NASA, $29,999 (Phase I), $225,238 (Phase II), and $79,697 (Phase IIE)
- Goldman, J., Menezes, J., and Baker, R. J., (2021-2022) "Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling," UNLV Sports Research & Innovation Initiative. Proof of Concept Grant Program, $50,000
- Baker, R. Jacob, (2019-2021) "Dual-Mode, Extended Near-Infrared, Focal Plane Arrays Fabricated with CMOS Compatible GeSiSn Alloy Materials," DARPA, $149,998
- Baker, R. Jacob, (2018-2020) "Geiger Mode SiGe Receiver for Long-Range Optical Communications," NASA, $99,996

- Baker, R. Jacob, (2019) "Improved Quantum Efficiency Photo-Detector," Navy, $29,999
- Baker, R. Jacob, (2018-2019) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit – Phase I," NASA, $29,999
- Baker, R. Jacob, (2017-2019) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), $266,029
- Baker, R. Jacob, (2017-2019) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, $299,605
- Baker, R. Jacob, (2016-2018) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, $299,665

DOCTORAL STUDENT SUPERVSION

10. Sachin Namboodiri – A Multi-channel MCP-PMT based Readout Integrated Circuit for LiDAR Applications (2020)
9. Wenlan Wu – High-Speed Radhard Mega-Pixel CIS Camera for High-Energy Physics (2019)
8. Kostas Moutafis – A Highly-Sensitive Global-Shutter CMOS Image Sensor with On-Chip Memory for Hundreds of kilo-frames per second Scientific Experiments (2019)
7. Yiyan Li – Portable High Throughput Digital Microfluidics and On-Chip Bacteria Cultures (2016)
6. Yacouba Moumouni – Designing, Building, and Testing a Solar Thermoelectric Generation, STEG, for Energy Delivery to Remote Residential Areas in Developing Regions (2015)
5. Qawi IbnZayd Harvard – Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design (2011)
4. Vishal Saxena – K-Delta-1-Sigma Modulators for Wideband Analog-to-Digital Conversion (2010)
3. Robert Russell Hay – Digitally-Tunable Surface Acoustic Wave Resonator (2009)
2. Xiangli Li (the first Boise State University College of Engineering PhD graduate) – MOSFET Modulated Dual Conversion Gain CMOS Image Sensors (2008)
1. Feng Lin, Research and Design of Low Jitter, Wide Locking-Range Phase-Locked and Delay-Locked Loops (2000)

MASTERS STUDENT SUPERVISION

91. Jazmine Boloor – Survey of how Irregular Pathways in the Electrical System of the Human Heart Link to Different Heart Arrhythmias (2023)
90. Abraham Lopez – An Avalanche-Transistor-Based Pulse Generator Design For Infrared Laser Applications (2023)
89. David Santiago – Development of an Automated GPIB System for Characterization of SiGe Avalanche Photodiodes (2023)
88. Minsung Cho – Studies of Forward Projection Algorithms and Implementation on PC and FPGA (2023)
87. Armani Alvarez – A Control Integrated Circuit for a Hysteretic Flyback Power Converter (2022)
86. Francisco Mata-carlos – A Wearable Electronic Monitoring Device for Low Pressure Garment Applications and Temperature Analysis for Prevention of Ulceration and Infection (2022)
85. Daniel Senda – Designs and Outcomes of Transcranial Magnetic Stimulation (TMS) and Repetitive Transcranial Magnetic Stimulation (rTMS) Circuits (2021)
84. James Skelly – Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling (2021)
83. Gonzalo Arteaga – Current-mode photon-counting circuit with SiGe BiCMOS input stage (2020)
82. Jason Silic – Design and Fabrication of a 6-bit Current-Mode ADC for Lidar and High-Speed Applications (2020)
81. Brandon Wade (2020)
80. Mario Valles Montenegro – Front-End CMOS Transimpedance Amplifiers on a Silicon Photomultiplier Resistant to Fast Neutron Fluence (2020)
79. Jonathan DeBoy (2018)
78. Dane Gentry – Design, Layout, and Testing of SiGe APDs Fabricated in a BiCMOS Process (2018)
77. James Mellot – Variable Transition Time Inverters in a Digital Delay Line with Analog Storage for Processing Fast Signals and Pulses (2018)
76. Eric Monahan – High Speed Fast Transient Digitizer Design and Simulation (2018)
75. Shada Sharif – Design and Analysis of First and Second Order K-Delta-1-Sigma Modulators in Multiple Fabrication Processes (2018)
74. Vikas Vinayaka – Analysis and Design of Analog Front-End Circuitry for Avalanche Photodiodes (APD) and Silicon Photo-Multipliers (SiPM) in Time-of-Flight Applications (2018)

73. Claire Tsagkari – Design, Fabrication and Testing of a Capacitive Sensor Using Delta-Sigma Modulation (2017)
72. Kevin Buck – Fast Transient Digitizer and PCB Interface (2015)
71. Marzieh Sharbat Maleki (2015)
70. Angsuman Roy – Design, Fabrication and Testing of Monolithic Low-Power Passive Sigma-Delta Analog-to-Digital Converters (2015)
69. Daniel Anderson – Design and Implementation of an Instruction Set Architecture and Instruction Execution Unit for the RZ9 Coprocessor System (2014)
68. Jared Gordon – Design and Fabrication of an Infrared Optical Pyrometer ASIC (2013)
67. Justin Butterfield (2012)
66. Adam Johnson – Methods and Considerations for Testing Resistive Memories (2012)
65. Ben Millemon – CMOS Characterization, Modeling, and Circuit Design in the Presence of Random Local Variation (2012)
64. Justin Wood (2012)
63. Chamunda Ndinawe Chamunda (2011)
62. Gary VanAckern – Design Guide for CMOS Process On-Chip 3D Inductors using Thru-Wafer Vias (2011)
61. Lucien Jan Bissey – High-Voltage Programmable Delta-Sigma Modulation Voltage-Control Circuit (2010)
60. Kaijun Li (2010)
59. Yingting Li (co-supervised with Maria Mitkova) (2010)
58. Lael Matthews (co-supervised with Said Ahmed-Zaid) (2010)
57. Priyanka Mukeshbhai Parikh (2010)
56. Todd Plum (co-supervised with Jeff Jessing) – Design and Fabrication of a Chemicapacitive Sensor for the Detection of Volatile Organic Compounds (2010)
55. Rahul Srikonda (2010)
54. Avani Falgun Trivedi (2010)
53. Kuang Ming Yap – Gain and Offset Error Correction for CMOS Image Sensors using Delta-Sigma Modulation (2010)
52. Mahesh Balasubramanian – Phase Change Memory - Array Development and Sensing Circuits using Delta-Sigma Modulation (2009)
51. Lincoln Bollschweiler (2009)
50. Shantanu Gupta (2009)
49. Qawi Harvard – Wide I_O DRAM Architecture Utilizing Proximity Communication (2009)
48. Avinash Rajagiri (2009)
47. Ramya Ramarapu (2009)
46. Harikrishna Rapole (2009)
45. Aruna Vadla (2009)
44. Hemanth Ande (2008)
43. Curtis Cahoon – Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References (2008)
42. Prashanth Busa (2008)
41. John McCoy III (2008)
40. Dennis Montierth – Using Delta-Sigma-Modulation for Sensing in a CMOS Imager (2008)
39. Rudi Rashwand (2008)
38. Barsha Shrestha (co-supervised with Zhu Han) – Wireless Access in Vehicular Environments using Bit Torrent and Bargaining (2008)
37. Eric Becker – Design of an Integrated Half-Cycle Delay Line Duty Cycle Corrector Delay Locked Loop (2007)
36. Matthew Leslie – Noise-Shaping Sense Amplifier for Cross-Point Arrays (2007)
35. Jose Monje (2007)
34. Sanghyun Park (2007)
33. Vishal Saxena – Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers (2007)
32. Meshack Appikatla (2006)
31. Eric Booth – Wide Range, Low Jitter Delay-Locked Loop Using a Graduated Digital Delay Line and Phase Interpolator (2006)

30. Sucheta Das (2006)
29. Krishna Duvvada – High Speed Digital CMOS Input Buffer Design (2006)
28. Krishnamraju Kurra (2006)
27. Soumya Narasimhan (2006)
26. Roger Porter (2006)
25. David Butler – Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes (2005)
24. Dragos Dimitriu (2005)
23. Surendranath Eruvuru – Sensing Circuit Design for an Ion Mobility Spectrometer (2005)
22. Sandhya Sandireddy (2005)
21. Harish Singidi (2005)
20. Indira Vemula – Delta-Sigma Modulator Used in CMOS Imagers (2005)
19. Bhavana Kollimarla – A 1-Bit Analog-to-Digital Converter Using Delta Sigma Modulation for Sensing in CMOS Imagers (2004)
18. Sandeep Pemmaraju – High Voltage Charge Pump Circuit for an Ion Mobility Spectrometer (2004)
17. Ravindra Puthumbaka – Circuit Design for an Ion Mobility Spectrometer (2004)
16. Brandon Roth – Comparison of Asynchronous vs. Synchronous Design Technologies using a 16-bit Binary Adder (2004)
15. Jennifer Taylor – Reading and Writing Flash Memory Using Delta-Sigma Modulation (2004)
14. Jing Plaisted – Methods for Memory Testing (2003)
13. Murugesh Subramaniam – Flash Memory Sensing Using Averaging (2003)
12. Brian Johnson – Application of an Asynchronous FIFO in a DRAM Data Path (2002)
11. Scott Ward – Electrostatic Discharge (ESD) Protection in CMOS (2002)
10. Tyler Gomm – Design of a Delay-Locked Loop with a DAC-Controlled Analog Delay Line (2001)
9. Gexin Huang (2001)
8. Chris Atkins (2000)
7. Thaddeus Black (2000)
6. Zuxu Qin (2000)
5. Hao Chen (1999)
4. Doug Hackler (co-supervised with Steve Parke) – TMOS: A Novel Design for MOSFET Technology (1999)
3. Song Liu – Design of a CMOS 6-bit Folding and Interpolating Analog-to-Digital Converter (1999)
2. Ben Ba (1997)
1. Brent Keeth – A Novel Architecture for Advanced High Density Dynamic Random Access Memories (1996)

GRANTED US PATENTS

152. Baker, R. J., “Quantizing circuits having improved sensing,” **10,658,018**, May 19, 2020.
151. Baker, R. J., “Quantizing circuits having improved sensing,” **10,403,339**, September 3, 2019.
150. Baker, R. J., “Digital Filters with Memory,” **10,366,744**, July 30, 2019.
149. Baker, R. J., “Quantizing circuits having improved sensing,” **10,127,954**, November 13, 2018.
148. Baker, R. J. and Parkinson, W., “NMOS regulated voltage reference,” **9,753,481**, September 5, 2017.
147. Baker, R. J., “Digital Filters with Memory,” **9,734,894**, August 15, 2017.
146. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **9,697,883**, July 7, 2017
145. Baker, R. J., “Comparators for delta-sigma modulators,” **9,641,193**, May 2, 2017.
144. Baker, R. J., “Quantizing circuits having improved sensing,” **9,449,664**, September 20, 2016.
143. Baker, R. J., “Error detection for multi-bit memory,” **9,336,084**, May 10, 2016.
142. Baker, R. J. and Keeth, B., “Optical interconnect in high-speed memory systems,” **9,299,423**, March 29, 2016.
141. Baker, R. J., “Methods for sensing memory elements in semiconductor devices,” **9,299,405**, March 29, 2016.
140. Baker, R. J., “Comparators for delta-sigma modulators,” **9,135,962**, September 15, 2015.
139. Baker, R. J., “Resistive memory element sensing using averaging,” **9,081,042**, July 14, 2015.
138. Baker, R. J., “Digital Filters with Memory,” **9,070,469**, June 30, 2015.
137. Baker, R. J., "Reference current sources,” **8,879,327**, November 4, 2014.
136. Baker, R. J. and Beigel, K. D., “Multi-resistive integrated circuit memory,” **8,878,274**, November 4, 2014.
135. Baker, R. J., “Methods for sensing memory elements in semiconductor devices,” **8,854,899**, October 7, 2014.

134. Baker, R. J., "Quantizing circuits with variable parameters," **8,830,105**, September 9, 2014.
133. Baker, R. J., "Integrators for delta-sigma modulators," **8,754,795**, June 17, 2014.
132. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,717,220**, May 6, 2014.
131. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **8,712,249**, April 29, 2014.
130. Baker, R. J., "Resistive memory element sensing using averaging," **8,711,605**, April 29, 2014.
129. Baker, R. J., "Memory with correlated resistance," **8,681,557**, March 25, 2014.
128. Baker, R. J., "Reference current sources," **8,675,413**, March 18, 2014.
127. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,582,375**, November 12, 2013.
126. Linder, L. F., Renner, D., MacDougal, M., Geske, J., and Baker, R. J., "Dual well read-out integrated circuit (ROIC)," **8,581,168**, November 12, 2013.
125. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **8,516,292**, August 20, 2013.
124. Baker, R. Jacob, "Resistive memory element sensing using averaging," **8,441,834**, May 14, 2013.
123. Qawi, Q. I., Drost, R. J., and Baker, R. Jacob, "Increased DRAM-array throughput using inactive bitlines," **8,395,947**, March 12, 2013.
122. Baker, R. Jacob, "Memory with correlated resistance," **8,289,772**, October 16, 2012.
121. Lin, F. and Baker, R. Jacob, "Phase splitter using digital delay locked loops," **8,218,708**, July 10, 2012.
120. Baker, R. Jacob, "Subtraction circuits and digital-to-analog converters for semiconductor devices," **8,194,477**, June 5, 2012.
119. Baker, R. J., "Digital Filters for Semiconductor Devices," **8,149,646**, April 3, 2012.
118. Baker, R. J., "Error detection for multi-bit memory," **8,117,520**, February 14, 2012.
117. Baker, R. J., "Integrators for delta-sigma modulators," **8,102,295**, January 24, 2012.
116. Baker, R. J., "Devices including analog-to-digital converters for internal data storage locations," **8,098,180**, January 17, 2012.
115. Baker, R. J. and Beigel, K. D., "Multi-resistive integrated circuit memory," **8,093,643**, January 10, 2012.
114. Baker, R. J., "Quantizing circuits with variable parameters," **8,089,387**, January 3, 2012.
113. Baker, R. J., "Reference current sources," **8,068,367**, November 29, 2011.
112. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,068,046**, November 29, 2011.
111. Baker, R. J., "Systems and devices including memory with built-in self-test and methods of making using the same," **8,042,012**, October 18, 2011.
110. Baker, R. J., "Memory with correlated resistance," **7,969,783**, June 28, 2011.
109. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **7,941,056**, May 10, 2011.
108. Baker, R. J., "K-delta-1-sigma modulator," **7,916,054**, March 29, 2011.
107. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,877,623**, January 25, 2011.
106. Lin, F. and Baker, R. J., "Phase splitter using digital delay locked loops," **7,873,131**, January 18, 2011.
105. Hush, G. and Baker, R. J., "Complementary bit PCRAM sense amplifier and method of operation," **7,869,249**, January 11, 2011.
104. Baker, R. J., "Subtraction circuits and digital-to-analog converters for semiconductor devices," **7,839,703**, November 23, 2010.
103. Baker, R. J., "Digital Filters with Memory" **7,830,729**, November 9, 2010.
102. Baker, R. J., "Systems and devices including memory with built-in self test and methods of making using the same," **7,818,638**, October 19, 2010.
101. Baker, R. J., "Integrators for delta-sigma modulators," **7,817,073**, October 19, 2010.
100. Baker, R. J., "Digital filters for semiconductor devices," **7,768,868**, August 3, 2010.
99. Baker, R. J., "Quantizing circuits with variable reference signals," **7,733,262**, June 8, 2010.
98. Baker, R. J., "Quantizing circuits for semiconductor devices," **7,667,632**, February 23, 2010.
97. Baker, R. J., and Beigel, K. D., "Multi-resistive integrated circuit memory," **7,642,591**, January 5, 2010.
96. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,616,474**, November 10, 2009.
95. Baker, R. J., "Resistive memory element sensing using averaging," **7,577,044**, Aug. 18, 2009.

94. Baker, R. J., "Quantizing circuits with variable parameters," **7,538,702**, May 26, 2009.
93. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,528,877**, May 5, 2009.
92. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,515,188**, April 7, 2009.
91. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,495,964**, February 24, 2009.
90. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,489,575**, February 10, 2009.
89. Baker, R. J., "Per column one-bit ADC for image sensors," **7,456,885**, November 25, 2008.
88. Staples, T. and Baker, R. J., "Input buffer design using common-mode feedback," **7,449,953**, November 11, 2008.
87. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,421,607**, September 2, 2008.
86. Baker, R. J., "Methods for resistive memory element sensing using averaging," **7,372,717**, May 13, 2008.
85. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,366,021**, April 29, 2008.
84. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor and method of operation," **7,366,003**, April 29, 2008.
83. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,330,390**, February 12, 2008.
82. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,319,620**, January 15, 2008.
81. Staples, T. and Baker, R. J., "Method and apparatus providing input buffer design using common-mode feedback," **7,310,018**, December 18, 2007.
80. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,286,428**, October 23, 2007.
79. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,271,635**, September 18, 2007.
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77. Hush, G., Baker, R. J., and Moore, J., "Skewed sense AMP for variable resistance memory sensing," **7,251,177**, July 31, 2007.
76. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor," **7,242,603**, July 10, 2007.
75. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,237,136**, June 26, 2007.
74. Moore, J. and Baker, R. J., "Rewrite prevention in a variable resistance memory," **7,224,632**, May 29, 2007.
73. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **7,151,698**, December 19, 2006.
72. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **7,151,689**, December 19, 2006.
71. Baker, R. J., "Resistive memory element sensing using averaging," **7,133,307**, Nov. 7, 2006.
70. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **7,123,525**, October 17, 2006.
69. Baker, R. J., and Beigel, K. D., "Integrated circuit memory with offset capacitor," **7,109,545**, September 19, 2006.
68. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,102,932**, September 5, 2006.
67. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,095,667**, August 22, 2006.
66. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,082,045**, July 25, 2006.
65. Baker, R. J., "System and method for sensing data stored in a resistive memory element using one bit of a digital count," **7,009,901**, March 7, 2006.
64. Hush, G. and Baker, R. J., "Complementary bit resistance memory sensor and method of operation," **7,002,833**, February 21, 2006.
63. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **6,987,701**, January 17, 2006.

62. Baker, R. J., “Adjusting the frequency of an oscillator for use in a resistive sense amp,” **6,985,375**, January 10, 2006.
61. Baker, R. J., “Method for reducing power consumption when sensing a resistive memory,” **6,954,392**, October 11, 2005.
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59. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **6,954,390**, October 11, 2005.
58. Lin, F. and Baker, R. J., “Phase splitter using digital delay locked loops,” **6,950,487**, September 27, 2005.
57. Baker, R. J., “Method and apparatus for measuring current as in sensing a memory cell,” **6,930,942**, August 16, 2005.
56. Baker, R. J., “Offset compensated sensing for a magnetic random access memory,” **6,917,534**, July 12, 2005.
55. Baker, R. J., “Dual loop sensing scheme for resistive memory elements,” **6,914,838**, July 5, 2005.
54. Baker, R. J., “High speed low power input buffer,” **6,914,454**, July 5, 2005.
53. Baker, R. J., and Beigel, K. D., “Method for stabilizing or offsetting voltage in an integrated circuit,” **6,913,966**, July 5, 2005.
52. Moore, J. and Baker, R. J., “PCRAM rewrite prevention,” **6,909,656**, June 21, 2005.
51. Baker, R. J., “Integrated charge sensing scheme for resistive memories,” **6,901,020**, May 31, 2005.
50. Hush, G., Baker, R. J., and Moore, J., “Skewed sense AMP for variable resistance memory sensing,” **6,888,771**, May 3, 2005.
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48. Moore, J. and Baker, R. J., “PCRAM rewrite prevention,” **6,882,578**, April 19, 2005.
47. Baker, R. J., “Integrated charge sensing scheme for resistive memories,” **6,870,784**, March 22, 2005.
46. Baker, R. J., “Sensing method and apparatus for a resistive memory device,” **6,859,383**, February 22, 2005.
45. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **6,856,564**, February 15, 2005.
44. Baker, R. J., “Offset compensated sensing for a magnetic random access memory,” **6,856,532**, February 15, 2005.
43. Baker, R. J., “Dual loop sensing scheme for resistive memory elements,” **6,829,188**, Dec. 7, 2004.
42. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **6,826,102**, Nov. 30, 2004.
41. Baker, R. J., “Resistive memory element sensing using averaging,” **6,822,892**, Nov. 23, 2004.
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39. Baker, R. J., “Wordline driven method for sensing data in a resistive memory array,” **6,809,981**, Oct. 26, 2004.
38. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **6,798,705**, Sept. 28, 2004.
37. Baker, R. J., “Methods and apparatus for measuring current as in sensing a memory cell,” **6,795,359**, Sept. 21, 2004.
36. Hush, G. and Baker, R. J., “Complementary bit PCRAM sense amplifier and method of operation,” **6,791,859**, Sept. 14, 2004.
35. Baker, R. J., “Method and apparatus for sensing resistance values of memory cells,” **6,785,156**, August 31, 2004.
34. Lin, F. and Baker, R. J., “Phase detector for all-digital phase locked and delay locked loops,” **6,779,126**, August 17, 2004.
33. Baker, R. J., and Lin, F. "Digital dual-loop DLL design using coarse and fine loops," **6,774,690**, August 10, 2004.
32. Hush, G., Baker, R. J., and Voshell, T., “Producing walking one pattern in shift register,” **6,771,249**, August 3, 2004.
31. Baker, R. J., “Sensing method and apparatus for resistance memory device,” **6,741,490**, May 25, 2004.
30. Li, W., Schoenfeld, A., and Baker, R. J., “Method and apparatus for providing symmetrical output data for a double data rate DRAM,” **6,704,881**, March 9, 2004.
29. Baker, R. J., “Method and system for writing data in an MRAM memory device,” **6,687,179**, February 3, 2004.
28. Baker, R. J., “High speed digital signal buffer and method,” **6,683,475**, January 27, 2004.
27. Baker, R. J., “High speed low power input buffer,” **6,600,343**, July 29, 2003.
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22. Baker, R. J. and Beigel, K. D., "Electronic device with interleaved portions for use in integrated circuits," **6,509,245**, January 21, 2003.
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20. Baker, R. J., "High-speed digital signal buffer and method," **6,483,347**, November 19, 2002.
19. Baker, R. J., and Lin, F., "Digital dual-loop DLL design using coarse and fine loops," **6,445,231**, September 3, 2002.
18. Baker, R. J., "Method and apparatus for receiving synchronous data," **6,424,684**, July 23, 2002.
17. Baker, R. J. and Beigel, K. D., "Comb-shaped capacitor for use in integrated circuits," **6,410,955**, June 25, 2002.
16. Baker, R. J., "High-speed, low-power input buffer," **6,407,588**, June 18, 2002.
15. Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "Method and apparatus for improving the performance of digital delay locked loop circuits," **6,316,976**, Nov. 13, 2001.
14. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,256,234**, July 3, 2001.
13. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,104,209**, August 15, 2000.
12. Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "Method and apparatus for improving the performance of digital delay locked loop circuits," **6,069,506**, May 30, 2000.
11. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,026,051**, February 15, 2000.
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9. Baker, R. J., and Manning, T. A., "Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same," **5,953,284**, September 14, 1999.
8. Baker, R. J., "Fully-differential amplifier," **5,953,276**, September 14, 1999.
7. Hush, G., Baker, R. J., and Voshell, T., "Timing Control for a Matrixed Scanned Array". **5,909,201**, June 1, 1999.
6. Hush, G. and Baker, R. J., "Field emission display having pulsed capacitance current control," **5,894,293**, April 13, 1999.
5. Baker, R. J., "Adaptively biased voltage regulator and operating method," **5,874,830**, February 23, 1999.
4. Hush, G. Baker, R. J., and Voshell, T., "Serial to Parallel Conversion with a Phase-Locked Loop," **5,818,365**, October 1, 1998.
3. Hush, G., Baker, R. J., and Voshell, T., "Timing Control for a Matrixed Scanned Array," **5,638,085**, June 10, 1997.
2. Wilson, A. J., Baker, R. J., and Schoenfeld, A., "Waveshaping circuit generating two rising slopes for a sense amplifier pulldown device," **5,614,856**, March 25, 1997.
1. Hush, G., Baker, R. J., and Voshell, T., "Serial to Parallel Conversion with a PLL," **5,598,156**, January 28, 1997.

INVITED TALKS (PARTIAL LISTING)

- Harvard, Q. I. and Baker, R. J., “Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design,” a presentation covering semiconductor packaging, DRAM architectures, and I/O circuits. The goal of this work is to investigate replacing the currently used dual in-line memory modules (DIMMs) with a smaller and a lower power memory module, a “Nano-Module.”
- Baker, R. J., and Campbell, K. A., “Reconfigurable Analog Electronics using the Memristor.”
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3. Boyce, D.E. and Baker, R. J., "A Complete Layout System for the PC," *IEEE 40th International Midwest Symposium on Circuits and Systems*, 1997.
2. Baker, R. J., and Blair, J. J., "Step response considerations and the design of a suitable step generator for high speed digitizer testing," *LLNL's Third Annual Workshop on High Speed Digitizers,* April 3-4, Las Vegas, Nevada, 1991.
1. Baker, R. J., "Step-recovery diodes sharpen pulses," *Engineering Design News Magazine*, pp. 154-156, May 10, 1990.

EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services in electrical and computer engineering are listed below. I have been deposed 105 times, given expert testimony at 14 trials (7 USITC, 2 D. Del., 1 Arbitr., 1 S.D. Cal., 1 N.D. Ga., 1 D. Ore., and 1 E.D. Tex.), and participated in 1 mediation.

DLA Piper LLP (Palo Alto, CA and Austin, TX)

Case – *BOE Technology Group Co., Ltd.* v. Optronic Sciences LLC
Case Numbers – IPR2024-01130, IPR2024-01133, and IPR2024-01134. Petitions filed on July 5, 2024
Case Subject Matter – Imaging pixels, layout, and fabrication. Light emitting devices, including packaging, covers, and structures.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Dentons US LLP (Washington, DC)

Case – *Reolink Digital Technology Co., Ltd.* v. KT Imaging US, LLC

Case Numbers – IPR2024-01154 and IPR2024-01155. Petitions filed on July 3, 2024

Case Subject Matter – Image sensor structure and package with integrated lens module for digital image products such as digital cameras, camera phones, video phones, fingerprint readers and so on.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/019,560, 90/019,962, and 90/019,964. Requests filed on July 1, 2024

Case Numbers – 90/019,556, 90/019,557, and 90/019,558. Requests filed on June 28, 2024.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for ex parte reviews.

Banner Witcoff (Chicago, IL and Washington, DC)

Case – *ZF Friedrichshafen AG, ZF Active Safety and Electronics US LLC, and Nissan Motor Company, Ltd.* v. Foras Technologies, Ltd.

Case Number – IPR2024-00969. Petition filed on June 24, 2024.

Case Subject Matter – Detecting loss of lockstep between pairs of processors and loss of lockstep recovery

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Fish & Richardson P.C. (San Diego, CA and Boston, MA)

Case – *Vicor Corporation* v. Delta Electronics, Inc.

Case Numbers – IPR2024-00704, IPR2024-00705, IPR2024-00706, and IPR2024-00715. Petitions filed on March 25, 2024.

Case Subject Matter – Power converters including design, packaging, heatsinking and manufacturing. Resonant converters with overcurrent protection.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Winston & Strawn LLP (Los Angeles, CA and Redwood City, CA)

Case – *Silicon Motion, Inc.* v. Unification Technologies LLC

Case Number – IPR2024-00199. Petition filed on December 18, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Garlick & Markison, LLC (Austin, TX)

Case – *NXP USA, Inc.* v. Bell Semiconductor, LLC

Case Numbers – IPR2024-00167 and IPR2024-00168. Petitions filed on November 9, 2023.

Case Subject Matter – Semiconductor manufacturing processes, fabrication and packaging of integrated circuits, layout and routing of signal lines.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019288. Request filed on October 20, 2023.

Case Subject Matter – Power conversion device to drive an alternating-current motor for an electric vehicle.

Work Performed – Provided expert consulting services and wrote declaration.

Haynes and Boone, LLP (Dallas, TX)

Case – *Western Digital Technologies, Inc.* v. Longitude Licensing LTD.

Case Number – IPR2023-01200. Petition filed on July 14, 2023.

Case Subject Matter – Communications between a memory controller and memory.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Mojo Mobility, Inc.

Case Numbers – IPR2023-01094, IPR2023-01095, IPR2023-01096, IPR2023-01097, IPR2023-01098, IPR2023-01099, IPR2023-01100, and IPR2023-01124. Petitions filed on June 30, 2023.

Case Numbers – IPR2023-01101 and IPR2023-01102. Petitions filed on June 29, 2023.

Case Numbers – IPR2023-01091, IPR2023-01092, and IPR2023-01093. Petitions filed on June 28, 2023.

Case Numbers – IPR2023-01086, IPR2023-01087, IPR2023-01088, IPR2023-01089, and IPR2023-01090. Petitions filed on June 27, 2023.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Winston & Strawn LLP (Los Angeles, CA, Redwood City, CA, Chicago, IL, and Houston, TX)

Case – Unification Technologies LLC v. *Silicon Motion, Inc.*

Case Number – Texas, ED (Marshall) 2:23-cv-00267. Complaint filed June 2, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services.

Norton Rose Fulbright LLP (Austin, TX and Dallas, TX)

Case – *Current Lighting Solutions, LLC d/b/a GE Current* v. Jiaxing Super Lighting Electric Appliance Co., Ltd.

Case Numbers – IPR2023-00979 and IPR2023-00980. Petitions filed on May 31, 2023.

Case Number – IPR2023-00270. Petition filed on December 19, 2022.

Case Number – IPR2023-00271. Petition filed on December 14, 2022.

Case Subject Matter – LED lighting, lamps, tube lamps, assembly, and associated circuits and electronics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes review.

Baker Botts LLP (Dallas, TX)

Case – *Lennox Industries Inc.* v. Rosen Technologies LLC

Case Numbers – IPR2023-00715, IPR2023-00716, IPR2023-00717, IPR2023-00718, and IPR2023-00719. Petitions filed on March 29, 2023.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Cooley LLP (Palo Alto, CA)

Case – *Nintendo Co., Ltd. and Nintendo of America Inc.* v. Polaris PowerLED Technologies, LLC

Case Number – IPR2023-00778. Petition filed on March 28, 2023.

Case Subject Matter – Visual displays, circuit design, and related technologies.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Bracewell LLP (New York, NY and Seattle, WA)

Case – *Kioxia America, Inc. and Kioxia Corporation* v. BiTMICRO LLC

Case Numbers – IPR2023-00741, IPR2023-00742, and IPR2023-00743. Petitions filed on March 23, 2023.

Case Subject Matter – Solid-state storage devices utilizing multi-profile memory controllers. Optimizing memory operations in a memory system suitable for use in an electronic storage device. Supplying energy to a cache memory using a super capacitor.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Bookoff McAndrews, PLLC (Washington, DC)

Case – *Lenovo Inc. and Motorola Mobility LLC* v. Theta IP, LLC

Case Numbers – IPR2023-00694, IPR2023-00697, and IPR2023-00698. Petitions filed on March 7, 2023.

Case Subject Matter – Power in wireless communication circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA)

Case – Semiconductor Design Technologies LLC v. *Cadence Design Systems, Inc.*

Case Number – California, ND 3:23-cv-01001. Complaint filed March 6, 2023.

Case Subject Matter – Semiconductor design support device/method and manufacturing method for semiconductor integrated circuit.

Work Performed – Provided expert consulting services.

McDermott Will & Emery LLP (Chicago, IL and Austin, TX)

Case – *Xilinx, Inc.* v. Polaris Innovations Limited

Case Numbers – IPR2023-00513 and IPR2023-00514. Petitions filed on February 6, 2023.

Case Subject Matter – Methods for terminating a memory chip with various termination resistances and output drivers for integrated circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed**.**

Willkie Farr & Gallagher LLP (San Franciso, CA)

Case –Bell Semiconductor, LLC. v. *Synopsys, Inc.*

Case Number – California, SD 3:22-cv-00594. Complaint filed on January 31, 2023.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services and wrote expert reports.

Fish & Richardson P.C. (Washington, DC, Atlanta, GA, and Boston, MA)

Case – Element Capital Commercial Company PTE. LTD v. *BOE Technology Group Co. LTD and Motorola (Wuhan) Mobility*

Case Number – Texas, ED (Marshall) 2:22-cv-00118. Complaint filed January 11, 2023.

Case Subject Matter – Display technology, layout, circuit design, pixel design and fabrication.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Baker Botts LLP (San Franciso, CA and New York, NY) and O'Melveny & Myers LLP (Los Angeles, CA)

Case – Polaris PowerLED, LLC v. *Samsung Electronics and Samsung Display*

Case Number – Texas, ED (Marshall) 2:22-cv-00469. Complaint filed December 12, 2022.

Case Subject Matter – active matrix organic light-emitting diode (AMOLED) displays, controlling the intensity of light-emitting diodes in backlights of displays, control circuits for adjusting current delivery based upon temperature.

Work Performed – Provided expert consulting services including writing a declaration for claim construction.

Arnold & Porter (Los Angeles and Palo Alto, CA) and Willkie Farr & Gallagher LLP (San Franciso, CA)

Case – *Synopsys, Inc. and Cadence Design Systems, Inc.* v. Bell Semiconductor, LLC.

Case Number – Delaware, 1:22-cv-01512. Complaint filed on November 18, 2022.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/015155 and 90/015156. Requests filed on November 7, 2022.

Case Number – 90/015134. Request filed on October 14, 2022.

Case Number – 90/015130. Request filed on September 30, 2022.

Case Subject Matter – Packaging and fabrication of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declaration.

Russ August & Kabat (Los Angeles, CA)

Case – *Resonant Systems, Inc.* v. Sony
Case Number – Texas, ED (Marshall) 2:22-cv-00424. Complaint filed on October 26, 2022.
Case Subject Matter – Linear vibration modules and linear-resonant vibration modules.
Work Performed – Provided expert consulting services and wrote claim construction disclosure.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA) and Willkie Farr & Gallagher LLP (San Francisco, CA)

Case – Bell Semiconductor, LLC v. *NXP*, SMC, Micron, Nvidia, *Advanced Micro Devices (AMD)*, *Acer*, Infineon, Qualcomm, Motorola Mobility, and Western Digital
Case Number – ITC Investigation No. 337-TA-1340. Complaint filed October 6, 2022.
Case Subject Matter – Electronic devices, semiconductor devices, and components.
Work Performed – Provided expert consulting services.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Daedalus Prime LLC v. *Samsung Electronics* and Qualcomm Inc.
Case Number – ITC Investigation No. 337-TA-1335. Complaint filed September 12, 2022.
Case Subject Matter – Semiconductor devices, mobile devices, and components.
Work Performed – Provided expert consulting services.

Fish & Richardson P.C. (Boston, MA, Houston, TX, and Washington, DC)

Case – Sonrai Memory LTD. v. *Micron Technology, Inc.*
Case Number – Texas, WD (Waco) 6:22-cv-00855 and Texas, WD (Waco) 1:23-cv-01407. Complaint filed August 16, 2022.
Case Subject Matter – Portable RAM drive and variable charge pump circuit with dynamic load.
Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Russ August & Kabat (Los Angeles, CA and New York, NY)

Case – *NextGen Innovations, LLC* v. Infinera, Fujitsu, AT&T, and Nokia
Case Number – Texas, ED (Marshall) 2:22-cv-00306, Texas, ED (Marshall) 2:22-cv-00307, Texas, ED (Marshall) 2:22-cv-00308, and Texas, ED (Marshall) 2:22-cv-00309. Complaints filed on August 9, 2022.
Case Subject Matter – optical transmission systems including optical components for encoding, transmission (fiber optic transmitters and receivers), and decoding of data and related standards and concepts.
Work Performed – Provided expert consulting services, wrote claim construction disclosure, wrote expert reports, and was deposed twice.

DLA Piper (Chicago, IL and Washington, DC)

Case – Ampt, LLC v. *SolarEdge Technologies, Inc.*
Case Number – ITC Investigation No. 337-TA-1327. Complaint filed July 28, 2022.
Case Subject Matter – Solar power optimizers, inverters, and components.
Work Performed – Provided expert consulting services including writing declarations for claim construction, expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Signify North America Corporation v. *Shenzhen Intellirocks Tech Co.*
Case Number – Texas, WD (Waco) 6:22-cv-00760. Complaint filed on July 8, 2022.
Case Subject Matter – LED packaging, circuits, and systems.
Work Performed – Provided expert consulting services including writing declaration for claim construction. Was deposed.

Baker Botts LLP (Dallas, TX)

Case – Rosen Technologies LLC v. *Lennox Industries Inc.*
Case Number – Texas, ND (Dallas) 3:22-cv-00732. Complaint filed on June 7, 2022.
Case Subject Matter – Thermostat system communications, programming, and displays.
Work Performed – Provided expert consulting services.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Scramoge Technology Ltd.
Case Numbers – IPR2022-01052, IPR2022-01053, and IPR2022-01058. Petitions filed on May 26, 2022.
Case Numbers – IPR2022-01054, IPR2022-01055, IPR2022-01056, and IPR2022-01057. Petitions filed on May 24, 2022.
Case Number – IPR2022-00939. Petition filed on April 29, 2022.
Case Subject Matter – An antenna that supports wireless charging using switching power supplies such as flyback converters.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Ex Parte Reexaminations
Case Number – 90/015020. Request filed on May 2, 2022.
Case Number – 90/014906. Request filed on November 12, 2021.
Case Number – 90/014899. Request filed on November 10, 2021.
Case Number – 90/014888. Request filed on October 21, 2021.
Case Numbers – 90/014886 and 90/014887. Requests filed on October 20, 2021.
Case Number – 90/014885. Request filed on October 19, 2021.
Case Subject Matter – Universal Serial Bus (USB) for charging.
Work Performed – Provided expert consulting services and wrote declarations**.**

DLA Piper (Chicago, IL, Austin, TX, and Washington, DC)

Case – *SolarEdge Technologies, Inc.* v. Fronius International GMBH
Case Number – IPR2022-00849. Petition filed on April 14, 2022.
Case Subject Matter – Mechanical assembly and enclosure whereby an upper housing part is detached from a lower housing part using a "rotate-and-lift" feature.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Kirkland & Ellis LLP (New York, NY)

Case – *Samsung Electronics Co.* v. Sonrai Memory Ltd.
Case Numbers – IPR2022-00305 and IPR2022-00306. Petitions filed on December 10, 2021.
Case Subject Matter – USB devices and circuits for saving power.
Work Performed – Provided expert consulting services including writing declarations for inter partes reviews.

Haynes and Boone, LLP (Washington, DC)

Case – *Unified Patents, LLC* v. Arigna Technology Limited
Case Number – IPR2022-00285. Petition filed on December 9, 2021.
Case Subject Matter – High voltage driver circuit for driving power devices such as insulated gate bipolar transistors (IGBTs).
Work Performed – Provided expert consulting services, wrote declaration for inter partes review and was deposed.

Paul Hastings LLP (Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Lynk Labs, Inc.
Case Numbers – IPR2022-00149 and IPR2022-00150. Petitions filed on November 12, 2021
Case Numbers – IPR2022-00100 and IPR2022-00101. Petitions filed on October 28, 2021.
Case Numbers – IPR2022-00051, IPR2022-00052, and IPR2022-00098. Petitions filed on October 27, 2021.
Case Numbers – IPR2021-01575 and IPR2021-01576. Petitions filed on October 1, 2021.
Case Numbers – IPR2021-01299, IPR2021-01300, IPR2021-01345, IPR2021-01346, and IPR2021-01347. Petitions filed on September 7, 2021.
Case Subject Matter – Circuit design, including switching power supply design (e.g., flyback), rectifiers, power factor correction, etc. for lighting and displays using light emitting diodes (LEDs).
Work Performed – Provided expert consulting services, wrote declarations, and was deposed ten times.

Haynes and Boone, LLP (Plano, TX)

Case – *Pure Storage, Inc.* v. Digital Cache, LLC

Case Number – IPR2022-00121. Petition filed on October 29, 2021.

Case Subject Matter – Non-volatile memory (NVM) devices capable of retaining stored data in case of a power failure.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Banner Witcoff (Washington, DC)

Case – *SolarEdge Technologies Ltd.* v. Koolbridge Solar, Inc.

Case Numbers – IPR2022-00007, IPR2022-00008, IPR2022-00009, IPR2022-00010, IPR2022-00011, and IPR2022-00012. Petitions filed on October 11, 2021.

Case Numbers – IPR2022-00013, IPR2022-00014, and IPR2022-00015. Petitions filed on October 8, 2021.

Case Subject Matter – DC-to-AC converters using full-bridges, multi-level conversion for power systems, and other electronics for harvesting solar energy.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. LED Wafer Solutions LLC

Case Number – IPR2021-01554. Petition filed on September 20, 2021.

Case Number – IPR2021-01526. Petition filed on September 10, 2021.

Case Number – IPR2021-01506. Petition filed on September 7, 2021.

Case Number – IPR2021-01491. Petition filed on September 3, 2021.

Case Subject Matter – Packaging of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declarations.

Paul Hastings, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/014,846. Request filed on August 30, 2021.

Case Subject Matter – Wireless power transmission and ways to wirelessly charge and/or discharge a battery.

Work Performed – Provided expert consulting services and wrote declaration.

Jones Day (San Diego, CA and Pittsburgh, PA)

Case – *SOLiD, Inc.* v. CommScope Technologies LLC

Case Numbers – IPR2021-01390, IPR2021-01391, IPR2021-01392, IPR2021-01393, and IPR2021-01394. Petitions filed on August 12, 2021.

Case Subject Matter – Digital antenna system that enables extension of radio frequency (RF) analog signals from base stations to areas (e.g., inside of buildings) where access to such signals is inhibited.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019,015. Request filed on July 20, 2021.

Case Subject Matter – Voltage-controlled oscillator (VCO) temperature compensation.

Work Performed – Provided expert consulting services and wrote declaration.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – *Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC* v. Unification Technologies LLC

Case Numbers – IPR2021-00940, IPR2021-00941, and IPR2021-00942. Petitions filed on June 4, 2021.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Kaijet Technology v. *Sanho Corporation*

Case Number – IPR2021-00886. Petition filed on April 30, 2021.

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services for inter partes review, wrote declaration, was deposed.

O'Melveny & Myers LLP (Los Angeles, CA and New York, NY)

Case – Solas OLED LTD. v. *Samsung Electronics Co. LTD.*

Case Number – Texas, ED (Marshall) 2:21-cv-00105. Complaint filed March 22, 2021.

Case Subject Matter – Touch-sensors for gesture recognition and signal processing for capacitive touch displays.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

O'Melveny & Myers LLP (San Francisco, CA)

Case – Super Interconnect Technologies LLC v. *Google LLC*

Case Number – Texas, ED (Marshall) 2:18-cv-00463 (complaint filed November 2, 2018) and Texas, WD (Waco) 6:21-cv-00259 (complaint filed March 15, 2021).

Case Subject Matter – Transmission of data and clock signals. Serial signals such as transition minimized differential signaling. Communications between processors and non-volatile storage such as Universal Flash Storage (UFS) and embedded MultiMedia Controller (eMMC).

Work Performed – Provided expert consulting services and wrote expert reports.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Fundamental Innovation Systems International LLC v. *Anker Innovations and Fantasia Trading LLC d/b/a Ankerdirect*

Case Number – Delaware, 1:21-cv-00339. Complaint filed on March 5, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – *TCT Mobile Inc. and TCL Communication, Inc.* v. Fundamental Innovation Systems International LLC

Case Numbers – IPR2021-00597, IPR2021-00598, and IPR2021-00599. Petitions filed on February 26, 2021.

Case Number – IPR2021-00428. Petition filed on January 13, 2021.

Case Number – IPR2021-00410. Petition filed on January 11, 2021.

Case Number – IPR2021-00395. Petition filed on December 31, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews. Was deposed twice.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung, Inc.* v. Pictos Technologies, Inc.

Case Number – IPR2021-00557. Petition filed on February 18, 2021.

Case Number – IPR2021-00436. Petition filed on January 19, 2021.

Case Numbers – IPR2021-00437 and IPR2021-00438. Petitions filed on January 15, 2021.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

O'Melveny & Myers LLP (San Francisco, CA) and DLA Piper (New York, NY)

Case – Solas OLED Ltd. v. *BOE Technology Group Co. Ltd. and Samsung Electronics*

Case Number – ITC Investigation No. 337-TA-1243. Complaint filed January 5, 2021.

Case Subject Matter – Active matrix OLED display devices and components

Work Performed – Provided expert consulting services, wrote expert reports, was deposed, and testified at trial.

Paul Hastings LLP (Washington, DC)

Case – *Samsung, Inc.* v. Garrity Power Services LLC

Case Number – IPR2021-00389. Petition filed on December 31, 2020.

Case Subject Matter – Power electronics including full-bridge PWM modules for wireless power transmission using magnetic coupling via antennas and transformers. Design of inductors and coils.

Work Performed – Provided expert consulting services and wrote declaration for inter partes reviews.

Morgan, Lewis & Bockius LLP (Palo Alto, CA and Shanghai, CN)

Case – Monolithic Power Systems, Inc. v. *Meraki Integrated Circuit Technology, Inc. and Promate Electronic Company, LTD.*

Case Number – Texas, WD (Waco) 6:20-cv-00876. Complaint filed on December 24, 2020.

Case Subject Matter – Design of switching power supplies including synchronous rectification.

Work Performed – Provided expert consulting services including declaration for claim construction, trade secret analysis and declaration, and Markman tutorial.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – *Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC; Dell Technologies Inc.; Dell Inc.; and HP Inc.* v. Unification Technologies LLC

Case Numbers – IPR2021-00343, IPR2021-00344, and IPR2021-00345. Petitions filed on December 22, 2020.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews, wrote declarations, and was deposed.

Jones Day (Chicago, IL and Dallas, TX)

Case – WSOU Investments, LLC d/b/a Brazos Licensing and Development v. *Xilinx, Inc.*

Case Numbers – Delaware, 1:20-cv-01231 and Delaware, 1:20-cv-01233. Complaints filed on November 23, 2020 and September 16, 2020.

Case Subject Matter – Controlling power cycles in communication devices and transferring multiple asynchronous clock signals.

Work Performed – Provided expert consulting services, wrote claim construction declaration, wrote expert reports, and was deposed.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Cosemi Technologies, Inc. v. EverPro Technologies, Fibbr Technologies, *Logitech, Inc.*, and Facebook Technologies

Case Number – ITC Investigation No. 337-TA-1233. Complaint filed October 28, 2020.

Case Subject Matter – Data cables, including HDMI, Display Port, and USB Type A, USB Type C and USB Type A/C data cables.

Work Performed – Provided expert consulting services.

Kirkland & Ellis LLP (Boston, MA and New York, NY)

Case – Pictos Technologies, Inc. v. *Samsung Electronics Co., LTD. and Samsung Semiconductor, Inc.*

Case Number – ITC Investigation No. 337-TA-1231. Complaint filed September 25, 2020.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, correction of bad pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote expert report.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Fundamental Innovation Systems International LLC v. *TCT Mobile Inc. and TCL Communication, Inc.*

Case Number – Delaware, 1:20-cv-00552. Complaint filed on September 11, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations, expert report on invalidity, and was deposed.

Walters Wilson LLP (Redwood City, CA)

Case – *Western Digital Corporation and SanDisk, LLC* v. Martin Kuster

Case Numbers – IPR2020-01410 and IPR2020-01411. Petitions filed on August 3, 2020.

Case Subject Matter – Computer connectors such as universal serial bus (USB) that connect to peripheral devices such as mice, keyboards, displays, printers, external storage, etc.

Work Performed – Provided expert consulting services for inter partes review, wrote declarations and was deposed.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – *Advanced Micro Devices, Inc.* v. Monterey Research, LLC

Case Number – IPR2020-01315. Petition filed on July 16, 2020.

Case Number – IPR2020-00985. Petition filed on May 26, 2020.

Case Subject Matter – Reading and writing to semiconductor memory such as SRAM and double data rate (DDR) DRAM. Buffer circuits with variable current supplies for controlling the rise and fall times of output signals.

Work Performed – Provided expert consulting services for inter partes review, wrote declarations and was deposed twice.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Unification Technologies LLC v. *Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC*

Case Number – Texas, WD (Waco) 6:20-cv-00500. Complaint filed June 5, 2020.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, and was deposed.

Ari Law, P.C. (Palo Alto, CA) and Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – *Sanho Corporation* v. Kaijet Technology, Magic Control Technology, and Star View Global

Case Numbers – Georgia, ND (Atlanta) 1:18-cv-05385 (third amended complaint filed November 14, 2019) and Georgia, ND (Atlanta) 1:20-cv-02150 (filed May 19, 2020).

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, and expert reports. Was deposed and testified at trial.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Fundamental Innovation Systems International LLC v. *Coolpad Group Limited, Coolpad Technologies, Inc., and Yulong Computer Telecommunication Scientific Co. Ltd.*

Case Number – Texas, ED (Marshall) 2:20-cv-00117. Complaint filed on April 23, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA and Shanghai, China)

Case – *SMIC, Americas* v. Innovative Foundry Technologies LLC

Case Numbers – IPR2020-00837 and IPR2020-00839. Petitions filed on April 14, 2020.

Case Subject Matter – Methods of manufacturing a semiconductor component, such as a short-channel MOS device, including forming graded-junctions using spacers along the sidewalls of a transistor's gate.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Russ August & Kabat (Los Angeles, CA)

Case – *Oyster Optics, LLC* v. Ciena Corporation

Case Number – California, ND (Oakland) 3:20-cv-02354. Complaint filed on April 7, 2020.

Case Subject Matter – Fiber optic telecommunication systems.

Work Performed – Provided expert consulting services, wrote claim construction declaration, and was deposed.