

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.,

Petitioner,

v.

INTELLECTUAL VENTURES II, LLC,

Patent Owner.

Case No. IPR2024-01226

U.S. Patent No. 7,646,835

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

PATENT OWNER’S EXHIBIT LIST.....	vi
I. INTRODUCTION.....	1
II. THE '835 PATENT.....	2
A. Background	2
B. Detailed Description	2
C. Relevant Prosecution History of the '835 Patent.....	6
III. CHALLENGED CLAIMS OF THE '835 PATENT	7
IV. PRIOR ART RELIED ON IN PETITION.....	8
A. Johnson	8
B. Jeddeloh	12
C. Keeth	15
V. THE PETITION FAILS TO DEMONSTRATE A REASONABLE LIKELIHOOD OF SUCCESS ON THE MERITS	17
A. Ground 1: Claims 1-23 are not obvious over Johnson in view of Jeddeloh	18
1. The proposed combination of Johnson and Jeddeloh does not teach each and every element of the claims.....	18
a. Johnson does not teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...” as required by Claim 1.....	18
1) The motivation to modify Johnson that was provided in the Petition is insufficient.	20
2) The argument in the Petition does not establish that the cited art is “...systematically altering...”	22
3) Johnson, at best, relates to separately “...altering a phase shift...” and not “...systematically altering...”	23
4) The arguments in the Petition do not establish that components of the Johnson are useable for calibration.	23

5) CCLK is not a sampling signal in Johnson, contrary to the argument in the Petition.....	24
b. Jeddeloh does not cure the deficiency in Johnson because Jeddeloh also does not teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...”	25
1) The motivation to combine Johnson and Jeddeloh that was provided in the Petition is insufficient.	25
2) The argument in the Petition does not establish that the cited art is “...systematically altering...”	26
3) Jeddeloh, at best, relates to separately “...altering a phase shift...” and not “...systematically altering...”	29
4) The arguments in the Petition do not establish that components of the Jeddeloh are useable for calibration.	29
B. Ground 2: Johnson In View Of Keeth Does Not Render The Claims Obvious	31
1. The Proposed Combination Of Johnson And Keeth Does Not Teach Each And Every Element Of The Claims	32
a. Johnson does not teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...”	32
b. Keeth does not cure the deficiency in Johnson because Keeth also does not teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...”	32
1) The motivation to combine Johnson and Keeth that was provided in the Petition is insufficient.....	33
2) The Petition does not establish that the cited art is “...systematically altering...”	34
3) Keeth, at best, relates to separately “...altering a phase shift...” and not “...systematically altering...”	35

C.	Ground 3: The Challenged Claims Are Not Obvious Over Johnson In View Of Jeddelloh And In View Of Keeth.....	37
1.	The Proposed Combination Of Johnson, Jeddelloh, And Keeth Does Not Teach Each And Every Element Of The Challenged Claims.	38
a.	Claims 4-6, 9-11, and 13-19 depend from independent claims 1, 7, and 12, respectively.....	38
VI.	SUMMARY OF ARGUMENTS ON THE MERITS	38
VII.	THE BOARD SHOULD EXERCISE ITS DISCRETION AND DENY INSTITUTION UNDER 35 U.S.C. § 325(d), UNDER ADVANCED BIONICS.....	40
A.	Section 325(d) applies because substantially the same art and arguments were presented during prosecution, and the office did not materially err in allowing the challenged claims.	40
B.	Inter Partes Review Should Not Be Instituted For Ground 1, because the Advanced Bionics Framework is met.....	44
1.	Part 1 Of The <i>Advanced Bionics</i> Framework Is Met For Ground 1	44
a.	Johnson	45
b.	Jeddelloh	52
2.	Part 2 Of The <i>Advanced Bionics</i> Framework Is Met For Ground 1	55
C.	Inter Partes Review Should Not Be Instituted For Ground 2, because the Advanced Bionics Framework is met.....	57
1.	Part 1 Of The <i>Advanced Bionics</i> Framework Is Met For Ground 2	57
a.	Johnson	57
b.	Keeth	58
2.	Part 2 Of The <i>Advanced Bionics</i> Framework Is Met For Ground 2	64

A. Inter Partes Review Should Not Be Instituted For Ground 3, because the <i>Advanced Bionics</i> Framework is met.....	65
1. Part 1 Of The <i>Advanced Bionics</i> Framework Is Met For Ground 3	65
2. Part 2 Of The Advanced Bionics Framework Is Met For Ground 3	65
VIII. CONCLUSION	66

PATENT OWNER'S EXHIBIT LIST

EX2001	Declaration of Terry R. Lee
EX2002	Curriculum Vitae of Terry R. Lee
EX2003	A High-Resolution CMOS Time-to Digital Converter Utilizing a Vernier Delay Line (Dudek)
EX2004	U.S. Patent No. 5,781,766 to Davis (“Davis ’766”)
EX2005	U.S. Patent No. 6,016,282 to Keeth (“Keeth ’282”)
EX2006	U.S. Patent No. 6,101,197 to Keeth (“Keeth ’197”)
EX2007	U.S. Patent No. 6,553,472 to Yang (“Yang ’472”)
EX2008	U.S. Patent Publication No. 2002/0078316 (“Nakamura”)
EX2009	U.S. Patent Publication No. 2003/0122696 (“Johnson”)
EX2010	U.S. Patent Publication No. 2003/0231543A1 (“Matsui”)
EX2011	U.S. Patent Publication No. 2004/0160833A1 (“Suzuki”)

I. INTRODUCTION

The Petition for *Inter Partes* Review of U.S. Patent No. 7,646,835 B1 (“Petition,” Paper #2) challenges claims 1-23 (“Challenged Claims”) of U.S. Patent No. 7,646,835 (“’835 Patent,” EX1001) under three statutory grounds. [See Petition, 3]. Claims 1-3, 7-8, and 12 are only challenged under Grounds 1 and 2. Claims 4-6, 9-11, and 13-19 are challenged under Grounds 1, 2, and 3, and claims 20-23 are challenged under Ground 1 only. [See Petition, 3].

The Board should find that Petitioner has failed to demonstrate the unpatentability of the Challenged Claims. The cited references lack at least one limitation of each of the Challenged Claims, and would not have been combined for the reasons alleged in the Petition by a person of ordinary skill in the art. Patent Owner’s explanations herein are supported by the Declaration of Terry E. Lee, an expert in the field. [See EX2001, 2002].

On the issue of discretionary denial, the Petition cites references that are duplicative and/or cumulative of art that was considered by the Office during the prosecution of the ’835 Patent, to raise arguments which are also cumulative of arguments that were made during the prosecution of the ’835 Patent. [See *Infra* §VII and EX1003]. Based on these facts, and as explained more fully below, the *Advanced Bionics* analysis and *Becton Dickenson* factors favor a discretionary denial of the Petition under 35 U.S.C. § 325(d). [See *Infra* §VII].

II. THE '835 PATENT

A. Background

The '835 Patent is focused on the problem of ensuring reliable operation, given narrow specification margins in the design and fabrication of high-performance memory integrated circuit devices (e.g., DDR memory). [See EX1001, 1:14-20]. In the past, slower memory bus speeds allowed significant specification margins in the design and fabrication of a given memory module. [EX1001, 1:20-22]. However, modern memory integrated circuit designs require exacting control of critical timing specifications, and design parameters must be strictly maintained to keep the entire system in balance. [EX1001, 1:22-25]. A stable DDR memory module must provide reliability, speed, and proper timing to [e]nsure the overall system (e.g., CPU, bridge components, peripheral busses, etc.) operates at peak performance. [EX1001, 1:25-29]. “Thus, what is required is a solution that can ensure critical timing specifications remain within certain specified parameters.” [EX1001, 1:29-31].

B. Detailed Description

The '835 Patent discusses embodiments which provide a method and system for automatically calibrating intra-cycle timing relationships among command signals, data signals, and sampling signals for an integrated circuit device. [See EX1001, 2:14-18, 3:3-7. See EX2001 ¶55].

In example embodiments, a command signal corresponds to a command/address bus signal, a data signal corresponds to a data bus (DQ) signal, and a sampling signal corresponds to a sampling signal bus (DQS) signal. [See EX1001, 3:3-7]. Accordingly, example embodiments automatically calibrate intra-cycle timing relationships among signals of the command/address bus, DQ bus, and DQS bus. [See EX1001, 3:3-7. See EX2001, ¶57].

The automatic calibration process adds a significant amount of “extra margin” to the specifications of a memory system. [See EX1001, 3:49-51]. For example, DDR timing specifications are so stringent that even slight variations can have an impact on overall system performance and cause intermittent timing-related DIMM failures. [See EX1001, 3:51-57 See EX2001 ¶56]. The extra margin provided increases the reliability rate of computer systems incorporating such high performance integrated circuit devices, and/or increases the maximum obtainable performance of such computer systems. [See EX1001, 3:58-64].

Further, the variable operating parameters that are automatically calibrated can be efficiently explored (e.g., varied about a specified point of operation) even in cases where no stable initial condition is known. [See EX1001, 3:65-4:3 EX2001 ¶56]. Thus, for example, even if a given printed circuit board (PCB) may not be properly manufactured within specified tolerances, the PCB may still be used because, unlike the prior art, no particular point of stable operation in the

configuration space is required. [See EX1001, 4:5-7. See EX2001 ¶56]. “What is needed is merely that some region of the configuration space (not known *a priori*) be operable.” [EX1001, 4:7-9. See EX2001 ¶57].

Accordingly, embodiments automatically search the configuration space for a device by altering the device parameters (e.g., the phase relationship among command signals, data signals, sampling signals, etc.), to find an operating point (e.g., an optimal operating point) even if the device is inoperable at its supposed specified initial operating point (e.g., at the specified values for the parameters). [See EX1001, 4:13-20. See EX2001 ¶57].

Figure 1 of the '835 Patent illustrates a command/address bus 102 (corresponding to command signals), a data bus (DQ) 103 (corresponding to data signals), and a sampling signal bus (DQS) 104 (corresponding to sampling signals). [See EX1001, 2:63-3:1].

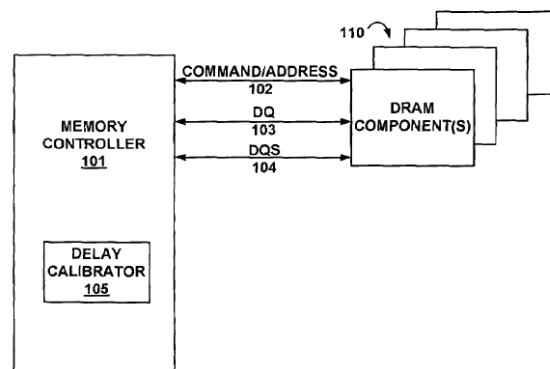


FIGURE 1

Figure 5 of the '835 Patent illustrates a diagram 500 illustrating a typical case where three parameters, x, y, and z, are varied across a range of adjustment to obtain valid windows for a DDR memory. [See EX1001, 5:25-27]. In the case of a DDR DRAM component, for example, the x parameter can correspond to a phase range of command/address signals, the y parameter can correspond to a phase range of DQ signals, and the z parameter can correspond to a phase range of DQS signals. [See EX1001, 5:29-33]. A valid region 520 illustrates a region “...within which the values of the x, y, and z parameters result in the correct operation of the device.” [See EX1001, 5:34-37].

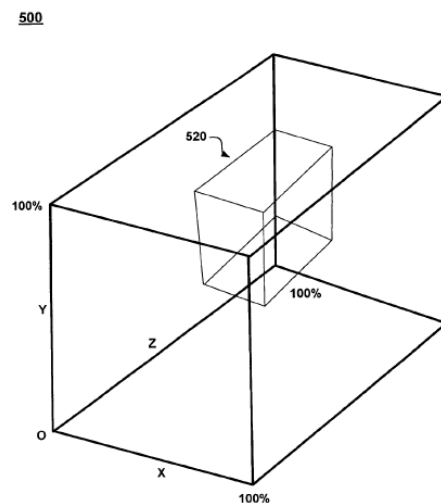


FIGURE 5

The valid region 520 is determined by systematically altering the variable parameters. [See EX1001, 5:53-54]. Each of the parameters (i.e., x, y, and z) can be

varied simultaneously (e.g., it is multi-variate). [See EX1001, 5:61-64]. This can be performed relatively quickly to determine whether any valid region of operation exists for a given device. [See EX1001, 6:7-9].

An additional benefit provided by automatic calibration is that the variable operating parameters of an integrated circuit device can be efficiently explored even in those cases where no stable initial condition is known. [See EX1001, 3:65-4:3]. Unlike the prior art, no particular point of initial stable operation in the configuration space is required. [See EX1001, 4:6-7, and EX2001 ¶56]. “What is needed is merely that some region of the configuration space (not known a-priori) be operable.” [See EX1001, 4:7-9, and EX2001 ¶57].

C. Relevant Prosecution History of the '835 Patent

The '835 Patent is based on U.S. Patent App. No. 10/716,320 (the '320 Application), filed November 17, 2003, and issued on January 12, 2010. [See EX1003, and EX1001]. During the course of examination, the Examiner rejected pending claims over several references. [See EX1003].

For example, in the Office Action of January 8, 2007, the Examiner cited U.S. Patent No. 6,115,318 to Keeth (“Keeth '282”). [See EX1003, 300]. In the Office Action of January 25, 2008, the Examiner cited U.S. Patent Publication No. 2003/0122696 to Johnson (“Johnson '696”). [See EX1003, 216]. In the Reply of March 12, 2009, the claims were amended to reflect the currently challenged claims.

[See EX1003, 89-97]. All of these claims were allowed in the Notice of Allowance dated May 14, 2009, which states that the

“...references do not disclose altering inter-cycle timing relationships between signals by altering a phase shift of command signals, a phase shift of data signals, and a phase shift of sampling signals by altering a phase shift of command signals, a phase shift of data signals, and a phase shift of sampling to determine a valid operation range of an integrated circuit device...”

[See EX1003, 69].

Accordingly, it is clear that during prosecution the Examiner considered the Challenged Claims in view of both Keeth '282 and Johnson '696. [See EX1003, 69, 89-97, 216, 300]. Keeth '282 and Johnson '696 substantially overlap the text of Petitioner's exhibits EX1006 (“Keeth”) and EX1004 (“Johnson,”) and are duplicative of, and/or cumulative of, art cited in the Petition. [See *Infra*, §VII].

III. CHALLENGED CLAIMS OF THE '835 PATENT

Independent Claim 1 is representative of the Challenged Claims, and recites:

1. A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the method comprising:
 - generating command signals to access an integrated circuit component;
 - accessing data signals to convey data for the integrated circuit component;
 - accessing sampling signals to control sampling of the data signals; and
 - systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device,

wherein the valid operation range includes an optimal operation point for the integrated circuit device.

Claim 1 captures the aspects of the disclosed systematic exploration of the configuration space of an integrated circuit device emphasized above. [See Infra §2B] Claim 1 expressly recites systematically altering a phase shift of the command signals, the data signals, and the sampling signals to determine a valid operation range of the integrated circuit device.

IV. PRIOR ART RELIED ON IN PETITION

The Petition advances three grounds, citing three alleged prior art references.

A. Johnson

U.S. Patent No. 6,434,081 to Johnson et al. (Johnson) [EX1004] issued on August 13, 2002, and was based on U.S. Patent Application No. 09/570,481, filed May 12, 2000. [See EX1004, Page 1, and §§(21) and (22)].

Johnson relates to the calibration of a data path relative to a clock signal. [See EX1004, Abstract]. Johnson discusses a “...calibration technique which is useful for calibrating the timing of control and data signals...” [EX1004, 1:6-7]. Johnson discusses “...a timing synchronization of clock signals CCLK (command clock signal) and DCLK (data clock signal) with data provided on an incoming command path (CA) ... (for the CCLK signal) ... and on the data paths DQ (for the DCLK

signal) so that incoming data is correctly sampled...” [EX1004, 1:42-48]. The CCLK, DCLK, CA, and DQ signals of Johnson are illustrated in Fig. 3 of Johnson:

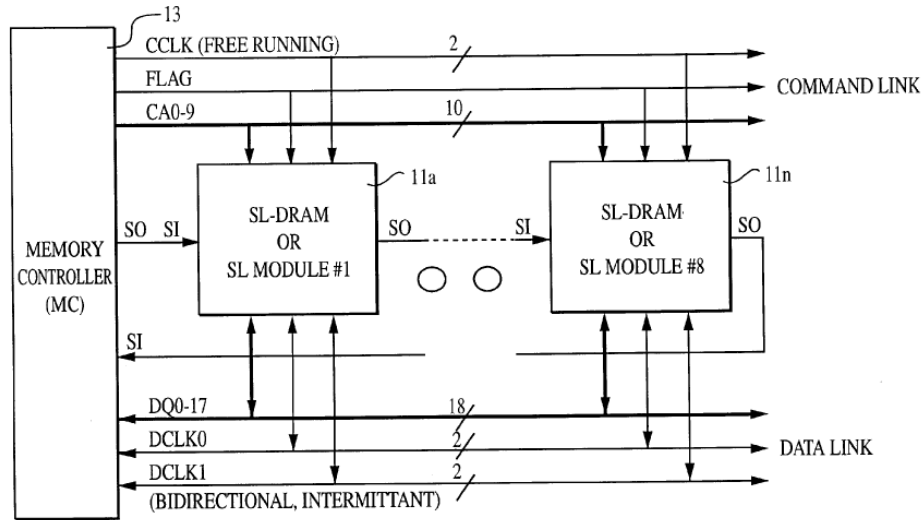


FIG. 3

The CCLK, DCLK, CA, and DQ signals of Johnson are also illustrated in Fig. 4 of Johnson:

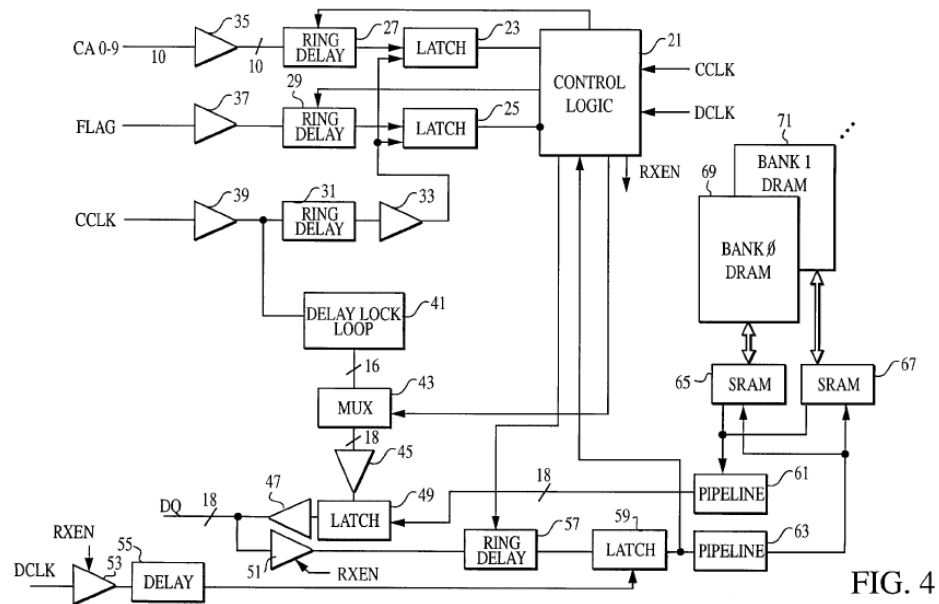


FIG. 4

In order to ensure proper timing of the various memory operations performed by the SDRAM modules 11a...11n, the FIG. 4 circuit must be synchronized to ensure that the incoming data is properly clocked in by the clock signals CCLK and DCLK. [See EX1004, 4:27-31. See EX2001, ¶¶63-65]. A synchronization pattern is applied to each of the data input paths CA0-9 while the synchronization pattern is sampled in latches 23 and 25. [See EX1004, 4:31-35. See EX2001 ¶¶63-65]. “The control logic circuit 21 steps through all possible delay positions of ring delays 27 and 29 as the synchronization pattern sampling is performed and stores patterns representing which delay values for the ring delays 27 and 29 provide for a correct sampling and recognition [of the synchronization pattern].” [See EX1004, 4:36-41]. In this way, Johnson determines delays for aligning CA0-9 with the corresponding clock signal. [See EX1004, 4:41-44. See EX2001 ¶¶63-65].

The same calibration procedure may also be applied to each of the CMD data paths CA0-9 and to each of the data paths of the DQ bus. [See EX1004, 6:7-12]. Johnson recognizes that calibrating all of the CA lines and/or all of the DQ lines in this way will not ensure parallel alignment of data across all incoming paths. [See EX1004, 6:7-12. See EX2001 ¶¶64-65]. Figure 2 of Johnson illustrates this problem:

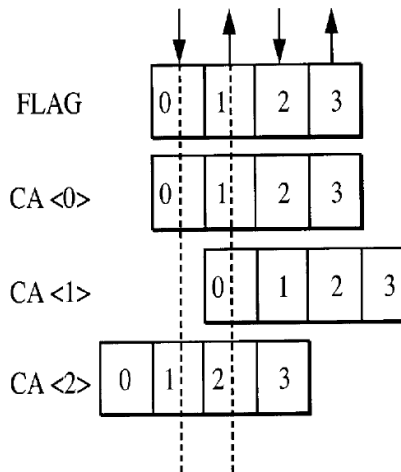


FIG. 2

Johnson addresses this issue by calibrating a first CA line against the corresponding clock signal, and then calibrates the remaining CA lines against a previously calibrated CA line. [See EX1004, 6:34-41]. Similar operations are performed on the DQ lines. [See EX1004, 6:46-48].

In the calibration of CA and DQ, an underlying assumption of Johnson is that the timing of the corresponding CCLK or DCLK signal is correct. [See EX1004, 6:34-41, EX2001 ¶¶64-66]. In other words, CA and DQ are aligned to the CCLK or DCLK signal, or to other CA or DQ signals. [See EX1004, 6:34-48. See, EX2001 ¶100]. In no event are CCLK or DCLK signals aligned with CA or DQ signals in Johnson. [See, EX2001 ¶100]. This is understandable, because Johnson is entirely focused on calibrating of data and control paths in a way that also results in parallel alignment of all of the CA signals and all of the DQ signals, and is unconcerned with calibration of the clock signals, or with determining a valid operating envelope of an

integrated circuit. [See EX1004, Abstract, 2:43-53]. In fact, manipulating the corresponding clock signals would complicate the process envisaged by Johnson, without providing any benefit. [See, EX2001 ¶100].

At best, Johnson adjusts a first parameter (i.e., CA) against a second parameter (i.e., CCLK), and assumes that the second parameter is valid. [See EX1004, 4:41-44. See EX2001 ¶100]. This is entirely unlike the '835 patent, where the phase shift of three different signals are adjusted systematically to determine a valid operation range, without assuming that any are valid initially. [See EX1001, 3:65-4:3, 4:6-9, 5:53-54, 5:61-64, 6:7-9. See EX2001 ¶¶97-101].

B. Jeddeloh

U.S. Patent No. 6,629,222 to Jeddeloh (Jeddeloh) [EX1005] issued on September 30, 2003 and was based on U.S. Patent Application No. 09/352,719, filed July 13, 1999.

Jeddeloh relates to an apparatus that synchronizes a data signal and a data strobe signal received from a random access memory. [EX1005, Abstract. See EX2001 ¶66]. According to Jeddeloh, designing an interface that receives a data strobe signal from a DDR memory during a read operation presents challenges because a certain amount of skew typically arises between the data signal and the data strobe signal. [See EX1005, 1:54-57]. If this skew is large enough, a data strobe edge, which is used to latch the data signal, can move from the center of the “data

eye” of the data signal into a transitional region or into another data eye. [See EX1005, 1:57-61]. This may cause spurious data to be latched during a read operation. [See EX1005, 1:61-62].

Jeddeloh proposes a programmable delay circuit to delay a data strobe signal so as to synchronize the data strobe signal with the data signal. [See EX1005, 2:23-25]. In particular, a data strobe signal is used to clock data into a memory interface, and a delay circuit is configured to delay the data strobe signal so as to synchronize the data strobe signal with the data signal. [See EX1005, 2:17-25]. Jeddeloh also discusses determining delay values by performing test read operations. [See EX1005, 2:31-35]. Figure 3 of Jeddeloh illustrates this arrangement:

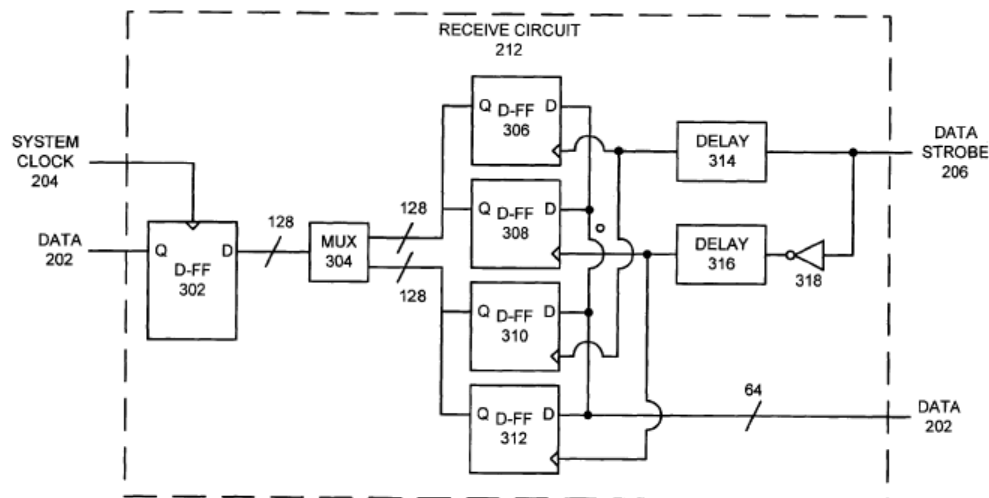


FIG. 3

As shown in Figure 3 of Jeddeloh, data strobe signal 206 passes through delay circuit 314 and also passes through inverter 318 and delay circuit 316. [See EX1005,

5:24-28]. The delay circuits 314 and 316 can be programmed to precisely synchronize data strobe signal 206 with data signal 202. [See EX1005, 5:31-33. See EX2001 ¶68].

In the calibration of the data strobe signal, an underlying assumption of Jeddeloh is that the timing of the corresponding data signal is correct. [See EX1005, and EX2001 ¶68]. In other words, the data strobe signal is aligned to the data signal. In no event are data signals aligned with the data strobe signal in Jeddeloh. [See EX2001 ¶66]. This is understandable, because Jeddeloh is entirely focused on calibrating the data strobe in a way that aligns with the data signals, and is unconcerned with the calibration of the data signal – in fact, as noted above, Jeddeloh expressly contemplates that the delay circuits precisely synchronize data strobe signal with the data signal. [See EX1005, 1:31-33]. Accordingly, manipulating the corresponding data signals would complicate the process envisioned by Jeddeloh, without providing any benefit. [See EX2001 ¶¶82-83, 93].

Jeddeloh, like Johnson, at best, adjusts a first parameter (i.e., data strobe) against a second parameter (i.e., data signal), and assumes that the second parameter is valid. [See EX1005, 1:31-33, EX2001, ¶¶98-99]. As in Johnson, this is entirely unlike the '835 patent, where the phase shift of three different signals are adjusted systematically to determine a valid operation range, without assuming that any are valid initially. [See EX1001, 3:65-4:3, 4:6-9, 5:53-54, 5:61-64, 6:7-9].

C. Keeth

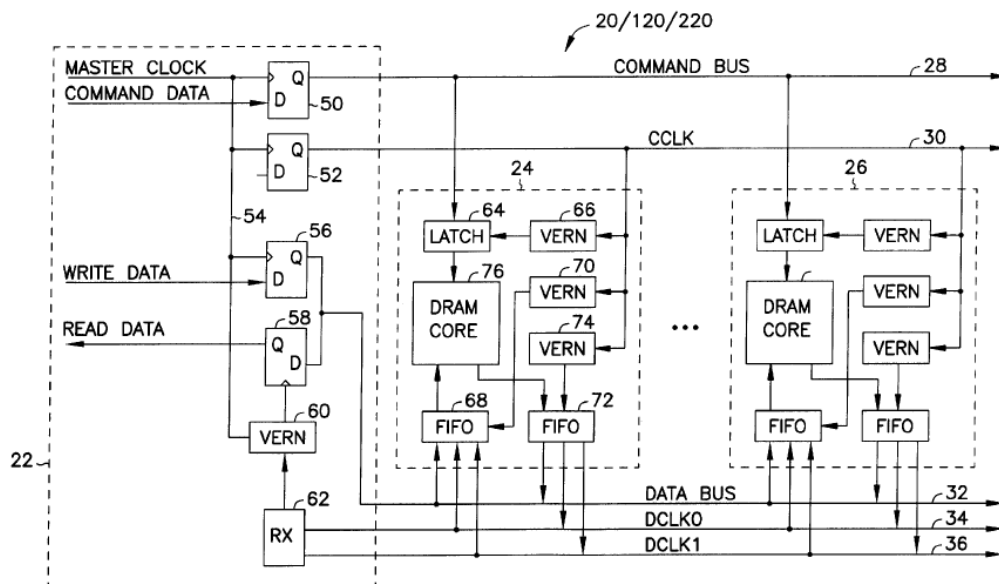
U.S. Patent No. 6,115,318 to Keeth (“Keeth”) [EX1006] issued on September 5, 2000 and was based on U.S. Patent Application No. 08/759,351, filed December 3, 1996.

Keeth relates to a vernier clock adjustment circuit that provides a rising-edge clock signal representing the input signal delayed by a rising-edge delay and a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay. [See EX1006, 1:63-2:1]. According to Keeth, the portion of a clock cycle which can be devoted to clocking valid data becomes quite small, and errors in clocking data can occur at increased transmission speeds because of known effects such as duty cycle variation, bus position of a given memory device, timing drift, loading variations, clock jitter, clock skew, noise, overshoot, and ringing. [See EX1006, 1:43-50].

Keeth proposes that the vernier clock adjustment circuit more accurately and precisely compensates for the effects of duty cycle variation, bus position of a given memory device, timing drift, loading variations, clock jitter, clock skew, noise, overshoot, and ringing by individually adjusting both the rising-edge and falling-edge timings [of the clock signal] either independently or interdependently from each other. [See EX1006, 2:46-53]. According to Keeth, as a result, data is

accurately clocked in the memory devices even at higher data transmission rates.

Figure 7 of Keeth illustrates vernier clock adjustment circuits 60, 66, 70, and 74:



In Keeth, for example, the memory controller sends commands to DRAM, and a CCLK adjustment vernier circuit is adjusted to optimally receive the commands from the command bus. [See EX1006, 8:10-18]. Also, in Keeth, for example, the memory controller sends data to DRAM, and a DCLK adjustment vernier circuit is adjusted to optimally receive the data from the data bus. [See EX1006, 8:18-21].

command signal is correct. [See EX1006, 8:26-32]. In other words, the clock signal is aligned to the data or command signal. [Id]. This is understandable, because Keeth is entirely focused on calibrating individual signals in a way that aligns their rising and falling edges, and is unconcerned with multivariate optimization of several signals. [See EX1006, 1:43-50]. In fact, manipulating corresponding signals (e.g., data and data clock) together would complicate the process envisioned by Keeth, without providing any benefit. [See EX2001 ¶¶134-135].

Keeth, like both Johnson and Jeddeloh, at best adjusts a first parameter (i.e., CCLK) against a second parameter (i.e., data bus), and assumes that the timing of the second parameter is valid. [See EX1006, 8:26-32, and See EX2001 ¶¶134-135] As in both Johnson and Jeddeloh, this is entirely unlike the '835 patent, where the phase shift of three different signals are adjusted systematically to determine a valid operation range, without assuming that any are valid initially. [See EX1001, 3:65-4:3, 4:6-9, 5:53-54, 5:61-64, 6:7-9, and EX2001 ¶¶134-135].

V. THE PETITION FAILS TO DEMONSTRATE A REASONABLE LIKELIHOOD OF SUCCESS ON THE MERITS

The Petition challenges the Challenged Claims under three statutory grounds. See Petition, 3. These grounds are deficient, as described below.

A. Ground 1: Claims 1-23 are not obvious over Johnson in view of Jeddeloh

In Ground 1, the Petition challenges claims 1-23 as obvious over Johnson in view of Jeddeloh. [See Petition §X.A.1.]. This allegation is deficient for several reasons.

First, Johnson does not disclose or teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...” as required by Claim 1. Second, Jeddeloh does not disclose or teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...” as required by Claim 1. The Petition refers to these aspects of Claim 1 as Claim Element 1.4a.

1. The proposed combination of Johnson and Jeddeloh does not teach each and every element of the claims

- a. Johnson does not teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...” as required by Claim 1.**

Petitioner argues, essentially, that Johnson teaches adjusting delays of the CA line, argued to be equivalent to “command signals,” to synchronize with CCLK, argued to be equivalent to “sampling signals.” [See Petition, 17].

Petitioner also argues that Johnson teaches adjusting delays of the DQ line, argued to be equivalent to “data signals,” to synchronize with DCLK, argued to be equivalent to “sampling signals.” [See Petition, 17].

Petitioner argues that Johnson teaches a signal calibration process such that “serial and parallel calibration of all data paths is achieved” and that as a result, timing relationships between all of the command signals, data signals, and sampling signals are calibrated. [See Petition, 19, citing Ex 1004, 4:56-58 and Ex 1002, ¶111]. Patent Owner (“PO”) notes however that the cited portions of Johnson and EX1002 do not in fact support the broad statement that “timing relationships between all of the command signals, data signals, and sampling signals are calibrated”. [Id.] PO notes that both the cited portion of Johnson and EX1002, at best, discuss only alignment of data relative to clock, or command relative to clock, and do not discuss either alignment of clock relative to any other signals, or calibration of “timing relationships between all of the command signals, data signals, and sampling signals.” [Id.]

In fact, Petitioner concedes that Johnson does not teach adjusting delays of CCLK or DCLK to synchronize with anything. [See Petition, 33-34].

Instead, Petitioner argues that the presence of certain delay elements associated with CCLK and DCLK as suggesting that CCLK or DCLK could also be synchronized with CA and DQ respectively, and therefore it would be obvious to do so to provide "additional alignment", thus rendering obvious "...altering a phase shift of ... the sampling signals..." as in claim 1 of the '835 Patent. [See Petition, 33-34].

This argument by Petitioner fails for several reasons.

1) The motivation to modify Johnson that was provided in the Petition is insufficient.

First, the only reasons offered in the Petition to suggest that it would be obvious to modify Johnson in this way is that it is (a) possible, and therefore obvious, or (b) would provide "additional alignment" and therefore would be obvious. [See Petition, 33-34]. However, it is, at best, speculative that adjusting delays of CCLK and DCLK would provide "additional alignment." [See, EX2001, ¶100]. Petitioner provides no explanation for this conclusory statement, nothing in the cited references suggests this, and since Johnson already aligns CA and DQ with CLK and DLK, in the context of simply aligning signals, which is offered as the motivation for modifying Johnson in this way, it would be a duplication of effort to adjust CCLK to align with CA when CA has already been adjusted to align with CCLK. [See Petition, 33-34, EX1004, 4:31-35, 6:34-48, See, EX2001, ¶100]. The argument in the Petition, and supporting testimony in Petitioner's Expert Report as to the

modification of Johnson to also adjust delays of CCLK and DCLK are mere conclusory statements and do not even attempt to answer the lingering question as to why this would be obvious.

In *Facebook v. Windy City Innovations, LLC*, the Court affirmed the Board's holding that independent claim 1 was not unpatentable as obvious over the asserted prior art when "the Board considered Facebook's expert's testimony but determined that it did not add materially to Petitioner's unpersuasive attorney argument," because it merely repeated Petitioner's argument, nearly verbatim, without citation to the basis for his testimony." 973 F.3d 1321, 1340-41 (Fed. Cir. 2020). In fact, the Federal Circuit expressly held that "conclusory expert testimony and attorney argument cannot constitute substantial evidence." *Acoustic Tech., Inc. v. Itron Networked Sols., Inc.*, 949 F.3d 1366, 1375 (Fed. Cir. 2020).

Here, Petitioner's expert, like in *Facebook* and *Acoustic Tech*, has only offered conclusory, unsupported statements that mirror the attorney argument in the Peition. Accordingly, the testimony in Petitioner's expert report should be given little, if any, weight. And since Petitioner's expert report is the only evidence submitted for the obviousness of modifying Johnson to adjust delays of CCLK and DCLK, this Petition should not be instituted.

2) The argument in the Petition does not establish that the cited art is “...systematically altering...”

Second, the adjustment of CA to synchronize with CCLK is independent of the adjustment of DQ to synchronize with DCLK, and is not "...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device..." as in Claim 1 of the '835 Patent. [See EX1004, 4:31-35, 6:34-48 See, EX2001 ¶101]. This aspect of claim 1 is illustrated by Fig. 5 of the '835 Patent, where three variables are explored to determine whether a single range made up of valid combinations of the three variables exist. [See EX1001, Fig. 5, 5:53-64, 6:7-9, See, EX2001 ¶¶59-60].

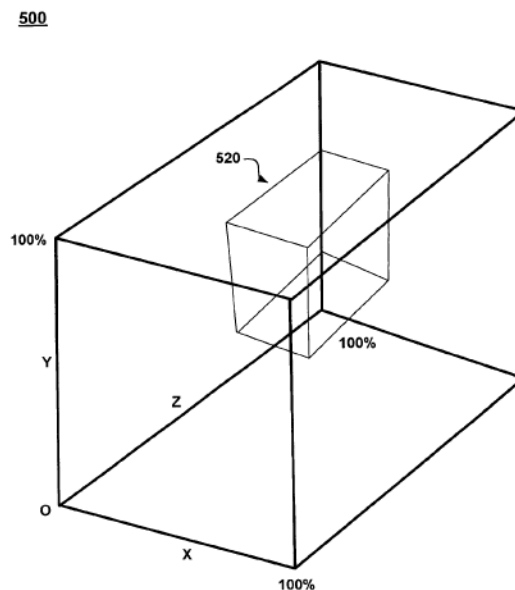


FIGURE 5

Such systematic adjustment, and the proffered motivation of providing "additional alignment," is entirely beside the point for the goal of Johnson, which is to determine separate valid delays for CA against CCLK, and for DQ against DCLK, respectively. [See EX1004, Abstract, 2:43-52. See, EX2001 ¶101].

**3) Johnson, at best, relates to separately
“...altering a phase shift...” and not
“...systematically altering...”**

Third, this is also true even if it were assumed for the sake of argument that it would be obvious to synchronize CLK with CA and DCLK with DQ. [See EX1004, Abstract, 2:43-52. See, EX2001 ¶101]. At best, this would yield separately "...altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals..." but would still not yield "...systematically altering..." the multiple phase shifts "...to determine a valid operation range of the integrated circuit device...", at least because Johnson neither determines a single valid operation range based on systematic exploration of all three variables, nor was it argued to do so. [See EX1004, Abstract, 2:43-52, 6:7-12; and EX2001 ¶101]. At best, Johnson determines two separate valid operation ranges, each based on fewer than the three variables. No single valid operation range is based on the three variables. [See EX1004, 6:34-41, 46-48; and EX2001 ¶101]

**4) The arguments in the Petition do not establish
that components of the Johnson are useable for
calibration.**

Fourth, The Petition draws a false equivalence between delay 55 and DLL 41 on the one hand, and the ring delays that are adjusted in the calibration of CA and DQ to argue that. [See Petition, 30-33 ¶1]. The ring delays are specifically described in Johnson as being used for the calibration process, whereas delay 55 and DLL 41 are neither described as ring delays nor as being used for a calibration process in Johnson. [See EX1004, 6:34-41, 46-48; and EX2001 ¶108].

**5) CCLK is not a sampling signal in Johnson,
contrary to the argument in the Petition**

Fifth, it is of note that CCLK is not a sampling signal, based on the specification of Johnson and The Petition's own arguments. [See EX2001, ¶64]. Even if it were assumed for the sake of argument that the DQ of Johnson corresponds to data signals, only DCLK would be sampling signals. [See EX2001, ¶65]. There is no alignment of CA with DCLK, and accordingly, no equivalence to "...systematically altering ... the command signals, and ... the sampling signals..." [See EX2001, ¶65]. Johnson relates essentially to data capture against a timing reference. [See EX2001, ¶64-65]. There is no discussion of or motivation to align commands to DQ or DQS. [See EX2001, ¶64-65].

- b. Jeddeloh does not cure the deficiency in Johnson because Jeddeloh also does not teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...”**

As discussed above, the Petition essentially concedes that Johnson does not disclose adjusting delays of CCLK or DCLK to synchronize with anything. [See Supra §V.A.1.a.]. The Petition argues that even if Johnson does not teach this element, Jeddeloh teaches this element. [See Petition, 34-35]. The Petition argues that Jeddeloh teaches synchronizing a data strobe signal with a data signal received from random access memory, using a programmable delay circuit. [See Petition, 35-36]. This suffers from the same deficiency as Johnson. In addition, the proposed combination suffers from the following shortcomings.

1) The motivation to combine Johnson and Jeddeloh that was provided in the Petition is insufficient.

First, the only reasons offered to suggest that it would be obvious to modify Johnson in this way is that it is (a) possible, and therefore obvious, or (b) would provide "additional alignment" and therefore would be obvious. [See Petition, 36].

However, it is, at best, speculative that adjusting delays of CCLK and DCLK would provide "additional alignment." [See, EX2001, ¶100]. The Petition provides

no explanation for this conclusory statement; nothing in the cited references suggests this, and since Johnson already aligns CA and DQ with CLK and DLK, in the context of simply aligning signals, which is offered as the motivation for modifying Johnson in this way, it would be a duplication of effort to adjust CCLK to align with CA when CA has already been adjusted to align with CCLK. [See EX1004, 4:31-35, 6:34-48. See, EX2001 ¶100].

The argument in the Petition and supporting testimony in Petitioner's Expert Report as to the modification of Johnson to also adjust delays of CCLK and DCLK are mere conclusory statements and do not even attempt to answer the lingering question as to why this would be obvious. As discussed above, conclusory expert testimony and unsupported attorney arguments cannot qualify as substantial evidence, as reaffirmed in *Acoustic Tech* and *Facebook*. Accordingly, the testimony in Petitioner's expert report should be given little, if any, weight. And since Petitioner's expert report is the only evidence submitted for the obviousness of modifying Johnson to adjust delays of CCLK and DCLK, this Petition should not be instituted.

2) The argument in the Petition does not establish that the cited art is "...systematically altering..."

Second, the adjustment of CA to synchronize with CCLK is independent of the adjustment of DQ to synchronize with DCLK, and is not "...systematically

altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device..." as in Claim 1 of the '835 Patent. [See EX1004, 4:31-35, 6:34-48; and EX2001 ¶¶100-101]. This aspect of Claim 1 is illustrated by Fig. 5 of the '835 Patent, where three variables are explored to determine whether a single range made up of valid combinations of the three variables exist. [See EX1001, Fig. 5, 5:53-64, 6:7-9; and EX2001 ¶101]. Such systematic adjustment is entirely beside the point for the goal of Johnson, and the proffered motivation of providing "additional alignment," which is to determine separate valid delays for CA against CCLK, and for DQ against DCLK, respectively. [See EX1004, Abstract, 2:43-52; and EX2001 ¶101].

Additionally, in *In re Ratti*, the Court held that a combination of references is improper if it renders the combined references inoperable for their intended purpose. 270 F.2d 810, 813, 47 C.C.P.A. 1059 (1959)). The Federal Circuit emphasized that a modification leading to an incompatible or inoperative result fails to support a finding of obviousness. In *In re Ratti*, the combination of prior art references would have required substantial alterations that changed the fundamental operation of the devices involved, thus making the combination non-functional. Similarly, the United States Patent and Trademark Office, Manual of Patent Examining Procedure

(MPEP)¹ explains that *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984) held that “[i]f a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.” (MPEP §2143.01). Accordingly, as explained in *In re Ratti* and *In re Gordon*, a proposed combination of references is improper under 35 U.S.C. §103 when the combination would render the references inoperable for their intended purpose.

The Petitioner’s proposed combination of Johnson and Jeddeloh would lead to a device that is not operable for its intended purpose. [See, EX2001 ¶¶100-101]. Since Johnson already aligns CA and DQ with CLK and DCLK, Petitioner’s proposed combination whereby CLK and DCLK are aligned with CA and DQ would interfere with the determination of separate valid delays for CA against CCLK, and for DQ against DCLK, respectively, since CA has already been adjusted to align with CCLK, and DQ has already been aligned with DCLK. [See, EX2001 ¶¶100-101].

¹ “The MPEP has no binding force ... but is entitled to notice so far as it is an official interpretation of statutes or regulations with which it is not in conflict.” *Litton Sys. v. Whirlpool Corp.*, 728 F.2d 1423, 1439 (Fed. Cir. 1984).

**3) Jeddeloh, at best, relates to separately
“...altering a phase shift...” and not
“...systematically altering...”**

Third, even if it were assumed for the sake of argument that it would be obvious to synchronize CLK with CA and DCLK with DQ in Johnson based on the programmable delay of the data strobe in Jeddeloh – at best, this would yield separately "...altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals..." but would still not yield "...systematically altering..." the multiple phase shifts "...to determine a valid operation range of the integrated circuit device...", at least because Johnson neither determines a single valid operation range based on a systematic exploration of all three variables, nor was it argued to do so. [See EX1004, Abstract, 2:43-52, 6:7-12, See, EX2001 ¶¶100-101]. At best, Johnson determines two separate valid operation ranges, each based on fewer than the three variables. No single valid operation range is based on the three variables. [See EX1004, 6:34-41, 46-48 See, EX2001 ¶¶100-101].

**4) The arguments in the Petition do not establish
that components of the Jeddeloh are useable for
calibration.**

Fourth, it is notable that the delay elements 314, 316 of Jeddeloh apply only to the data strobe 206, and not to the data signal 202. [See EX1004, Fig. 3]. To the extent that it was argued that a combination of Jeddeloh with Johnson would yield

“...systematically altering...” Jeddeloh lacks the basic hardware to accomplish this. Accordingly, the only reason POSITA would combine Johnson and Jeddeloh would be impermissible hindsight. In this case, there is no reason aside from the specification of the '835 Patent itself, which is impermissible hindsight. (*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007); *In re Kotzab*, 217 F.3d 1365, 1369 (Fed. Cir. 2000) (holding hindsight is impermissible in an obviousness analysis, as the determination must be based on the perspective of a person of ordinary skill in the art at the time of the invention, without using knowledge gleaned from the invention itself (*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007)))). Further, as explained by the Federal Circuit, “[t]o satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements.” *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Instead, the Petitioner has the burden to submit facts to the record that show “[w]hether the prior art discloses a claim limitation, whether a skilled artisan would have been motivated to modify or combine teachings in the prior art, and whether she would have had a reasonable expectation of success in doing so.” *Univ. of Strathclyde v. Clear-Vu Lighting LLC*, 17 F.4th 155, 160 (Fed. Cir. 2021). If the petition does not clearly demonstrate how the cited prior art meets each claim element, the Petitioner will fail to meet its burden.

Accordingly, the delay elements in Jeddeloh apply only to the data strobe, not the data signal, making it incapable of achieving the systematic alterations suggested

in combination with Johnson. Any rationale for combining Jeddeloh and Johnson relies solely on impermissible hindsight, as there is no evidence aside from the specification of the '835 Patent itself to support the combination. Additionally, the Federal Circuit requires a petitioner to provide more than conclusory statements, demonstrating with facts how the prior art discloses claim limitations, a motivation to combine, and a reasonable expectation of success, as emphasized in *In re Magnum Oil Tools Int'l, Ltd.* and *Univ. of Strathclyde v. Clear-Vu Lighting LLC*. Petitioner's failure to provide this detailed analysis means the Petitioner has failed meet its burden to prove obviousness under 35 U.S.C §103.

B. Ground 2: Johnson In View Of Keeth Does Not Render The Claims Obvious

In Ground 2, the Petition challenges the claims 1-3, 7-8, and 12 as obvious over Johnson in view of Keeth. [See Petition §X.B.1]. This allegation is deficient for several reasons.

First, Johnson does not disclose or teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...” as required by Claim 1. Second, Keeth does not disclose or teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...” as required by Claim 1.

1. The Proposed Combination Of Johnson And Keeth Does Not Teach Each And Every Element Of The Claims

- a. Johnson does not teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...”**

Johnson does not teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...” as discussed above regarding Ground 1. [See supra §V.A.1.a.]

- b. Keeth does not cure the deficiency in Johnson because Keeth also does not teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...”**

As mentioned regarding Ground 1, The Petition essentially concedes that Johnson does not disclose adjusting delays of CCLK or DCLK to synchronize with anything. [See Supra §V.A.1.a]. With respect to claim 1, Ground 2 repeats all arguments with respect to Johnson, except to argue that if Johnson does not teach “...systematically altering a phase shift of the sampling signals...” then Keeth teaches this element. [See Petition, 74-81]. In particular, the Petition points to the individual adjustment of rising and falling edge timings of DCLK signals, as discussed in Keeth,

as teaching this element. [Id]. The Petition argues that the manner of adjusting the Vernier delays amounts to "...systematically altering..." based on a dictionary definition of the word systematic. [See Petition, 79-80]. This fails for several reasons.

1) The motivation to combine Johnson and Keeth that was provided in the Petition is insufficient.

First, the only reasons offered to suggest that it would be obvious to modify Johnson in this way is that it is (a) possible, and therefore obvious, or (b) would correct alignment of signals in a memory device, and therefore would be obvious. [See Petition, 80-81].

However, it is, at best, speculative that adjusting delays of CCLK and DCLK would provide additional alignment. [See EX2001, ¶¶127, 133-135]. The Petition provides no explanation for this conclusory statement, nothing in the cited references suggests this, and since Johnson already aligns CA and DQ with CLK and DLK, in the context of simply aligning signals, which is offered as the motivation for modifying Johnson in this way, it would be a duplication of effort to adjust CCLK to align with CA when CA has already been adjusted to align with CCLK. [See Id.].

The argument in the Petition, and supporting testimony in Petitioner's Expert Report as to the modification of Johnson based on Keeth to also adjust delays of CCLK and DCLK are mere conclusory statements and do not even attempt to answer the lingering question as to why this would be obvious. As discussed above, in *Facebook*, the Federal Circuit held that conclusory expert testimony merely echoing

attorney arguments without substantive support cannot constitute substantial evidence for proving obviousness. Here, Petitioner's argument exclusively relies upon the Petitioner's conclusory statements that directly mirror the Petition without any additional support.

Accordingly, the testimony in Petitioner's expert report should be given little, if any, weight. And since Petitioner's expert report is the only evidence submitted for the obviousness to modify Johnson to also adjust delays of CCLK and DCLK, this Petition should not be instituted.

2) The Petition does not establish that the cited art is "...systematically altering..."

Second, the adjustment of CA to synchronize with CCLK is independent of the adjustment of DQ to synchronize with DCLK, and is not "...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device..." as in Claim 1 of the '835 Patent. [See EX2001, ¶¶127-135]. This aspect of claim 1 is illustrated by Fig. 5 of the '835 Patent, where three variables are explored to determine whether a single range made up of valid combinations of the three variables exist. [See EX1001, Fig. 5, 5:53-64, 6:7-9, ¶¶127-135]. Such systematic adjustment is entirely beside the point for the goal of Johnson, and the proffered motivation of providing "additional alignment," which is to separately determine separate valid delays for CA against CCLK, and for DQ

against DCLK, respectively. [See EX1004, Abstract, 2:43-52; and EX2001, ¶¶127-135].

The Federal Circuit has consistently held that a combination of prior art references is improper under 35 U.S.C. § 103 if it renders the combined references inoperable or fundamentally alters their intended purpose. (see *In re Ratti* and *In re Gordon*). Here, the Petitioner's proposed combination is improper because the Petitioner's proposed combination of Johnson and Keeth would lead to a device that is not operable for its intended purpose. [See EX2001, ¶¶127, 133-135]. Since Johnson already aligns CA and DQ with CLK and DCLK, Petitioner's proposed combination whereby CLK and DCLK are aligned with CA and DQ would interfere with the determination of separate valid delays for CA against CCLK, and for DQ against DCLK, respectively, since CA has already been adjusted to align with CCLK, and DQ has already been aligned with DCLK. [See *Id.*].

3) Keeth, at best, relates to separately "...altering a phase shift..." and not "...systematically altering..."

Third, this is also true even if it were assumed for the sake of argument that it would be obvious to synchronize CLK with CA and DCLK with DQ in Johnson based on the vernier adjustment of CCLK and DCLK in Keeth – at best, this would yield separately "...altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals..." but would still not yield

"...systematically altering..." the multiple phase shifts "...to determine a valid operation range of the integrated circuit device...", at least because Johnson neither determines a single valid operation range based on systematic exploration of all three variables, nor was it argued to do so. [See EX2001, ¶¶127, 133-135]. At best, Johnson determines two separate valid operation ranges, each based on fewer than the three variables. No single valid operation range is based on the three variables. See EX1004, 6:34-41, 46-48; and EX2001, ¶¶127, 133-135].

Accordingly, the only reason POSITA would combine Johnson and Keeth would be impermissible hindsight. In this case, there is no reason aside from the specification of the '835 Patent itself, which is impermissible hindsight. (*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007); *In re Kotzab*, 217 F.3d 1365, 1369 (Fed. Cir. 2000) (holding hindsight is impermissible in an obviousness analysis, as the determination must be based on the perspective of a person of ordinary skill in the art at the time of the invention, without using knowledge gleaned from the invention itself (*In re Kotzab*, 217 F.3d 1365, 1369 (Fed. Cir. 2000)))). Further, as explained by the Federal Circuit, "[t]o satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Instead, the Petitioner has the burden to submit facts to the record that show "[w]hether the prior art discloses a claim limitation, whether a skilled artisan would have been motivated to modify or

combine teachings in the prior art, and whether she would have had a reasonable expectation of success in doing so.” *Univ. of Strathclyde v. Clear-Vu Lighting LLC*, 17 F.4th 155, 160 (Fed. Cir. 2021). If the petition does not clearly demonstrate how the cited prior art meets each claim element, the Petitioner will fail to meet its burden.

C. Ground 3: The Challenged Claims Are Not Obvious Over Johnson In View Of Jeddeloh And In View Of Keeth

In Ground 3, the Petition challenges claims 4-6, 9-11, and 13-19 as obvious over Johnson in view of Jeddeloh and in view of Keeth. [See Petition §X.C.1]. This allegation is deficient for several reasons.

First, Johnson does not disclose or teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...” as required by claim 1, and discussed above regarding Ground 1. [See *supra*, §V.A.1.a].

Second, Jeddeloh does not disclose or teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device...” as required by claim 1, and discussed above regarding Ground 1. [See *supra*, §V.A.1.b].

Third, Keeth does not disclose or teach “...systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the

sampling signals to determine a valid operation range of the integrated circuit device...” as required by claim 1, and discussed above regarding Ground 2. [See supra, §V.B.1.b].

1. The Proposed Combination Of Johnson, Jeddeloh, And Keeth Does Not Teach Each And Every Element Of The Challenged Claims.

a. Claims 4-6, 9-11, and 13-19 depend from independent claims 1, 7, and 12, respectively.

Claims 4-6, 9-11, and 13-19 depend from independent claims 1, 7, and 12 respectively, which are valid as discussed above. [See Supra, §§V.A. and V.B.] Thus, Ground 3 suffers from the same deficiencies as Ground 1 and Ground 2. Id.

VI. SUMMARY OF ARGUMENTS ON THE MERITS

With respect to Ground 1, for the reasons explained above, the Petition has failed to demonstrate a reasonable likelihood of success of establishing that independent claims 1, 7, 12, 20 and 23 are unpatentable. [See Supra, §V.A.]. With respect to the other claims challenged in Ground 1 (i.e., dependent claims 2-6, 8-11, 13-19, and 21-22), the Petition has failed to demonstrate a reasonable likelihood of success of establishing the unpatentability of these dependent claims, because the Petition has failed to demonstrate a reasonable likelihood of success of establishing that the independent claims (i.e., claims 1, 7, 12, 20 and 23) from which these dependent claims depend are unpatentable. [See Supra, §V.A.].

Similarly, with respect to Ground 2, for the reasons explained above, the Petition has failed to demonstrate a reasonable likelihood of success of establishing that independent claims 1, 7, and 12 are unpatentable. [See Supra, §V.B.]. With respect to the other claims challenged in Ground 1 (i.e., dependent claims 2-3 and 8), the Petition has failed to demonstrate a reasonable likelihood of success of establishing the unpatentability of these dependent claims, because the Petition has failed to demonstrate a reasonable likelihood of success of establishing that the independent claims (i.e., claims 1, 7, and 12) from which these dependent claims depend are unpatentable. [See Supra, §V.B.].

Further, with respect to Ground 3, for the reasons explained above, the Petition has failed to demonstrate a reasonable likelihood of success of establishing that dependent claims 4-6, 9-11, and 13-19 are unpatentable. [See Supra, §V.C.]. The Petition has failed to demonstrate a reasonable likelihood of success of establishing the unpatentability of these dependent claims, because the Petition has failed to demonstrate a reasonable likelihood of success of establishing that the corresponding independent claims (i.e., claims 1, 7, and 12) from which these dependent claims depend are unpatentable. [See Supra, §V.C.].

VII. THE BOARD SHOULD EXERCISE ITS DISCRETION AND DENY INSTITUTION UNDER 35 U.S.C. § 325(d), UNDER ADVANCED BIONICS

A. Section 325(d) applies because substantially the same art and arguments were presented during prosecution, and the office did not materially err in allowing the challenged claims.

The Board should exercise its discretion under 35 U.S.C. § 325(d) to deny institution of inter partes review of the challenged claims of the '835 Patent because the prior art and arguments presented in the Petition are substantially the same as those previously considered by the USPTO during prosecution. Specifically, the primary reference (Johnson '696) and a secondary reference (Keeth '318) were directly cited and evaluated by the Office, and the additional reference (Jeddeloh) is merely cumulative. The Petitioner has failed to demonstrate any material error in the USPTO's prior consideration of these references, as required under the *Advanced Bionics* two-part framework, which directs the Board to defer to prior Office evaluations unless material error is shown. Applying the precedential *Becton Dickinson* factors, it is clear that the asserted art overlaps significantly with prior art evaluated during prosecution, the arguments are cumulative, and there is no compelling reason to revisit the USPTO's conclusions. Thus, each factor strongly supports denying institution in this case.

A patent (Johnson '696) corresponding to the primary reference relied upon for Grounds 1, 2 and 3 of the Petition (Johnson), was cited during prosecution of the

'835 Patent. [See supra, §II.C.]. Moreover, Johnson '696 was directly cited in an Office Action and considered by the USPTO during prosecution of the '835 Patent. [See EX1003, 222].

Further, a patent (Keeth '318) corresponding to a secondary reference relied upon for Grounds 2 and 3 of the Petition (Keeth) was cited during prosecution of the '835 Patent. [See supra, §II.C.]. Moreover, Keeth '318 was directly cited in an Office Action and considered by the USPTO during prosecution of the '835 Patent. [See supra, §II.C.].

The other prior art relied upon in the Petition (Jeddeloh) is merely cumulative, at least with Keeth '318, which was considered by the Office during prosecution of the '835 Patent. [See Supra, §II.C.].

Finally, the Petitioner does not point out any material error in the USPTO's previous consideration of Johnson '696, and does not adequately point out any material error in the USPTO's previous consideration of Keeth '318. [See Infra, §§VII.B.2. and VII.C.2].

Under 35 U.S.C. § 325(d), the Board has discretion to deny institution because the same or substantially the same prior art or arguments were previously presented to the Office. *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GMBH*, IPR2019-01469, Paper 6 at 7-9 (PTAB Feb. 13, 2020) (precedential) ("*Advanced Bionics*"). In *Advanced Bionics*, the Board applied a two-part framework in

considering whether to exercise discretion to deny institution under § 325(d): “(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics*, IPR2019-01469, Paper 6 at 8.

Within this two-part framework, the Board considers a number of non-exclusive factors in evaluating whether to exercise its discretion under § 325(d). *See Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, first para.); see also *Advanced Bionics*, Paper 6 at 9–11. The precedential section of *Becton, Dickinson* sets forth the following non-exclusive factors (“BD Factors”) for consideration:

- (a) The similarities and material differences between the asserted art and the prior art involved during examination;
- (b) The cumulative nature of the asserted art and the prior art evaluated during examination;
- (c) The extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection
- (d) The extent of overlap between the arguments made during examination and the manner in which petitioner relies on the prior art;

- (e) Whether petitioner has pointed out sufficiently how the examiner erred in its evaluation of the asserted prior art; and
- (f) The extent to which additional evidence and facts presented in the petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson, IPR2017-01586, Paper 8 at 17-18.

BD Factors (a), (b) and (d) can be applied broadly to determine whether “substantially the same art” or the “same or substantially the same arguments previously were presented to the Office” under Part 1 of the two-part *Advanced Bionics* framework (“*Advanced Bionics Part 1*”). *Advanced Bionics*, Paper 7 at 1820. If it is determined that *Advanced Bionics* Part 1 is met, *Becton Dickinson* Factors (c), (e), and (f) can be applied broadly to determine whether “petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims” under Part 2 of the two-part *Advanced Bionics* framework (“*Advanced Bionics Part 2*”) is met. *Id.* Here, each factor weighs in favor of denying institution. “At bottom, this framework reflects a commitment to defer to previous Office evaluations of the evidence of record unless material error is shown.” [*Id.*, 9].

As a result, the Board should exercise its discretion under 35 U.S.C. § 325(d) to deny institution of inter partes review of the challenged claims of the ‘835 Patent. The prior art references and arguments relied upon in the Petition are substantially identical to those already considered and rejected by the USPTO during prosecution. Under the *Advanced Bionics* framework and the *Becton Dickinson* factors, the

Petitioner has failed to establish any material error in the Office’s prior evaluation of Johnson ’696, Keeth ’318, or the cumulative nature of Jeddeloh. The lack of new evidence or compelling reasoning to revisit these prior determinations supports deferring to the USPTO's original conclusions, ensuring that the integrity and efficiency of the patent examination process are upheld. Accordingly, the Petition does not warrant institution of review.

B. Inter Partes Review Should Not Be Instituted For Ground 1, because the Advanced Bionics Framework is met.

Ground 1 of the Petition alleges that Claims 1-14 of the ’835 Patent are obvious over Johnson in combination with Jeddeloh. [See Petition §X.A.1.]

1. Part 1 Of The *Advanced Bionics* Framework Is Met For Ground 1

To satisfy *Advanced Bionics* Part 1, the Patent Owner needs only to show that the Petition cites references that were substantially the same as references previously presented to the United States Patent and Trademark Office (USPTO). *See Advanced Bionics*, Paper 7 at 21; *see also Weatherford U.S., L.P. v. Eventure Global Technology, Inc.*, IPR2020-01661, Paper 15, at 23 (PTAB Apr. 15, 2021) (“*Weatherford*”).

With respect the issue of whether “the same or substantially the same” art or arguments were previously presented to the Office during prosecution of the Challenged Claims, Regarding Johnson and Jeddeloh, the Petition makes an

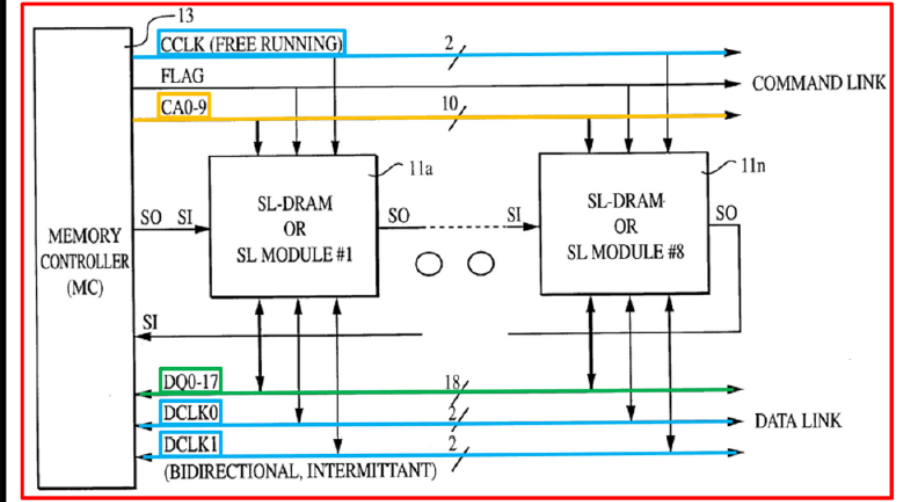
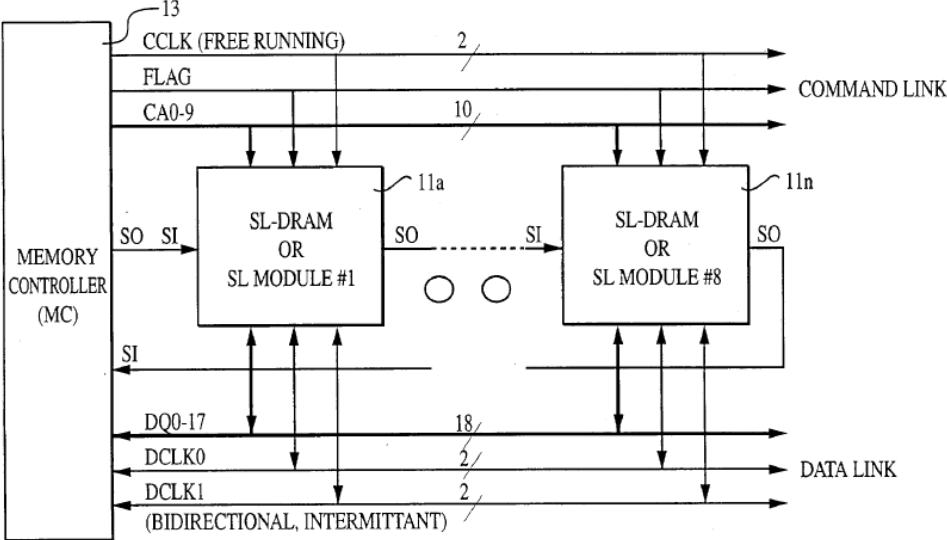
incorrect, omnibus statement that “Johnson [and] Jeddeloh ... are ... not substantially the same or cumulative of references considered during examination. [See Petition, 86].

PO respectfully notes however that both Johnson and Jeddeloh are indeed duplicative and/or cumulative of references considered by the Office during prosecution of the 835 Patent, as follows.

a. Johnson

In Ground 1, Johnson was the primary reference cited as rendering Claims 1-14 of the '835 Patent obvious. However, Johnson '696 was cited by the Office and considered during prosecution of the '835 Patent. [See Supra, §II.C.]. Johnson '696 substantially overlaps with both the text and figures of Johnson, and accordingly is both duplicative, and cumulative, of art cited in the Petition.

For example, Figure 3 of Johnson and its detailed description are heavily cited in the Petition, which includes an annotated version of Figure 3 that “illustrates the relevant signals.” [See Petition, 17-18]. Figure 3 of *Johnson and its detailed description are identical to Figure 1 of Johnson '696 and its detailed description*, as shown in the tables below.

Johnson (as annotated by Petitioner)	"A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device"  FIG. 3
Johnson '686	 FIG. 1

Johnson	Johnson '686
[EX1004, 3:30-47] An SLDRAM system with which the present invention may be used is illustrated in FIG. 3. It includes a	[EX2009, ¶[0023]] An exemplary SLDRAM system which may employ the invention is illustrated in FIG. 1. It includes a plurality of

plurality of SDRAM modules 11 a . . . 11 n which are accessed and controlled by a memory controller 13. Memory controller 13 provides a command link to each of the SDRAM modules 11 a . . . 11 n which includes a clock signal CCLK on inverted and non-inverted clock signal paths, a 1 bit FLAG signal on a FLAG data path, and a 10 bit command bus data path CA0-9. In addition, SDRAM input/output enabling signals SO, SI are provided from memory controller 13 in daisy chain fashion to the SDRAM modules 11 a . . . 11 n. In addition, a bi-directional data bus DQO-17 is provided between memory controller 13 and each of the SDRAM modules 11 a . . . 11 n, as are bi-directional data clocks DCLKO and DCLKI. The clock DCLKO is used to strobe input/output data into and out of the SDRAM modules, a process for which the DCLKI signal path is also intermittently used.	SDRAM modules 11 a . . . 11 n which are accessed and controlled by a memory controller 13. Memory controller 13 provides a command link to each of the SDRAM modules 11 a . . . 11 n which includes a clock signal CCLK on inverted and non-inverted clock signal paths, a 1 bit FLAG signal and a 10 bit command bus CAO-9. In addition, SDRAM input/output signals SO, SI are provided from memory controller 13 in daisy chain fashion to the SDRAM modules 11 a . . . 11 n. In addition, a bi-directional data bus DQO-17 is provided between memory controller 13 and each of the SDRAM modules 11 a . . . 11 n, as are bi-directional data clocks DCLKO and DCLKI. The clock DCLKO is used to strobe input/output data into and out of the SDRAM modules, a process for which the DCLKI signal path is also intermittently used.
--	---

Figure 4 of Johnson, and its detailed description, are also cited in the Petition, which also includes an annotated version of Figure 4 of Johnson [See Petition, 21-22]. Figure 4 of Johnson and its detailed description are also identical to Figure 2 of Johnson '696 and its detailed description, as shown in the table below.

Johnson (as annotated by Petitioner)	FIG. 4
Johnson '686	FIG. 2

Johnson	Johnson '686
[EX1004, 3:48-57] FIG. 4 illustrates a simplified relevant portion of one of the SLD RAM modules 11 a . . . 11 n. It includes a control logic	[EX2009, ¶[0024]-[0028]] [0024] FIG. 2 illustrates a simplified relevant portion of one of the SLD RAM modules

circuit 21, latches 23, 25, 49, 59, delay devices 27, 29, 31, 55, 57 which may be ring delay devices, buffers 35, 37, 39, 33, 45, 47, 51, 53, a delay lock loop 41, multiplexer 43, pipeline circuits 61, 63, SRAM input/ output circuits 65 and 67, and respective memory banks Bank0 and Bank1 69, 71. It should be noted that although two memory banks are illustrated in FIG. 4, this is just illustrative, as any number of memory banks can be used. Control logic circuit 21 receives and analyzes commands on the CA0-9 bus and controls the input/output (I/O) access operations of the memory banks 69, 71. The control logic circuit 21 also receives the FLAG signal, and the clock signals CCLK, DCLK. The signals on each of the command bus paths CA0-9 are passed through respective adjustable ring delay circuits 27 and into respective latches 23 where the signals are latched by a CCLK signal, as buffered by buffer 39, delayed by delay 31 and buffered by buffer 33. The signal CCLK also passes from buffer 39 into a delay lock loop circuit 41 which provides 16 clock signals into a multiplexer 43. The multiplexer provides 18 clock output signals through respective buffers 45 to 18 latches 49 which latch data output from the memory banks 69, 71. The output data from memory banks 69, 71 pass into SRAMS 65, 67 which act as I/O	11 a . . . 11 n. It includes a control logic circuit 21, latches 23, 25, 49, 59, delay devices 27, 29, 31, 55, 57 which may be ring delay devices, buffers 35, 37, 39, 33, 45, 47, 51, 53, a delay lock loop 41, multiplexer 43, pipeline circuits 61, 63, SRAM input/ output circuits 65 and 67, and respective memory banks Bank0 and Bank1 69, 71. It should be noted that although two memory banks are illustrated in FIG. 2, this is just illustrative, as any number of memory banks can be used. [0025] Control logic circuit 21 receives and analyzes commands on the CAO-9 bus and controls the input/output (I/O) access operations of the memory banks 69, 71. The control logic circuit 21 also receives the FLAG signal and the clock signal CCLK [0026] The signals on each of the command bus paths CAO- 9 are passed through respective adjustable ring delay circuits 27 and into respective latches 23 where the signals are latched by a CCLK signal, as buffered by buffer 39, delayed by delay 31 and buffered by buffer 33. [0027] The signal CCLK also passes from buffer 39 into a delay lock loop circuit 41 which provides 16 clock signals into a multiplexer 43. The multiplexer provides 18 clock output signals through respective buffers 45 to 18
--	--

buffers and pass through pipeline circuit 61 before being loaded into latches 49. The output data latched in latches 49 is provided to respective buffer amplifiers 47 and from there is passed back to memory controller 13 (FIG. 3) via data bus DQ. Data which is to be input to memory banks 69, 71 is supplied by memory controller 13 (FIG. 3) on the DQ data bus, is passed through gated buffers 51 through ring delays 57 on each path of the data bus, into latches 59, through pipeline circuit 63. From pipeline circuit 63, input data on the DQ bus passes into buffer SRAM 65, 67 and into a memory bank 69, 71.	latches 49 which latch data output from the memory banks 69, 71. The output data from memory banks 69, 71 pass into SRAMS 65, 67 which act as I/O buffers and pass through pipeline circuit 61 before being loaded into latches 49. The output data latched in latches 49 is provided to respective buffer amplifiers 47 and from there is passed back to memory controller 13 via data bus DQ. [0028] Data which is to be input to memory banks 69, 71 is supplied by memory controller 13 on the DQ data bus, is passed through gated buffers 51 through ring delays 57 on each path of the data bus, into latches 59, through pipeline circuit 63. From pipeline circuit 63, input data on the DQ bus passes into buffer SRAM 65, 67 and into a memory bank 69, 71.
---	--

Johnson 1:42-48 is cited as teaching “...a phase shift of the command signals...” and “...a phase shift of the data signals...” [See Petition, §X.A.]. *This text is identical to corresponding text in Johnson ’696 as shown in the table below.*

Johnson	Johnson ’686
[EX1004, 1:42-48] One of the several calibration procedures which is performed in current SLDRAM devices is a timing synchronization of clock signals CCLK (command clock signal) and DCLK (data clock signal) with data provided	[EX2009, ¶[0006]] [0006] One of the several calibration procedures which is performed in current SLDRAM devices is a timing synchronization of clock signals CCLK (command clock signal) and DCLK (data clock signal) with data provided

on an incoming command path CA and FLAG path (for the CCLK signal) and on the data paths DQ (for the DCLK signal) so that incoming data is correctly sampled.	on incoming command paths CA and the FLAG path (for the CCLK signal) and on the data paths DQ (for the DCLK signal) so that incoming data is correctly sampled.
---	---

Johnson 7:52-57 is cited as teaching “...systematically altering...” [See Petition, 32] This text is similar to, and cumulative of, Johnson ’696 as shown in the table below.

Johnson	Johnson ’686
[EX1004, 7:52-57] As described above, the control logic circuit 21 steps through all possible delay values of ring delay 57 b, and notes those delays which produce a coincidence of the calibration pattern on data paths DQ<0> and DQ<1>, and selects a final delay value for delay 57 b which is at or near the center of acceptable delays.	[EX2009, ¶[0043]] [0043] ... As noted, in a preferred embodiment, the logic circuit 113 will actually control the ring delay such that it steps through all possible delay values with logic circuit 113 noting which of those delay values produced calibration of the data path. After all delay values have been stepped through, the logic circuit 113 will set as a final delay value for the ring delay, e.g. ring delay 29, the delay value which is at or near the middle of the range of delay values which produced signal path calibration.

Accordingly, with respect to Johnson, it is clear that with respect to *Advanced Bionics* Part 1, the Petition cites references that were substantially the same as

references previously presented to the United States Patent and Trademark Office (USPTO).

b. Jeddeloh

In Ground 1, Jeddeloh was a secondary reference cited as rendering Claims 1-14 of the '835 Patent obvious. However, Keeth '282 was cited by the Office and considered during prosecution of the '835 Patent. [See Supra, §2.C.] Keeth, cited in the Petition, substantially overlaps with both the text and figures of Keeth '282 [See Infra, §VII.C.1.b]. Jeddeloh was cited in the petition for the same purposes as Keeth. [Compare Petition, §X.A. with Petition, §X.B. 2].

An example of the correspondence between Jeddeloh and Keeth is illustrated in the table below:

Jeddeloh	Keeth
[Petition, 34-35] To the extent Patent Owner argues that Johnson does not teach and/or render obvious systematically altering a phase shift of sampling signals, Jeddeloh teaches this element. Ex-1002, ¶137. Jeddeloh discloses synchronizing “a data signal and a data strobe signal received from a random access memory.” Ex-1005, Abstract. A “second programmable delay circuit is configured to delay the data strobe signal so as to synchronize the data strobe signal with the data signal	[Petition, 74] To the extent Patent Owner argues that Johnson does not explicitly disclose or render obvious the recited “systematically altering [] a phase shift of the sampling signals,” Keeth teaches this element. Ex-1002, ¶239. Keeth discloses a similar memory system, which includes a command bus 28 “for carrying address and control information from memory controller 22 to the DRAM modules,” and a bi-directional data bus 32 for “carrying write data from memory controller 22 to

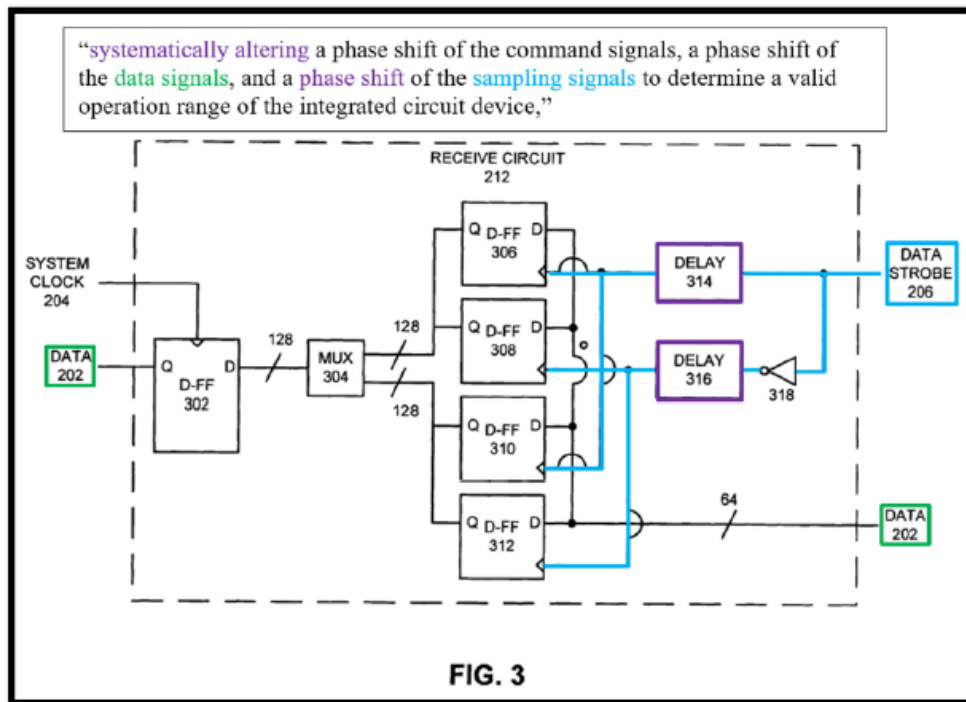
received from the random access memory.” Id. Jeddeloh’s data strobe signals are “sampling signals.” Ex-1002, ¶137.

Jeddeloh teaches a system that “selects a [] delay value in the middle of a valid range of [] delay values” by “performing test read operations using a plurality of different combinations of different [] delay values.” Ex-1005, 7:19-24; Abstract. Annotated Figure 3 below illustrates Jeddeloh’s delay of data strobe signals.

the DRAM modules and further carrying read data from the DRAM modules to memory controller 22.” Ex-1006, 3:44-56. A “free-running clock (CCLK) [is] provided on a clock line 30 from memory controller 22” (the recited “sampling signals”) and two bi-directional data clocks DCLK0 and DCLK1 (the recited “sampling signals”) “are respectively provided on clock line 34 and clock line 36.” Id.; Ex-1002, ¶241. Annotated Figure 1 below illustrates the sampling signals (blue) and the data signals (green).

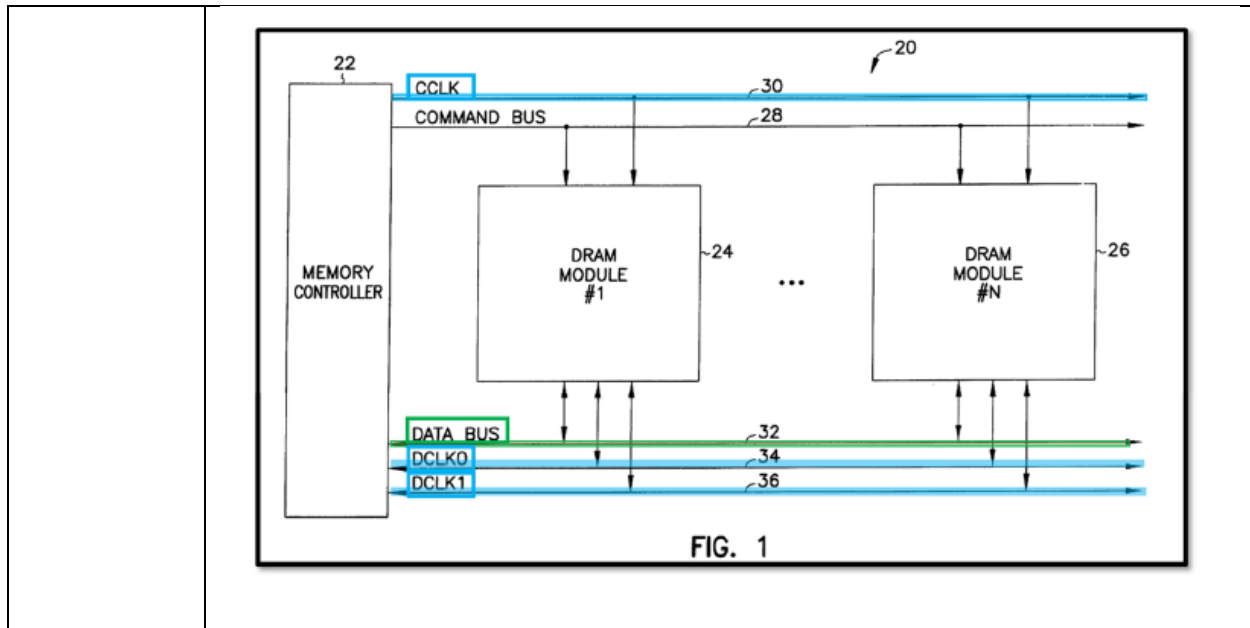
Jeddeloh

[Petition, 35]



Keeth

[Petition, 75]



As shown here, both Jeddelloh and Keeth were argued to teach “systematically altering a phase shift of sampling signals” in the Petition. [See Petition, 34-37 and 74-81]. The cited portions of both Jeddelloh and Keeth purport to include sampling signals for capture of a data line. Keeth ’282, considered by the Office, includes the same portions as Keeth. [See *Infra*, §VII.C.1.b.]. Accordingly, Jeddelloh discloses substantially the same information as Keeth ’282, which was considered by the Office. Thus, Jeddelloh is duplicative and/or cumulative with Keeth ’282, and accordingly, with respect to Jeddelloh, it is clear that with respect to *Advanced Bionics* Part 1, the Petition cites references that were substantially the same as references previously presented to the United States Patent and Trademark Office (USPTO).

2. Part 2 Of The *Advanced Bionics* Framework Is Met For Ground 1

To satisfy *Advanced Bionics* Part 2, the burden is on the Petitioner to demonstrate that the Office erred in a manner material to the patentability of the challenged claims. *See Advanced Bionics*, Paper 8, at 20-23; *Weatherford*, Paper 19, at 19-21. The Board in *Advanced Bionics* stressed the significance of the Petitioner's burden in this regard. As the Board stated in *Advanced Bionics*:

If a condition in the first part of the framework is satisfied and the petitioner fails to make a showing of material error, ***the Director generally will exercise discretion not to institute inter partes review. If reasonable minds can disagree regarding the purported treatment of the art or arguments, it cannot be said that the Office erred in a manner material to patentability.*** At bottom, this framework reflects a commitment to defer to previous Office evaluations of the evidence of record unless material error is shown

Advanced Bionics, Paper 6 at 8-9 (emphasis added).

Regarding alleged material error with respect to Johnson and Jeddeloh, the Petition makes a single, omnibus statement that “the Examiner must have necessarily overlooked invalidating disclosures of the art that was examined, constituting material error. *Advanced Bionics*, IPR 2019-01469, Paper 6, 10 (listing silence as evidence of error and stating *Becton Dickinson* ‘factors (c), (e), and (f) relate to whether the petitioner has demonstrated a material error by the Office’). As stated above in detail, Johnson in combination with Jeddeloh and/or Keeth teaches every

element of the Challenged Claims and renders the Challenged Claims obvious. To the extent any reference that was examined could be considered cumulative of these prior art references, the Examiner should have rejected the Challenged Claims at least under §103 and maintained the rejections(s).” [See Petition, 87].

This statement by Petitioner fails to demonstrate that the Office erred in a manner material to the patentability of challenged claims as required by *Advanced Bionics*. According to BD factor (e), for example, "Petitioner must demonstrate that the Examiner erred in the evaluation of the prior art, for example, by showing that the Examiner misapprehended or overlooked specific teachings in the relevant prior art such that the error by the Office was material to the patentability of the challenged claims." [See *Supra*, §VII.A.]

Instead, Petitioner offers what amounts to a conclusory statement that the Examiner erred because he did not reject the claims. However it is fundamental that “conclusory expert testimony and attorney argument cannot constitute substantial evidence.” *Acoustic Tech., Inc. v. Itron Networked Sols., Inc.*, 949 F.3d 1366, 1375 (Fed. Cir. 2020).

Accordingly, for Ground 1, it is clear that with respect to *Advanced Bionics* Part 2, the Petitioner has failed to demonstrate that the Office erred in a manner material to the patentability of the challenged claims.

C. Inter Partes Review Should Not Be Instituted For Ground 2, because the Advanced Bionics Framework is met.

Ground 2 of the Petition alleges that 1-3, 7-8, and 12 of the '835 Patent are obvious over Johnson in combination with Keeth. [See Petition §X.B.1].

1. Part 1 Of The *Advanced Bionics* Framework Is Met For Ground 2

To satisfy *Advanced Bionics* Part 1, the Patent Owner needs only to show that the Petition cites references that were substantially the same as references previously presented to the United States Patent and Trademark Office (USPTO). [See Supra §VII.B.1].

PO respectfully notes that both Johnson and Keeth are indeed duplicative and/or cumulative of references considered by the Office during prosecution of the '835 Patent, as follows.

a. Johnson

In Ground 2, the Petition adopts its application of Johnson set forth regarding Ground 1. [See Petition, 73]. As discussed regarding Ground 1, Johnson '696 was cited during prosecution of the '835 Patent, and Johnson '696 substantially overlaps the text of Johnson, and accordingly is cumulative of art cited in the Petition with respect to Ground 2 also. [See Supra, §VII.B.1.a]

b. Keeth

In Ground 2, the Petition cites Keeth as teaching “...systematically altering [] a phase shift of the sampling signals...” as in claim 1. [See Petition, 74-81].

With respect to both Johnson and Keeth, regarding the issue of whether “the same or substantially the same” art or arguments were previously presented to the Office during prosecution of the Challenged Claims, the Petition makes a single, incorrect, conclusory, and omnibus statement that “Johnson, Jeddeloh and Keeth ... are ... not substantially the same or cumulative of references considered during examination. [See Petition, 86].

With respect to Keeth specifically, the Petition makes only one other statement, that “[t]o the extent Patent Owner argues that Keeth is cumulative of US 6,016,282 (“Keeth ’282”), Keeth ’282 was never considered by the Office for its disclosure of “systematically altering [] a phase shift of the sampling signals...” and “...was only considered for its disclosure of “coarse delay adjustments” and “fine delay adjustments...” [See Petition, 86-87].

Petitioner appears to imply that for Keeth ’282 to correspond to the same art, or cumulative art having been cited during prosecution for purposes of the *Advanced Bionics* framework, it would need to have been directly applied to the same claim elements during prosecution as in the Petition.

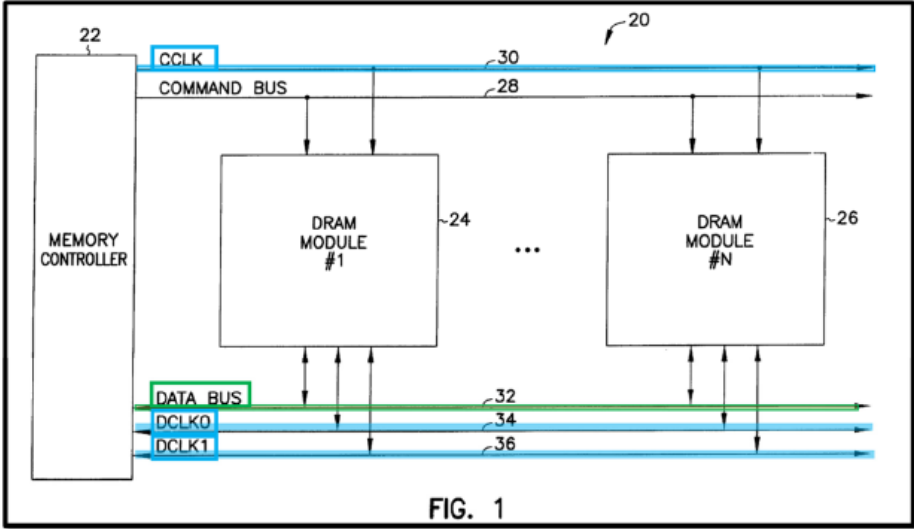
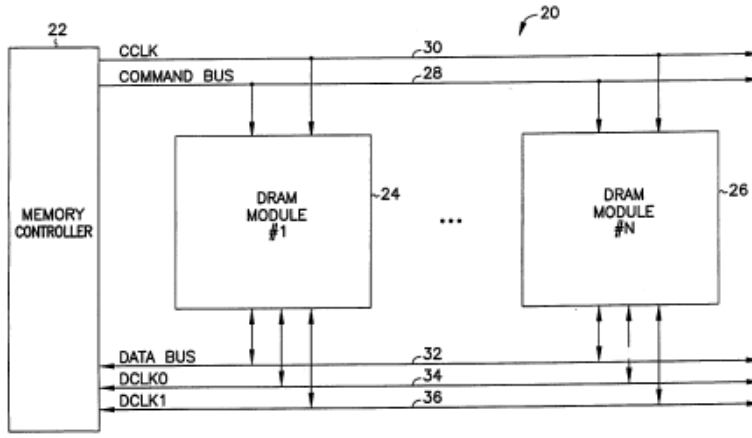
PO respectfully notes however that for Part 1 of the *Advanced Bionics* framework, if the “same or substantially the same prior art or arguments were previously provided to the Office,” then the Board’s decisions generally have required a showing that the Office erred in evaluating the art or arguments. [See *Advanced Bionics*, Paper 7 at 8 (emphasis added)]. Petitioner has made essentially no argument, apart from the omnibus argument above, that the “same or substantially the same prior art ... [was not] previously provided to the Office with respect to Keeth and Keeth ’282. [See *Id.* (emphasis added)].

Nor could Petitioner make such an argument, since the specifications of Keeth and Keeth ’282, which was expressly considered by the Office and over which the Challenged Claims were allowed, are virtually identical.

Keeth ’282 was also cited during prosecution of the ’835 Patent. [See *Infra*]. The specification of the entire specification of Keeth ’282 is virtually identical to the entire specification Keeth, and accordingly is both duplicative, and cumulative, of art cited in the Petition. [Compare EX1006 with EX2005].

For example, Figure 1 of Keeth and its detailed description are heavily cited in the Petition, which includes an annotated version of Figure 1 that “illustrates the sampling signals (blue) and the data signals (green).” [See Petition, 74-75]. Figure 1

of Keeth and its detailed description are identical to Figure 1 of Keeth '282 and its detailed description, as shown in the tables below. [Compare EX1006 with EX2005].

Keeth (as annotated by Petitioner)	 FIG. 1
Keeth '282	 FIG. 1

Keeth	Keeth '282
[EX1006, 3:38-56]	[EX2005, 3:38-56]
Overview of Memory Systems	Overview of Memory Systems

A memory system is illustrated generally at 20 in FIG. 1. Memory system 20 includes a memory controller 22 and N DRAM modules such as indicated at 24 and 26. The DRAM modules, such as modules 24 and 26, each comprise at least one DRAM device. A command bus 28 is an unidirectional bus for carrying address and control information from memory controller 22 to the DRAM modules. Address and control information is typically transferred from memory controller 22 on command bus 28 in uniform packets. For example, if a packet is four times the width of command bus 28, a command packet is transferred in four cycles on each edge of a free-running clock (CCLK) provided on a clock line 30 from memory controller 22. A data bus 32 is a bidirectional bus carrying write data from memory controller 22 to the DRAM modules and further carrying read data from the DRAM modules to memory controller 22. Two bidirectional data clocks, DCLK0 and DCLK1, are respectively provided on clock line 34 and clock line 36.	A memory system is illustrated generally at 20 in FIG. 1. Memory system 20 includes a memory controller 22 and N DRAM modules such as indicated at 24 and 26. The DRAM modules, such as modules 24 and 26, each comprise at least one DRAM device. A command bus 28 is an unidirectional bus for carrying address and control information from memory controller 22 to the DRAM modules. Address and control information is typically transferred from memory controller 22 on command bus 28 in uniform packets. For example, if a packet is four times the width of command bus 28, a command packet is transferred in four cycles on each edge of a free-running clock (CCLK) provided on a clock line 30 from memory controller 22. A data bus 32 is a bidirectional bus carrying write data from memory controller 22 to the DRAM modules and further carrying read data from the DRAM modules to memory controller 22. Two bidirectional data clocks, DCLK0 and DCLK1, are respectively provided on clock line 34 and clock line 36.
---	---

Figure 7 of Keeth and its detailed description, were also heavily cited in the Petition, which includes an annotated version of Figure 7 that “shows the vernier clock adjustment circuits 70 and 74 and corresponding CCLK signals.” [See Petition, 78-79]. Figure 7 of Keeth and its detailed description are identical to Figure 7 of

Keeth '282 and its detailed description, as shown in the tables below. [Compare EX1006 with EX2005].

Keeth
(as
annotated
by
Petitioner)

Keeth '282

Keeth	Keeth '282
[EX1006, 6:54-7:3]	[EX2005, 6:51-67]

The vernier clock adjustment circuitry and other related circuitry of memory system 20 (or memory systems 120 and 220) is illustrated in block diagram form in FIG. 7. As illustrated in FIG. 7, memory controller 22 includes a command register 50 for providing commands to command bus 28 and a CCLK register 52 for providing the CCLK to clock line 30. A master clock is provided on a line 54 to registers 50 and 52. A write data register 56 is also clocked by the master clock on line 54 and provides write data to data bus 32. A read data register 58 receives read data from data bus 32 and receives its clock from an optional vernier clock adjustment circuit 60. Vernier clock adjustment circuit 60 receives the master clock from line 54 and the active one of the data clocks DCLK0 or DCLK1 via a register multiplexer 62, which receives DCLK0 and DCLK1 from clock lines 34 and 36.	The vernier clock adjustment circuitry and other related circuitry of memory system 20 (or memory systems 120 and 220) is illustrated in block diagram form in FIG. 7. As illustrated in FIG. 7, memory controller 22 includes a command register 50 for providing commands to command bus 28 and a CCLK register 52 for providing the CCLK to clock line 30. A master clock is provided on a line 54 to registers 50 and 52. A write data register 56 is also clocked by the master clock on line 54 and provides write data to data bus 32. A read data register 58 receives read data from data bus 32 and receives its clock from an optional vernier clock adjustment circuit 60. Vernier clock adjustment circuit 60 receives the master clock from line 54 and the active one of the data clocks DCLK0 or DCLK1 via a register multiplexer 62, which receives DCLK0 and DCLK1 from clock lines 34 and 36.
---	---

Accordingly, with respect to Keeth, it is clear that with respect to *Advanced Bionics* Part 1, the Petition cites references that were substantially the same as references previously presented to the United States Patent and Trademark Office (USPTO).

2. Part 2 Of The *Advanced Bionics* Framework Is Met For Ground 2

Petitioner did not address the consideration of Johnson '696, discussed above, during prosecution of the '835 Patent, and thus has failed to demonstrate that the Office erred in a manner material to the patentability of the challenged claims with respect to Johnson. [See Supra, §VII.B.2.].

Petitioner argues that “Keeth '282 was never considered by the Office for its disclosure of “systematically altering [] a phase shift of the sampling signals” and that Keeth '282 was only considered for its disclosure of “coarse delay adjustments” and “fine delay adjustments.” [See Petition, 87].

However, during prosecution, the USPTO issued a Notice of Allowance dated May 14, 2009, which allows all claims [See EX1003, 69], after Keeth '282 was cited by the Examiner. [See EX1003, 301]. Accordingly, it is clear that during prosecution the Examiner considered the Challenged Claims in view of both Keeth '282 and Johnson '696. [See EX1003, 69, 89-97, 216, 300. See Supra §2.C].

Accordingly, with respect to Ground 2, it is clear that with respect to *Advanced Bionics* Part 2, the Petitioner has failed to demonstrate that the Office erred in a manner material to the patentability of the challenged claims.

A. Inter Partes Review Should Not Be Instituted For Ground 3, because the *Advanced Bionics* Framework is met.

Ground 3 of the Petition alleges that Claims 4-6, 9-11, and 13-19 of the '835 Patent are obvious over Johnson in combination with Jeddeloh and Keeth. [See Petition §X.C.1].

1. Part 1 Of The *Advanced Bionics* Framework Is Met For Ground 3

Johnson, Jeddeloh, and Keeth, are all substantially the same or cumulative of references cited to uspto per above. [See Supra §B.1., C1.]. Accordingly, with respect to Ground 3, it is clear that with respect to *Advanced Bionics* Part 1, the Petition cites references that were substantially the same as references previously presented to the United States Patent and Trademark Office (USPTO).

2. Part 2 Of The *Advanced Bionics* Framework Is Met For Ground 3

The Petitioner did not establish that the USPTO erred in considering references duplicative or cumulative of Johnson, Jeddeloh, or Keeth, per above. [See Supra, §§VII.B.2 and VII.C.2.].

Accordingly, with respect to *Advanced Bionics* Part 2, the Petitioner has failed to demonstrate that the Office erred in a manner material to the patentability of the challenged claims.

VIII. CONCLUSION

For the above reasons, PO respectfully requests that the Board deny institution of the Petition.

Respectfully submitted,

Dated: November 27, 2024

By: /Brandon R. Theiss/
Brandon R. Theiss
Registration No. 70,507
Counsel for Patent Owner
Intellectual Ventures II LLC

CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Patent Owner Preliminary Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 13,955 words, excluding the parts of this Patent Owner's Preliminary Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Preliminary Response.

Respectfully submitted,

Dated: November 27, 2024

By: /Brandon R. Theiss/
Brandon R. Theiss
Registration No. 70,507
Counsel for Patent Owner
Intellectual Ventures II LLC

CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a copy of the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** was served via email (as consented to by counsel) on November 27, 2024 to lead and backup counsel of record for Petitioners as follows:

Dinesh Melwani
dmelwani@bomcip.com

Ankit Aggarwal
aaggarwal@bomcip.com

William Uhr
wuhr@bomcip.com

Bookoff McAndrews, PLLC
2000 Pennsylvania Avenue NW
Suite 4001
Washington, D.C. 20006
Service email: docketing@bomcip.com

Dated: November 27, 2024

By: /Brandon R. Theiss/
Brandon R. Theiss (Reg. No. 70,507)
Volpe Koenig
Counsel for Patent Owner
Intellectual Ventures II LLC